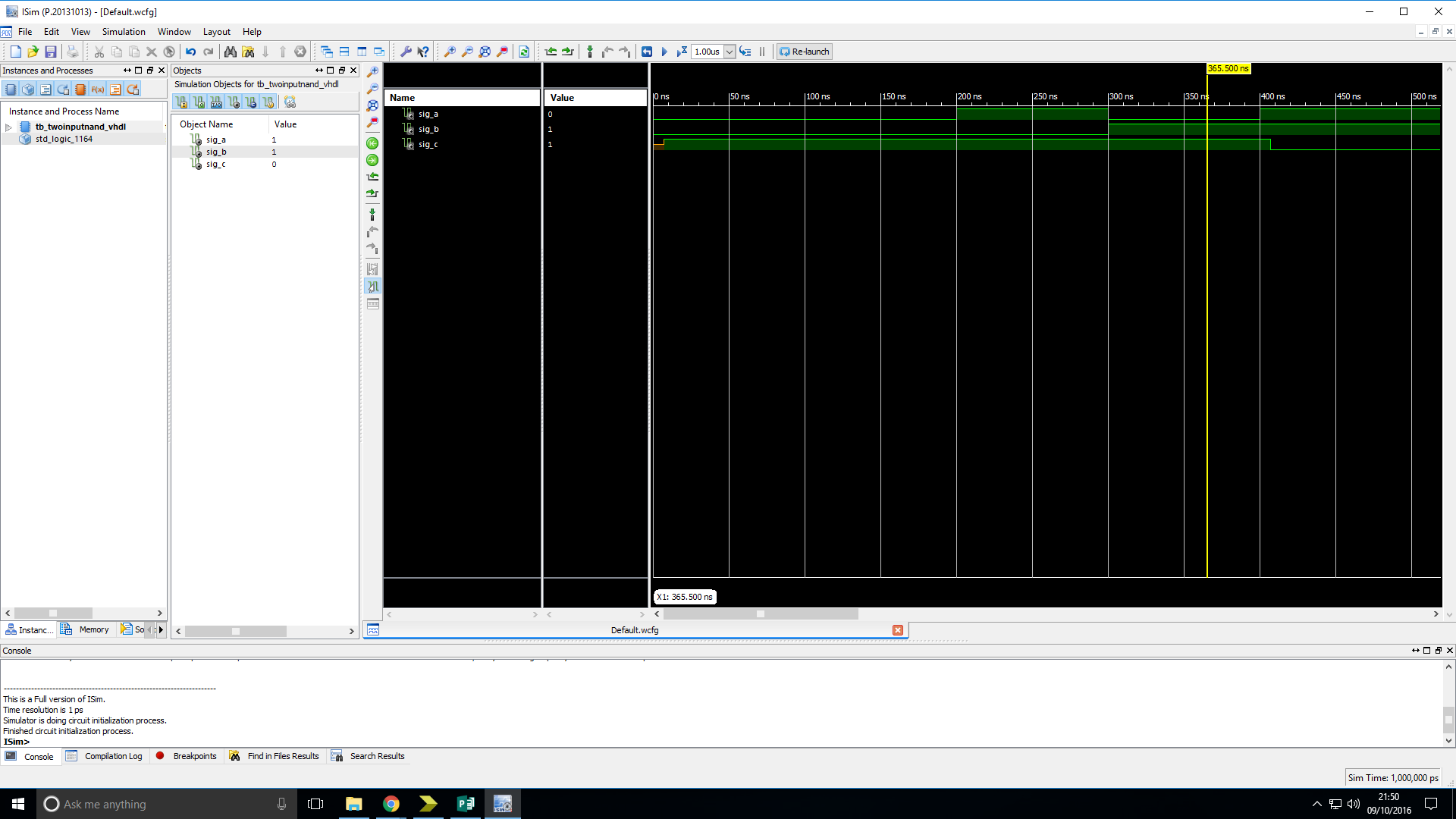


Figure: Simulation timing diagram of Inverter gate showing its behaviour when tested with all possible inputs.

Figure: Simulation timing diagram of the two-input NAND gate showing its behaviour when tested with all possible inputs.

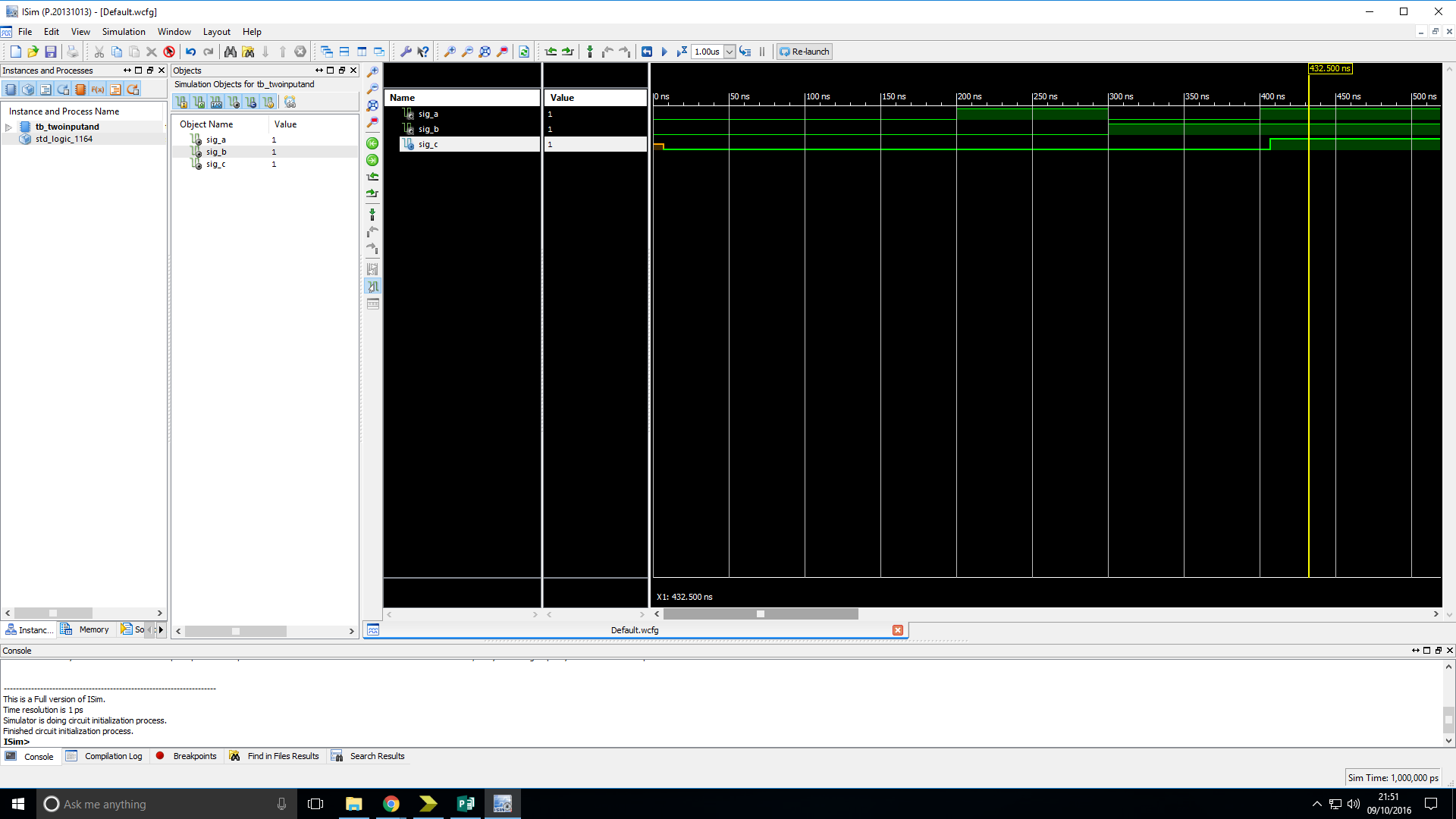


Figure: Simulation timing diagram of two-input AND gate showing its behaviour when tested with all possible inputs.

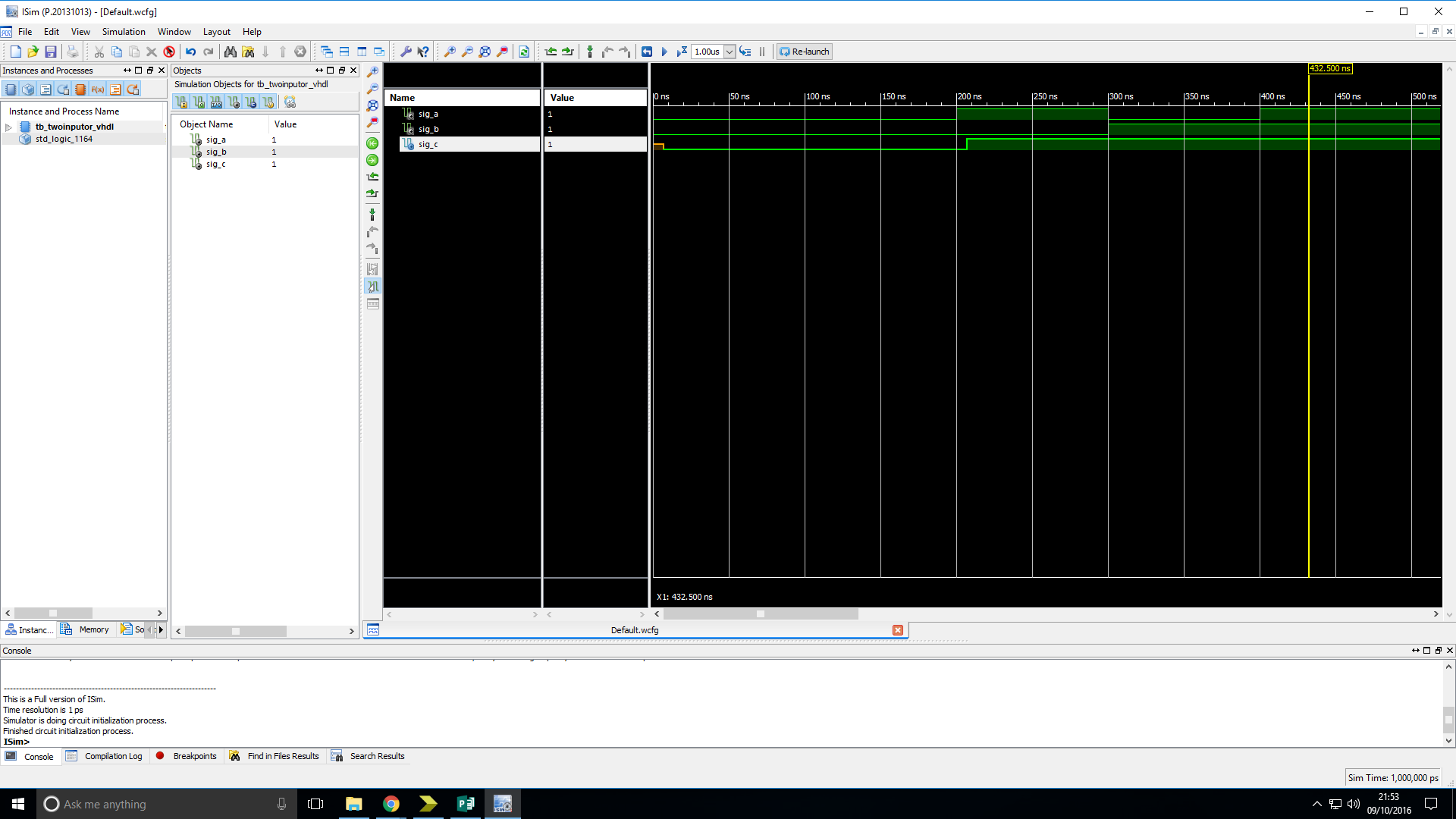


Figure: Simulation timing diagram of two-input OR gate showing its behaviour when tested with all possible inputs.

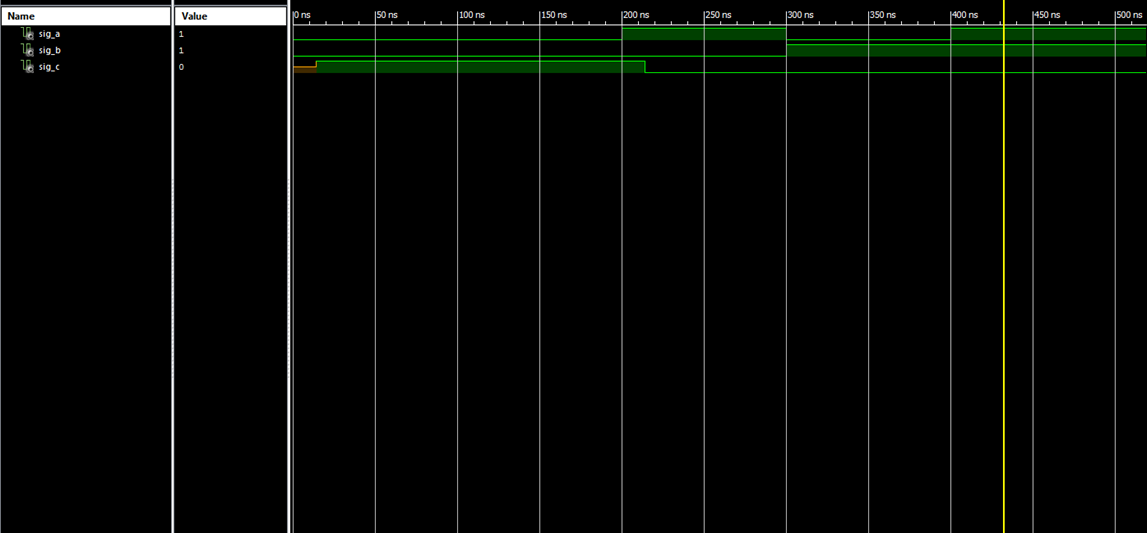


Figure: Simulation timing diagram of two-input XOR gate showing its behaviour when tested with all possible inputs.

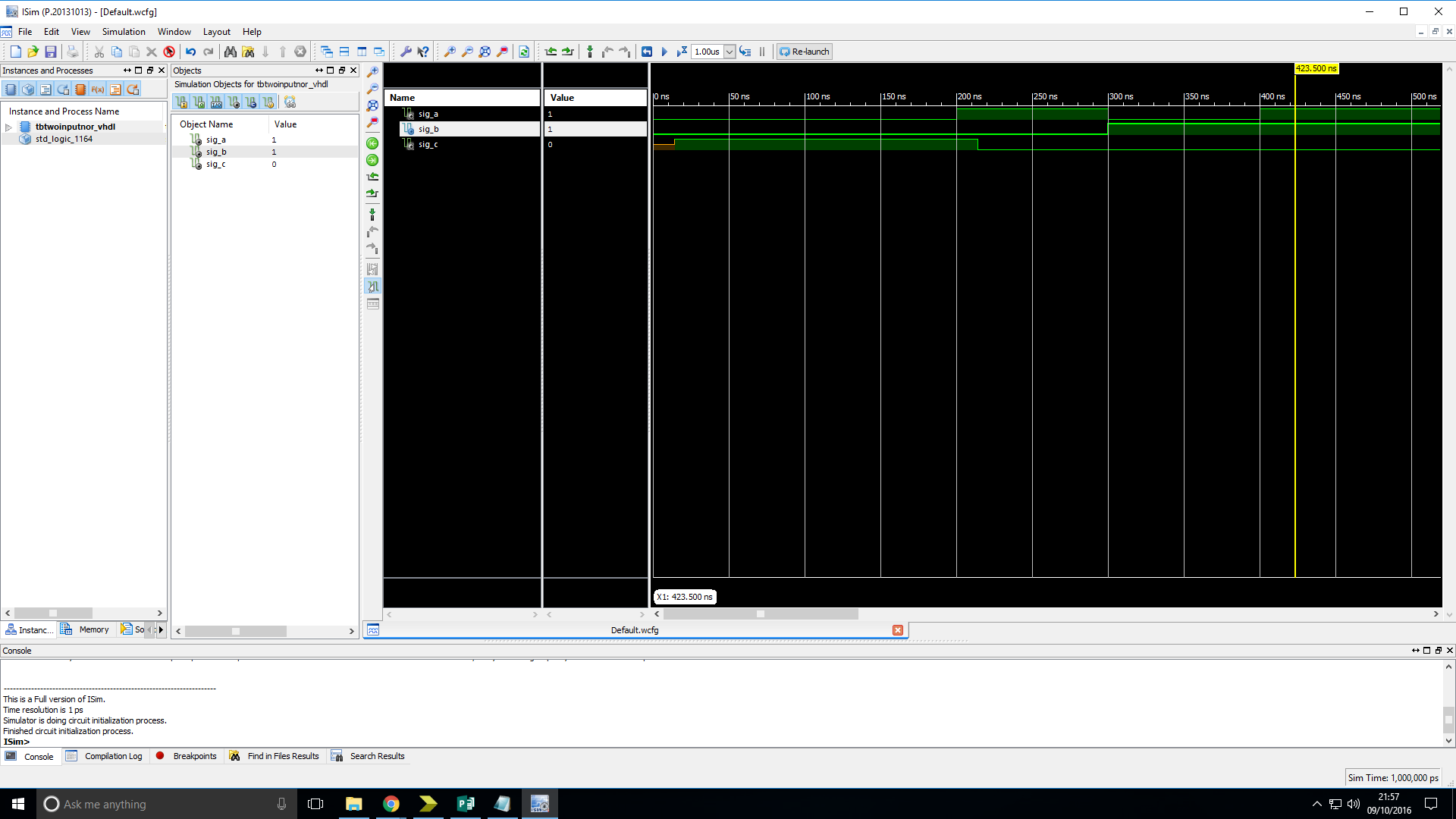


Figure: Simulation timing diagram of two-input NOR gate showing its behaviour when tested with all possible inputs.

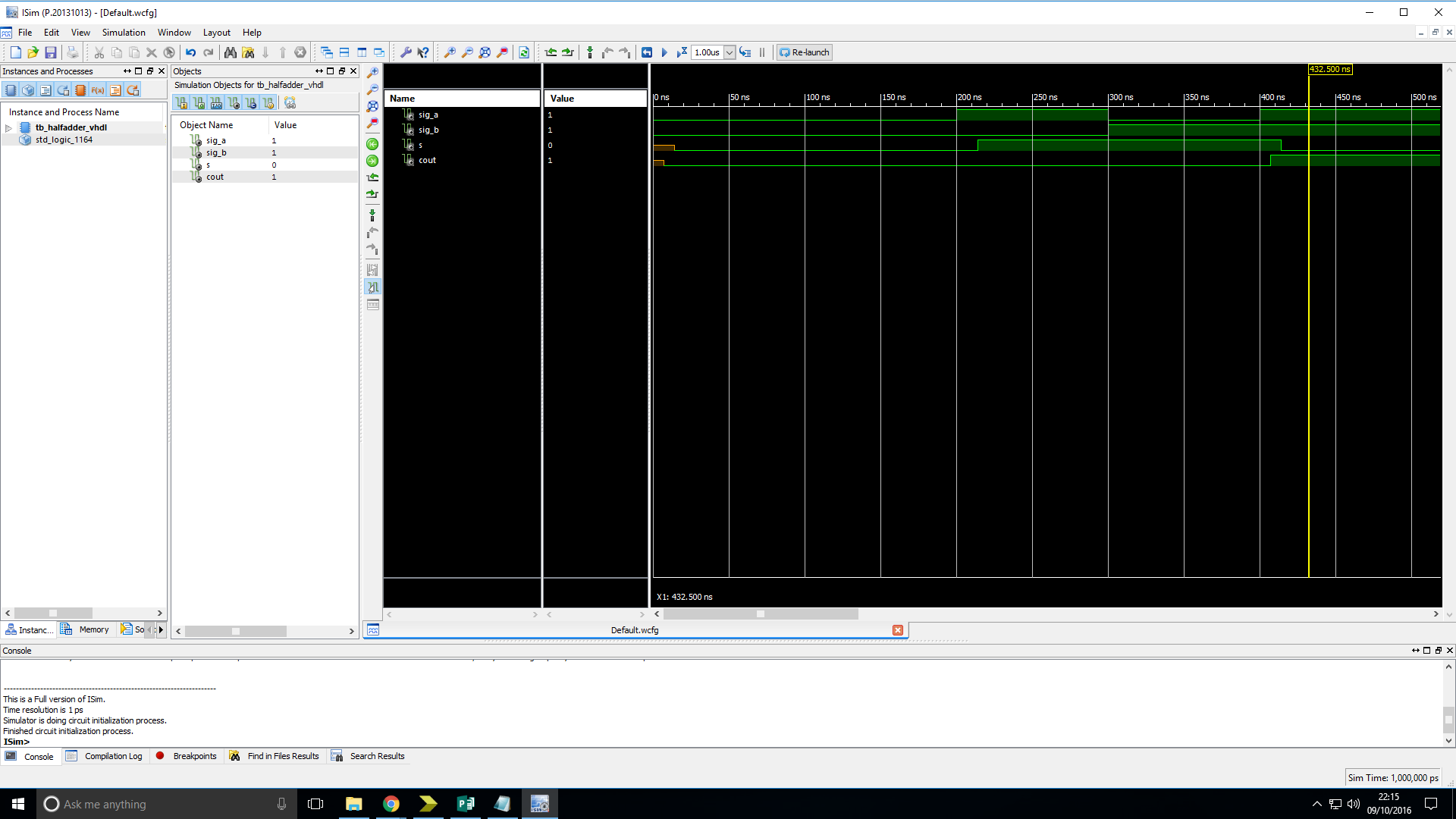


Figure: Simulation timing diagram of Half Adder showing its behaviour when tested with all possible inputs.

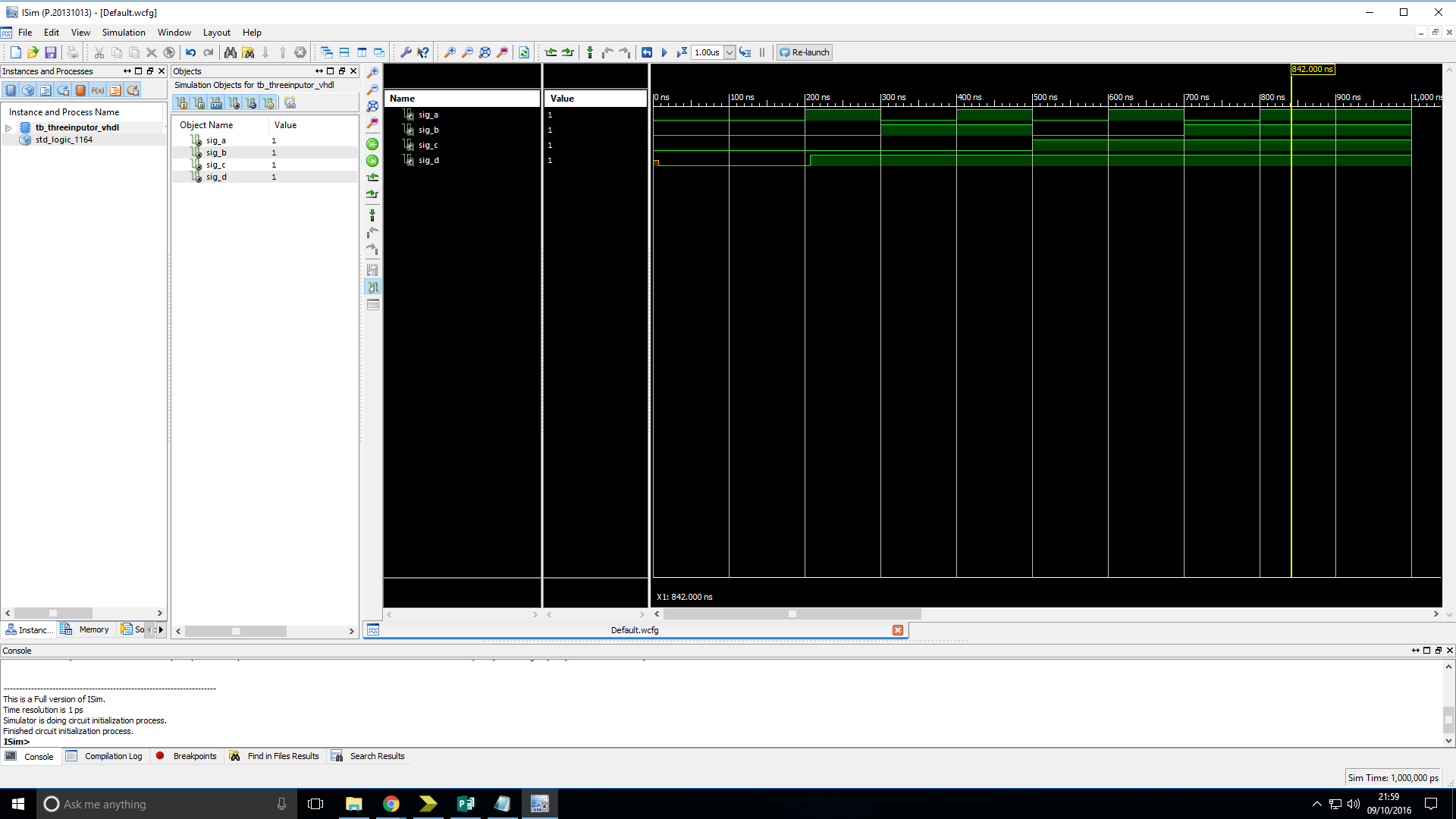


Figure: Simulation timing diagram of three-input OR gate showing its behaviour when tested with all possible inputs.

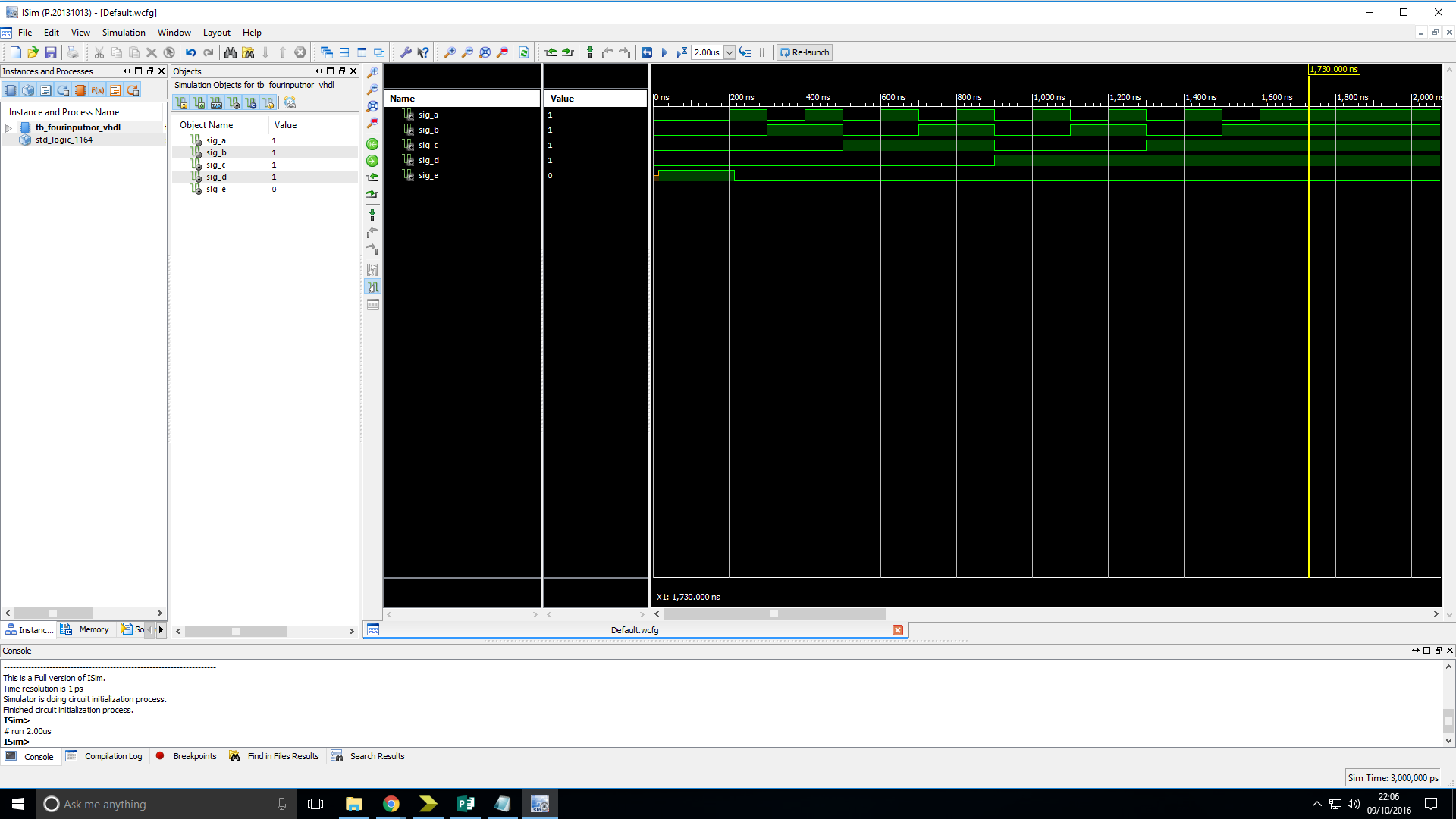


Figure: Simulation timing diagram of four-input NOR gate showing its behaviour when tested with all possible inputs.

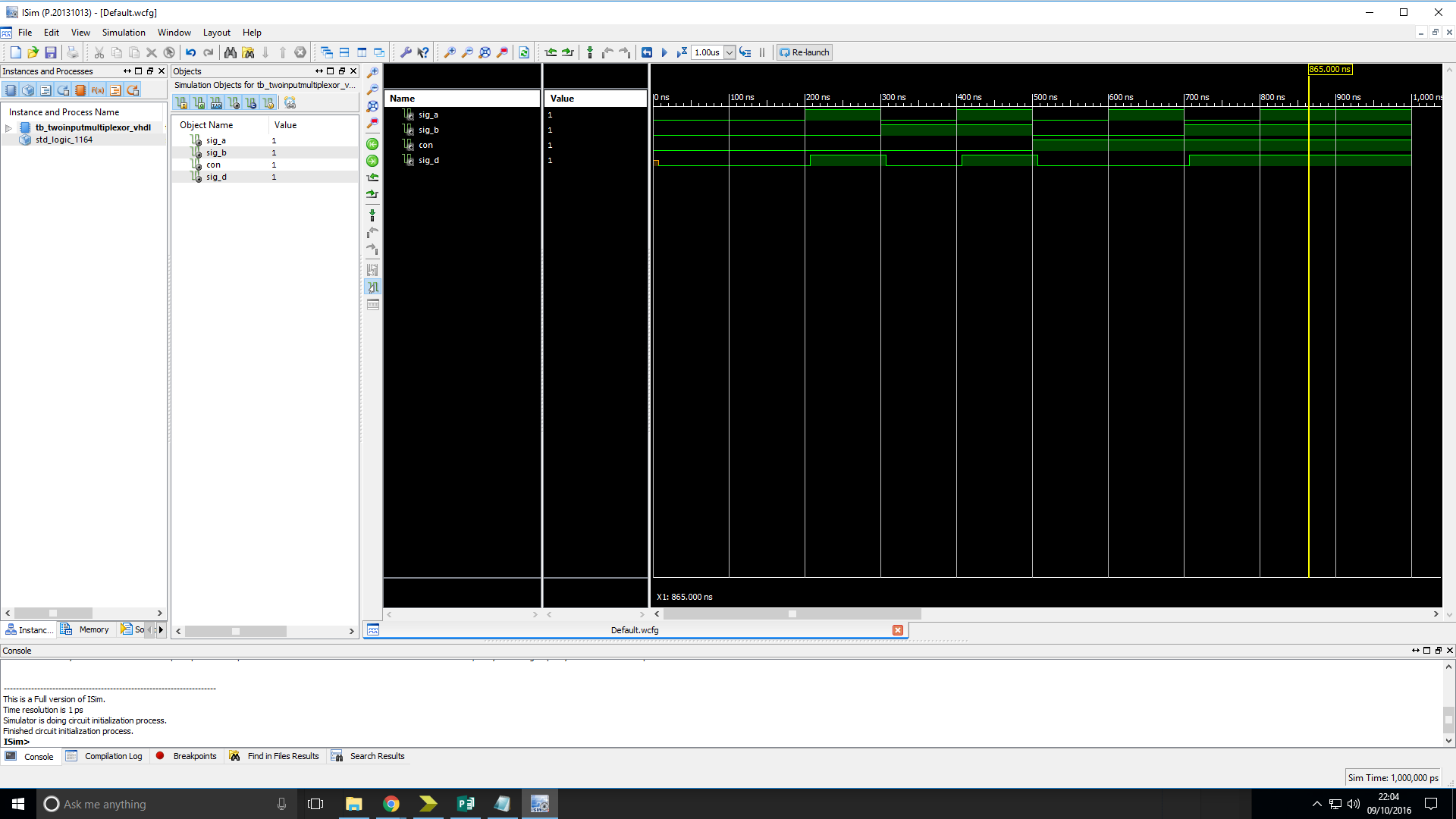


Figure: Timing diagram of two-input Multiplexer showing its behaviour when tested with all possible inputs.

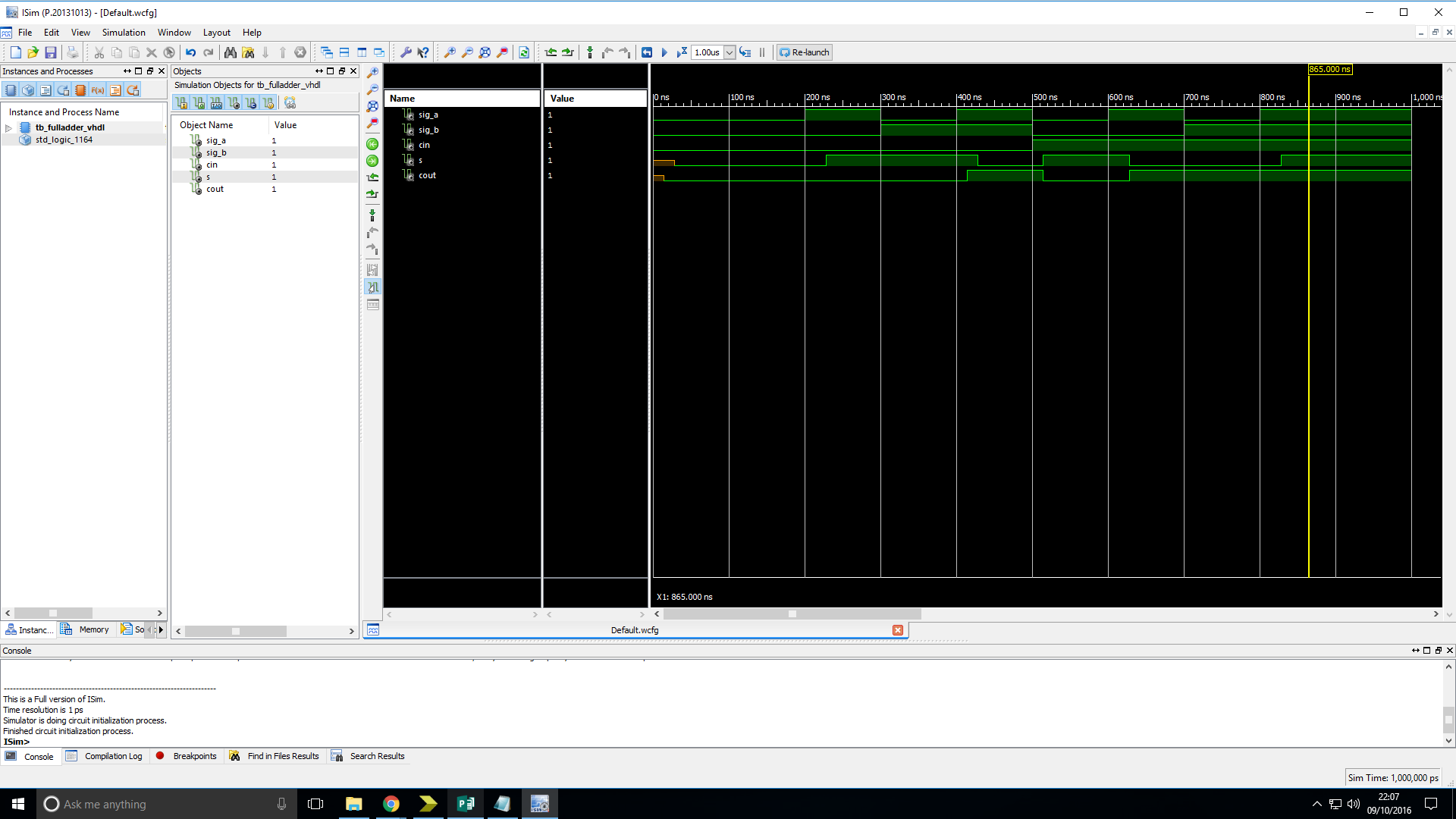


Figure: Timing diagram of Full Adder showing its behaviour when tested with all possible inputs.