**Lab 3- Hierarchy Design**

* n-bit register with LOAD/~HOLD and tristate output enable (nbit\_RegLH\_TriOut.vhd)
  + n-bit register with LOAD/~HOLD control (nbit\_RegLH.vhd)
    - n-bit 2-input multiplexer (lab 2) (nbitTwoInputMux\_VHDL.vhd)
      * Two-input mux (lab 1) (TwoInputMultiplexor\_VHDL.vhd)
    - n-bit register (nbitReg.vhd)
      * D-flipflop (dFlipFlop .vhd)
  + n-bit tri-state buffer (nbit\_triState.vhd)
    - tri-state buffer (code provided) (tri\_buff.vhd)

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* n-bit shift register with parallel load input (nbit\_ShiftReg\_ParalLoad.vhd)
  + n-bit 2-input multiplexer (lab 2) (nbitTwoInputMux\_VHDL.vhd)
    - Two-input mux (lab 1) (TwoInputMultiplexor\_VHDL.vhd)
  + n-bit register (nbitReg.vhd)
    - D-flipflop (dFlipFlop .vhd)
* 4-bit linear feedback shift register (4bit\_linearFeedback\_shiftReg.vhd)
  + XOR\_gate (lab 1) (TwoInputXOR\_VHDL.vhd)
  + n-bit shift-register (code provided) (nbit\_shiftreg.vhd)
    - n-bit register (nbitReg.vhd)
      * D-flipflop (dFlipFlop .vhd)
* n-bit Universal shift register (nbit\_Uni\_shiftReg.vhd)
  + Shift-Rotate Unit (lab 2) (shift\_rotate.vhd)
    - Two-input mux (lab 1) (two\_input\_mux.vhd)
    - Four-input mux (lab 2) (four\_input\_mux.vhd)
  + n-bit register (nbitReg.vhd)
    - D-flipflop (dFlipFlop .vhd)
* n-bit twisted-ring counter (nbit\_twistRing\_count.vhd)
  + Not Gate (lab 1) (Inverter\_VHDL.vhd)
  + n-bit shift-register (code provided) (nbit\_shiftreg.vhd)