**Lab 6- Hierarchy Design**

* **Microprogram-controlled Datapath** 
  + **Microprogrammed controller unit** 
    - **Control ROM**\*(alteration lab5))
    - State Counter (nbit\_syncCount\_parLoad.vhd)
      * N-bit incrementer (nbit\_incrementor.vhd)
        + Half-adder (lab 1) (HalfAdder\_VHDL.vhd)

Two input AND (lab 1) (TwoInputAND\_VHDL.vhd)

Two input XOR (lab 1) (TwoInputXOR\_VHDL.vhd)

* + - * N-bit 2 input MUX (lab 2) (nbitTwoInputMux\_VHDL.vhd)
        + Two input MUX (lab1) (TwoInputMultiplexor\_VHDL.vhd)
      * N-bit register (lab 3) (nbitReg.vhd)
        + D-flip flop (dFlipFlop.vhd)
    - **Function Decode logic**
    - Condition multiplexer (four-input mux)(lab2)
  + **Data path unit** 
    - Register File
      * 3 X 8 decoder
      * 8 x n-bit Register File (eight\_by\_nbit\_regFile.vhd
        + n-bit RFC register (nbit\_RFC\_reg.vhd)

Register File Cell (RFC) (reg\_fileCell.vhd)

2-input mux (lab1) (TwoInputMultiplexor\_VHDL.vhd)

D flip-flop (lab3) (dFlipFlop.vhd)

Tri-state buffer (lab3) (tri\_buff.vhd)

* + - ~~Combinational unit~~ 
      * ALU (lab2)
        + Arithmetic Unit

Four-bit two-input mux

Two-input mux (from lab 1)

Four-bit Adder/Subtractor

Four-bit XOR control

XOR gate (lab 1)

Four-bit LAC adder

Four-bit LAC

n-bit Adder

Full Adder (lab 1)

* + - * Shifter (lab2)
        + Shift-Rotate Unit

Two-input mux (from lab 1)

Four-input mux

* + - * + Shift control logic
      * Output buffer (n-bit load/hold register tri out) (nbit\_RegLH\_TriOut.vhd)
        + n-bit register with LOAD/~HOLD control (nbit\_RegLH.vhd)

n-bit 2-input multiplexer (lab 2) (nbitTwoInputMux\_VHDL.vhd)

Two-input mux (lab 1) (TwoInputMultiplexor\_VHDL.vhd)

n-bit register (nbitReg.vhd)

D-flipflop (dFlipFlop .vhd)

* + - * + n-bit tri-state buffer (nbit\_triState.vhd)

tri-state buffer (code provided) (tri\_buff.vhd)

* + - * Input multiplexer (n-bit two-input mux)

Two-input mux (from lab 1)

* + - * **Status logic (statusLogic.vhd)**