**Lab 4- Hierarchy Design**

* n-bit asynchronous (ripple) counter (to be made) **(nbit\_asynRipCount)**
  + T-Flip-flop (provided Lab 3) (T\_flipflop.vhd)
* 4-bit synchronous counter (to be made) **(4bit\_syncCount.vhd)**
  + Next state logic (sub component) **(count\_nextStateLog.vhd)**
  + 4-bit register (lab 3) (nbitReg.vhd)
    - D-flip flop (dFlipFlop.vhd)
* 4-bit synchronous up/down counter (to be made) **(4bit\_syncUpDown\_count.vhd)**
  + 4-bit adder/subtractor (lab 2) (fourbitAdderSubtractor\_VHDL.vhd)
    - Four-bit XOR control (nbit\_xor\_contol.vhd)
      * XOR gate (from lab 1) (TwoInputXOR\_VHDL.vhd)
    - Four-bit LAC adder (four\_bit\_LAC.vhd)
      * Four-bit LAC (FourBitLACAdder\_VHDL.vhd)
      * n-bit Adder (nbit\_Adder\_VHDL.vhd)
        + Full Adder (FullAdder\_VHDL.vhd)
  + N-bit register (lab 3) (nbitReg.vhd)
    - D-flip flop (dFlipFlop.vhd)
* Modulo-m counter with asynchronous reset (to be made) **(modm\_countAsynRes.vhd)**
  + 8-bit comparator (to be made) **(eightbit\_comparator.vhd)**
  + OR gate (lab 1) (TwoInputOR\_VHDL.vhd)
  + N-bit synchronous counter with enable (provided) (nbit\_count\_enable.vhd)
    - N-bit incrementer (to be made) **(nbit\_incrementor.vhd)**
    - Half-adder (lab 1) (HalfAdder\_VHDL.vhd)
      * Two input AND (lab 1) (TwoInputAND\_VHDL.vhd)
      * Two input XOR (lab 1) (TwoInputXOR\_VHDL.vhd)
    - N-bit register (lab 3) (nbitReg.vhd)
      * D-flip flop (dFlipFlop.vhd)
* Modulo-m counter with synchronous reset (to be made) **(modm\_countSyncRes.vhd)**
  + 8-bit comparator (to be made) **(eightbit\_comparator.vhd)**
  + N-bit synchronous counter parallel load input(to be made)**(nbit\_syncCount\_parLoad.vhd)**
    - N-bit incrementer (to be made) **(nbit\_incrementor.vhd)**
      * Half-adder (lab 1) (HalfAdder\_VHDL.vhd)
        + Two input AND (lab 1) (TwoInputAND\_VHDL.vhd)
        + Two input XOR (lab 1) (TwoInputXOR\_VHDL.vhd)
    - N-bit 2 input MUX (lab 2) (nbitTwoInputMux\_VHDL.vhd)
      * Two input MUX (lab1) (TwoInputMultiplexor\_VHDL.vhd)
    - N-bit register (lab 3) (nbitReg.vhd)
      * D-flip flop (dFlipFlop.vhd)
* Clothes washer control state machine (provided) (washer\_controller.vhd)
  + 2 input MUX (lab 1) (TwoInputMultiplexor\_VHDL.vhd)
  + Next state logic (sub component) **(washer\_nextStateLog.vhd)**
  + N-bit register (lab 3) (nbitReg.vhd)
    - D-flip flop (dFlipFlop.vhd)
  + Output logic (sub component) **(washer\_outputLog.vhd)**