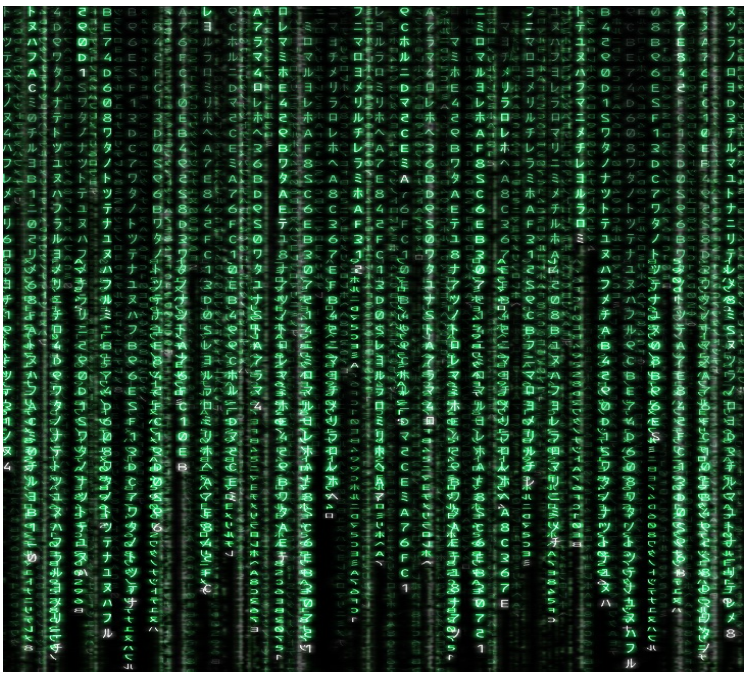

Digital Logic Design

[Circuit Design]

Digital Logic Design (DLD) is a fundamental subject for the engineering students worldwide. In application, it has built the foundation of modern electronic systems. It is established on binary code, a series of zeroes and ones where each value possesses an opposite meaning. However, the information conveyed throughout the electronic systems with logic gates. There are three basic logic gates generally used for circuit design, i.e., AND, OR and NOT (/Inverter). Well, many engineering students find it difficult to design the digital circuits properly while pursuing the DLD course in colleges or universities. Therefore, I will try to assist those students by sharing my lab works with them. Besides, for designing the circuits I have used the *Circuit Maker* software, but perhaps you can use some other tools such as the *Electronics Workbench* instead.

Pankaj Bhowmik
CS Graduate

List of Circuits

Now, I am going to share the list of circuits which I have designed thru my DLD lab course.

00. Design of Basic gates and with Universal gates i.e., AND, OR, NOT, NAND, NOR.
01. Design of a Half-Adder circuit.
02. Design of a Full-Adder circuit (with two Half-Adder with an additional OR gate).
03. Design of a Half-Subtractor circuit.
04. Design of a Full-Subtractor circuit (with two Half- Subtractor with an additional OR gate).
05. Convert a Full-Adder circuit to Full-Subtractor circuit.
06. Convert a Full-Subtractor circuit to Full-Adder circuit.
07. Code Conversion: Binary-to-Gray.
08. Code Conversion: Gray-to-Binary.
09. Code Conversion: Binary-to-2s' complement.
10. Code Conversion: BCD-to-Xcess-3.
11. Design of a Look-Ahead carry generator circuit.
12. Design of a 4-bit Full-Adder circuit with Look-Ahead carry generator.
13. Design of a 2-to-4 line Decoder (2x4) circuit.
14. Design of a 3-to-8 line Decoder (3x8) circuit.
15. Design of a 4x16 Decoder with two 3x8 Decoder using combinational IC.
16. Design of a Full-Adder circuit with 3x8 decoder.
17. Design of an Octal-to-Binary Encoder.
18. Design of a 4-to-1 line Multiplexer (4x1 MUX) circuit.
19. Design of a 8-to-1 line Multiplexer (8x1MUX) circuit.
20. Design of a 4x1 MUX circuit using Full-Adder Minterm {F(A,B,C)=sum(1,3,5,6)}.
21. Design of a Mode-5 Counter.
22. Design of a Mode-10 Counter.
23. Design of a Mode-13 Counter.
24. Design of a 5X32 Decoder with four 3X8 Decoder using combinational IC.
25. Design of a 0,1,2,3 Counter.
26. Design of a Binary Up Counter.
27. Design of a Binary Down Counter.
28. Design of a Binary Up-Down Counter.
29. Design of a Ripple Up Counter.
30. Design of a Ripple Down Counter.
31. Design of a BCD Ripple Counter.
32. Design of a Serial Input Serial Output (SISO) Shift-Register.
33. Design of a Serial Input Parallel Output (SIPO) Shift-Register.
34. Design of a Parallel Input Parallel Output (PIPO) Shift-Register.

A comprehensive analysis (block diagram, logic diagram, design procedure, workflow, truth table) of all these circuits are discussed in the book "***Digital Logic and Computer Design***" by ***M. MORRIS MANO***. One suggestion worth mentioning is that all these circuits are designed with logic gates, so the (.CKT) source files should be simulated on 'Digital Mode'.