Pinalkumar J. Engineer

CONTACT
INFORMATION

Assistant Professor
Department of Electronics Engineering
Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat
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RESEARCH
INTERESTS

Accelerated computing FPGA based system design, VLSI architecture for real-time signal/image processing, High performance embedded computing, Embedded and real-time systems.

CURRENT
ACADEMIC
APPOINTMENTS

Assistant Professor
Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat   January 2007 to present

PREVIOUS
ACADEMIC
APPOINTMENTS

Assistant Professor
Charusat University of Science & Technology   August 2003 to January 2007

Lecturer (Temporary)
M S University of Baroda   August 2001 to August 2003
Faculty of Technology & Engineering

EDUCATION

Ph.D.   2019
Indian Institute of Technology Bombay

M. E.(Microprocessor Systems & Applications)   2002
M S University of Baroda

B.E.(Instrumentation & Control Engineering)   1999
L D College of Engineering, Ahmedabad

REFEREED
JOURNAL
PUBLICATIONS

[J7] **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *Scalable implementation of particle filter-based visual object tracking on network-on-chip (NoC)*. Journal of Real-Time Image Processing, March-2019.

[J6] B Chandra Sekhar Naik, Anudeep J, Srinivas Lakavath and **Pinalkumar Engineer**. *FPGA Implementation of Earth Mover's Distance*. International Journal of Emerging Technology and Advanced Engineering, 4(6):June-2014.

[J5] Rahul V. Mehta, **Pinalkumar Engineer** and Milind S. Shah . *Multiple PicoBlazes-Review and Implementation*. International Journal of Emerging Technology and Advanced Engineering, 3(3):March-2013.

[J4] Sanjay Trivedi, B. S. Raman, **Pinalkumar Engineer** and Dr. Mihir Shah and . *Field Programmable Gate Array Based Control Signal Generator for Pulsed Radar*. International Journal of Embedded Systems and Applications (IJESA), 2(3): September 2012.

[J3] Rahul V. Shah, Amit Jain, Rutul B. Bhatt, **Pinalkumar Engineer** and Ekata Mehul. *Mean-Shift Algorithm: Verilog HDL Approach*. International Journal of Advanced Research in Computer and Communication Engineering, 1(2):78–85, April 2012.

[J2] Sanjay Trivedi, B. S. Raman, **Pinalkumar Engineer** and Dr. Mihir Shah. *Design of a Unified Timing Signal Generator (uTSG) for Pulsed Radar*. International Journal of Electronics and Communication Engineering & Technology (IJECET), 3(1): June 2012.

[J1] Dhaval Modi and Harsh Sitapara and Rahul V. Shah and Ekata Mehul and **Pinalkumar Engineer**. *Integrating MATLAB with verification HDLs for functional verification of image and video processing ASIC*. International Journal of Computer Science & Emerging Technologies, 2(2):258–265, 2011. http://www.ijcset.excelingtech.co.uk/vol2Issue2/09-vol2issue2.pdf

CONFERENCE
PUBLICATIONS

[C12] Syam Sanal, **Pinalkumar Engineer**. *Multithreaded Image Processing Using ReconOS on Reconfigurable Computing System*. In: International Conference on Emerging Trends and Innovations In Engineering And Technological Research (ICETIETR) 2018. doi:https://doi.org/10.1109/ICETIETR.2018.8529099

[C11] Dharmesh Patel, **Pinalkumar Engineer**. *Design and Implementation of Quasi Cyclic Low Density Parity Check (QC-LDPC) Code on FPGA*. In: International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET 2017), March 22 – 24, 2017. doi:http://ieeexplore.ieee.org/document/8299744/

[C10] Vinay B. Y. Kumar, **Pinalkumar Engineer**, Mandar Datar, Yatish Turakhia, Saurabh Agarwal, Sanket Diwale and Sachin B. Patkar. *Framework for Application Mapping over Packet-Switched Network of FPGAs: Case Studies*. In: Second International Workshop on FPGAs for Software Programmers (FSP 2015), September 1 – 4, 2015. doi:http://arxiv.org/abs/1508.06823

[C9] Anudeep J, B Chandra Sekhar Naik, and **Pinalkumar J Engineer**. *GPU Implementation of Earth Mover's Distance*. In: 3rd International Conference on Information Technology and Science (ICITS 2015) March 27-30, 2015.

[C8] **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *Parameterizable FPGA Framework for Particle Filter Based Object Tracking in Video*. In: 28th International Conference on VLSI Design, VLSID 2015, Bangalore, India, January 3-7, 2015. pp. 35–40. doi:10.1109/VLSID.2015.11

[C7] Sumeet Agrawal, **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *FPGA Implementation of particle filter based object tracking in video*. In: 3rd International Symposium on Electronic System Design (ISED), Kolkata, 19th-22nd December 2012. pp. 82–86. doi:10.1109/ISED.2012.41

[C6] Suraj Das, Atit Jariwala and **Pinalkumar Engineer**. *Modified architecture for real-time face detection using FPGA*. In: 3rd Nirma University International Conference on Engineering (Nuicone-2012), Nirma University, Ahmedabad, Dec 6-8,2012. pp. 1–5. doi:10.1109/NUICONE.2012.6493235

[C5] Suraj Das, Atit Jariwala and **Pinalkumar Engineer**. *FPGA based stream processing of edge and skin detection algorithms*. In: International Conference on Advanced Computing and Communication Technologies (ICACCT-2012) at Asia Pacific Institute of Information Technology SD India, Panipat (Haryana) on November 3,2012.

[C4] Rahul V. Shah, Amit Jain, Rutul B Bhatt, **Pinalkumar Engineer** and Ekata Mehul. *Mean-Shift Algorithm: Verilog HDL Approach*. In: Proceedings of the Third International Conference on Trends in Information, Telecommunication and Computing, 2013. pp 181-194. doi:10.1007/978-1-4614-3363-7_21

[C3] Dhaval Modi, Harsh Sitapara, Rahul Shah, Ekata Mehul, **Pinalkumar Engineer**. *Combining Power of MATLAB with SystemVerilog for Image and Video Processing ASIC Verification*. In: ADVANCES IN NETWORK SECURITY AND APPLICATIONS, Communications in Computer and Information Science series 2011, 196(1). pp 181-193. doi:10.1007/978-3-642-22540-6_19

[C2] Dhaval Modi, Harsh Sitapara, Rahul V Shah, Ekata Mehul, **Pinalkumar Engineer**. *Enhancing verification capability using system Verilog and Matlab",*. In: 2nd International conference on Signals, Systems and Automation (ICSSA-2011), January 2011. pp 513-516.

[C1] Hiren Mewada, Pinal K. Patel, **Pinalkumar Engineer**. *FPGA based implementation of computationally efficient Daubchies 9/7 DWT using Lifting scheme*. In: International Conference on Emerging Techniques in Electronics, Computing Embedded System & VLSI Design(ICEVD-2008) at Dr. VV Patil College of Engineering, Ahmednagar, March 20-21, 2008. pp 130.

CONFERENCE
POSTERS

[P1] **Pinalkumar Engineer**, Ayan Mishra, Rajbabu Velmurugan and Sachin B. Patkar. *GPU implementation of Particle Filter based Object Tracking*. In: GPU Technology Conference, GTC 2015, San Jose, California, USA, 2015. Poster abstract.

INDUSTRY
INTERACTIONS

[I4] **ARM Ltd.** Donation PSoC 4 BluetoothÂő Low Energy (BLE) 4.1 Compliant Pioneer Kits (10 Nos.) for Setting-up Embedded IoT Lab under ARM University program (July 19, 2018).

[I3] **ARM Ltd.** Donation of Keil uVision MDK-ARM version licenses (100 Nos.) for one year (November 23, 2017-November 22, 2018) under ARM University program.

[I2] **Amdocs** One team from SVNIT entered into Top 5 of Grand finale event of *Amdocs Innovation Lab-2017*.

[I1] **Freescale Semiconductor India Pvt. Ltd.** Two teams from SVNIT was a 1st place and 3rd place winners in Grand finale event of *Freescale Cup-2011*.

EXPERT
LECTURES

[E25] *IP integration*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 12, 2017

[E24] *RTL Synthesis*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 12, 2017

[E23] *Implementation using Vivado*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 11, 2017

[E22] *Introduction to Robotics*. at: Essar Technology Day, Essar Ltd, Hazira, September 13, 2017

[E21] *Inkscape*. in: STTP on Paper and Article Writing with LaTeX at Electronics Engineering Department, S V National Institute of Technology, Surat, January 24, 2017.

[E20] *Introduction to Parallel Computing*. in: One day Training under Industry defined research project under Newton-Bhabha Fund at Parul University, Vadodara, March 15, 2017.

[E19] *Introduction to Linux*. at: Electronics Engineering Department, Government College of Engineering, Valsad, October 15, 2016.

[E18] *Hardware/Software co-design for Embedded System design*. at: Electronics Engineering Department, Dr. S. S. Gandhi Government College of Engineering, Surat, September 29, 2016.

[E17] *Image processing using GPU*. in: STTP on Emerging Trends in Signal & Image Processing (ETSiP) at Electronics Engineering Department, S V National Institute of Technology, Surat, September 17, 2016.

[E16] *FreeRTOS*. at: V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa, February 13, 2015.

[E15] *Embedded Image processing using FPGAs*. at:GUJCOST Sponsored workshop on Software and Hardware Realization for Image & Video Processing and its Applications. V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa. January 29, 2015.

[E14] *Real-time Image processing using OpenCV and GPU*. at: GUJCOST Sponsored workshop on Software and Hardware Realization for Image & Video Processing and its Applications. V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa. January 29, 2015.

[E13] *Multithreading Programming using pThreads and CUDA*. at: TEQIP-II sponsored Workshop on High Performance Computing-Architectures and applications for Engineer and Scientists. SVNIT, Surat. January 25, 2015.

[E12] *Hardware & Software co-design for secure embedded systems*. at: C K Pithawala College of Engineering & Technology, Surat. August 30, 2015.

[E11] *Embedded System Design Methodology*. at: Mindbend. SVNIT, Surat. October 25, 2013.

[E10] *ARM processor Pin Functioning and Instruction Set*. at: STTP on Embedded System Design using Assembly and C Language. Institute of Diploma Studies, Nirma University. May 30, 2012.

[E9] *Introduction to PIC Microcontrollers*. at: STTP on Embedded System Design using Assembly and C Language. Institute of Diploma Studies, Nirma University. May 29, 2012.

[E8] *Design, Implementation & Modeling of Mixed Design Embedded Systems*. at: STTP on Advanced on Embedded Systems. RK University, Rajkot. December 20, 2011.

[E7] *Structural Modelling*. at: SMDP II Sponsored ISF Organised two day workshop on VHDL. ECED, SVNIT, SURAT. September 19, 2010.

[E6] *Use of Analog and Digital Oscilloscopes*. at: ISF(IETE), SVNIT. November 21, 2009.

[E5] *Hardware Description Languages*. at: National Workshop on VLSI Design tools sponsored by SMDP-II Project. ECED, SVNIT, SURAT. February 28- March 1, 2009.

[E4] *Introduction to HDL*. at: Faculty Development Program sponsored by TEQIP. ECED, SVNIT, SURAT. December 15-19, 2008.

[E3] *ARM 7 Core*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

[E2] *ARM Processors-Why ARM & Various Families*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

[E1] *ARM 7 Instruction Set*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

PROFESSIONAL **Conference Service**
SERVICE
- Local Organizing Committee: EAI International Conference on FUTURE INTERNET TECH-NOLOGIES AND TRENDS, 2017. August 31 - September 2 2017

- Local Organizing Committee: 2nd International Conference on Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2014. December 26-27, 2014

- Local Organizing Committee: 1st International Conference on Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2012. December 19-21, 2012

PROFESSIONAL
MEMBERSHIPS
- Institute of Electrical and Electronics Engineers (IEEE) (2009–present)
- The Institution of Electronics and Telecommunication Engineers (IETE) (2002–present)