CHAPTER 2

PIC18F Microcontroller Series

PIC16-series microcontrollers have been around for many years. Although these are excellent general purpose microcontrollers, they have certain limitations. For example, the program and data memory capacities are limited, the stack is small, and the interrupt structure is primitive, all interrupt sources sharing the same interrupt vector. PIC16-series microcontrollers also do not provide direct support for advanced peripheral interfaces such as USB, CAN bus, etc., and interfacing with such devices is not easy. The instruction set for these microcontrollers is also limited. For example, there are no multiplication or division instructions, and branching is rather simple, being a combination of *skip* and *goto* instructions.

Microchip Inc. has developed the PIC18 series of microcontrollers for use in high-pin-count, high-density, and complex applications. The PIC18F microcontrollers offer cost-efficient solutions for general purpose applications written in C that use a real-time operating system (RTOS) and require a complex communication protocol stack such as TCP/IP, CAN, USB, or ZigBee. PIC18F devices provide flash program memory in sizes from 8 to 128Kbytes and data memory from 256 to 4Kbytes, operating at a range of 2.0 to 5.0 volts, at speeds from DC to 40MHz.

The basic features of PIC18F-series microcontrollers are:

- 77 instructions
- PIC16 source code compatible
- Program memory addressing up to 2Mbytes
- Data memory addressing up to 4Kbytes

- DC to 40MHz operation
- 8 × 8 hardware multiplier
- Interrupt priority levels
- 16-bit-wide instructions, 8-bit-wide data path
- Up to two 8-bit timers/counters
- Up to three 16-bit timers/counters
- Up to four external interrupts
- High current (25mA) sink/source capability
- Up to five capture/compare/PWM modules
- Master synchronous serial port module (SPI and I^2C modes)
- Up to two USART modules
- Parallel slave port (PSP)
- Fast 10-bit analog-to-digital converter
- Programmable low-voltage detection (LVD) module
- Power-on reset (POR), power-up timer (PWRT), and oscillator start-up timer (OST)
- Watchdog timer (WDT) with on-chip RC oscillator
- In-circuit programming

In addition, some microcontrollers in the PIC18F family offer the following special features:

- Direct CAN 2.0 bus interface
- Direct USB 2.0 bus interface
- Direct LCD control interface
- TCP/IP interface
- ZigBee interface
- Direct motor control interface

Most devices in the PIC18F family are source compatible with each other. Table 2.1 gives the characteristics of some of the popular devices in this family. This chapter offers a detailed study of the PIC18FXX2 microcontrollers. The architectures of most of the other microcontrollers in the PIC18F family are similar.

The reader may be familiar with the programming and applications of the PIC16F series. Before going into the details of the PIC18F series, it is worthwhile to compare the features of the PIC18F series with those of the PIC16F series.

The following are similarities between PIC16F and PIC18F:

- Similar packages and pinouts
- Similar special function register (SFR) names and functions
- Similar peripheral devices

Table 2.1: The 18FXX2 microcontroller family

Feature	PIC18F242	PIC18F252	PIC18F442	PIC18F452
Program memory (Bytes)	16K	32K	16K	32K
Data memory (Bytes)	768	1536	768	1536
EEPROM (Bytes)	256	256	256	256
I/O Ports	A,B,C	A,B,C	A,B,C,D,E	A,B,C,D,E
Timers	4	4	4	4
Interrupt sources	17	17	18	18
Capture/compare/PWM	2	2	2	2
Serial communication	MSSP USART	MSSP USART	MSSP USART	MSSP USART
A/D converter (10-bit)	5 channels	5 channels	8 channels	8 channels
Low-voltage detect	yes	yes	yes	yes
Brown-out reset	yes	yes	yes	yes
Packages	28-pin DIP 28-pin SOIC	28-pin DIP 28-pin SOIC	40-pin DIP 44-pin PLCC 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin TQFP

- Subset of PIC18F instruction set
- Similar development tools

The following are new with the PIC18F series:

- Number of instructions doubled
- 16-bit instruction word
- Hardware 8 × 8 multiplier
- More external interrupts
- Priority-based interrupts
- Enhanced status register
- Increased program and data memory size
- Bigger stack
- Phase-locked loop (PLL) clock generator
- Enhanced input-output port architecture
- Set of configuration registers
- Higher speed of operation
- Lower power operation

2.1 PIC18FXX2 Architecture

As shown in Table 2.1, the PIC18FXX2 series consists of four devices. PIC18F2X2 microcontrollers are 28-pin devices, while PIC18F4X2 microcontrollers are 40-pin devices. The architectures of the two groups are almost identical except that the larger devices have more input-output ports and more A/D converter channels. In this section we shall be looking at the architecture of the PIC18F452 microcontroller in detail. The architectures of other standard PIC18F-series microcontrollers are similar, and the knowledge gained in this section should be enough to understand the operation of other PIC18F-series microcontrollers.

The pin configuration of the PIC18F452 microcontroller (DIP package) is shown in Figure 2.1. This is a 40-pin microcontroller housed in a DIL package, with a pin configuration similar to the popular PIC16F877.

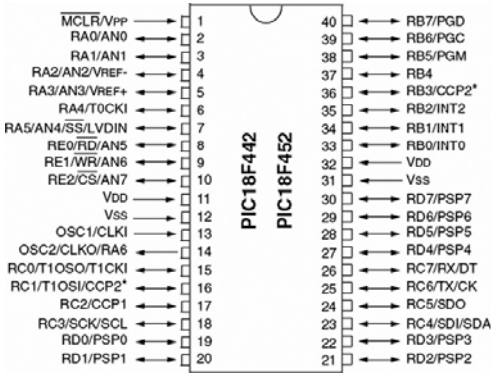


Figure 2.1: PIC18F452 microcontroller DIP pin configuration

Figure 2.2 shows the internal block diagram of the PIC18F452 microcontroller. The CPU is at the center of the diagram and consists of an 8-bit ALU, an 8-bit working accumulator register (WREG), and an 8 × 8 hardware multiplier. The higher byte and the lower byte of a multiplication are stored in two 8-bit registers called PRODH and PRODL respectively.

The program counter and program memory are shown in the upper left portion of the diagram. Program memory addresses consist of 21 bits, capable of accessing 2Mbytes of program memory locations. The PIC18F452 has only 32Kbytes of program memory, which requires only 15 bits. The remaining 6 address bits are redundant and not used. A table pointer provides access to tables and to the data stored in program memory. The program memory contains a 31-level stack which is normally used to store the interrupt and subroutine return addresses.

The data memory can be seen at the top center of the diagram. The data memory bus is 12 bits wide, capable of accessing 4Kbytes of data memory locations. As we shall see later, the data memory consists of special function registers (SFR) and general purpose registers, all organized in banks.

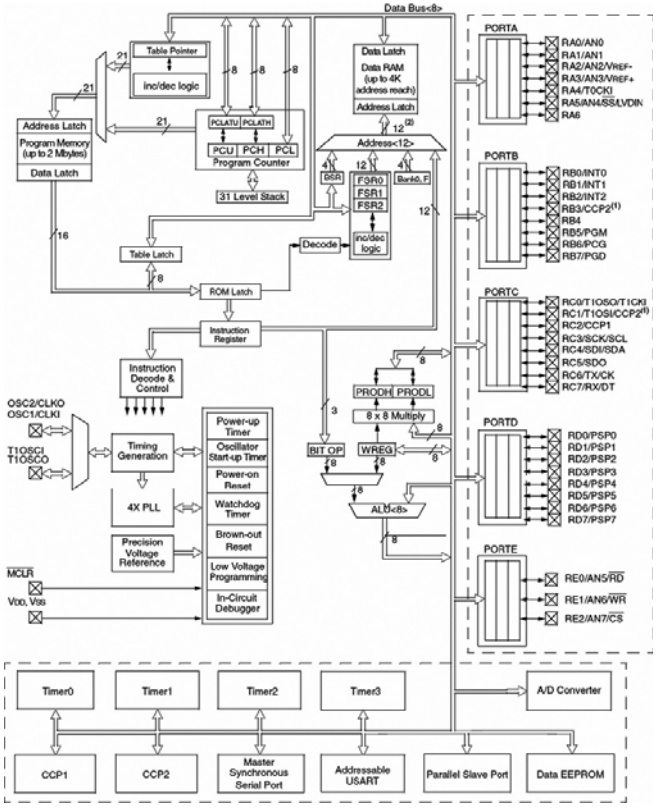


Figure 2.2: Block diagram of the PIC18F452 microcontroller

The bottom portion of the diagram shows the timers/counters, capture/compare/PWM registers, USART, A/D converter, and EEPROM data memory. The PIC18F452 consists of:

- 4 timers/counters
- 2 capture/compare/PWM modules
- 2 serial communication modules
- 8 10-bit A/D converter channels
- 256 bytes EEPROM

The oscillator circuit, located at the left side of the diagram, consists of:

- Power-up timer
- Oscillator start-up timer
- Power-on reset
- Watchdog timer
- Brown-out reset
- Low-voltage programming
- In-circuit debugger
- PLL circuit
- Timing generation circuit

The PLL circuit is new to the PIC18F series and provides the option of multiplying up the oscillator frequency to speed up the overall operation. The watchdog timer can be used to force a restart of the microcontroller in the event of a program crash. The in-circuit debugger is useful during program development and can be used to return diagnostic data, including the register values, as the microcontroller is executing a program.

The input-output ports are located at the right side of the diagram. The PIC18F452 has five parallel ports named PORTA, PORTB, PORTC, PORTD, and PORTE. Most port pins have multiple functions. For example, PORTA pins can be used as parallel inputs-outputs or analog inputs. PORTB pins can be used as parallel inputs-outputs or as interrupt inputs.

2.1.1 Program Memory Organization

The program memory map is shown in Figure 2.3. All PIC18F devices have a 21-bit program counter and hence are capable of addressing 2Mbytes of memory space. User memory space on the PIC18F452 microcontroller is 00000H to 7FFFH. Accessing a nonexistent memory location (8000H to 1FFFFFH) will cause a read of all 0s. The reset vector, where the program starts after a reset, is at address 0000. Addresses 0008H and

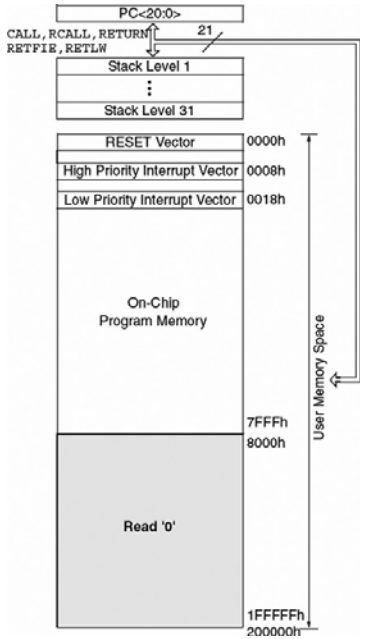


Figure 2.3: Program memory map of PIC18F452

0018H are reserved for the vectors of high-priority and low-priority interrupts respectively, and interrupt service routines must be written to start at one of these locations.

The PIC18F microcontroller has a 31-entry stack that is used to hold the return addresses for subroutine calls and interrupt processing. The stack is not part of the program or the data memory space. The stack is controlled by a 5-bit stack pointer which is initialized to 00000 after a reset. During a subroutine call (or interrupt) the stack pointer is first incremented, and the memory location it points to is written with the contents of the program counter. During the return from a subroutine call (or interrupt), the memory location the stack pointer has pointed to is decremented. The projects in this book are based on using the C language. Since subroutine and interrupt call/return operations are handled automatically by the C language compiler, their operation is not described here in more detail.

Program memory is addressed in bytes, and instructions are stored as two bytes or four bytes in program memory. The least significant byte of an instruction word is always stored in an even address of the program memory.

An instruction cycle consists of four cycles: A fetch cycle begins with the program counter incrementing in Q1. In the execution cycle, the fetched instruction is latched into the instruction register in cycle Q1. This instruction is decoded and executed during cycles Q2, Q3, and Q4. A data memory location is read during the Q2 cycle and written during the Q4 cycle.

2.1.2 Data Memory Organization

The data memory map of the PIC18F452 microcontroller is shown in Figure 2.4. The data memory address bus is 12 bits with the capability to address up to 4Mbytes. The memory in general consists of sixteen banks, each of 256 bytes, where only 6 banks are used. The PIC18F452 has 1536 bytes of data memory (6 banks × 256 bytes each) occupying the lower end of the data memory. Bank switching happens automatically when a high-level language compiler is used, and thus the user need not worry about selecting memory banks during programming.

The special function register (SFR) occupies the upper half of the top memory bank. SFR contains registers which control operations such as peripheral devices, timers/counters, A/D converter, interrupts, and USART. Figure 2.5 shows the SFR registers of the PIC18F452 microcontroller.

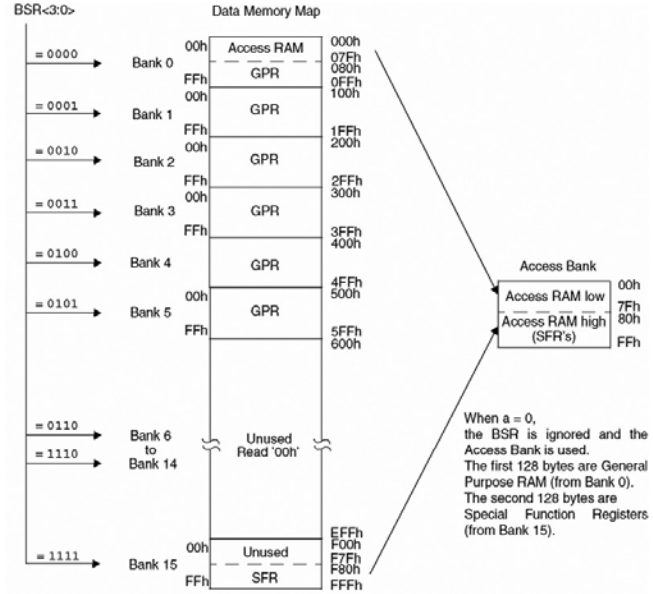


Figure 2.4: The PIC18F452 data memory map

2.1.3 The Configuration Registers

PIC18F452 microcontrollers have a set of configuration registers (PIC16-series microcontrollers had only one configuration register). Configuration registers are programmed during the programming of the flash program memory by the programming device. These registers are shown in Table 2.2. Descriptions of

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(3)	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2(3)	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2(3)	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2(3)	FBCh	CCPR2H	F9Ch	—
FFBh	PCLATU	FDBh	PLUSW2(3)	FBBh	CCPR2L	F9Bh	—
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	—
FF9h	PCL	FD9h	FSR2L	FB9h	—	F99h	—
FF8h	TBLPTRU	FD8h	STATUS	FB8h	—	F98h	—
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	—	F97h	—
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	—	F96h	TRISE(2)
FF5h	TABLAT	FD5h	T0CON	FB5h	—	F95h	TRISD(2)
FF4h	PRODH	FD4h	—	FB4h	—	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—
FF0h	INTCON3	FD0h	RCON	FB0h	—	F90h	—
FEFh	INDF0(3)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—
FEEh	POSTINC0(3)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—
FEDh	POSTDEC0(3)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(2)
FECh	PREINC0(3)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(2)
FEBh	PLUSW0(3)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	—	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—
FE7h	INDF1(3)	FC7h	SSPSTAT	FA7h	EECON2	F87h	—
FE6h	POSTINC1(3)	FC6h	SSPCON1	FA6h	EECON1	F86h	—
FE5h	POSTDEC1(3)	FC5h	SSPCON2	FA5h	—	F85h	—
FE4h	PREINC1(3)	FC4h	ADRESH	FA4h	—	F84h	PORTE(2)
FE3h	PLUSW1(3)	FC3h	ADRESL	FA3h	—	F83h	PORTD(2)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	—	FA0h	PIE2	F80h	PORTA

Figure 2.5: The PIC18F452 SFR registers

these registers are given in Table 2.3. Some of the more important configuration registers are described in this section in detail.

CONFIG1H

The CONFIG1H configuration register is at address 300001H and is used to select the microcontroller clock sources. The bit patterns are shown in Figure 2.6.

Table 2.2: PIC18F452 configuration registers

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	—	—	OSCSEN	—	—	FOSC2	FOSC1	FOSC0	--1- -111
300002h	CONFIG2L	—	—	—	—	BORV1	BORV0	BOREN	PWRTEN	---- 1111
300003h	CONFIG2H	—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN	---- 1111
300005h	CONFIG3H	—	—	—	—	—	—	—	CCP2MX	---- ---1
300006h	CONFIG4L	DEBUG	—	—	—	—	LVP	—	STVREN	1--- -1-1
300008h	CONFIG5L	—	—	—	—	CP3	CP2	CP1	CP0	---- 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	—	—	WRT3	WRT2	WRT1	WRT0	---- 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	—	—	EBTR3	EBTR2	EBTR1	EBTR0	---- 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	(1)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 0100

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

Table 2.3: PIC18F452 configuration register descriptions

Configuration bits	Description
OSCSEN	Clock source switching enable
FOSC2:FOSC0	Oscillator modes
BORV1:BORV0	Brown-out reset voltage
BOREN	Brown-out reset enable
PWRTEN	Power-up timer enable
WDTPS2:WDTPS0	Watchdog timer postscale bits
WDTEN	Watchdog timer enable
CCP2MX	CCP2 multiplex
DEBUG	Debug enable
LVP	Low-voltage program enable
STVREN	Stack full/underflow reset enable
CP3:CP0	Code protection
CPD	EEPROM code protection
CPB	Boot block code protection
WRT3:WRT0	Program memory write protection
WRTD	EPROM write protection
WRTB	Boot block write protection
WRTC	Configuration register write protection
EBTR3:EBTR0	Table read protection
EBTRB	Boot block table read protection
DEV2:DEV0	Device ID bits (001 = 18F452)
REV4:REV0	Revision ID bits
DEV10:DEV3	Device ID bits

U-0	U-0	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
—	—	OSCSEN	—	—	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCSEN**: Oscillator System Clock Switch Enable bit
1 = Oscillator system clock switch option is disabled (main oscillator is source)
0 = Oscillator system clock switch option is enabled (oscillator switching is enabled)

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **FOSC2:FOSC0**: Oscillator Selection bits
111 = RC oscillator w/ OSC2 configured as RA6
110 = HS oscillator with PLL enabled/Clock frequency = (4 x Fosc)
101 = EC oscillator w/ OSC2 configured as RA6
100 = EC oscillator w/ OSC2 configured as divide-by-4 clock output
011 = RC oscillator
010 = HS oscillator
001 = XT oscillator
000 = LP oscillator

Figure 2.6: CONFIG1H register bits

CONFIG2L

The CONFIG2L configuration register is at address 300002H and is used to select the brown-out voltage bits. The bit patterns are shown in Figure 2.7.

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	BORV1	BORV0	BOREN	PWRTEN
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BORV1:BORV0:** Brown-out Reset Voltage bits
11 = VBOR set to 2.5V
10 = VBOR set to 2.7V
01 = VBOR set to 4.2V
00 = VBOR set to 4.5V

bit 1 **BOREN:** Brown-out Reset Enable bit
1 = Brown-out Reset enabled
0 = Brown-out Reset disabled

bit 0 **PWRTEN:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

Figure 2.7: CONFIG2L register bits

CONFIG2H

The CONFIG2H configuration register is at address 300003H and is used to select the watchdog operations. The bit patterns are shown in Figure 2.8.

2.1.4 The Power Supply

The power supply requirements of the PIC18F452 microcontroller are shown in Figure 2.9. As shown in Figure 2.10, PIC18F452 can operate with a supply voltage of 4.2V to 5.5V at the full speed of 40MHz. The lower power version, PIC18LF452, can operate from 2.0 to 5.5 volts. At lower voltages the maximum clock frequency is 4MHz, which rises to 40MHz at 4.2V. The RAM data retention voltage is specified as 1.5V and will be lost if the power supply voltage is lowered below this value. In practice, most microcontroller-based systems are operated with a single +5V supply derived from a suitable voltage regulator.

2.1.5 The Reset

The reset action puts the microcontroller into a known state. Resetting a PIC18F microcontroller starts execution of the program from address 0000H of the

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3-1 **WDTPS2:WDTPS0:** Watchdog Timer Postscale Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8
010 = 1:4
001 = 1:2
000 = 1:1

bit 0 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled (control is placed on the SWDTEN bit)

Figure 2.8: CONFIG2H register bits

PIC18LFXX2 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18FXX2 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
	VDD	**Supply Voltage**					
D001		PIC18LFXX2	2.0	—	5.5	V	HS, XT, RC and LP Osc mode
D001		PIC18FXX2	4.2	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	0.7	V	See Section 3.1 (Power-on Reset) for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 3.1 (Power-on Reset) for details
	VBOR	**Brown-out Reset Voltage**					
D005		PIC18LFXX2					
		BORV1:BORV0 = 11	1.98	—	2.14	V	85°C ≥ T ≥ 25°C
		BORV1:BORV0 = 10	2.67	—	2.89	V	
		BORV1:BORV0 = 01	4.16	—	4.5	V	
		BORV1:BORV0 = 00	4.45	—	4.83	V	
D005		PIC18FXX2					
		BORV1:BORV0 = 1x	N.A.	—	N.A.	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	4.16	—	4.5	V	
		BORV1:BORV0 = 00	4.45	—	4.83	V	

Legend: Shading of rows is to assist in readability of the table.

Figure 2.9: The PIC8F452 power supply parameters

program memory. The microcontroller can be reset during one of the following operations:

- Power-on reset (POR)
- MCLR reset
- Watchdog timer (WDT) reset
- Brown-out reset (BOR)
- Reset instruction

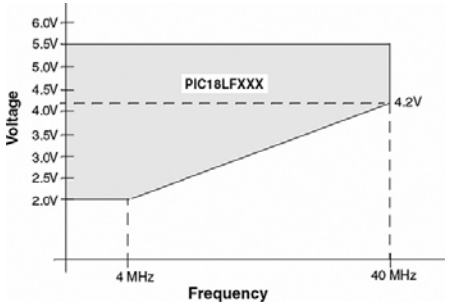


Figure 2.10: Operation of PIC18LF452 at different voltages

- Stack full reset
- Stack underflow reset

Two types of resets are commonly used: power-on reset and external reset using the MCLR pin.

Power-on Reset

The power-on reset is generated automatically when power supply voltage is applied to the chip. The MCLR pin should be tied to the supply voltage directly or, preferably, through a 10K resistor. Figure 2.11 shows a typical reset circuit.

For applications where the rise time of the voltage is slow, it is recommended to use a diode, a capacitor, and a series resistor as shown in Figure 2.12.

In some applications the microcontroller may have to be reset externally by pressing a button. Figure 2.13 shows the circuit that can be used to reset the microcontroller externally. Normally the MCLR input is at logic 1. When the RESET button is pressed, this pin goes to logic 0 and resets the microcontroller.

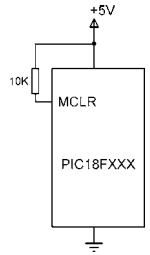


Figure 2.11: Typical reset circuit

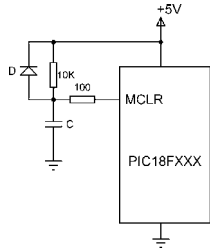


Figure 2.12: Reset circuit for slow-rising voltages

2.1.6 The Clock Sources

The PIC18F452 microcontroller can be operated from an external crystal or ceramic resonator connected to the microcontroller's OSC1 and OSC2 pins. In addition, an external resistor and capacitor, an external clock source, and in some models internal oscillators can be used to provide clock pulses to the microcontroller. There are eight clock sources on the PIC18F452 microcontroller, selected by the configuration register CONFIG1H. These are:

- Low-power crystal (LP)
- Crystal or ceramic resonator (XT)

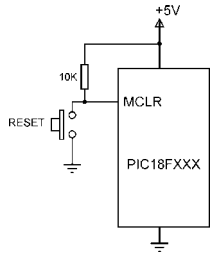


Figure 2.13: External reset circuit

- High-speed crystal or ceramic resonator (HS)
- High-speed crystal or ceramic resonator with PLL (HSPLL)
- External clock with $F_{OSC/4}$ on OSC2 (EC)
- External clock with I/O on OSC2 (port RA6) (ECIO)
- External resistor/capacitor with $F_{OSC/4}$ output on OSC2 (RC)
- External resistor/capacitor with I/O on OSC2 (port RA6) (RCIO)

Crystal or Ceramic Resonator Operation

The first several clock sources listed use an external crystal or ceramic resonator that is connected to the OSC1 and OSC2 pins. For applications where accuracy of timing is important, a crystal should be used. And if a crystal is used, a parallel resonant crystal must be chosen, since series resonant crystals do not oscillate when the system is first powered.

Figure 2.14 shows how a crystal is connected to the microcontroller. The capacitor values depend on the mode of the crystal and the selected frequency. Table 2.4 gives the recommended values. For example, for a 4MHz crystal frequency, use 15pF capacitors. Higher capacitance increases the oscillator stability but also increases the start-up time.

Resonators should be used in low-cost applications where high accuracy in timing is not required. Figure 2.15 shows how a resonator is connected to the microcontroller.

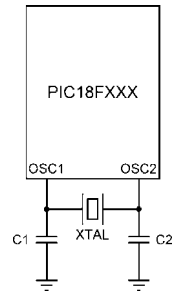


Figure 2.14: Using a crystal as the clock input

Table 2.4: Capacitor values

Mode	Frequency	C1,C2 (pF)
LP	32 KHz	33
	200 KHz	15
XT	200 KHz	22–68
	1.0 MHz	15
	4.0 MHz	15
HS	4.0 MHz	15
	8.0 MHz	15–33
	20.0 MHz	15–33
	25.0 MHz	15–33

The LP (low-power) oscillator mode is advised in applications to up to 200KHz clock. The XT mode is advised to up to 4MHz, and the HS (high-speed) mode is advised in applications where the clock frequency is between 4MHz to 25MHz.

An external clock source may also be connected to the OSC1 pin in the LP, XT, or HS modes as shown in Figure 2.16.

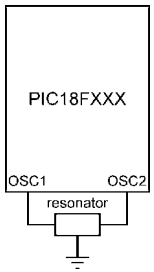


Figure 2.15: Using a resonator as the clock input

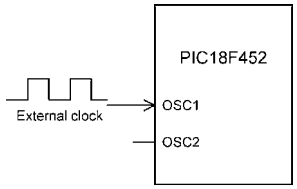


Figure 2.16: Connecting an external clock in LP, XT, or HS modes

External Clock Operation

An external clock source can be connected to the OSC1 input of the microcontroller in EC and ECIO modes. No oscillator start-up time is required after a power-on reset. Figure 2.17 shows the operation with the external clock in EC mode. Timing pulses at the frequency $F_{OSC/4}$ are available on the OSC2 pin. These pulses can be used for test purposes or to provide pulses to external devices.

The ECIO mode is similar to the EC mode, except that the OSC2 pin can be used as a general purpose digital I/O pin. As shown in Figure 2.18, this pin becomes bit 6 of PORTA (i.e., pin RA6).

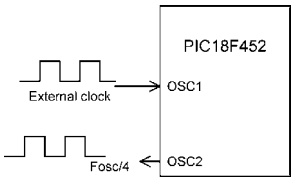


Figure 2.17: External clock in EC mode

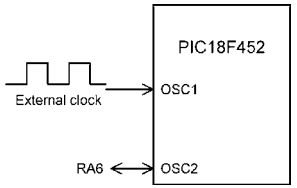


Figure 2.18: External clock in ECIO mode

Resistor/Capacitor Operation

In the many applications where accurate timing is not required we can use an external resistor and a capacitor to provide clock pulses. The clock frequency is a function of the resistor, the capacitor, the power supply voltage, and the temperature. The clock frequency is not accurate and can vary from unit to unit due to manufacturing and component tolerances. Table 2.5 gives the approximate clock frequency with various resistor and capacitor combinations. A close approximation of the clock frequency is 1/(4.2RC), where R should be between 3K and 100K and C should be greater than 20pF.

In RC mode, the oscillator frequency divided by 4 ($F_{OSC/4}$) is available on pin OSC2 of the microcontroller. Figure 2.19 shows the operation at a clock frequency of approximately 2MHz, where R = 3.9K and C = 30pF. In this application the clock frequency at the output of OSC2 is 2MHz/4 = 500KHz.

Table 2.5: Clock frequency with RC

C (pF)	R (K)	Frequency (MHz)
22	3.3	3.3
	4.7	2.3
	10	1.08
30	3.3	2.4
	4.7	1.7
	10	0.793

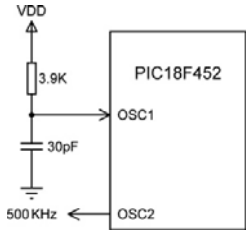


Figure 2.19: 2MHz clock in RC mode

RCIO mode is similar to RC mode, except that the OSC2 pin can be used as a general purpose digital I/O pin. As shown in Figure 2.20, this pin becomes bit 6 of PORTA (i.e., pin RA6).

Crystal or Resonator with PLL

One of the problems with using high-frequency crystals or resonators is electromagnetic interference. A Phase Locked Loop (PLL) circuit is provided that can be enabled to multiply the clock frequency by 4. Thus, for a crystal clock frequency of 10MHz, the

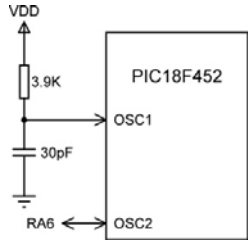


Figure 2.20: 2MHz clock in RCIO mode

internal operation frequency will be multiplied to 40MHz. The PLL mode is enabled when the oscillator configuration bits are programmed for HS mode.

Internal Clock

Some devices in the PIC18F family have internal clock modes (although the PIC18F452 does not). In this mode, OSC1 and OSC2 pins are available for general purpose I/O (RA6 and RA7) or as $F_{OSC/4}$ and RA7. An internal clock can be from 31KHz to 8MHz and is selected by registers OSCCON and OSCTUNE. Figure 2.21 shows the bits of internal clock control registers.

Clock Switching

It is possible to switch the clock from the main oscillator to a low-frequency clock source. For example, the clock can be allowed to run fast in periods of intense activity and slower when there is less activity. In the PIC18F452 microcontroller this is controlled by bit SCS of the OSCCON register. In microcontrollers of the PIC18F family that do support an internal clock, clock switching is controlled by bits SCS0 and SCS1 of OSCCON. It is important to ensure that during clock switching unwanted glitches do not occur in the clock signal. PIC18F microcontrollers contain circuitry to ensure error-free switching from one frequency to another.

OSCCON register

IDLEN	IRCF2	IRCF1	IRCF0	OSTS	I0FS	SCSI	SCS0

IDLEN 0 Run mode enabled
1 Idle mode enabled

IRCF2:IRCF0 000 31 KHz
001 125 KHz
010 250 KHz
011 500 KHz
100 1 MHz
101 2 MHz
110 4 MHz
111 8 MHz

OSTS 0 Oscillator start-up timer running
1 Oscillator start-up timer expired

IOFS 0 Internal oscillator unstable
1 Internal oscillator stable

SCSI:SCS0 00 Primary oscillator
01 Timer 1 oscillator
10 Internal oscillator
11 Internal oscillator

OSCTUNE register

X	X	T5	T4	T3	T2	T1	T0

XX011111 Maximum frequency

XX000001
XX000000 Center frequency
XX111111

XX100000 Minimum frequency

Figure 2.21: Internal clock control registers

2.1.7 Watchdog Timer

In PIC18F-series microcontrollers family members the watchdog timer (WDT) is a free-running on-chip RC-based oscillator and does not require any external components. When the WDT times out, a device RESET is generated. If the device is in SLEEP mode, the WDT time-out will wake it up and continue with normal operation.

The watchdog is enabled/disabled by bit SWDTEN of register WDTCON. Setting SWDTEN = 1 enables the WDT, and clearing this bit turns off the WDT. On the PIC18F452 microcontroller an 8-bit postscaler is used to multiply the basic time-out

period from 1 to 128 in powers of 2. This postscaler is controlled from configuration register CONFIG2H. The typical basic WDT time-out period is 18ms for a postscaler value of 1.

2.1.8 Parallel I/O Ports

The parallel ports in PIC18F microcontrollers are very similar to those of the PIC16 series. The number of I/O ports and port pins varies depending on which PIC18F microcontroller is used, but all of them have at least PORTA and PORTB. The pins of a port are labeled as RPn, where *P* is the port letter and *n* is the port bit number. For example, PORTA pins are labeled RA0 to RA7, PORTB pins are labeled RB0 to RB7, and so on.

When working with a port we may want to:

- Set port direction
- Set an output value
- Read an input value
- Set an output value and then read back the output value

The first three operations are the same in the PIC16 and the PIC18F series. In some applications we may want to send a value to the port and then read back the value just sent. The PIC16 series has a weakness in the port design such that the value read from a port may be different from the value just written to it. This is because the reading is the actual port bit pin value, and this value can be changed by external devices connected to the port pin. In the PIC18F series, a latch register (e.g., LATA for PORTA) is introduced to the I/O ports to hold the actual value sent to a port pin. Reading from the port reads the latched value, which is not affected by any external device.

In this section we shall be looking at the general structure of I/O ports.

PORTA

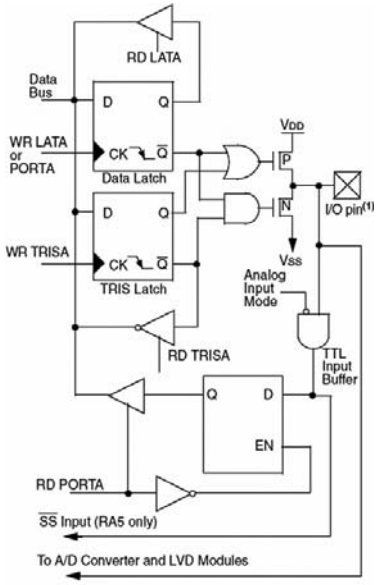
In the PIC18F452 microcontroller PORTA is 7 bits wide and port pins are shared with other functions. Table 2.6 shows the PORTA pin functions.

Table 2.6: PIC18F452 PORTA pin functions

Pin	Description
RA0/AN0	
RA0	Digital I/O
AN0	Analog input 0
RA1/AN1	
RA1	Digital I/O
AN1	Analog input 1
RA2/AN2/VREF−	
RA2	Digital I/O
AN2	Analog input 2
VREF−	A/D reference voltage (low) input
RA3/AN3/VREF+	
RA3	Digital I/O
AN3	Analog input 3
VREF+	A/D reference voltage (high) input
RA4/T0CKI	
RA4	Digital I/O
T0CKI	Timer 0 external clock input
RA5/AN4/SS/LVDIN	
RA5	Digital I/O
AN4	Analog input 4
SS	SPI Slave Select input
RA6	Digital I/O

The architecture of PORTA is shown in Figure 2.22. There are three registers associated with PORTA:

- Port data register—PORTA
- Port direction register—TRISA
- Port latch register—LATA



Note 1: I/O pins have protection diodes to VDD and Vss.

Figure 2.22: PIC18F452 PORTA RA0–RA3 and RA5 pins

PORTA is the name of the port data register. The TRISA register defines the direction of PORTA pins, where a logic 1 in a bit position defines the pin as an input pin, and a 0 in a bit position defines it as an output pin. LATA is the output latch register which shares the same data latch as PORTA. Writing to one is equivalent to writing to the other. But reading from LATA activates the buffer at the top of the diagram, and the value held in the PORTA/LATA data latch is transferred to the data bus independent of the state of the actual output pin of the microcontroller.

Bits 0 through 3 and 5 of PORTA are also used as analog inputs. After a device reset, these pins are programmed as analog inputs and RA4 and RA6 are configured as digital inputs. To program the analog inputs as digital I/O, the ADCON1 register (A/D register) must be programmed accordingly. Writing 7 to ADCON1 configures all PORTA pins as digital I/O.

The RA4 pin is multiplexed with the Timer 0 clock input (T0CKI). This is a Schmitt trigger input and an open drain output.

RA6 can be used as a general purpose I/O pin, as the OSC2 clock input, or as a clock output providing $F_{OSC/4}$ clock pulses.

PORTB

In PIC18F452 microcontroller PORTB is an 8-bit bidirectional port shared with interrupt pins and serial device programming pins. Table 2.7 gives the PORTB bit functions.

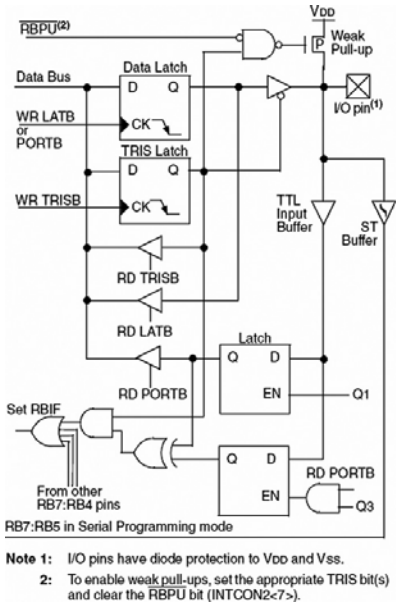
PORTB is controlled by three registers:

- Port data register—PORTB
- Port direction register—TRISB
- Port latch register—LATB

The general operation of PORTB is similar to that of PORTA. Figure 2.23 shows the architecture of PORTB. Each port pin has a weak internal pull-up which can be enabled by clearing bit RBPU of register INTCON2. These pull-ups are disabled on a power-on reset and when the port pin is configured as an output. On a power-on reset, PORTB pins are configured as digital inputs. Internal pull-ups allow input devices such as switches to be connected to PORTB pins without the use of external pull-up resistors. This saves costs because the component count and wiring requirements are reduced.

Table 2.7: PIC18F452 PORTB pin functions

Pin	Description
RB0/INT0	
RB0	Digital I/O
INT0	External interrupt 0
RB1/INT1	
RB1	Digital I/O
INT1	External interrupt 1
RB2/INT2	
RB2	Digital I/O
INT2	External interrupt 2
RB3/ CCP2	
RB3	Digital I/O
CCP2	Capture 2 input, compare 2, and PWM2 output
RB4	Digital I/O, interrupt on change pin
RB5/PGM	
RB5	Digital I/O, interrupt on change pin
PGM	Low-voltage ICSP programming pin
RB6/PGC	
RB6	Digital I/O, interrupt on change pin
PGC	In-circuit debugger and ICSP programming pin
RB7/PGD	
RB7	Digital I/O, interrupt on change pin
PGD	In-circuit debugger and ICSP programming pin



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (INTCON2<7>).

Figure 2.23: PIC18F452 PORTB RB4–RB7 pins

Port pins RB4–RB7 can be used as interrupt-on-change inputs, whereby a change on any of pins 4 through 7 causes an interrupt flag to be set. The interrupt enable and flag bits RBIE and RBIF are in register INTCON.

PORTC, PORTD, PORTE, and Beyond

In addition to PORTA and PORTB, the PIC18F452 has 8-bit bidirectional ports PORTC and PORTD, and 3-bit PORTE. Each port has its own data register (e.g., PORTC), data