



The diagram illustrates the die architecture of a multi-core processor. It features a central horizontal bar for the Shared L3 Cache, four individual cores arranged in a row above it, and a large block on the left for the Processor Graphics. To the right of the cores is a vertical block for the System Agent, Display Engine & Memory Controller. At the bottom is a horizontal bar for the Memory Controller I/O. The entire die is represented by a colorful, abstract pattern of yellow, blue, and green.

**Processor
Graphics**

Core

Core

Core

Core

**System
Agent,
Display
Engine &
Memory
Controller**

including
Display, PCIe*
and DMI I/Os

Shared L3 Cache**

Memory Controller I/O