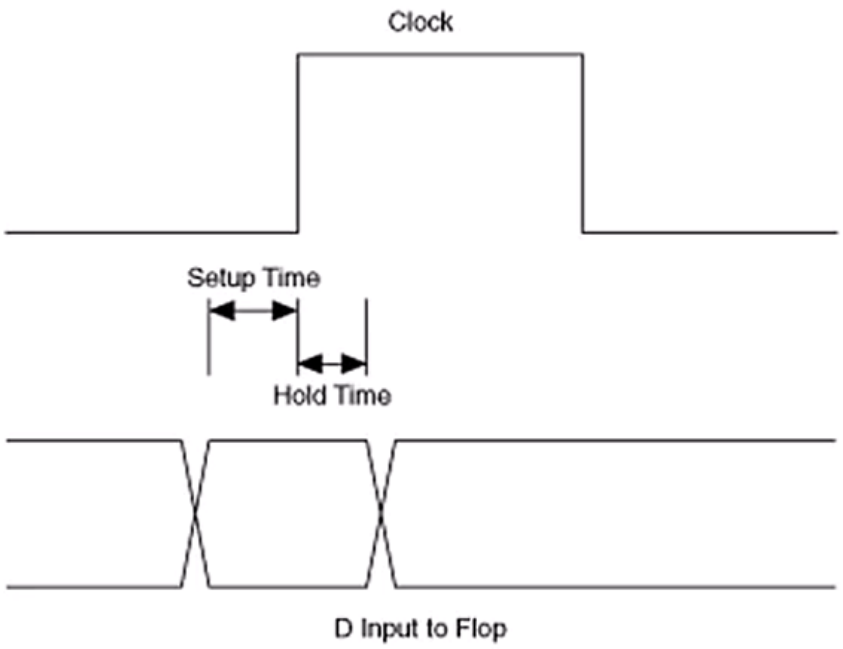
Question 3

- “Setup Time” and “hold time” describe the timing requirements on the data input of the flip-flop or register with respect to the clock
- A **positive setup time** describes the length of time that the data (to be clocked into the flip-flop) must be available and stable before the active clock edge
- A **positive hold time** describes the length of time that the data (to be clocked into the flip-flop) must remain available and stable after the active clock edge
- Diagram below is from lecture, used to visual setup and hold times



Source: The Ultimate Hitchhiker's Guide to Verification