Module 2 - Lab 2 Report

Resources	Lab 1	Lab 2
Slice LUTs as Logic	8	8
Slice LUTs as Memory	0	0
Slice Registers as Flip Flop	0	0
Slice Registers as Latch	0	0
Number of bonded IOBs	51	51
Number of Clocks	0	0

Both the Conditional Signal Assignment and the Process implementations have the same synthesis results. This makes sense as the logic is exactly the same between the implementations.

This analysis is further proven by looking at the RTL schematics, which do not show any differences between the two implementations.