The Operation of the FIFO in the DP8390, DP83901, DP83902 and DP83905

National Semiconductor
Application Note 886
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1.0 INTRODUCTION

To accommodate the different rates at which data comes from (or goes to) the network and goes to (or comes from) the system memory, the NIC contains a 16-byte FIFO for buffering data between the bus and the media. The FIFO threshold is programmable, allowing filling (or emptying) the FIFO with different burst lengths. When the FIFO has filled to its programmed threshold, the local DMA channel transfers these bytes or words into local memory. It is crucial that the local DMA is given access to the bus within a minimum bus latency time, otherwise a FIFO underrun (or overrun) occurs. During transmission the DMA writes data into the FIFO and the Transmit Serializer reads data from the FIFO and transmits it. During reception the Receive Deserializer writes data into the FIFO and the DMA reads data from the FIFO.

2.0 FIFO THRESHOLD

The DMA transfers between the FIFO and memory occur in bursts beginning when the FIFO threshold is reached. The threshold takes on different meanings during transmission and reception. During reception the FIFO threshold refers to the number of bytes in the FIFO. During transmission the FIFO threshold refers to the number of empty bytes in the FIFO: the size of the FIFO (16) $-$ # bytes in FIFO. Bits FT0 and FT1 in the Data Configuration Register set the FIFO threshold to 2 bytes, 4 bytes, 8 bytes, or 12 bytes (1 word, 2 words, 4 words, or 6 words).

The threshold for the first burst is different than subsequent thresholds as discussed in detail in Sections 3.0 and 4.0. The values in Tables I and II are derived from the timing diagrams in Section 6.0. The first threshold refers to the state of the FIFO at point B in the timing diagrams, and the threshold refers to the state of the FIFO at point D. The discussion below refers to the threshold, not the first threshold.

The FIFO logic operates differently in reception and transmission. During reception in byte mode, a threshold is indicated when approximately the n $+$ 14th bit has entered the FIFO; thus, with an 8-byte threshold, the NIC issues Bus Request (BREQ) when the FIFO contains 9 bytes and 6 bits. For reception in word mode, BREQ is generated when approximately n $+$ 22 bits have entered the FIFO; thus with a 2-word threshold, BREQ is issued when the 54th bit has entered the FIFO. Refer to Table I for the exact receive thresholds for each case.

During transmission in byte mode, a threshold is indicated when approximately the n $+$ 12th bit has entered the FIFO; thus with an 8-byte threshold, the NIC issues BREQ when the FIFO contains 9 bytes and 4 bits. For transmission in word mode, BREQ is generated when approximately n $+$ 29 bits have entered the FIFO. Thus, with a 4-word threshold (equivalent to an 8-byte threshold), BREQ is issued when the 96th bit has entered the FIFO. Refer to Table II for the exact transmit thresholds for each case.

TABLE I. Receive Packet Thresholds

Receive Packet Cases	First Threshold	Threshold
Word Mode, 1 Word Threshold	4 Words, 11 bits	2 Words, 5 bits
Word Mode, 2 Word Threshold	4 Words, 10 bits	3 Words, 6 bits
Word Mode, 4 Word Threshold	5 Words, 7 bits	5 Words, 5 bits
Word Mode, 6 Word Threshold	6 Words, 8 bits	6 Words, 6 bits
Byte Mode, 2 Byte Threshold	9 Bytes, 2 bits	3 Bytes, 4 bits
Byte Mode, 4 Byte Threshold #1	9 Bytes, 2 bits	5 Bytes, 6 bits
Byte Mode, 4 Byte Threshold #2	9 Bytes, 6 bits	5 Bytes, 6 bits
Byte Mode, 8 Byte Threshold	10 Bytes	9 Bytes, 6 bits
Byte Mode, 12 Byte Threshold	13 Bytes, 7 bits	13 Bytes, 5 bits

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TABLE II. Transmit Packet Thresholds

Transmit Packet Cases	First Threshold	Threshold
Word Mode, 1 Word Threshold	6 Words	3 Words, 12 bits
Word Mode, 2 Word Threshold	4 Words, 3 bits	3 Words, 13 bits
Word Mode, 4 Word Threshold	5 Words, 13 bits	5 Words, 13 bits
Word Mode, 6 Word Threshold	7 Words, 13 bits	7 Words, 13 bits
Byte Mode, 2 Byte Threshold	12 Words, 1 bit	(See Timing Diagram, *Figure 14*)
Byte Mode, 4 Byte Threshold	12 Bytes, 1 bit	5 Bytes, 5 bits
Byte Mode, 8 Byte Threshold	9 Bytes, 6 bits	9 Bytes, 4 bits
Byte Mode, 12 Byte Threshold	13 Bytes, 6 bits	13 Bytes, 4 bits

3.0 FIFO OPERATION DURING RECEIVE

At the beginning of reception, the NIC stores the entire Address field of each incoming packet in the FIFO to determine whether the packet matches its Physical Address Registers or maps to one of its Multicast Registers. Therefore, the first local DMA transfer does not occur until after 8 bytes (4 words) have accumulated in the FIFO, regardless of the value of the threshold. This affects the bus latencies at 2 byte, 4 byte, 1 word, and 2 word thresholds during the first receive BREQ. Thus the threshold for the first burst that is loaded into memory differs from the remaining threshold values. Refer to Table I for the exact threshold values.

4.0 FIFO OPERATION DURING TRANSMIT

Before transmitting, the NIC performs a prefetch from memory to load the FIFO. The number of bytes prefetched is the programmed FIFO threshold, except for 1 byte, 1 word, and 2 word thresholds which prefetch 4 bytes, 2 words, and 4 words respectively. The next BREQ is not issued until after the NIC actually begins transmitting data, i.e., after Preamble and SFD. The threshold for the first burst that is loaded from memory following the prefetched data often differs from the remaining threshold values. Refer to Table II for the exact threshold values.

5.0 FIFO UNDERRUNS AND OVERRUNS

To assure that there is no overwriting of data, the FIFO logic flags an overrun if it becomes full before bus acknowledge is returned. To assure that there is no lost data, the FIFO flags an underrun if it becomes empty before bus acknowledge is returned. There are two causes which produce overruns and underruns:

1. The bus latency is so long that the FIFO has filled (or emptied) before the local DMA has serviced the FIFO.
2. The bus latency or bus data rate has slowed the throughput of the local DMA to a point where it is slower than the network data rate (10 Mb/s). This second condition is also dependent upon DMA clock and data width (byte wide or word wide).

The worst case condition ultimately limits the overall bus latency that the NIC can tolerate.

6.0 TIMING DIAGRAMS

The following pages contain detailed timing diagrams and descriptions of every possible receive and transmit mode transfer. The descriptions are of 2, 4, 8, and 12 byte transfers (on an 8-bit Novell board) and 1, 2, 4, and 6 word transfers (on a 16-bit Novell board). For each transfer, the bus clock runs at 20.0 MHz. Tables III and IV summarize the information found in the receive and transmit transfer diagrams respectively.

TABLE III. Receive Packet Transfers

Receive Packet Cases	After SFD to BREQ Asserted (Point A to B)	BREQ Asserted to $\overline{\text{MWR}}$ Deasserted (Point B to C)	$\overline{\text{MWR}}$ Deasserted to BREQ Asserted (Point C to D)	BREQ Asserted to $\overline{\text{MWR}}$ Deasserted (Point D to E)
Word Mode 1 Word Threshold	75 ± 4 bits Shifted In	7 Words Removed 52 bits Shifted In	22 bits Shifted In	2 Words Removed 12 bits Shifted In
Word Mode 2 Word Threshold	74 ± 2 bits Shifted In	4 Words Removed 16 bits Shifted In	28 bits Shifted In	2 Words Removed 6 bits Shifted In
Word Mode 4 Word Threshold	87 ± 2 bits Shifted In	4 Words Removed 9 bits Shifted In	53 bits Shifted In	4 Words Removed 9 bits Shifted In
Word Mode 6 Word Threshold	104 ± 2 bits Shifted In	6 Words Removed 14 bits Shifted In	80 bits Shifted In	6 Words Removed 14 bits Shifted In
Byte Mode 2 Byte Threshold	74 ± 2 bits Shifted In	18 Bytes Removed 86 bits Shifted In	12 bits Shifted In	2 Bytes Removed 6 bits Shifted In
Byte Mode 4 Byte Threshold #1	74 ± 1 bit Shifted In	8 Bytes Removed 23 bits Shifted In	21 bits Shifted In	4 Bytes Removed 10 bits Shifted In
Byte Mode 4 Byte Threshold #2	78 ± 1 bit Shifted In	12 Bytes Removed 38 bits Shifted In	26 bits Shifted In	4 Bytes Removed 10 bits Shifted In
Byte Mode 8 Byte Threshold	80 ± 2 bits Shifted In	8 Bytes Removed 18 bits Shifted In	44 bits Shifted In	8 Bytes Removed 18 bits Shifted In
Byte Mode 12 Byte Threshold	111 ± 2 bits Shifted In	12 Bytes Removed 26 bits Shifted In	68 bits Shifted In	12 Bytes Removed 26 bits Shifted In

TABLE IV. Transmit Packet Transfers

Transmit Packet Cases	Initial Loading to BREQ Asserted (Point A to B)	BREQ Asserted to $\overline{\text{MRD}}$ Deasserted (Point B to C)	$\overline{\text{MRD}}$ Deasserted to BREQ Asserted (Point C to D)	BREQ Asserted to $\overline{\text{MRD}}$ Deasserted (Point D to E)
Word Mode 1 Word Threshold	2 Words Loaded 0 bits Shifted Out	7 Words Loaded 52 bits Shifted Out	24 bits Shifted Out	2 Words Loaded 12 bits Shifted Out
Word Mode 2 Word Threshold	4 Words Loaded 3 bits Shifted Out	2 Words Loaded 6 bits Shifted Out	20 bits Shifted Out	2 Words Loaded 6 bits Shifted Out
Word Mode 4 Word Threshold	4 Words Loaded 29 bits Shifted Out	4 Words Loaded 14 bits Shifted Out	54 bits Shifted Out	4 Words Loaded 9 bits Shifted in
Word Mode 6 Word Threshold	6 Words Loaded 93 bits Shifted Out	6 Words Loaded 14 bits Shifted in	82 bits Shifted Out	6 Words Loaded 14 bits Shifted in
Byte Mode 2 Byte Threshold	4 Bytes Loaded 1 bit Shifted Out	(Refer to Timing Diagram *Figure 14*)	(Refer to Timing Diagram *Figure 14*)	(Refer to Timing Diagram *Figure 14*)
Byte Mode 4 Byte Threshold	4 Bytes Loaded 1 bit Shifted Out	15 Bytes Loaded 49 bits Shifted Out	19 bits Shifted Out	4 Bytes Loaded 10 bits Shifted Out
Byte Mode 8 Byte Threshold	8 Bytes Loaded 22 bits Shifted Out	8 Bytes Loaded 18 bits Shifted Out	44 bits Shifted Out	8 Bytes Loaded 18 bits Shifted Out
Byte Mode 12 Byte Threshold	12 Bytes Loaded 78 bits Shifted Out	12 Bytes Loaded 26 bits Shifted Out	68 bits Shifted Out	12 Bytes Loaded 26 bits Shifted Out

RECEIVE PACKET

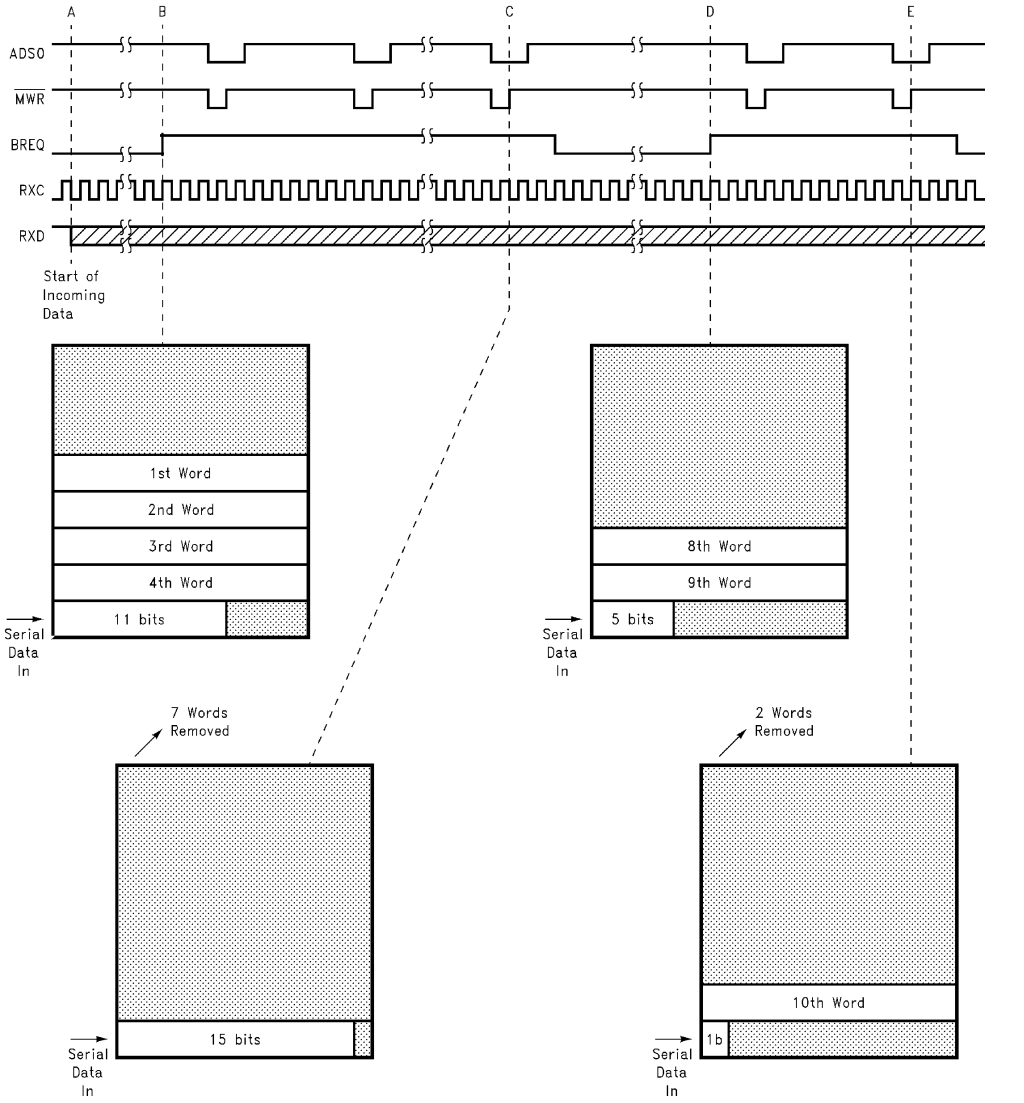

FIGURE 1. Receive Packet—Word Mode, 1 Word Threshold

After the preamble and the Start of Frame Delimiter (SFD) (Point A), the FIFO shifts in 75 ± 4 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 7 words into memory while shifting in 52 bits of data until $\overline{\text{MWR}}$ is deasserted (Point C). BREQ is asserted when there are 2 words and 5 bits in the FIFO (Point D). Two words are removed from the FIFO and stored in memory, while 12 bits are shifted into the FIFO until $\overline{\text{MWR}}$ is deasserted (Point E). D and E are repeated until the packet is complete.

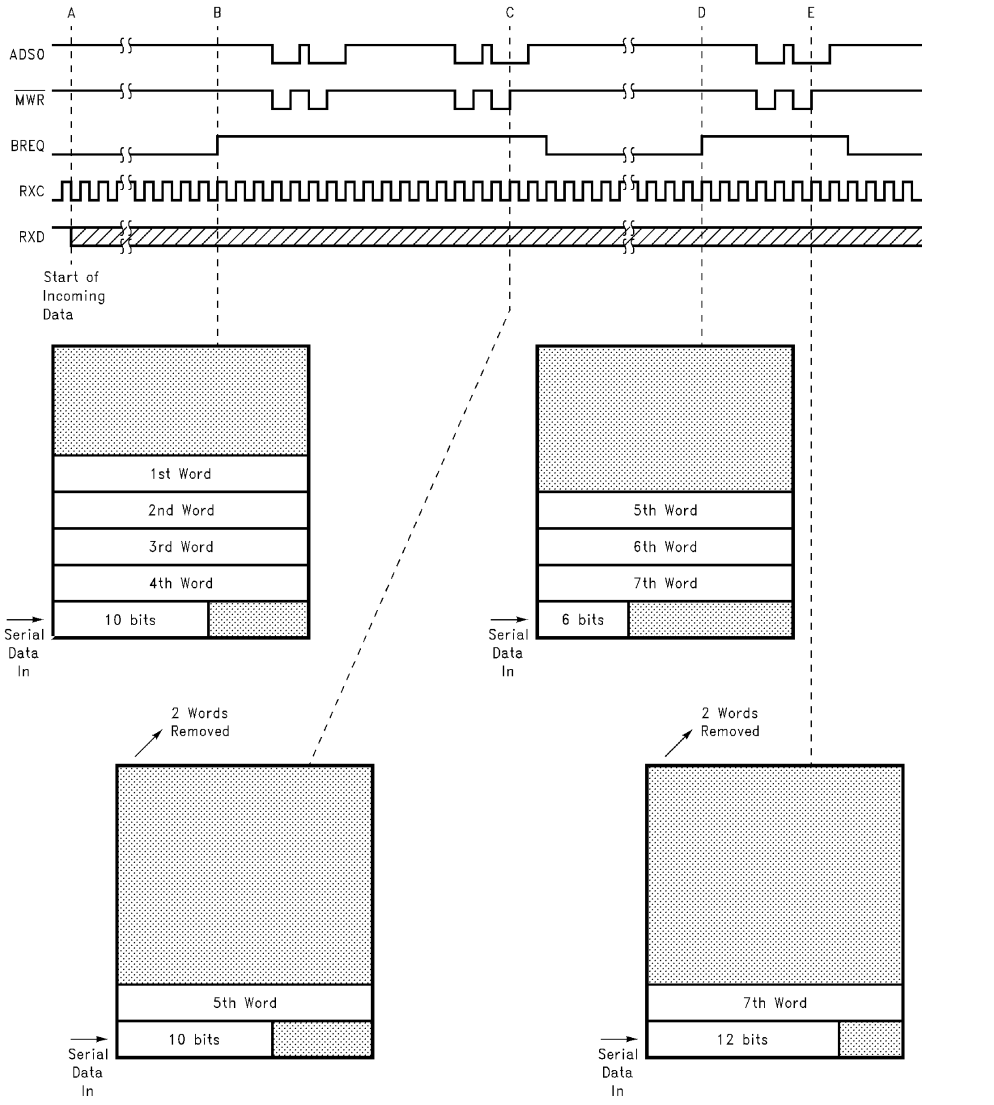

FIGURE 2. Receive Packet—Word Mode, 2 Word Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 74 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 2 bursts of 2 words each into memory while shifting in 16 bits of data until $\overline{MWR}$ is deasserted (Point C). BREQ is asserted when there are 3 words and 6 bits in the FIFO (Point D). Two words are removed from the FIFO and stored in memory, while 6 bits are shifted into the FIFO until $\overline{MWR}$ is deasserted (Point E). D and E are repeated until the packet is complete.

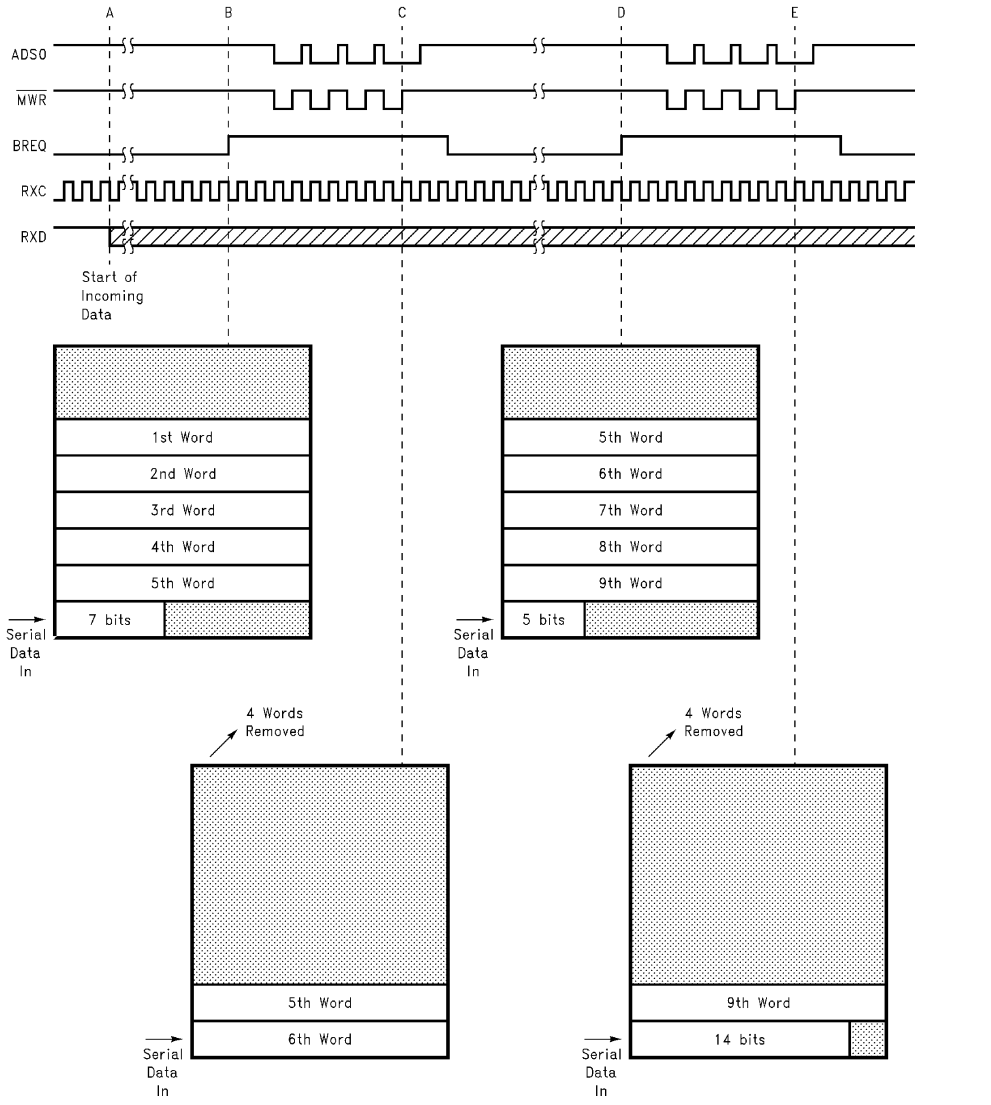

FIGURE 3. Receive Packet—Word Mode, 4 Word Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 87 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 1 burst of 4 words into memory while shifting in 9 bits of data until $\overline{\text{MWR}}$ is deasserted (Point C). BREQ is asserted when there are 5 words and 5 bits in the FIFO (Point D). Again, 4 words are removed from the FIFO and stored in memory, while 9 bits are shifted into the FIFO until $\overline{\text{MWR}}$ is deasserted (Point E). D and E are repeated until the packet is complete.

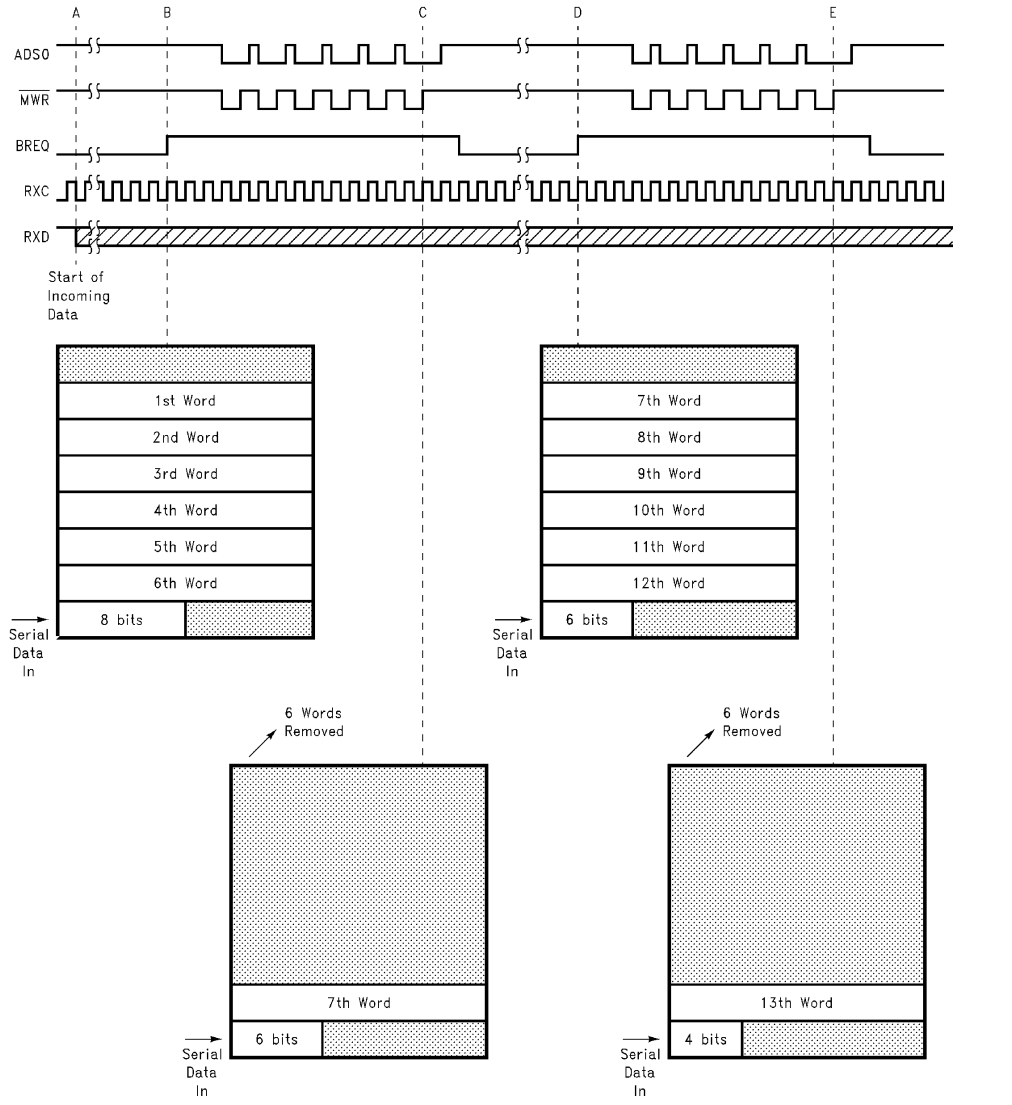

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FIGURE 4. Receive Packet—Word Mode, 6 Word Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 104 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 1 burst of 6 words into memory while shifting in 14 bits of data until $\overline{MWR}$ is deasserted (Point C). BREQ is asserted when there are 6 words and 6 bits in the FIFO (Point D). Again, 6 words are removed from the FIFO and stored in memory, while 14 bits are shifted into the FIFO until $\overline{MWR}$ is deasserted (Point E). D and E are repeated until the packet is complete.

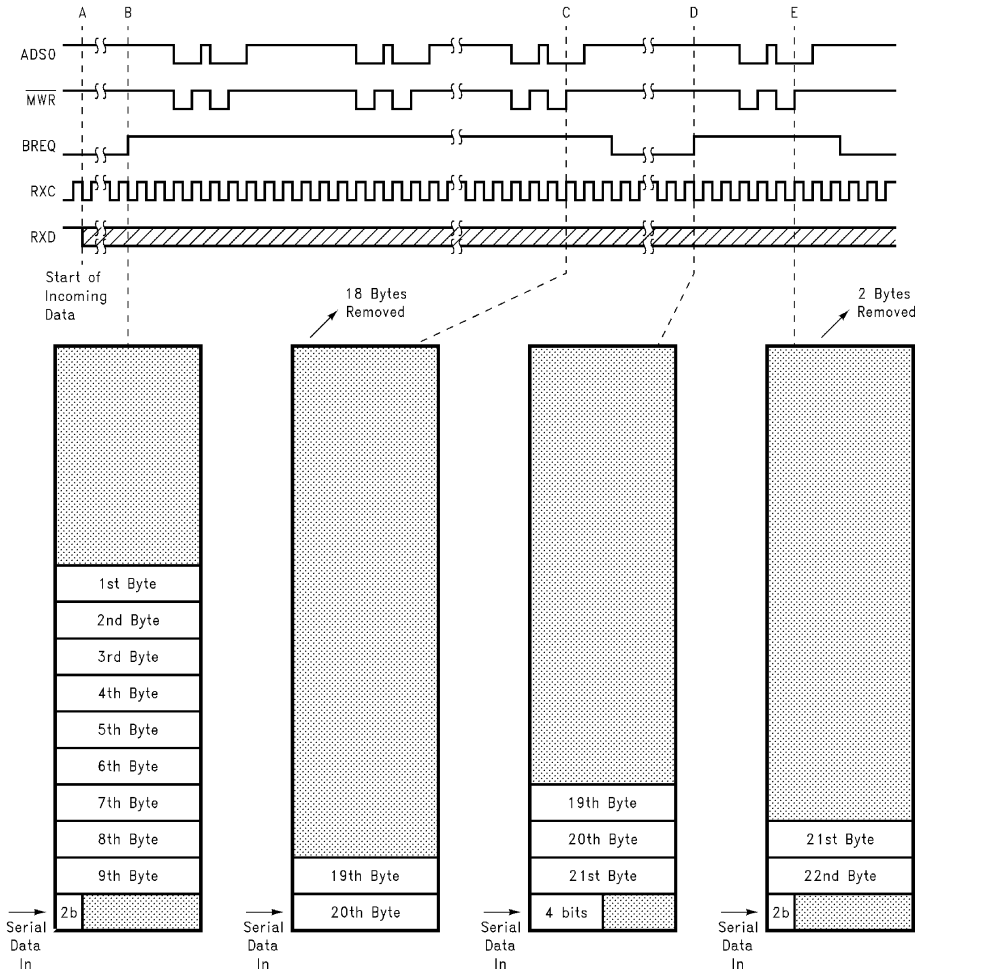

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FIGURE 5. Receive Packet—Byte Mode, 2 Byte Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 74 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 9 bursts of 2 bytes each into memory while shifting in 86 bits of data until $\overline{MWR}$ is deasserted (Point C). BREQ is asserted when there are 12 bytes and 4 bits in the FIFO (Point D). Two bytes are removed from the FIFO and stored in memory, while 6 bits are shifted into the FIFO until $\overline{MWR}$ is deasserted (Point E). D and E are repeated until the packet is complete.

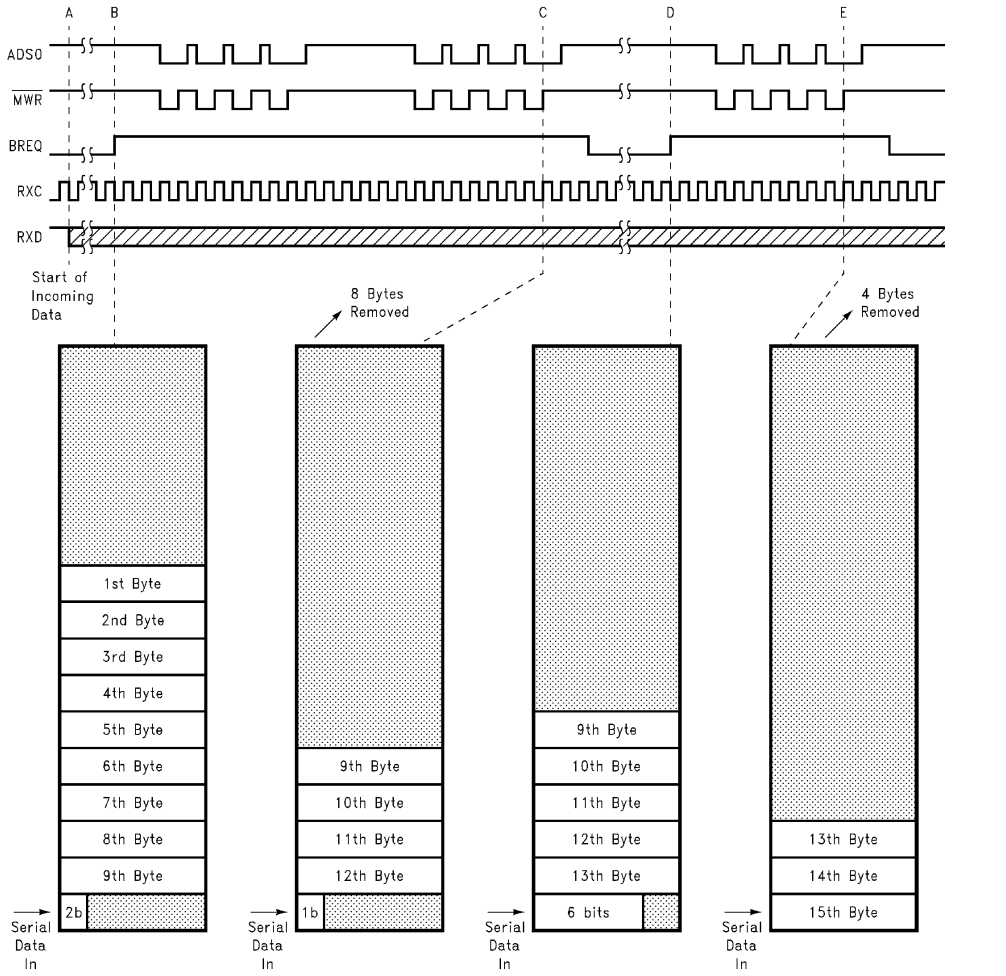

FIGURE 6. Receive Packet—Byte Mode, 4 Byte Threshold—First Situation

After the preamble and the SFD (Point A), the FIFO shifts in 74 ± 1 bit of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 2 bursts of 4 bytes each into memory while shifting in 23 bits of data until $\overline{\text{MWR}}$ is deasserted (Point C). BREQ is asserted when there are 5 bytes and 6 bits in the FIFO (Point D). Four bytes are removed from the FIFO and stored in memory, while 10 bits are shifted into the FIFO until $\overline{\text{MWR}}$ is deasserted (Point E). D and E are repeated until the packet is complete.

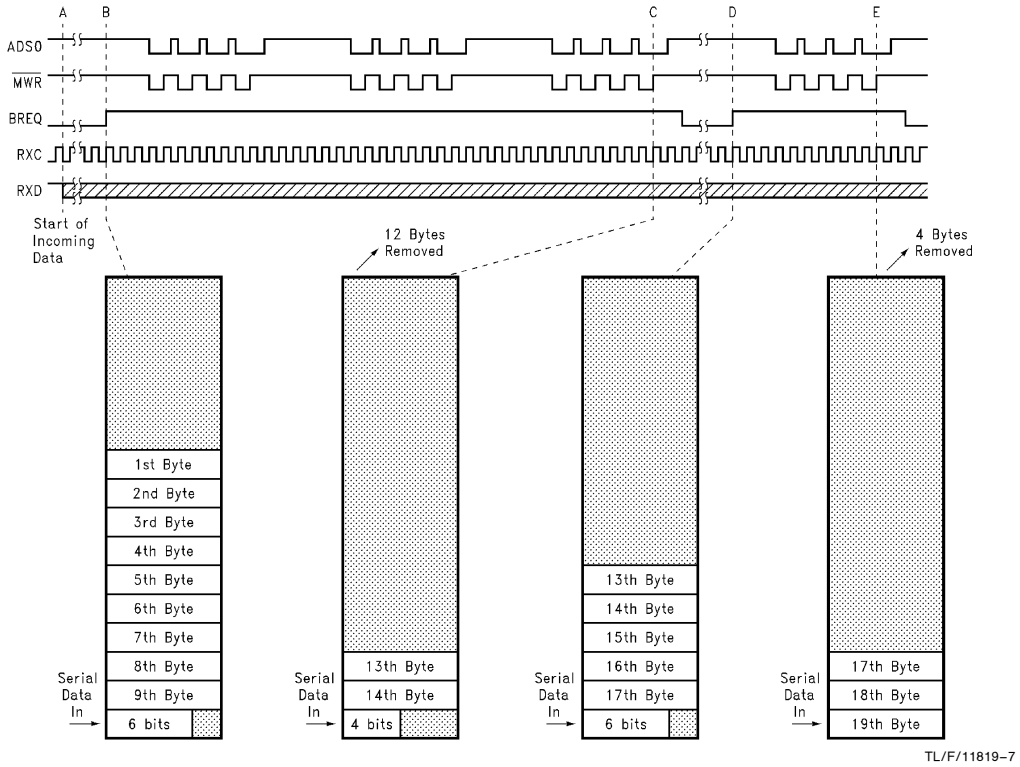

FIGURE 7. Receive Packet—Byte Mode, 4 Byte Threshold—Second Situation

After the preamble and the SFD (Point A), the FIFO shifts in 78 ± 1 bit of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 3 bursts of 4 bytes each into memory while shifting in 38 bits of data until $\overline{MWR}$ is deasserted (Point C). BREQ is asserted when there are 5 bytes and 6 bits in the FIFO (Point D). Four bytes are removed from the FIFO and stored in memory, while 10 bits are shifted into the FIFO until $\overline{MWR}$ is deasserted (Point E). D and E are repeated until the packet is complete.

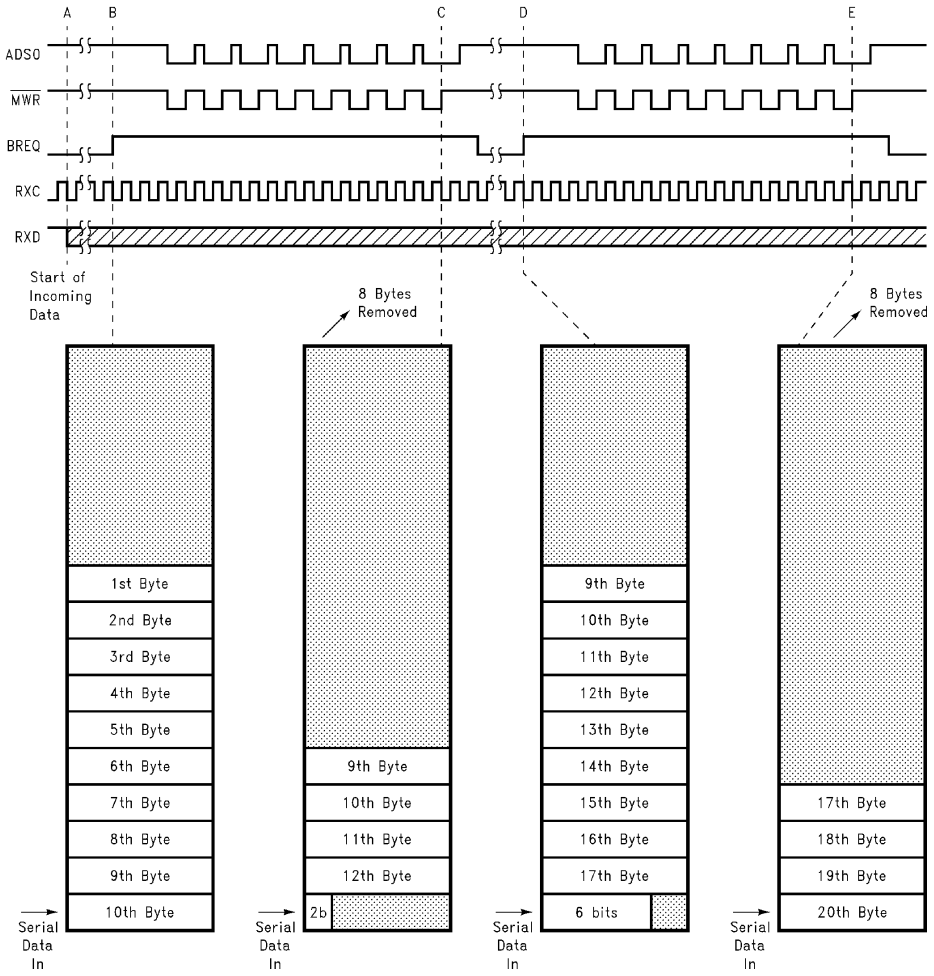

FIGURE 8. Receive Packet—Byte Mode, 8 Byte Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 80 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 1 burst of 8 bytes into memory while shifting in 18 bits of data until $\overline{\text{MWR}}$ is deasserted (Point C). BREQ is asserted when there are 9 bytes and 6 bits in the FIFO (Point D). Again, 8 bytes are removed from the FIFO and stored in memory, while 10 bits are shifted into the FIFO until $\overline{\text{MWR}}$ is deasserted (Point E). D and E are repeated until the packet is complete.

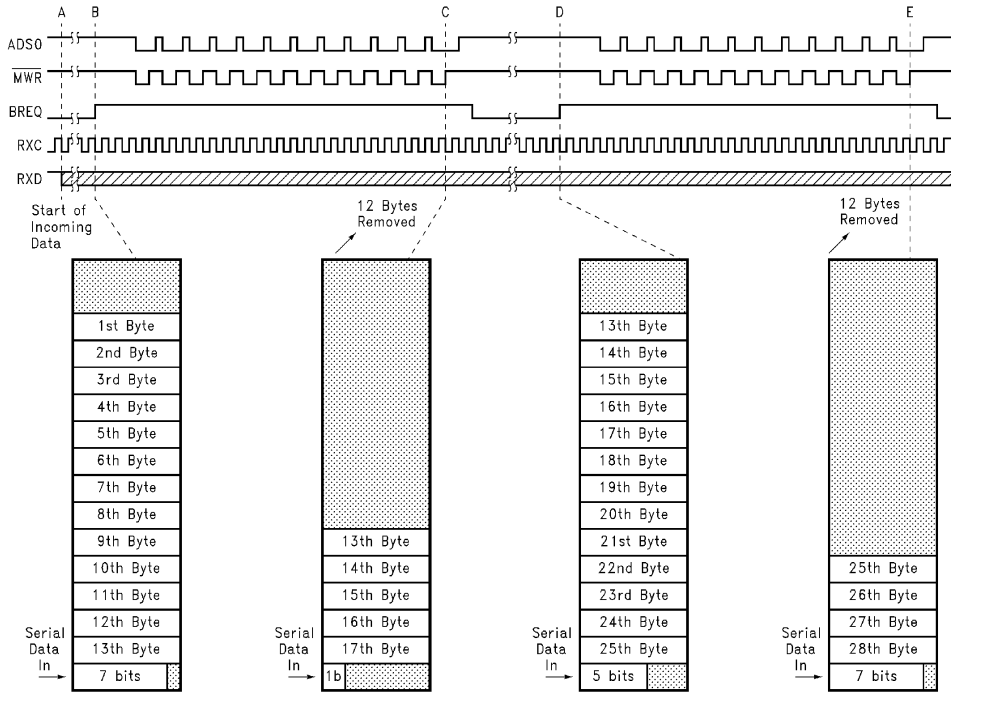

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FIGURE 9. Receive Packet—Byte Mode, 12 Byte Threshold

After the preamble and the SFD (Point A), the FIFO shifts in 111 ± 2 bits of data (depending on the location of the SFD with respect to t1 of the DMA sequence) before BREQ is asserted (Point B). The FIFO transfers 1 burst of 12 bytes into memory while shifting in 26 bits of data until $\overline{\text{MWR}}$ is deasserted (Point C). BREQ is asserted when there are 13 bytes and 5 bits in the FIFO (Point D). Again, 12 bytes are removed from the FIFO and stored in memory, while 26 bits are shifted into the FIFO until $\overline{\text{MWR}}$ is deasserted (Point E). D and E are repeated until the packet is complete.

TRANSMIT PACKET

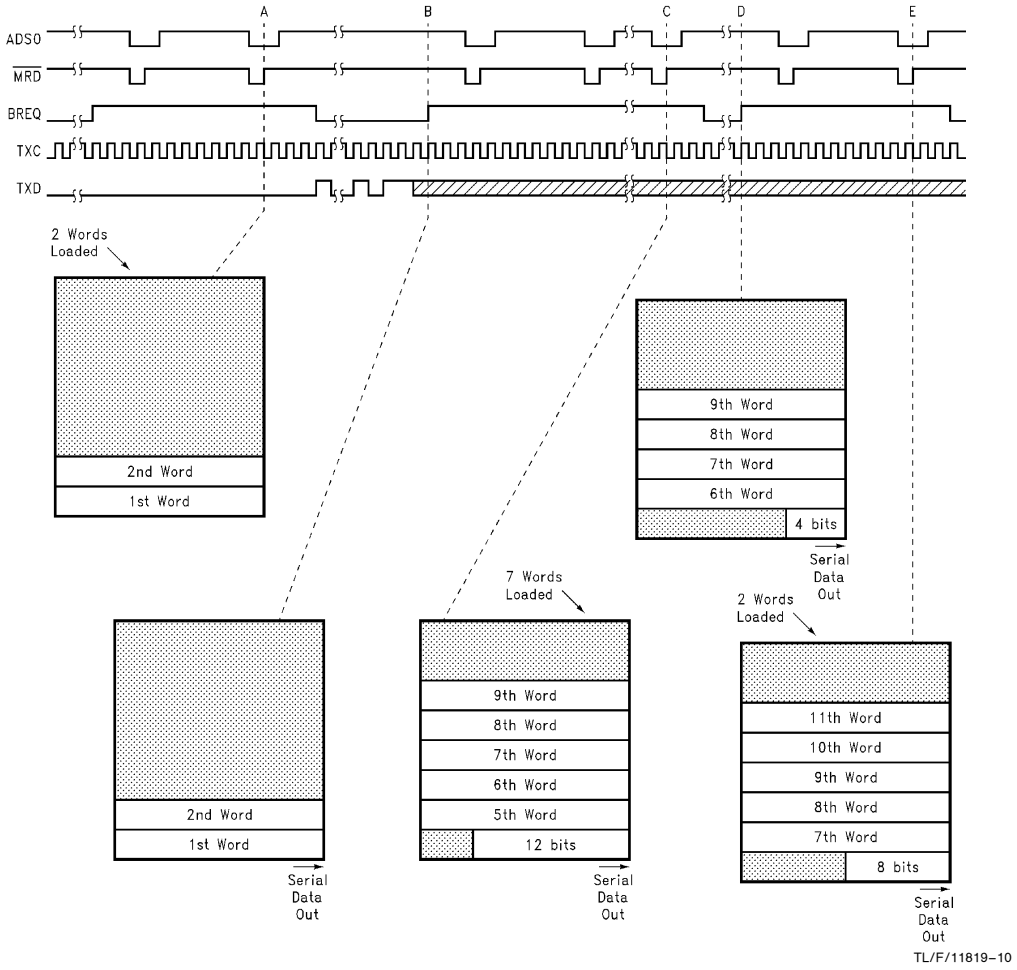

FIGURE 10. Transmit Packet—Word Mode, 1 Word Threshold

The FIFO prefetches 2 words from memory (point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO, and BREQ is asserted (Point B). During this burst, 7 words are loaded into the FIFO from memory while 52 bits are shifted out until $\overline{\text{MRD}}$ is deasserted (Point C). The next BREQ comes when there are 4 words and 4 bits in the FIFO (Point D). Two words are loaded into the FIFO from memory while 12 bits are shifted out (Point E). D and E are repeated until the packet is complete.

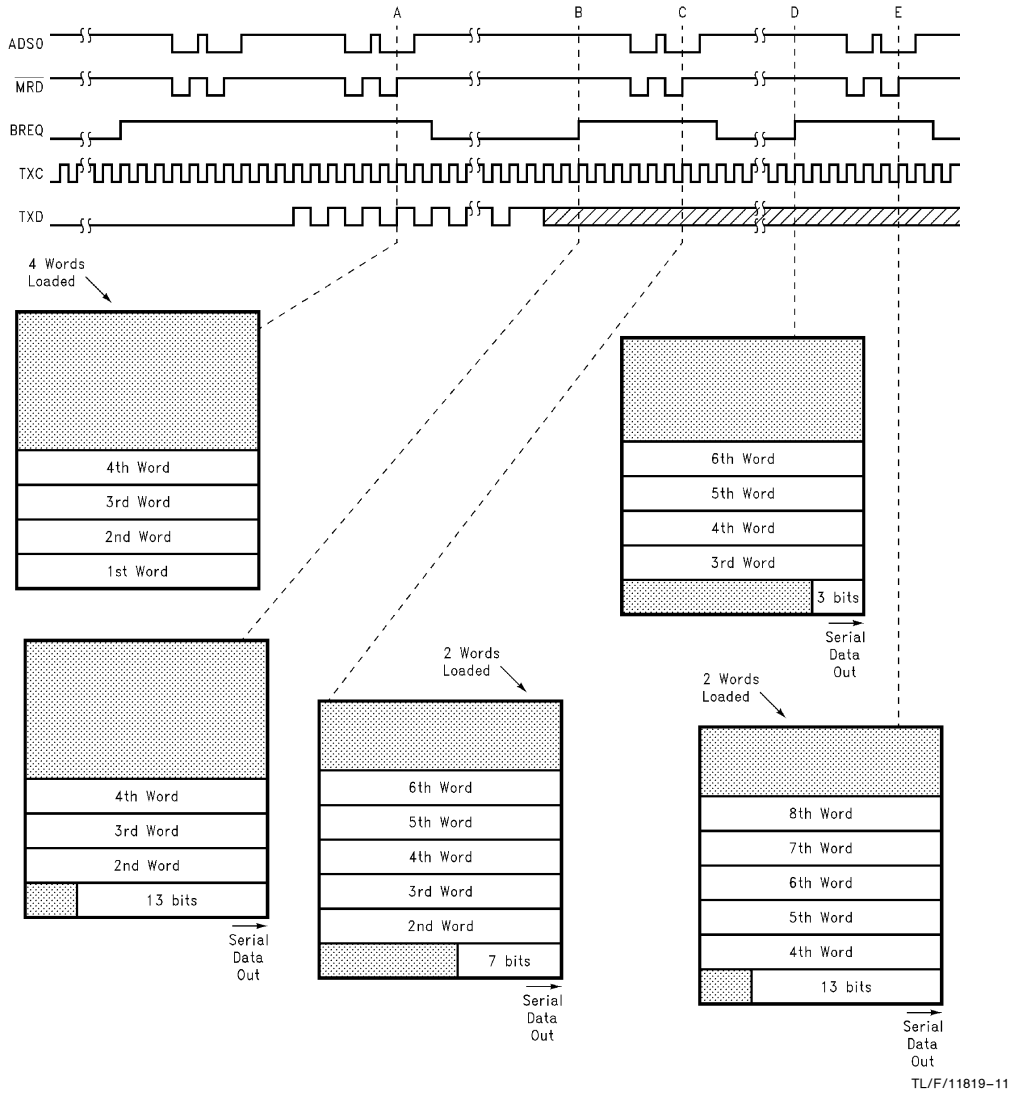

FIGURE 11. Transmit Packet—Word Mode, 2 Word Threshold

The FIFO prefetches 2 bursts of 2 words each from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 3 bits are shifted out, BREQ is asserted (Point B). During this burst, 2 words are loaded into the FIFO from memory while 6 bits are shifted out until $\overline{MRD}$ is deasserted (Point C). The next BREQ comes when there are 4 words and 3 bits in the FIFO (Point D). Again, 2 words are loaded into the FIFO from memory while 6 bits are shifted out (Point E). D and E are repeated until the packet is complete.

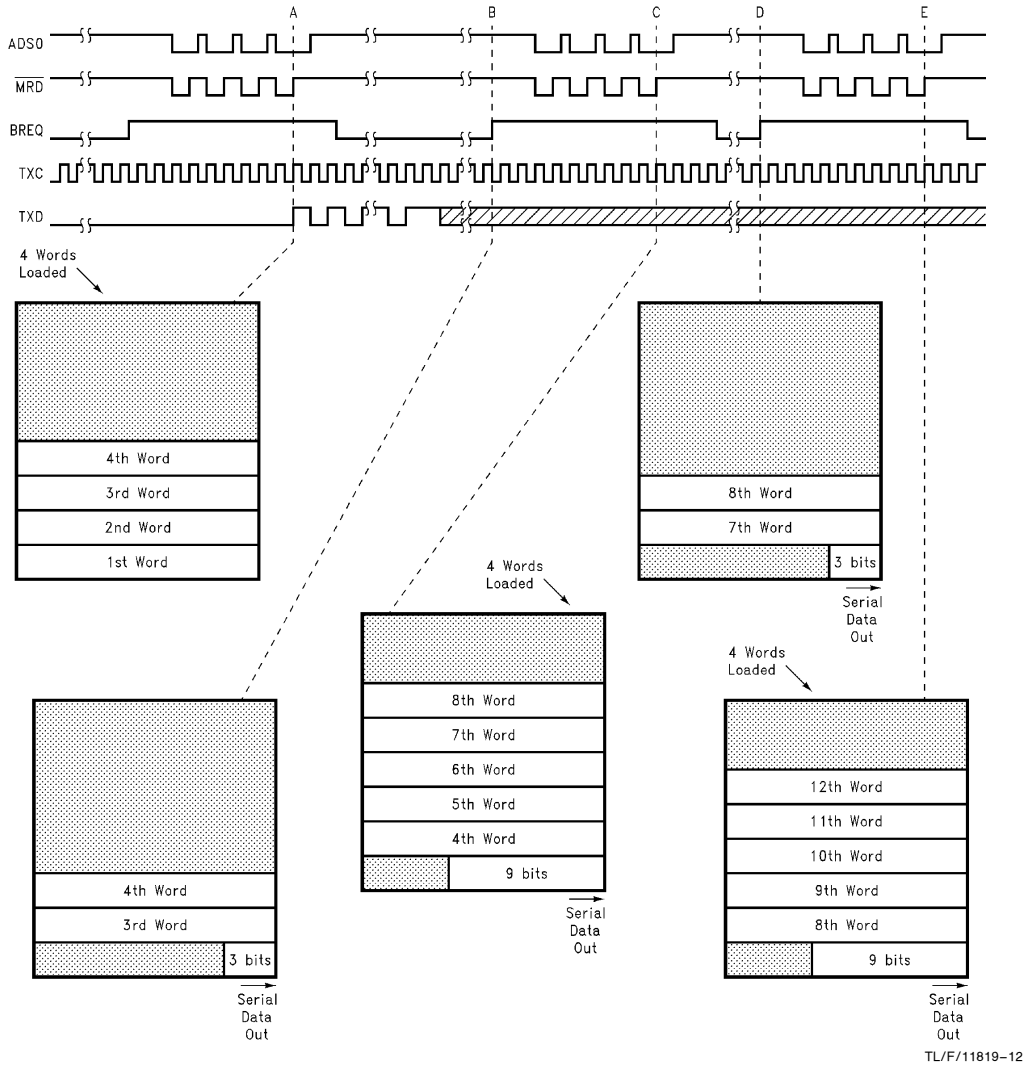

FIGURE 12. Transmit Packet—Word Mode, 4 Word Threshold

The FIFO prefetches 4 words from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 29 bits are shifted out, BREQ is asserted (Point B). During this burst, 4 words are loaded into the FIFO from memory while 9 bits are shifted out until $\overline{\text{MRD}}$ is deasserted (Point C). The next bus request comes when there are 2 words and 3 bits in the FIFO (Point D). Again, 4 words are loaded into the FIFO from memory while 9 bits are shifted out (Point E). D and E are repeated until the packet is complete.

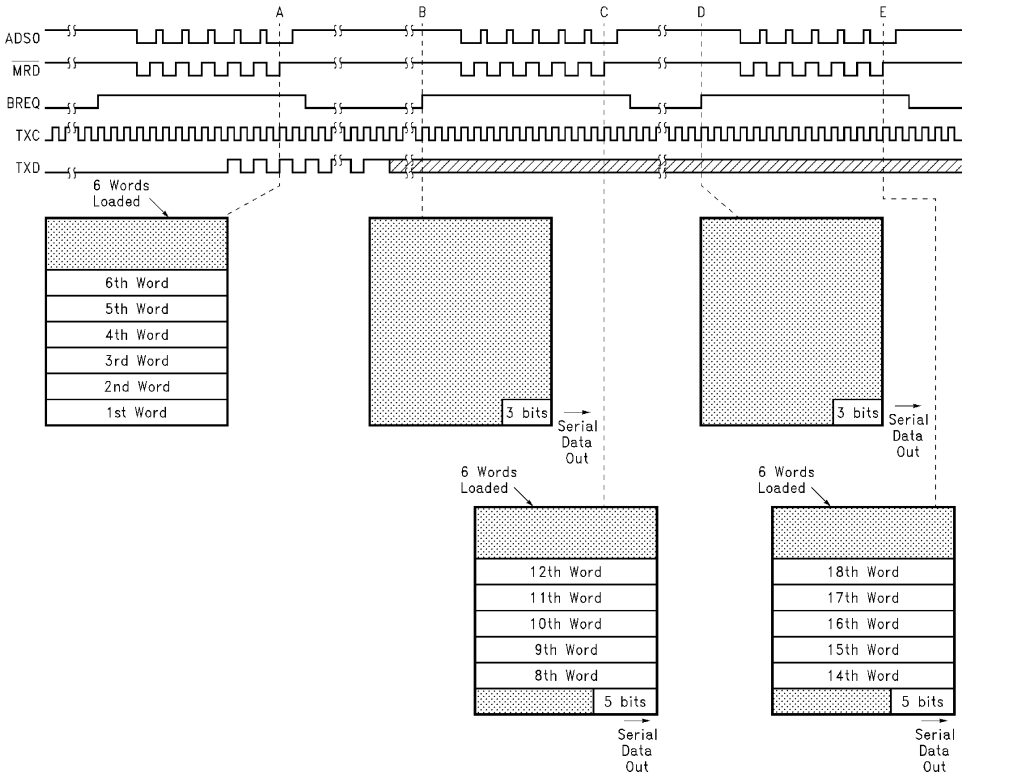

FIGURE 13. Transmit Packet—Word Mode, 6 Word Threshold

The FIFO prefetches 6 words from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 93 bits are shifted out, BREQ is asserted (Point B). During this burst, 6 words are loaded into the FIFO from memory while 14 bits are shifted out until $\overline{\text{MRD}}$ is deasserted (Point C). The next bus request comes when there are 3 bits in the FIFO (Point D). Again, 6 words are loaded into the FIFO from memory while 14 bits are shifted out (Point E). D and E are repeated until the packet is complete.

Note: At Point B, the 7th word is latched in approximately 10 ns before its first bit is clocked out. Occasionally, 94 bits will be shifted out before the first BREQ. In this case, the first bit of the 7th word and every 6th word from then on will be corrupted. Since no error occurs, this mode should not be used.

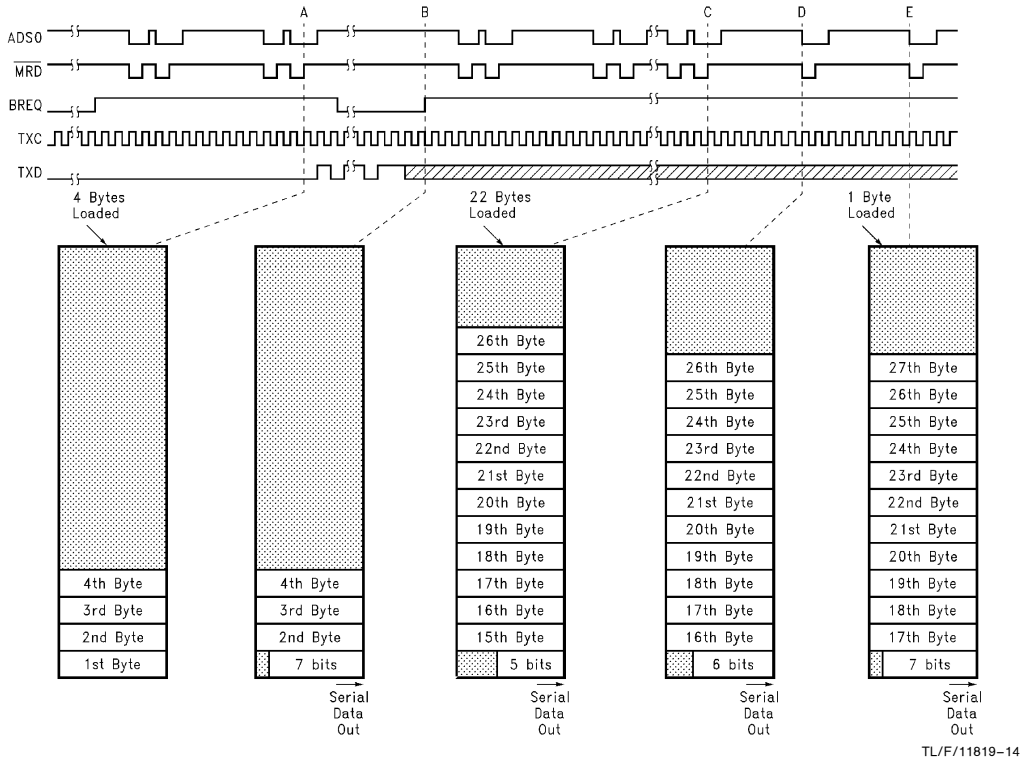

FIGURE 14. Transmit Packet—Byte Mode, 2 Byte Threshold

The FIFO prefetches 2 bursts of 2 bytes each from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 1 bit is shifted out, BREQ is asserted (Point B). Eleven bursts of two bytes each are loaded into the FIFO from memory while 106 bits are shifted out (Point C). At this point the bursts become one byte instead of two bytes (Point D). The FIFO loads 1 byte from memory while 7 bits are shifted out (Point E). D and E are repeated until the packet is complete.

Note: BREQ remains asserted until the entire packet is transmitted.

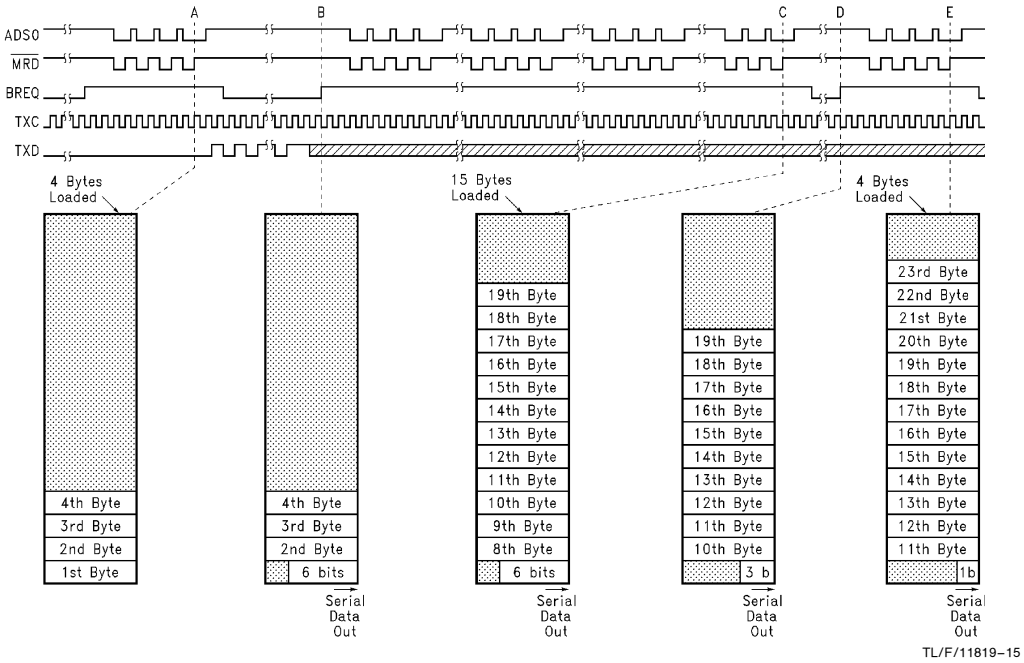

FIGURE 15. Transmit Packet—Byte Mode, 4 Byte Threshold

The FIFO prefetches 4 bytes from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 1 bit is shifted out, BREQ is asserted (Point B). Four bursts of 4, 4, 4, and 3 bytes, respectively, are loaded into the FIFO from memory while 49 bits are shifted out until $\overline{\text{MRD}}$ is deasserted (Point C). The next bus request comes when there are 10 bytes and 3 bits in the FIFO (Point D). Four bytes are loaded into the FIFO from memory while 10 bits are shifted out (Point E). D and E are repeated until the packet is complete.

Note: Some samples prefetched two bursts of 4 bytes each, and only 2 bursts of 4 bytes each were loaded into the FIFO between Points B and C. Both the cases sometimes had bursts of 3 bytes after point D, continuing until the packet is completed. A pattern could not be developed. This does not corrupt any bits and no error occurs.

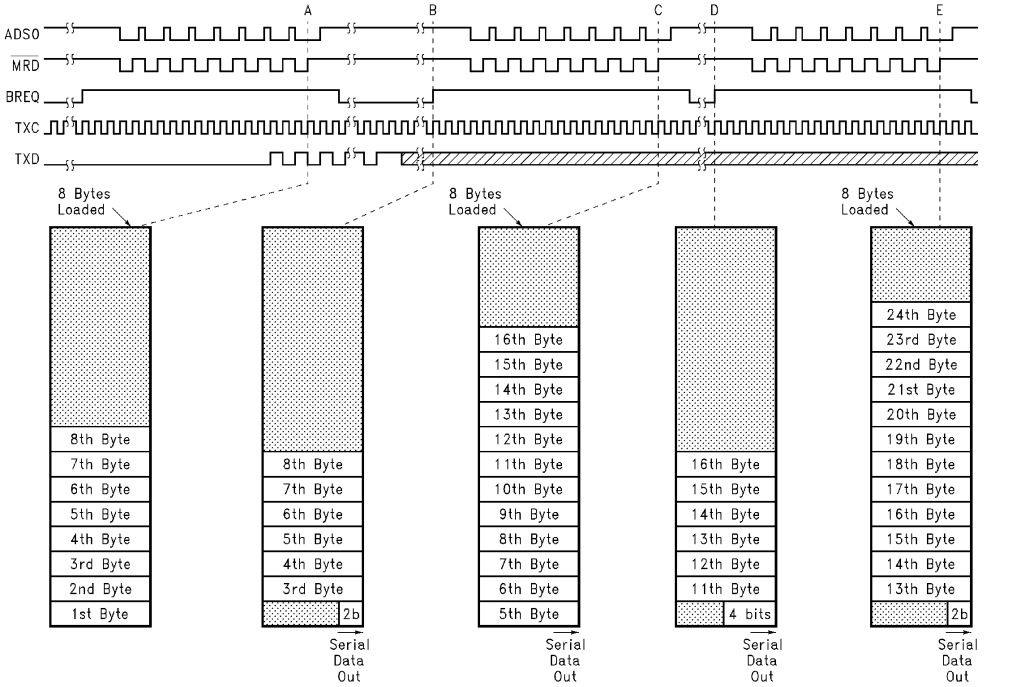

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FIGURE 16. Transmit Packet—Byte Mode, 8 Byte Threshold

The FIFO prefetches 8 bytes from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 22 bits are shifted out, BREQ is asserted (Point B). During this burst, 8 bytes are loaded into the FIFO from memory while 18 bits are shifted out until $\overline{MRD}$ is deasserted (Point C). The next bus request comes when there are 6 bytes and 4 bits in the FIFO (Point D). Again, 8 bytes are loaded into the FIFO from memory while 18 bits are shifted out (Point E). D and E are repeated until the packet is complete.

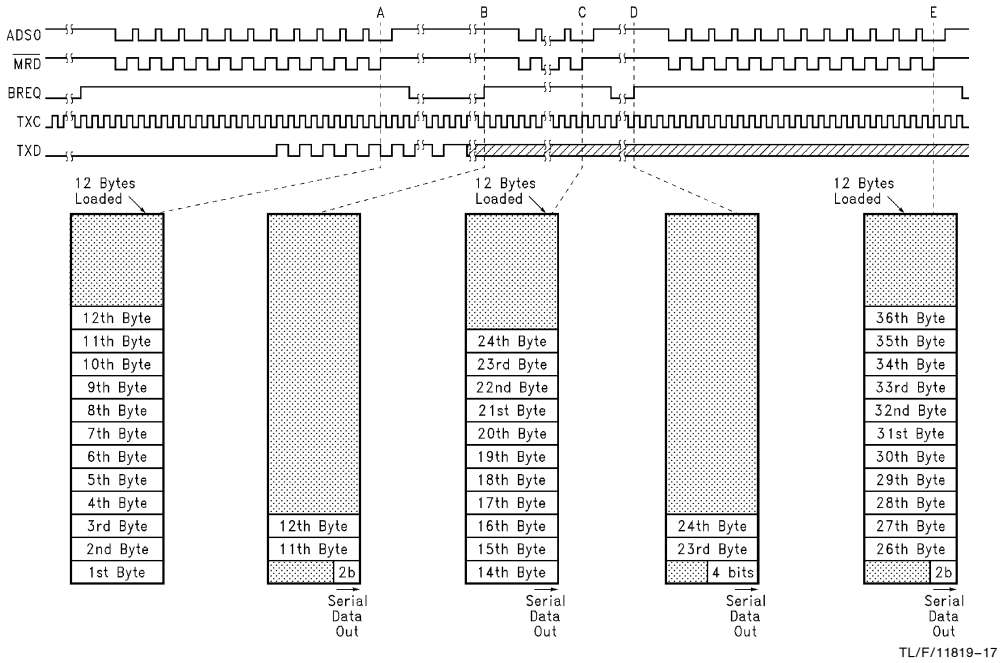

FIGURE 17. Transmit Packet—Byte Mode, 12 Byte Threshold

The FIFO prefetches 12 bytes from memory (Point A). The preamble starts during these prefetches. After the preamble and the Start of Frame Delimiter are transmitted, data is shifted out of the FIFO. After 78 bits are shifted out, BREQ is asserted (Point B). During this burst, 12 bytes are loaded into the FIFO from memory while 26 bits are shifted out until $\overline{\text{MRD}}$ is deasserted (Point C). The next bus request comes when there are 2 bytes and 4 bits in the FIFO (Point D). Again, 12 bytes are loaded into the FIFO from memory while 26 bits are shifted out (Point E). D and E are repeated until the packet is complete.

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