# ENEL 617 WINTER 2017 PROJECT REPORT

Millimeter-Wave Double Balanced Gilbert Mixer

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# 1 PROJECT MOTIVATION

A double balanced mixer that would be used as part of a BPSK Modulator circuit to generate a spread spectrum radar waveform in the automotive frequency band (77-81 GHz) is presented. A similar modulator that uses a double-balanced mixer is described in [3]. The original design benchmarks for this mixer and the achieved final results are outlined in Table 1.

| Parameter | Original Targets | Achieved |
|---|---|---|
| Supply Voltage | 1.8V | 0.85V |
| Power Consumption | 5mW | ≈ **4.8mW** |
| Gain (dB) | 5 | ≈ **-13 dB** |
| Input Match | 50Ω | **45.5 + j0.1Ω** |
| Output Match | 730Ω | **48.9 + j0.1Ω** |
| NF | 10dB | ≈ **16 dB** |
| P1dB | – | ≈ 1.5dB |
| IP3 | – | ≈ 9.5dB |

Table 1: Mixer Design Targets and Achieved

The original values were generated based on a few simple simulations/calculations and a power budget provided by Dr. Belostotski. The power budget was the control variable that is set as an absolute requirement. Once the Id-gm characteristics were understood from simulation, the gain estimate was calculated using the following equation.

$$G = \frac{2}{\pi} \frac{R_L}{R_s + \frac{1}{g_m}}; \tag{1}$$

The exact values including plots for the final results will be clearly outlined. Furthermore, deviations from original to achieved results will be described in detail. A different design topology was used in the final design than in the original biased circuit used to calculate the conversion gain. Some targets (such as output impedance) were changed intentionally (for practical purposes) while other values were adjusted based on non-ideal aspects of the circuit. A

derivation of conversion gain will be provided in the theory of operation section. A suitable value of $R_L$ was chosen based on biasing and achieving high gain. The interest in this particular-type of radar stems from spread-spectrum technology's built in interference rejection, which is an indispensable feature for automotive radar. This type of radar has recently been demonstrated in SiGe technology [1, 4]. 65nm technology is chosen because the Figure of Merit, $f_T \approx 160GHz$, making it suitable for this millimeter-wave application.

**Note** that simulations are redone in Matlab for ease of viewing. Original plots from Cadence are available in the Appendix.

## 1.1 Radar Theory of Operation

To demonstrate how this mixer could be used in a practical application, the theory of the type of radar is discussed. A simplified block diagram of an example spread spectrum ranging system is shown in Figure 1. The BPSK modulator is used to spread the carrier with a pseudorandom code. The parameters of the code, which govern the LO mixing frequency, are designed to provide an adequate range resolution within the context of automotive radar. The achievable range resolution of the radar system is related to the chip rate (mixer LO) of the code through Equation 2. This is fairly intuitive as the frequency of this signal determines the time-resolution, thereby determining the resolution of range.

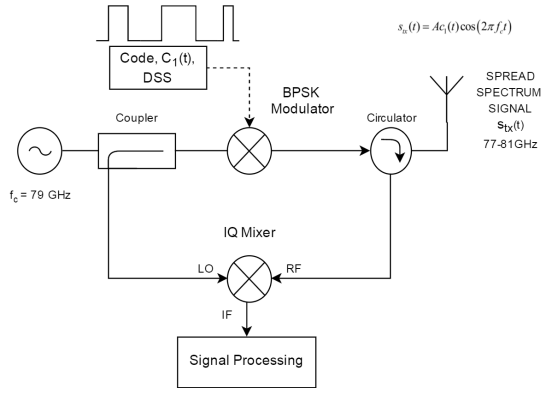


Figure 1: Radar Transceiver Block Diagram

$$d_{min} \leq \frac{c}{2f_c} \tag{2}$$

Therefore to achieve a $10cm$ range resolution a chip rate of $1.5GHz$ is chosen. The rest of the code can be designed by choosing the appropriate length.

$$T_p = \frac{N}{f_c} \tag{3}$$

and then achievable unambiguous range of the radar becomes

$$d_{max} \leq \frac{c}{2T_p} \tag{4}$$

Since the code is pseudorandom, the LO frequency could be any integer division of $1.5GHz$ i.e $0.75GHz, 0.5GHz$ etc. For the purposes of design we will simulate with just a $1.5GHz$ signal to demonstrate the maximum bandwidth of operation.

# 2 Mixer Theory of Operation

## 2.1 Basic Principle

The Gilbert Cell is a linear time-varying circuit. The concept behind this circuit is intuitive. The RF transistors act as amplifiers which change the input voltage to a current. The LO ports act as switches that commutate the output. This creates the time-domain multiplication function. Figure 2 demonstrates this concept.

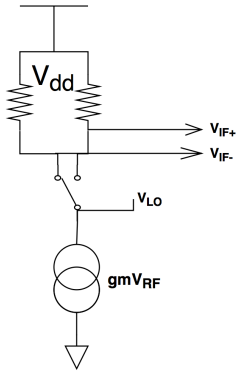


Figure 2: Mixer Theory

Since the Gilbert Cell is a double balanced, i.e. both RF and LO inputs are differential, the signals get subtracted out at IF. Therefore, there should be very little of the RF and LO frequencies present at the output.

## 2.2 Conversion Gain

As previously mentioned, the LO differential pairs essentially act as switches thereby allowing current to flow through resistors $R_1$ and $R_2$.

$$I_1 = I_{RF}F_T \tag{5}$$

and

$$I_2 = I_{RF}F_T(t - \frac{T_{LO}}{2}) \tag{6}$$

where $F_T$ is the square wave with period $T_{LO}$. The voltage at IF is equal to:

$$V_{IF} = V_{DD} - I_1R_L - (V_{DD} - I_2R_L) \tag{7}$$

$$V_{IF}(t) = I_{RF}(t)R_L[F_T(t - \frac{T_{LO}}{2}) - F_T] \tag{8}$$

Since $F_T$ is a square wave it can be seen that multiplying by $F_T(t - \frac{T_{LO}}{2}) - F_T$ is the same as multiplying by a square wave with amplitudes ranging from 1 to -1. Using the Fourier expansion of this square wave we get

$$V_{IF}(t) = I_{RF}(t)R_L[\frac{4}{\pi}cos(\omega_{LO}t)...] \tag{9}$$

$$V_{IF}(t) = \frac{2}{\pi}g_{m1}R_LV_{RF}cos((\omega_{RF} - \omega_{LO})t) \tag{10}$$

The peak conversion gain is then:

$$\frac{V_{IF,p}}{V_{RF,p}} = \frac{2}{\pi}g_{m1}R_L \tag{11}$$

If you have a source resistor then the gain drops proportionally, arriving at Equation 1.

## 2.3 Biasing

Biasing was done to maximize $g_m$ for gain while remaining under the power budget. With a $V_{dd}$ of 0.85V the total bias current can be calculated:

$$I_{DC} = \frac{5mW}{0.85V} = 5.9mA \tag{12}$$

## 2.4 RF Port Matching

Originally the RF port was going to be matched with a 50Ω source resistor. After understanding that the matching of this circuit could be designed using the same methodology as a source-degenerated LNA topology and also encountering voltage headroom problems, it became apparent that using source and gate inductors to match was the best option. The source inductor is used to match to 50Ω and the source and gate inductors combined are used to resonate out $C_{gs}$ (and in the case of high frequency many other parasitics).

$$50\Omega = \omega_T Ls \tag{13}$$

$$\frac{1}{w(sC_{gs} + C_{others})} = \omega(L_s + L_g) \tag{14}$$

For 65nm technology $\omega_T \approx 2\pi \times 160GHz$ [2]. This method of calculating input impedance is derived by ignoring the common gate transistor, other capacitances and $g_{ds}$ of the common source (RF) transistor.

This method is greatly oversimplified for an 80GHz circuit, seeing as there are parasitic capacitances and a finite output resistance. Therefore an attempt is made to create an improved input impedance model. This is discussed in Section 4.3

## 2.5 IF Port Matching

The output matching circuit was originally conceived to be resistive. Again, after learning more about the method of designing this circuit and the limitations involved, it became clear that an LC tank was required. Therefore the tank was designed to resonate at the desired frequency and the resistive load chosen to meet the output impedance requirement. Furthermore to get an output impedance as high as 700Ω a very large resistance would be required. This is because $g_{ds}$, which is in parallel with the load resistor, is of a very similar magnitude. As will be discussed in the simulation section, none of these values were as expected because of all the transistor parameters not taken into account.

## 2.6 Noise

Analyzing noise in active double-balanced mixers is complicated. The same methods studied for LNA noise optimization can be implemented however there are other variables that must be considered. As will be discussed in later sections, mixing with a sin wave (as is done in simulation) will increase noise figure. Furthermore, with this design there are quite a few resistors and no noise optimization is actually considered. Typical SSB of between 10-15dB is to be expected for this type of mixer therefore the achieved value seems acceptable.

## 2.7 Linearity

This design was largely done without taking linearity into consideration. The source inductor naturally provides some improvements because of negative feedback.

# 3 Design Variations and Final Circuit Schematic

## 3.1 Circuit Schematic

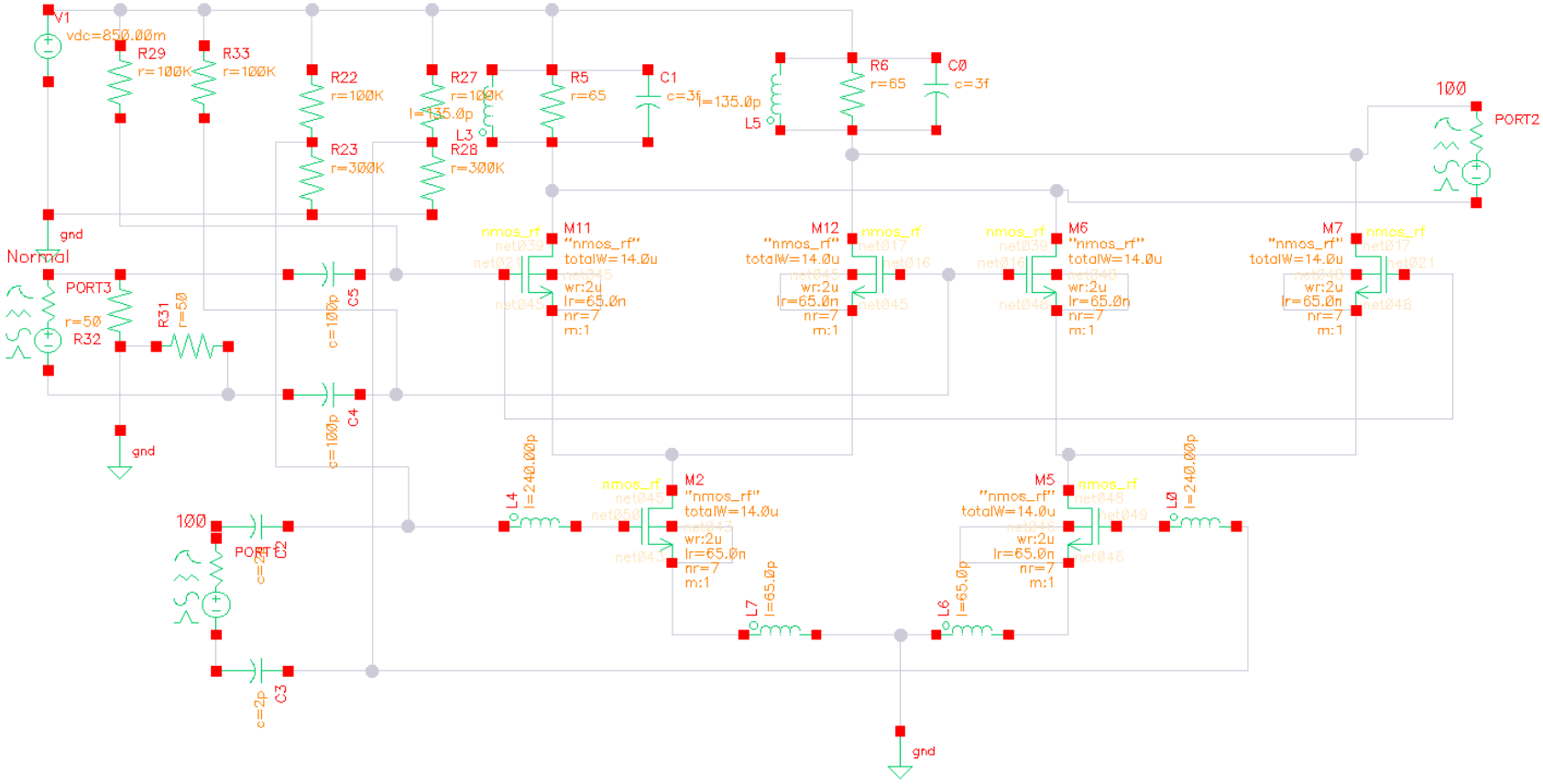


Figure 3: Final Design

| Component | Final Values |
|---|---|
| $W$, Transistor Width | $14\mu H$ |
| $L$, Transistor Length | $65nm$ |
| $L_s$, Source Inductor | $65pH$ |
| $L_g$, Gate Inductor | $240pH$ |
| $R_L$, Source Resistance | $65\Omega$ |
| $L_T$, Tank Inductor | $130pH$ |
| $C_T$, Tank Capacitor | $3pF$ |
| $C_c$, DC block/AC Short Cap | $100pF$ |
| $V_{bias,LO}$ | 0.85V |
| $V_{bias,RF}$ | 0.64V |

Table 2: Mixer Final Component Values

### 3.2 Overall Design Strategy Variation

At first the circuit was designed with a 1.8V power supply and a cascode type current mirror for biasing. However, this topology was causing many problems. First of all, the node at the current mirror had to maintain at least $\approx 0.4$V for the current mirror to function properly. Voltage headroom and being able to design for a $V_{od}$ of $\approx 0.1$V while also staying under the power budget of 5mW became an issue. Since, in this configuration, the current had to be kept low $V_{ds}$ was high, further aggravating the voltage headroom issue. Furthermore operating at 1.8V is not advised since that is the breakdown of 65nm technology.

After (a couple weeks of) using that topology, it became apparent that the best option was to scrap the current mirror. Dropping the supply voltage also allowed for more current, thereby reducing $V_{ds}$. An LC tank was also added to increase voltage headroom and it later became apparent that those components would also be required for output matching because of all the parasitics present. This then allowed for an increase in transistor width, which in turn increases the transconductance and thereby the gain. Originally with the power restriction, the largest achievable transconductance was $\approx 5mS$ and the overdrive voltage was $\approx 50mV$. After the topology change it was much easier to achieve an overdrive voltage of $\approx 100mV$ and $g_m \approx 14mS$. All final values are shown in Table 3.

### 3.3 Output Impedance Change

At first, an output resistance of $730\Omega$ was chosen to achieve the target gain of approximately 5dB based on calculations using Equation 1. This was not a very well thought out choice. It would be unusual to have such a high output impedance since the practical implementation of this would need to interface with other circuits (namely a PA). Therefore the target was reduced to $50\Omega$. The reduction in gain from this change was somewhat compensated by the fact that $g_m$ is now improved.

### 3.4 Conversion Gain Change

With the other changes outlined, it is now pertinent to recalculate conversion gain. Using Equation 11 and using values of $g_m = 14mS$ and $R_L = 50ohm$

$$G = 20\log(\frac{2}{\pi}g_m R_L) \approx -7dB \tag{15}$$

**Note** that this calculation is done with a square wave which maximizes conversion gain. During simulation, mixing is done with a sine wave and so there is a period of time where both transistors in the differential pair are on. This reduces gain and increases noise figure. We would then expect the simulated gain to be below this calculation. In fact, the gain equation is reduced proportionally to $\Delta T$, the time of overlapping drain current waveforms in the switching pair.

$$G = 2\pi g_m R_L(1 - \frac{2\Delta T}{T_{LO}}) \tag{16}$$

# 4 Simulated Results

## 4.1 Transistor Biasing and Power Consumption

Table 3: Final Values For DC Analysis

(a) RF Transistors

| Parameter | Value |
|---|---|
| $I_D$ | 2.819mA |
| $C_{gs}$ | 9.468fF |
| $C_{gd}$ | 3.613fF |
| $g_m$ | 14.94mA/V |
| $g_{ds}$ | 2.94mA/V |
| $V_{ds}$ | 331mV |
| $V_{gs}$ | 646mV |
| $V_{th}$ | 414mV |

(b) LO Transistors

| Parameter | Value |
|---|---|
| $I_D$ | 1.409mA |
| $C_{gs}$ | 8.754fF |
| $C_{gd}$ | 3.216fF |
| $g_m$ | 12.18mA/V |
| $g_{ds}$ | 1.38mA/V |
| $V_{ds}$ | 510mV |
| $V_{gs}$ | 511mV |
| $V_{th}$ | 402mV |

Overdrive voltage for LO transistors was lower than RF transistors. This is because it was important that the LO transistors would fall into triode and cutoff with the corresponding LO swing. The overdrive voltage for the RF transistors was designed high to get high transconductance while still remaining in saturation. The total current $I_{DC} = 2.819mA \times 2 = 5.638mA$ gives a power consumption of $P = 5.638mA \times 0.85V = 4.8mW$

## 4.2 Conversion Gain

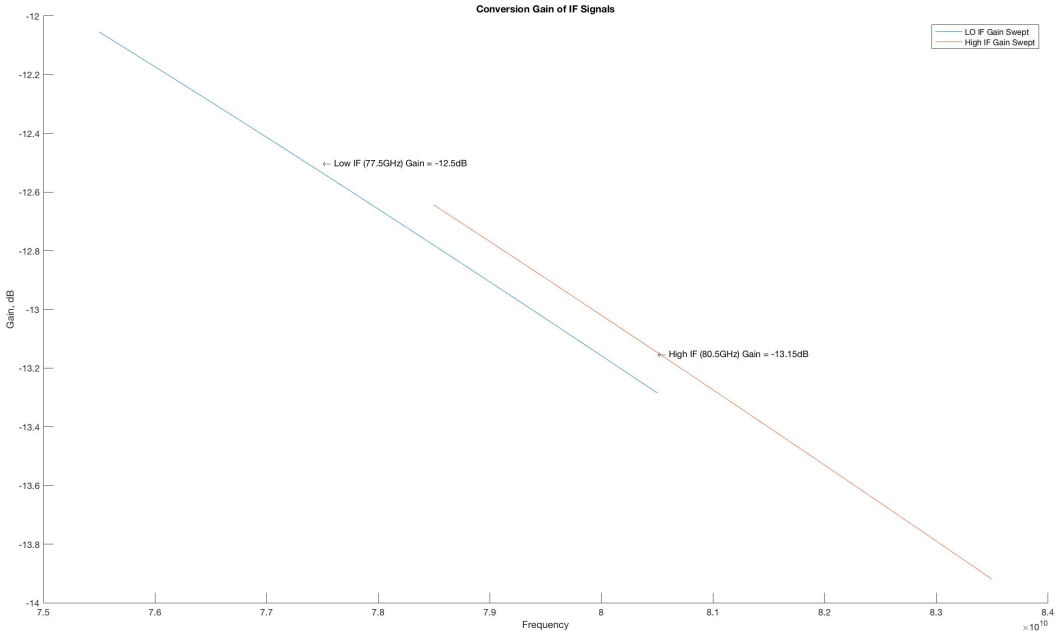


Figure 4: Swept Gain for Lo/Hi IF

The achieved conversion gain (once matched) is slightly lower then the calculated value based on Equation 16 as expected because of the slow switching of the LO transistors.
**Note** RMS spectrum is shown in the Appendix.

## 4.3 Input and Output Matching

### 4.3.1 Theory

As previously discussed, the source degenerated topology input impedance is defined by the simple circuit seen below.

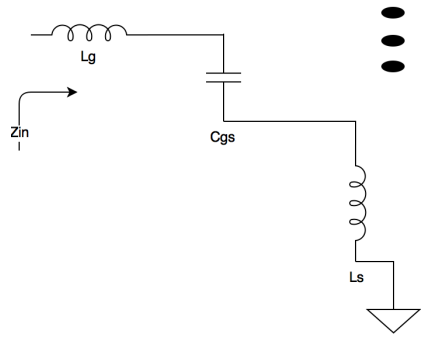


Figure 5: Simplified Input Impedance

From this model, Initial values of $Ls = 50pH$ and $L_g = 390pH$ are picked based on the simulated bias value of $C_{gs}$. As a side exercise, an attempt at producing an analytical improved impedance model for the cascode which considers $g_{ds}$ and $C_{gd}$ of both transistors was done and is shown in Appendix B. This model was then used in Matlab with chosen values of $L_s$ in an attempt to get an optimized answer as opposed to the oversimplified number produced by the source degenerated cadcode LNA model. In theory, once values of $L_s$ were analyzed then a more accurate value of $L_g$ could also be chosen based on the remaining reactance. However the calculations produced by this model and Matlab did not seem to be any closer than the original model. In the end, changing the values based on simulation seemed to be the only reliable method.

After iterative simulation the values of $Ls = 65pH$ and $L_g = 240pH$ were picked as shown in Table 2. These are relatively close to the original guess. It would be expected that the final gate inductance value would be lower than the initial guess because $C_{others}$ i.e. the parasitics would reduce the value of Equation 14.

### 4.3.2 Results

Good matching is achieved as shown in Figure 6. Several iterations of plotting the impedance on the Smith Chart tool in Cadence was used to achieve the required input match. The values for the output components are quite different then originally expected. The resistance is slightly higher (65 as opposed to 50). This can be explained by noting that $g_{ds}$ of the LO transistor is in parallel with $R_L$ therefore a higher Resistor value is needed to achieve 50Ω. The tank was originally designed using

$$\omega = \frac{1}{\sqrt{LC}}$$

with a chosen value of C = 3pF to start the Inductor value comes out to be approximately 1.3nH. However, after simulated the final value of the inductor chose was about 1/10th that value (Note Dr. Belostotski ignore the conversation we had about it being higher... I got it backwards). This makes sense because of all the parasitic capacitances that are present. The -10dB bandwidth for both S11 and S22 extends past the entire operating band.

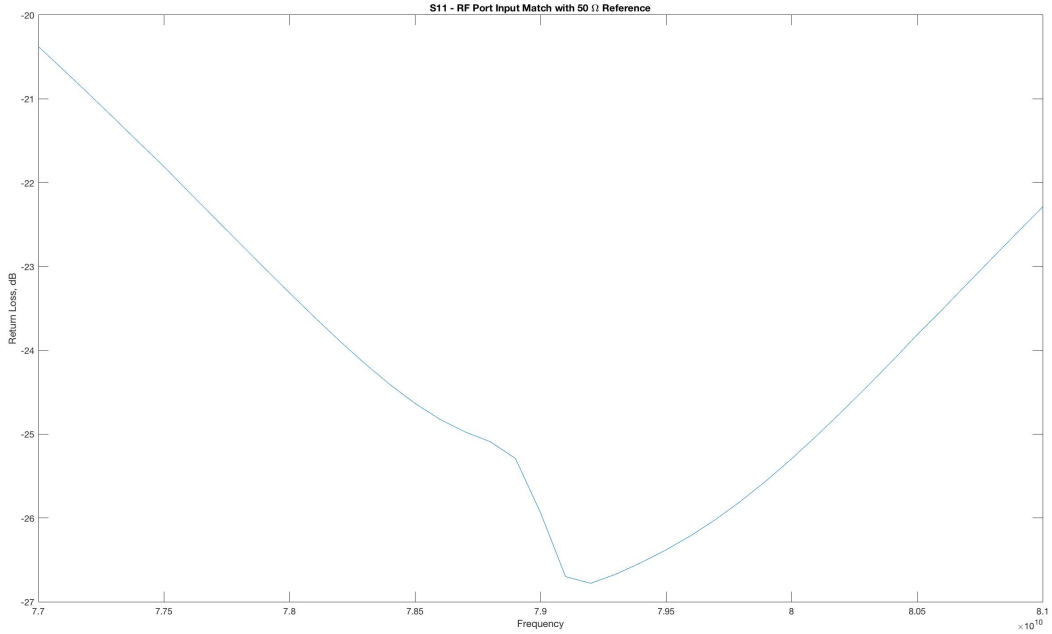


Figure 6: Final Return Loss of RF Port

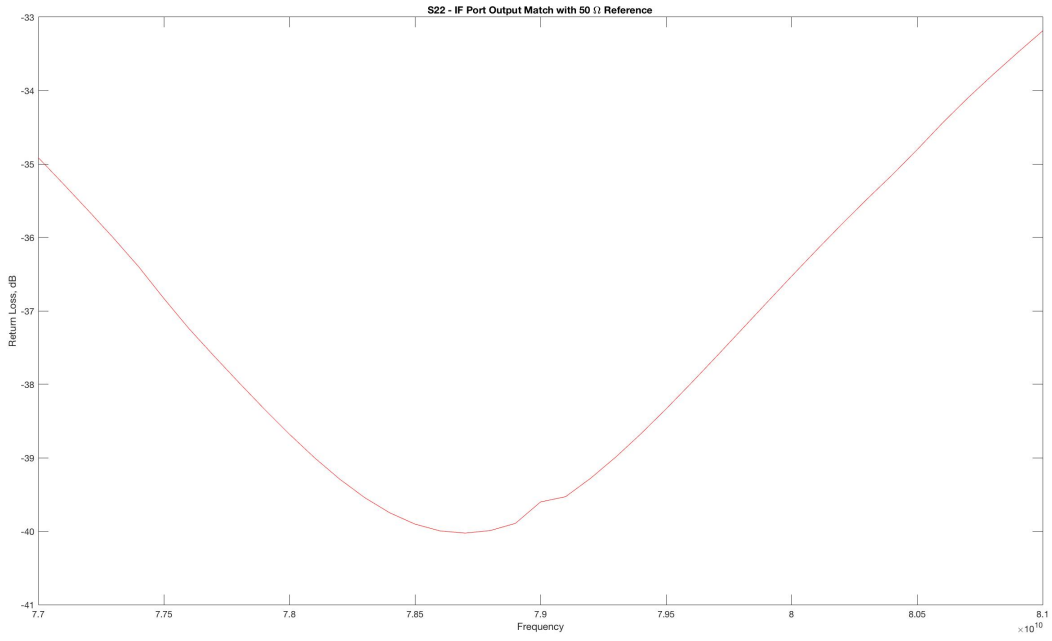


Figure 7: Final Return Loss of IF Port

The matching for the LO ports is simply done with two, 50Ω resistors. Simulations showed almost infinitely small return loss as expected.

## 4.4 Noise Figure

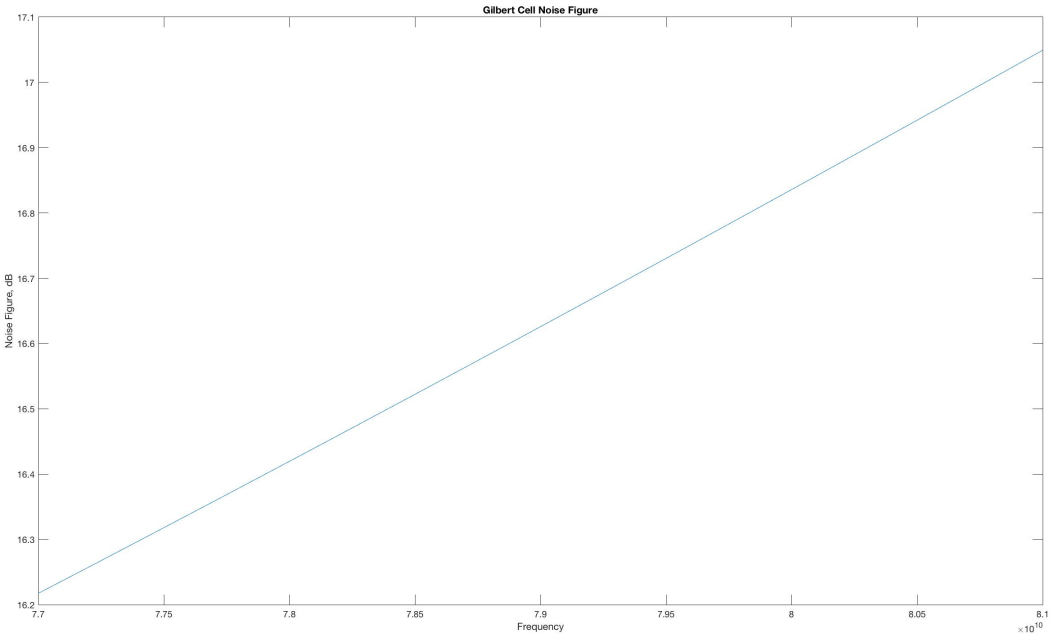


Figure 8: Final NF

## 4.5 P1dB & IP3

The simulated values for P1dB and IP3 seem reasonable. The power is compressed at $\approx$ 1dBm input and so this mixer could seemingly be used in the proposed implementation. Although much further system analysis would obviously be required. The estimate of $IIP3 \approx P1dB + 10dB$ seems to be relatively accurate.

# 5 Discussion & Future Improvements

The first goal of this project, which was to learn a lot, was certainly achieved. With regards to millimeter wave design it is clear that many of the design techniques/equations used at lower frequencies will not be very accurate. Additional un-idealities such as inductor Q and bulk modulation are not even taken into account in these simulations. For example, many iterations of S-Parameter analysis was required to get the circuit matched properly, particularly the output impedance which had values that were very different than initial estimates. It's apparent that the power budget would need to be increased to get reasonable gain. Furthermore, voltage headroom becomes an important consideration at millimeter wave because of the small breakdown voltage.

# 6 References


[1] Herman Jalli Ng, Reinhard Feger, and Andreas Stelzer. "A fully-integrated 77-GHz UWB pseudo-random noise radar transceiver with a programmable sequence generator in SiGe technology". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.8 (2014), pp. 2444–2455.

[2] Behzad Razavi. *RF Microelectronics (2Nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. 2nd. Upper Saddle River, NJ, USA: Prentice Hall Press, 2011. ISBN: 0137134738, 9780137134731.

[3] Bernd Schleicher, Çagri A Ulusoy, and Hermann Schumacher. "A biphase modulator circuit for impulse radio-UWB applications". In: *IEEE microwave and wireless components letters* 20.2 (2010), pp. 115–117.

[4] Saverio Trotta et al. "A 79GHz SiGe-bipolar spread-spectrum TX for automotive radar". In: *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*. IEEE. 2007, pp. 430–613.

# A Cadence Simulation Plots

## A.1 Conversion Gain

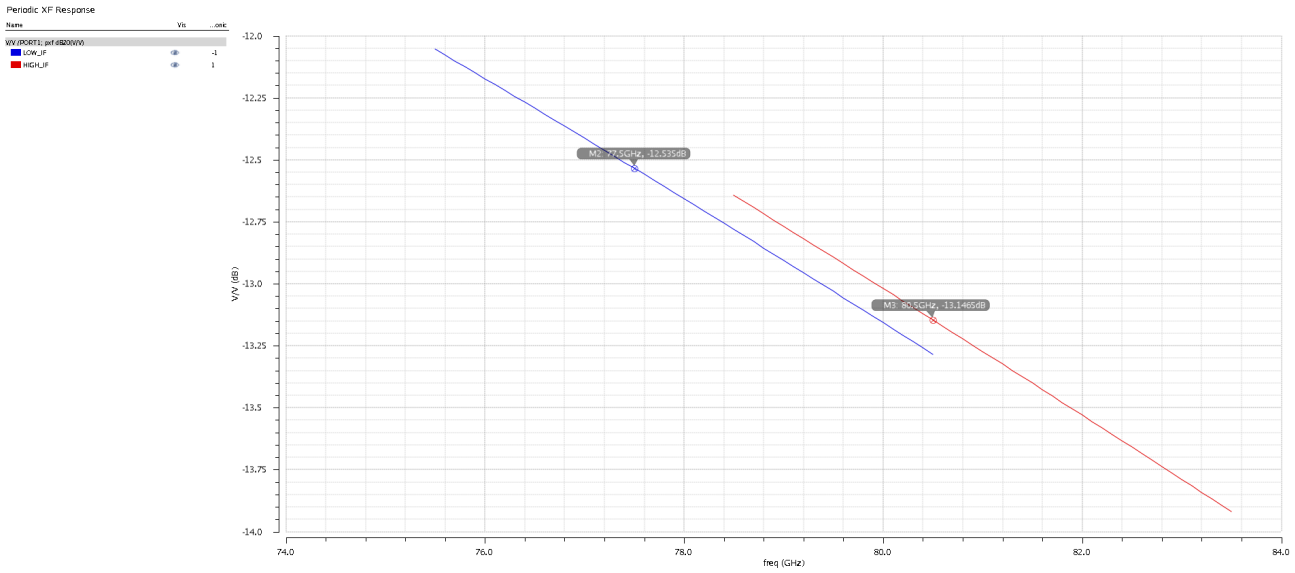


Figure 9: Conversion Gain Cadence

## A.2 RMS Spectrum

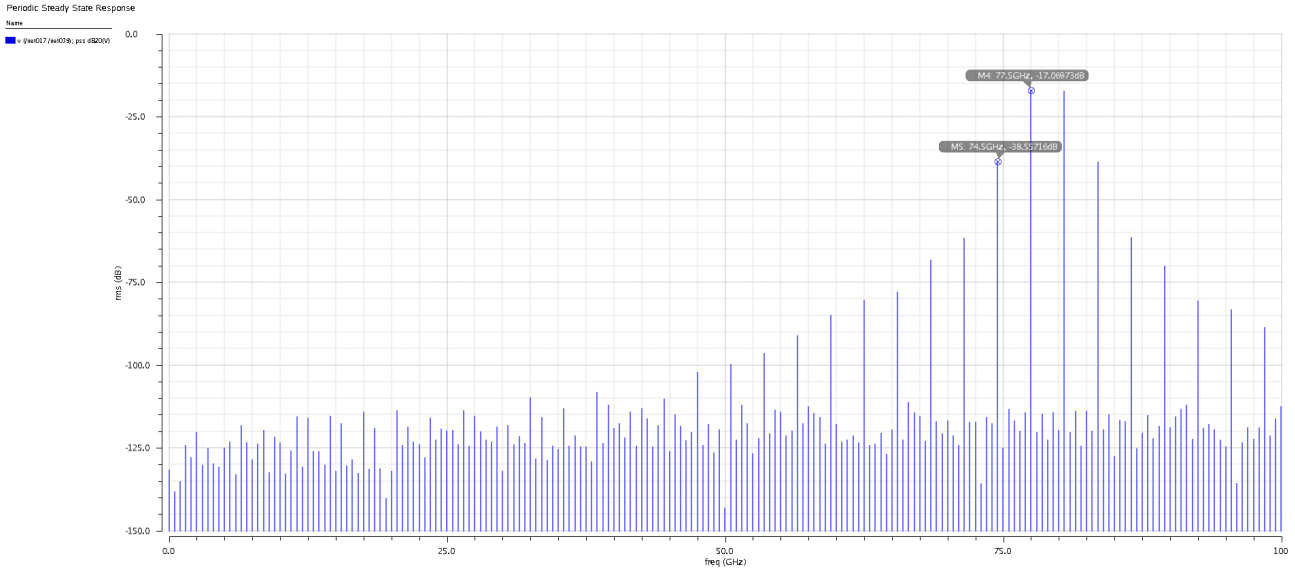


Figure 10: RMS Spectrum Cadence

## A.3 Noise Figure

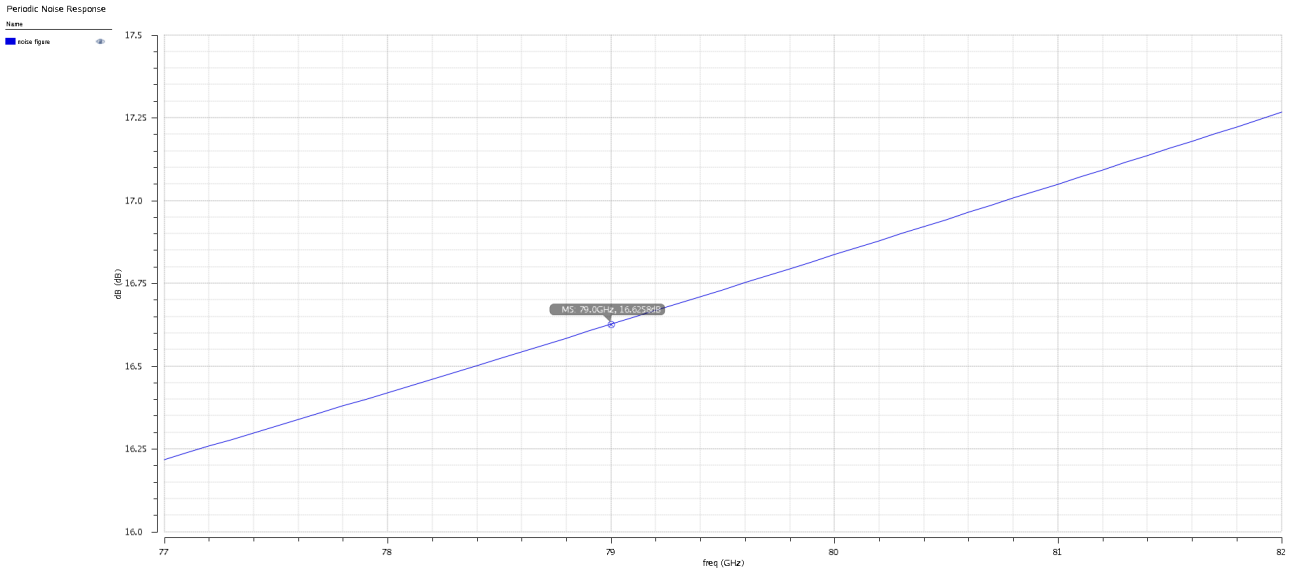


Figure 11: Noise Figure Cadence

## A.4 P1dB

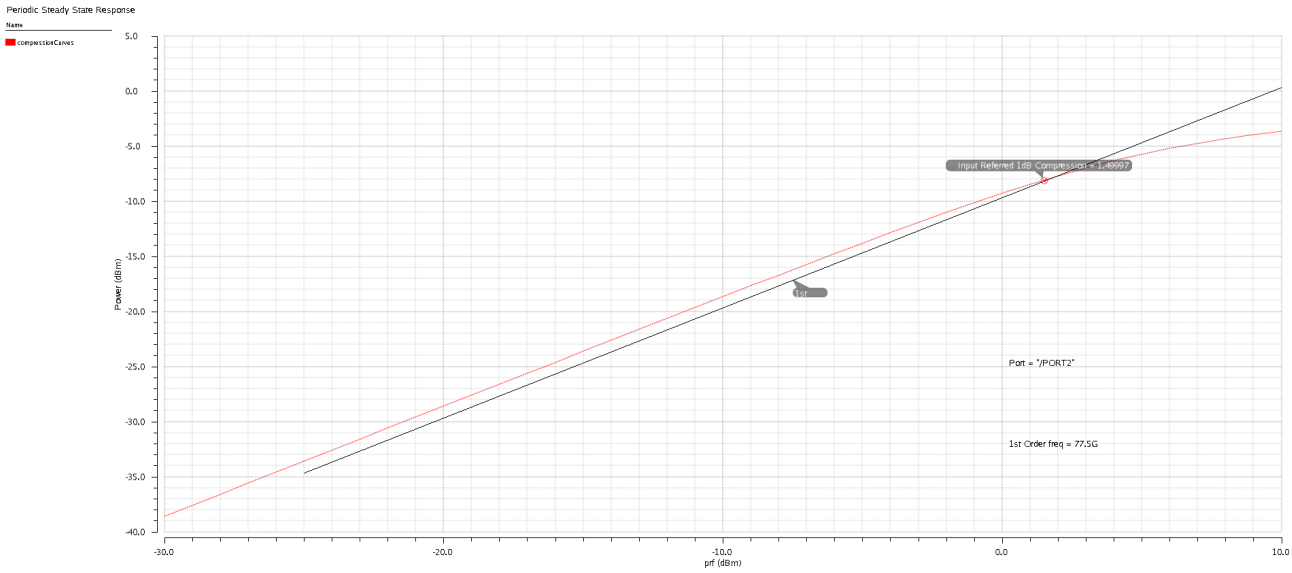


Figure 12: P1dB Cadence

## A.5 IP3

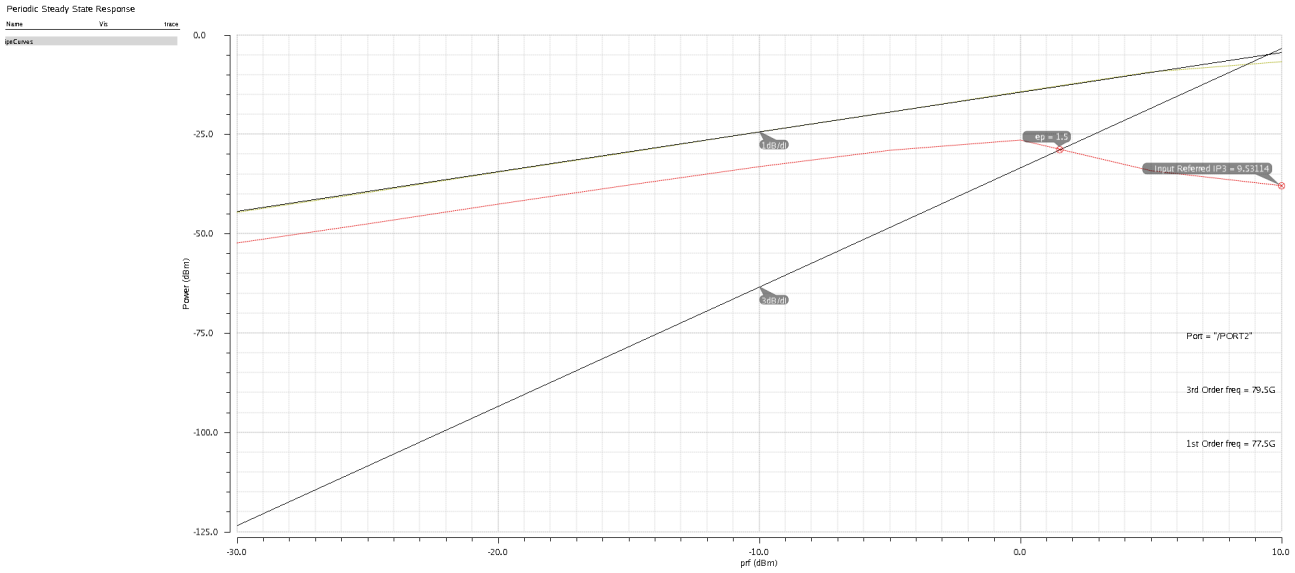


Figure 13: IP3 Cadence

## A.6 S11

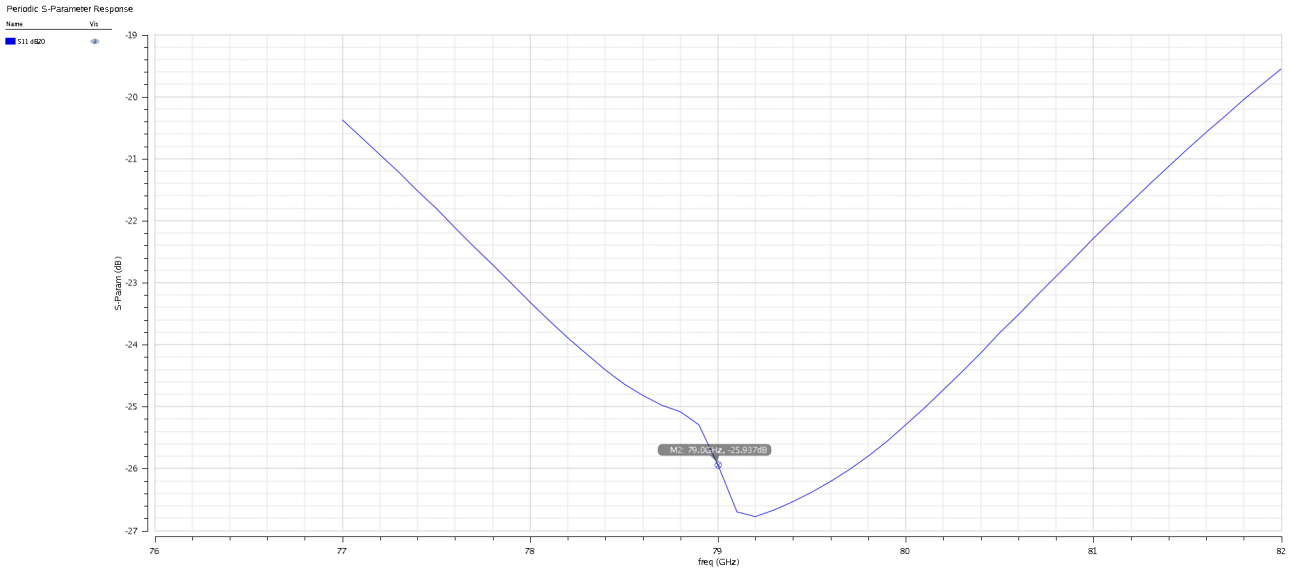


Figure 14: RF Port Match

## A.7 S22

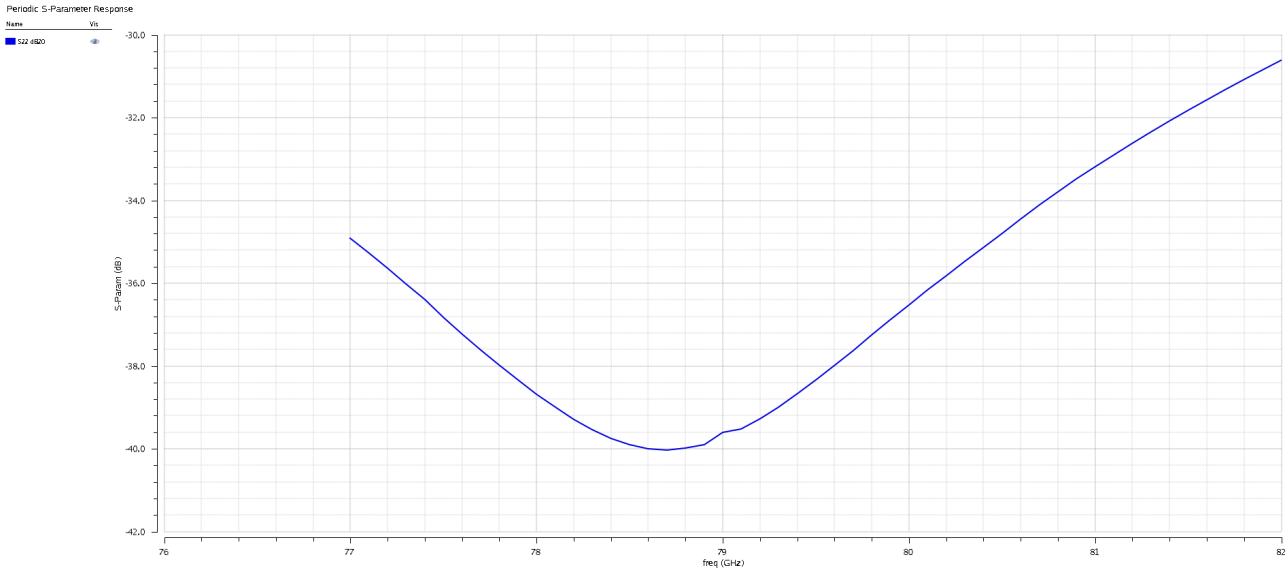


Figure 15: IF Port Match

# B Improved Impedance Model

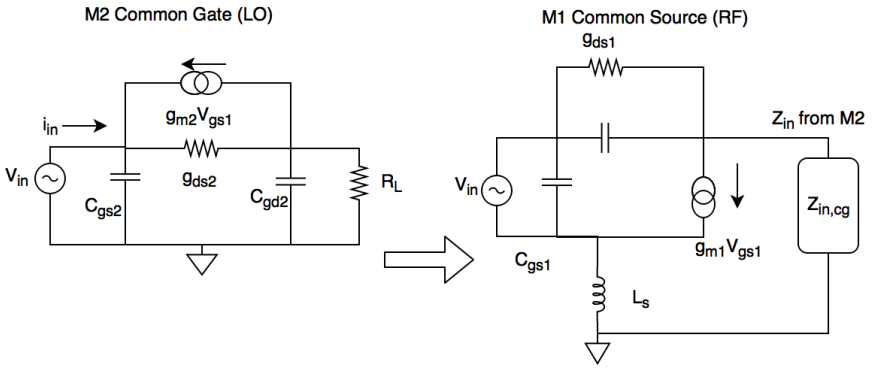


Figure 16: Small Signal Models for Transistors

First we take a look at the impedance looking into the common gate (LO) transistor. We'll call this transistor M2 as seen in Figure

$$i_{in} = V_{in}sC_{gs} + g_m V_{in} + (V_{in} - V_{out})g_{ds}$$

@ $V_{out}$

$$V_{out}(sC_{gd} + g_L + g_{ds}) + V_{out}g_L + (V_{out} - V_{in})g_{ds} = g_m V_{in}$$

$$Z_{in} = \frac{1}{sC_{gs} + g_m + g_{ds} - \frac{(g_m + g_{ds})g_{ds}}{g_{ds} + g_L + sC_{gd}}}$$

Now analyzing the impedance looking into the source degenerated common source (RF) transistor terminated with the impedance of the common gate we just found.

$$i_i n = (V_{in} - V_s)sC_{gs} + (V_{in} - V_{out})sC_{gd} + (V_{in} - V_{out})g_{ds}$$

@ $V_s$

$$(V_s - V_{in})sC_{gs} + V_s/L_s = (V_{in} - V_s)g_m$$

$$V_s = \frac{(sC_g s + g_m)V_{in}}{sC_{gs} + g_m + \frac{1}{sL_s}} = X \times V_{in}$$

@ $V_{out}$

$$V_{out}(y_{in}) + g_m V_{in} - g_m X V_{in} + V_{out}sC_{gd} - V_{in}sC_{gd} + V_{out}(g_{ds}) - V_{in}(g_{ds}) = 0$$

$$V_{out} = \frac{(g_m X + sC_{gd} + g_{ds} - g_m)V_{in}}{y_{in} + sC_{gd} + g_{ds}} = Y \times V_{in}$$

From here we can calculate the complete Input impedance looking into the RF port:

$$Z_{in,total} = \frac{1}{sC_{gs} - XsC_{gs} + sC_{gd} - YsC_{gd} + g_{ds} - Yg_{ds}}$$

With a given value of $L_s$ in Matlab it was possible to calculate the Real and Img impedances looking into the port. While this was an interesting exercise it did not prove to be any more accurate than the simplified method. This is likely because of all the other parasitics that are still not taken into account.