ENEL 617 WINTER 2017 PROJECT REPORT

Millimeter-Wave Double Balanced Gilbert Mixer

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1 Glossary

2 PROJECT MOTIVATION

In this project, I present a double balanced mixer that would be used as part of a BPSK Modulator circuit to generate a spread spectrum radar waveform in the automotive frequency band (77-81 GHz). A similar modulator that uses a double-balanced mixer is described in [3]. The original design benchmarks for this mixer and the achieved final results are outlined in Table 1.

Parameter	Original	Achieved
Supply Voltage	1.8V	0.85V
Power Consumption	5mW	≈ **4.8mW**
Gain (dB)	5	≈ **-13 dB**
Input Match	50Ω	**45.5 + j0.1Ω**
Output Match	730Ω	**48.9 + j0.1Ω**
NF	10dB	≈ **16 dB**
P1dB	–	≈ 1.5dB
IP3	–	≈ 9.5dB

Table 1: Mixer Design Goals

The original values were generated based on a few simple simulations/calculations and a power budget provided by Dr. Belostotski. The power budget was the control variable that I set as an absolute requirement. Once the Id-gm characteristics were understood from simulation, the gain estimate was calculated using the following equation.

$$G = \frac{2}{\pi} \frac{R_L}{R_s + \frac{1}{g_m}}; \tag{1}$$

The exact values including plots for the final results will be clearly outlined. Furthermore, deviations from original to achieved results will be described in detail. A different design topology was used in the final design than in the original biased circuit used to calculate the conversion gain. Some targets (such as output impedance) were changed intentionally (for practical purposes) while other values were adjusted based on non-ideal aspects of the circuit. A

derivation of conversion gain will be provided in the theory of operation section. A suitable value of R_L was chosen based on biasing and achieving high gain. This value, and others, deviate greatly from the final design. A thorough explanation of the reasons for deviating are provided. The interest in this particular-type of radar stems from spread-spectrum technology's built in interference rejection, which is an indispensable feature for automotive radar. This type of radar has recently been demonstrated in SiGe technology [1, 4]. 65nm technology is chosen because the Figure of Merit, $f_T \approx 160GHz$, making it suitable for this millimeter-wave application.

2.1 Radar Theory of Operation

To demonstrate how this mixer could be used in a practical application, the theory of the type of radar is discussed. A simplified block diagram of an example spread spectrum ranging system is shown in Figure 1. The BPSK modulator is used to spread the carrier with a pseudorandom code. The parameters of the code, which govern the LO mixing frequency, are designed to provide an adequate range resolution within the context of automotive radar. The achievable range resolution of the radar system is related to the chip rate (mixer LO) of the code through Equation 2.

$$d_{min} \leq \frac{c}{2f_c} \tag{2}$$

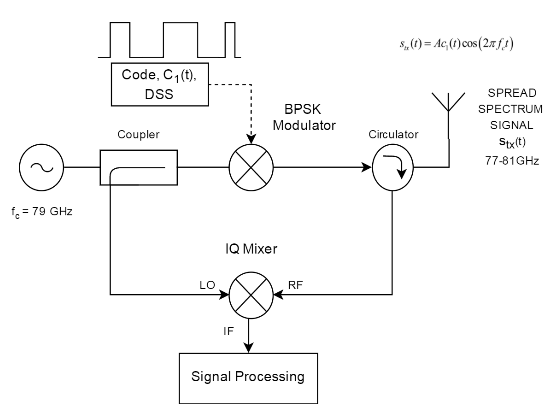

Figure 1: Radar Transceiver Block Diagram

Therefore to achieve a $10cm$ range resolution a chip rate of $1.5GHz$ is chosen. The rest of the code can be designed by choosing the appropriate length.

$$T_p = \frac{N}{f_c} \tag{3}$$

and then achievable unambiguous range of the radar becomes

$$d_{max} \leq \frac{c}{2T_p} \tag{4}$$

Since the code is pseudorandom, the LO frequency could be any integer division of $1.5GHz$ i.e $0.75GHz, 0.5GHz$ etc. For the purposes of design we will simulate with just a $1.5GHz$ signal to demonstrate the maximum bandwidth of operation.

3 Mixer Theory of Operation

3.1 Basic Principle

The Gilbert Cell is a linear time-varying circuit. The concept behind this circuit is intuitive. The RF transistors act as transconductance amplifiers which change the input voltage to a current. The differential ports act as switches that commutate the output. This creates the time-domain multiplication function. Figure 2 demonstrates this concept.

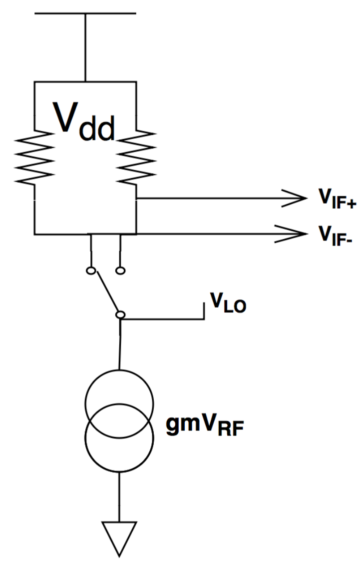

Figure 2: Mixer Theory

Since the Gilbert Cell is a double balanced i.e. both RF and LO inputs are differential, the feedthroughs get subtracted out at IF therefore there should be very little of the RF and LO frequencies at the output.

3.2 RF Port Matching

Originally, as mentioned, the RF port was going to be matched with a 50 ohm source resistor. After understanding that the matching of this circuit could be designed using the same methodology as a source-degenerated LNA topology and also encountering voltage headroom problems, it became apparent that using source and gate inductors to match was the best option. The source inductor is used to match to 50 ohm and the source and gate inductors combined are used to resonate out C_{gs} (and in the case of high frequency many other parasitics).

$$50\Omega = \omega_T Ls \tag{5}$$

$$\frac{1}{w(sC_{gs} + C_{others})} = \omega(L_s + L_g) \tag{6}$$

For 65nm technology $\omega_T \approx 2\pi \times \omega_T$ [2]. This is derived by assuming that impedance looking into the common gate (LO) stage is high, it also ignores all other capacitances and g_ds of RF transistors.

This method is greatly oversimplified for an 80GHz circuit, seeing as there are parasitic capacitances and finite output resistance. Therefore an attempt is made to create an improved input impedance model. Then initial values are calculated using both models. After the simulated values are finalized there is a discussion outlining whether the improved model was useful.

3.3 IF Port Matching

The output matching circuit was originally conceived to be resistive. Again, after I actually learned how to design this circuit, it became clear that an LC tank was required. Therefore the tank was designed to resonate at the desired frequency and the resistive load chosen to meet the output impedance requirement. As will be discussed in the simulation section, none of these values were as expected because of finite g_{ds} and parasitics.

3.4 Conversion Gain

As previously mentioned, the LO differential pairs essentially act as switches. Thereby allowing current to flow through resistors R_1 and R_2. Therefore we have:

$$I_1 = I_{RF}F_T \tag{7}$$

and

$$I_2 = I_{RF}F_T(t - \frac{T_{LO}}{2}) \tag{8}$$

where F_T is the square wave with period T_{LO}. Therefore the voltage at IF is equal to:

$$V_{IF} = V_{DD} - I_1R_L - (V_{DD} - I_2R_L) \tag{9}$$

$$V_{IF}(t) = I_{RF}(t)[F_T(t - \frac{T_{LO}}{2}) - F_T] \tag{10}$$

Since F_T is a square wave it can be seen that multipling by $F_T(t - \frac{T_{LO}}{2}) - F_T$ is the same as multiplying by a square wave with amplitudes ranging from 1 to -1. Using the Fourier expansion of this square wave we have

$$V_{IF}(t) = I_{RF}(t)R_L[\frac{4}{\pi}cos(\omega_{LO}t)...] \tag{11}$$

$$V_{IF}(t) = \frac{2}{\pi}g_{m1}R_LV_{RF}cos((\omega_{RF} - \omega_{LO})t) \tag{12}$$

The peak conversion gain is then:

$$\frac{V_{IF,p}}{V_{RF,p}} = \frac{2}{\pi}g_{m1}R_L \tag{13}$$

If you have a source resistor then the gain drops proportionally, arriving at Equation 1.

4 Design Variations and Final Circuit Schematic

4.1 Circuit Schematic

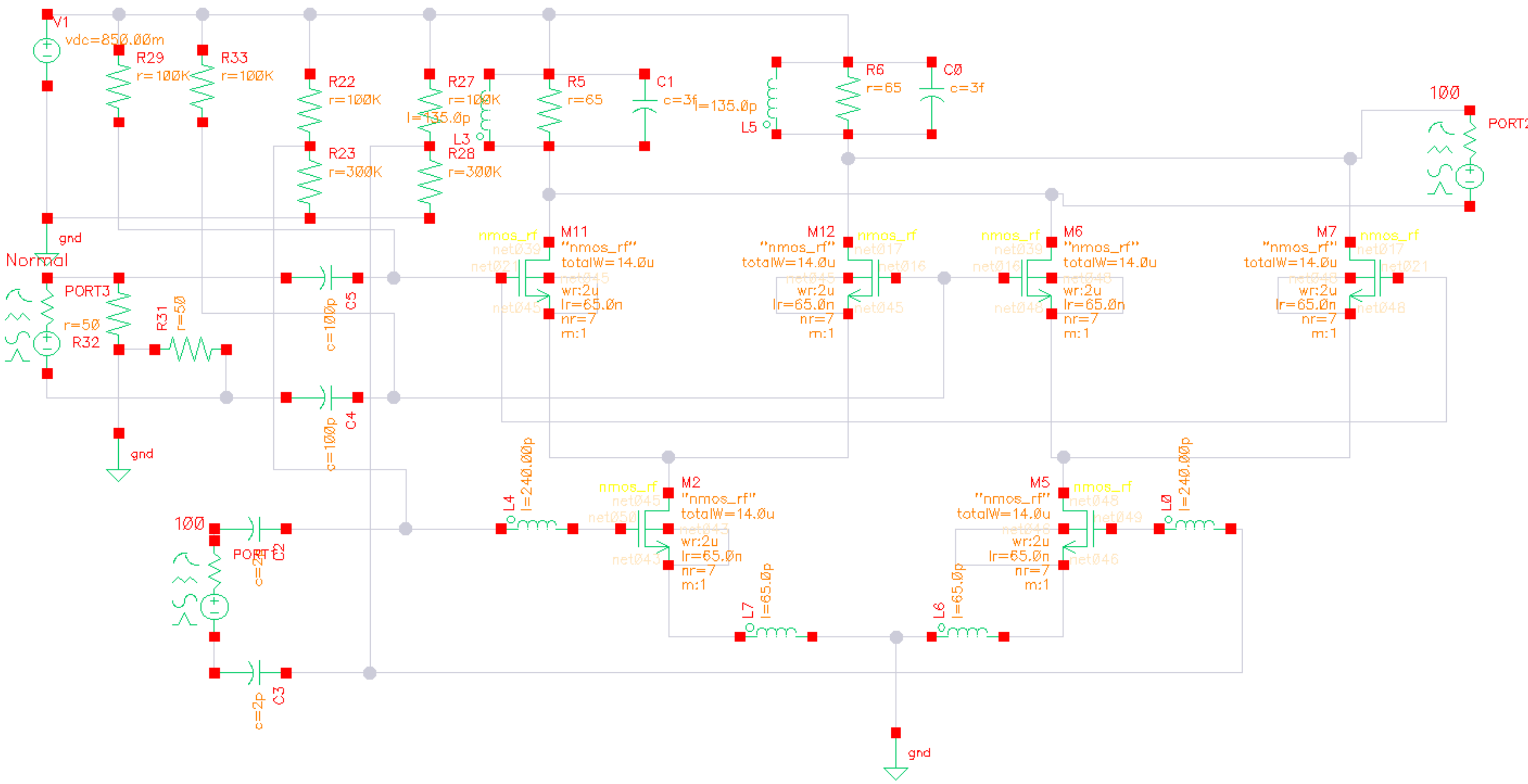

Figure 3: Final Design

Component	Final Values
W, Transistor Width	$14\mu H$
L, Transistor Length	$65nm$
L_s, Source Inductor	$65pH$
L_g, Gate Inductor	$240pH$
R_L, Source Resistance	65Ω
L_T, Tank Inductor	$130pH$
C_T, Tank Capacitor	$3pF$
C_c, DC block/AC Short Cap	$100pF$
$V_{bias,LO}$	0.85V
$V_{bias,RF}$	0.64V

Table 2: Mixer Final Component Values

At first the circuit was designed with a 1.8V power supply and a current mirror for biasing as seen in figure X. However, this topology was causing many problems. First of all, node X had to be maintained at $\approx$ 0.4V for the current mirror to function properly. This was causing a lot of problems because of voltage headroom and being able to design for a V_{od} of $\approx$ 0.1V while also staying under the power budget of 5mW. Therefore after (many weeks) of using that topology, I realized I could scrap the current mirror and lower the voltage. An LC tank was also added to increase voltage headroom and it later became apparent that those components would also be required for output matching because of all the parasitics present. This then allowed me to increase the widths of the transistor, therefore increases the transconductance while still staying below the allotted power budget. The original transconductance was around 5mA/V while, as mentioned, the overdrive voltage was around 50mV (not good). After the supply voltage/topology change was implemented the transconductance achieved was WHAT NUMBA as shown in table BLAH At first, an output resistance of 730Ω was chosen to give approximately 5dB of gain based on fig REF. However, it was decided that it would be unusual to have such a high output impedance since in practice this device would need to interface with other components (PA). Therefore the target was reduced to 50Ω. The reduction in gain was somewhat compensated by the fact that I was now able to get a bigger gm with the reduced power supply.

5 Simulated Results

Table 3: Experiment Results-I

(a) RF Transistors

Parameter	Value
I_D	2.819mA
C_{gs}	9.468fF
C_{gd}	3.613fF
g_m	14.94mA/V
g_{ds}	2.94mA/V
V_{ds}	331mV
V_{gs}	646mV
V_{th}	414mV

(b) LO Transistors

Parameter	Value
I_D	1.409mA
C_{gs}	8.754fF
C_{gd}	3.216fF
g_m	12.18mA/V
g_{ds}	1.38mA/V
V_{ds}	510mV
V_{gs}	511mV
V_{th}	402mV

Overdrive voltage for LO transistors was lower than RF transistors. This is because it was important that the LO transistors would fall into triode and cutoff with the corresponding LO swing. The overdrive voltage for the RF transistors was designed high to get high transconductance while still remaining in saturation.

5.1 Transistor Biasing and Power Consumption

5.2 Conversion Gain

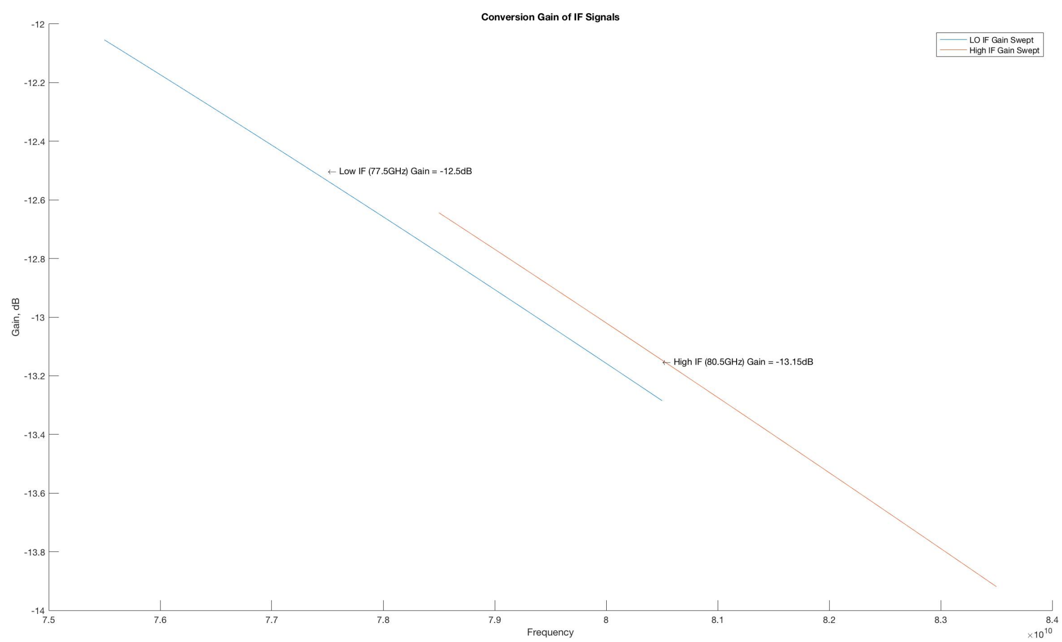

Figure 4: Swept Gain for Lo/Hi IF

5.3 Input and Output Matching

5.3.1 Theory

As previously discussed, the source degenerated topology input impedance is defined by the simple circuit seen below.

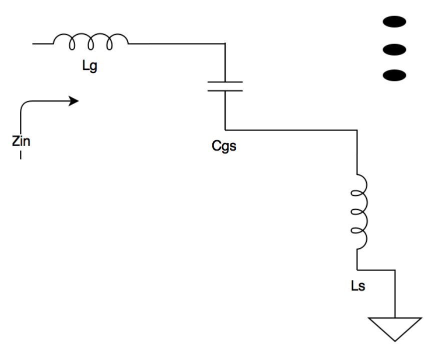

Figure 5: Simplified Input Impedance

From this model, Initial values of 50pH and 370pH are picked based on the simulated bias value of C_{gs}. As a side exercise, an attempt at producing an analytical improved impedance model for the cascode which considers g_{ds} and C_{gd} of both transistors was done and is shown in Appendix B. This model was then used in Matlab with chosen values of L_s in an attempt to get an optimized value as opposed to the value produced by the simplified source degenerated cadcode LNA model. In theory, once values of L_s were analyzed then a more accurate value of L_g could also be chosen based on the remaining reactance. However the values produced by this model and Matlab did not seem to be any closer than the original model. In the end, changes the values based on simulation seemed to be the best method.

After iterative simulation the values of $Ls = 65pH$ and $L_g = 240pH$ were picked as shown in Table 2. These are relatively close to the original guess. It is intuitive that both inductances would be higher because of all the additional parasitic capacitances.

5.3.2 Results

Excellent matching is achieved as shown in Figure 6

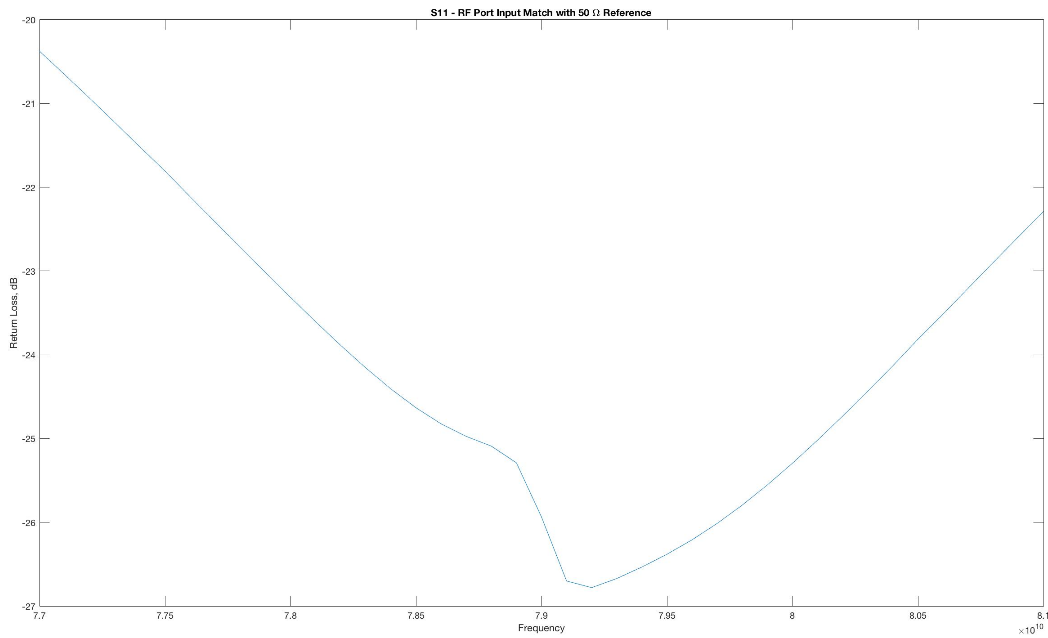

Figure 6: Final Return Loss of RF Port

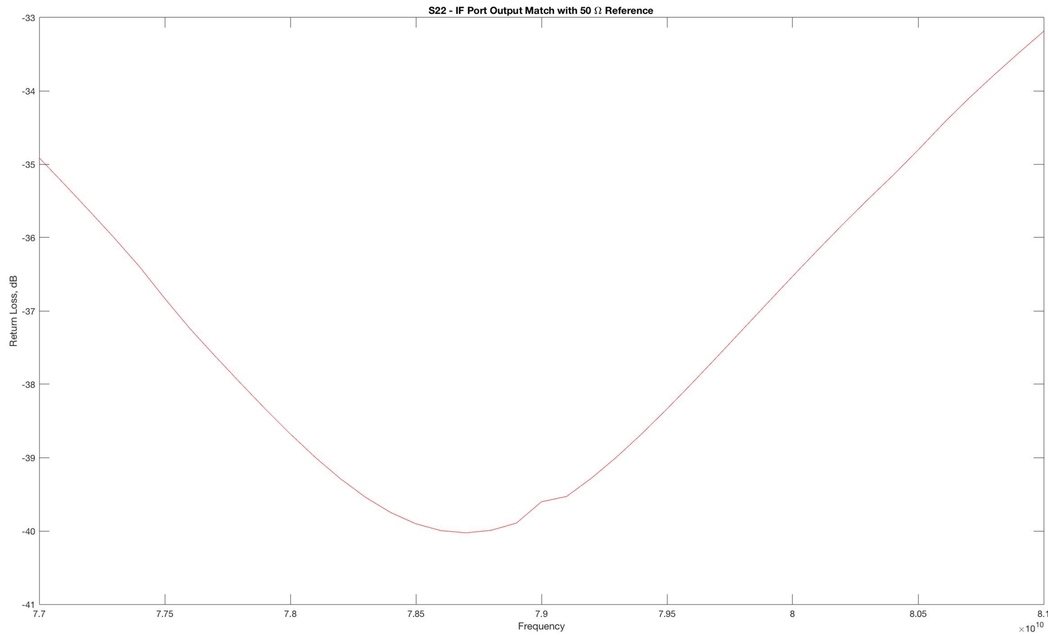

Figure 7: Final Return Loss of IF Port

The matching for the LO ports is simply done with 2 50Ω resistors. Simulations showed almost infinitely small return loss as expected.

5.4 Noise Figure

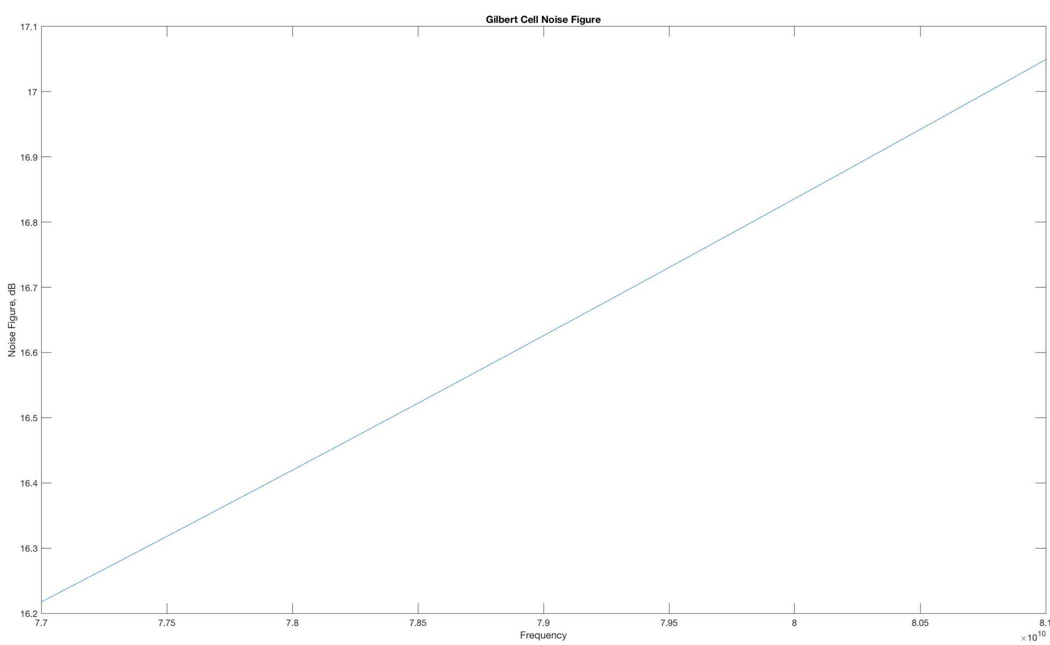

Figure 8: Final NF

5.5 P1dB & IP3

Write some stuff about this...

6 Discussion

6.1 Future Improvements

7 References

[1] Herman Jalli Ng, Reinhard Feger, and Andreas Stelzer. "A fully-integrated 77-GHz UWB pseudo-random noise radar transceiver with a programmable sequence generator in SiGe technology". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.8 (2014), pp. 2444–2455.

[2] Behzad Razavi. *RF Microelectronics (2Nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. 2nd. Upper Saddle River, NJ, USA: Prentice Hall Press, 2011. ISBN: 0137134738, 9780137134731.

[3] Bernd Schleicher, Çagri A Ulusoy, and Hermann Schumacher. "A biphase modulator circuit for impulse radio-UWB applications". In: *IEEE microwave and wireless components letters* 20.2 (2010), pp. 115–117.

[4] Saverio Trotta et al. "A 79GHz SiGe-bipolar spread-spectrum TX for automotive radar". In: *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*. IEEE. 2007, pp. 430–613.

A Cadence Simulation Plots

A.1 Conversion Gain

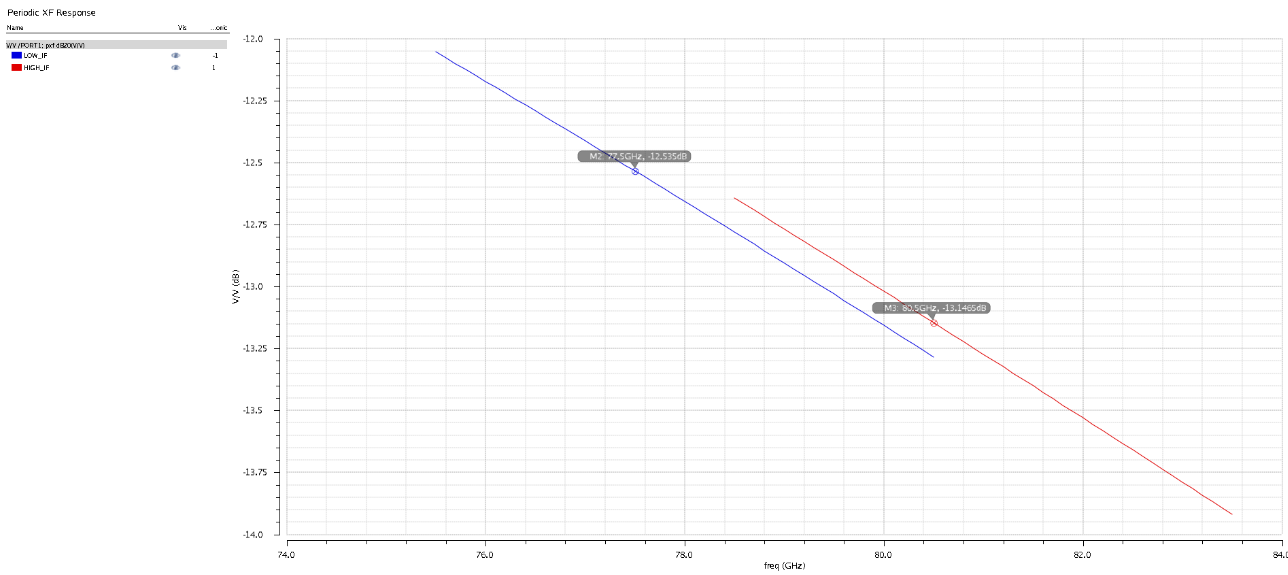

Figure 9: Conversion Gain Cadence

A.2 RMS Spectrum

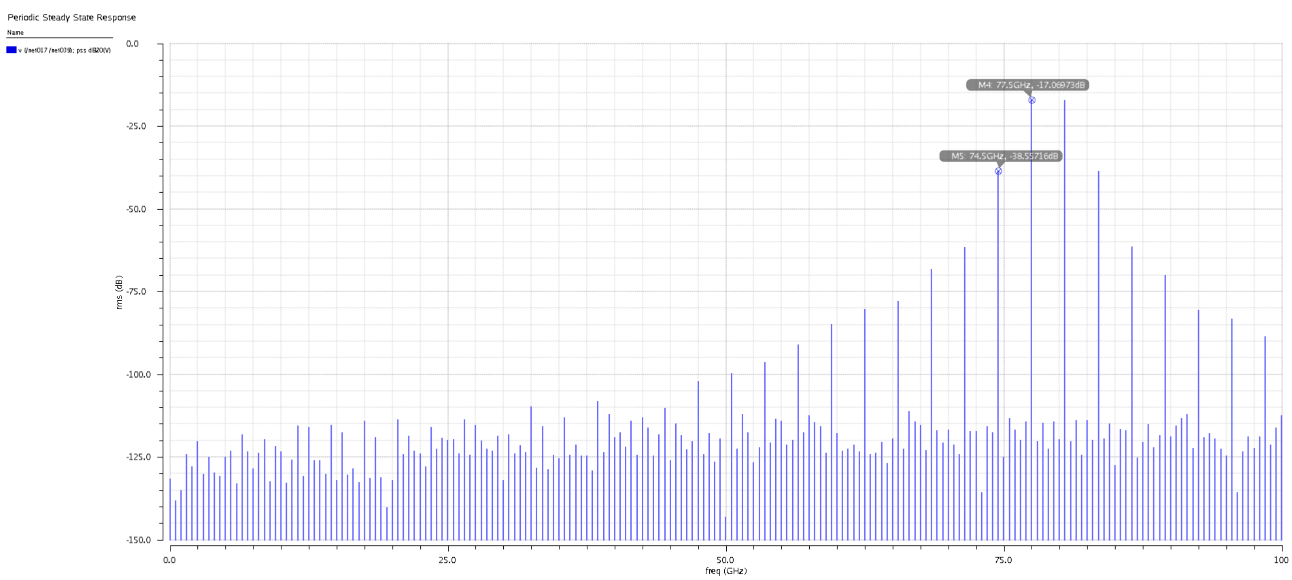

Figure 10: RMS Spectrum Cadence

A.3 Noise Figure

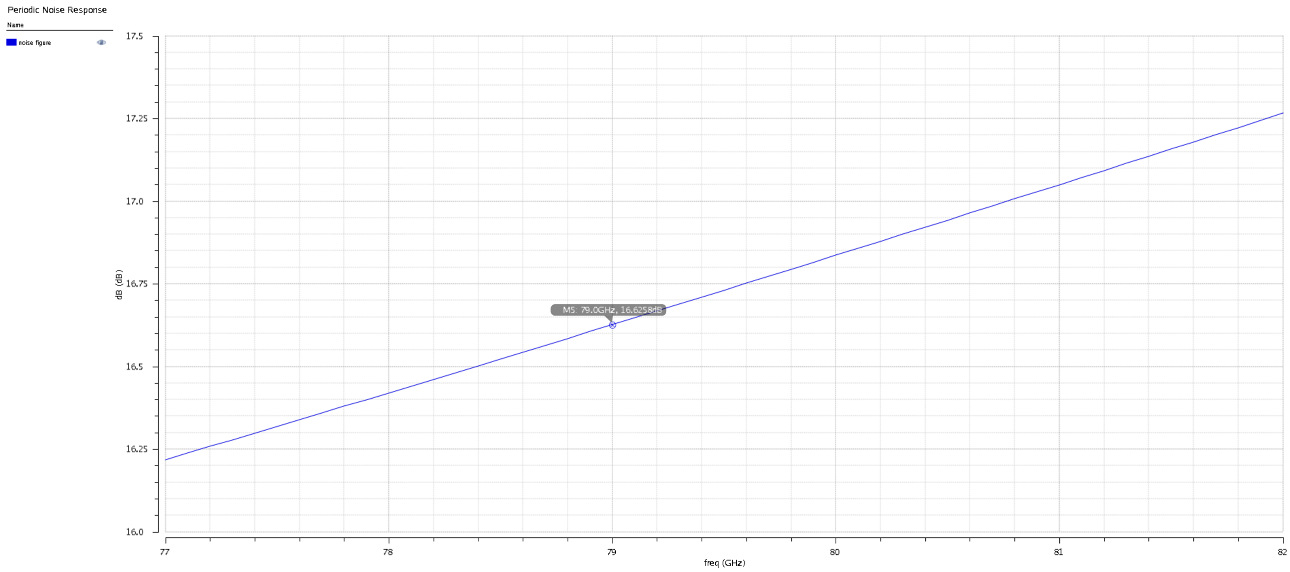

Figure 11: Noise Figure Cadence

A.4 P1dB

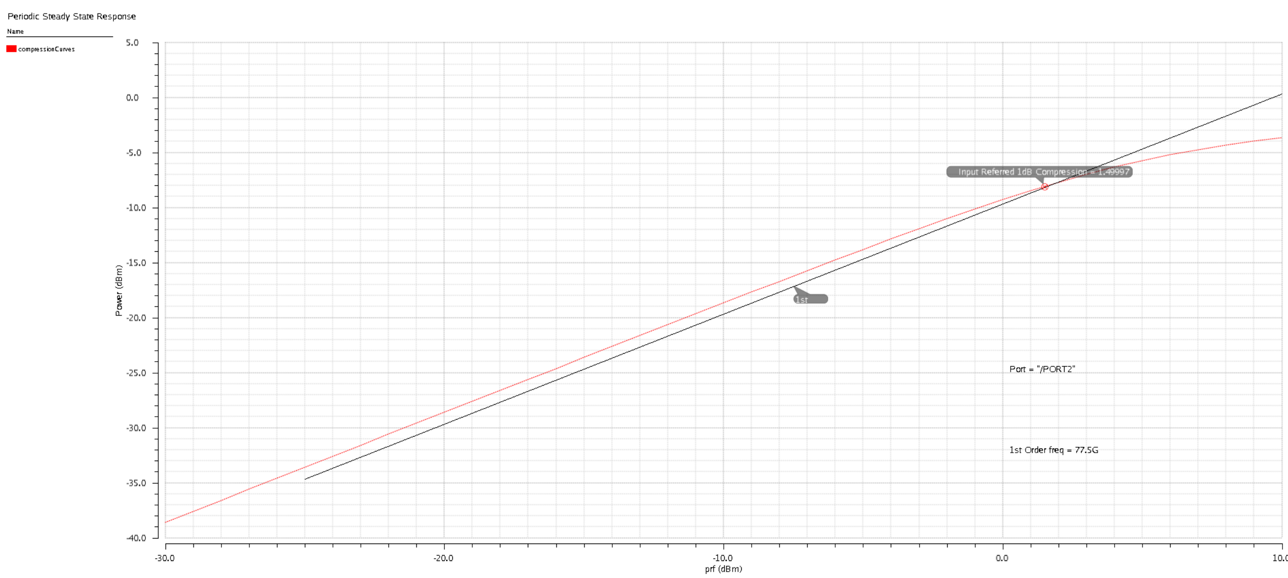

Figure 12: P1dB Cadence

A.5 IP3

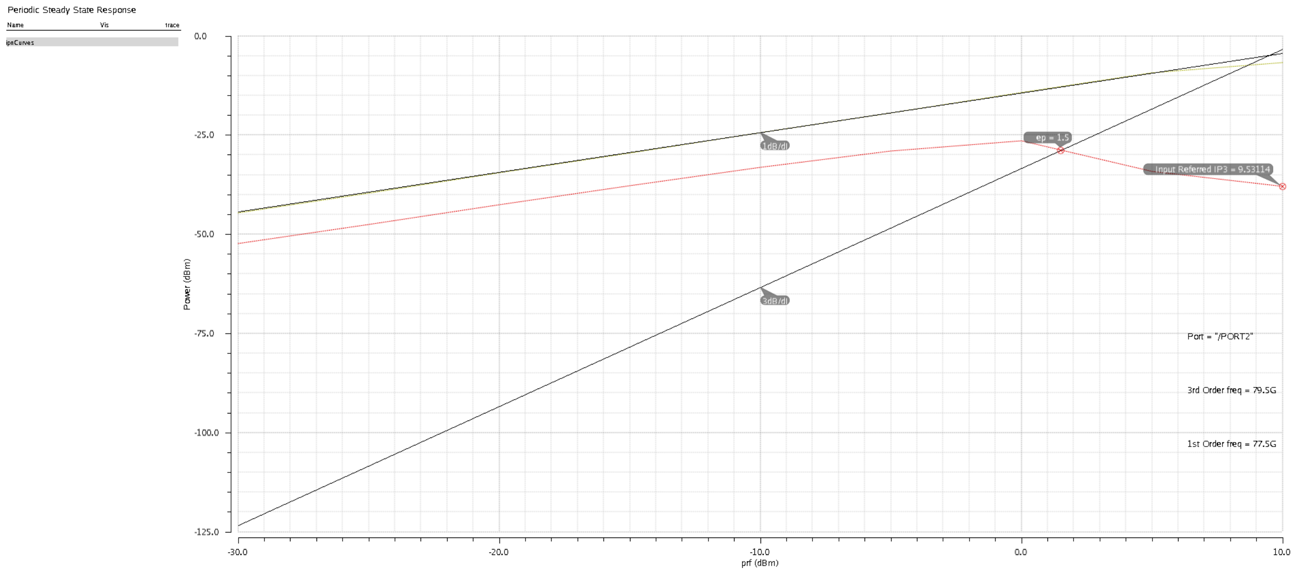

Figure 13: IP3 Cadence

A.6 S11

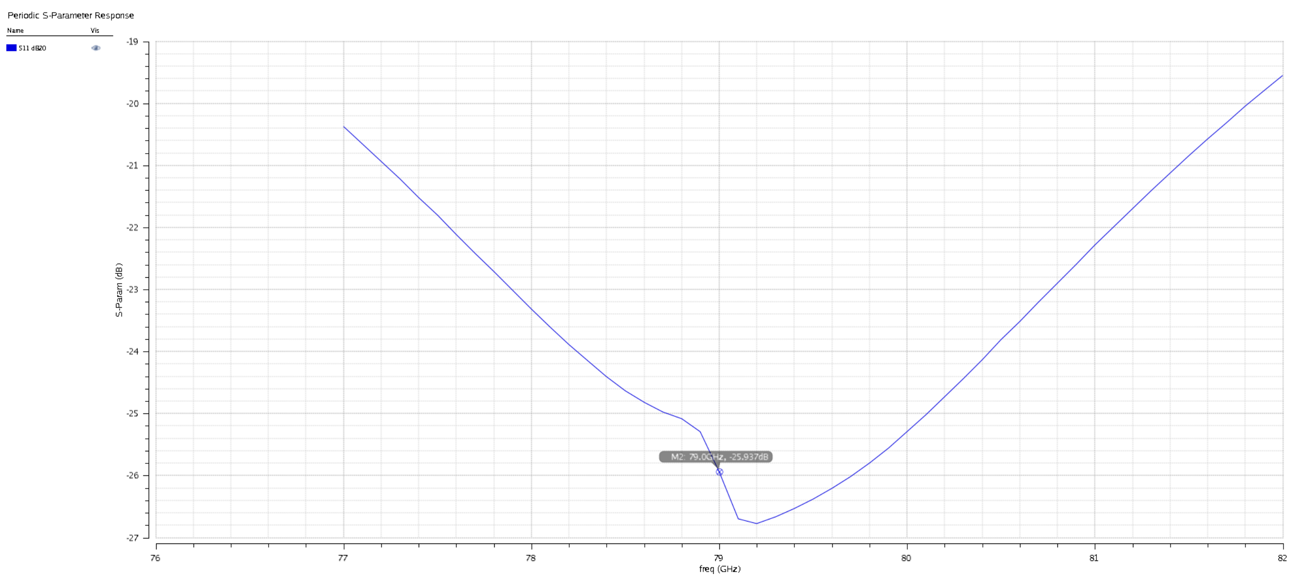

Figure 14: RF Port Match

A.7 S22

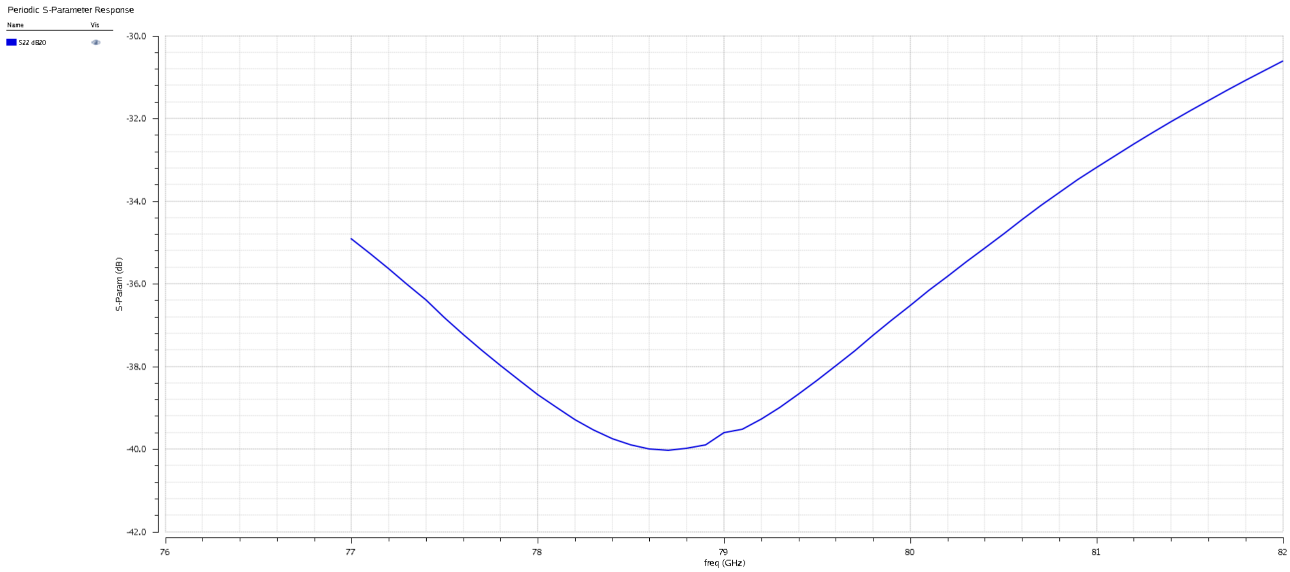

Figure 15: IF Port Match

B Improved Impedance Model