

# Number Representation

## Floating point representation Architecture

IEEE

It having 2 part

① Mantissa / precision

↓  
Sign in fixed no.

② exponent

→ designates position of  
Sign decimal or binary point -

$M \times \gamma^e$

$M = \text{mantissa}$ ,  $\gamma = \text{exponent}$

$\gamma = \text{radix}$

~~Ex:-~~ 0.3145

0.3145  $\times 10^3$   
M e

Or 0.003145  $\times 10^4$

0.3145  $\times 10^4 \times 10^{-2}$

Normalized form for

① digital =  $0.\text{ddd} \times 10^e$

② binary =  $0.\text{bbb} \times 2^e$

In binary NO:-

1111.00  
 $0.1111100 \times 2^5$

Floating point representation only the mantissa & exponent are represented

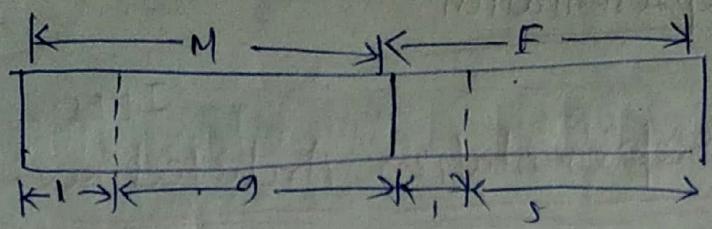
Floating point representation only for mantissa & exponent  
Radix is assumed

### 16 bit representation

In 16 bit representation having following fields

① Mantissa: 10 bit signed magnitude

② Exponent: 6 bit signed magnitude value



Represent the following floating point no. in 16 bit formate

$$\textcircled{1} \quad (12.25)_{10}$$

Step 1

$$8 + 4 + \frac{1}{4}$$

$$16 \ 8 \ 4 \ 2 \ 1 = \frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \dots$$

$$\rightarrow 1:100 \cdot 01$$

Step 2

Normalize  $\rightarrow$

$$0.110001 \times 2^4$$

Normalized for 16 bit

In decimal

$$0.ddd \dots \times 10^e$$

In binary

$$0.bbb \times 2^e$$

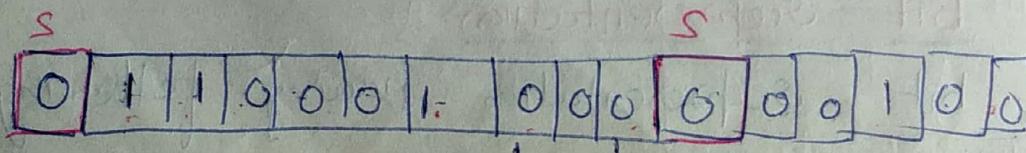
Step 3

16 bit

represent

M - 10 bit

e - 6 bit



Note :- If digit less than 8 bit then add zero after digit in Mantiss.

In the exponent part we add the zero front of the digit of e

If given

$$\begin{array}{r} 0.110001000 \\ \times 10^4 \\ \hline 110001000 \end{array}$$

$$M = 110001000$$

$$E = 4$$

$$\text{num} - M \times 2^E$$

$$= 110001000 \times 2^4$$

Ques

$$(-17.5)_{10}$$

$$- (10000 \times 1)_2$$

$$= 0.100011 \times 2^5$$

$$M = 100011000$$

$$E = 5$$

$$\boxed{\begin{array}{r|rr} S & M & e \\ \hline 1 & 100011000 & 010000 \end{array}}$$

Ques

$$(0.375)_{10}$$

$$\Rightarrow = 1/4 + 1/8$$

$$= (0.011)_2$$

Normalize

$$= 0.11 \times 2^{-1}$$

Exponent

$$= -1$$

$$\boxed{\begin{array}{r|rr} S & M & e \\ \hline 0 & 110000000 & -100001 \end{array}}$$

Ques

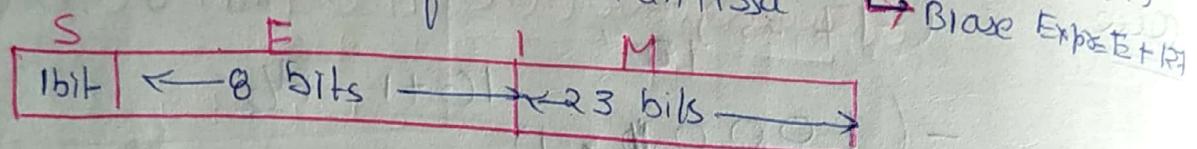
There are single (32) & double (64) floating point representation

① 32 bit version. - it is also known as Single floating point representation having the following field

S<sub>0</sub> - Sign bit (1bit) (+/-) Use for mantissa

E<sub>0</sub> - 8 bits for exponent range  $-2^7$  to  $2^7-1$  (128 to 127)

M<sub>0</sub> - 23 bits for mantissa



Normalize

$$1.bbb \times 2^{e-1}$$

$$1.111 = 1.\underbrace{1111}_{M} \times 2^{+3}$$

$$0.111 = 1.\underbrace{111}_{M} \times 2^{-1}$$

$$0.001 = 1.\underbrace{001}_{M} \times 2^{-3}$$

If exponent  $\neq 0$

$$N = (-1)^S \times 1.bbb \times 2^{\text{exp}-127}$$

If exponent = 0

$$N = (-1)^S \times 0.bbb \times 2^{\text{exp}-128}$$

Ques Represent the following floating point no.

In 32 bit IEEE-754 format

$$(-17.5)_{10}$$

$$\text{ddd}dd842 \oplus 1/2 1/8$$

$$-(10001.1)_2$$

$$10101.11$$

Normalize  $1.00011 \times 2^4$

$$01011$$

$$101.011$$

$$S = -1$$

$$M = 000110000000000000000000$$

$$\text{Exp} = 4 + 127 = 128 + 2 + 1$$

$$\boxed{\begin{array}{c|c|c} S & E & M \\ \hline 1 & 100000 & 00011 - 18 \text{ bit } 0 \\ \hline \end{array}}$$

$$\begin{array}{ccccccc} 128 & 64 & 32 & 16 & 8 & 4 & 1 \\ | & | & | & | & | & | & | \\ 1 & 0 & 0 & 0 & 0 & 0 & 1 \end{array}$$

$$N = (-1)^S \times 1.bbbb \times 2^{\text{Exp} - 127}$$

$$N = -1 \times 1.00011 \times 2^{131 - 127}$$

$$N = -1 \times 10001.1 \times 2^4 = -17\frac{1}{2}$$

Ques

0 - 6  $\frac{5}{8}$  represented in 32 bit version

$$= -6\frac{5}{8}$$

$$= - (4+2+\frac{1}{8}+\frac{1}{2})$$

$$= - (4+2+1\frac{1}{2}+\frac{1}{8})$$

$$= -(1\underset{1}{1}0 \cdot 1001)_2$$

$$1 \cdot 10101 \times 2^2$$

$$S = -1$$

$$M = 1.0101 - 18 \text{ bit } 0$$

$$2+127 = 129$$

127 = 1000000  
g e M  

1110000001	10101 - 18 bit
------------	----------------

$$N = (-1)^s \times 1.bbb\bar{b} \times 2^{exp - 127}$$

$$= -1 \cdot \underbrace{1.10101}_{x_2} \cdot x_2^{129 - 127}$$

$$= - \underbrace{110 \cdot 101}_{= 2} = -6 \cdot 5/2$$

$$\begin{array}{r} & 8 \\ \overline{60} & 1111011 \\ 6432148 & 421 \\ \hline & 000000008000 \end{array}$$

$$127 - 4 = 123$$

$$N = (-1)^0 \times (1,00000) \times 2^{\frac{123-172}{10}}$$

$$N = (-1)^0 \times (1.00000) \gamma_2^{-4}$$

bad ooo...!

0001-000  
B2 V2 X6 V13

$$\frac{A}{\pi} = 11/6$$

$$\begin{aligned}104 + \\24 - 14 \\= 16 - 5 \\= 11\end{aligned}$$

$$(-1)^0 \times 1.00101 \times 2^{130-127}$$

$$(-1)^0 \times \underbrace{1.00101}_{10} \times 2^4$$

$$= 1.00101 = 18 \frac{1}{2}$$

Ques What is decimal value of the following floating point no?

$$\begin{array}{r} 1.001010010100000\dots \\ \hline \text{s} \quad \text{e} \quad \text{m} \end{array}$$

$$\begin{aligned} & (-1)^1 \times 1.00101 \times 2^{130-127} \\ &= -\cdot \underbrace{1.00101}_{10} \times 2^3 \\ &= -1.00101 \\ &= -9 \frac{1}{4} \end{aligned}$$

Ques What is the largest no. that can be represented in 32 bit floating point using the IEEE 754 format?

$$\begin{array}{r} 0, \underbrace{1111110}_{1-23 \text{ bit}}, \underbrace{1}_{M} \\ \text{s} \quad \text{e} \quad \text{m} \end{array}$$

$$M = (-1)^0 \times 2^{127} \times 1.00000$$

$$M = (-1)^0 \times 2^{127} \times \underbrace{1.00000}_{10 \text{ digits}}$$

$$1.000000000000000\dots = 1.7 \times 10^{37}$$

$$= 10 \text{ digits} = 3.4 \times 10^{37}$$

What is the smallest no closer to zero that can be represented in 32 bit FP using the IEEE 754 format

0000 - -- 31 time 1010A1 01

$$2 \times (2^{0-127}) \times (0.00000001)$$

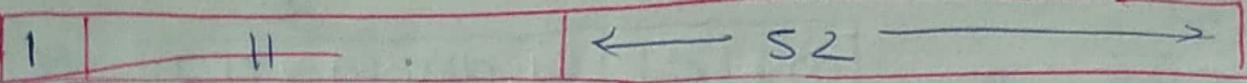
## 64 bit Representation

- 32 bit floating point "fp" is used  
usually called single precision "fp"  
A double precision FP "fp" requires  
64 bits
  - In double precision the following no  
of bits are used

$S = 1$  bit (+/-) for mantissa

F : 11 bit : Bias from  $-2^{10}$  to  $2^{10}-1$   
 $(-1024 \text{ to } 1023)$

$$M = 52 \text{ bit} \stackrel{?}{=} E + 1023 \text{ for mantissa}$$



ex  $\neq 0$

$$N = (-1)^S \times 1.bbb \times 2^{E-1023} \quad 1 \leq E \leq 1024$$

$$Ex = 0$$

$$N = (-1)^S \times 0.bbb \times 2^{E-1022} \quad 0 \leq E \leq 1023$$

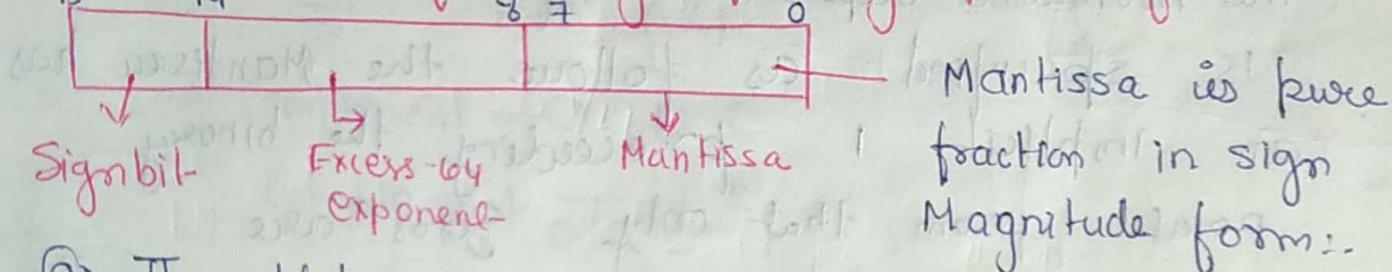
Q. Represent the following no in 64 bit format

$$(-171.75)_{10}$$

Convert

128	64	32	16	8	4	1	2	1	127
1	2	3	4	5	6	7	8	9	0

Q. Consider the following floating point format



- (a) The additional no.  $0.239 \times 2^{13}$  has the following hexadecimal representation (without normalization & rounding off)

- (a) 0D24      (b) 0D4D      (c) 4D0D      (d) 4D3D

Soln

$$N = 1 \times (-1)^S \times 1.bbb \times 2^{E-64}$$

$E+64$	$13+64=77$	$16+8+4+1$
64	32	16

1      0      0      1      1      1      0      1

$$M = 0.239 \times 2 = 0.478$$

$$M = 0.478 \times 2 = 0.956$$

$$M = 0.956 \times 2 = 1.912$$

$$M = 0.912 \times 2 = 1.824$$

$$M = 1.824 \times 2 = 1.684$$

$$M = 1.684 \times 2 = 1.296$$

$$M = 1.296 \times 2 = 0.592$$

$$M = 0.592 \times 2 = 1.184$$

$$0.239 = 0.0011101$$

15	14	8	7
0	1001101	0011101	
4	D	3	D

Ques  
11

The normalized representation of the above fraction is specified as follows the Mantissa has an implicit point assuming that only zeros are preceding the binary normalized rep. of the above no.  $0.239 \times 2^3$  is

(A) 0A20

(B) 1123

(C) 4DD0

(D) 4AED

N =

$$0.239 \times 2^3 = 0.0011101 \times 2^3$$

$$1.11101 \times 2^{3-3}$$

$$1.11101 \times 2^{10}$$

M =

11101

E =

$$10 + 64 = 74 \quad 64 + 8 + 2$$

$$Q \quad \boxed{0 \ 1001010} \quad \boxed{11101000} \quad M$$

4      8      e      8

Ans 9008

Ques The no. ~~is~~ 43 in 2's complement representation

is

$$64 \ 32 \ 16 \ 8 \ 4 \ 2 \ 1$$

$$43 \rightarrow 1 \ 0 \ 1 \ 0 \ 1 \ 1$$

1's complement

$$0 \ 1 \ 0 \ 1 \ 0 \ 0$$

$$+1$$

2's complement

$$\overline{0 \ 1 \ 0 \ 1 \ 0 \ 1}$$

Ans

Ques The 2's complement of -15 is

$$15 = 16 + 8 + 4 + 2 + 1$$

$$15 = 1 \ 1 \ 1 \ 1$$

$$1's \text{ complement} = 000 \ 0$$

$$2^{st} \text{ complement} \overline{0 \ 0 \ 0 \ 1}$$

$$-15 = 1 \ 0 \ 0 \ 0 \ 1$$

Ques All Binary no is 2's complement representation which of the following no. representation

is divisible by

$$\underline{\underline{11111011}} \ 9$$

- a)  $\underline{\underline{11100111}} \xrightarrow{Sol^*} 00011000 + 1 = \underline{\underline{00011001}} \ 13$
- b)  $\underline{\underline{11100100}} \xrightarrow{Sol^*} 00011011 + 1 = \underline{\underline{00011100}} \ 12$
- c)  $\underline{\underline{11010111}} \xrightarrow{Sol^*} 00101000 + 1 = \underline{\underline{00101001}} \ 29$
- d)  $\underline{\underline{11011011}} \xrightarrow{Sol^*} 00100100 + 1 = \underline{\underline{00100101}} \ 25$

Ques

The decimal value 0.25

(a) Is equivalent to binary value 0.1

(b)  $\frac{1}{2} + \frac{1}{4} = 0.11$

(c)  $\frac{1}{2} + \frac{1}{4} + \frac{1}{8} = 0.101$

(d) Can not be represented in binary form

$$\begin{array}{r}
 0.25 \\
 \boxed{8 \ 4 \ 2 \ 1 \cdot 1_2 \ 1_4 \ 0} \\
 \underline{- \ 0 \ 1} \\
 \hline
 \end{array}
 \quad \text{Ans} \quad .01$$

Ques

The range of integer that can be represented by an n bit's complement no sys.

(a)  $-2^{n-1}$  to  $2^{n-1} - 1$

(b)  $-(2^{n-1} - 1)$  to  $2^{n-1} - 1$

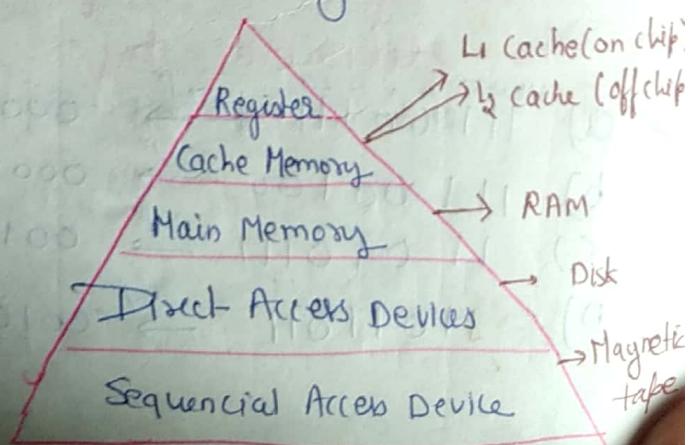
(c)  $-2^{n-1}$  to  $2^{n-1}$

(d)  $-2^{n-1} + 1$  to  $2^{n-1} + 1$

## Memory Hierarchy

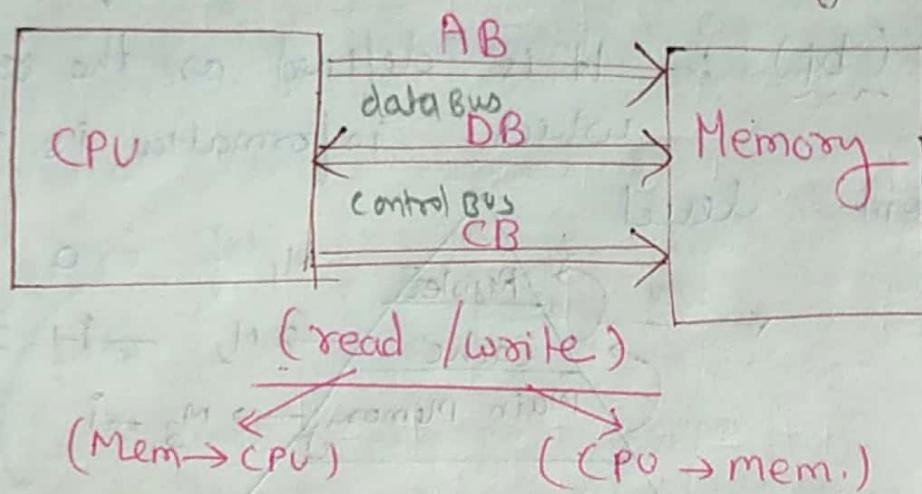
The execution speed of a program is dependent on the speed with which instruction & data is transferred b/w processor & memory

- \* storage capacity increases
- \* access time increases
- \* frequency duration decreases
- \* speed decreases



- ① Increasing Capacity as goes down
- ② Increasing Access time goes down
- ③ Decreasing frequency of access of memory goes down
- ④ Decreasing speed of memory
- ⑤ Decreasing cost per bit

Note There is a large speed gap b/w CPU & Memory



Memory is about 1000 times slower than CPU.

To make an efficient computer system it is not possible to depend only on single memory component but on multilevel memory hierarchy

The memory hierarchy is used to match the bandwidth of memory w.r.t C.P.U.

There are 5 parameters characterised thus mem. tech.

(1) Access time ( $t_{A,i}$ )  $\Rightarrow$  It is defined as the round trip time for the CPU to the  $i^{\text{th}}$  level memory. It can range from a few nano-sec. to mili-second

(ii) Memory size ( $s_i$ ) :- It is defined as the no. of byte or words in the level  $i$ .

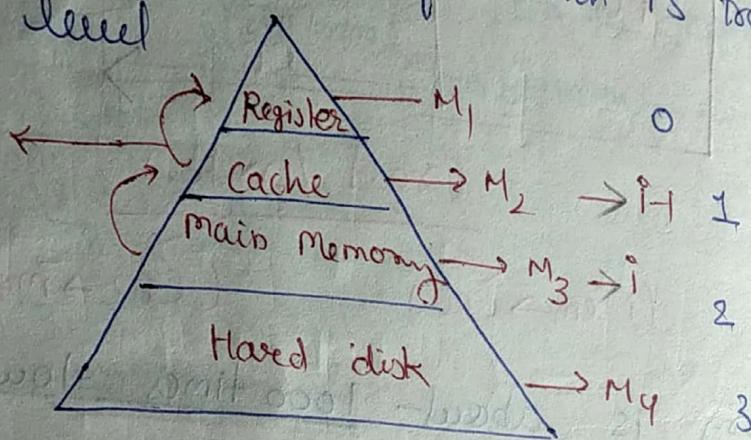
(iii) Cost ( $C_i$ ) :- The cost of the  $i^{\text{th}}$  level is estimated by formula

$$C_i * s_i$$

Where  $C_i = \text{cost per byte/bit}$   
 $s_i = \text{no of byte or word.}$

(iv) Bandwidth ( $b_i$ ) :- It is defined as the rate at which information is transferred b/w adjacent levels.

Rate \*



(v) Unit of transfer ( $x_i$ ) :- It is defined as gain size for data transfer b/w the level  $i$  and  $i+1$ .

Note

from fig \*

level 2

level 1

①  $t_i < t_{i-1}$  access time

②  $s_i > s_{i-1}$  memory size

③  $C_i < C_{i-1}$  cost

④  $f_i > f_{i-1}$

⑤  $x_i > x_{i-1}$

⑥  $b_i < b_{i-1}$  bandwidth

$$[f_i \times b_i]$$

$$s_i = \frac{t_i}{f_i}$$

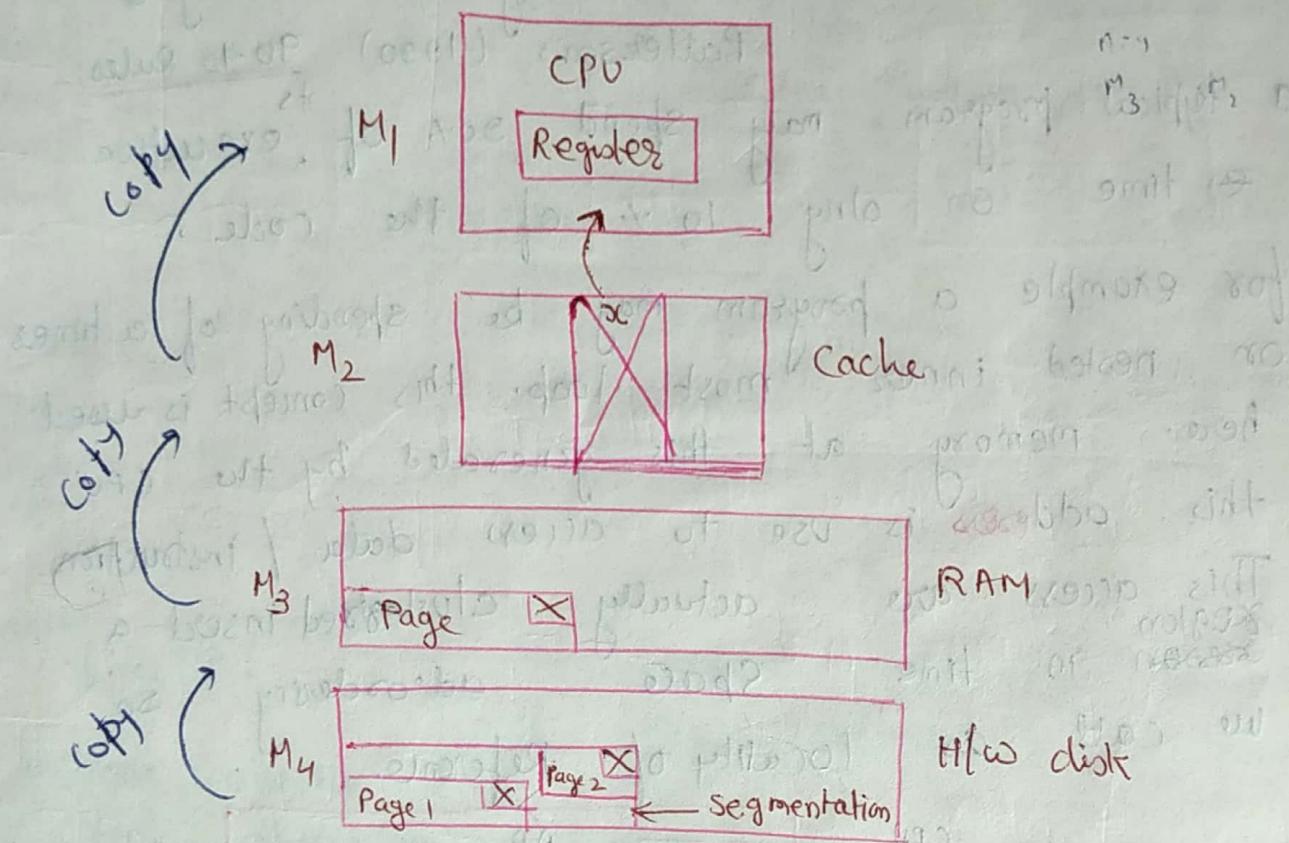
$$s_i = \frac{b_i}{f_i}$$

# Property of Memory hierarchy

## ① Inclusion Property:-

$$M_1 \leq M_2 \leq M_3 \leq \dots \leq M_n$$

it means that all information is originally stored in the outermost level  $M_n$  during the processing. Subset of  $M_n$  is copied into  $M_{n-1}$  similarly subset of  $M_{n-1}$  are copied into  $M_{n-2}$  and so on.



② Coherence Property :- Coherence property means that at the successively memory level must be consistent. This simply means that if a word is changed in Cache ( $M_2$  level) then copy of that word must be updated immediately at higher level but memory hierarchy is to be maintained. There are 2 procedures to update the higher level memory hierarchy :-

(A) Write through :- It means that immediate update in  $M_{i+1}$ , if a word is modified in  $M_i$  (write without any delay)

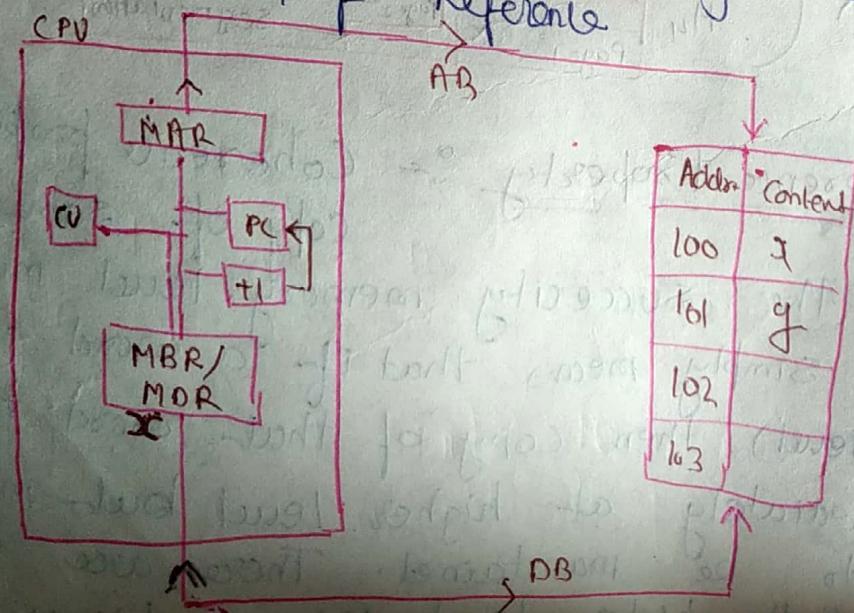
(B) Write Back:- It means delaying the update in  $M_{i+1}$ , until the word being modified in  $M_i$  is replaced or removed from  $M_i$ .

(C) Locality of Reference:- According to Hennessy & Patterson's (1990), 90-10 Rules.

A typical program may spend 90% of its execution time on only 10% of the code.

for example a program may be spending most of the time in nested inner loops. This concept is used here. memory addresses are used to access data / instruction clustered in a space. so, address ordering is maintained.

Locality of Reference

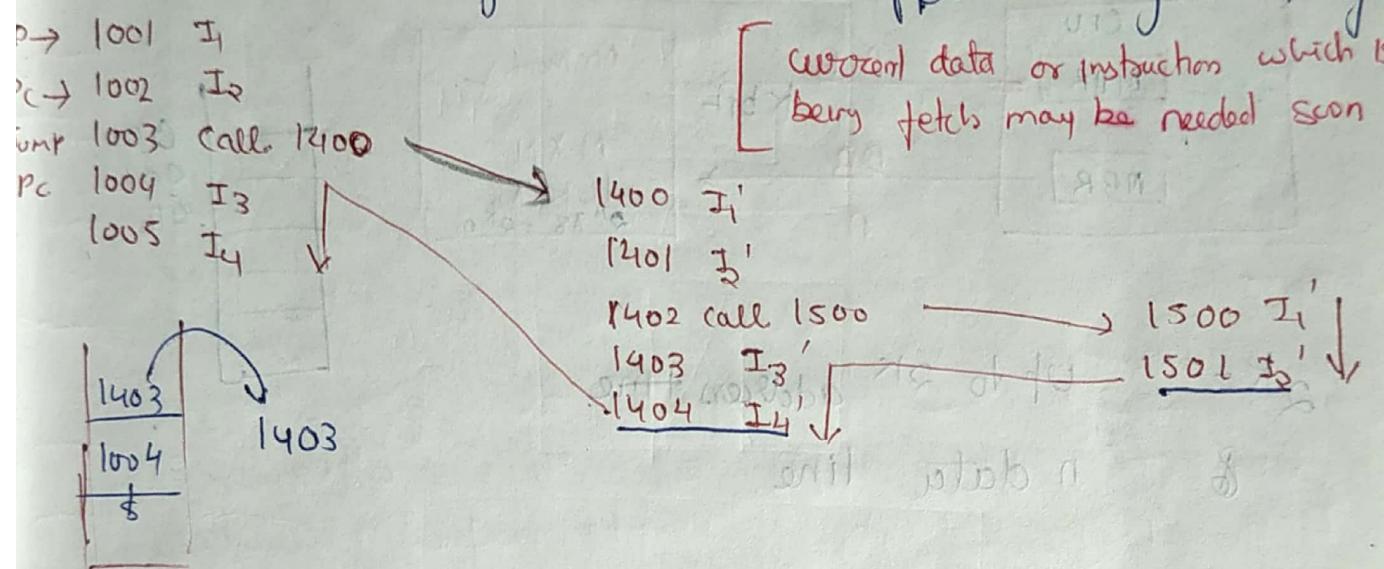


1 - Memory add. Register  
2 - Memory data register

There are 3 type of locality of reference

- ① Temporal Locality
- ② Spatial
- ③ Sequential

① Temporal Locality:- It tends to clustered the access in the recently use area. (variable), for example once a loop entered or a subroutine is called some part of soft. program will be referenced again & again



### ② Spatial

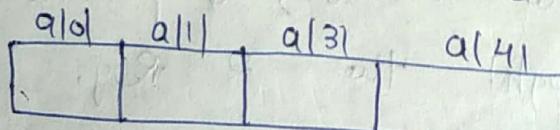
to one another

Ex:- operation on array

This tends to cluster the access of item whose address of near

[Instruction or data near to the current main memory location may needed soon]

a(0) & a(1) are near by so spatial



locality

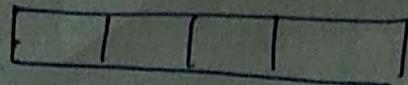
### ③ Sequential

Sequential order or access of the array so Sequential locality of reference.

It means sequential order of execution of instruction

Sequential order of access of the array so

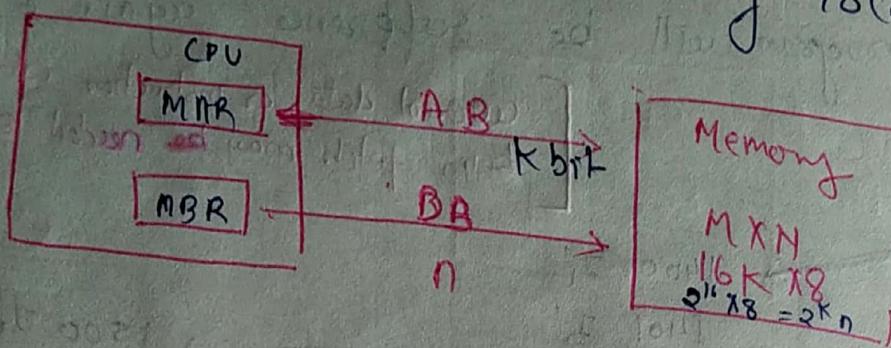
Ex: large data array is sequential



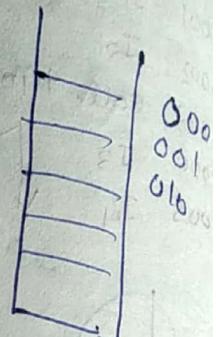
#### (4) Semiconductor Memory:-

Processor is capable of addressing  $2^{16}$  =  $2^{10} \times 2^6$  = 64 KB memory location

16 bit address and memory location



$2^K =$   
Up to  $2^K$  address line  
&  $n$  data line



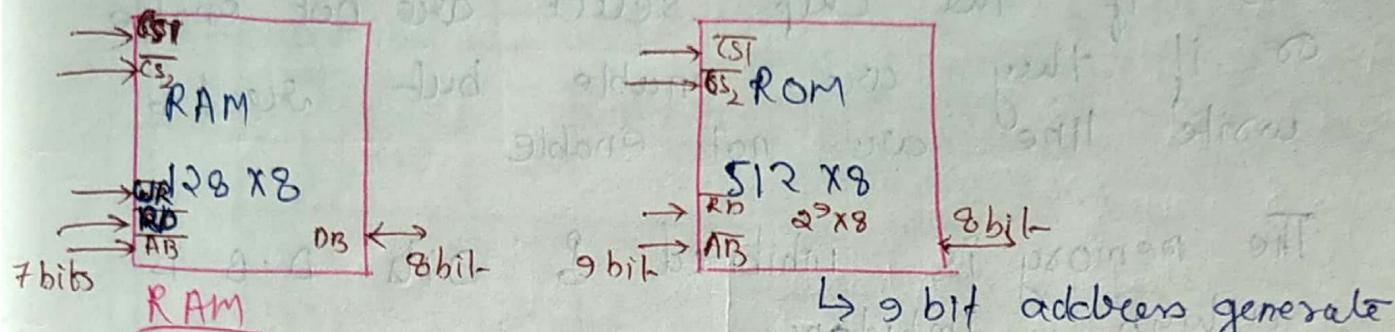
$$4 \text{ GB} = \begin{aligned} &\rightarrow 4 \times 2^{10} \text{ MB} \\ &\rightarrow 4 \times 2^{20} \text{ KB} \\ &\rightarrow 4 \times 2^{30} \text{ B} \\ &\rightarrow 2^{32} \text{ B} \end{aligned}$$

Data transfer between memory & processor  
place through the 2 Reg.  
① MAR  
② MBR

If MAR is  $K$  bit long  
MBR is  $n$  bit long

Then memory contain up to  $2^k$  add. unit  
 During a memory cycle  $n$  bits are transfer  
 b/w memory & processor over the processor  
 bus which has  $k$  add. line and  $n$  data line

### Memory connection to CPU



A RAM chip is best suited for comm. with the CPU if it has one or more control line to select the chip only when needed

It has by bidirectional DB that allow transfer of data either M.M to CPU during a read operation or CPU to memory for write operation

This Bidirectional bus can be constructed using 3 state

Buffer . 3 state Buff. has 3 possible state

- 1) logic 1
- 2) logic 0
- 3) high impedance

High impedance behave like an open -ckf means the o/p does not carry any signal it lead to very high resistance and hence no current flow.

The unit is in operation only when  $CS_1 = 1$

$$\text{&} \overline{CS_2} = 0$$

The bar on top of 2<sup>nd</sup> chip select  $\overline{CS_2}$  this input is enable when it is equal to zero

$$\text{i.e., } \overline{CS_2} = 0$$

Thus if the chip select are not enable or if they are enable but read & write line are not enable

The memory is inhibited & D<sub>B</sub> is a high impedance

### ROM

The 2<sup>nd</sup> chip select line must be

$CS_1 = 1$  and  $\overline{CS_2} = 0$  for the unit to be operational otherwise the D<sub>B</sub> is in high impedance there is no read & write control

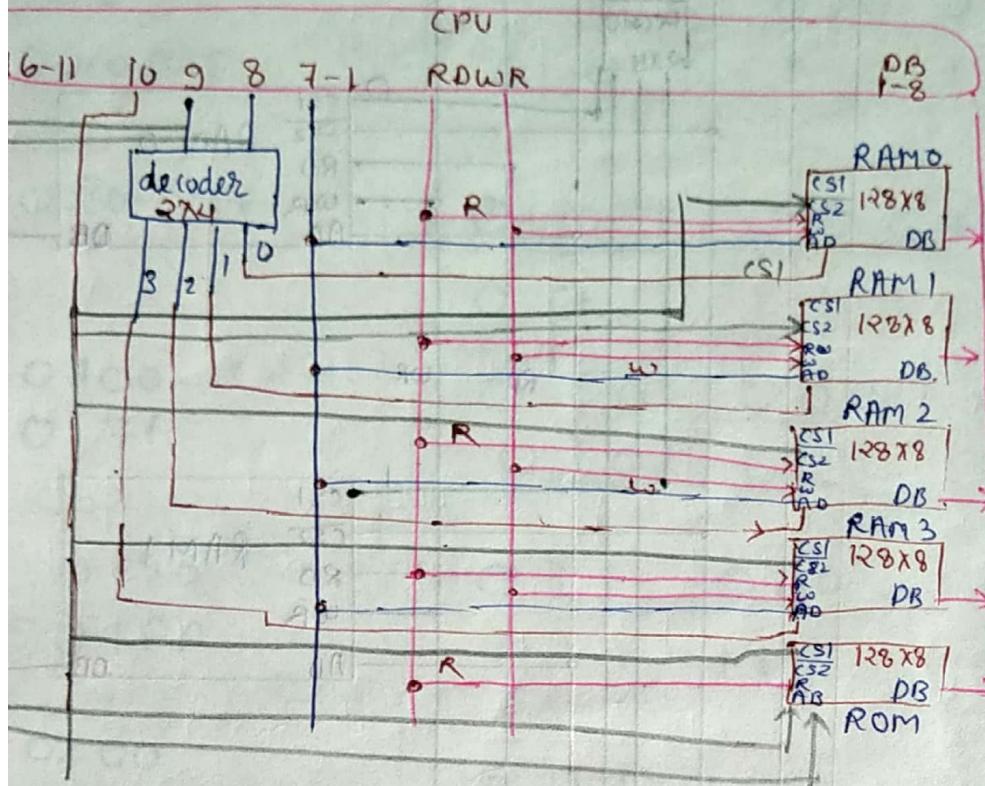
because the unit can be only read thus when the chip is selected the byte selected by the selected address appears to be in the Data

CS <sub>1</sub>	CS <sub>2</sub>	RD	WR	Memfunc	State of D <sub>B</sub>
0	0	x	x	Inhibit	H.I.
0	1	x	x	-	-
1	0	0	1	Write	W/P data to RAM
1	0	1	x	Read	I/O data from RAM
1	1	x	x	Inhibit	High impedance

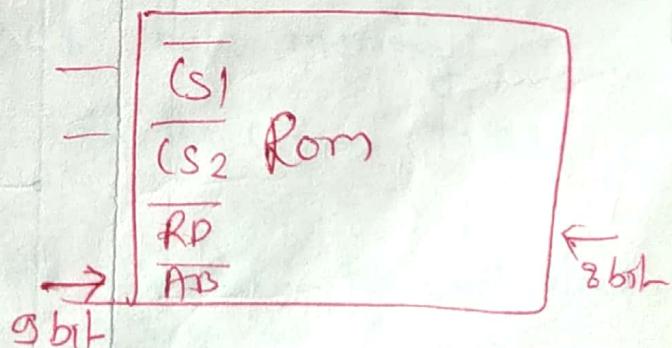
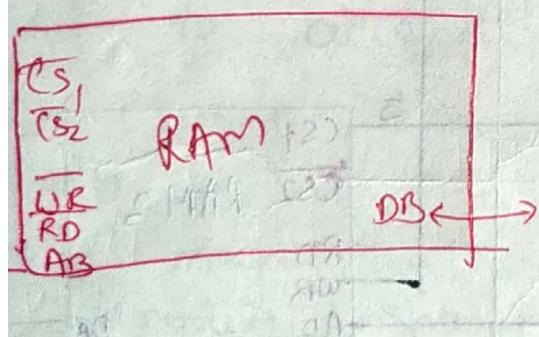
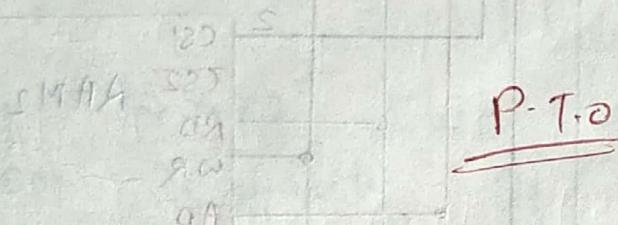
$$\left\{ \begin{array}{l} 1024 \times 8 \\ \text{RAM} = 128 \times 8 \rightarrow 2^7 \times 8 \\ \text{ROM} = 512 \times 8 \rightarrow 2^9 \times 8 \end{array} \right. \quad 1K \times 8$$

$$\text{ROM} = 512 \times 8 = 1 \text{ chip}$$

$$\text{RAM} = \frac{(1024 - 512)}{128} = \frac{512}{128} = 4 \text{ chip}$$

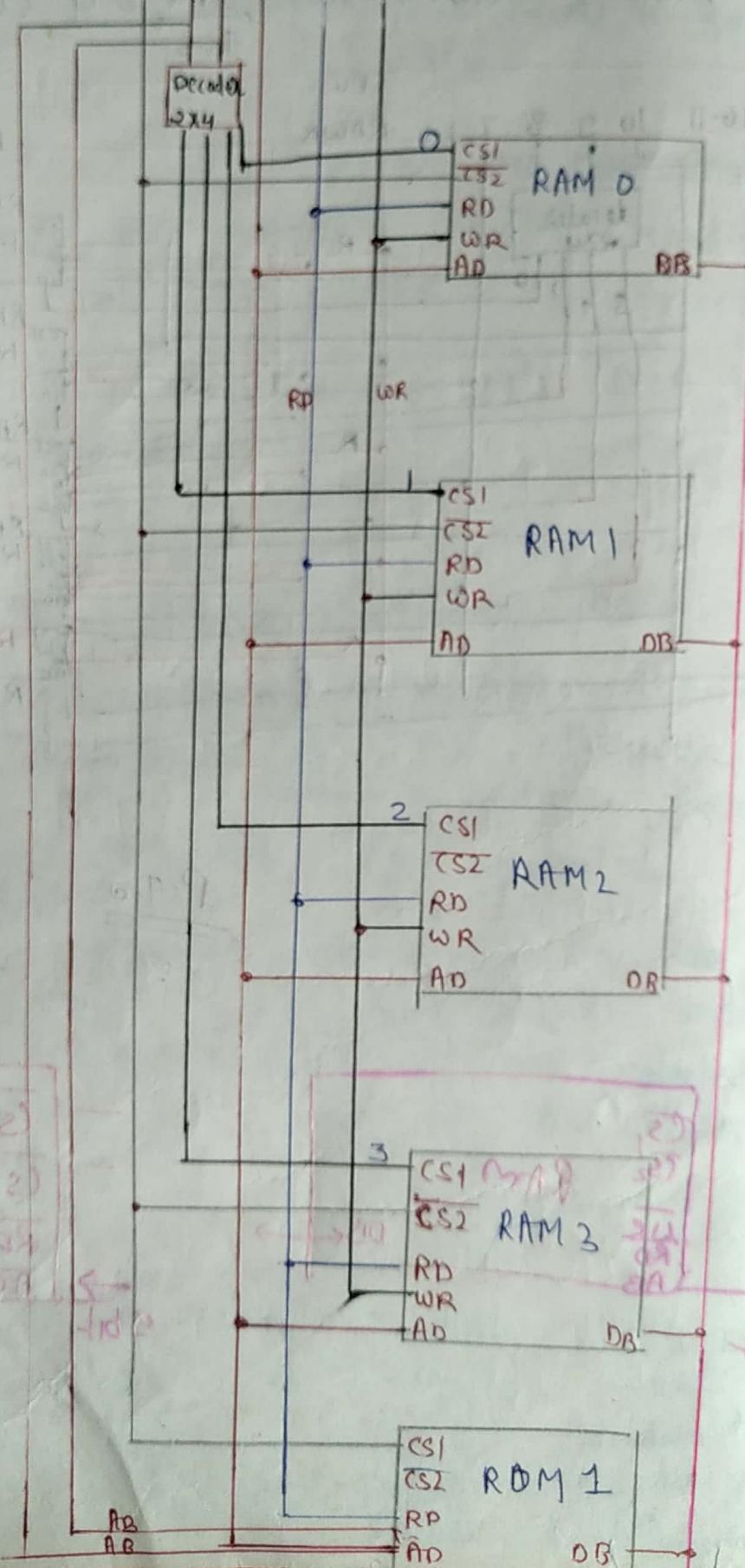


$$\begin{aligned} & \frac{4}{(128 \times 4) \times 8} + \frac{1}{512 \times 8} \\ &= 512 \times 8 \\ &+ 512 \times 8 \\ &= 1024 \times 8 \end{aligned}$$



CPU

Ad 16 15 14 13 12 11 10 9 8 7-1 RD WR data bus DB  
7-8 1-8



## Address Mapping

Address:-		16 - 11	10	9	8	7	6	5	4	3	2	1
Chip	↓	0000	0	0	0	0	0	0	0	0	0	0
RAM0	0000-00FF		0	0	0	1	1	1	1	1	1	1
RAM1	0080-00FF		0	0	1	0	0	0	0	0	0	0
RAM2	0100-017F		0	1	0	0	0	0	0	0	0	0
RAM3	0180-01FF		0	1	1	0	0	0	0	0	0	0
RAM4	0200-03FF		1	0	0	0	0	0	0	0	0	0
			1	1	1	1	1	1	1	1	1	1

Ques How many 128x8 chip needed to provide a mem capacity of 2048 byte

- (A) Ans How many line address bus must be used to access 2048 byte memory
- (B) How many this line will be common to all chip
- (C) How many line are used (decoded) to specify the size of chip

$$\begin{aligned}
 & \frac{2^{10}}{128} \times 2 \times 8 = 2^4 \\
 & \frac{2048}{128} \times 8 = \frac{2^11}{2^7} = 2^4 = 16 \text{ chip}
 \end{aligned}$$

11 address  
8 data line

Mem chip = 2048 byte

No. of RAM chip =  $\frac{\text{Mem. chip}}{\text{size of RAM}}$

$$\text{No. of RAM chip} = \frac{2048 \times 8}{128 \times 8} = 16$$

(a) address line =  $2^{11} \times 8$   
= 11 address line

(b) command to address line =  $128 \times 8 - 0010$   
 $2^7 \times 8 - 1110$   
= 7 address

(c) decoded bit use = 4 bit

4 line must be decoded  $4 \times 16$ , size  
of decoded

A Micro processor use RAM chip  $1024 \times 1$   
Capacity

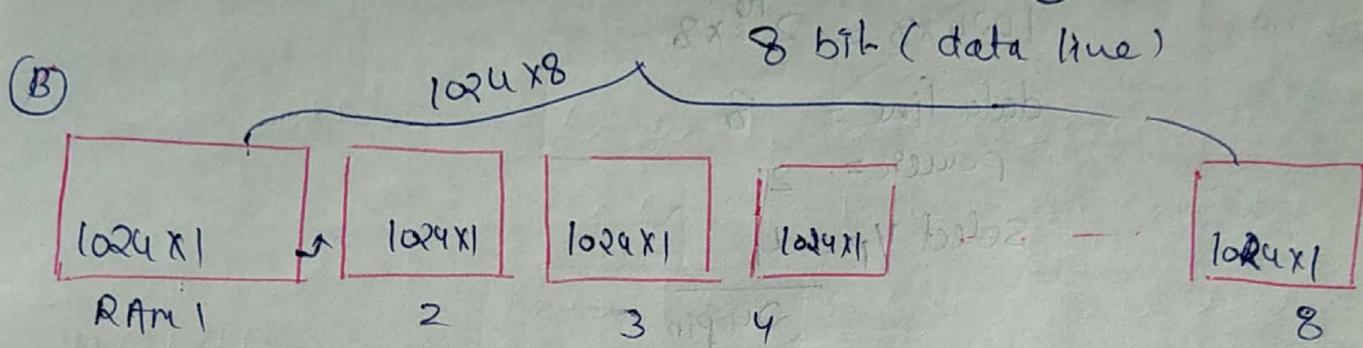
- (A) How many chips are needed & How  
should there add line be connected  
to provide the mem. capacity of  
1024 byte.
- (B) How many chips are needed to  
provide a mem capacity 16 KB  
explain in word How the add. are  
connected to the address bus.

① RAM chip - T024 x 1

$$\text{No. of RAM} = \frac{\text{Mem. Capa}u}{\text{Size of Ram}} = \frac{1024 \times 8}{1024 \times 1} = 8$$

$$\text{address line} = 10 = 12^{10} = 1024$$

10 address line connected to chip



## Parallel Connection.

(B) 16 K.B

$$\text{No. of RAM} = \frac{\text{Mem. capacity}}{\text{Size of 1 byte}} = \frac{16 \text{ K} \times 8}{1024 \times 1} = 128$$

$$\text{Address line} = 16 \times 2^{10} \times 8 = 2^{14} \times 8$$

= 14 bit use

0000	0,01	$R_1$	$R_2$	$R_8$
0001	1	$R_1$	$R_2$	$R_8$
15				

Ques A Rom chip of  $1024 \times 8$  has 4 select I/P & operate from a 5 volt power supply How many pins for IC packages

$$1024 \times 8 = 2^{10} \times 8$$

$$\text{data line} = 8$$

$$\text{power} = 2$$

$$\text{Select I/P} = 4$$

24 pin

A Computer employ RAM chip of  $256 \times 8$  and Rom chip of  $1024 \times 8$  RAM & ROM needed the comp. sys needed 4 interface unit each with 4 register a memory map I/O configuration is used The 2 highest order bits of the address bus are assign 00 for RAM 01 for ROM 10 for interface register How many add. RAM ROM chip are needed give the RAM, ROM & Interf for RAM -  $256 \times 8$  -  $2^7 \times 8$  7 address Rom -  $1024 \times 8$  -  $2^{10} \times 8$  10 address

Needed memory

2KB - RAM

4KB - ROM

4 - Interface Each with 4 regis

$$\text{No. of RAM} = \frac{\frac{256 \times 8}{\text{given}}}{2^8 \times 8} = \frac{2 \times 10^3}{2^8 \times 8}$$

$$\text{No. of ROM} = \frac{\frac{\text{total memory size}}{\text{given ROM size}}}{2^8 \times 8} = 8$$

Rough

$$\begin{aligned} \text{RAM} &= 2K \\ &= 2^1 \times 10^3 \\ &= 11 \end{aligned}$$

ROM

$$\begin{aligned} 4K &= 2^2 \times 10^3 \\ &= 16 \end{aligned}$$

IR 16

0000  
1111

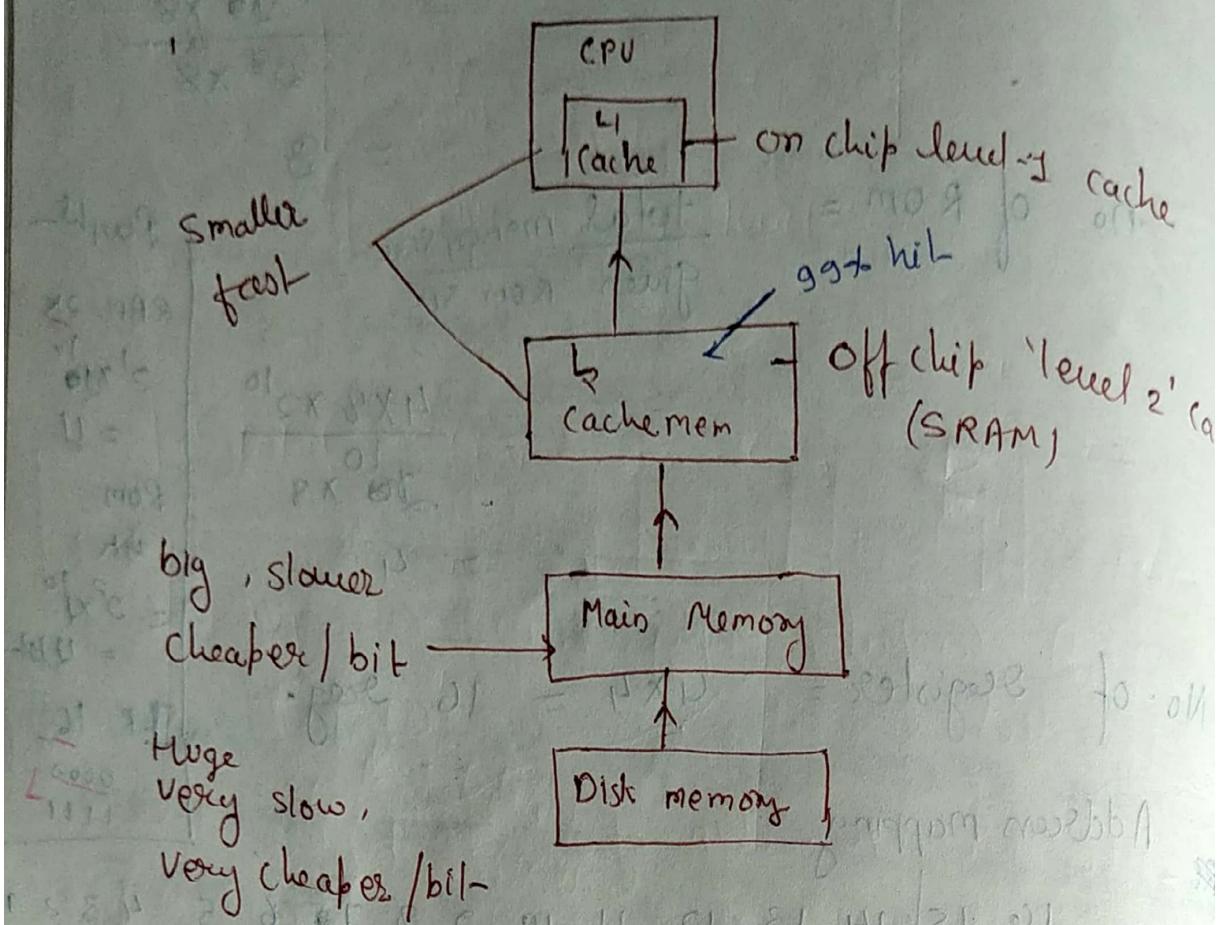
$$\text{No. of Register} = 4 \times 4 = 16 \text{ Reg.}$$

RF Address mapping

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X
0000-0FFF	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
ROM	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
4000-4FFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IR	1	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X
8000-800F	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

# Memory Capacity Planning



There are 3 technology

① Hit Ratio :- When an information item is found

hit at  $m_i [m_1, m_2, m_3, \dots]$  it is a hit  
else it is a miss so we define the

hit ratio  $H_i$  at  $m_i$  as the probability  
that a an information item  
found in  $m_i$  will be

So miss ratio of  $m_i$  is

$$M_i = 1 - H_i$$

The hit ratio are independent  
with there var value Q to 1

$$\text{Hit ratio} = \frac{\text{no of hit}}{\text{no of hit} + \text{no. of miss}}$$

The access frequency to  $M_i$  is level is given by

$$f_i = (1-h_1)(1-h_2) \dots (1-h_{i-1}) h_i$$

Ex If memory Hierarchy level is 3

$$f_3 = (1-h_1)(1-h_2) h_3$$

$$\sum_{i=1}^n f_i = 1$$

$$f_1 > f_2 > f_3 > f_i$$

This implies that in the levels of memory are accessed more often than outer level of the memory

(2) Effective access type  $T_{eff}$  of a memory

key is defined as follows

$$T_{eff} = h_1 t_1 + (1-h_1) h_2 t_2 + (1-h_1)(1-h_2) h_3 t_3 + \dots + (1-h_1)(1-h_2) \dots (1-h_{i-1}) h_i t_i$$

Ex:- If MH is 2 level (Memory hierarchy - MH)

$$T_{eff} = h_1 t_1 + (1-h_1) h_2 t_2$$

$T_{eff}$  depends on the program behaviour and the memory design choice

$h_1$  = hit ratio of level 1

$t_1$  = access time of  $h_1$

more priority to hit ratio

for program access

Total cost of Memory hierarchy :-

Is define as

⇒

$$C_{\text{total}} = \sum_{i=1}^n C_i S_i$$

Ex

if MH is 3 level

$S_i$  = size of

$$C_{\text{total}} = C_1 S_1 + C_2 S_2 + C_3 S_3$$

$C_i$  = cost / bits/byte

⇒

$$C_{\text{avg}} = \frac{\sum_{i=1}^n C_i S_i}{\sum_{i=1}^n S_i}$$

Ex

$$C_{\text{avg}} = \frac{C_1 S_1 + C_2 S_2 + C_3 S_3}{S_1 + S_2 + S_3}$$

Ques NH - based program

Consider a 2 level memory Hierarchy let

$H_1, H_2$  denote hit ratio  $H_1 \neq H_2$

$C_i S_i$  cost be the cost/kg bit

$S_1, S_2 \rightarrow$  memory capacity,  $t_1, t_2 \rightarrow$  access time

- (a) Under what condition will the avg cost of entire memory sys approach  $S_2$
- (b) find  $T_{\text{eff}}$  or  $T_{\text{avg}}$  of hit this hiear.
- (c) let  $\gamma = \frac{t_2}{t_1}$  be the speed ratio of 2 memory  
let  $E = t_1/t_2$  be the access efficiency of memory

Express E in term of  $\gamma$  & H

- (a) plot E against H for  $R = 5, 20 \& 100$  respectively - by graph
- (b) What is the hit factor h to make  $E > 0.95$  if  $\gamma = 100$

(a)  $C_{avg} = \frac{G \cdot S_1 + G \cdot S_2}{S_1 + S_2}$

if  $S_2 \gg S_1$

$S_2 \approx 0$

$$C_{avg} = \frac{G S_2}{S_2} = C_2$$

for  $C_{avg}$  to approach  $C_2$  condition is,  
 $S_2 \gg S_1$

(b)  $T_{eff} = h t_1 + (1-h) h_2 t_2$  given  $h_2 = h_1$   
 $h_1 = h$

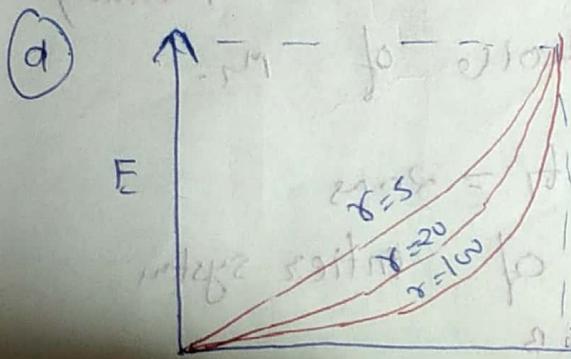
$$T_{eff} = T_a = h t + (1-h) h t_2$$

(c) given  $\gamma = \frac{t_2}{t_1}$

$$E = \frac{t_1}{T_a}$$

$$E = \frac{t_1}{h t_1 + (1-h) h t_2} = \frac{1}{h + (1-h) \frac{t_2}{t_1}}$$

$$E = \frac{1}{h + (1-h) \gamma}$$



(e)  $E > 0.95, \gamma = 100$

$$\frac{1}{h + (1-h) \gamma} > 0.95$$

$$\frac{1}{h + (1-h) 100} > 0.95$$

$$h = 99.95\%$$

Given that in a 2 level virtual memory  $t_{q_1} = 10^{-7}$  sec find h ? It shows that at least 90 %.

$t_{q_2} = 10^{-2}$  sec

$$\gamma = \frac{t_{q_1}}{t_{q_2}} = \frac{10^{-7}}{10^{-2}} = 10^5$$

$$E = \frac{1}{h + (1-h)\gamma}$$

$$0.9 = \frac{1}{h + (1-h)10^5}$$

$$0.9h + (1-h)10^5 \times 0.9 = 1$$

$$0.9h = 10^5 \times 0.9h + 90000 = 1$$

$$h = 99.99\%$$

Ques You are ask to perform capacity planning for a 2 level memory system.

$S_1$  ( $m_1$  cache) has 3 choices :- 64 kB, 128 kB & 256 kB  
 $S_2$  ( $m_2$  Main Memory) has 4 MB capacity  
 given that

$$C_1 = 20 \text{ C}_2$$

$$t_1 = 10^{-7}$$

$$\gamma = \frac{10^{-7}}{10^{-2}}, \quad \gamma = 10$$

Cache hit ratio 0.7, 0.9 & 0.98 respectively  
 for above 3 choice of  $m_1$ .

(A) find  $t_{q_1}$  in term of  $t_1 = 20 \text{ ns}$

(B) find Avg. byte cost of entire system

$$S = \$ 0.2 / \text{KB}$$

① Compose the 3 memory design.

given -  $\sigma = 10$ ,  $G = 20 \text{ C}_2$ ,  $t_Q = 10\text{t}_1$ ,

② (i)  $T_{eff} = h_1 t_1 + (1-h_1) h_2 t_2 + (h_1 h_2)(1+h_2) t_3 h_3$

64  $T_a = 0.7 \times 20 \times 10^9 + (1-0.7) 10 \times 20 \times 10^9$

$T_a = (0.7 \times 20 + (1-0.7) 200) \times 10^9$   
 $= (1.4 + 0.3 \times 200) \times 10^9$

$= (1.4 + 60) 10^9 \text{ ns} = 74 \text{ ns}$

$T_a = 74 \text{ ns}$

putting (i)  $T_a = [h_1 + (1-h_1) \times 10] t_1$

$1000 \times h_1 \times 0.3 = 10 \text{ ns} \quad T_a = 38 \text{ ns}$

$h_1 = 0.99 \quad T_a = 23.6 \text{ ns}$

③  $200 \cdot 0.0 = 12 \quad \text{Avg} = \frac{G(S_1 + S_2 S_2)}{S_1 + S_2}$

$\text{Avg} = \frac{20 G_1 S_1 + G_2 S_2}{21 S_1 + S_2}$

$\text{Avg} = \frac{20 \times 0.2 \times S_1 + 0.2 \times 4 \times 1024}{S_1 + 400}$

$\text{Avg} = \frac{4 S_1 + 800}{S_1 + 400}$

$S_1 = 64 \text{ KB} = \text{Avg} = 0.26$

$S_2 = 128 \text{ KB}, \text{ Avg} = 0.32$

$S_3 = 256 \text{ KB}, \text{ Avg} = 0.43$

for the design choice the product access time and Avg. Cost is

① 1<sup>st</sup> Product

2<sup>nd</sup>

3<sup>rd</sup>

$$S_1 \times C_{Avg} + T_a = \text{Product}$$

$$S_1 \times C_{Avg} \times T_a = 19.24$$

$$11 + 12.16 = 23.16$$

$$11 + 10.18 = 21.18$$

The 3<sup>rd</sup> option are Best choice.

Consider the 2 level M-H  $M_1$  &  $M_2$

Access time are  $T_1$  &  $T_2$

cost / byte are  $C_1$  &  $C_2$  & capacity

are  $S_1$  &  $S_2$  respectively

$H_1 = 0.95$ , at the 1<sup>st</sup> level

① find  $t_{eff}$  for the memory sys.

② Total cost -

③  $t_1 = 20 \text{ ns}, S_1 = 512 \text{ KB}, C_1 = 0.01 \text{ /byte}, S = \$0.00$

$$\rightarrow h_1 t_1 + (1-h_1) h_2 t_2$$

The cost of the sys is upper bounded by

\\$15000 &  $T_{eff}$  is 40 ns. what

are  $S_2$  &  $t_2$

$$\textcircled{A} \quad T_{\text{eff}} = h_1 t_1 + (1-h_1) t_2$$

$$= 0.95 t_1 + (1-0.95) t_2 \text{ (approx)}$$

$$T_{\text{eff}} = 0.95 t_1 + 0.05 t_2$$

problem

10001

\textcircled{B}

$$\text{total Avg} = \frac{C_1 S_1 + C_2 S_2}{S_1 + S_2}$$

$$C_{\text{total}} = C_1 S_1 + C_2 S_2$$

\textcircled{C}

$$T_{\text{eff}} = 0.95 t_1 + 0.05 t_2$$

$$40 \text{ ns} = 0.95 \times 20 + 0.05 \times t_2$$

$$t_2 = 42 \text{ ns}$$

$$C_{\text{total}} = C_1 S_1 + C_2 S_2$$

$$1500 = 0.01 \times 512 \times 1024 + 0.005 \times S_2$$

$$15000 = 512 \times 1000 + 0.005 \times S_2$$

$$15000 - 5120 = 5120 + 0.005 \times S_2$$

$$\frac{10880 \times 1000}{0.005} = S_2$$

$$21760 \quad S_2 \quad S_2 = 18.4$$

Consider  
to the  
and  
data

$M_1$  &  $M_2$   $\rightarrow M_1$  is directly connected  
CPU determining the Avg. cost / byte  
the Aug. access time for the  
given below.

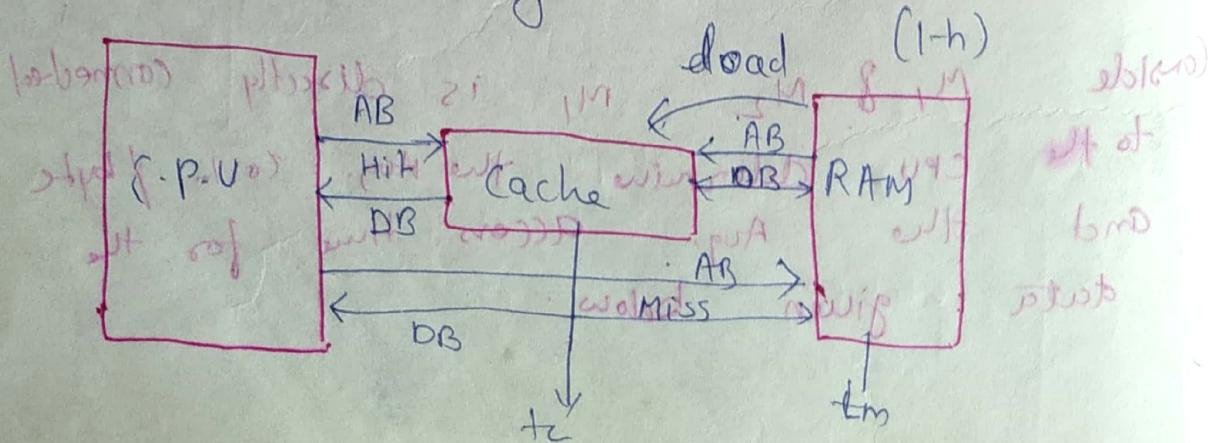
Memory level	Capacity	Cost	Access time	Hit H
M <sub>1</sub>	1024	0.1	10 <sup>-8</sup>	0.9
M <sub>2</sub>	2 <sup>16</sup>	0.01	10 <sup>-6</sup>	-

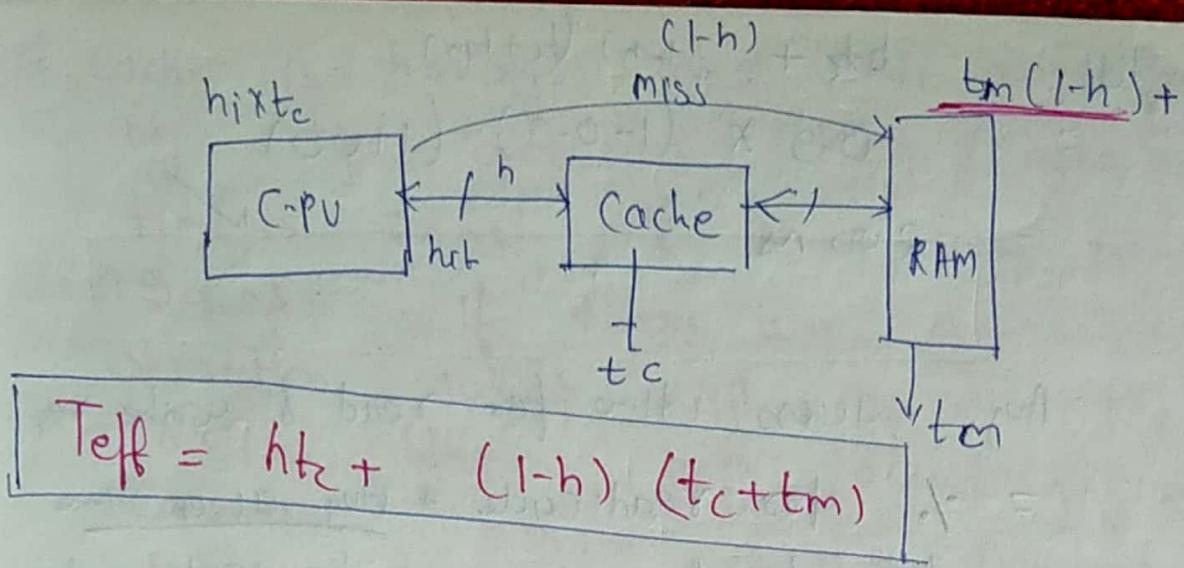
$$C_{avg} = \frac{C_1 S_1 + C_2 S_2}{S_1 + S_2} = \frac{0.1 \times 1024 + 0.01 \times 2^{16}}{1024 + 2^{16}} = 0.01138$$

$$T_u = h_1 t_1 + (1-h_1) t_2 \\ = 1.09 \times 10^{-7}$$

## Cache Memory

- It is stand b/w RAM & CPU
- It is also a RAM [ static RAM (SRAM) ]  
→ transistor
- It is faster Memory No need of buffer
- It contains most heavily used data





Ques The access time of a cache memory is 100 ns. It is estimated that of main memory 1000 n request for read cycle and the hit Ratio for write cycle through processes of use.

- (A) What is the avg. access time of a sys. Considering that is the avg. access time of the sys for both read & write request,
- (B) What is the hit ratio taking in to consideration the write cycle,

Given :-  $t_c = 100 \text{ ns}$   
 $t_m = 1000 \text{ ns}$

Read

$$T_{eff} = h \cdot t_c + (h+1)(t_c + t_m)$$

$$T_{eff} = [0.9 \times 100 + (0.1) (1000)] \approx 180 \text{ ns}$$

$$\begin{aligned}
 &= 0.9 \times (1-0.9) (1100) \\
 &= 200 \text{ ns}
 \end{aligned}$$

Q) Avg. access time for read & write  $\rightarrow$   
~~for read cycle + Avg. access time~~  
~~for read  $\approx$  + % for write  $\times b_m$~~   
~~of program 80% + 20%  $\times$  1000~~  
~~so I prompt access for point~~  
~~program  $\Rightarrow$  360 ns but below it is 360 ns~~  
~~minimum bus delay of 100 ns~~

Q) find hit ratio in write cycle  
~~row  $\times$  bus = 0.9  $\times$  0.9  $\times$  0.9  $\times$  1.0~~  
~~hit = % of read  $\times$  hit read~~  
~~+ % of write  $\times$  hit write~~

P) In case of write processor  $hw = 10$

~~hit for write  $\times$  0.9  $\times$  0.9~~

~~hit for write  $\times$  0.9  $\times$  0.9~~

~~hit for write  $\times$  0.9  $\times$  0.9~~

Our Cache is having 80% hit ratio for only read operation so let Cache access time is 20ns & M-M access time 120ns. If there are 60% write operation what will be the hit ratio when both read and write consider. Assume what is the Avg. for both read & write requests.

Given

$$t_c = 20\text{ ns}$$

$$t_m = 120\text{ ns}$$

$$80\% \times (1 - 1)$$

$$\text{dps out} = ?$$

$$h = 0.8$$

$$\% W \text{ op} = 60\%$$

$$\therefore \text{Read} \rightarrow 40\%$$

$$\text{Avg.} = 40\% \times 0.8 + 60\% \times 0 \\ \cdot 32$$

Find Avg for both read and write request

= % Read of  $\times$  Avg access time for

A word read with write for命中 + 60% for miss

$$\text{for read} = 0.40 \times 32 + 0.60 \times 120$$

$$\text{for write} = 0.40 \times [h t_c + (1-h) (t_c + t_m)] + 0.60 \times t_m$$

$$\text{dps out} = 0.40 \times [0.8 \times 32 + (0.2)(120 + 20)] + 0.60 \times 120$$

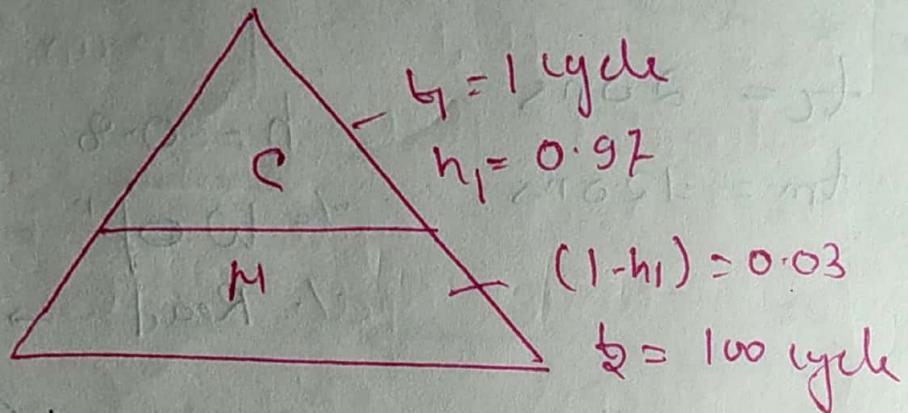
$$\text{dps out} = 0.40 \times [0.8 \times 32 + (0.2)(120 + 20)] + 0.60 \times 120$$

A memory consists of a cache and a main memory. If it takes one cycle to complete a cache hit & 100 cycles to complete a cache miss.

A cache miss what is the average access time if the hit rate in the cache is

97.0%.

What is the average access time if the hit rate in the cache is 97%.



$$= h_{\text{hit}} t_{\text{hit}} + h_{\text{miss}} t_{\text{miss}}$$

$$= 0.97 \times 1 + 0.03 \times 100$$

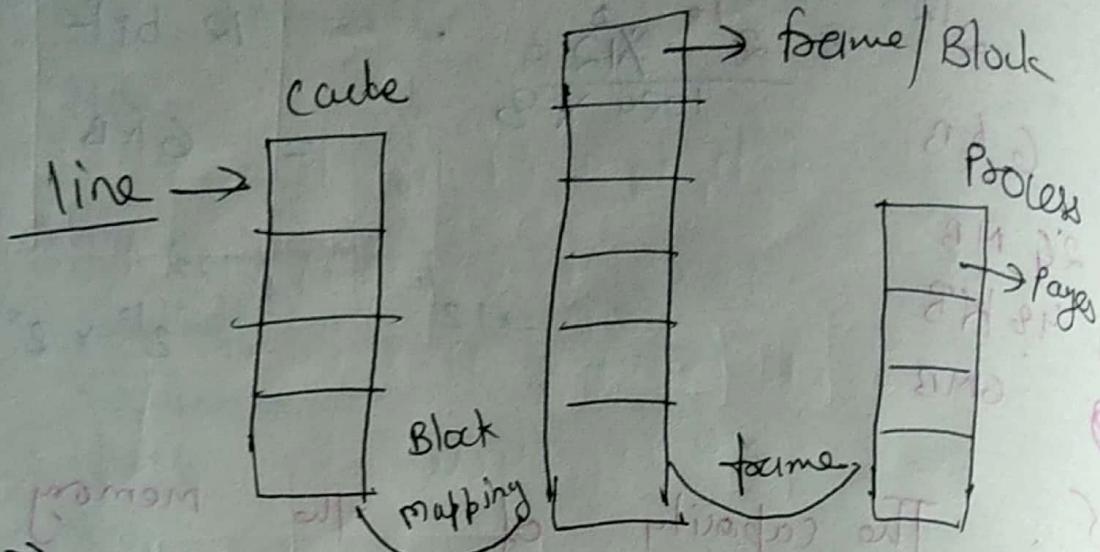
$$= 0.97 + 3$$

$$= 3.97 \text{ cycle.}$$

## Mapping

### Direct mapping

M.P



Assumption → Main Memory divided into frames / block  
(virtually)

Cache → It divided into lines

Each Block size is equal to the line

### Question

(1)  $w = 1B$  assum.)

Main memory 64 words and cache having 16 words and Size of block  $\leq$  word  
given

Size of Block = 4 words

① No of Block in Main memory = ?

$$= \frac{64}{4} = 16 \text{ block}$$

# Main Memory

0	0 1 2 3	4 words
1	4 5 6 7	
2	8 9 10 11	
3	12 13 14 15	
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15	60 61 62 63	64 word

Q2 No. of line in cache  $\rightarrow$  2

In cache No. of Block = 16

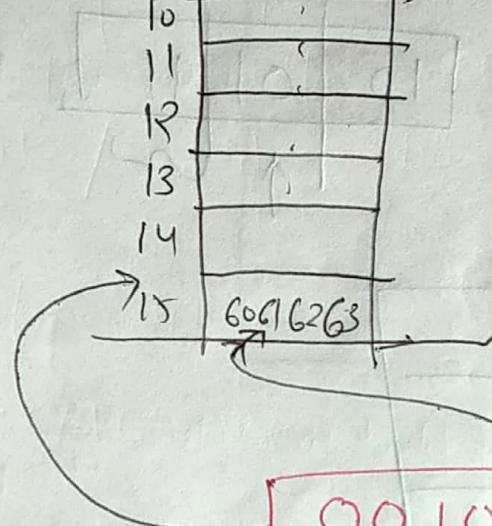
$$\text{line} = \frac{16 \text{ word}}{4 \text{ word}}$$

~~10 10 11 11~~  
 $= 4 \text{ line}$

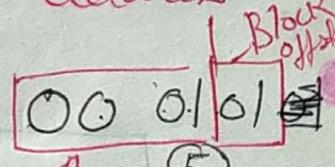
Cache

0	0 4 8 12
1	1 5 9 13
2	2 6 10 14
3	3 7 11 15

RR manner



(CPU generates 6 bit for address)



Block no.

Block off set

Block Nb.

