```
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/two_level.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 16 2025 20:23:31
gem5 executing on 5cb9d529d43a, pid 39
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/two_level.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
```

RAM 0.83 GB CPU 0.62% Disk: 15.03 GB used (limit 1006.85 GB) >_ Terminal

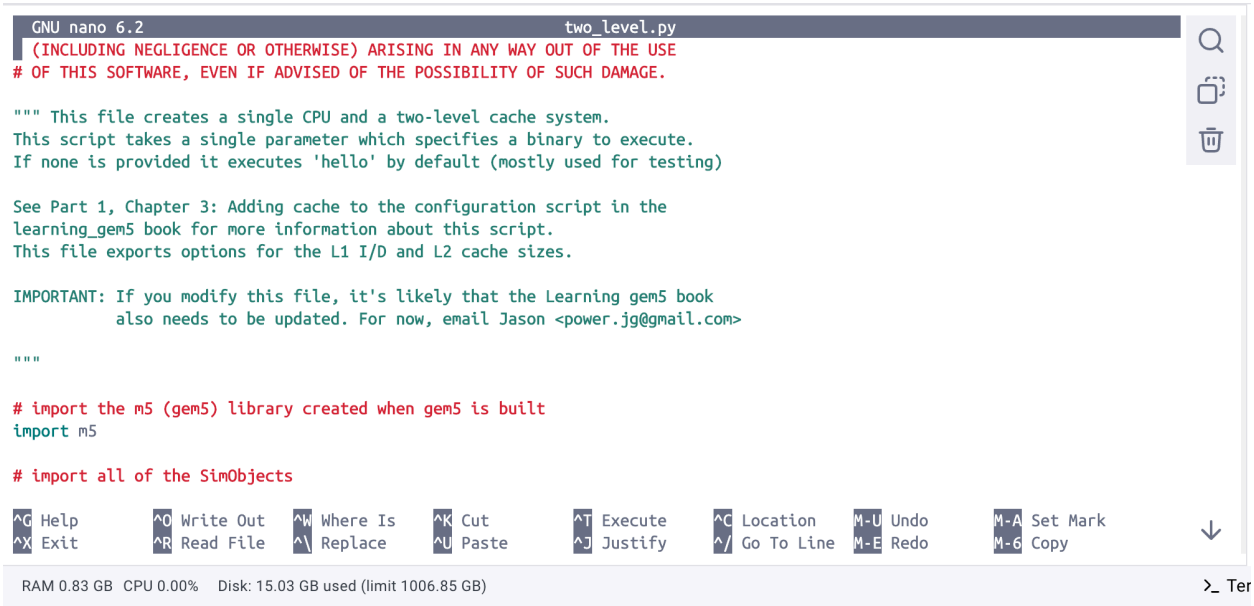
Successful simulation of two level cache configuration, /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/two_level.py

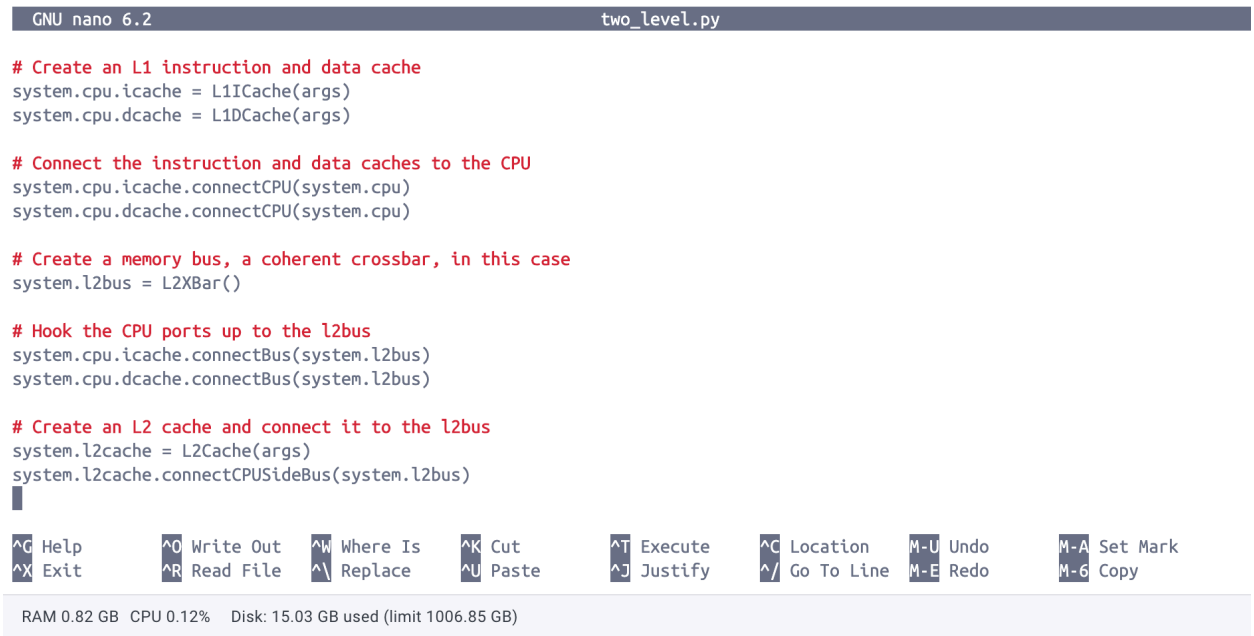
This python file has L1 and L2caches. From the below statistics we can see that the L2 cache miss rate is high with 98%

Statistics:

Cache Performance Metrics

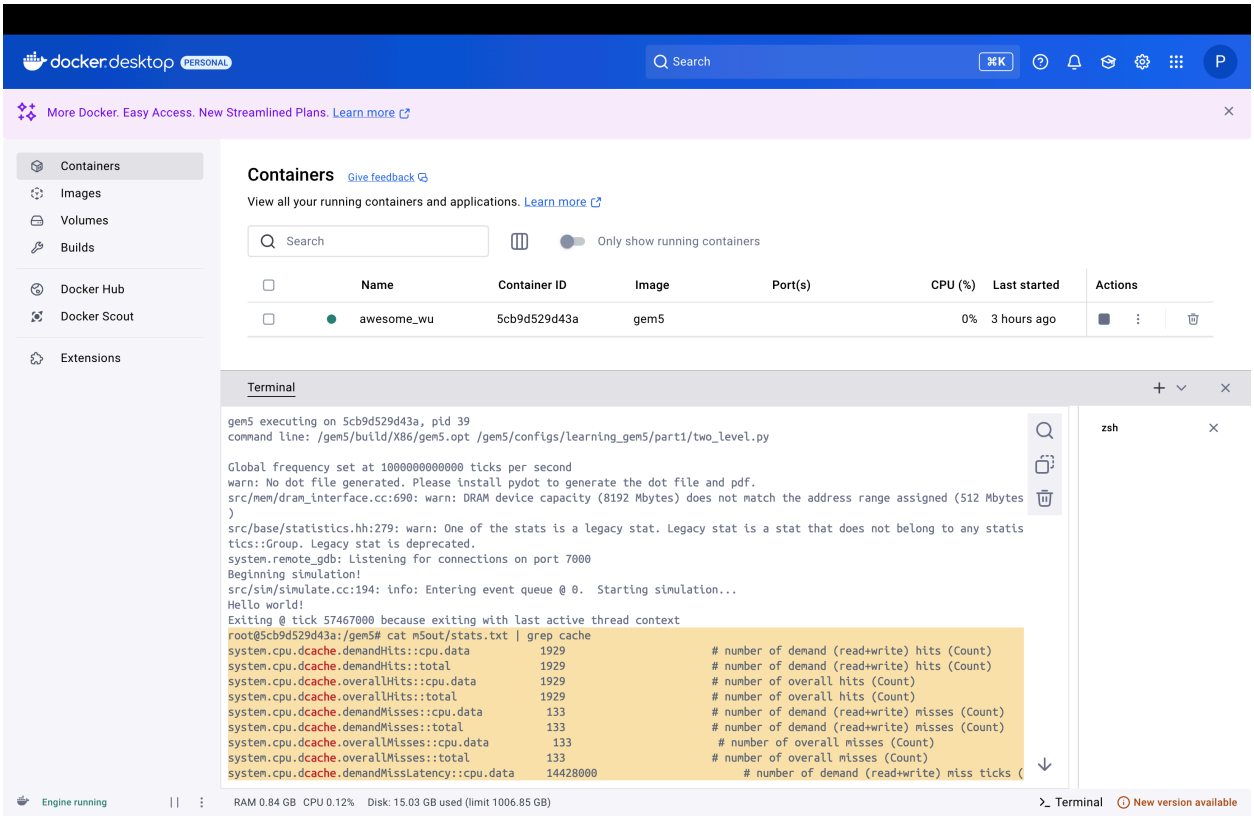
	Metric	Value
1	L1 DCache Hits	1929.0
2	L1 DCache Misses	133.0
3	L1 DCache Miss Rate	0.0645
4	L1 ICache Hits	7680.0
5	L1 ICache Misses	234.0
6	L1 ICache Miss Rate	0.02957
7	L2 Cache Hits	6.0
8	L2 Cache Misses	361.0
9	L2 Cache Miss Rate	0.98365
10	L1 DCache Avg Miss Latency	108481.2
11	L1 ICache Avg Miss Latency	101799.1
12	L2 Cache Avg Miss Latency	100515.2





cat m5out/stats.txt | grep cache, This is the command used to get the statistics related to Cache.

Above pictures shows the python file I ran that has CPU, L1,L2 caches set.



Build command: **/gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/two_level.py**

Statistics for two level.py:

```
root@5cb9d529d43a:/gem5# cat m5out/stats.txt | grep cache
system.cpu.dcache.demandHits::cpu.data          1929                # number of demand
(read+write) hits (Count)
system.cpu.dcache.demandHits::total             1929                # number of demand
(read+write) hits (Count)
system.cpu.dcache.overallHits::cpu.data         1929                # number of overall hits
(Count)
system.cpu.dcache.overallHits::total            1929                # number of overall hits (Count)
system.cpu.dcache.demandMisses::cpu.data         133                # number of demand
(read+write) misses (Count)
system.cpu.dcache.demandMisses::total            133                # number of demand
(read+write) misses (Count)
system.cpu.dcache.overallMisses::cpu.data        133                # number of overall misses
(Count)
system.cpu.dcache.overallMisses::total           133                # number of overall misses
(Count)
system.cpu.dcache.demandMissLatency::cpu.data    14428000           # number of
demand (read+write) miss ticks (Tick)
system.cpu.dcache.demandMissLatency::total    14428000              # number of demand
(read+write) miss ticks (Tick)
```

system.cpu.dcache.overallMissLatency::cpu.data 14428000 # number of overall miss ticks (Tick)
system.cpu.dcache.overallMissLatency::total 14428000 # number of overall miss ticks (Tick)
system.cpu.dcache.demandAccesses::cpu.data 2062 # number of demand (read+write) accesses (Count)
system.cpu.dcache.demandAccesses::total 2062 # number of demand (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::cpu.data 2062 # number of overall (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::total 2062 # number of overall (read+write) accesses (Count)
system.cpu.dcache.demandMissRate::cpu.data 0.064500 # miss rate for demand accesses (Ratio)
system.cpu.dcache.demandMissRate::total 0.064500 # miss rate for demand accesses (Ratio)
system.cpu.dcache.overallMissRate::cpu.data 0.064500 # miss rate for overall accesses (Ratio)
system.cpu.dcache.overallMissRate::total 0.064500 # miss rate for overall accesses (Ratio)
system.cpu.dcache.demandAvgMissLatency::cpu.data 108481.203008 # average overall miss latency in ticks ((Tick/Count))
system.cpu.dcache.demandAvgMissLatency::total 108481.203008 # average overall miss latency in ticks ((Tick/Count))
system.cpu.dcache.overallAvgMissLatency::cpu.data 108481.203008 # average overall miss latency ((Tick/Count))
system.cpu.dcache.overallAvgMissLatency::total 108481.203008 # average overall miss latency ((Tick/Count))
system.cpu.dcache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.cpu.dcache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.cpu.dcache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dcache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dcache.demandMshrMisses::cpu.data 133 # number of demand (read+write) MSHR misses (Count)
system.cpu.dcache.demandMshrMisses::total 133 # number of demand (read+write) MSHR misses (Count)
system.cpu.dcache.overallMshrMisses::cpu.data 133 # number of overall MSHR misses (Count)
system.cpu.dcache.overallMshrMisses::total 133 # number of overall MSHR misses (Count)
system.cpu.dcache.demandMshrMissLatency::cpu.data 14162000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.dcache.demandMshrMissLatency::total 14162000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.dcache.overallMshrMissLatency::cpu.data 14162000 # number of overall MSHR miss ticks (Tick)

system.cpu.dcache.overallMshrMissLatency::total 14162000 # number of overall MSHR miss ticks (Tick)
system.cpu.dcache.demandMshrMissRate::cpu.data 0.064500 # mshr miss ratio for demand accesses (Ratio)

```
33:        # Connect L1 to L2 ◆
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# grep --color='auto' -P -n "[^\x00-\x7F]" /gem5/configs/learning_gem5/par
t1/simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/simple_cache_
sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:56:27
gem5 executing on 5cb9d529d43a, pid 172
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/simple_cache_sim.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes
)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statis
tics::Group. Legacy stat is deprecated.
src/cpu/base.cc:181: fatal: Number of ISAs (0) assigned to the CPU does not equal number of threads (1).
Memory Usage: 624712 KBytes
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1#
```

`simple_cache_sim.py,` I tried building this python file with the caches, CPU set

For **caches.py** but I am getting errors.

```
import m5
from m5.objects import System, SrcClockDomain, VoltageDomain, TimingSimpleCPU,
SystemXBar, Root, MemCtrl, DDR3_1600_8x8
from caches import L1ICache, L1DCache, L2Cache

class MySystem(System):
```

```
    def __init__(self, opts):
        super(MySystem, self).__init__()

        # Set up system
        self.clk_domain = SrcClockDomain()
        self.clk_domain.clock = "1GHz"
        self.clk_domain.voltage_domain = VoltageDomain()

        self.mem_mode = "timing"
        self.mem_ranges = [m5.objects.AddrRange("512MB")]

        # Create CPU
        self.cpu = TimingSimpleCPU()

        # Attach L1 caches
        self.cpu.icache = L1ICache(opts)
        self.cpu.dcache = L1DCache(opts)
        self.l2cache = L2Cache(opts)

        # Create system buses
        self.l2bus = SystemXBar()
        self.membus = SystemXBar()  # Main memory bus

        # Correct L1 connections
        self.cpu.icache.cpu_side = self.cpu.icache_port
        self.cpu.dcache.cpu_side = self.cpu.dcache_port

        # Connect L1 to L2
        self.cpu.icache.connectBus(self.l2bus)
        self.cpu.dcache.connectBus(self.l2bus)
        self.l2cache.connectCPUSideBus(self.l2bus)

        # Connect L2 cache to memory bus
        self.l2cache.connectMemSideBus(self.membus)

        # Create memory controller
        self.mem_ctrl = MemCtrl()
        self.mem_ctrl.dram = DDR3_1600_8x8()
        self.mem_ctrl.dram.range = self.mem_ranges[0]

        # Connect memory controller to system bus
        self.mem_ctrl.port = self.membus.mem_side_ports

# Create system and root object
opts = None  # Use default options
system = MySystem(opts)
root = Root(full_system=False, system=system)

# Instantiate the simulation
m5.instantiate()
print("Beginning gem5 simulation...")
exit_event = m5.simulate()
print(f"Exiting @ tick {m5.curTick()} because {exit_event.getCause()}")
```

Terminal Logs:

```
pushyamithrakotakonda@Pushyas-MacBook-Air ~ % docker ps
CONTAINER ID   IMAGE     COMMAND   CREATED       STATUS       PORTS     NAMES
5cb9d529d43a   gem5      "bash"    3 weeks ago   Up 2 hours             awesome_wu
pushyamithrakotakonda@Pushyas-MacBook-Air ~ % docker exec -it awesome_wu bash

root@5cb9d529d43a:/gem5# ls
CODE-OF-CONDUCT.md  MAINTAINERS.yaml  TESTING.md   ext      optional-requirements.txt
site_scons
CONTRIBUTING.md     README           build        hello    plot_stats.py            src
COPYING             RELEASE-NOTES.md  build_opts   hello.c  pyproject.toml           system
KCONFIG.md          SConsopts        build_tools  include  requirements.txt         tests
LICENSE             SConstruct       configs      m5out    run_hello.py             util
root@5cb9d529d43a:/gem5#
root@5cb9d529d43a:/gem5# cd build
root@5cb9d529d43a:/gem5/build# ls
ARM  X86
root@5cb9d529d43a:/gem5/build# cd X86
root@5cb9d529d43a:/gem5/build/X86# ls
arch  config  debug  enums  gem5.build  gem5py    kern          mem     proto  sim  systemc
base  cpu     dev    ext    gem5.opt    gem5py_m5  learning_gem5  params  python  sst
root@5cb9d529d43a:/gem5/build/X86# build/X86/gem5.opt configs/example/gem5_library/
simple-cache.py
bash: build/X86/gem5.opt: No such file or directory
root@5cb9d529d43a:/gem5/build/X86# ls -l gem5.opt
-rwxr-xr-x 1 root root 772096568 Feb  1 20:01 gem5.opt
root@5cb9d529d43a:/gem5/build/X86# ./gem5.opt ../../configs/example/gem5_library/simple-
cache.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 16 2025 20:19:08
gem5 executing on 5cb9d529d43a, pid 30
command line: ./gem5.opt ../../configs/example/gem5_library/simple-cache.py

Script ../../configs/example/gem5_library/simple-cache.py not found
Usage
=====
  gem5.opt [gem5 options] script.py [script options]

gem5 is copyrighted software; use the --copyright option for details.

Options
```

```
=======
--help, -h              show this help message and exit
--build-info, -B        Show build information
--copyright, -C         Show full copyright information
--readme, -R            Show the readme
--outdir=DIR, -d DIR    Set the output directory to DIR [Default: m5out]
--redirect-stdout, -r   Redirect stdout (& stderr, without -e) to file
--redirect-stderr, -e   Redirect stderr to file
--silent-redirect       Suppress printing a message when redirecting stdout or
                        stderr
--stdout-file=FILE      Filename for -r redirection [Default: simout]
--stderr-file=FILE      Filename for -e redirection [Default: simerr]
--listener-mode={on,off,auto}
                        Port (e.g., gdb) listener mode (auto: Enable if
                        running interactively) [Default: auto]
--allow-remote-connections
                        Port listeners will accept connections from anywhere
                        (0.0.0.0). Default is only localhost.
--interactive, -i       Invoke the interactive interpreter after running the
                        script
--pdb                   Invoke the python debugger before running the script
--path=PATH[:PATH], -p PATH[:PATH]
                        Prepend PATH to the system path when invoking the
                        script
--quiet, -q             Reduce verbosity
--verbose, -v           Increase verbosity
-c cmd                  program passed in as string (terminates option list)
-s                      IGNORED, only for compatibility with python. don'tadd
                        user site directory to sys.path; also PYTHONNOUSERSITE

Statistics Options
------------------
--stats-file=FILE       Sets the output file for statistics [Default:
                        stats.txt]
--stats-help            Display documentation for available stat visitors

Configuration Options
---------------------
--dump-config=FILE      Dump configuration output file [Default: config.ini]
--json-config=FILE      Create JSON output of the configuration [Default:
                        config.json]
--dot-config=FILE       Create DOT & pdf outputs of the configuration
                        [Default: config.dot]
--dot-dvfs-config=FILE  Create DOT & pdf outputs of the DVFS configuration
                        [Default: none]

Debugging Options
-----------------
--debug-break=TICK[,TICK]
                        Create breakpoint(s) at TICK(s) (kills process if no
                        debugger attached)
--debug-help            Print help on debug flags
--debug-flags=FLAG[,FLAG]
                        Sets the flags for debug output (-FLAG disables a
```

```
                    flag)
--debug-start=TICK      Start debug output at TICK
--debug-end=TICK        End debug output at TICK
--debug-file=FILE       Sets the output file for debug. Append '.gz' to the
                    name for it to be compressed automatically [Default:
                    cout]
--debug-activate=EXPR[,EXPR]
                    Activate EXPR sim objects
--debug-ignore=EXPR     Ignore EXPR sim objects
--remote-gdb-port=REMOTE_GDB_PORT
                    Remote gdb base port (set to 0 to disable listening)

Help Options
------------
--list-sim-objects      List all built-in SimObjects, their params and default
                    values
root@5cb9d529d43a:/gem5/build/X86# ls /gem5/configs/example/gem5_library/
arm-hello.py       power-hello.py           x86-npb-benchmarks.py
arm-ubuntu-run.py  riscv-fs.py              x86-parsec-benchmarks.py
checkpoints        riscv-ubuntu-run.py      x86-spec-cpu2006-benchmarks.py
dramsys            riscvmatched-fs.py       x86-spec-cpu2017-benchmarks.py
looppoints         riscvmatched-hello.py    x86-ubuntu-run-with-kvm.py
memory_traffic.py  x86-gapbs-benchmarks.py  x86-ubuntu-run.py
root@5cb9d529d43a:/gem5/build/X86# cd ..
root@5cb9d529d43a:/gem5/build# ls
ARM  X86
root@5cb9d529d43a:/gem5/build# cd ..
root@5cb9d529d43a:/gem5# ls
CODE-OF-CONDUCT.md  MAINTAINERS.yaml  TESTING.md   ext      optional-requirements.txt
site_scons
CONTRIBUTING.md     README            build        hello    plot_stats.py            src
COPYING             RELEASE-NOTES.md  build_opts   hello.c  pyproject.toml           system
KCONFIG.md          SConsopts         build_tools  include  requirements.txt         tests
LICENSE             SConstruct        configs      m5out    run_hello.py             util
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# ls
boot  common  deprecated  dist  dram  example  learning_gem5  network  nvm  ruby  splash2
topologies
root@5cb9d529d43a:/gem5/configs# cd example
root@5cb9d529d43a:/gem5/configs/example# ls
apu_se.py              gpufs          memtest.py              ruby_random_test.py
arm                    hmc_hello.py   noc_config              sc_main.py
dramsys.py             hmc_tgen.cfg   read_config.py          se.py
etrace_replay.py       hmctest.py     riscv                   sst
fs.py                  hsaTopology.py  ruby_direct_test.py
garnet_synth_traffic.py  lupv         ruby_gpu_random_test.py
gem5_library           memcheck.py    ruby_mem_test.py
root@5cb9d529d43a:/gem5/configs/example# cd ..
root@5cb9d529d43a:/gem5/configs# ls
boot  common  deprecated  dist  dram  example  learning_gem5  network  nvm  ruby  splash2
topologies
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# ls
README  part1  part2  part3
```

root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
caches.py simple-arm.py simple-riscv.py simple.py two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# **/gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/two_level.py**
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb 1 2025 19:59:14
gem5 started Feb 16 2025 20:23:31
gem5 executing on 5cb9d529d43a, pid 39
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1**/two_level.py**

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 57467000 because exiting with last active thread context
root@5cb9d529d43a:/**gem5# cat m5out/stats.txt | grep cache**
system.cpu.dcache.demandHits::cpu.data   1929   # number of demand (read+write) hits (Count)
system.cpu.dcache.demandHits::total   1929   # number of demand (read+write) hits (Count)
system.cpu.dcache.overallHits::cpu.data   1929   # number of overall hits (Count)
system.cpu.dcache.overallHits::total   1929   # number of overall hits (Count)
system.cpu.dcache.demandMisses::cpu.data   133   # number of demand (read+write) misses (Count)
system.cpu.dcache.demandMisses::total   133   # number of demand (read+write) misses (Count)
system.cpu.dcache.overallMisses::cpu.data   133   # number of overall misses (Count)
system.cpu.dcache.overallMisses::total   133   # number of overall misses (Count)
system.cpu.dcache.demandMissLatency::cpu.data   14428000   # number of demand (read+write) miss ticks (Tick)
system.cpu.dcache.demandMissLatency::total   14428000   # number of demand (read+write) miss ticks (Tick)
system.cpu.dcache.overallMissLatency::cpu.data   14428000   # number of overall miss ticks (Tick)
system.cpu.dcache.overallMissLatency::total   14428000   # number of overall miss ticks (Tick)

system.cpu.dcache.demandAccesses::cpu.data 2062 # number of demand (read+write) accesses (Count)
system.cpu.dcache.demandAccesses::total 2062 # number of demand (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::cpu.data 2062 # number of overall (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::total 2062 # number of overall (read+write) accesses (Count)
system.cpu.dcache.demandMissRate::cpu.data 0.064500 # miss rate for demand accesses (Ratio)
system.cpu.dcache.demandMissRate::total 0.064500 # miss rate for demand accesses (Ratio)
system.cpu.dcache.overallMissRate::cpu.data 0.064500 # miss rate for overall accesses (Ratio)
system.cpu.dcache.overallMissRate::total 0.064500 # miss rate for overall accesses (Ratio)
system.cpu.dcache.demandAvgMissLatency::cpu.data 108481.203008 # average overall miss latency in ticks ((Tick/Count))
system.cpu.dcache.demandAvgMissLatency::total 108481.203008 # average overall miss latency in ticks ((Tick/Count))
system.cpu.dcache.overallAvgMissLatency::cpu.data 108481.203008 # average overall miss latency ((Tick/Count))
system.cpu.dcache.overallAvgMissLatency::total 108481.203008 # average overall miss latency ((Tick/Count))
system.cpu.dcache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.cpu.dcache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.cpu.dcache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dcache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dcache.demandMshrMisses::cpu.data 133 # number of demand (read+write) MSHR misses (Count)
system.cpu.dcache.demandMshrMisses::total 133 # number of demand (read+write) MSHR misses (Count)
system.cpu.dcache.overallMshrMisses::cpu.data 133 # number of overall MSHR misses (Count)
system.cpu.dcache.overallMshrMisses::total 133 # number of overall MSHR misses (Count)
system.cpu.dcache.demandMshrMissLatency::cpu.data 14162000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.dcache.demandMshrMissLatency::total 14162000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.dcache.overallMshrMissLatency::cpu.data 14162000 # number of overall MSHR miss ticks (Tick)
system.cpu.dcache.overallMshrMissLatency::total 14162000 # number of overall MSHR miss ticks (Tick)
system.cpu.dcache.demandMshrMissRate::cpu.data 0.064500 # mshr miss ratio for demand accesses (Ratio)

system.cpu.dcache.demandMshrMissRate::total 0.064500 # mshr miss ratio for demand accesses (Ratio)
system.cpu.dcache.overallMshrMissRate::cpu.data 0.064500 # mshr miss ratio for overall accesses (Ratio)
system.cpu.dcache.overallMshrMissRate::total 0.064500 # mshr miss ratio for overall accesses (Ratio)
system.cpu.dcache.demandAvgMshrMissLatency::cpu.data 106481.203008 # average overall mshr miss latency ((Tick/Count))
system.cpu.dcache.demandAvgMshrMissLatency::total 106481.203008 # average overall mshr miss latency ((Tick/Count))
system.cpu.dcache.overallAvgMshrMissLatency::cpu.data 106481.203008 # average overall mshr miss latency ((Tick/Count))
system.cpu.dcache.overallAvgMshrMissLatency::total 106481.203008 # average overall mshr miss latency ((Tick/Count))
system.cpu.dcache.replacements 0 # number of replacements (Count)
system.cpu.dcache.ReadReq.hits::cpu.data 1057 # number of ReadReq hits (Count)
system.cpu.dcache.ReadReq.hits::total 1057 # number of ReadReq hits (Count)
system.cpu.dcache.ReadReq.misses::cpu.data 56 # number of ReadReq misses (Count)
system.cpu.dcache.ReadReq.misses::total 56 # number of ReadReq misses (Count)
system.cpu.dcache.ReadReq.missLatency::cpu.data 6325000 # number of ReadReq miss ticks (Tick)
system.cpu.dcache.ReadReq.missLatency::total 6325000 # number of ReadReq miss ticks (Tick)
system.cpu.dcache.ReadReq.accesses::cpu.data 1113 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.dcache.ReadReq.accesses::total 1113 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.dcache.ReadReq.missRate::cpu.data 0.050314 # miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.ReadReq.missRate::total 0.050314 # miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.ReadReq.avgMissLatency::cpu.data 112946.428571 # average ReadReq miss latency ((Tick/Count))
system.cpu.dcache.ReadReq.avgMissLatency::total 112946.428571 # average ReadReq miss latency ((Tick/Count))
system.cpu.dcache.ReadReq.mshrMisses::cpu.data 56 # number of ReadReq MSHR misses (Count)
system.cpu.dcache.ReadReq.mshrMisses::total 56 # number of ReadReq MSHR misses (Count)
system.cpu.dcache.ReadReq.mshrMissLatency::cpu.data 6213000 # number of ReadReq MSHR miss ticks (Tick)
system.cpu.dcache.ReadReq.mshrMissLatency::total 6213000 # number of ReadReq MSHR miss ticks (Tick)
system.cpu.dcache.ReadReq.mshrMissRate::cpu.data 0.050314 # mshr miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.ReadReq.mshrMissRate::total 0.050314 # mshr miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.ReadReq.avgMshrMissLatency::cpu.data 110946.428571 # average ReadReq mshr miss latency ((Tick/Count))

system.cpu.dcache.ReadReq.avgMshrMissLatency::total 110946.428571 # average ReadReq mshr miss latency ((Tick/Count))
system.cpu.dcache.WriteReq.hits::cpu.data 872 # number of WriteReq hits (Count)
system.cpu.dcache.WriteReq.hits::total 872 # number of WriteReq hits (Count)
system.cpu.dcache.WriteReq.misses::cpu.data 77 # number of WriteReq misses (Count)
system.cpu.dcache.WriteReq.misses::total 77 # number of WriteReq misses (Count)
system.cpu.dcache.WriteReq.missLatency::cpu.data 8103000 # number of WriteReq miss ticks (Tick)
system.cpu.dcache.WriteReq.missLatency::total 8103000 # number of WriteReq miss ticks (Tick)
system.cpu.dcache.WriteReq.accesses::cpu.data 949 # number of WriteReq accesses(hits+misses) (Count)
system.cpu.dcache.WriteReq.accesses::total 949 # number of WriteReq accesses(hits+misses) (Count)
system.cpu.dcache.WriteReq.missRate::cpu.data 0.081138 # miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.WriteReq.missRate::total 0.081138 # miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.WriteReq.avgMissLatency::cpu.data 105233.766234 # average WriteReq miss latency ((Tick/Count))
system.cpu.dcache.WriteReq.avgMissLatency::total 105233.766234 # average WriteReq miss latency ((Tick/Count))
system.cpu.dcache.WriteReq.mshrMisses::cpu.data 77 # number of WriteReq MSHR misses (Count)
system.cpu.dcache.WriteReq.mshrMisses::total 77 # number of WriteReq MSHR misses (Count)
system.cpu.dcache.WriteReq.mshrMissLatency::cpu.data 7949000 # number of WriteReq MSHR miss ticks (Tick)
system.cpu.dcache.WriteReq.mshrMissLatency::total 7949000 # number of WriteReq MSHR miss ticks (Tick)
system.cpu.dcache.WriteReq.mshrMissRate::cpu.data 0.081138 # mshr miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.WriteReq.mshrMissRate::total 0.081138 # mshr miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.WriteReq.avgMshrMissLatency::cpu.data 103233.766234 # average WriteReq mshr miss latency ((Tick/Count))
system.cpu.dcache.WriteReq.avgMshrMissLatency::total 103233.766234 # average WriteReq mshr miss latency ((Tick/Count))
system.cpu.dcache.power_state.pwrStateResidencyTicks::UNDEFINED 57467000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.dcache.tags.tagsInUse 80.923627 # Average ticks per tags in use ((Tick/Count))
system.cpu.dcache.tags.totalRefs 2062 # Total number of references to valid blocks. (Count)
system.cpu.dcache.tags.sampledRefs 133 # Sample count of references to valid blocks. (Count)
system.cpu.dcache.tags.avgRefs 15.503759 # Average number of references to valid blocks. ((Count/Count))
system.cpu.dcache.tags.warmupTick 220000 # The tick when the warmup percentage was hit. (Tick)

system.cpu.dcache.tags.occupancies::cpu.data 80.923627 # Average occupied blocks per tick, per requestor ((Count/Tick))
system.cpu.dcache.tags.avgOccs::cpu.data 0.079027 # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.dcache.tags.avgOccs::total 0.079027 # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.dcache.tags.occupanciesTaskId::1024 133 # Occupied blocks per task id (Count)
system.cpu.dcache.tags.ageTaskId_1024::0 11 # Occupied blocks per task id, per block age (Count)
system.cpu.dcache.tags.ageTaskId_1024::1 122 # Occupied blocks per task id, per block age (Count)
system.cpu.dcache.tags.ratioOccsTaskId::1024 0.129883 # Ratio of occupied blocks and all blocks, per task id (Ratio)
system.cpu.dcache.tags.tagAccesses 4257 # Number of tag accesses (Count)
system.cpu.dcache.tags.dataAccesses 4257 # Number of data accesses (Count)
system.cpu.dcache.tags.power_state.pwrStateResidencyTicks::UNDEFINED 57467000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.icache.demandHits::cpu.inst 7680 # number of demand (read+write) hits (Count)
system.cpu.icache.demandHits::total 7680 # number of demand (read+write) hits (Count)
system.cpu.icache.overallHits::cpu.inst 7680 # number of overall hits (Count)
system.cpu.icache.overallHits::total 7680 # number of overall hits (Count)
system.cpu.icache.demandMisses::cpu.inst 234 # number of demand (read+write) misses (Count)
system.cpu.icache.demandMisses::total 234 # number of demand (read+write) misses (Count)
system.cpu.icache.overallMisses::cpu.inst 234 # number of overall misses (Count)
system.cpu.icache.overallMisses::total 234 # number of overall misses (Count)
system.cpu.icache.demandMissLatency::cpu.inst 23821000 # number of demand (read+write) miss ticks (Tick)
system.cpu.icache.demandMissLatency::total 23821000 # number of demand (read+write) miss ticks (Tick)
system.cpu.icache.overallMissLatency::cpu.inst 23821000 # number of overall miss ticks (Tick)
system.cpu.icache.overallMissLatency::total 23821000 # number of overall miss ticks (Tick)
system.cpu.icache.demandAccesses::cpu.inst 7914 # number of demand (read+write) accesses (Count)
system.cpu.icache.demandAccesses::total 7914 # number of demand (read+write) accesses (Count)
system.cpu.icache.overallAccesses::cpu.inst 7914 # number of overall (read+write) accesses (Count)
system.cpu.icache.overallAccesses::total 7914 # number of overall (read+write) accesses (Count)
system.cpu.icache.demandMissRate::cpu.inst 0.029568 # miss rate for demand accesses (Ratio)

system.cpu.icache.demandMissRate::total 0.029568 # miss rate for demand accesses (Ratio)
system.cpu.icache.overallMissRate::cpu.inst 0.029568 # miss rate for overall accesses (Ratio)
system.cpu.icache.overallMissRate::total 0.029568 # miss rate for overall accesses (Ratio)
system.cpu.icache.demandAvgMissLatency::cpu.inst 101799.145299 # average overall miss latency in ticks ((Tick/Count))
system.cpu.icache.demandAvgMissLatency::total 101799.145299 # average overall miss latency in ticks ((Tick/Count))
system.cpu.icache.overallAvgMissLatency::cpu.inst 101799.145299 # average overall miss latency ((Tick/Count))
system.cpu.icache.overallAvgMissLatency::total 101799.145299 # average overall miss latency ((Tick/Count))
system.cpu.icache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.cpu.icache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.cpu.icache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.cpu.icache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.cpu.icache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.icache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.icache.demandMshrMisses::cpu.inst 234 # number of demand (read+write) MSHR misses (Count)
system.cpu.icache.demandMshrMisses::total 234 # number of demand (read+write) MSHR misses (Count)
system.cpu.icache.overallMshrMisses::cpu.inst 234 # number of overall MSHR misses (Count)
system.cpu.icache.overallMshrMisses::total 234 # number of overall MSHR misses (Count)
system.cpu.icache.demandMshrMissLatency::cpu.inst 23353000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.icache.demandMshrMissLatency::total 23353000 # number of demand (read+write) MSHR miss ticks (Tick)
system.cpu.icache.overallMshrMissLatency::cpu.inst 23353000 # number of overall MSHR miss ticks (Tick)
system.cpu.icache.overallMshrMissLatency::total 23353000 # number of overall MSHR miss ticks (Tick)
system.cpu.icache.demandMshrMissRate::cpu.inst 0.029568 # mshr miss ratio for demand accesses (Ratio)
system.cpu.icache.demandMshrMissRate::total 0.029568 # mshr miss ratio for demand accesses (Ratio)
system.cpu.icache.overallMshrMissRate::cpu.inst 0.029568 # mshr miss ratio for overall accesses (Ratio)
system.cpu.icache.overallMshrMissRate::total 0.029568 # mshr miss ratio for overall accesses (Ratio)
system.cpu.icache.demandAvgMshrMissLatency::cpu.inst 99799.145299 # average overall mshr miss latency ((Tick/Count))
system.cpu.icache.demandAvgMshrMissLatency::total 99799.145299 # average overall mshr miss latency ((Tick/Count))

system.cpu.icache.overallAvgMshrMissLatency::cpu.inst 99799.145299 # average overall mshr miss latency ((Tick/Count))
system.cpu.icache.overallAvgMshrMissLatency::total 99799.145299 # average overall mshr miss latency ((Tick/Count))
system.cpu.icache.replacements 57 # number of replacements (Count)
system.cpu.icache.ReadReq.hits::cpu.inst 7680 # number of ReadReq hits (Count)
system.cpu.icache.ReadReq.hits::total 7680 # number of ReadReq hits (Count)
system.cpu.icache.ReadReq.misses::cpu.inst 234 # number of ReadReq misses (Count)
system.cpu.icache.ReadReq.misses::total 234 # number of ReadReq misses (Count)
system.cpu.icache.ReadReq.missLatency::cpu.inst 23821000 # number of ReadReq miss ticks (Tick)
system.cpu.icache.ReadReq.missLatency::total 23821000 # number of ReadReq miss ticks (Tick)
system.cpu.icache.ReadReq.accesses::cpu.inst 7914 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.icache.ReadReq.accesses::total 7914 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.icache.ReadReq.missRate::cpu.inst 0.029568 # miss rate for ReadReq accesses (Ratio)
system.cpu.icache.ReadReq.missRate::total 0.029568 # miss rate for ReadReq accesses (Ratio)
system.cpu.icache.ReadReq.avgMissLatency::cpu.inst 101799.145299 # average ReadReq miss latency ((Tick/Count))
system.cpu.icache.ReadReq.avgMissLatency::total 101799.145299 # average ReadReq miss latency ((Tick/Count))
system.cpu.icache.ReadReq.mshrMisses::cpu.inst 234 # number of ReadReq MSHR misses (Count)
system.cpu.icache.ReadReq.mshrMisses::total 234 # number of ReadReq MSHR misses (Count)
system.cpu.icache.ReadReq.mshrMissLatency::cpu.inst 23353000 # number of ReadReq MSHR miss ticks (Tick)
system.cpu.icache.ReadReq.mshrMissLatency::total 23353000 # number of ReadReq MSHR miss ticks (Tick)
system.cpu.icache.ReadReq.mshrMissRate::cpu.inst 0.029568 # mshr miss rate for ReadReq accesses (Ratio)
system.cpu.icache.ReadReq.mshrMissRate::total 0.029568 # mshr miss rate for ReadReq accesses (Ratio)
system.cpu.icache.ReadReq.avgMshrMissLatency::cpu.inst 99799.145299 # average ReadReq mshr miss latency ((Tick/Count))
system.cpu.icache.ReadReq.avgMshrMissLatency::total 99799.145299 # average ReadReq mshr miss latency ((Tick/Count))
system.cpu.icache.power_state.pwrStateResidencyTicks::UNDEFINED 57467000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.icache.tags.tagsInUse 91.477423 # Average ticks per tags in use ((Tick/Count))
system.cpu.icache.tags.totalRefs 7914 # Total number of references to valid blocks. (Count)
system.cpu.icache.tags.sampledRefs 234 # Sample count of references to valid blocks. (Count)

system.cpu.icache.tags.avgRefs 33.820513 # Average number of references to valid blocks. ((Count/Count))
system.cpu.icache.tags.warmupTick 107000 # The tick when the warmup percentage was hit. (Tick)
system.cpu.icache.tags.occupancies::cpu.inst 91.477423 # Average occupied blocks per tick, per requestor ((Count/Tick))
system.cpu.icache.tags.avgOccs::cpu.inst 0.357334 # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.icache.tags.avgOccs::total 0.357334 # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.icache.tags.occupanciesTaskId::1024 177 # Occupied blocks per task id (Count)
system.cpu.icache.tags.ageTaskId_1024::0 45 # Occupied blocks per task id, per block age (Count)
system.cpu.icache.tags.ageTaskId_1024::1 132 # Occupied blocks per task id, per block age (Count)
system.cpu.icache.tags.ratioOccsTaskId::1024 0.691406 # Ratio of occupied blocks and all blocks, per task id (Ratio)
system.cpu.icache.tags.tagAccesses 16062 # Number of tag accesses (Count)
system.cpu.icache.tags.dataAccesses 16062 # Number of data accesses (Count)
system.cpu.icache.tags.power_state.pwrStateResidencyTicks::UNDEFINED 57467000 # Cumulative time (in ticks) in various power states (Tick)
system.l2bus.pktCount_system.cpu.icache.mem_side_port::system.l2cache.cpu_side_port 525 # Packet count per connected requestor and responder (Count)
system.l2bus.pktCount_system.cpu.dcache.mem_side_port::system.l2cache.cpu_side_port 266 # Packet count per connected requestor and responder (Count)
system.l2bus.pktSize_system.cpu.icache.mem_side_port::system.l2cache.cpu_side_port 14976 # Cumulative packet size per connected requestor and responder (Byte)
system.l2bus.pktSize_system.cpu.dcache.mem_side_port::system.l2cache.cpu_side_port 8512 # Cumulative packet size per connected requestor and responder (Byte)
system.l2cache.demandHits::cpu.inst 6 # number of demand (read+write) hits (Count)
system.l2cache.demandHits::total 6 # number of demand (read+write) hits (Count)
system.l2cache.overallHits::cpu.inst 6 # number of overall hits (Count)
system.l2cache.overallHits::total 6 # number of overall hits (Count)
system.l2cache.demandMisses::cpu.inst 228 # number of demand (read+write) misses (Count)
system.l2cache.demandMisses::cpu.data 133 # number of demand (read+write) misses (Count)
system.l2cache.demandMisses::total 361 # number of demand (read+write) misses (Count)
system.l2cache.overallMisses::cpu.inst 228 # number of overall misses (Count)
system.l2cache.overallMisses::cpu.data 133 # number of overall misses (Count)
system.l2cache.overallMisses::total 361 # number of overall misses (Count)
system.l2cache.demandMissLatency::cpu.inst 22523000 # number of demand (read+write) miss ticks (Tick)
system.l2cache.demandMissLatency::cpu.data 13763000 # number of demand (read+write) miss ticks (Tick)

system.l2cache.demandMissLatency::total 36286000 # number of demand (read+write) miss ticks (Tick)
system.l2cache.overallMissLatency::cpu.inst 22523000 # number of overall miss ticks (Tick)
system.l2cache.overallMissLatency::cpu.data 13763000 # number of overall miss ticks (Tick)
system.l2cache.overallMissLatency::total 36286000 # number of overall miss ticks (Tick)
system.l2cache.demandAccesses::cpu.inst 234 # number of demand (read+write) accesses (Count)
system.l2cache.demandAccesses::cpu.data 133 # number of demand (read+write) accesses (Count)
system.l2cache.demandAccesses::total 367 # number of demand (read+write) accesses (Count)
system.l2cache.overallAccesses::cpu.inst 234 # number of overall (read+write) accesses (Count)
system.l2cache.overallAccesses::cpu.data 133 # number of overall (read+write) accesses (Count)
system.l2cache.overallAccesses::total 367 # number of overall (read+write) accesses (Count)
system.l2cache.demandMissRate::cpu.inst 0.974359 # miss rate for demand accesses (Ratio)
system.l2cache.demandMissRate::cpu.data 1 # miss rate for demand accesses (Ratio)
system.l2cache.demandMissRate::total 0.983651 # miss rate for demand accesses (Ratio)
system.l2cache.overallMissRate::cpu.inst 0.974359 # miss rate for overall accesses (Ratio)
system.l2cache.overallMissRate::cpu.data 1 # miss rate for overall accesses (Ratio)
system.l2cache.overallMissRate::total 0.983651 # miss rate for overall accesses (Ratio)
system.l2cache.demandAvgMissLatency::cpu.inst 98785.087719 # average overall miss latency in ticks ((Tick/Count))
system.l2cache.demandAvgMissLatency::cpu.data 103481.203008 # average overall miss latency in ticks ((Tick/Count))
system.l2cache.demandAvgMissLatency::total 100515.235457 # average overall miss latency in ticks ((Tick/Count))
system.l2cache.overallAvgMissLatency::cpu.inst 98785.087719 # average overall miss latency ((Tick/Count))
system.l2cache.overallAvgMissLatency::cpu.data 103481.203008 # average overall miss latency ((Tick/Count))
system.l2cache.overallAvgMissLatency::total 100515.235457 # average overall miss latency ((Tick/Count))
system.l2cache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.l2cache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.l2cache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.l2cache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.l2cache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))

system.l2cache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.l2cache.demandMshrMisses::cpu.inst 228 # number of demand (read+write) MSHR misses (Count)
system.l2cache.demandMshrMisses::cpu.data 133 # number of demand (read+write) MSHR misses (Count)
system.l2cache.demandMshrMisses::total 361 # number of demand (read+write) MSHR misses (Count)
system.l2cache.overallMshrMisses::cpu.inst 228 # number of overall MSHR misses (Count)
system.l2cache.overallMshrMisses::cpu.data 133 # number of overall MSHR misses (Count)
system.l2cache.overallMshrMisses::total 361 # number of overall MSHR misses (Count)
system.l2cache.demandMshrMissLatency::cpu.inst 17963000 # number of demand (read+write) MSHR miss ticks (Tick)
system.l2cache.demandMshrMissLatency::cpu.data 11103000 # number of demand (read+write) MSHR miss ticks (Tick)
system.l2cache.demandMshrMissLatency::total 29066000 # number of demand (read+write) MSHR miss ticks (Tick)
system.l2cache.overallMshrMissLatency::cpu.inst 17963000 # number of overall MSHR miss ticks (Tick)
system.l2cache.overallMshrMissLatency::cpu.data 11103000 # number of overall MSHR miss ticks (Tick)
system.l2cache.overallMshrMissLatency::total 29066000 # number of overall MSHR miss ticks (Tick)
system.l2cache.demandMshrMissRate::cpu.inst 0.974359 # mshr miss ratio for demand accesses (Ratio)
system.l2cache.demandMshrMissRate::cpu.data 1 # mshr miss ratio for demand accesses (Ratio)
system.l2cache.demandMshrMissRate::total 0.983651 # mshr miss ratio for demand accesses (Ratio)
system.l2cache.overallMshrMissRate::cpu.inst 0.974359 # mshr miss ratio for overall accesses (Ratio)
system.l2cache.overallMshrMissRate::cpu.data 1 # mshr miss ratio for overall accesses (Ratio)
system.l2cache.overallMshrMissRate::total 0.983651 # mshr miss ratio for overall accesses (Ratio)
system.l2cache.demandAvgMshrMissLatency::cpu.inst 78785.087719 # average overall mshr miss latency ((Tick/Count))
system.l2cache.demandAvgMshrMissLatency::cpu.data 83481.203008 # average overall mshr miss latency ((Tick/Count))
system.l2cache.demandAvgMshrMissLatency::total 80515.235457 # average overall mshr miss latency ((Tick/Count))
system.l2cache.overallAvgMshrMissLatency::cpu.inst 78785.087719 # average overall mshr miss latency ((Tick/Count))
system.l2cache.overallAvgMshrMissLatency::cpu.data 83481.203008 # average overall mshr miss latency ((Tick/Count))
system.l2cache.overallAvgMshrMissLatency::total 80515.235457 # average overall mshr miss latency ((Tick/Count))
system.l2cache.replacements 0 # number of replacements (Count)
system.l2cache.ReadExReq.misses::cpu.data 77 # number of ReadExReq misses (Count)

system.l2cache.ReadExReq.misses::total 77 # number of ReadExReq misses (Count)
system.l2cache.ReadExReq.missLatency::cpu.data 7718000 # number of ReadExReq miss ticks (Tick)
system.l2cache.ReadExReq.missLatency::total 7718000 # number of ReadExReq miss ticks (Tick)
system.l2cache.ReadExReq.accesses::cpu.data 77 # number of ReadExReq accesses(hits+misses) (Count)
system.l2cache.ReadExReq.accesses::total 77 # number of ReadExReq accesses(hits+misses) (Count)
system.l2cache.ReadExReq.missRate::cpu.data 1 # miss rate for ReadExReq accesses (Ratio)
system.l2cache.ReadExReq.missRate::total 1 # miss rate for ReadExReq accesses (Ratio)
system.l2cache.ReadExReq.avgMissLatency::cpu.data 100233.766234 # average ReadExReq miss latency ((Tick/Count))
system.l2cache.ReadExReq.avgMissLatency::total 100233.766234 # average ReadExReq miss latency ((Tick/Count))
system.l2cache.ReadExReq.mshrMisses::cpu.data 77 # number of ReadExReq MSHR misses (Count)
system.l2cache.ReadExReq.mshrMisses::total 77 # number of ReadExReq MSHR misses (Count)
system.l2cache.ReadExReq.mshrMissLatency::cpu.data 6178000 # number of ReadExReq MSHR miss ticks (Tick)
system.l2cache.ReadExReq.mshrMissLatency::total 6178000 # number of ReadExReq MSHR miss ticks (Tick)
system.l2cache.ReadExReq.mshrMissRate::cpu.data 1 # mshr miss rate for ReadExReq accesses (Ratio)
system.l2cache.ReadExReq.mshrMissRate::total 1 # mshr miss rate for ReadExReq accesses (Ratio)
system.l2cache.ReadExReq.avgMshrMissLatency::cpu.data 80233.766234 # average ReadExReq mshr miss latency ((Tick/Count))
system.l2cache.ReadExReq.avgMshrMissLatency::total 80233.766234 # average ReadExReq mshr miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.hits::cpu.inst 6 # number of ReadSharedReq hits (Count)
system.l2cache.ReadSharedReq.hits::total 6 # number of ReadSharedReq hits (Count)
system.l2cache.ReadSharedReq.misses::cpu.inst 228 # number of ReadSharedReq misses (Count)
system.l2cache.ReadSharedReq.misses::cpu.data 56 # number of ReadSharedReq misses (Count)
system.l2cache.ReadSharedReq.misses::total 284 # number of ReadSharedReq misses (Count)
system.l2cache.ReadSharedReq.missLatency::cpu.inst 22523000 # number of ReadSharedReq miss ticks (Tick)
system.l2cache.ReadSharedReq.missLatency::cpu.data 6045000 # number of ReadSharedReq miss ticks (Tick)
system.l2cache.ReadSharedReq.missLatency::total 28568000 # number of ReadSharedReq miss ticks (Tick)
system.l2cache.ReadSharedReq.accesses::cpu.inst 234 # number of ReadSharedReq accesses(hits+misses) (Count)
system.l2cache.ReadSharedReq.accesses::cpu.data 56 # number of ReadSharedReq accesses(hits+misses) (Count)

system.l2cache.ReadSharedReq.accesses::total 290 # number of ReadSharedReq accesses(hits+misses) (Count)
system.l2cache.ReadSharedReq.missRate::cpu.inst 0.974359 # miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.missRate::cpu.data 1 # miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.missRate::total 0.979310 # miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.avgMissLatency::cpu.inst 98785.087719 # average ReadSharedReq miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.avgMissLatency::cpu.data 107946.428571 # average ReadSharedReq miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.avgMissLatency::total 100591.549296 # average ReadSharedReq miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.mshrMisses::cpu.inst 228 # number of ReadSharedReq MSHR misses (Count)
system.l2cache.ReadSharedReq.mshrMisses::cpu.data 56 # number of ReadSharedReq MSHR misses (Count)
system.l2cache.ReadSharedReq.mshrMisses::total 284 # number of ReadSharedReq MSHR misses (Count)
system.l2cache.ReadSharedReq.mshrMissLatency::cpu.inst 17963000 # number of ReadSharedReq MSHR miss ticks (Tick)
system.l2cache.ReadSharedReq.mshrMissLatency::cpu.data 4925000 # number of ReadSharedReq MSHR miss ticks (Tick)
system.l2cache.ReadSharedReq.mshrMissLatency::total 22888000 # number of ReadSharedReq MSHR miss ticks (Tick)
system.l2cache.ReadSharedReq.mshrMissRate::cpu.inst 0.974359 # mshr miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.mshrMissRate::cpu.data 1 # mshr miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.mshrMissRate::total 0.979310 # mshr miss rate for ReadSharedReq accesses (Ratio)
system.l2cache.ReadSharedReq.avgMshrMissLatency::cpu.inst 78785.087719 # average ReadSharedReq mshr miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.avgMshrMissLatency::cpu.data 87946.428571 # average ReadSharedReq mshr miss latency ((Tick/Count))
system.l2cache.ReadSharedReq.avgMshrMissLatency::total 80591.549296 # average ReadSharedReq mshr miss latency ((Tick/Count))
system.l2cache.power_state.pwrStateResidencyTicks::UNDEFINED 57467000 # Cumulative time (in ticks) in various power states (Tick)
system.l2cache.tags.tagsInUse 187.697743 # Average ticks per tags in use ((Tick/Count))
system.l2cache.tags.totalRefs 424 # Total number of references to valid blocks. (Count)
system.l2cache.tags.sampledRefs 361 # Sample count of references to valid blocks. (Count)
system.l2cache.tags.avgRefs 1.174515 # Average number of references to valid blocks. ((Count/Count))
system.l2cache.tags.warmupTick 86000 # The tick when the warmup percentage was hit. (Tick)
system.l2cache.tags.occupancies::cpu.inst 106.725514 # Average occupied blocks per tick, per requestor ((Count/Tick))
system.l2cache.tags.occupancies::cpu.data 80.972228 # Average occupied blocks per tick, per requestor ((Count/Tick))

```
system.l2cache.tags.avgOccs::cpu.inst        0.026056                # Average percentage of
cache occupancy ((Ratio/Tick))
system.l2cache.tags.avgOccs::cpu.data        0.019769                # Average percentage of
cache occupancy ((Ratio/Tick))
system.l2cache.tags.avgOccs::total           0.045825                # Average percentage of
cache occupancy ((Ratio/Tick))
system.l2cache.tags.occupanciesTaskId::1024          361             # Occupied blocks per
task id (Count)
system.l2cache.tags.ageTaskId_1024::0            56                  # Occupied blocks per task
id, per block age (Count)
system.l2cache.tags.ageTaskId_1024::1            305                 # Occupied blocks per task
id, per block age (Count)
system.l2cache.tags.ratioOccsTaskId::1024     0.088135               # Ratio of occupied
blocks and all blocks, per task id (Ratio)
system.l2cache.tags.tagAccesses                  3753                # Number of tag accesses
(Count)
system.l2cache.tags.dataAccesses                 3753                # Number of data accesses
(Count)
system.l2cache.tags.power_state.pwrStateResidencyTicks::UNDEFINED     57467000
# Cumulative time (in ticks) in various power states (Tick)
system.membus.pktCount_system.l2cache.mem_side_port::system.mem_ctrl.port          722
# Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.l2cache.mem_side_port::total          722             #
Packet count per connected requestor and responder (Count)
system.membus.pktSize_system.l2cache.mem_side_port::system.mem_ctrl.port        23104
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.l2cache.mem_side_port::total        23104           #
Cumulative packet size per connected requestor and responder (Byte)
root@5cb9d529d43a:/gem5# ls
CODE-OF-CONDUCT.md  MAINTAINERS.yaml  TESTING.md  ext      optional-requirements.txt
site_scons
CONTRIBUTING.md     README            build       hello    plot_stats.py            src
COPYING             RELEASE-NOTES.md  build_opts  hello.c  pyproject.toml           system
KCONFIG.md          SConsopts         build_tools include  requirements.txt         tests
LICENSE             SConstruct        configs     m5out    run_hello.py             util
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# ls
boot  common  deprecated  dist  dram  example  learning_gem5  network  nvm  ruby  splash2
topologies
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# ls
README  part1  part2  part3
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__  caches.py  simple-arm.py  simple-riscv.py  simple.py  two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano  /gem5/configs/
learning_gem5/part1/caches.pyroot@5cb9d529d43a:/gem5/configs/learning_gem5/part1#
nano two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
caches.py
gem5 Simulator System.  https://www.gem5.org
```

```
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 16 2025 21:03:12
gem5 executing on 5cb9d529d43a, pid 48
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/caches.py

root@5cb9d529d43a:/gem5# ls
CODE-OF-CONDUCT.md  MAINTAINERS.yaml  TESTING.md  ext      optional-requirements.txt  site_scons
CONTRIBUTING.md     README            build       hello    plot_stats.py              src
COPYING             RELEASE-NOTES.md  build_opts  hello.c  pyproject.toml             system
KCONFIG.md          SConsopts         build_tools include  requirements.txt           tests
LICENSE             SConstruct        configs     m5out    run_hello.py               util
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# ls
boot  common  deprecated  dist  dram  example  learning_gem5  network  nvm  ruby  splash2  topologies
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# ls
README  part1  part2  part3
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__  caches.py  simple-arm.py  simple-riscv.py  simple.py  two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/caches.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 16 2025 23:35:52
gem5 executing on 5cb9d529d43a, pid 53
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/caches.py

root@5cb9d529d43a:/gem5# ls m5out/
config.ini  config.json  fs  stats.txt
root@5cb9d529d43a:/gem5# cat m5out/stats.txt | grep cache
root@5cb9d529d43a:/gem5# nano caches.py
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5/part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano caches.py


Use "fg" to return to nano.

[1]+  Stopped                 nano caches.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano caches.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano caches.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano caches.py
```

root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# **cat caches.py**

```
# -*- coding: utf-8 -*-
# Copyright (c) 2015 Jason Power
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#
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# SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT
# LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE,
# DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY
# THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
# (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
# OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

""" Caches with options for a simple gem5 configuration script

This file contains L1 I/D and L2 caches to be used in the simple
gem5 configuration script. It uses the SimpleOpts wrapper to set up command
line options from each individual class.
"""

import m5
from m5.objects import Cache

# Add the common scripts to our path
m5.util.addToPath("../../")

from common import SimpleOpts

# Some specific options for caches
# For all options see src/mem/cache/BaseCache.py


class L1Cache(Cache):
    """Simple L1 Cache with default values"""

    assoc = 2
    tag_latency = 2
    data_latency = 2
```

```
    response_latency = 2
    mshrs = 4
    tgts_per_mshr = 20

    def __init__(self, options=None):
        super(L1Cache, self).__init__()
        pass

    def connectBus(self, bus):
        """Connect this cache to a memory-side bus"""
        self.mem_side = bus.cpu_side_ports

    def connectCPU(self, cpu):
        """Connect this cache's port to a CPU-side port
        This must be defined in a subclass"""
        raise NotImplementedError


class L1ICache(L1Cache):
    """Simple L1 instruction cache with default values"""

    # Set the default size
    size = "16kB"

    SimpleOpts.add_option(
        "--l1i_size", help=f"L1 instruction cache size. Default: {size}"
    )

    def __init__(self, opts=None):
        super(L1ICache, self).__init__(opts)
        if not opts or not opts.l1i_size:
            return
        self.size = opts.l1i_size

    def connectCPU(self, cpu):
        """Connect this cache's port to a CPU icache port"""
        self.cpu_side = cpu.icache_port


class L1DCache(L1Cache):
    """Simple L1 data cache with default values"""

    # Set the default size
    size = "64kB"

    SimpleOpts.add_option(
        "--l1d_size", help=f"L1 data cache size. Default: {size}"
    )

    def __init__(self, opts=None):
        super(L1DCache, self).__init__(opts)
        if not opts or not opts.l1d_size:
            return
        self.size = opts.l1d_size
```

```
    def connectCPU(self, cpu):
        """Connect this cache's port to a CPU dcache port"""
        self.cpu_side = cpu.dcache_port


class L2Cache(Cache):
    """Simple L2 Cache with default values"""

    # Default parameters
    size = "256kB"
    assoc = 8
    tag_latency = 20
    data_latency = 20
    response_latency = 20
    mshrs = 20
    tgts_per_mshr = 12

    SimpleOpts.add_option("--l2_size", help=f"L2 cache size. Default: {size}")

    def __init__(self, opts=None):
        super(L2Cache, self).__init__()
        if not opts or not opts.l2_size:
            return
        self.size = opts.l2_size

    def connectCPUSideBus(self, bus):
        self.cpu_side = bus.mem_side_ports

    def connectMemSideBus(self, bus):
        self.mem_side = bus.cpu_side_ports
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 00:46:25
gem5 executing on 5cb9d529d43a, pid 64
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

AttributeError: Class ClockDomain has no parameter clock

At:
  src/python/m5/SimObject.py(908): __setattr__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(11): __init__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(49): <module>
  src/python/m5/main.py(629): main
```

```
root@5cb9d529d43a:/gem5# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 00:50:16
gem5 executing on 5cb9d529d43a, pid 67
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

SyntaxError: unmatched ')' (simple_cache_sim.py, line 11)

At:
  src/python/m5/main.py(606): main
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5/part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__  caches.py  simple-arm.py  simple-riscv.py  simple.py  simple_cache_sim.py
two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 00:51:50
gem5 executing on 5cb9d529d43a, pid 70
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

NameError: name 'Clock' is not defined

At:
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(11): __init__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(49): <module>
  src/python/m5/main.py(629): main
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5/part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
```

```
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 00:55:08
gem5 executing on 5cb9d529d43a, pid 72
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

NameError: name 'Clock' is not defined

At:
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(11): __init__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(49): <module>
  src/python/m5/main.py(629): main
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5/part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 00:59:35
gem5 executing on 5cb9d529d43a, pid 74
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

ValueError: cannot convert '1GHZ' to latency
Error setting param SrcClockDomain.clock to 1GHZ


At:
  src/python/m5/util/convert.py(144): convert
  src/python/m5/util/convert.py(164): toNum
  src/python/m5/util/convert.py(213): anyToLatency
  src/python/m5/params.py(1779): __init__
  src/python/m5/params.py(222): convert
  src/python/m5/params.py(356): <listcomp>
  src/python/m5/params.py(355): convert
  src/python/m5/SimObject.py(880): __setattr__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(11): __init__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(49): <module>
  src/python/m5/main.py(629): main
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5/part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
```

```
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:04:33
gem5 executing on 5cb9d529d43a, pid 76
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

AttributeError: 'float' object has no attribute 'endswith'
Error setting param SrcClockDomain.clock to 1e-09


At:
  src/python/m5/params.py(1774): __init__
  src/python/m5/params.py(222): convert
  src/python/m5/params.py(361): convert
  src/python/m5/SimObject.py(880): __setattr__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(12): __init__
  /gem5/configs/learning_gem5/part1/simple_cache_sim.py(50): <module>
  src/python/m5/main.py(629): main
root@5cb9d529d43a:/gem5# cd /gem5/configs/learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# ls
README  part1  part2  part3
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__  caches.py  simple-arm.py  simple-riscv.py  simple.py  simple_cache_sim.py
two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ,,
bash: cd: ,,: No such file or directory
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
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gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:08:04
gem5 executing on 5cb9d529d43a, pid 80
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
```

```
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
src/cpu/base.cc:181: fatal: Number of ISAs (0) assigned to the CPU does not equal number of threads (1).
Memory Usage: 624712 KBytes
root@5cb9d529d43a:/gem5# cd gem5/configs/learning_gem5/part1/simple_cache_sim.py
bash: cd: gem5/configs/learning_gem5/part1/simple_cache_sim.py: No such file or directory
root@5cb9d529d43a:/gem5# cd gem5/configs/learning_gem5/part1
bash: cd: gem5/configs/learning_gem5/part1: No such file or directory
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# ls
boot common deprecated dist dram example learning_gem5 network nvm ruby splash2 topologies
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__ caches.py simple-arm.py simple-riscv.py simple.py simple_cache_sim.py two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
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gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:13:14
gem5 executing on 5cb9d529d43a, pid 84
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/simple_cache_sim.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
src/cpu/base.cc:181: fatal: Number of ISAs (0) assigned to the CPU does not equal number of threads (1).
Memory Usage: 624708 KBytes
root@5cb9d529d43a:/gem5# ls /gem5/build/X86/cpu
BaseCPU.py.cc       DummyChecker.py.pyo     base.o            probes
BaseCPU.py.o        FuncUnit.py.cc          checker           profile.o
BaseCPU.py.pyo      FuncUnit.py.o           exetrace.o        reg_class.o
CPUTracers.py.cc    FuncUnit.py.pyo         func_unit.o       simple
CPUTracers.py.o     InstPBTrace.py.cc       inst_pb_trace.o   simple_thread.o
CPUTracers.py.pyo   InstPBTrace.py.o        inteltrace.o      static_inst.o
CheckerCPU.py.cc    InstPBTrace.py.pyo      kvm               testers
CheckerCPU.py.o     StaticInstFlags.py.cc   minor             thread_context.o
```

CheckerCPU.py.pyo StaticInstFlags.py.o nativetrace.o thread_state.o
CpuCluster.py.cc StaticInstFlags.py.pyo nop_static_inst.o timing_expr.o
CpuCluster.py.o TimingExpr.py.cc null_static_inst.o trace
CpuCluster.py.pyo TimingExpr.py.o o3
DummyChecker.py.cc TimingExpr.py.pyo pc_event.o
DummyChecker.py.o activity.o pred
root@5cb9d529d43a:/gem5# grep -r "class " /gem5/src/cpu/
/gem5/src/cpu/CPUTracers.py:class ExeTracer(InstTracer):
/gem5/src/cpu/CPUTracers.py: cxx_class = "gem5::trace::ExeTracer"
/gem5/src/cpu/CPUTracers.py:class IntelTrace(InstTracer):
/gem5/src/cpu/CPUTracers.py: cxx_class = "gem5::trace::IntelTrace"
/gem5/src/cpu/CPUTracers.py:class NativeTrace(ExeTracer):
/gem5/src/cpu/CPUTracers.py: cxx_class = "gem5::trace::NativeTrace"
/gem5/src/cpu/FuncUnit.py:class OpClass(Enum):
/gem5/src/cpu/FuncUnit.py:class OpDesc(SimObject):
/gem5/src/cpu/FuncUnit.py: cxx_class = "gem5::OpDesc"
/gem5/src/cpu/FuncUnit.py:class FUDesc(SimObject):
/gem5/src/cpu/FuncUnit.py: cxx_class = "gem5::FUDesc"
/gem5/src/cpu/pred/btb.hh:class DefaultBTB
/gem5/src/cpu/pred/bpred_unit.hh: * Basically a wrapper class to hold both the branch
predictor
/gem5/src/cpu/pred/bpred_unit.hh:class BPredUnit : public SimObject
/gem5/src/cpu/pred/multiperspective_perceptron_tage_64KB.hh:class
MPP_StatisticalCorrector_64KB : public MPP_StatisticalCorrector
/gem5/src/cpu/pred/multiperspective_perceptron_tage_64KB.hh:class
MultiperspectivePerceptronTAGE64KB :
/gem5/src/cpu/pred/loop_predictor.hh:class LoopPredictor : public SimObject
/gem5/src/cpu/pred/loop_predictor.hh: * derived class prediction information in the base
class.
/gem5/src/cpu/pred/multiperspective_perceptron_tage.hh:class MPP_TAGE : public TAGEBase
/gem5/src/cpu/pred/multiperspective_perceptron_tage.hh:class MPP_LoopPredictor : public
LoopPredictor
/gem5/src/cpu/pred/multiperspective_perceptron_tage.hh:class MPP_StatisticalCorrector :
public StatisticalCorrector
/gem5/src/cpu/pred/multiperspective_perceptron_tage.hh:class
MultiperspectivePerceptronTAGE : public MultiperspectivePerceptron
/gem5/src/cpu/pred/BranchPredictor.py:class IndirectPredictor(SimObject):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::IndirectPredictor"
/gem5/src/cpu/pred/BranchPredictor.py:class SimpleIndirectPredictor(IndirectPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::SimpleIndirectPredictor"
/gem5/src/cpu/pred/BranchPredictor.py:class BranchPredictor(SimObject):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::BPredUnit"
/gem5/src/cpu/pred/BranchPredictor.py:class LocalBP(BranchPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::LocalBP"
/gem5/src/cpu/pred/BranchPredictor.py:class TournamentBP(BranchPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TournamentBP"
/gem5/src/cpu/pred/BranchPredictor.py:class BiModeBP(BranchPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::BiModeBP"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGEBase(SimObject):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::TAGEBase"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE(BranchPredictor):

/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::TAGE"
/gem5/src/cpu/pred/BranchPredictor.py:class LTAGE_TAGE(TAGEBase):
/gem5/src/cpu/pred/BranchPredictor.py:class LoopPredictor(SimObject):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::LoopPredictor"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_TAGE(TAGEBase):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_TAGE"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_TAGE_64KB(TAGE_SC_L_TAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_TAGE_64KB"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_TAGE_8KB(TAGE_SC_L_TAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_TAGE_8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class LTAGE(TAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::LTAGE"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_LoopPredictor(LoopPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_LoopPredictor"
/gem5/src/cpu/pred/BranchPredictor.py:class StatisticalCorrector(SimObject):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::StatisticalCorrector"
/gem5/src/cpu/pred/BranchPredictor.py:# Given this, the TAGE_SC_L class is left abstract
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L(LTAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L"
/gem5/src/cpu/pred/BranchPredictor.py:class
TAGE_SC_L_64KB_LoopPredictor(TAGE_SC_L_LoopPredictor):
/gem5/src/cpu/pred/BranchPredictor.py:class
TAGE_SC_L_8KB_LoopPredictor(TAGE_SC_L_LoopPredictor):
/gem5/src/cpu/pred/BranchPredictor.py:class
TAGE_SC_L_64KB_StatisticalCorrector(StatisticalCorrector):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_64KB_StatisticalCorrector"
/gem5/src/cpu/pred/BranchPredictor.py:class
TAGE_SC_L_8KB_StatisticalCorrector(StatisticalCorrector):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_8KB_StatisticalCorrector"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_64KB(TAGE_SC_L):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_64KB"
/gem5/src/cpu/pred/BranchPredictor.py:class TAGE_SC_L_8KB(TAGE_SC_L):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::TAGE_SC_L_8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class MultiperspectivePerceptron(BranchPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptron"
/gem5/src/cpu/pred/BranchPredictor.py:class
MultiperspectivePerceptron8KB(MultiperspectivePerceptron):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptron8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class
MultiperspectivePerceptron64KB(MultiperspectivePerceptron):

/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptron64KB"
/gem5/src/cpu/pred/BranchPredictor.py:class MPP_TAGE(TAGEBase):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class = "gem5::branch_prediction::MPP_TAGE"
/gem5/src/cpu/pred/BranchPredictor.py:class MPP_LoopPredictor(LoopPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_LoopPredictor"
/gem5/src/cpu/pred/BranchPredictor.py:class MPP_StatisticalCorrector(StatisticalCorrector):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_StatisticalCorrector"
/gem5/src/cpu/pred/BranchPredictor.py:class
MultiperspectivePerceptronTAGE(MultiperspectivePerceptron):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptronTAGE"
/gem5/src/cpu/pred/BranchPredictor.py:class
MPP_StatisticalCorrector_64KB(MPP_StatisticalCorrector):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_StatisticalCorrector_64KB"
/gem5/src/cpu/pred/BranchPredictor.py:class
MultiperspectivePerceptronTAGE64KB(MultiperspectivePerceptronTAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptronTAGE64KB"
/gem5/src/cpu/pred/BranchPredictor.py:class MPP_TAGE_8KB(MPP_TAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_TAGE_8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class MPP_LoopPredictor_8KB(MPP_LoopPredictor):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_LoopPredictor_8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class
MPP_StatisticalCorrector_8KB(MPP_StatisticalCorrector):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MPP_StatisticalCorrector_8KB"
/gem5/src/cpu/pred/BranchPredictor.py:class
MultiperspectivePerceptronTAGE8KB(MultiperspectivePerceptronTAGE):
/gem5/src/cpu/pred/BranchPredictor.py: cxx_class =
"gem5::branch_prediction::MultiperspectivePerceptronTAGE8KB"
/gem5/src/cpu/pred/2bit_local.hh:class LocalBP : public BPredUnit
/gem5/src/cpu/pred/tage_sc_l.cc: * TAGE-SC-L branch predictor base class (devised by Andre
Seznec)
/gem5/src/cpu/pred/tage_sc_l_64KB.hh:class TAGE_SC_L_TAGE_64KB : public
TAGE_SC_L_TAGE
/gem5/src/cpu/pred/tage_sc_l_64KB.hh:class TAGE_SC_L_64KB_StatisticalCorrector : public
StatisticalCorrector
/gem5/src/cpu/pred/tage_sc_l_64KB.hh:class TAGE_SC_L_64KB : public TAGE_SC_L
/gem5/src/cpu/pred/multiperspective_perceptron_tage_8KB.hh:class MPP_TAGE_8KB : public
MPP_TAGE
/gem5/src/cpu/pred/multiperspective_perceptron_tage_8KB.hh:class
MPP_LoopPredictor_8KB : public MPP_LoopPredictor
/gem5/src/cpu/pred/multiperspective_perceptron_tage_8KB.hh:class
MPP_StatisticalCorrector_8KB : public MPP_StatisticalCorrector
/gem5/src/cpu/pred/multiperspective_perceptron_tage_8KB.hh:class
MultiperspectivePerceptronTAGE8KB :
/gem5/src/cpu/pred/tage_base.cc: // Nothing for this base class implementation

/gem5/src/cpu/pred/tage_sc_l_8KB.hh:class TAGE_SC_L_TAGE_8KB : public TAGE_SC_L_TAGE
/gem5/src/cpu/pred/tage_sc_l_8KB.hh:class TAGE_SC_L_8KB_StatisticalCorrector : public StatisticalCorrector
/gem5/src/cpu/pred/tage_sc_l_8KB.hh:class TAGE_SC_L_8KB : public TAGE_SC_L
/gem5/src/cpu/pred/ras.hh:class ReturnAddrStack
/gem5/src/cpu/pred/tage_base.hh:class TAGEBase : public SimObject
/gem5/src/cpu/pred/tage_base.hh: * storing derived class prediction information in the
/gem5/src/cpu/pred/tage_base.hh: * storing derived class prediction information in the
/gem5/src/cpu/pred/tage_base.hh: * For this base TAGE class it does nothing
/gem5/src/cpu/pred/bi_mode.hh:class BiModeBP : public BPredUnit
/gem5/src/cpu/pred/multiperspective_perceptron_64KB.hh:class MultiperspectivePerceptron64KB : public MultiperspectivePerceptron
/gem5/src/cpu/pred/multiperspective_perceptron.hh:class MultiperspectivePerceptron : public BPredUnit
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class MPPBranchInfo
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class LocalHistories
/gem5/src/cpu/pred/multiperspective_perceptron.hh: * Base class to implement the predictor tables.
/gem5/src/cpu/pred/multiperspective_perceptron.hh: /** Reference to the branch predictor class */
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class GHIST : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class ACYCLIC : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class MODHIST : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class BIAS : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class RECENCY : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class IMLI : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class PATH : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class LOCAL : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class MODPATH : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class GHISTPATH : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class GHISTMODPATH : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class BLURRYPATH : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class RECENCYPOS : public HistorySpec
/gem5/src/cpu/pred/multiperspective_perceptron.hh: class SGHISTPATH : public HistorySpec
/gem5/src/cpu/pred/ltage.hh:class LTAGE : public TAGE
/gem5/src/cpu/pred/ltage.hh: // Base class methods.
/gem5/src/cpu/pred/ltage.hh: * derived class prediction information in the base class.
/gem5/src/cpu/pred/tage.hh:class TAGE: public BPredUnit
/gem5/src/cpu/pred/tage.hh: // Base class methods.
/gem5/src/cpu/pred/simple_indirect.hh:class SimpleIndirectPredictor : public IndirectPredictor
/gem5/src/cpu/pred/multiperspective_perceptron_8KB.hh:class MultiperspectivePerceptron8KB : public MultiperspectivePerceptron
/gem5/src/cpu/pred/statistical_corrector.hh:class StatisticalCorrector : public SimObject
/gem5/src/cpu/pred/tournament.hh:class TournamentBP : public BPredUnit
/gem5/src/cpu/pred/indirect.hh:class IndirectPredictor : public SimObject
/gem5/src/cpu/pred/tage_sc_l.hh: * TAGE-SC-L branch predictor base class (devised by Andre Seznec)
/gem5/src/cpu/pred/tage_sc_l.hh:class TAGE_SC_L_TAGE : public TAGEBase
/gem5/src/cpu/pred/tage_sc_l.hh:class TAGE_SC_L_LoopPredictor : public LoopPredictor

/gem5/src/cpu/pred/tage_sc_l.hh:class TAGE_SC_L: public LTAGE
/gem5/src/cpu/minor/execute.cc: for (int op_class = No_OpClass + 1; op_class <
Num_OpClasses; op_class++) {
/gem5/src/cpu/minor/pipe_data.hh: * Contains class definitions for data flowing between
pipeline stages in
/gem5/src/cpu/minor/pipe_data.hh:class BranchData /* : public ReportIF, public BubbleIF */
/gem5/src/cpu/minor/pipe_data.hh:class ForwardLineData /* : public ReportIF, public BubbleIF
*/
/gem5/src/cpu/minor/pipe_data.hh:class ForwardInstData /* : public ReportIF, public BubbleIF
*/
/gem5/src/cpu/minor/trace.hh:template <class ...Args>
/gem5/src/cpu/minor/trace.hh:template <class ...Args>
/gem5/src/cpu/minor/trace.hh:template <class ...Args>
/gem5/src/cpu/minor/func_unit.hh: * also allow for future additions to op class checking */
/gem5/src/cpu/minor/func_unit.hh:class MinorOpClass : public SimObject
/gem5/src/cpu/minor/func_unit.hh:class MinorOpClassSet : public SimObject
/gem5/src/cpu/minor/func_unit.hh: /** Does this set support the given op class */
/gem5/src/cpu/minor/func_unit.hh:class MinorFUTiming: public SimObject
/gem5/src/cpu/minor/func_unit.hh: /** Does the extra decode in this object support the given
op class */
/gem5/src/cpu/minor/func_unit.hh:class MinorFU : public SimObject
/gem5/src/cpu/minor/func_unit.hh:class MinorFUPool : public SimObject
/gem5/src/cpu/minor/func_unit.hh:/** Container class to box instructions in the FUs to make
those
/gem5/src/cpu/minor/func_unit.hh:class QueuedInst
/gem5/src/cpu/minor/func_unit.hh:class FUPipeline : public FUPipelineBase, public FuncUnit
/gem5/src/cpu/minor/activity.hh:class MinorActivityRecorder : public ActivityRecorder
/gem5/src/cpu/minor/decode.hh:class Decode : public Named
/gem5/src/cpu/minor/cpu.hh:class Pipeline;
/gem5/src/cpu/minor/cpu.hh:class MinorCPU : public BaseCPU
/gem5/src/cpu/minor/cpu.hh: /** Provide a non-protected base class for Minor's Ports as
derived
/gem5/src/cpu/minor/cpu.hh: class MinorCPUPort : public RequestPort
/gem5/src/cpu/minor/pipeline.hh: * class itself
/gem5/src/cpu/minor/pipeline.hh:class Pipeline : public Ticked
/gem5/src/cpu/minor/exec_context.hh:class Execute;
/gem5/src/cpu/minor/exec_context.hh:class ExecContext : public gem5::ExecContext
/gem5/src/cpu/minor/lsq.hh:class Execute;
/gem5/src/cpu/minor/lsq.hh:class LSQ : public Named
/gem5/src/cpu/minor/lsq.hh: class DcachePort : public MinorCPU::MinorCPUPort
/gem5/src/cpu/minor/lsq.hh: class LSQRequest :
/gem5/src/cpu/minor/lsq.hh: class SpecialDataRequest : public LSQRequest
/gem5/src/cpu/minor/lsq.hh: class FailedDataRequest : public SpecialDataRequest
/gem5/src/cpu/minor/lsq.hh: class BarrierDataRequest : public SpecialDataRequest
/gem5/src/cpu/minor/lsq.hh: class SingleDataRequest : public LSQRequest
/gem5/src/cpu/minor/lsq.hh: class SplitDataRequest : public LSQRequest
/gem5/src/cpu/minor/lsq.hh: class StoreBuffer : public Named
/gem5/src/cpu/minor/buffers.hh:/** Interface class for data with reporting/tracing facilities. This
/gem5/src/cpu/minor/buffers.hh:class ReportIF
/gem5/src/cpu/minor/buffers.hh:/** Interface class for data with 'bubble' values. This interface
doesn't
/gem5/src/cpu/minor/buffers.hh:class BubbleIF
/gem5/src/cpu/minor/buffers.hh:class ReportTraitsAdaptor
/gem5/src/cpu/minor/buffers.hh:class ReportTraitsPtrAdaptor

/gem5/src/cpu/minor/buffers.hh:class NoBubbleTraits
/gem5/src/cpu/minor/buffers.hh:class BubbleTraitsAdaptor
/gem5/src/cpu/minor/buffers.hh:class BubbleTraitsPtrAdaptor
/gem5/src/cpu/minor/buffers.hh:class MinorBuffer : public Named, public
TimeBuffer<ElemType>
/gem5/src/cpu/minor/buffers.hh:class Latch
/gem5/src/cpu/minor/buffers.hh: class Input
/gem5/src/cpu/minor/buffers.hh: class Output
/gem5/src/cpu/minor/buffers.hh:/** A pipeline simulating class that will stall (not advance when
advance()
/gem5/src/cpu/minor/buffers.hh:class SelfStallingPipeline : public MinorBuffer<ElemType,
ReportTraits>
/gem5/src/cpu/minor/buffers.hh:/** Base class for space reservation requestable objects */
/gem5/src/cpu/minor/buffers.hh:class Reservable
/gem5/src/cpu/minor/buffers.hh:class Queue : public Named, public Reservable
/gem5/src/cpu/minor/buffers.hh: * The purpose of this class is to allow the faster operation of
queues of
/gem5/src/cpu/minor/buffers.hh: * class name */
/gem5/src/cpu/minor/buffers.hh:class InputBuffer : public Reservable
/gem5/src/cpu/minor/fetch2.cc: // Collect some basic inst class stats
/gem5/src/cpu/minor/dyn_inst.hh:class MinorDynInst;
/gem5/src/cpu/minor/dyn_inst.hh:class InstId
/gem5/src/cpu/minor/dyn_inst.hh:class MinorDynInst;
/gem5/src/cpu/minor/dyn_inst.hh:class MinorDynInst : public RefCounted
/gem5/src/cpu/minor/execute.hh:class Execute : public Named
/gem5/src/cpu/minor/fetch1.hh:class Fetch1 : public Named
/gem5/src/cpu/minor/fetch1.hh: class IcachePort : public MinorCPU::MinorCPUPort
/gem5/src/cpu/minor/fetch1.hh: class FetchRequest :
/gem5/src/cpu/minor/fetch2.hh:class Fetch2 : public Named
/gem5/src/cpu/minor/scoreboard.hh:class Scoreboard : public Named
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorOpClass(SimObject):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorOpClass"
/gem5/src/cpu/minor/BaseMinorCPU.py: opClass = Param.OpClass("op class to match")
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorOpClassSet(SimObject):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorOpClassSet"
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorFUTiming(SimObject):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorFUTiming"
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorFU(SimObject):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorFU"
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorFUPool(SimObject):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorFUPool"
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultIntFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultIntMulFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultIntDivFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultFloatSimdFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultPredFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultMemFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultMiscFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultVecFU(MinorFU):
/gem5/src/cpu/minor/BaseMinorCPU.py:class MinorDefaultFUPool(MinorFUPool):
/gem5/src/cpu/minor/BaseMinorCPU.py:class ThreadPolicy(Enum):
/gem5/src/cpu/minor/BaseMinorCPU.py:class BaseMinorCPU(BaseCPU):
/gem5/src/cpu/minor/BaseMinorCPU.py: cxx_class = "gem5::MinorCPU"
/gem5/src/cpu/thread_state.hh:class Checkpoint;

/gem5/src/cpu/BaseCPU.py:class BaseCPU(ClockedObject):
/gem5/src/cpu/BaseCPU.py: cxx_class = "gem5::BaseCPU"
/gem5/src/cpu/DummyChecker.py:class DummyChecker(CheckerCPU):
/gem5/src/cpu/DummyChecker.py: cxx_class = "gem5::DummyChecker"
/gem5/src/cpu/reg_class.hh:// "Standard" register class names. Using these is encouraged but optional.
/gem5/src/cpu/reg_class.hh:class RegClass;
/gem5/src/cpu/reg_class.hh:class RegClassIterator;
/gem5/src/cpu/reg_class.hh:class BaseISA;
/gem5/src/cpu/reg_class.hh:/** Register ID: describe an architectural register with its class and index.
/gem5/src/cpu/reg_class.hh:class RegId
/gem5/src/cpu/reg_class.hh: friend class RegClassIterator;
/gem5/src/cpu/reg_class.hh: /** Return a const char* with the register class name. */
/gem5/src/cpu/reg_class.hh:class RegClassOps
/gem5/src/cpu/reg_class.hh:class RegClassIterator;
/gem5/src/cpu/reg_class.hh:class RegClass
/gem5/src/cpu/reg_class.hh: RegClass reg_class = *this;
/gem5/src/cpu/reg_class.hh: RegClass reg_class = *this;
/gem5/src/cpu/reg_class.hh: template <class RegType>
/gem5/src/cpu/reg_class.hh: RegClass reg_class = *this;
/gem5/src/cpu/reg_class.hh:class RegClassIterator
/gem5/src/cpu/reg_class.hh: friend class RegClass;
/gem5/src/cpu/reg_class.hh:class TypedRegClassOps : public RegClassOps
/gem5/src/cpu/reg_class.hh:class VecElemRegClassOps : public TypedRegClassOps<ValueType>
/gem5/src/cpu/reg_class.hh:class PhysRegId : private RegId
/gem5/src/cpu/dummy_checker.hh: * Specific non-templated derived class used for SimObject configuration.
/gem5/src/cpu/dummy_checker.hh:class DummyChecker : public CheckerCPU
/gem5/src/cpu/inst_pb_trace.hh:class Inst;
/gem5/src/cpu/inst_pb_trace.hh:class ThreadContext;
/gem5/src/cpu/inst_pb_trace.hh:class InstPBTraceRecord : public InstRecord
/gem5/src/cpu/inst_pb_trace.hh:class InstPBTrace : public InstTracer
/gem5/src/cpu/inst_pb_trace.hh: friend class InstPBTraceRecord;
/gem5/src/cpu/CpuCluster.py:class CpuCluster(SubSystem):
/gem5/src/cpu/CpuCluster.py: cxx_class = "gem5::CpuCluster"
/gem5/src/cpu/CpuCluster.py: # class variables
/gem5/src/cpu/nativetrace.hh:class ThreadContext;
/gem5/src/cpu/nativetrace.hh:class NativeTrace;
/gem5/src/cpu/nativetrace.hh:class NativeTraceRecord : public ExeTracerRecord
/gem5/src/cpu/nativetrace.hh:class NativeTrace : public ExeTracer
/gem5/src/cpu/nativetrace.hh: template<class T>
/gem5/src/cpu/thread_context.hh:class BaseCPU;
/gem5/src/cpu/thread_context.hh:class BaseMMU;
/gem5/src/cpu/thread_context.hh:class BaseTLB;
/gem5/src/cpu/thread_context.hh:class CheckerCPU;
/gem5/src/cpu/thread_context.hh:class Checkpoint;
/gem5/src/cpu/thread_context.hh:class InstDecoder;
/gem5/src/cpu/thread_context.hh:class PortProxy;
/gem5/src/cpu/thread_context.hh:class Process;
/gem5/src/cpu/thread_context.hh:class System;
/gem5/src/cpu/thread_context.hh:class Packet;
/gem5/src/cpu/thread_context.hh: * ThreadState is an abstract class that exactly defines the

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/gem5/src/cpu/thread_context.hh:class ThreadContext : public PCEventScope
/gem5/src/cpu/StaticInstFlags.py:# - The IsInteger and IsFloating flags are based on the class of registers
/gem5/src/cpu/StaticInstFlags.py:class StaticInstFlags(Enum):
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu_impl.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/thread_context.hh: * Derived ThreadContext class for use with the Checker.  The template
/gem5/src/cpu/checker/thread_context.hh: * parameter is the ThreadContext class used by the specific CPU being
/gem5/src/cpu/checker/thread_context.hh:template <class TC>
/gem5/src/cpu/checker/thread_context.hh:class CheckerThreadContext : public ThreadContext
/gem5/src/cpu/checker/thread_context.hh:    /** The main CPU's ThreadContext, or class that implements the
/gem5/src/cpu/checker/cpu.hh:class ThreadContext;
/gem5/src/cpu/checker/cpu.hh:class Request;
/gem5/src/cpu/checker/cpu.hh:class CheckerCPU : public BaseCPU, public ExecContext
/gem5/src/cpu/checker/cpu.hh: * Templated Checker class.  This Checker class is templated on the
/gem5/src/cpu/checker/cpu.hh:template <class DynInstPtr>
/gem5/src/cpu/checker/cpu.hh:class Checker : public CheckerCPU
/gem5/src/cpu/regfile.hh:class RegFile
/gem5/src/cpu/func_unit.hh://    (1) OpDesc - Describes the operation class & latencies
/gem5/src/cpu/func_unit.hh:class OpDesc : public SimObject
/gem5/src/cpu/func_unit.hh:class FUDesc : public SimObject
/gem5/src/cpu/func_unit.hh:class FuncUnit
/gem5/src/cpu/activity.hh: * ActivityRecorder helper class that informs the CPU if it can switch
/gem5/src/cpu/activity.hh:class ActivityRecorder
/gem5/src/cpu/InstPBTrace.py:class InstPBTrace(InstTracer):
/gem5/src/cpu/InstPBTrace.py:    cxx_class = "gem5::trace::InstPBTrace"
/gem5/src/cpu/trace/TraceCPU.py:class TraceCPU(BaseCPU):
/gem5/src/cpu/trace/TraceCPU.py:    cxx_class = "gem5::TraceCPU"
/gem5/src/cpu/trace/trace_cpu.hh: * encapsulated in the subclass ElasticDataGen.
/gem5/src/cpu/trace/trace_cpu.hh: * Therefore, the Trace CPU also models hardware resources. A sub-class to
/gem5/src/cpu/trace/trace_cpu.hh: * class as a down counter is used to implement multi Trace CPU simulation
/gem5/src/cpu/trace/trace_cpu.hh:class TraceCPU : public BaseCPU
/gem5/src/cpu/trace/trace_cpu.hh:     * IcachePort class that interfaces with L1 Instruction Cache.
/gem5/src/cpu/trace/trace_cpu.hh:    class IcachePort : public RequestPort
/gem5/src/cpu/trace/trace_cpu.hh:     * DcachePort class that interfaces with L1 Data Cache.
/gem5/src/cpu/trace/trace_cpu.hh:    class DcachePort : public RequestPort
/gem5/src/cpu/trace/trace_cpu.hh:    class FixedRetryGen
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/gem5/src/cpu/trace/trace_cpu.hh: class InputStream
/gem5/src/cpu/trace/trace_cpu.hh: class ElasticDataGen
/gem5/src/cpu/trace/trace_cpu.hh: class GraphNode
/gem5/src/cpu/trace/trace_cpu.hh: * The HardwareResource class models structures that hold the in-flight
/gem5/src/cpu/trace/trace_cpu.hh: class HardwareResource
/gem5/src/cpu/trace/trace_cpu.hh: class InputStream
/gem5/src/cpu/thread_context.cc: const auto *vec_class = regClasses.at(VecRegClass);
/gem5/src/cpu/thread_context.cc: const auto *vec_pred_class = regClasses.at(VecPredRegClass);
/gem5/src/cpu/thread_context.cc: const auto *mat_class = regClasses.at(MatRegClass);
/gem5/src/cpu/exetrace.hh:class ThreadContext;
/gem5/src/cpu/exetrace.hh:class ExeTracerRecord : public InstRecord
/gem5/src/cpu/exetrace.hh:class ExeTracer : public InstTracer
/gem5/src/cpu/inteltrace.hh:class IntelTraceRecord : public InstRecord
/gem5/src/cpu/inteltrace.hh:class IntelTrace : public InstTracer
/gem5/src/cpu/decode_cache.hh:template<class Value, Addr CacheChunkShift = 12>
/gem5/src/cpu/decode_cache.hh:class AddrMap
/gem5/src/cpu/base.hh:class BaseCPU;
/gem5/src/cpu/base.hh:class CheckerCPU;
/gem5/src/cpu/base.hh:class ThreadContext;
/gem5/src/cpu/base.hh:class CPUProgressEvent : public Event
/gem5/src/cpu/base.hh:class BaseCPU : public ClockedObject
/gem5/src/cpu/static_inst_fwd.hh:class StaticInst;
/gem5/src/cpu/exec_context.hh: * The ExecContext is an abstract base class the provides the
/gem5/src/cpu/exec_context.hh: * Register accessor methods in this class typically provide the index
/gem5/src/cpu/exec_context.hh: * @note The methods in this class typically take a raw pointer to the
/gem5/src/cpu/exec_context.hh:class ExecContext
/gem5/src/cpu/timebuf.hh:template <class T>
/gem5/src/cpu/timebuf.hh:class TimeBuffer
/gem5/src/cpu/timebuf.hh: friend class wire;
/gem5/src/cpu/timebuf.hh: class wire
/gem5/src/cpu/timebuf.hh: friend class TimeBuffer;
/gem5/src/cpu/timing_expr.hh:class TimingExprLet;
/gem5/src/cpu/timing_expr.hh:class TimingExprEvalContext
/gem5/src/cpu/timing_expr.hh:class TimingExpr : public SimObject
/gem5/src/cpu/timing_expr.hh:class TimingExprLiteral : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprSrcReg : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprLet : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprRef : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprUn : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprBin : public TimingExpr
/gem5/src/cpu/timing_expr.hh:class TimingExprIf : public TimingExpr
/gem5/src/cpu/simple/BaseSimpleCPU.py:class BaseSimpleCPU(BaseCPU):
/gem5/src/cpu/simple/BaseSimpleCPU.py: cxx_class = "gem5::BaseSimpleCPU"
/gem5/src/cpu/simple/BaseTimingSimpleCPU.py:class BaseTimingSimpleCPU(BaseSimpleCPU):
/gem5/src/cpu/simple/BaseTimingSimpleCPU.py: cxx_class = "gem5::TimingSimpleCPU"
/gem5/src/cpu/simple/atomic.hh:class AtomicSimpleCPU : public BaseSimpleCPU
/gem5/src/cpu/simple/atomic.hh: class AtomicCPUPort : public RequestPort
/gem5/src/cpu/simple/atomic.hh: class AtomicCPUDPort : public AtomicCPUPort

/gem5/src/cpu/simple/BaseAtomicSimpleCPU.py:class
BaseAtomicSimpleCPU(BaseSimpleCPU):
/gem5/src/cpu/simple/BaseAtomicSimpleCPU.py: cxx_class = "gem5::AtomicSimpleCPU"
/gem5/src/cpu/simple/base.hh:class Checkpoint;
/gem5/src/cpu/simple/base.hh:class Process;
/gem5/src/cpu/simple/base.hh:class Processor;
/gem5/src/cpu/simple/base.hh:class ThreadContext;
/gem5/src/cpu/simple/base.hh: class InstRecord;
/gem5/src/cpu/simple/base.hh: class BPredUnit;
/gem5/src/cpu/simple/base.hh:class SimpleExecContext;
/gem5/src/cpu/simple/base.hh:class BaseSimpleCPU : public BaseCPU
/gem5/src/cpu/simple/exec_context.hh:class BaseSimpleCPU;
/gem5/src/cpu/simple/exec_context.hh:class SimpleExecContext : public ExecContext
/gem5/src/cpu/simple/timing.hh:class TimingSimpleCPU : public BaseSimpleCPU
/gem5/src/cpu/simple/timing.hh: class SplitMainSenderState : public Packet::SenderState
/gem5/src/cpu/simple/timing.hh: class SplitFragmentSenderState : public
Packet::SenderState
/gem5/src/cpu/simple/timing.hh: class FetchTranslation : public BaseMMU::Translation
/gem5/src/cpu/simple/timing.hh: class TimingCPUPort : public RequestPort
/gem5/src/cpu/simple/timing.hh: class IcachePort : public TimingCPUPort
/gem5/src/cpu/simple/timing.hh: class DcachePort : public TimingCPUPort
/gem5/src/cpu/simple/probes/SimPoint.py:class SimPoint(ProbeListenerObject):
/gem5/src/cpu/simple/probes/SimPoint.py: cxx_class = "gem5::SimPoint"
/gem5/src/cpu/simple/probes/simpoint.hh:class SimPoint : public ProbeListenerObject
/gem5/src/cpu/simple/BaseNonCachingSimpleCPU.py:class
BaseNonCachingSimpleCPU(BaseAtomicSimpleCPU):
/gem5/src/cpu/simple/BaseNonCachingSimpleCPU.py: cxx_class =
"gem5::NonCachingSimpleCPU"
/gem5/src/cpu/simple/noncaching.hh:class NonCachingSimpleCPU : public AtomicSimpleCPU
/gem5/src/cpu/nop_static_inst.cc:class NopStaticInst : public StaticInst
/gem5/src/cpu/profile.hh:class ThreadContext;
/gem5/src/cpu/profile.hh:class FunctionProfile;
/gem5/src/cpu/profile.hh: class SymbolTable;
/gem5/src/cpu/profile.hh:class BaseStackTrace
/gem5/src/cpu/profile.hh:class ProfileNode
/gem5/src/cpu/profile.hh: friend class FunctionProfile;
/gem5/src/cpu/profile.hh:class FunctionProfile
/gem5/src/cpu/profile.hh: friend class ProfileNode;
/gem5/src/cpu/TimingExpr.py:class TimingExpr(SimObject):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExpr"
/gem5/src/cpu/TimingExpr.py:class TimingExprLiteral(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprLiteral"
/gem5/src/cpu/TimingExpr.py:class TimingExpr0(TimingExprLiteral):
/gem5/src/cpu/TimingExpr.py:class TimingExprSrcReg(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprSrcReg"
/gem5/src/cpu/TimingExpr.py:class TimingExprLet(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprLet"
/gem5/src/cpu/TimingExpr.py:class TimingExprRef(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprRef"
/gem5/src/cpu/TimingExpr.py:class TimingExprOp(Enum):
/gem5/src/cpu/TimingExpr.py:class TimingExprUn(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprUn"
/gem5/src/cpu/TimingExpr.py:class TimingExprBin(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprBin"

/gem5/src/cpu/TimingExpr.py:class TimingExprIf(TimingExpr):
/gem5/src/cpu/TimingExpr.py: cxx_class = "gem5::TimingExprIf"
/gem5/src/cpu/kvm/device.hh:class KvmDevice
/gem5/src/cpu/kvm/timer.hh:class BaseKvmTimer
/gem5/src/cpu/kvm/timer.hh:class PosixKvmTimer : public BaseKvmTimer
/gem5/src/cpu/kvm/timer.hh:class PerfKvmTimer : public BaseKvmTimer
/gem5/src/cpu/kvm/vm.hh:class BaseKvmCPU;
/gem5/src/cpu/kvm/vm.hh:class System;
/gem5/src/cpu/kvm/vm.hh:class Kvm
/gem5/src/cpu/kvm/vm.hh: friend class KvmVM;
/gem5/src/cpu/kvm/vm.hh:class KvmVM : public SimObject
/gem5/src/cpu/kvm/vm.hh: friend class BaseKvmCPU;
/gem5/src/cpu/kvm/vm.hh: class MemorySlot
/gem5/src/cpu/kvm/perfevent.hh:class PerfKvmCounterConfig
/gem5/src/cpu/kvm/perfevent.hh:class PerfKvmCounter
/gem5/src/cpu/kvm/KvmVM.py:class KvmVM(SimObject):
/gem5/src/cpu/kvm/KvmVM.py: cxx_class = "gem5::KvmVM"
/gem5/src/cpu/kvm/base.hh:class ThreadContext;
/gem5/src/cpu/kvm/base.hh: * Base class for KVM based CPU models
/gem5/src/cpu/kvm/base.hh:class BaseKvmCPU : public BaseCPU
/gem5/src/cpu/kvm/base.hh: class KVMCpuPort : public RequestPort
/gem5/src/cpu/kvm/BaseKvmCPU.py:class BaseKvmCPU(BaseCPU):
/gem5/src/cpu/kvm/BaseKvmCPU.py: cxx_class = "gem5::BaseKvmCPU"
/gem5/src/cpu/static_inst.hh:class Packet;
/gem5/src/cpu/static_inst.hh:class ExecContext;
/gem5/src/cpu/static_inst.hh:class ThreadContext;
/gem5/src/cpu/static_inst.hh:class SymbolTable;
/gem5/src/cpu/static_inst.hh:class InstRecord;
/gem5/src/cpu/static_inst.hh: * The main component of this class is the vector of flags and the
/gem5/src/cpu/static_inst.hh:class StaticInst : public RefCounted, public StaticInstFlags
/gem5/src/cpu/static_inst.hh: * with the base class accessors.
/gem5/src/cpu/testers/traffic_gen/dram_gen.hh:class DramGen : public RandomGen
/gem5/src/cpu/testers/traffic_gen/GUPSGen.py:class GUPSGen(ClockedObject):
/gem5/src/cpu/testers/traffic_gen/GUPSGen.py: cxx_class = "gem5::GUPSGen"
/gem5/src/cpu/testers/traffic_gen/base_gen.hh: * Declaration of the base generator class for all
generators.
/gem5/src/cpu/testers/traffic_gen/base_gen.hh:class BaseTrafficGen;
/gem5/src/cpu/testers/traffic_gen/base_gen.hh:class SimObject;
/gem5/src/cpu/testers/traffic_gen/base_gen.hh: * Base class for all generators, with the shared
functionality and
/gem5/src/cpu/testers/traffic_gen/base_gen.hh:class BaseGen
/gem5/src/cpu/testers/traffic_gen/base_gen.hh:class StochasticGen : public BaseGen
/gem5/src/cpu/testers/traffic_gen/exit_gen.hh:class ExitGen : public BaseGen
/gem5/src/cpu/testers/traffic_gen/traffic_gen.hh:class TrafficGen : public BaseTrafficGen
/gem5/src/cpu/testers/traffic_gen/idle_gen.hh:class IdleGen : public BaseGen
/gem5/src/cpu/testers/traffic_gen/trace_gen.hh:class TraceGen : public BaseGen
/gem5/src/cpu/testers/traffic_gen/trace_gen.hh: class InputStream
/gem5/src/cpu/testers/traffic_gen/pygen.hh:class GEM5_LOCAL PyTrafficGen : public
BaseTrafficGen
/gem5/src/cpu/testers/traffic_gen/nvm_gen.hh:class NvmGen : public RandomGen
/gem5/src/cpu/testers/traffic_gen/strided_gen.hh:class StridedGen : public StochasticGen
/gem5/src/cpu/testers/traffic_gen/base.hh:class BaseGen;
/gem5/src/cpu/testers/traffic_gen/base.hh:class StreamGen;
/gem5/src/cpu/testers/traffic_gen/base.hh:class System;

/gem5/src/cpu/testers/traffic_gen/base.hh:class BaseTrafficGen : public ClockedObject
/gem5/src/cpu/testers/traffic_gen/base.hh: friend class BaseGen;
/gem5/src/cpu/testers/traffic_gen/base.hh: class TrafficGenPort : public RequestPort
/gem5/src/cpu/testers/traffic_gen/dram_rot_gen.hh:class DramRotGen : public DramGen
/gem5/src/cpu/testers/traffic_gen/linear_gen.hh:class LinearGen : public StochasticGen
/gem5/src/cpu/testers/traffic_gen/PyTrafficGen.py:class PyTrafficGen(BaseTrafficGen):
/gem5/src/cpu/testers/traffic_gen/PyTrafficGen.py: cxx_class = "gem5::PyTrafficGen"
/gem5/src/cpu/testers/traffic_gen/BaseTrafficGen.py:class StreamGenType(ScopedEnum):
/gem5/src/cpu/testers/traffic_gen/BaseTrafficGen.py:class BaseTrafficGen(ClockedObject):
/gem5/src/cpu/testers/traffic_gen/BaseTrafficGen.py: cxx_class = "gem5::BaseTrafficGen"
/gem5/src/cpu/testers/traffic_gen/random_gen.hh:class RandomGen : public StochasticGen
/gem5/src/cpu/testers/traffic_gen/stream_gen.hh:class StreamGen
/gem5/src/cpu/testers/traffic_gen/stream_gen.hh:class FixedStreamGen : public StreamGen
/gem5/src/cpu/testers/traffic_gen/stream_gen.hh:class RandomStreamGen : public StreamGen
/gem5/src/cpu/testers/traffic_gen/gups_gen.hh: * Contatins the description of the class
GUPSGen. GUPSGen is a simobject
/gem5/src/cpu/testers/traffic_gen/gups_gen.hh:class GUPSGen : public ClockedObject
/gem5/src/cpu/testers/traffic_gen/gups_gen.hh: * @brief definition of the GenPort class
which is of the type RequestPort.
/gem5/src/cpu/testers/traffic_gen/gups_gen.hh: class GenPort : public RequestPort
/gem5/src/cpu/testers/traffic_gen/hybrid_gen.hh:class HybridGen : public BaseGen
/gem5/src/cpu/testers/traffic_gen/TrafficGen.py:class TrafficGen(BaseTrafficGen):
/gem5/src/cpu/testers/traffic_gen/TrafficGen.py: cxx_class = "gem5::TrafficGen"
/gem5/src/cpu/testers/memtest/MemTest.py:class MemTest(ClockedObject):
/gem5/src/cpu/testers/memtest/MemTest.py: cxx_class = "gem5::MemTest"
/gem5/src/cpu/testers/memtest/memtest.hh: * The MemTest class tests a cache coherent
memory system by
/gem5/src/cpu/testers/memtest/memtest.hh:class MemTest : public ClockedObject
/gem5/src/cpu/testers/memtest/memtest.hh: class CpuPort : public RequestPort
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.py:class
GarnetSyntheticTraffic(ClockedObject):
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.py: cxx_class =
"gem5::GarnetSyntheticTraffic"
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.hh:class Packet;
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.hh:class
GarnetSyntheticTraffic : public ClockedObject
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.hh: class CpuPort :
public RequestPort
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.hh: class
GarnetSyntheticTrafficSenderState : public Packet::SenderState
/gem5/src/cpu/testers/garnet_synthetic_traffic/GarnetSyntheticTraffic.hh: friend class
MemCompleteEvent;
/gem5/src/cpu/testers/gpu_ruby_test/CpuThread.py:class CpuThread(TesterThread):
/gem5/src/cpu/testers/gpu_ruby_test/CpuThread.py: cxx_class = "gem5::CpuThread"
/gem5/src/cpu/testers/gpu_ruby_test/cpu_thread.hh:class CpuThread : public TesterThread
/gem5/src/cpu/testers/gpu_ruby_test/DmaThread.py:class DmaThread(TesterThread):
/gem5/src/cpu/testers/gpu_ruby_test/DmaThread.py: cxx_class = "gem5::DmaThread"
/gem5/src/cpu/testers/gpu_ruby_test/TesterDma.py:class TesterDma(DmaDevice):
/gem5/src/cpu/testers/gpu_ruby_test/TesterDma.py: cxx_class = "gem5::TesterDma"
/gem5/src/cpu/testers/gpu_ruby_test/episode.cc:// ---------- Action class
----
/gem5/src/cpu/testers/gpu_ruby_test/tester_thread.hh:class TesterThread : public
ClockedObject

/gem5/src/cpu/testers/gpu_ruby_test/tester_thread.hh: class TesterThreadEvent : public
Event
/gem5/src/cpu/testers/gpu_ruby_test/tester_thread.hh: class DeadlockCheckEvent : public
Event
/gem5/src/cpu/testers/gpu_ruby_test/tester_dma.hh:class TesterDma : public DmaDevice
/gem5/src/cpu/testers/gpu_ruby_test/episode.hh:class ProtocolTester;
/gem5/src/cpu/testers/gpu_ruby_test/episode.hh:class TesterThread;
/gem5/src/cpu/testers/gpu_ruby_test/episode.hh:class Episode
/gem5/src/cpu/testers/gpu_ruby_test/episode.hh: class Action
/gem5/src/cpu/testers/gpu_ruby_test/episode.hh: enum class Type
/gem5/src/cpu/testers/gpu_ruby_test/dma_thread.hh:class DmaThread : public TesterThread
/gem5/src/cpu/testers/gpu_ruby_test/TesterThread.py:class TesterThread(ClockedObject):
/gem5/src/cpu/testers/gpu_ruby_test/TesterThread.py: cxx_class = "gem5::TesterThread"
/gem5/src/cpu/testers/gpu_ruby_test/README:ProtocolTester.hh/cc -- This is the main tester
class that orchestrates the
/gem5/src/cpu/testers/gpu_ruby_test/README:TesterThread.hh/cc   -- This is abstract class
for CPU threads and GPU
/gem5/src/cpu/testers/gpu_ruby_test/README:CpuThread.hh/cc   -- Thread class for CPU
threads. Not fully implemented yet
/gem5/src/cpu/testers/gpu_ruby_test/README:GpuWavefront.hh/cc   -- Thread class for GPU
wavefronts.
/gem5/src/cpu/testers/gpu_ruby_test/GpuWavefront.py:class GpuWavefront(TesterThread):
/gem5/src/cpu/testers/gpu_ruby_test/GpuWavefront.py: cxx_class = "gem5::GpuWavefront"
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh:class TesterThread;
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh:class CpuThread;
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh:class GpuWavefront;
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh:class ProtocolTester : public
ClockedObject
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh: class SeqPort : public RequestPort
/gem5/src/cpu/testers/gpu_ruby_test/protocol_tester.hh: class GMTokenPort : public
TokenRequestPort
/gem5/src/cpu/testers/gpu_ruby_test/ProtocolTester.py:class ProtocolTester(ClockedObject):
/gem5/src/cpu/testers/gpu_ruby_test/ProtocolTester.py: cxx_class = "gem5::ProtocolTester"
/gem5/src/cpu/testers/gpu_ruby_test/gpu_wavefront.hh:class GpuWavefront : public
TesterThread
/gem5/src/cpu/testers/gpu_ruby_test/gpu_wavefront.hh: // may be redefined by a child class
of GpuWavefront
/gem5/src/cpu/testers/gpu_ruby_test/address_manager.hh:class AddressManager
/gem5/src/cpu/testers/gpu_ruby_test/address_manager.hh: class LastWriter
/gem5/src/cpu/testers/gpu_ruby_test/address_manager.hh: class AtomicStruct
/gem5/src/cpu/testers/rubytest/Check.hh:class SubBlock;
/gem5/src/cpu/testers/rubytest/Check.hh:class Check
/gem5/src/cpu/testers/rubytest/RubyTester.hh:class RubyTester : public ClockedObject
/gem5/src/cpu/testers/rubytest/RubyTester.hh: class CpuPort : public RequestPort
/gem5/src/cpu/testers/rubytest/RubyTester.py:class RubyTester(ClockedObject):
/gem5/src/cpu/testers/rubytest/RubyTester.py: cxx_class = "gem5::RubyTester"
/gem5/src/cpu/testers/rubytest/CheckTable.hh:class Check;
/gem5/src/cpu/testers/rubytest/CheckTable.hh:class RubyTester;
/gem5/src/cpu/testers/rubytest/CheckTable.hh:class CheckTable
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.hh:class DirectedGenerator;
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.hh:class RubyDirectedTester : public
ClockedObject
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.hh: class CpuPort : public
RequestPort

/gem5/src/cpu/testers/directedtest/InvalidateGenerator.hh:class InvalidateGenerator : public
DirectedGenerator
/gem5/src/cpu/testers/directedtest/DirectedGenerator.hh:class DirectedGenerator : public
SimObject
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py:class DirectedGenerator(SimObject):
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py: cxx_class =
"gem5::DirectedGenerator"
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py:class
SeriesRequestGenerator(DirectedGenerator):
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py: cxx_class =
"gem5::SeriesRequestGenerator"
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py:class
InvalidateGenerator(DirectedGenerator):
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py: cxx_class =
"gem5::InvalidateGenerator"
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py:class
RubyDirectedTester(ClockedObject):
/gem5/src/cpu/testers/directedtest/RubyDirectedTester.py: cxx_class =
"gem5::RubyDirectedTester"
/gem5/src/cpu/testers/directedtest/SeriesRequestGenerator.hh:class
SeriesRequestGenerator : public DirectedGenerator
/gem5/src/cpu/translation.hh: * This class captures the state of an address translation. A
translation
/gem5/src/cpu/translation.hh: * a page boundary. In this case, this class is shared by two data
/gem5/src/cpu/translation.hh:class WholeTranslationState
/gem5/src/cpu/translation.hh: * This class represents part of a data address translation. All
state for
/gem5/src/cpu/translation.hh: * class does not need to know whether the translation is split or
not. The
/gem5/src/cpu/translation.hh: * translation state class indicate that the whole translation is
complete
/gem5/src/cpu/translation.hh:template <class ExecContextPtr>
/gem5/src/cpu/translation.hh:class DataTranslation : public BaseMMU::Translation
/gem5/src/cpu/probes/pc_count_tracker.hh:class PcCountTracker : public ProbeListenerObject
/gem5/src/cpu/probes/pc_count_pair.hh:class PcCountPair
/gem5/src/cpu/probes/PcCountTracker.py:class PcCountTrackerManager(SimObject):
/gem5/src/cpu/probes/PcCountTracker.py: """This class manages global PC-count pair
tracking.
/gem5/src/cpu/probes/PcCountTracker.py: cxx_class = "gem5::PcCountTrackerManager"
/gem5/src/cpu/probes/PcCountTracker.py:class PcCountTracker(ProbeListenerObject):
/gem5/src/cpu/probes/PcCountTracker.py: cxx_class = "gem5::PcCountTracker"
/gem5/src/cpu/probes/pc_count_tracker_manager.hh:class PcCountTrackerManager : public
SimObject {
/gem5/src/cpu/pc_event.hh:class ThreadContext;
/gem5/src/cpu/pc_event.hh:class PCEventQueue;
/gem5/src/cpu/pc_event.hh:class System;
/gem5/src/cpu/pc_event.hh:class PCEventScope;
/gem5/src/cpu/pc_event.hh:class PCEvent
/gem5/src/cpu/pc_event.hh:class PCEventScope
/gem5/src/cpu/pc_event.hh:class PCEventQueue : public PCEventScope
/gem5/src/cpu/pc_event.hh: class MapCompare
/gem5/src/cpu/pc_event.hh:class BreakPCEvent : public PCEvent
/gem5/src/cpu/pc_event.hh:class PanicPCEvent : public PCEvent
/gem5/src/cpu/simple_thread.hh:class BaseCPU;

/gem5/src/cpu/simple_thread.hh:class CheckerCPU;
/gem5/src/cpu/simple_thread.hh: * separate fetch and commit PC's), this SimpleThread class provides
/gem5/src/cpu/simple_thread.hh:class SimpleThread : public ThreadState, public ThreadContext
/gem5/src/cpu/simple_thread.hh: const auto &reg_class = reg_file.regClass;
/gem5/src/cpu/simple_thread.hh: const auto &reg_class = reg_file.regClass;
/gem5/src/cpu/simple_thread.hh: const auto &reg_class = reg_file.regClass;
/gem5/src/cpu/simple_thread.hh: const auto &reg_class = reg_file.regClass;
/gem5/src/cpu/inst_res.hh:class InstResult
/gem5/src/cpu/CheckerCPU.py:class CheckerCPU(BaseCPU):
/gem5/src/cpu/CheckerCPU.py: cxx_class = "gem5::CheckerCPU"
/gem5/src/cpu/cluster.hh:class CpuCluster : public SubSystem
/gem5/src/cpu/o3/inst_queue.cc: OpClass op_class = (*list_order_it).queueType;
/gem5/src/cpu/o3/inst_queue.cc: // This will avoid trying to schedule a certain op class if there are no
/gem5/src/cpu/o3/inst_queue.cc: OpClass op_class = (*order_it).queueType;
/gem5/src/cpu/o3/inst_queue.cc: if (op_class != No_OpClass) {
/gem5/src/cpu/o3/inst_queue.cc: OpClass op_class = ready_inst->opClass();
/gem5/src/cpu/o3/inst_queue.cc: OpClass op_class = inst->opClass();
/gem5/src/cpu/o3/fu_pool.hh:class FUDesc;
/gem5/src/cpu/o3/fu_pool.hh:class FuncUnit;
/gem5/src/cpu/o3/fu_pool.hh:class FUPool : public SimObject
/gem5/src/cpu/o3/fu_pool.hh: class FUIdxQueue
/gem5/src/cpu/o3/fu_pool.hh: /** Per op class queues of FUs that provide that capability. */
/gem5/src/cpu/o3/mem_dep_unit.hh:class CPU;
/gem5/src/cpu/o3/mem_dep_unit.hh:class InstructionQueue;
/gem5/src/cpu/o3/mem_dep_unit.hh: * utilize. Thus this class should be most likely be rewritten for other
/gem5/src/cpu/o3/mem_dep_unit.hh:class MemDepUnit
/gem5/src/cpu/o3/mem_dep_unit.hh: class MemDepEntry;
/gem5/src/cpu/o3/mem_dep_unit.hh: class MemDepEntry
/gem5/src/cpu/o3/commit.hh:class ThreadState;
/gem5/src/cpu/o3/commit.hh:class Commit
/gem5/src/cpu/o3/thread_state.hh:class Process;
/gem5/src/cpu/o3/thread_state.hh:class CPU;
/gem5/src/cpu/o3/thread_state.hh:class ThreadState : public gem5::ThreadState
/gem5/src/cpu/o3/probe/ElasticTrace.py:class ElasticTrace(ProbeListenerObject):
/gem5/src/cpu/o3/probe/ElasticTrace.py: cxx_class = "gem5::o3::ElasticTrace"
/gem5/src/cpu/o3/probe/ElasticTrace.py: # User is forced to provide these when an instance of this class is created.
/gem5/src/cpu/o3/probe/elastic_trace.hh:class CPU;
/gem5/src/cpu/o3/probe/elastic_trace.hh:class ElasticTrace : public ProbeListenerObject
/gem5/src/cpu/o3/probe/elastic_trace.hh: * Take the fields of the request class object that are relevant to create
/gem5/src/cpu/o3/probe/SimpleTrace.py:class SimpleTrace(ProbeListenerObject):
/gem5/src/cpu/o3/probe/SimpleTrace.py: cxx_class = "gem5::o3::SimpleTrace"
/gem5/src/cpu/o3/probe/simple_trace.hh:class SimpleTrace : public ProbeListenerObject
/gem5/src/cpu/o3/thread_context.hh: * Derived ThreadContext class for use with the O3CPU. It
/gem5/src/cpu/o3/thread_context.hh:class ThreadContext : public gem5::ThreadContext
/gem5/src/cpu/o3/regfile.hh:class UnifiedFreeList;
/gem5/src/cpu/o3/regfile.hh:class PhysRegFile
/gem5/src/cpu/o3/regfile.hh: panic("Unsupported register class type %d.", type);

/gem5/src/cpu/o3/regfile.hh: panic("Unrecognized register class type %d.", type);
/gem5/src/cpu/o3/regfile.hh: panic("Unrecognized register class type %d.", type);
/gem5/src/cpu/o3/regfile.hh: panic("Unsupported register class type %d.", type);
/gem5/src/cpu/o3/regfile.hh: panic("Unrecognized register class type %d.", type);
/gem5/src/cpu/o3/dyn_inst_ptr.hh:class DynInst;
/gem5/src/cpu/o3/rename_map.hh: * Register rename map for a single class of registers (e.g., integer
/gem5/src/cpu/o3/rename_map.hh: * or floating point). Because the register class is implicitly
/gem5/src/cpu/o3/rename_map.hh:class SimpleRenameMap
/gem5/src/cpu/o3/rename_map.hh: * register class (e.g., rename()) take register ids,
/gem5/src/cpu/o3/rename_map.hh: * while methods that do specify a register class (e.g., renameInt())
/gem5/src/cpu/o3/rename_map.hh:class UnifiedRenameMap
/gem5/src/cpu/o3/rename_map.hh: auto reg_class = arch_reg.classValue();
/gem5/src/cpu/o3/rename_map.hh: if (reg_class == InvalidRegClass) {
/gem5/src/cpu/o3/rename_map.hh: } else if (reg_class == MiscRegClass) {
/gem5/src/cpu/o3/BaseO3CPU.py:class SMTFetchPolicy(ScopedEnum):
/gem5/src/cpu/o3/BaseO3CPU.py:class SMTQueuePolicy(ScopedEnum):
/gem5/src/cpu/o3/BaseO3CPU.py:class CommitPolicy(ScopedEnum):
/gem5/src/cpu/o3/BaseO3CPU.py:class BaseO3CPU(BaseCPU):
/gem5/src/cpu/o3/BaseO3CPU.py: cxx_class = "gem5::o3::CPU"
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:class DependencyEntry
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:class DependencyGraph
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/dep_graph.hh:template <class DynInstPtr>
/gem5/src/cpu/o3/free_list.hh:class UnifiedRenameMap;
/gem5/src/cpu/o3/free_list.hh: * Free list for a single class of registers (e.g., integer
/gem5/src/cpu/o3/free_list.hh: * or floating point). Because the register class is implicitly
/gem5/src/cpu/o3/free_list.hh:class SimpleFreeList
/gem5/src/cpu/o3/free_list.hh: template<class InputIt>
/gem5/src/cpu/o3/free_list.hh: * FreeList class that simply holds the list of free integer and floating
/gem5/src/cpu/o3/free_list.hh: * class can be named simply "FreeList".
/gem5/src/cpu/o3/free_list.hh:class UnifiedFreeList
/gem5/src/cpu/o3/free_list.hh: * internal per-class free lists and associate those with its
/gem5/src/cpu/o3/free_list.hh: * per-class rename maps. See UnifiedRenameMap::init().
/gem5/src/cpu/o3/free_list.hh: friend class UnifiedRenameMap;
/gem5/src/cpu/o3/free_list.hh: template<class InputIt>
/gem5/src/cpu/o3/decode.hh:class CPU;
/gem5/src/cpu/o3/decode.hh: * Decode class handles both single threaded and SMT
/gem5/src/cpu/o3/decode.hh:class Decode
/gem5/src/cpu/o3/cpu.hh:class Checker;
/gem5/src/cpu/o3/cpu.hh:class ThreadContext;
/gem5/src/cpu/o3/cpu.hh:class Checkpoint;
/gem5/src/cpu/o3/cpu.hh:class Process;
/gem5/src/cpu/o3/cpu.hh:class ThreadContext;

/gem5/src/cpu/o3/cpu.hh:class CPU : public BaseCPU
/gem5/src/cpu/o3/cpu.hh: friend class ThreadContext;
/gem5/src/cpu/o3/rename.hh:class Rename
/gem5/src/cpu/o3/checker.hh: * Specific non-templated derived class used for SimObject
configuration.
/gem5/src/cpu/o3/checker.hh:class Checker : public gem5::Checker<DynInstPtr>
/gem5/src/cpu/o3/lsq_unit.hh:class IEW;
/gem5/src/cpu/o3/lsq_unit.hh:class LSQUnit
/gem5/src/cpu/o3/lsq_unit.hh: class LSQEntry
/gem5/src/cpu/o3/lsq_unit.hh: class SQEntry : public LSQEntry
/gem5/src/cpu/o3/lsq_unit.hh: enum class AddrRangeCoverage
/gem5/src/cpu/o3/lsq_unit.hh: class WritebackEvent : public Event
/gem5/src/cpu/o3/store_set.hh:class StoreSet
/gem5/src/cpu/o3/checker.cc:class Checker<o3::DynInstPtr>;
/gem5/src/cpu/o3/rob.hh:class CPU;
/gem5/src/cpu/o3/rob.hh:class ROB
/gem5/src/cpu/o3/lsq.hh:class CPU;
/gem5/src/cpu/o3/lsq.hh:class IEW;
/gem5/src/cpu/o3/lsq.hh:class LSQUnit;
/gem5/src/cpu/o3/lsq.hh:class LSQ
/gem5/src/cpu/o3/lsq.hh: class LSQRequest;
/gem5/src/cpu/o3/lsq.hh: * DcachePort class for the load/store queue.
/gem5/src/cpu/o3/lsq.hh: class DcachePort : public RequestPort
/gem5/src/cpu/o3/lsq.hh: * This class holds the information about a memory operation. It
lives
/gem5/src/cpu/o3/lsq.hh: class LSQRequest : public BaseMMU::Translation, public
Packet::SenderState
/gem5/src/cpu/o3/lsq.hh: enum class State
/gem5/src/cpu/o3/lsq.hh: class SingleDataRequest : public LSQRequest
/gem5/src/cpu/o3/lsq.hh: // This class extends SingleDataRequest for the purpose
/gem5/src/cpu/o3/lsq.hh: class UnsquashableDirectRequest : public SingleDataRequest
/gem5/src/cpu/o3/lsq.hh: class SplitDataRequest : public LSQRequest
/gem5/src/cpu/o3/inst_queue.hh:class MemInterface;
/gem5/src/cpu/o3/inst_queue.hh:class FUPool;
/gem5/src/cpu/o3/inst_queue.hh:class CPU;
/gem5/src/cpu/o3/inst_queue.hh:class IEW;
/gem5/src/cpu/o3/inst_queue.hh:class InstructionQueue
/gem5/src/cpu/o3/inst_queue.hh: class FUCompletion : public Event
/gem5/src/cpu/o3/inst_queue.hh: * class to allow for easy mapping to FUs.
/gem5/src/cpu/o3/inst_queue.hh: /** Add an op class to the age order list. */
/gem5/src/cpu/o3/FUPool.py:class FUPool(SimObject):
/gem5/src/cpu/o3/FUPool.py: cxx_class = "gem5::o3::FUPool"
/gem5/src/cpu/o3/FUPool.py:class DefaultFUPool(FUPool):
/gem5/src/cpu/o3/dyn_inst.hh:class Packet;
/gem5/src/cpu/o3/dyn_inst.hh:class DynInst : public ExecContext, public RefCounted
/gem5/src/cpu/o3/dyn_inst.hh: /** Returns the opclass of this instruction. */
/gem5/src/cpu/o3/BaseO3Checker.py:class BaseO3Checker(CheckerCPU):
/gem5/src/cpu/o3/BaseO3Checker.py: cxx_class = "gem5::o3::Checker"
/gem5/src/cpu/o3/fetch.hh:class CPU;
/gem5/src/cpu/o3/fetch.hh: * Fetch class handles both single threaded and SMT fetch. Its
/gem5/src/cpu/o3/fetch.hh:class Fetch
/gem5/src/cpu/o3/fetch.hh: * IcachePort class for instruction fetch.
/gem5/src/cpu/o3/fetch.hh: class IcachePort : public RequestPort
/gem5/src/cpu/o3/fetch.hh: class FetchTranslation : public BaseMMU::Translation

```
/gem5/src/cpu/o3/fetch.hh:    class FinishTranslationEvent : public Event
/gem5/src/cpu/o3/fetch.hh:     * fault that happened.  Puts the data into the class variable
/gem5/src/cpu/o3/scoreboard.hh: * ready. This class operates on the unified physical register
space,
/gem5/src/cpu/o3/scoreboard.hh:class Scoreboard
/gem5/src/cpu/o3/iew.hh:class FUPool;
/gem5/src/cpu/o3/iew.hh:class IEW
/gem5/src/cpu/o3/FuncUnitConfig.py:class IntALU(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class IntMultDiv(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class FP_ALU(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class FP_MultDiv(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class SIMD_Unit(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class PredALU(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class ReadPort(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class WritePort(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class RdWrPort(FUDesc):
/gem5/src/cpu/o3/FuncUnitConfig.py:class IprPort(FUDesc):
root@5cb9d529d43a:/gem5#
```

```
root@5cb9d529d43a:/gem5#
scons build/X86/gem5.opt -j8 CPU_MODELS=all
scons: Reading SConscript files ...
Mkdir("/gem5/build/X86/gem5.build")
Checking for linker -Wl,--as-needed support... (cached) yes
Checking for compiler -gz support... (cached) yes
Checking for linker -gz support... (cached) yes
Info: Using Python config: python3-config
Checking for C header file Python.h... (cached) yes
Checking Python version... (cached) 3.10.12
Checking for accept(0,0,0) in C++ library None... (cached) yes
Checking for zlibVersion() in C++ library z... (cached) yes
Checking for C library tcmalloc_minimal... (cached) yes
Building in /gem5/build/X86
Using saved variables file(s) /gem5/build/X86/gem5.build/variables
Checking for shm_open("/test", 0, 0) in C library None... (cached) yes
Checking for C header file linux/if_tun.h... (cached) yes
Checking for GOOGLE_PROTOBUF_VERIFY_VERSION in C++ library protobuf... (cached) yes
Checking for C header file fenv.h... (cached) yes
Checking for C header file png.h... (cached) yes
Checking for clock_nanosleep(0,0,NULL,NULL) in C library None... (cached) yes
Checking for C header file valgrind/valgrind.h... (cached) no
Checking for H5Fcreate("", 0, 0, 0) in C library hdf5... (cached) no
Warning: Couldn't find HDF5 C++ libraries. Disabling HDF5 support.
Checking for C header file linux/kvm.h... (cached) yes
Checking for timer_create(CLOCK_MONOTONIC, NULL, NULL) in C library None... (cached)
yes
Checking for member exclude_host in struct perf_event_attr...(cached) yes
Checking for backtrace_symbols_fd((void *)1, 0, 0) in C library None... (cached) yes
Checking whether __i386__ is declared... (cached) no
Checking whether __x86_64__ is declared... (cached) no
```

```
Warning: Unrecognized architecture for systemc.
Checking for compiler -Wno-self-assign-overloaded support... (cached) yes
Checking for linker -Wno-free-nonheap-object support... (cached) yes
scons: done reading SConscript files.
scons: Building targets ...
 [VER TAGS]  -> X86/sim/tags.cc
scons: `build/X86/gem5.opt' is up to date.
scons: done building targets.
*** Summary of Warnings ***
Warning: Couldn't find HDF5 C++ libraries. Disabling HDF5 support.
root@5cb9d529d43a:/gem5# ls /gem5/build/X86/cpu/
BaseCPU.py.cc       DummyChecker.py.pyo     base.o            probes
BaseCPU.py.o        FuncUnit.py.cc          checker           profile.o
BaseCPU.py.pyo      FuncUnit.py.o           exetrace.o        reg_class.o
CPUTracers.py.cc    FuncUnit.py.pyo         func_unit.o       simple
CPUTracers.py.o     InstPBTrace.py.cc       inst_pb_trace.o   simple_thread.o
CPUTracers.py.pyo   InstPBTrace.py.o        inteltrace.o      static_inst.o
CheckerCPU.py.cc    InstPBTrace.py.pyo      kvm               testers
CheckerCPU.py.o     StaticInstFlags.py.cc   minor             thread_context.o
CheckerCPU.py.pyo   StaticInstFlags.py.o    nativetrace.o     thread_state.o
CpuCluster.py.cc    StaticInstFlags.py.pyo  nop_static_inst.o  timing_expr.o
CpuCluster.py.o     TimingExpr.py.cc        null_static_inst.o  trace
CpuCluster.py.pyo   TimingExpr.py.o         o3
DummyChecker.py.cc  TimingExpr.py.pyo       pc_event.o
DummyChecker.py.o   activity.o              pred
root@5cb9d529d43a:/gem5# scons -c build/X86
scons: Reading SConscript files ...
Error: No non-leaf 'build' dir found on target path. /gem5/build/X86
root@5cb9d529d43a:/gem5# ls
CODE-OF-CONDUCT.md  MAINTAINERS.yaml  TESTING.md   ext      optional-requirements.txt
site_scons
CONTRIBUTING.md     README            build        hello    plot_stats.py            src
COPYING             RELEASE-NOTES.md  build_opts   hello.c  pyproject.toml           system
KCONFIG.md          SConsopts         build_tools  include  requirements.txt         tests
LICENSE             SConstruct        configs      m5out    run_hello.py             util
root@5cb9d529d43a:/gem5# cd build
root@5cb9d529d43a:/gem5/build# ls
ARM  X86
root@5cb9d529d43a:/gem5/build# cd X86
root@5cb9d529d43a:/gem5/build/X86# ls
arch  config  debug  enums  gem5.build  gem5py    kern          m5out  params  python  sst
base  cpu     dev    ext    gem5.opt    gem5py_m5  learning_gem5  mem    proto   sim
systemc
root@5cb9d529d43a:/gem5/build/X86# ls
arch  config  debug  enums  gem5.build  gem5py    kern          m5out  params  python  sst
base  cpu     dev    ext    gem5.opt    gem5py_m5  learning_gem5  mem    proto   sim
systemc
root@5cb9d529d43a:/gem5/build/X86# cd cpu
root@5cb9d529d43a:/gem5/build/X86/cpu#
root@5cb9d529d43a:/gem5/build/X86/cpu# ls
BaseCPU.py.cc       DummyChecker.py.pyo     base.o            probes
BaseCPU.py.o        FuncUnit.py.cc          checker           profile.o
BaseCPU.py.pyo      FuncUnit.py.o           exetrace.o        reg_class.o
CPUTracers.py.cc    FuncUnit.py.pyo         func_unit.o       simple
```

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CPUTracers.py.o     InstPBTrace.py.cc       inst_pb_trace.o     simple_thread.o
CPUTracers.py.pyo   InstPBTrace.py.o        inteltrace.o        static_inst.o
CheckerCPU.py.cc    InstPBTrace.py.pyo      kvm                 testers
CheckerCPU.py.o     StaticInstFlags.py.cc   minor               thread_context.o
CheckerCPU.py.pyo   StaticInstFlags.py.o    nativetrace.o       thread_state.o
CpuCluster.py.cc    StaticInstFlags.py.pyo  nop_static_inst.o   timing_expr.o
CpuCluster.py.o     TimingExpr.py.cc        null_static_inst.o  trace
CpuCluster.py.pyo   TimingExpr.py.o         o3
DummyChecker.py.cc  TimingExpr.py.pyo       pc_event.o
DummyChecker.py.o   activity.o              pred
root@5cb9d529d43a:/gem5/build/X86/cpu# cd ..
root@5cb9d529d43a:/gem5/build/X86# cd ..
root@5cb9d529d43a:/gem5/build# cd ..
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# ls
__pycache__  caches.py  simple-arm.py  simple-riscv.py  simple.py  simple_cache_sim.py
two_level.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cat simple_cache_sim.py
import m5
from m5.objects import System, SrcClockDomain, VoltageDomain, X86TimingSimpleCPU,
SystemXBar, Root, MemCtrl, DDR3_1600_8x8
from caches import L1ICache, L1DCache, L2Cache
from m5.params import Clock

class MySystem(System):
    def __init__(self, opts):
        super(MySystem, self).__init__()

        # Set up system
        self.clk_domain = m5.objects.SrcClockDomain()
        self.clk_domain.clock =Clock('1GHz')
        self.clk_domain.voltage_domain = m5.objects.VoltageDomain()

        self.mem_mode = 'timing'
        self.mem_ranges = [m5.objects.AddrRange('512MB')]

        # Create CPU
        self.cpu = X86TimingSimpleCPU()

        # Attach L1 caches
        self.cpu.icache = L1ICache(opts)
        self.cpu.dcache = L1DCache(opts)
        self.l2cache = L2Cache(opts)

        # Create system bus
        self.membus = SystemXBar()

        # Connect L1 caches to CPU
        self.cpu.icache.connectCPU(self.cpu)
        self.cpu.dcache.connectCPU(self.cpu)

        # Connect L1 to L2 cache
```

```
        self.cpu.icache.connectBus(self.membus)
        self.cpu.dcache.connectBus(self.membus)

        # Connect L2 cache to memory bus
        self.l2cache.connectCPUSideBus(self.membus)

        # Create memory controller
        self.mem_ctrl = MemCtrl()
        self.mem_ctrl.dram = DDR3_1600_8x8()
        self.mem_ctrl.dram.range = self.mem_ranges[0]

        # Connect memory controller to system bus
        self.mem_ctrl.port = self.membus.mem_side_ports

# Create system and root object
opts = None  # Use default options
system = MySystem(opts)
root = Root(full_system=False, system=system)

# Instantiate the simulation
m5.instantiate()
print("Beginning gem5 simulation...")
exit_event = m5.simulate()
print(f"Exiting @ tick {m5.curTick()} because {exit_event.getCause()}")
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# cd ..
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd ..
root@5cb9d529d43a:/gem5/configs# cd ..
root@5cb9d529d43a:/gem5# /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:47:57
gem5 executing on 5cb9d529d43a, pid 163
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

UnicodeDecodeError: 'ascii' codec can't decode byte 0xe2 in position 383: ordinal not in
range(128)

At:
  /usr/lib/python3.10/encodings/ascii.py(26): decode
  src/python/m5/main.py(605): main
root@5cb9d529d43a:/gem5# cd configs
root@5cb9d529d43a:/gem5/configs# cd learning_gem5
root@5cb9d529d43a:/gem5/configs/learning_gem5# cd part1
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# /gem5/build/X86/gem5.opt /gem5/
configs/learning_gem5/part1/simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
```

```
gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:51:36
gem5 executing on 5cb9d529d43a, pid 165
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

UnicodeDecodeError: 'ascii' codec can't decode byte 0xe2 in position 553: ordinal not in
range(128)

At:
  /usr/lib/python3.10/encodings/ascii.py(26): decode
  src/python/m5/main.py(605): main
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# grep --color='auto' -P -n "[^\x00-
\x7F]" /gem5/configs/learning_gem5/part1/simple_cache_sim.py
17:        # Create CPU
33:        # Connect L1 to L2
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# /gem5/build/X86/gem5.opt /gem5/
configs/learning_gem5/part1/simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:54:57
gem5 executing on 5cb9d529d43a, pid 168
command line: /gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/
simple_cache_sim.py

UnicodeDecodeError: 'ascii' codec can't decode byte 0xe2 in position 1028: ordinal not in
range(128)

At:
  /usr/lib/python3.10/encodings/ascii.py(26): decode
  src/python/m5/main.py(605): main
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# grep --color='auto' -P -n "[^\x00-
\x7F]" /gem5/configs/learning_gem5/part1/simple_cache_sim.py
33:        # Connect L1 to L2
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# nano simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# grep --color='auto' -P -n "[^\x00-
\x7F]" /gem5/configs/learning_gem5/part1/simple_cache_sim.py
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1# /gem5/build/X86/gem5.opt /gem5/
configs/learning_gem5/part1/simple_cache_sim.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Feb  1 2025 19:59:14
gem5 started Feb 17 2025 01:56:27
gem5 executing on 5cb9d529d43a, pid 172
```

command line: **/gem5/build/X86/gem5.opt /gem5/configs/learning_gem5/part1/simple_cache_sim.py**

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
src/cpu/base.cc:181: fatal: Number of ISAs (0) assigned to the CPU does not equal number of threads (1).
Memory Usage: 624712 KBytes
root@5cb9d529d43a:/gem5/configs/learning_gem5/part1#