

Praveen Kumar

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INTERESTS	Hardware security, Physically Unclonable Functions, Computer architecture, Embedded Systems	
EDUCATION	Technische Universität Darmstadt , Hessen, Germany Masters in Distributed Software Systems, <i>GPA of 1.41 on German scale (converts to 3.59/4.0 in US system)</i> Indian Institute of Technology , Mumbai, India Bachelors in Electrical Engineering, <i>Cumulative Performance Index (CPI) of 7.16 on a scale of 10.00</i> Vijaya Ratna Junior College , Hyderabad, India Intermediate (class XII), BIE Andhra Pradesh, <i>Percentage: 94.8% (2010)</i> Gowtham Model School , Rajahmundry, India Secondary school education (class X), <i>Percentage: 90.3% (2008)</i>	
PUBLICATIONS	Stephan Heuser, Bradley Reaves, Praveen Kumar Pendyala, Henry Carter, Alexandra Dmitrienko, Negar Negar, William Enck, Ahmad-Reza Sadeghi and Patrick Traynor; "Phonion: Practical Protection of Metadata in Telephony Networks" <i>Proceedings on Privacy Enhancing Technologies (PoPETs) 2017</i> . Stephan Heuser, Marco Negro, Praveen Kumar Pendyala and Ahmad-Reza Sadeghi; "DroidAuditor: Forensic Analysis of Application-Layer Privilege Escalation Attacks on Android" <i>Financial Cryptography and Data Security Conference, 2016, Barbados</i> . Kong, J., F. Koushanfar, P. K. Pendyala, A. - R. Sadeghi, and C. Wachsmann; "PUFatt: Embedded Platform Attestation Based on Novel Processor-Based PUFs" <i>Design Automation Conference (DAC) 2014, Best paper candidate, San Francisco</i> .	
RESEARCH EXPERIENCE	Implementing dual core ALU based PUF on FPGA with symmetric block placement and PDL tuning Guide: Prof. Farinaz Koushanfar, Dr. Joonho Kong <i>Autumn 2013</i> <i>Adaptive Computing and Embedded Systems Lab, Rice University</i> Employed symmetric placement of logic blocks in the two cores of dual core PUF to obtain a symmetric design. Proposed and implemented Programmable Delay Logic to match the remaining delay skews due to routing asymmetries. Evaluated the whole model by collecting results on intra-chip variations and response entropy/stability for different/identical challenges. Also implemented the model on two different Xilinx XUPV5 FPGA chips to evaluate inter-chip variations. Results collected are used for proof-of-concept in the paper submitted to the Design Automation Conference, 2014. Paper accepted on Feb., 2014. Undergraduate Thesis: APIs to access DRAM of a virtex 5 FPGA Guide: Prof. Sachin Patkar <i>Autumn 2013</i> <i>Department of Electrical Engineering, IIT Bombay</i> Implemented APIs which facilitate sending huge amounts of data (250MB) from PC to FPGA. Also, developed modules to access this data from DRAM for computations within the FPGA. Data communication between FPGA and PC achieved using Microsoft SIRC and DRAM access using Memory Interface Generator (MIG) tools. Interface, Testing and Evaluation of an ultra-low power current based PUF Guide: Prof. Farinaz Koushanfar <i>Summer 2013</i> <i>Adaptive Computing and Embedded Systems Lab, Rice University</i>	

Designed the tester to evaluate a PUF chip. Employed Microsoft SIRC for FPGA-PC communication and developed verilog modules for communication with the PUF chip. Data (challenges) received by FPGA is serially transmitted to PUF - Physically Unclonable Function - A module used extensively in hardware security. The responses of the chip are read back and transmitted to PC for further analysis.

Analysis of measurement circuits and feasibility of implementation on FPGA

Guide: Prof. Farinaz Koushanfar

Summer 2013

Adaptive Computing and Embedded Systems Lab, Rice University

Analyzed delay measurement circuits, REBEL (Regional delay based logic) precision of 0.1 nanoseconds and TDC (Time to Digital convertor) precision of 0.01 nanoseconds, and the feasibility of their implementation on FPGA without any standalone modules.

Microcontroller board development and interfacing

Guide: Prof. M. B. Patil

Summer 2012

Department of Electrical Engineering, IIT Bombay

Worked on the development of a Microcontroller board using 89c5132 microcontroller chip. Interfaced TWI, SPI, watchdog timer, timers and counters of the chip and external slaves Graphic LCD, Hexpad, and Amplifier circuit with microcontroller. Also attempted to build a low cost MP3 player.

ACADEMIC PROJECTS

Greedy algorithm for activity and task scheduling

Guide: Prof. Sachin Patkar

Autumn 2013

Course: Foundations of VLSI CAD, Electrical Engineering

Implemented greedy algorithm for activity and task scheduling in Scilab, C++ and Python. Analysed the time order and actual execution time for 3 different implementations in the 3 languages - rudimentary scilab implementation with bubble sort, python implementation using in-built objects sort, c++ implementation with heap sort.

Image processing

Guide: Prof. Arjun Arunachalam

Autumn 2012

Course: Image processing, Electrical Engineering

Improved corrupted images of an MRI scan of the brain using the concept of Radon transform. Performed iterative image reconstruction techniques for image enhancement in MATLAB.

Gravity sensor based game development on FPGA

Guide: Prof. J. John, Prof. M. B. Patil

Spring 2012

Course: Digital Circuits Lab

Created generic libraries in Verilog for interfacing LCD display unit with FPGA and special focus on modularity. Employed a G-sensor for intuitive Human-Machine interaction to maximize end user experience. The game essential has objects coming in seven lanes and the target is to direct the main object, using controller, from crashing. Also implemented a over-time level up mechanism which makes the speeds of oncoming traffic a function of time.

Opamp design

Guide: Prof. Anil Kottantharayil

Spring 2012

Course: Analog Lab

Designed a 5-stage opamp using matched n-p-n and BJT (n-p-n and p-n-p) transistors. The characteristics of the opamp are gain: 10^5 v/v, input resistance: 100 ohm, output resistance: 10^3 ohm, CMRR: 80dB. We used two stages for resistance matching, two more for gain and one for CMRR.

Hand held scanner from Optical mouse

Guide: Prof. Vasi

Spring 2011

Course: Introduction to Electronics

Hand held scanner using components of an Optical mouse and a 10 page term paper describing its internal working mechanism in detail.

Classical Pocket tanks game using C++

Guide: Prof. D. B. Patak

Autumn 2010

Course: Introduction to Computer Programming & Utilization, Computer Sciences

EzWindows for Graphical Interface on Linux.

PERSONAL &
MISCELLANEOUS
PROJECTS

Google Summer of Code 2014

Guide: Vladimir Pantelic

Summer 2014

Working with Beagleboard.org to implement a Linux kernel USB driver for Android device to act as a remote display and controller for Linux over USB using Android Open Accessory Protocol.

MIT India Health Tech 2014

Guide: Achuta Kadambi, MIT Media Labs

May 2014

One of the 120 students from India selected to participate in the MIT Media Labs India Health Tech workshop. Developed a prototype to stitch the retinal images collected from an ordinary split lamp for advanced retinal analysis.

MIT AITI Program project

Guide: Dr. Bryan Drake, MIT

June 2012- August 2012

One of the 45 students from IIT Bombay selected to participate in the Massachusetts Institute of Technology Accelerating Information Technology Initiative (AITI) program. Developed the prototype of an Android application that gives a one touch alert with location to notify about an emergency. Pitched the idea & demonstrated the prototype at MIT-AITI startup showcase.

Android application development for Moodle

Web n Coding Club, IIT Bombay

Summer 2012

I developed an Android application for Moodle. The application has more than 50,000 downloads. Moodle is an Open Source Course Management System.

Institute bus tracking system

December 2012 - present

We designed and developed a novel way to track vehicles confined in a small campus using Xbee mesh network. I'm one of the 3 core team members of the team. Developed and proving support to the Web and Android applications along with minor contributions to the Microcontroller coding for Xbee communication.

Facilitating FPGA/Microcontroller programming from Android device

Autumn 2012

Cross compiled the source code of an FPGA programmer (urjtag), written in C, using NDK tools to generate an Android executable thereby porting it to Android. Investigated into and found appropriate substitutes for the dependencies and cross compiled the dependent libraries in case no substitutes are available. The current constraint is the lack of jtag driver support for Android.

Analysis of power consumption by smart meters

Summer 2012

I ran algorithms on the Green Button Data, an emerging format of data for power consumption, to predict possible savings, abnormally high usage, peak usage timings, alternative sources and this was the only submission from India in United States of America Energy Department competition. The algorithms run on huge data sets on the order of 1 million data points extracted from xml files of size more than 7 MB. All processing is done using PHP and MySQL.

Other Android development activities

2011 - 2014

Developed an app for promoting Literature at IIT Bombay (2014), Anti-theft application that automatically takes picture of intruder on wrong passcode (2012), Jelly bean notification demonstration app (2012).

Other Web development activities

2010 - 2014

Developed the administrator web interface of literature for IIT Bombay (2014), Developed the complete backend for an online shopping cart as a single member (2011), A Fully functional machinery website using Google maps in a team of 5 (2011 winter), Facebook application in a team of 3 (2010 summer)

TEST SCORES

- **GRE:** Verbal: 148/170, Quantitative: 165/170, Writing: 4.0/6.0
- **TOEFL:** Total: 99/120 (Reading: 26/30, Listening: 24/30, Speaking: 23/30, Writing: 26/30)

SCHOLASTIC
ACHIEVEMENTS

- Recipient of A. Richard Newton Young Student Fellowship at the Design Automation Conference (DAC), San Francisco, 2014.

- Secured All India category Rank 1 in IIT JEE 2010 among 470,000 students all over India
- Secured All India category Rank 1 in ISAT (Test for admission to Indian Institute of Space Technology), 2010
- Shortlisted for KVPY (Kishore Vaigyanik Protsahan Yojana) scholarship awarded by the Government of India, 2010
- Secured District 1st in Ramanujan Maths Talent Test 2005 conducted by the Ramunujan Mathematics Academy
- Secured District 3rd in Ramanujan Maths Talent Test 2006 conducted by the Ramunujan Mathematics Academy

EXTRA-CURRICULAR ACTIVITIES	<ul style="list-style-type: none"> ● 1st in Institute hack night: Participated as a one member team and developed an anti-theft Android application, MugShot. It silently captures the face of intruder, as an anti-theft measure, on failing to unlock the device. Also an active participant in Yahoo HackU and other coding events. ● Guinness world record: Part of the Guinness world record of highest number of people solving a Rubiks cube simultaneously, set by IIT Bombay. ● Blogging: maintaining my own technical blog which has got 130,000+ hits so far.
TECHNICAL SKILLS	<p>Programming: Assembly, Kernel C, C, C++, Java, Python, Verilog (HDL), BlueSpec</p> <p>Operating Systems: Linux (Debian, Ubuntu, Fedora), Windows</p> <p>Analysis and Publishing Tools: Matlab, Scilab, R, L^AT_EX</p> <p>Electronic Design Tools: Xilinx ISE (all), Quartus, Keil, LabView, Eagle, LTSpice, NGSpice</p> <p>FPGAs: Xilinx XUPV5, ML505, ML605, Altera De0nano</p> <p>Microcontrollers: 8085 (microprocessor), 8051 family, Raspberry Pi</p> <p>Web Development: HTML, CSS, JavaScript, Ajax, PHP, MySQL</p> <p>APIs: Android, Google Maps - Android V2, Web V3</p>
RELEVANT COURSES	<p>Electrical Engineering: Processor Design, System Design, Testing and Verification of VLSI Circuits, VLSI Design Lab, Advanced computing for electrical engineers, Foundations of VLSI CAD, Microprocessors, Digital systems, Image processing, Signals and systems, Control systems, Communication systems, Analog circuits, Network theory, Radar systems, Electromagnetic waves, Electronic Devices & Circuits</p> <p>Mathematics: Probability & Random Processes, Calculus, Linear Algebra, Data Analysis and Interpretation, Complex Analysis, Differential Equations I, Differential Equations II</p>
REFERENCES	<ul style="list-style-type: none"> ● Prof. Farinaz Koushanfar (Summer Internship Guide) Department of Electrical and Computer Engineering, Rice University, Houston, USA Email: farinaz@rice.edu ● Prof. Sachin Patkar (Undergraduate Research Thesis Guide) Department of Electrical Engineering, IIT Bombay, Mumbai, India Email: patkar@ee.iitb.ac.in ● Dr. Joonho Kong (Research Paper Co-Author and Guide) Adaptive Computing and Embedded Systems (ACES) Lab, Rice University, Houston, USA Email: joonho.kong@rice.edu