

# HDL Dependency Analysis Report

Project: RISC-V SoC Design | Generated: February 27, 2026 at 23:57

Files Analyzed: 15

## 1. Executive Summary

| Modules  | Instantiations | Max Depth  | Cycles            |
|----------|----------------|------------|-------------------|
| 12       | 11             | 3          | 0                 |
| Includes | Packages       | Interfaces | Symbol Collisions |
| 0        | 2              | 1          | 0                 |

## 2. Module Hierarchy

| Module              | Fan-In | Fan-Out | Depth | File            |
|---------------------|--------|---------|-------|-----------------|
| <b>soc_top</b>      | 0      | 4       | N/A   | soc_top.sv      |
| <b>cpu_core</b>     | 1      | 3       | 1     | cpu_core.sv     |
| <b>mem_ctrl</b>     | 1      | 1       | 1     | mem_ctrl.sv     |
| <b>bus_fabric</b>   | 1      | 1       | 1     | bus_fabric.sv   |
| <b>peripheral</b>   | 1      | 1       | 1     | peripheral.sv   |
| <b>alu</b>          | 1      | 0       | 1     | alu.sv          |
| <b>reg_file</b>     | 1      | 0       | 1     | reg_file.sv     |
| <b>decoder</b>      | 1      | 0       | 1     | decoder.sv      |
| <b>sram_bank</b>    | 1      | 0       | 2     | sram_bank.sv    |
| <b>arbiter</b>      | 1      | 0       | 1     | arbiter.sv      |
| <b>timer</b>        | 1      | 0       | 1     | timer.sv        |
| <b>unused_debug</b> | 0      | 0       | N/A   | unused_debug.sv |

## Root Modules

soc\_top, unused\_debug

## 3. Include Dependencies

## 4. Package Imports

| Package | Symbols Exported | Files Importing |
|---------|------------------|-----------------|
| axi_pkg | 3                | 2               |
| soc_pkg | 2                | 2               |

## 5. Parameter Overrides

| Instance | Module     | Parameter | Value  | Default |
|----------|------------|-----------|--------|---------|
| u_cpu    | cpu_core   | ADDR_W    | ADDR_W | 32      |
| u_cpu    | cpu_core   | DATA_W    | DATA_W | 32      |
| u_mem    | mem_ctrl   | ADDR_W    | ADDR_W | 32      |
| u_periph | peripheral | ID        | i      | 0       |
| u_regs   | reg_file   | clk       | clk    |         |
| u_regs   | reg_file   | WIDTH     | DATA_W | 32      |

## 6. Issues & Findings

## Recommendations

- Dependency graph is clean. Continue monitoring as design evolves.

## 7. Analysis Methodology

This report was generated using HDL dependency analysis, which extracts and resolves module hierarchies, include directives, package imports, parameter overrides, and interface bindings from Verilog/SystemVerilog source.

| Component               | Method   |
|-------------------------|--|
| <b>Module Hierarchy</b> | Regex parsing of module/endmodule; instance instantiation tracking |
| <b>Includes</b>         | Resolution of `include directives; circular dependency detection   |
| <b>Packages</b>         | SystemVerilog package definition and import resolution             |
| <b>Parameters</b>       | Extraction of parameter overrides in instance declarations         |
| <b>Interfaces</b>       | Interface and modport definition; binding analysis                 |
| <b>Symbols</b>          | Cross-file symbol resolution; collision detection                  |

### Issue Severity Definitions

- **Critical:** Module cycles, circular includes
- **High:** Unresolved includes, unresolved packages
- **Medium:** High fan-out, symbol collisions, type mismatches
- **Low:** Orphan modules, unused symbols