

HDL Dependency Analysis Report

Project: RISC-V SoC Design | Generated: February 27, 2026 at 23:57

Files Analyzed: 15

1. Executive Summary

Modules	Instantiations	Max Depth	Cycles
12	11	3	0
Includes	Packages	Interfaces	Symbol Collisions
0	2	1	0

2. Module Hierarchy

Module	Fan-In	Fan-Out	Depth	File
soc_top	0	4	N/A	soc_top.sv
cpu_core	1	3	1	cpu_core.sv
mem_ctrl	1	1	1	mem_ctrl.sv
bus_fabric	1	1	1	bus_fabric.sv
peripheral	1	1	1	peripheral.sv
alu	1	0	1	alu.sv
reg_file	1	0	1	reg_file.sv
decoder	1	0	1	decoder.sv
sram_bank	1	0	2	sram_bank.sv
arbiter	1	0	1	arbiter.sv
timer	1	0	1	timer.sv
unused_debug	0	0	N/A	unused_debug.sv

Root Modules

soc_top, unused_debug

3. Include Dependencies

4. Package Imports

Package	Symbols Exported	Files Importing
axi_pkg	3	2
soc_pkg	2	2

5. Parameter Overrides

Instance	Module	Parameter	Value	Default
u_cpu	cpu_core	ADDR_W	ADDR_W	32
u_cpu	cpu_core	DATA_W	DATA_W	32
u_mem	mem_ctrl	ADDR_W	ADDR_W	32
u_periph	peripheral	ID	i	0
u_regs	reg_file	clk	clk	
u_regs	reg_file	WIDTH	DATA_W	32

6. Issues & Findings

Recommendations

- Dependency graph is clean. Continue monitoring as design evolves.

7. Analysis Methodology

This report was generated using HDL dependency analysis, which extracts and resolves module hierarchies, include directives, package imports, parameter overrides, and interface bindings from Verilog/SystemVerilog source.

Component	Method
Module Hierarchy	Regex parsing of module/endmodule; instance instantiation tracking
Includes	Resolution of `include directives; circular dependency detection
Packages	SystemVerilog package definition and import resolution
Parameters	Extraction of parameter overrides in instance declarations
Interfaces	Interface and modport definition; binding analysis
Symbols	Cross-file symbol resolution; collision detection

Issue Severity Definitions

- **Critical:** Module cycles, circular includes
- **High:** Unresolved includes, unresolved packages
- **Medium:** High fan-out, symbol collisions, type mismatches
- **Low:** Orphan modules, unused symbols