MP6602

35V, Stepper Motor Driver with Stall Detection and Serial Interface

DESCRIPTION

The MP6602 is a stepper motor driver with a built-in indexer/translator and internal current regulation. The internal current sense means that the MP6602 does not require external current-sense resistors.

The MP6602 operates across a 4.5V to 35V input voltage (V_{IN}) range. It can deliver a motor current up to 4A per phase, depending on the ambient temperature and PCB layout.

The MP6602 can operate a bipolar or unipolar stepper motor in full, half-, quarter-, eighth-, 1/16-, and 1/32-step modes.

Internal safety and diagnostic features include rotor stall detection, open load detection, over-current protection (OCP), input over-voltage protection (OVP) and under-voltage protection (UVP), thermal warning, ad thermal shutdown.

The automatic hold current mode can lower the winding current to automatically save power when a full current is not required, such as when the motor is stopped or lightly loaded.

The motor's back EMF (BEMF) can be measured. The BEMF can be read via the serial interface for advanced diagnostic and control functions.

The serial interface sets control modes such as the step mode, direction, and output current. The serial interface can also read diagnostic registers. The STEP and DIR input pins can adjust motor motion without serial bus transactions.

The MP6602 is a highly integrated solution for stepper motor driving. It is available in a small QFN-25 (4mmx5mm) package.

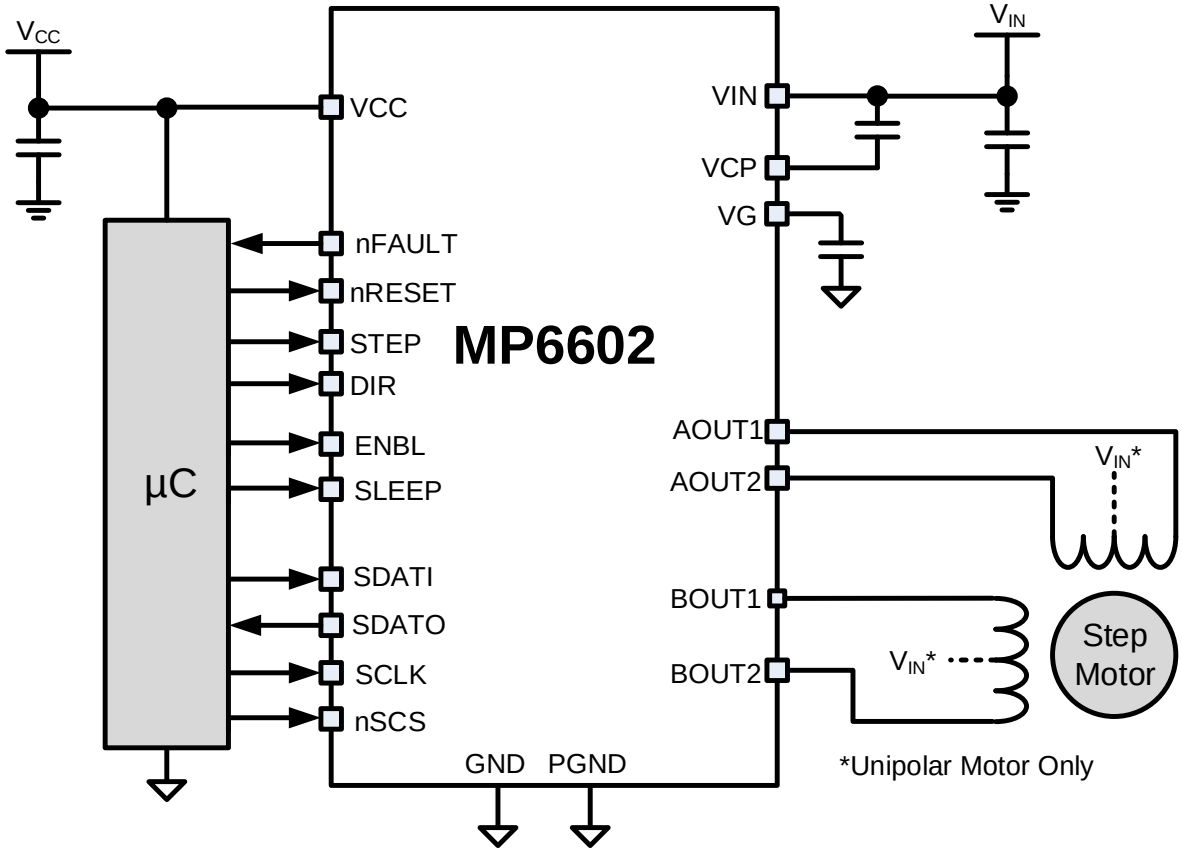
FEATURES

- 4.5V to 35V Operating Input Voltage (V_{IN}) with 40V Absolute Maximum
- Two Internal Full-Bridge Drivers
- Supports Unipolar Motor
- Up to 1/32-Step Microstepping
- Internal Current-Sensing and Regulation
- Low On Resistance:
  - High-Side MOSFET (HS-FET): 60mΩ
  - Low-Side MOSFET (LS-FET): 30mΩ
- Serial Control Interface
- Enable and Step Input Pins
- 3.3V and 5V Compatible Logic Supply
- 4A Maximum Output Current
- Automatic Hold Current
- Automatic Current Decay
- Diagnostic Functions, Including:
  - Rotor Stall Detection
  - Back EMF Measurement
  - Over-Current Protection (OCP)
  - Open Load Detection
  - Over-Voltage Protection (OVP)
  - Under-Voltage Protection (UVP)
  - Thermal Warning and Shutdown
- Fault Indication Output
- Available in a Space-Saving QFN-25 (4mmx5mm) Package

APPLICATIONS

- Bipolar Stepper Motors
- 3D Printers
- Laser Printers and Copiers
- Textile Machines

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6602GV	QFN-25 (4mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6602GV-Z).

TOP MARKING

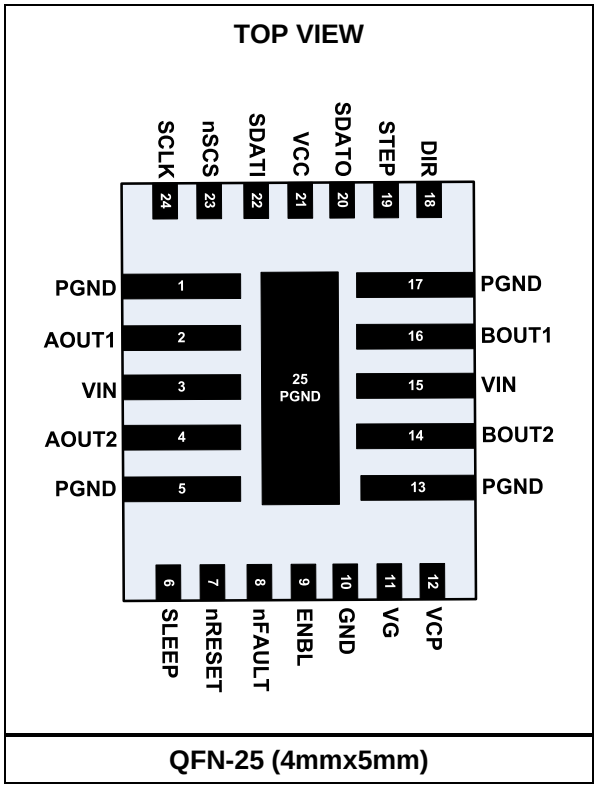
MPSYWW

MP6602

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6602: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-25 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
21	VCC	**Logic power supply.** Decouple the VCC pin to ground with a minimum 100nF ceramic capacitor.
3, 15	VIN	**Input supply voltage.** All VIN pins must be connected to the same supply. Decouple the VIN pin to ground with a minimum 100nF ceramic capacitor. It is recommended to use a 1µF capacitor. Note that additional bulk capacitance is required.
1, 5, 13, 17, 25	PGND	**Power ground for H-bridge outputs.**
10	GND	**Signal ground.**
2	AOUT1	**Bridge A output terminal 1.**
4	AOUT2	**Bridge A output terminal 2.**
16	BOUT1	**Bridge B output terminal 1.**
14	BOUT2	**Bridge B output terminal 2.**
12	VCP	**Charge pump output**. Connect a 1µF, 16V ceramic capacitor from the VCP pin to VIN.
23	nSCS	**Serial chip selection.** The nSCS pin is internally pulled up to VCC.
22	SDATI	**Serial data input.** The SDATI pin is pulled down internally.
20	SDATO	**Serial data output.** The SDATO pin is pulled down internally.
24	SCLK	**Serial clock.** Data shifts on the rising edge of SCLK. The SCLK pin is pulled down internally.
6	SLEEP	**Sleep mode input.** Pull the SLEEP pin to logic high to enter low-power sleep mode. The SLEEP pin is pulled down internally.
11	VG	**Low-side MOSFET (LS-FET) gate drive voltage.** Connect a 1µF, 16V ceramic capacitor from the VG pin to ground.
9	ENBL	**Enable input.** When the ENBL pin is active, the outputs are enabled and the STEP input is recognized. This pin can be active high or active low depending on what has been configured via the EN bit. ENBL is pulled down internally.
19	STEP	**Step input.** A rising edge on the STEP pin advances the motor by one increment. The STEP pin is pulled down internally.
18	DIR	**Direction input.** The DIR pin works in conjunction with the DIR bit in the CTRL register to set the step direction. This pin is pulled down internally.
8	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. It pulls to logic low if a fault condition is detected. The nFAULT pin needs an external pull-up resistor when it is used.
7	nRESET	**Device reset input.** Pull the nRESET pin to active low input to reset all registers to their initial states. The nRESET pin is internally pulled up to VCC.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
Supply voltage (V_{CC}) .....-0.3V to +7V
xOUTx voltage (V_{AOUT1}, V_{AOUT2}, V_{BOUT1}, V_{BOUT1})...
.....-0.7V to +45V
xOUTx voltage (V_{AOUT1}, V_{AOUT2}, V_{BOUT1}, V_{BOUT1})
(t < 100ns).....-2V
VCP .....V_{IN} to V_{IN} + 6.5V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
.....4.22W
Storage temperature ..... -55°C to +150°C
Junction temperature .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) .....±1.5kV
Charged device model (CDM) .....±1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 35V
Supply voltage (V_{CC}) .....3V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-25 (4mmx5mm).....29.6....2.1....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5		35	V
Logic supply voltage	V_{CC}		3	5	5.5	V
Quiescent current	I_{INQ}	ENBL = 0, SLEEP = 0, with no load		0.9	9.8	mA
	$I_{INSLEEP}$	SLEEP = 1		1.5		µA
	I_{CCQ}	ENBL = 0, SLEEP = 0, with no load		3.5		mA
	$I_{CCSLEEP}$	SLEEP = 1		1.3		µA
Internal MOSFETs						
Output on resistance	R_{HS}	I_{OUT} = 1A, T_J = 25°C		60	85	mΩ
		I_{OUT} = 1A, T_J = 85°C		75		mΩ
	R_{LS}	I_{OUT} = 1A, T_J = 25°C		30	55	mΩ
		I_{OUT} = 1A, T_J = 85°C		38		mΩ
Body diode forward voltage	V_F	I_{OUT} = 1A			1.1	V
Control Logic Inputs						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IN} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IN} = 0V	-20		+20	µA
Internal pull-down resistance	R_{PD}	To GND		500		kΩ
Internal pull-up resistance	R_{PU}	To VCC		500		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 5V			1	µA
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_RISE}				4.5	V
V_{IN} UVLO hysteresis	ΔV_{IN_RISE}			500		mV
V_{CC} UVLO rising threshold	V_{CC_RISE}				3	V
V_{CC} UVLO hysteresis	ΔV_{CC_RISE}			70		mV
V_{IN} over-voltage protection (OVP) rising threshold	V_{OVP}		35.2	37	39.5	V
V_{IN} OVP hysteresis	ΔV_{OVP}			2		V
Open load detection current	I_{OL}			180		µA
Over-current (OC) trip level	I_{OCP1}	Sinking	5	10		A
	I_{OCP2}	Sourcing	5	10		A
OC deglitch time	t_{OCP}			1		µs
Thermal shutdown temperature	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			15		°C
Thermal warning temperature	T_{TW}			150		°C

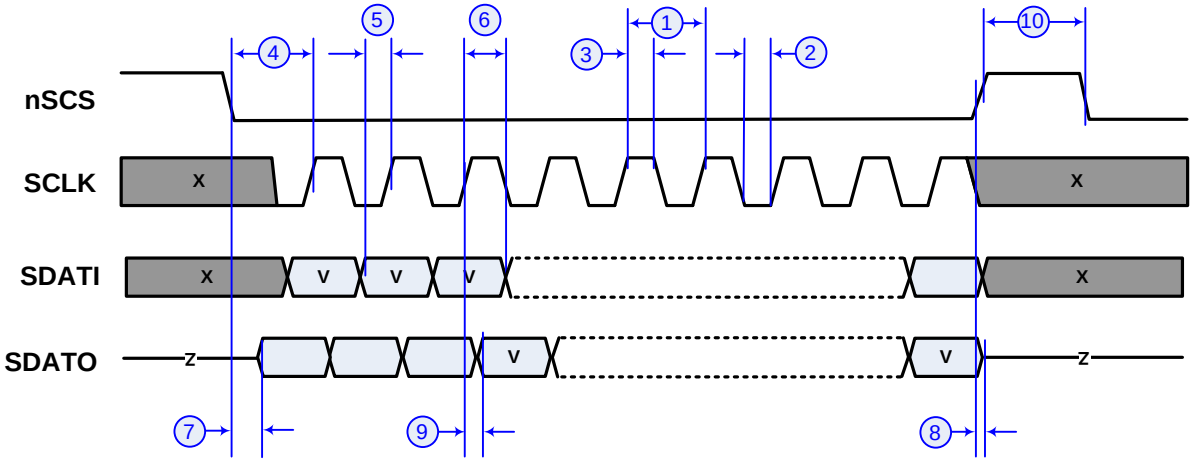
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current control						
Constant off time	t_{OFF}	OT2~OT0 = 100	35	40	45	µs
Blanking time	t_{BLANK}			2		µs
Crossover dead time	t_{DT}	HS off to LS on or LS off to HS on for one bridge arm		100		ns
Current trip accuracy	ΔI_{TRIP}	I = 71% to 100% of I_{PEAK}	-4.5		+4.5	%
		I = 38% to 67% of I_{PEAK}	-10		+10	%
		I < 34% of I_{PEAK}	-15		+ 15	%
Back EMF Measurement						
BEMF gain	A_{BEMF}	BEG = 000	0.085	0.1	0.115	V/V
		BEG = 001	0.185	0.2	0.215	
		BEG = 010	0.48	0.5	0.52	
		BEG = 011	0.98	1	1.02	
		BEG = 100	1.98	2	2.02	
		BEG = 101	4.93	5	5.06	
		BEG = 110	9.8	10	10.15	
		BEG = 111	19.4	20	20.4	
BEMF A/D accuracy	ΔADC	V_{BEMF} = 0.5V	-5		+5	LSB
		V_{BEMF} = 4.5V	-8		+8	

TIMIMG CHARACTERISTICS (5)

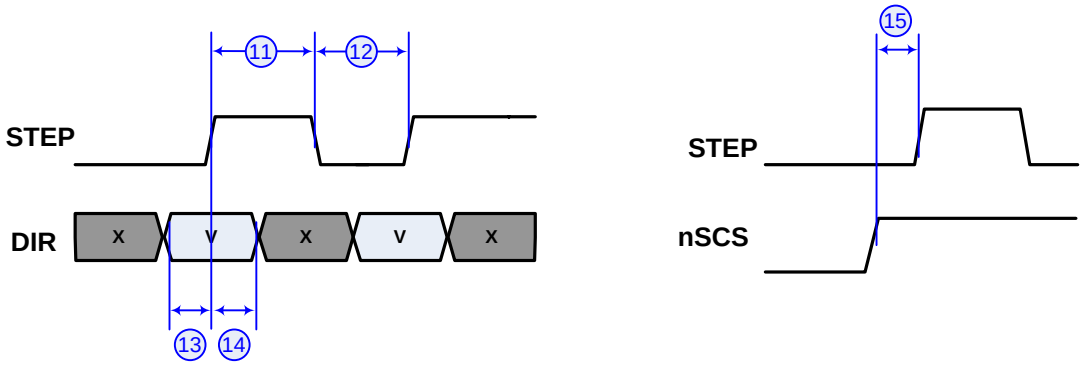
V_{IN} = 24V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted.



Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK cycle time	t1		100			ns
SCLK frequency			0.1		10	MHz
SCLK high time	t2		50			ns
SCLK low time	t3		50			ns
SCLK rise/fall time					50	ns
Set-up time nSCS low to SCLK rising	t4		30			ns
Set-up time SDATI valid to SCLK rising	t5		15			ns
Hold time SCLK rising to SDATI invalid	t6		10			ns
nSCS low to SDTAO enabled	t7		40			ns
nSCS high to SDATO Hi-Z	t8				50	ns
SCLK rising to SDATO valid	t9	C_L < 100pF			10	ns
nSCS inactive time	t10		100			ns

TIMIMG CHARACTERISTICS (5) *(continued)*

V_{IN} = 24V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted.



Parameter	Symbol	Condition	Min	Typ	Max	Units
STEP minimum high time	t11		1			µs
STEP minimum low time	t12		1			µs
Set-up time DIR to STEP rising	t13		200			ns
Hold time DIR to STEP rising	t14		200			ns
Minimum time nSCS inactive to STEP rising (6)	t15		2			µs

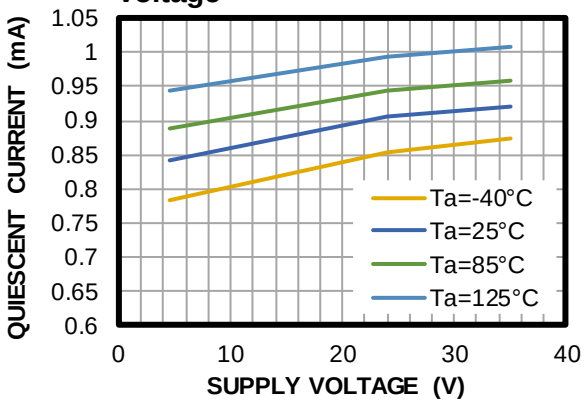
Notes:

5) Not subject to production testing. Specified by design.
6) This only applies to writes that change the state of the STEP, EN, or DIR bits in the CTRL register, or writes to the TSTP register.

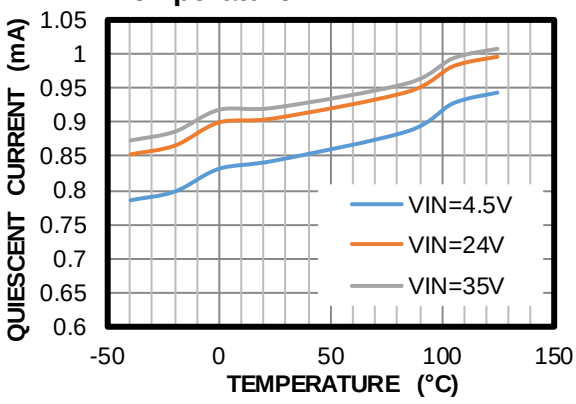
TYPICAL CHARACTERISTICS

V_{IN} = 24V, unless otherwise noted.

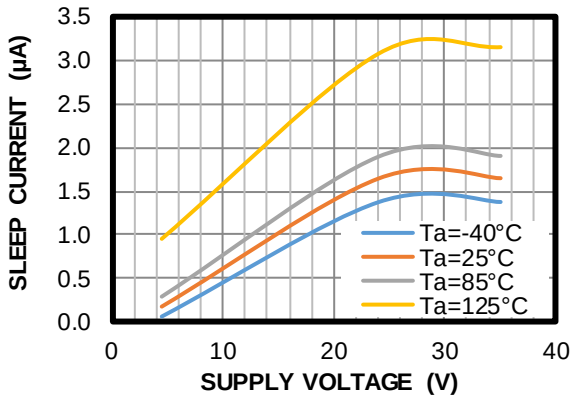
Quiescent Current vs. Supply Voltage



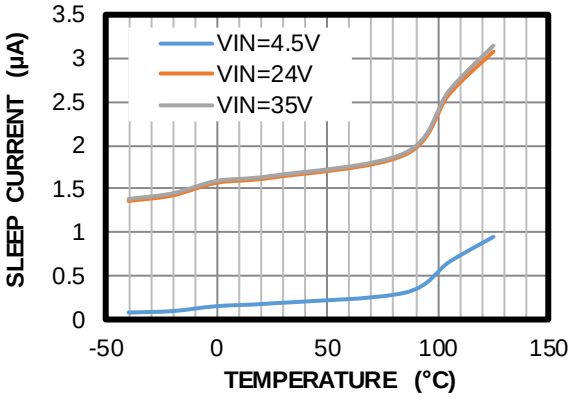
Quiescent Current vs. Temperature



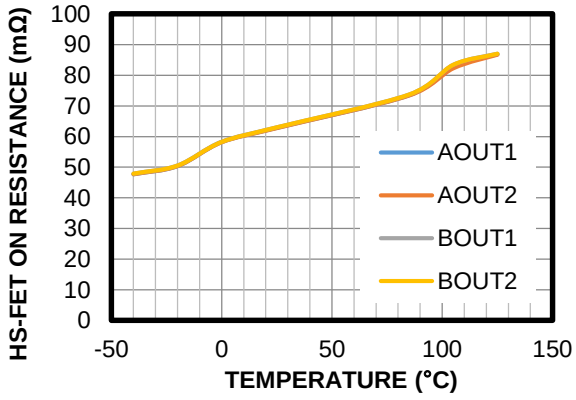
Sleep Current vs. Supply Voltage



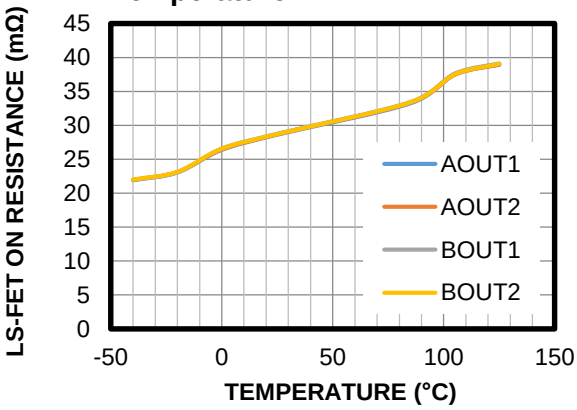
Sleep Current vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

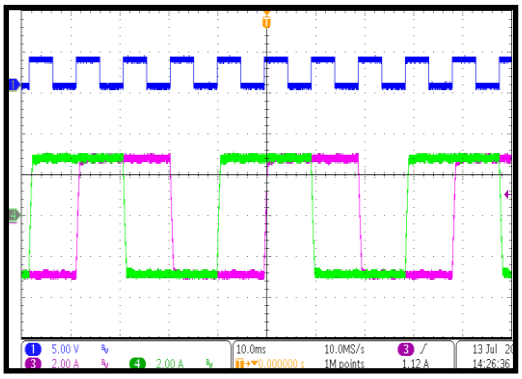


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, I_{PEAK} = 4A, T_A = 25°C, bipolar stepper motor (R = 0.8Ω, L = 7mH/phase), unless otherwise noted.

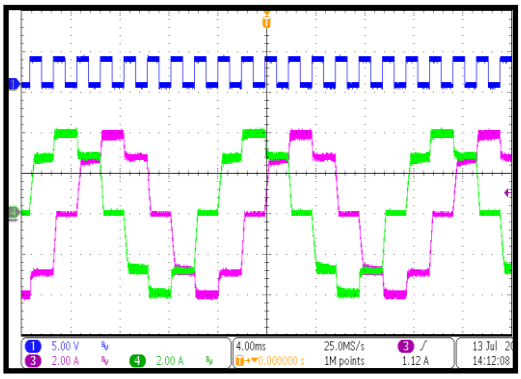
Full Step

CH1: STEP
CH4: I_{OUT-B}
CH3: I_{OUT-A}



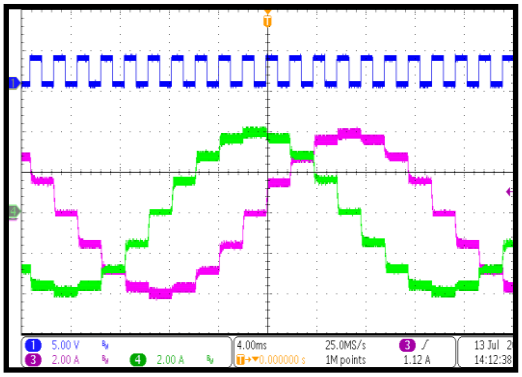
Half-Step

CH1: STEP
CH4: I_{OUT-B}
CH3: I_{OUT-A}



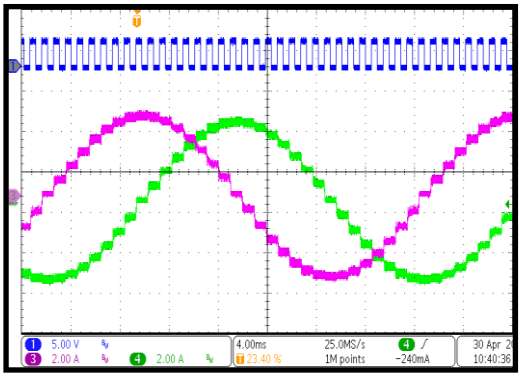
1/4 Microstepping

CH1: STEP
CH4: I_{OUT-B}
CH3: I_{OUT-A}



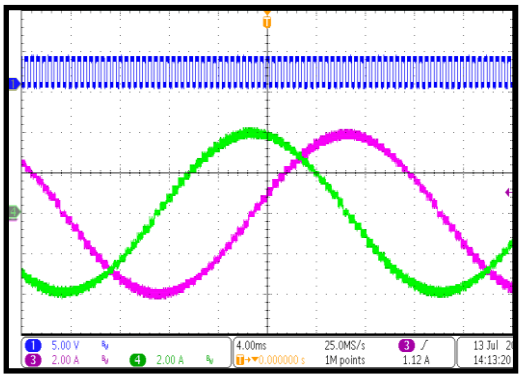
1/8 Microstepping

CH1: STEP
CH3: I_{OUT-A}
CH4: I_{OUT-B}



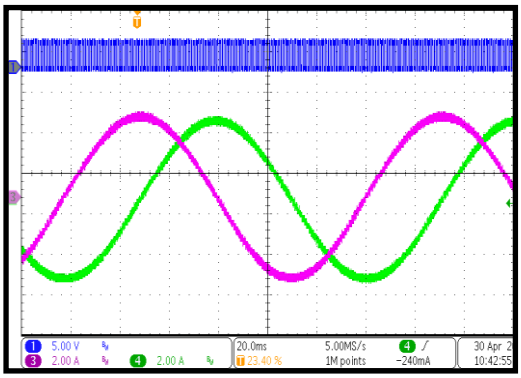
1/16 Microstepping

CH1: STEP
CH4: I_{OUT-B}
CH3: I_{OUT-A}



1/32 Microstepping

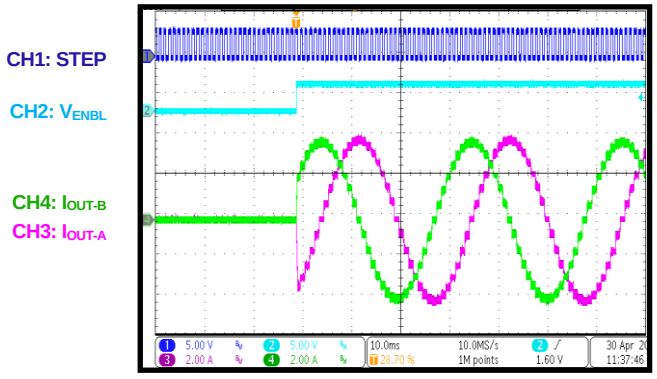
CH1: STEP
CH3: I_{OUT-A}
CH4: I_{OUT-B}



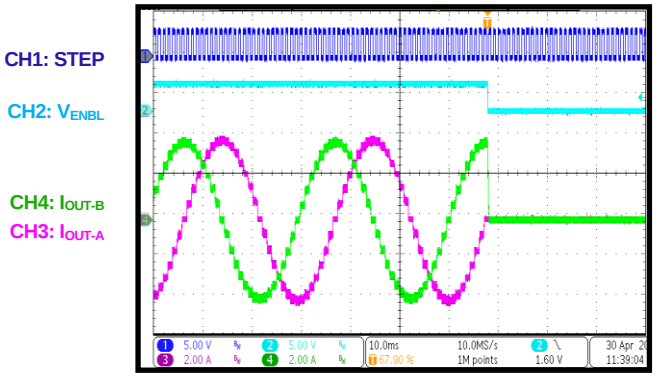
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, I_{PEAK} = 4A, T_A = 25°C, bipolar stepper motor (R = 0.8Ω, L = 7mH/phase), unless otherwise noted.

Output Enabled

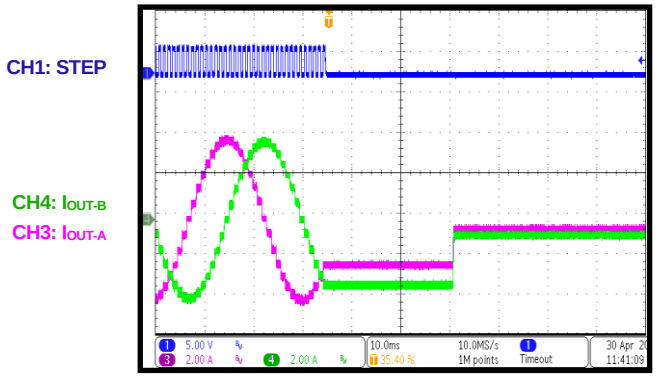


Output Disabled



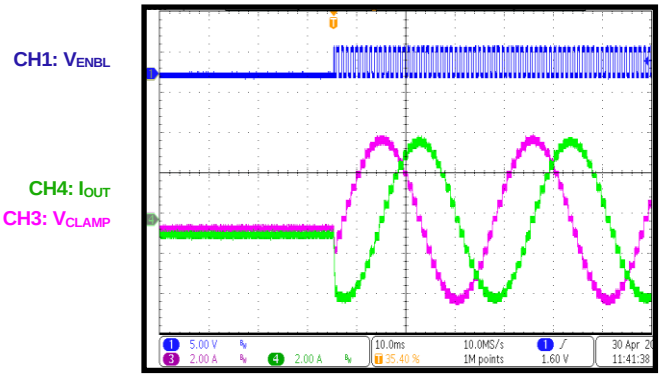
Automatic Hold Current Entry

Peak hold current = 1A



Automatic Hold Current Exit

Peak hold current = 1A



FUNCTIONAL BLOCK DIAGRAM

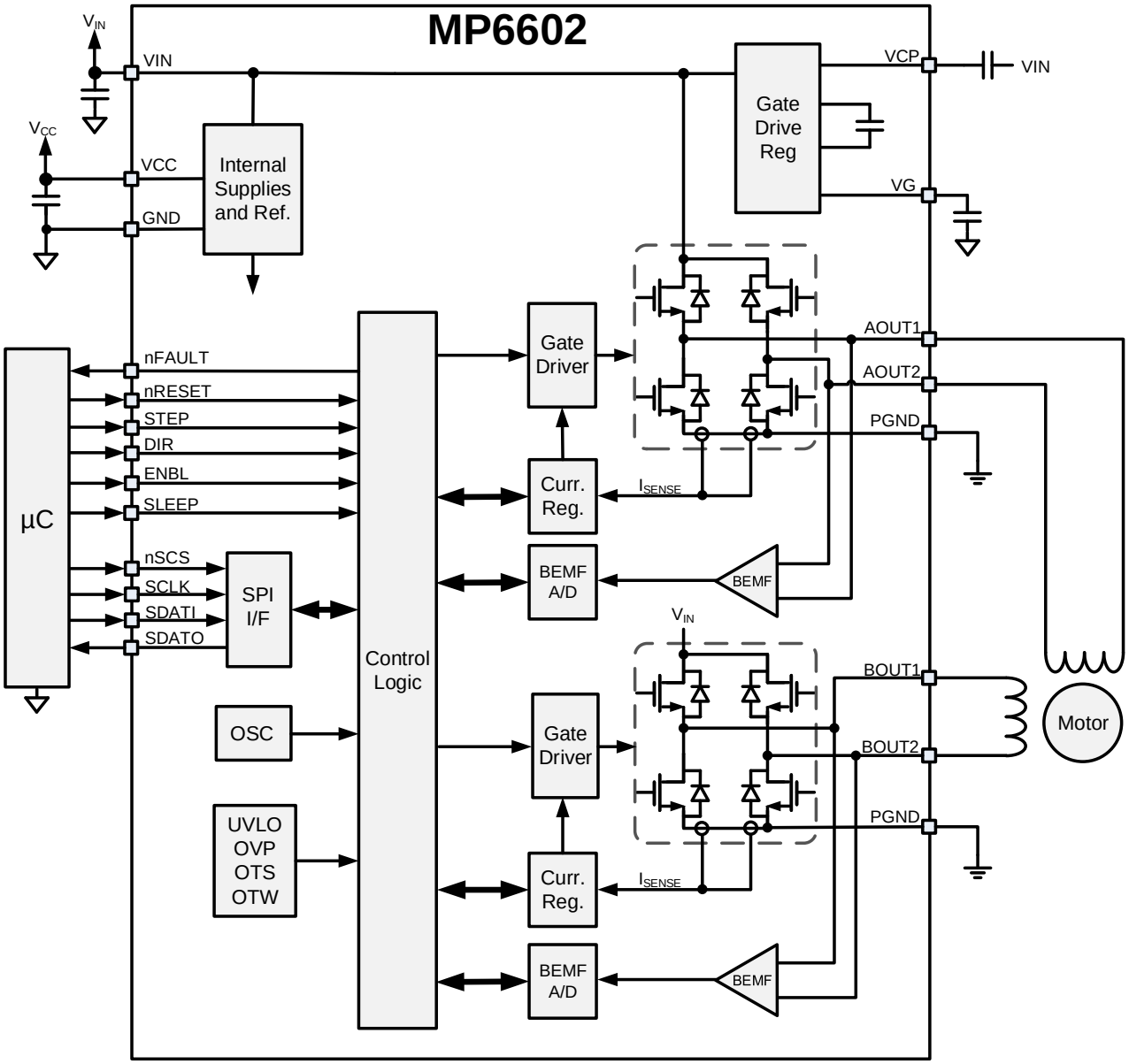


Figure 1: Functional Block Diagram

OPERATION

The MP6602 is an advanced stepper motor driver. It integrates eight N-channel power MOSFETs connected as two full H-bridges and operates across a wide 4.5V to 35V input voltage (V_{IN}) range.

A serial peripheral interface (SPI) configures device operation, reads back the device's status, and accesses diagnostic information. In addition, the motor may be stepped when logic signals are applied to the STEP and DIR input pins.

The MP6602 is designed to operate bipolar and unipolar stepper motors in full, half-, quarter-, eighth-, 1/16-, and 1/32-step modes. At each step, the current for each full-bridge is set by the output voltage of its digital-to-analog converter (DAC), which is controlled by the translator's output.

The currents in each of the two outputs are regulated with configurable, constant-off-time, pulse-width modulation (PWM) control circuitry.

The integrated, internal current sense removes the external current-sense resistor requirement. The peak motor current can be set by writing to the SPI interface.

nRESET, SLEEP, and ENBL Operation

Driving the nRESET pin's input active low initializes the device and resets all register contents to their start-up values. The H-bridge outputs are be disabled, the indexer is reset, and all faults are cleared. The nRESET pin has an internal pull-up resistor connected to the VCC pin.

Driving the SLEEP pin high puts the device in a low-power sleep state. In this state, the gate drive charge pump is stopped, and all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when SLEEP is active high.

When the MP6602 wakes up from a sleep state, it typically takes about 1ms before the device can issue a STEP command. This allows the internal circuitry to stabilize. The SLEEP pin has an internal pull-down resistor.

The ENBL pin works with the EN bit of the CTRL register to control the output drivers. The value from the pin is exclusive-ORed with the value of the register bit.

If the result is 1, the output H-bridge outputs are enabled, and the rising edges on the STEP pin are recognized. If the result is 0, the H-bridge outputs are disabled, and the STEP input is ignored.

For example, if the ENBL pin is low, then the outputs are enabled if the EN bit is set to 1; if the ENBL pin is high, the outputs are enabled if the EN bit is set to 0. Otherwise, the outputs are disabled.The ENBL pin has an internal pull-down resistor.

Stepping

To increment or decrement the contents in the TSTP register, there must be a rising edge on the STEP input, or a 1 must be written to the STEP bit in the CTRL register. To determine if the register is incremented or decremented, the state of DIR pin is exclusive-ORed with the DIR control bit.

The translator uses the value in the TSTP register to control the magnitude and direction of the current driven in each winding.

In addition to moving the motor using the STEP bit or input pin, the TSTP register can be accessed directly (read and written) via the SPI interface. This allows users to read back the current position or jump to any spot in the step table (see the Appendix 1 section on page 31).

Step Mode Selection

The MP6602 supports full step, half-step, quarter-step, eighth-step, 1/16-step, and 1/32-step modes for progressively finer step resolution and control. The step mode is selected by the MS2~MS0 bits in the CTRL register (see Table 1)

Table 1: CTRL Register

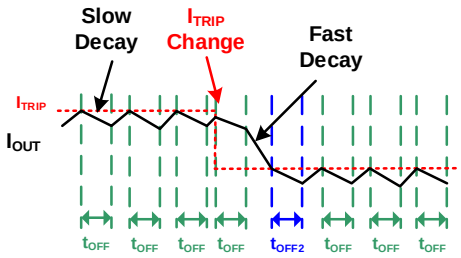
MS2~MS0	Step Mode
000	Full step (70%)
001	Half-step
010	Quarter-step
011 (reset value)	Eighth-step
100	1/16-step
101	1/32-step

Current Control Operation

The winding current is regulated by a constant off-time PWM current control circuit, which uses an automatic decay mode to accurately regulate the winding current. The process to regulate the winding current is described below.

1. At the beginning of a PWM cycle, a diagonal pair of MOSFETs turns on and drives current through the motor winding.
2. The current increases in the motor winding, which is then sensed by an internal current-sense circuit. Note that the MOSFETs are always on during the initial blanking time (t_{BLANK}).
3. When the current reaches the current trip threshold (I_{TRIP}), the internal current comparator turns off the high-side MOSFET (HS-FET) and turns on the low-side MOSFET (LS-FET). The winding current freewheels through the two LS-FETs (slow decay).
4. The current decays for the constant off time (t_{OFF}).
5. If the current is below the I_{TRIP} threshold at the end of t_{OFF}, then a new PWM cycle begins.
6. If the current exceeds the I_{TRIP} threshold, fast decay mode is initiated by reversing the state of the H-bridge outputs. This mode lasts until the winding current drops below I_{TRIP}.
7. Both LS-FETs turn on, and slow decay mode is activated for t_{OFF}. Then a new PWM cycle begins.

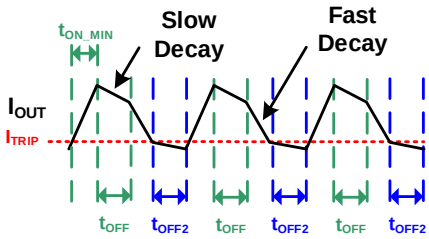
Figure 3 shows automatic decay mode operation when the current is being reduced due to a step input.



Slow decay during t_{OFF}, unless $I_{OUT} > I_{TRIP}$ at end of t_{OFF}

Figure 3: Automatic Decay Mode

In some cases (e.g. when there is a high voltage and low inductance, or small currents are being regulated), the minimum on time of the PWM cycle (set by the blanking time described above) can force the current to rise above the target I_{TRIP} level. In this case, both slow and fast decay mode alternate (see Figure 4).



Current regulation for low current / low inductance

Figure 4: Slow and Fast Decay Mode

t_{OFF} is determined by the OT2~OT0 bits in the CTRL register (see Table 2).

Table 2: OT2~OT0 Bits

OT2~OT0	Off Time (t_{OFF})
000	20μs
001	25μs
010	30μs
011	35μs
100 (reset value)	40μs
101	45μs
110	50μs
111	55μs

Unipolar Mode Operation

In unipolar mode, only one LS-FET for each winding is driven, while the other outputs are in high impedance. Unipolar mode always operates in slow decay mode, meaning there is no fast decay mode for unipolar motors.

Unipolar mode operation is described below.

1. The common terminal of the unipolar motor is connected to the power supply.
2. At the beginning of a PWM cycle, one LS-FET turns on. For a positive current, the xOUT1 (e.g. AOUT1 or BOUT1) pin's output is driven low. For a negative current, the xOUT2 (e.g. AOUT2 or BOUT2) pin is driven low.
3. The current increases in the motor winding, which is then sensed by an internal current-

sense circuit. Note that during t_{BLANK}, the MOSFETs are always turned on.

4. When the current reaches I_{TRIP}, the internal current comparator turns off the LS-FET and turns on the HS-FET. The winding current freewheels through the HS-FET (slow decay).
5. The current decays for t_{OFF}.
6. At the end of t_{OFF}, a new PWM cycle begins.

Unipolar operation can be selected via the UNI bit in the CTRL2 register.

Blanking Time

There is typically a current spike during the PWM turn-on time due to the body diode's reverse-recovery current, or the motor winding's distributed capacitance. This current spike must be filtered, or the current may be regulated at a value that is too low.

After the PWM cycle begins, the output of the current-sense comparator is ignored for a fixed blanking time. This blanking time also results in a minimum on time for the PWM cycle.

The blanking time (which is also the minimum on time) is configured via the BT2~BT0 bits in the CTRL2 register (see Table 3).

Table 3: BT2~BT0 Bits

BT2~BT0	Blanking Time (t_{BLANK})
0x00	250ns
0x01	500ns
0x02	1µs
0x03	1.5µs
0x04 (reset value)	2µs
0x05	2.5µs
0x06	3µs
0x07	3.5µs

Current Setting

The full-scale (100%) regulation current (I_{PEAK}) is set by the IS5~IS0 bits in the ISET register (see Table 4).

Table 4: IS5~IS0

IS5~IS0 (IL5~IL0)	Peak Current (I_{PEAK})	IS5~IS0 (IL5~IL0)	Peak Current (I_{PEAK})
0x00	125mA	0x10	2.13A
0x01	250mA	0x11	2.25A
0x02	375mA	0x12	2.38A
0x03	500mA	0x13	2.5A
0x04	625mA	0x14	2.63A
0x05	750mA	0x15	2.75A
0x06	875mA	0x16	2.88A
0x07	1.0A	0x17	3.0A
0x08	1.13A	0x18	3.12A
0x09 (reset value)	1.25A	0x19	3.25A
0x0A	1.38A	0x1A	3.38A
0x0B	1.5A	0x1B	3.5A
0x0C	1.63A	0x1C	3.63A
0x0D	1.75A	0x1D	3.75A
0x0E	1.88A	0x1E	3.88A
0x0F	2.0A	0x1F	4.0A

The translator output controls two digital-to-analog converters (DACs): one for each motor phase. This sets the regulated current (I) according to the value in the TSTP register and a fixed sine/cosine function, calculated with Equation (1):

$$I = \%I_{REG} \times I_{PEAK} \quad (1)$$

Where $\%I_{REG}$ is the percentage of I_{PEAK}. See Appendix 1 on page 31 for more details regarding the $\%I_{REG}$ values for each value in the TSTP register.

Automatic Hold Current

The current required in the windings of a stepper motor is dependent on the load torque applied to the motor. When the motor is stopped, the current can be reduced, which saves energy and reduces power dissipation. The automatic hold current circuitry automatically reduces the winding current when a full current is not required.

If automatic holding is enabled and there are no edges on the STEP input (or register) for a set time, the winding current changes to the I_{PEAK} value set by the IL5~IL0 register bits, which is scaled by the $\%I_{REG}$ value for the current step.

As soon as activity resumes on the STEP input, the current immediately increases to the I_{PEAK} current set by the IS5~IS0 bits, which is scaled by the $\%I_{REG}$ value of the current step.

The automatic hold function is controlled by the AH2~AH0 bits in the CTRL register. These bits set the amount of time that can pass without STEP activity until the automatic hold current function is activated. If the AH2~AH0 bits are set to 0, the automatic hold function is disabled (see Table 5).

Note that when automatic holding is activated, the stall detect counter is also reset (see the Stall Detection section on page 19 for more details).

Table 5: AH2~AH0 Bits

AH2~AH0	Automatic Hold Time	Min. Steps/Sec
0x00 (reset value)	Disabled	-
0x01	15.6ms	64
0x02	31.3ms	32
0x03	62.5ms	16
0x04	125ms	8
0x05	250ms	4
0x06	500ms	2
0x07	1000ms	1

Figure 5 shows the current control circuitry.

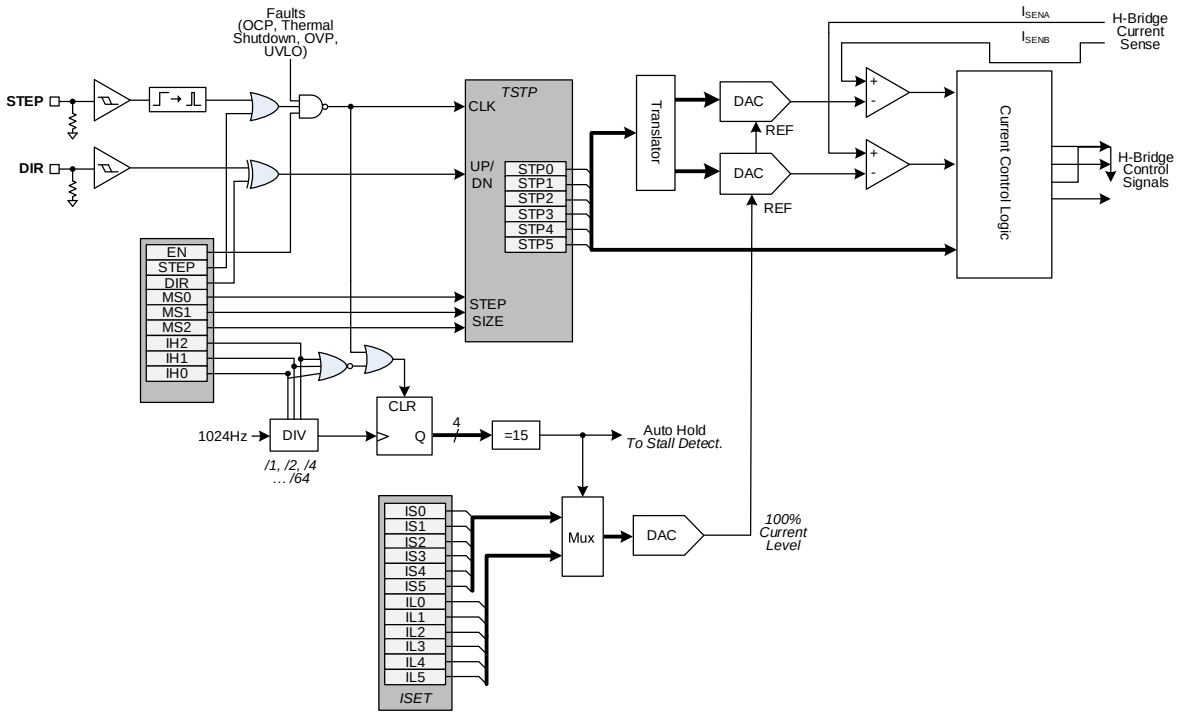


Figure 5: Current Control Circuitry

Diagnostic and Protection Functions

Fault Pin (nFAULT)

The nFAULT pin reports fault conditions. This pin is an open-drain output, and it is driven low when a fault condition occurs. If the fault condition is released, the nFAULT pin is pulled high by an external pull-up resistor.

The source of the fault can be determined by reading the FAULT and OCP registers via the SPI interface.

Over-Current Protection (OCP)

If the current though a MOSFET exceeds the over-current (OC) limit threshold, and lasts for longer than the OC deglitch time, an OCP event is detected. All MOSFETs in both H-bridges are disabled. The appropriate OCPxx bits in the OCP register are set, the OCP bit in the FAULT register is set, and the nFAULT pin is driven low.

The device stays in this state until the fault is cleared by writing a 1 to the OCPxx bit(s) that are set in the OCP register. This also clears the OCP bit in the FAULT register.

OC conditions are detected independently on both the HS-FETs and LS-FETs. OC conditions that result in an OC shutdown include the following: excessive current from an output to ground, supply, or to another output.

The bits in the OCP register can be read to determine if the fault was detected in an HS-FET or LS-FET, as well as whether the OC condition is on the A or B H-bridge.

Over-Voltage Protection (OVP)

If the input voltage on the VIN pin (V_{IN}) exceeds the over-voltage protection (OVP) threshold, the H-bridge outputs are disabled, the OVP bit in the FAULT register is set, and the nFAULT pin is driven low. This protection is released when V_{IN} drops below the OVP threshold, and the H-bridges are automatically re-enabled. Meanwhile, the bits remain set, and nFAULT is driven low. To clear the fault, write a 1 to the OVP bit.

V_{CC} and V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the under-voltage lockout (UVLO) threshold voltage, the H-bridge outputs are disabled, the VINUV and FLT bits in the FAULT register are set, and the nFAULT pin is driven low. When V_{IN} rises above the UVLO threshold, the H-bridges are automatically re-enabled. The nFAULT pin stays driven low, and the VINUV and FAULT bits remain set, until a 1 is written to the VINUV bit.

Note that if V_{IN} is applied after or at the same time as the VCC voltage (V_{CC}), the VINUV bit may be set at start-up, and the nFAULT pin may be driven active low for a short time.

If V_{CC} falls below its UV limit, the device is disabled and all registers are reset. When V_{CC} exceeds its UV threshold, the device is in the reset state. Meanwhile, the VCCUV register bit is set, and it remains set until a 1 is written to it. The nFAULT pin is not driven active low, and the global FLT bit is not set.

VCCUV is also set if the device is reset via the nRESET pin.

Thermal Warning

If the die temperature exceeds the thermal warning threshold, the OTW and FLT bits in the FAULT register are set, and the nFAULT pin is driven active low. In this scenario, the device remains fully operational. The bits remain set and nFAULT is driven low until the fault is cleared by writing a 1 to the OTW bit.

Thermal Shutdown

If the die temperature exceeds the safe limits, all of the MOSFETs in the H-bridge are disabled, the OTS and FLT bits are set, and the nFAULT pin is driven low. The device is disabled until a 1 is written to the TSD bit.

Open Load Detection

If enabled, the MP6602 can detect an open load condition on the outputs. An open load is only sensed when xOUT2 is driven high and xOUT1 is grounded.

If the winding current does not reach the configured I_{TRIP} threshold within 1ms, the xOUT1 output turns off and is pulled to ground by a resistance (about 20kΩ).

If an inductive load is present, the winding current freewheels and passes through the HS body diodes, so the xOUT1 pin is driven high. If no load is connected (e.g. if the motor winding was open), the output is pulled low by the resistance to ground. If the xOUT1 pin goes low, an open load error is detected.

Open load detection is operational in most situations, but it is subject to the following limitations:

- Due to the 1ms timer, open load detection does not work if the step rate exceeds 1000PPS.
- If the current takes longer than 1ms to reach I_{TRIP} in full-step mode, a false open load condition is detected. In this scenario, open load detection can be disabled.

If an open load is detected, the OLA (or OLB bit) and FLT bits in the FAULT register are set, and the nFAULT pin is driven active low. In this scenario, the device remains fully operational. The bits remain set, and nFAULT stays driven low, until the fault is cleared by writing a 1 to the set OLA or OLB bit.

Open load detection can be disabled by setting the OLDIS bit to 1.

Stall Detection

Stall detection works by sensing the back EMF (BEMF) of each phase when there is no current being driven through the winding. The differential voltage between the xOUT1 and xOUT2 pins is sampled before current is driven though the winding again.

Refer to application note AN189 on the MPS website for more details regarding how to configure stall detection.

Stall detection is disabled in unipolar mode.

The BEMF voltage is representative of the motor's BEMF, which is a function of the motor speed and the applied torque. When the motor is stalled, there is no BEMF, so the sampled voltage is almost equal to zero.

Note that since stall detection relies on measuring BEMF at a zero-current step, stall detection does not work in full-step mode. It also may not work at very slow step rates, since there is not enough BEMF to reliably detect a stall.

The BEMF voltage is sampled and digitized. If the BEMFSEL bit is set to 1, the real-time value from the ADC is used for stall detection. If this bit is set to 0, an average of the last 16 readings is used. This value is compared to a configurable threshold. If the BEMF is below the configured threshold for a configurable number of steps, a stall is reported.

The moment at which the BEMF is sampled can be configured via the CTRL2 register (see Table 6).

Table 6: Back EMF Sample Point

BES2~BES0	Back EMF Sample Point
0x00	100µs after zero current
0x01	200µs after zero current
0x02	400µs after zero current
0x03 (reset value)	End of zero current

The BEMF measurement can also be read directly in the BEMF register. A processor can use this information to implement advanced diagnostic and control features.

The STALL and BEMF registers contain several settings that relate to stall detection. To properly implement stall detection, these settings must be set correctly for the application and motor characteristics.

The BEG bits in the BEMF register set the gain or attenuation of the BEMF measurement. The full-scale input level applied to the ADC is 5V.

The BEG bits are set such that the ADC can accurately measure the BEMF at the point where stall detection is required. This BEMF level, which is always below the supply voltage, depends on motor construction and speed (see Table 7).

Table 7: BEMF Gain

BEG2~BEG0	Back EMF Gain	Full-Scale BEMF
0x00	0.1	50V
0x01	0.2	25V
0x02	0.5	10V
0x03 (reset value)	1	5V
0x04	2	2.5V
0x05	5	1V
0x06	10	500mV
0x07	20	250mV

The STH register bits in the STALL register set the BEMF threshold. If the BEMF is below this threshold, the stall counter is incremented; if BEMF exceeds this threshold, the counter is decremented. This is a percentage of the maximum BEMF (see Table 8).

Table 8: STH Register Bits

STH7~STH0	% of Max BEMF Voltage
0x00	No stall detected
0x01	0.4%
0x02	0.8%
…	…
0x7F	49.8%
0x80 (reset value)	50.2%
0x81	50.6%
…	…
0xFE	99.6%
0xFF	100%

The STD bits in the STALL register set the count that the stall counter must reach to report a stall condition (see Table 9 on page 20).

Table 9: Steps to Report a Stall

STD3~STD0	Steps Required to Report Stall
0x00 (reset value)	Stall detect disabled
0x01	1
0x02	2
…	…
0x0D	13
0x0E	14
0x0F	15

If the stall counter reaches the count set via the STD3~STD0 bits, a stall condition is reported.

The STALL and FLT bits in the FAULT register are set, and the nFAULT pin is driven active low. In this scenario, the device remains fully operational.

The bits remain set, and nFAULT is driven low. The fault is cleared by writing a 1 to the STALL bit.

Note that if automatic hold mode is activated, the stall detect counter is always 0.

Figure 6 shows the back EMF measurement and stall detection circuitry

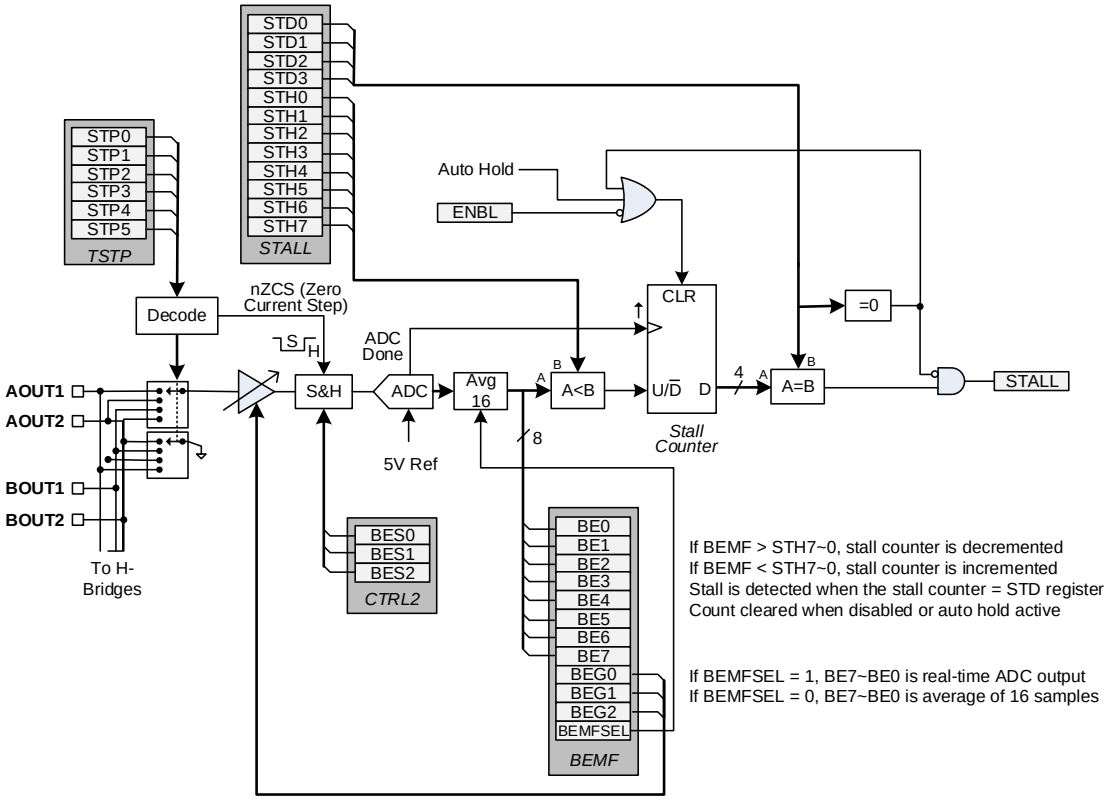


Figure 6: Back EMF Measurement and Stall Detection Circuitry

Serial Peripheral Interface (SPI) Control

The SPI uses a standard, 16-bit serial data packet, which is composed of 3 address bits, one read/write (R/W) bit, and 12 data bits. Serial data is clocked in to the SDATI pin by the rising edges on the SCLK pin, while the nSCS pin is held active low.

The first 3 bits sent are the address bits, which address one of eight registers inside the MP6602. The address bits select both the source of data to be shifted out the SDATO pin, as well as the destination of the new data being shifted in.

The fourth bit is a read/write bit. If clear, the sent data is ignored, and the register data is read out on the SDATO pin. If set, the next 12 bits sent are latched into the selected register at the end of the transfer.

The addressed register is updated on the rising edge of the nSCS input.

Figure 7 shows the SPI logic.

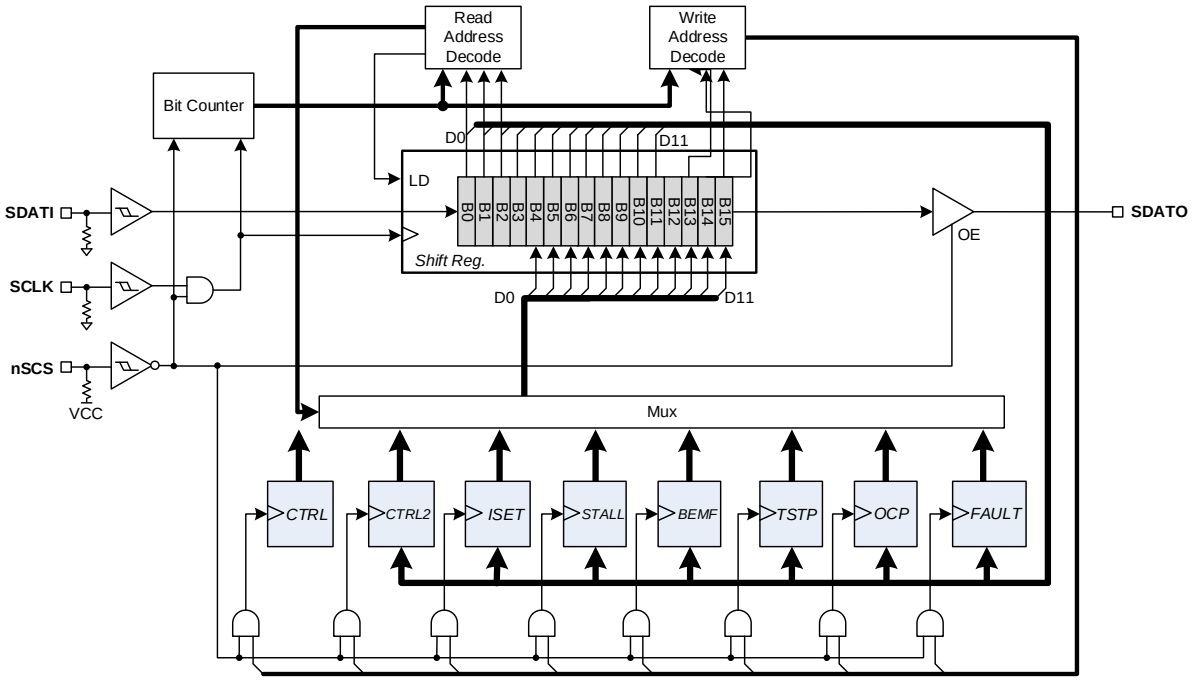


Figure 7: SPI Logic

Figure 8 shows how SPI data transfers are performed.

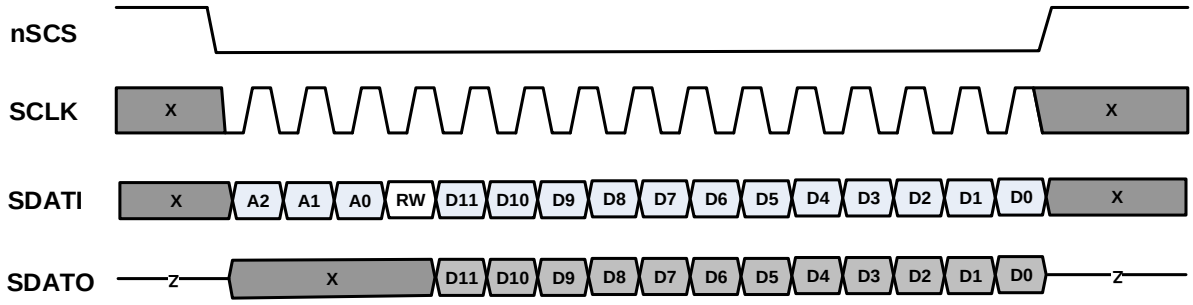


Figure 8: SPI Data Transfers

DIAGNOSTIC AND FAULT SUMMARY TABLE

Fault	Device Action	Bits Set	How to Clear Bits	nFAULT Active?
Over-current (OC)	Outputs latched off, stepping disabled	OCPxx, OCP, FLT	Write 1 to OCP (OCPxx cleared)	Yes, until OCP is cleared
V_{IN} over-voltage (OV)	Outputs and stepping disabled until V_{IN} < OVP threshold	OVP, FLT	Write 1 to OVP	Yes, until OVP is cleared
V_{IN} under-voltage (UV)	Outputs and stepping disabled until V_{IN} > UVLO threshold	VINUV, FLT	Write 1 to VINUV	Yes, until VINUV is cleared
V_{CC} UV (7)	Device reset	VCCUV	Write 1 to VCCUV	Never
Thermal Warning	None	OTW, FLT	Write 1 to OTW	Yes, until OTW is cleared
Thermal shutdown	Outputs latched off, stepping disabled	OTS, FLT	Write 1 to OTS	Yes, until OTS is cleared
Open load	None	OL,FLT	Write 1 to OLx	Yes, until OLx is cleared
Stall	None	STALL, FLT	Write 1 to STALL	Yes, until STALL is cleared

Notes:

7) The VCCUV bit is set whenever the device is reset (V_{CC} start-up or by the nRESET pin).

REGISTER DESCRIPTION

CTRL Register

Address: 0x00 read, 0x01 write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	AH2	0	Sets the automatic hold timer.
D10	R/W	AH1	0	
D9	R/W	AH0	0	
D8	R/W	OT2	1	Sets the fixed off time.
D7	R/W	OT1	0	
D6	R/W	OT0	0	
D5	R/W	MS2	0	Sets the step mode.
D4	R/W	MS1	1	
D3	R/W	MS0	1	
D2	R/W	DIR	0	When this bit is written to 1, the indexer is increments by one step. This bit is automatically reset to 0.
D1	R/W	STEP	0	This bit works with the DIR input pin to set the step direction.
D0	R/W	EN	0	This bit works with the ENBL input pin to enable the motor drive outputs.

CTRL2 Register

Address: 0x02 read, 0x03 write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	RSV3	-	Reserved bits. Must be written to 0.
D10	R/W	RSV2	-	
D9	R/W	RSV1	-	
D8	R/W	RSV0	-	
D7	R	RESERVED	-	Read-only.
D6	R/W	OLDIS	0	Write 1 to this bit to disable open load detection.
D5	R/W	BES1	1	Sets the back EMF sample point time.
D4	R/W	BES0	1	
D3	R/W	UNI	0	Write 1 to this bit to set the device to unipolar mode.
D2	R/W	BT2	1	Sets the blanking time.
D1	R/W	BT1	0	
D0	R/W	BT0	0	

ISET Register

Address: 0x04 read, 0x05 write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	IL5	0	Sets the peak (100%) current level during automatic hold mode.
D10	R/W	IL4	0	
D9	R/W	IL3	1	
D8	R/W	IL2	0	
D7	R/W	IL1	0	
D6	R/W	IL0	1	
D5	R/W	IS5	0	Sets the peak (100%) current level during stepping.
D4	R/W	IS4	0	
D3	R/W	IS3	1	
D2	R/W	IS2	0	
D1	R/W	IS1	0	
D0	R/W	IS0	1	

STALL Register

Address: 0x06 read, 0x07 write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	STH7	1	Sets the stall detection back EMF threshold.
D10	R/W	STH6	0	
D9	R/W	STH5	0	
D8	R/W	STH4	0	
D7	R/W	STH3	0	
D6	R/W	STH2	0	
D5	R/W	STH1	0	
D4	R/W	STH0	0	
D3	R/W	STD3	0	Sets the number of cycles required to detect a stall. 0: Stall detection disabled 1: Stall detection enabled
D2	R/W	STD2	0	
D1	R/W	STD1	0	
D0	R/W	STD0	0	

BEMF Register

Address = 0x08 read, 0x09 write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	BEMFSEL	0	0: The average of 16 samples 1: BE7~BE0 provides the real-time BEMF data
D10	R/W	BEG2	0	Sets the gain for the back EMF measurement.
D9	R/W	BEG1	1	
D8	R/W	BEG0	1	
D7	R	BE7	-	Returns the measured value of the BEMF at the last zero current step.
D6	R	BE6	-	
D5	R	BE5	-	
D4	R	BE4	-	
D3	R	BE3	-	
D2	R	BE2	-	
D1	R	BE1	-	
D0	R	BE0	-	

TSTP Register

Address: 0x0A read, 0x0B write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	RSVD	0	Reserved bits.
D10	R/W	RSVD	1	
D9	R/W	RSVD	0	
D8	R/W	RSVD	1	
D7	R/W	RSVD	0	
D6	R/W	STP6	0	Sets the current position for the indexer’s step table.
D5	R/W	STP5	0	
D4	R/W	STP4	1	
D3	R/W	STP3	0	
D2	R/W	STP2	0	
D1	R/W	STP1	0	
D0	R/W	STP0	0	

OCP Register

Address: 0x0C read, 0x0D write

Bits	R/W	Bit Name	Reset Value	Description
D11	R/W	RSVD	0	Reserved bits.
D10	R/W	RSVD	1	
D9	R/W	RSVD	0	
D8	R/W	RSVD	1	
D7	R/W	RSVD	0	
D6	R/W	RSVD	1	
D5	R/W	RSVD	0	
D4	R/W	RSVD	1	
D3	R/W	OCPAH	0	This bit is set if bridge A experiences a high-side OCP event (such as a short to ground).
D2	R/W	OCPAL	0	This bit is set if bridge A experiences a low-side OCP event (such as a short to VIN).
D1	R/W	OCPBH	0	This bit is set if bridge B experiences a high-side OCP event (such as a short to ground).
D0	R/W	OCPBL	0	This bit is set if bridge B experiences a low-side OCP event (such as a short to VIN).

FAULT Register

Address = 0x0E read, 0x0F write

Bits	R/W	Bit Name	Reset Value	Description
D11	-	RESERVED	-	Read-only.
D10	-	RESERVED	-	Read-only.
D9	R/W	STALL	0	This bit is set if a rotor stall is detected.
D8	R/W	OLA	0	This bit is set if an open load is detected on bridge A.
D7	R/W	OLB	0	This bit is set if an open load is detected on bridge B.
D6	R	OCP	0	This bit is the logical OR of the bits in the OCP register. Read-only.
D5	R/W	OTS	-	This bit is set if over-temperature (OT) shutdown occurs.
D4	R/W	OTW	-	This bit is set if the temperature exceeds the OT warning temperature.
D3	R/W	OVP	-	This bit is set if over-voltage protection (OVP) is activated.
D2	R/W	VINUV	0 (8)	This bit is set if V_{IN} falls below its under-voltage (UV) threshold.
D1	R/W	VCCUV	1	This bit is set if V_{CC} falls below its UV threshold. Set at start-up and reset condition.
D0	R	FLT	-	This bit is the logical OR of the other bits in the FAULT register except VCCUV and VINUV. FLT also reflects the state of the nFAULT pin's output. Read-only.

Note:

8) Depending on the start-up sequence, the VINUV bit may be set at start-up.

APPLICATION INFORMATION

Selecting the External Components

The MP6602 requires several capacitors for proper operation (see Table 11).

Table 11: Capacitor Selection

Component	Connection	Value	Comment
VG capacitor	Pin 11 to GND	1µF, 16V, X7R	Minimum value
VCP capacitor	Pin 12 to VIN	1µF, 16V, X7R	Minimum value
VCC bypass	Pin 21 to GND	100nF, 16V, X7R	Minimum value
VIN bypass capacitor 1	Pin 3 to pin 1 or 5 (to PGND)	1µF, 50V, X7R + 10µF, 50V	100nF minimum. Rated for V_{IN} at minimum. Additional bulk capacitors may be required. A 100µF electrolytic capacitor is recommended.
VIN bypass capacitor 2	Pin 15 to 13 or 17 (to PGND)	1µF, 50V, X7R + 10µF, 50V	

Unipolar Motor Operation

Although the MP6602 supports unipolar motor operation, the performance for unipolar motors is limited due to the structure of the output stage.

Many unipolar motors can be connected as bipolar motors by simply not connecting the center tap. This is the best option in terms of performance, but it requires that the V_{IN} supply to be at least 2 times the rated voltage of the motor to deliver the rated current.

When driving a unipolar motor that is rated at the same voltage as the V_{IN} supply, set the ISET register to a value slightly greater than the rated winding current. This will allow 100% duty cycle operation.

Note that many unipolar motors do not work well in step modes finer than a quarter-step.

PCB Layout Guidelines

The MP6602 relies on thermal conduction to dissipate power. A multi-layer PCB with a solid ground plane provides the best power dissipation and the lowest operating temperature.

On a well-designed 4-layer PCB, the temperature rise when driving 4A of motor current is about 26°C above the ambient temperature (T_A). Figure 9 shows a thermal image at 4A, 24V, 1/8-step operation.

Figure 9: Thermal Results

Figure 10 the shows the measured temperature rise vs. motor current under the same conditions (4A, 24V, 1/8-step operation).

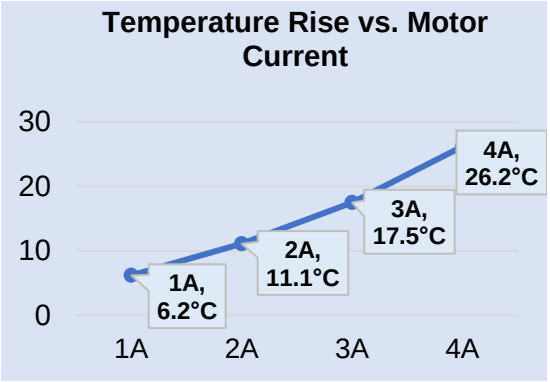
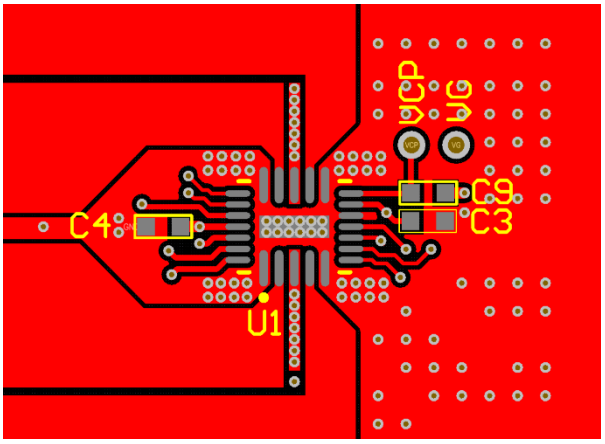


Figure 10: Measured Temperature Rise vs. Motor Current

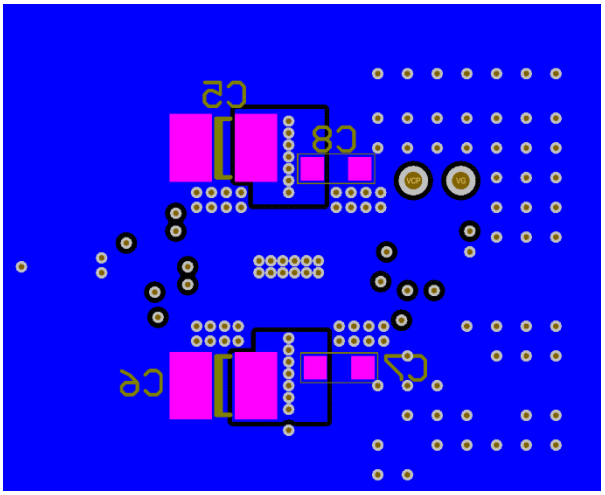
This PCB design has considerably lower thermal resistance that the JESD51-7 standard PCB. The standard PCB has only three thermal vias, and has a thermal resistance (θ_{JA}) of 29.6°C/W. This EVB design has 12 vias and a θ_{JA} of 18.5°C/W.

For the best results, refer to Figure 11 and follow the guidelines below:

1. Place multiple vias in the exposed pad to extract heat and move it to the environment.
2. To remove heat from the device, add additional copper areas on the outer layer connected to the VIN pins.
3. Place bypass capacitors directly adjacent to the supply pins.
4. Place the VIN bypass capacitors on the back side of the PCB.
5. Use multiple vias to connect the VIN and PGND pins of the device.
6. Connect PGND, AGND, and the exposed pad together under the device.



Top Layer



Bottom Layer

Figure 11: Recommended PCB Layout

The top layer is vital because it removes heat from the device. Note that many vias are used (especially on ground) to move heat from the top layer to an internal plane.

Figure 11 on page 28 uses a solid ground plane and an inner layer to route the power and signals. The bottom layer is mostly ground, while the VIN bypass capacitors are mounted on the back side.

TYPICAL APPLICATION CIRCUIT

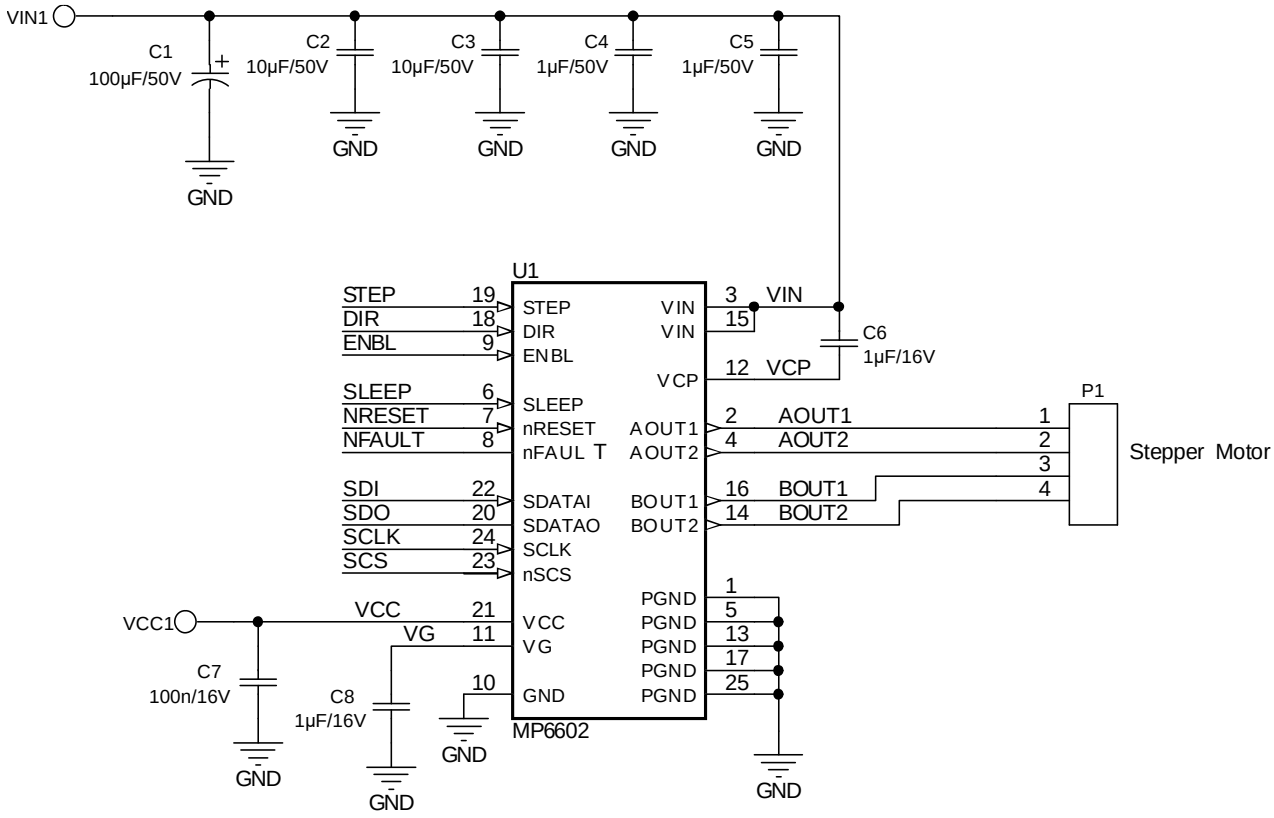


Figure 12: Typical Application Circuit

APPENDIX 1: RELATIVE CURRENT LEVEL SEQUENCE

1/32-Step #	1/16-Step #	1/8-Step #	Quarter-Step #	Half-Step #	Full Step #	Phase A Current (% of I_{PEAK})	Phase B Current (% of I_{PEAK})	Step Angle (°)	TSTP Register Value
1	1	1	1	1	-	100.00	0.00	0.0	0x00
2		-	-	-	-	99.88	4.91	2.8	0x01
3	2	-	-	-	-	99.52	9.80	5.6	0x02
4		-	-	-	-	98.92	14.67	8.4	0x03
5	3	2	-	-	-	98.08	19.51	11.3	0x04
6		-	-	-	-	97.00	24.30	14.1	0x05
7	4	-	-	-	-	95.69	29.03	16.9	0x06
8		-	-	-	-	94.15	33.69	19.7	0x07
9	5	3	2	-	-	92.39	38.27	22.5	0x08
10		-	-	-	-	90.40	42.76	25.3	0x09
11	6	-	-	-	-	88.19	47.14	28.1	0x0A
12		-	-	-	-	85.77	51.41	30.9	0x0B
13	7	4	-	-	-	83.15	55.56	33.8	0x0C
14		-	-	-	-	80.32	59.57	36.6	0x0D
15	8	-	-	-	-	77.30	63.44	39.4	0x0E
16		-	-	-	-	74.10	67.16	42.2	0x0F
17	9	5	3	2	1	70.71	70.71	45.0	0x10 (9)
18		-	-	-	-	67.16	74.10	47.8	0x11
19	10	-	-	-	-	63.44	77.30	50.6	0x12
20		-	-	-	-	59.57	80.32	53.4	0x13
21	11	6	-	-	-	55.56	83.15	56.3	0x14
22		-	-	-	-	51.41	85.77	59.1	0x15
23	12	-	-	-	-	47.14	88.19	61.9	0x16
24		-	-	-	-	42.76	90.40	64.7	0x17
25	13	7	4	-	-	38.27	92.39	67.5	0x18
26		-	-	-	-	33.69	94.15	70.3	0x19
27	14	-	-	-	-	29.03	95.69	73.1	0x1A
28		-	-	-	-	24.30	97.00	75.9	0x1B
29	15	8	-	-	-	19.51	98.08	78.8	0x1C
30		-	-	-	-	14.67	98.92	81.6	0x1D
31	16	-	-	-	-	9.80	99.52	84.4	0x1E
32		-	-	-	-	4.91	99.88	87.2	0x1F
33	17	9	5	3	-	0.00	100.00	90.0	0x20
34		-	-	-	-	-4.91	+99.88	92.8	0x21
35	18	-	-	-	-	-9.80	+99.52	95.6	0x22
36		-	-	-	-	-14.67	+98.92	98.4	0x23
37	19	10	-	-	-	-19.51	+98.08	101.3	0x24
38		-	-	-	-	-24.30	+97.00	104.1	0x25
39	20	-	-	-	-	-29.03	+95.69	106.9	0x26
40		-	-	-	-	-33.69	+94.15	109.7	0x27
41	21	11	6	-	-	-38.27	+92.39	112.5	0x28
42		-	-	-	-	-42.76	+90.40	115.3	0x29
43	22	-	-	-	-	-47.14	+88.19	118.1	0x2A
44		-	-	-	-	-51.41	+85.77	120.9	0x2B
45	23	12	-	-	-	-55.56	+83.15	123.8	0x2C
46		-	-	-	-	-59.57	+80.32	126.6	0x2D
47	24	-	-	-	-	-63.44	+77.30	129.4	0x2E
48		-	-	-	-	-67.16	+74.10	132.2	0x2F
49	25	13	7	4	2	-70.71	+70.71	135.0	0x30

50	-	-	-	-	-	-74.10	+67.16	137.8	0x31
51	26	-	-	-	-	-77.30	+63.44	140.6	0x32
52	-	-	-	-	-	-80.32	+59.57	143.4	0x33
53	27	14	-	-	-	-83.15	+55.56	146.3	0x34
54	-	-	-	-	-	-85.77	+51.41	149.1	0x35
55	28	-	-	-	-	-88.19	+47.14	151.9	0x36
56	-	-	-	-	-	-90.40	+42.76	154.7	0x37
57	29	15	8	-	-	-92.39	+38.27	157.5	0x38
58	-	-	-	-	-	-94.15	+33.69	160.3	0x39
59	30	-	-	-	-	-95.69	+29.03	163.1	0x3A
60	-	-	-	-	-	-97.00	+24.30	165.9	0x3B
61	31	16	-	-	-	-98.08	+19.51	168.8	0x3C
62	-	-	-	-	-	-98.92	+14.67	171.6	0x3D
63	32	-	-	-	-	-99.52	+9.80	174.4	0x3E
64	-	-	-	-	-	-99.88	+4.91	177.2	0x3F
65	33	17	9	5	-	-100.00	0.00	180.0	0x40
66	-	-	-	-	-	-99.88	-4.91	182.8	0x41
67	34	-	-	-	-	-99.52	-9.80	185.6	0x42
68	-	-	-	-	-	-98.92	-14.67	188.4	0x43
69	35	18	-	-	-	-98.08	-19.51	191.3	0x44
70	-	-	-	-	-	-97.00	-24.30	194.1	0x45
71	36	-	-	-	-	-95.69	-29.03	196.9	0x46
72	-	-	-	-	-	-94.15	-33.69	199.7	0x47
73	37	19	10	-	-	-92.39	-38.27	202.5	0x48
74	-	-	-	-	-	-90.40	-42.76	205.3	0x49
75	38	-	-	-	-	-88.19	-47.14	208.1	0x4A
76	-	-	-	-	-	-85.77	-51.41	210.9	0x4B
77	39	20	-	-	-	-83.15	-55.56	213.8	0x4C
78	-	-	-	-	-	-80.32	-59.57	216.6	0x4D
79	40	-	-	-	-	-77.30	-63.44	219.4	0x4E
80	-	-	-	-	-	-74.10	-67.16	222.2	0x4F
81	41	21	11	6	3	-70.71	-70.71	225.0	0x50
82	-	-	-	-	-	-67.16	-74.10	227.8	0x51
83	42	-	-	-	-	-63.44	-77.30	230.6	0x52
84	-	-	-	-	-	-59.57	-80.32	233.4	0x53
85	43	22	-	-	-	-55.56	-83.15	236.3	0x54
86	-	-	-	-	-	-51.41	-85.77	239.1	0x55
87	44	-	-	-	-	-47.14	-88.19	241.9	0x56
88	-	-	-	-	-	-42.76	-90.40	244.7	0x57
89	45	23	12	-	-	-38.27	-92.39	247.5	0x58
90	-	-	-	-	-	-33.69	-94.15	250.3	0x59
91	46	-	-	-	-	-29.03	-95.69	253.1	0x5A
92		-	-	-	-	-24.30	-97.00	255.9	0x5B
93	47	24	-	-	-	-19.51	-98.08	258.8	0x5C
94		-	-	-	-	-14.67	-98.92	261.6	0x5D
95	48	-	-	-	-	-9.80	-99.52	264.4	0x5E
96	-	-	-	-	-	-4.91	-99.88	267.2	0x5F
97	49	25	13	7	-	0.00	-100.00	270.0	0x60
98	-	-	-	-	-	+4.91	-99.88	272.8	0x61
99	50	-	-	-	-	+9.80	-99.52	275.6	0x62
100	-	-	-	-	-	+14.67	-98.92	278.4	0x63
101	51	26	-	-	-	+19.51	-98.08	281.3	0x64
102	-	-	-	-	-	+24.30	-97.00	284.1	0x65
103	52	-	-	-	-	+29.03	-95.69	286.9	0x66

104	-	-	-	-	-	+33.69	-94.15	289.7	0x67
105	53	27	14	-	-	+38.27	-92.39	292.5	0x68
106	-	-	-	-	-	+42.76	-90.40	295.3	0x69
107	54	-	-	-	-	+47.14	-88.19	298.1	0x6A
108	-	-	-	-	-	+51.41	-85.77	300.9	0x6B
109	55	28	-	-	-	+55.56	-83.15	303.8	0x6C
110	-	-	-	-	-	+59.57	-80.32	306.6	0x6D
111	56	-	-	-	-	+63.44	-77.30	309.4	0x6E
112	-	-	-	-	-	+67.16	-74.10	312.2	0x6F
113	57	29	15	8	4	+70.71	-70.71	315.0	0x70
114	-	-	-	-	-	+74.10	-67.16	317.8	0x71
115	58	-	-	-	-	+77.30	-63.44	320.6	0x72
116	-	-	-	-	-	+80.32	-59.57	323.4	0x73
117	59	30	-	-	-	+83.15	-55.56	326.3	0x74
118	-	-	-	-	-	+85.77	-51.41	329.1	0x75
119	60	-	-	-	-	+88.19	-47.14	331.9	0x76
120	-	-	-	-	-	+90.40	-42.76	334.7	0x77
121	61	31	16	-	-	+92.39	-38.27	337.5	0x78
122	-	-	-	-	-	+94.15	-33.69	340.3	0x79
123	62	-	-	-	-	+95.69	-29.03	343.1	0x7A
124	-	-	-	-	-	+97.00	-24.30	345.9	0x7B
125	63	32	-	-	-	+98.08	-19.51	348.8	0x7C
126	-	-	-	-	-	+98.92	-14.67	351.6	0x7D
127	64	-	-	-	-	+99.52	-9.80	354.4	0x7E
128	-	-	-	-	-	+99.88	-4.91	357.2	0x7F

Note:

9) This is the initial position at start-up, or when exiting sleep mode.

Figure 13 shows a full-step sequence. Figure 14 on page 34 shows a half-step sequence. Figure 15 on page 34 shows a quarter-step sequence. Figure 16 on page 35 shows an eighth-step sequence. Figure 17 on page 36 shows a 1/16-step sequence. Note that a 1/32-step sequence is not shown due to its complexity.

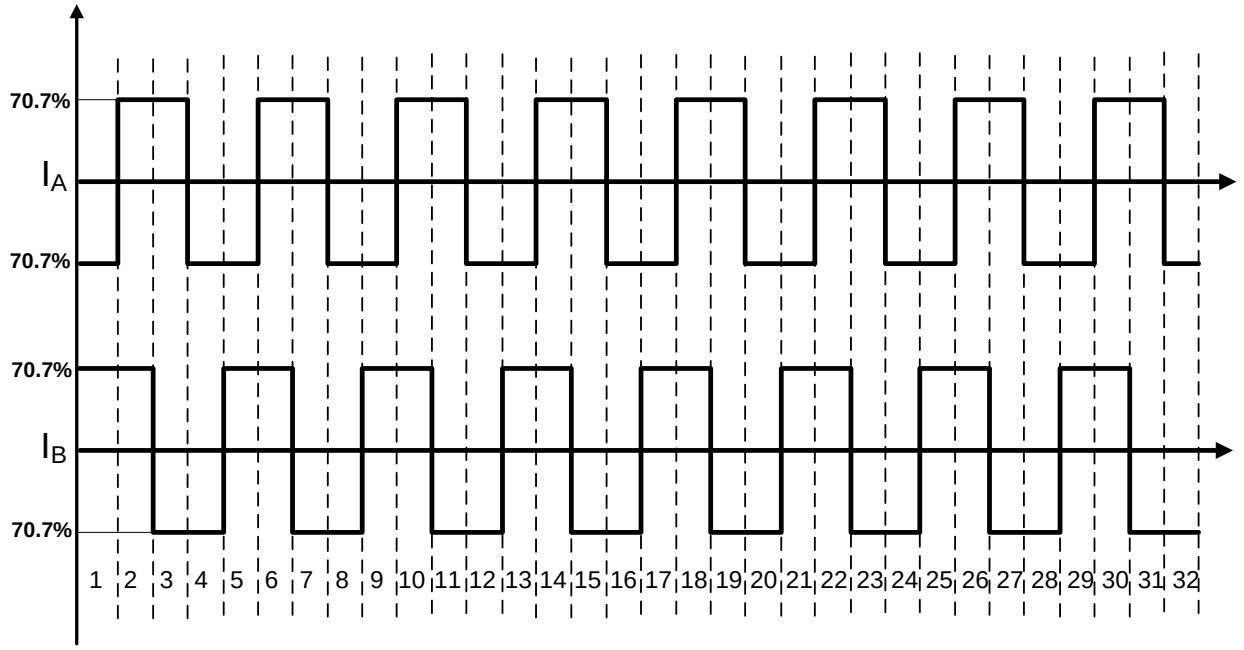


Figure 13: Full Step (4-Step Sequence)

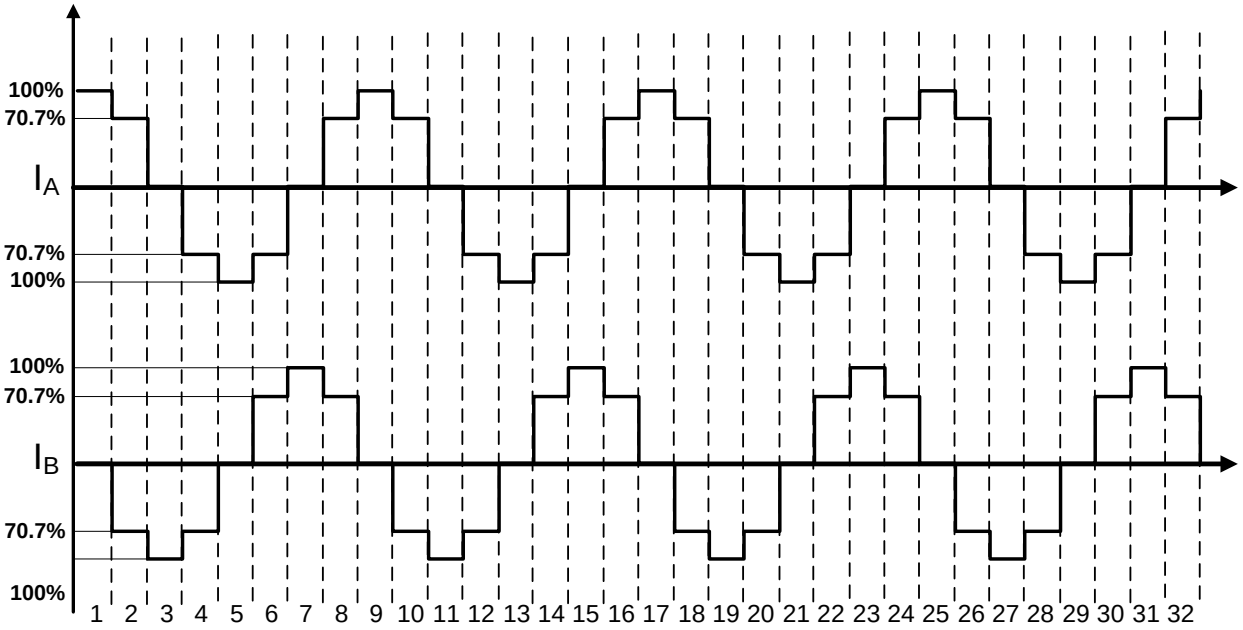


Figure 14: Half-Step (8-Step Sequence)

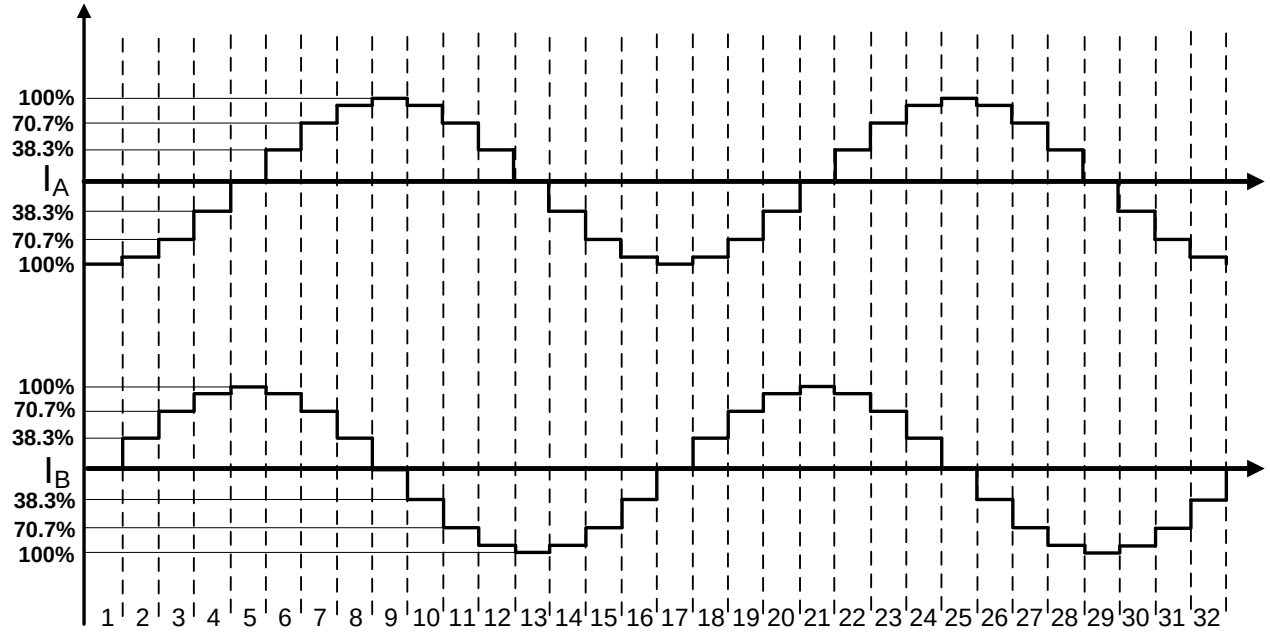


Figure 15: Quarter-Step (16-Step Sequence)

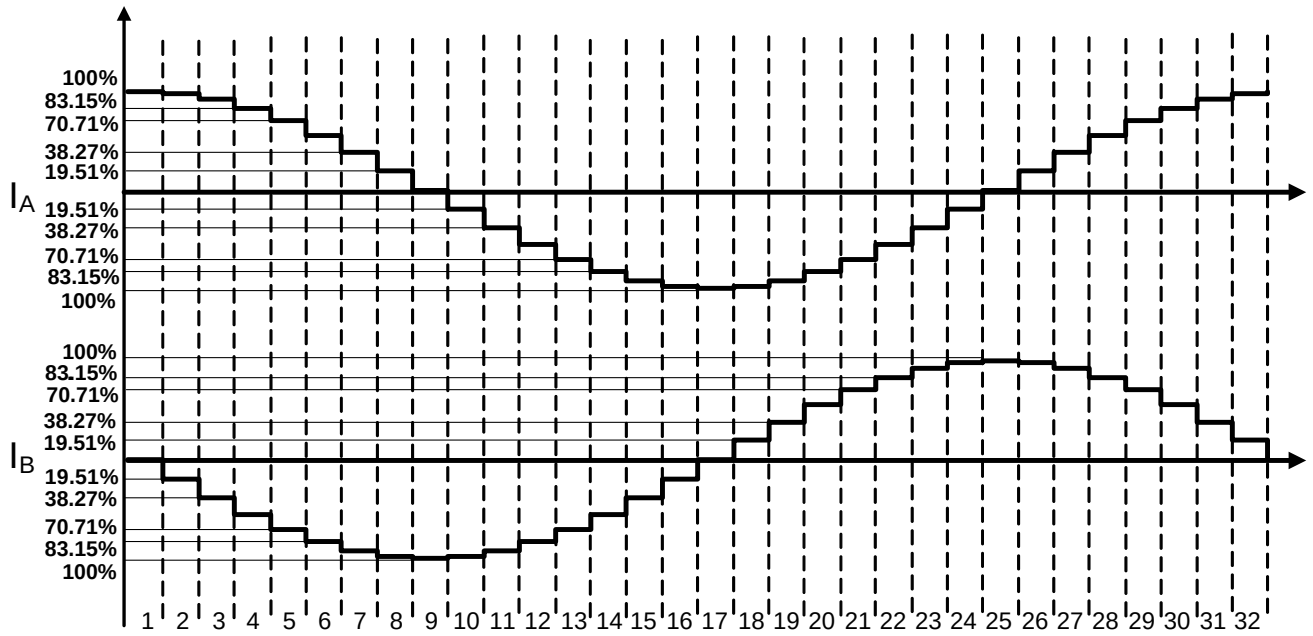


Figure 16: Eighth-Step (32-Step Sequence)

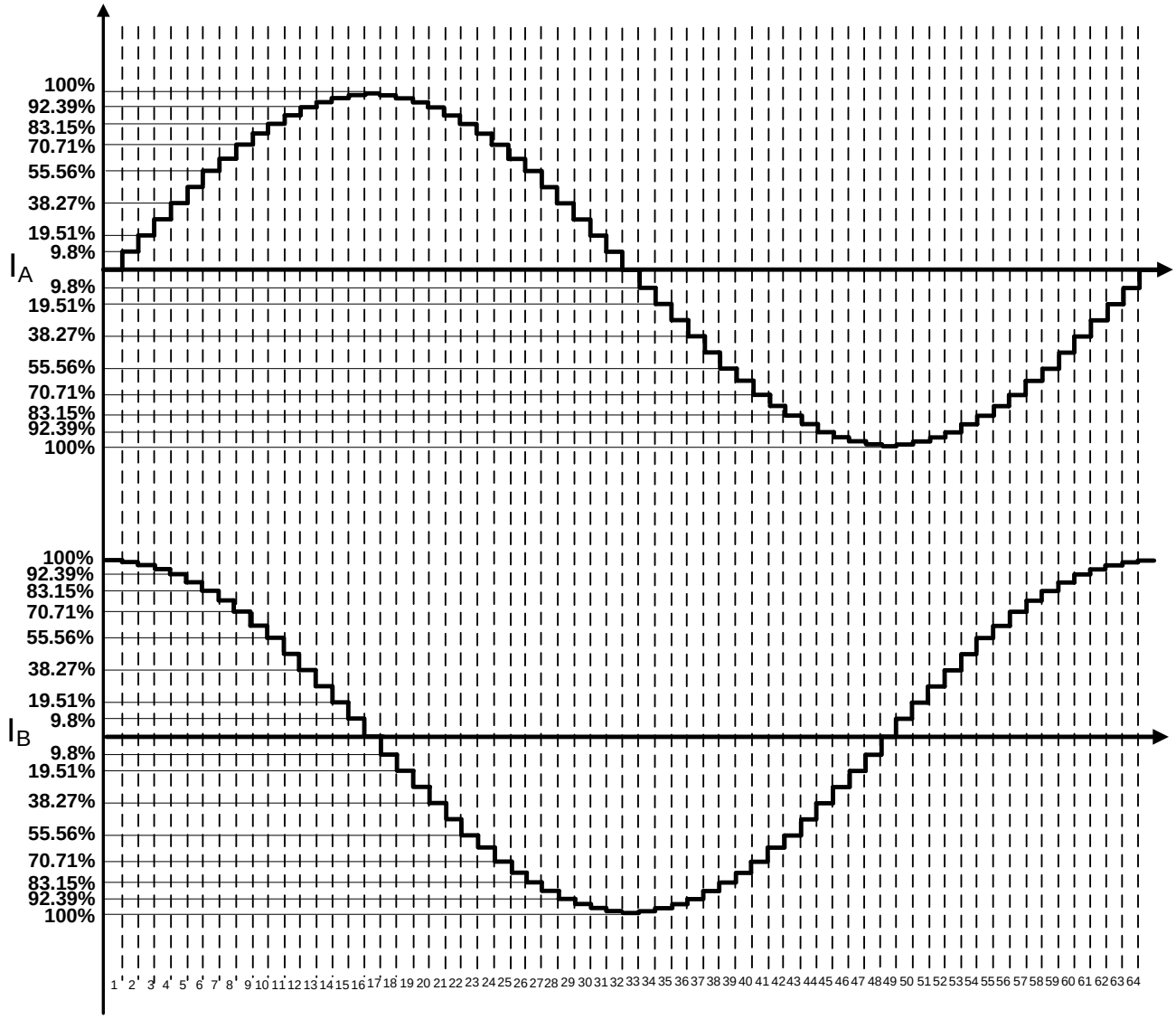
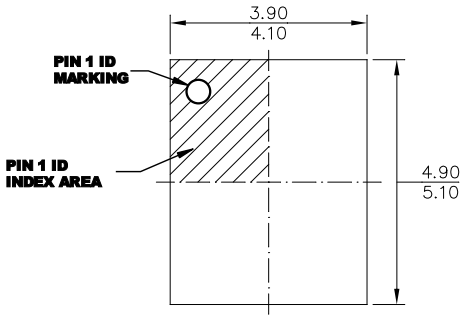


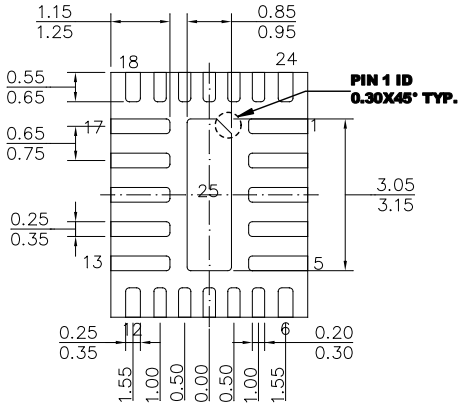
Figure 17: 1/16-Step (64-Step Sequences)

PACKAGE INFORMATION

QFN-25 (4mmx5mm)

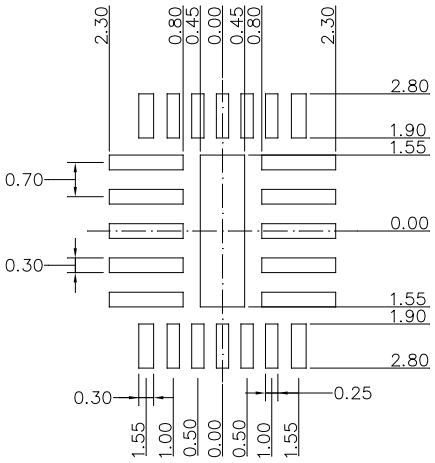


TOP VIEW



BOTTOM VIEW

SIDE VIEW

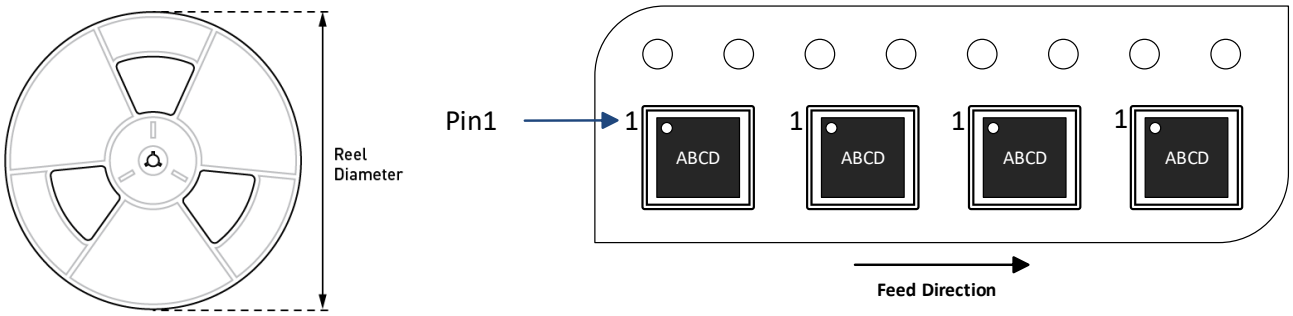


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6602GV-Z	QFN-25 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	X/XX/XXXX	Initial Release	-

Revision #	Revision Date	Description	Pages Updated
1.0	X/XX/XXXX	Initial Release	-