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DRV8462 Stepper Motor Driver with Automatic Microstepping, Silent step Decay Mode and Auto-torque

1 Features

- Stepper Motor Driver
  - SPI or H/W Interface with STEP/DIR pins
  - Up to 1/256 Microstepping Indexer
- 4.5 V to 60 V Operating Supply Voltage Range
- Low ON Resistance: 100 mΩ at 24 V, 25°C
- High Current Capacity Per Bridge:
  - DDW Package: 5A full-scale, 3.5A RMS
  - DDV Package: Up to 10A full-scale, 7A RMS
- Integrated current sensing and regulation
  - ±5% full-scale current accuracy
  - Optional external current sense resistor
- Smart tune, fixed slow, and mixed decay options
- Silent step Decay mode for silent operation at standstill and low speed
- Automatic Microstepping mode for microstep interpolation
- Customizable microstepping indexer table
- Auto-torque for load dependent current control
- Standstill Power Saving mode
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Separate logic supply voltage
- Protection and Diagnostic features
  - Sensorless Stall Detection
  - VM undervoltage lockout (UVLO)
  - Open-load Detection (OL)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)
  - Indexer zero position output (nHOME)

2 Applications

- Textile Machines
- Factory Automation, Stepper Drives and Robotics
- Medical Imaging, Diagnostics and Equipment
- Stage Lighting
- ATMs and Currency Counters
- PLC
- Printers
- 3D Printer
- Outdoor IP Camera
- Aerospace and Defense

3 Description

The DRV8462 is a fully integrated stepper motor driver for industrial applications. The device operates over a 4.5-V to 60-V supply range, and is capable of driving up to 5-A full-scale current with the DDW package; and up to 10-A full-scale current with the DDV package (dependent on PCB design).

The DRV8462 uses an internal current sense architecture to eliminate the need for external sense resistors. External sense resistors can also be connected for implementing closed-loop algorithms. Other than smart tune and mixed decay schemes, the device features a silent step decay mode for silent operation at standstill and low speed. The device can be controlled by SPI or H/W pin interface. The internal indexer supports up to 1/256 microstepping, and automatic microstepping mode allows interpolation of the input step pulses. The auto-torque feature reduces power loss by adjusting the output current as per load torque demand. In addition, the standstill power saving mode reduces power loss during motor holding condition.

A low-power sleep mode ensures ultra-low quiescent current. Internal protection features are provided for supply undervoltage lockout, sensorless stall detection, open-load detection, output overcurrent, and device overtemperature.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DRV8462DDWR	HTSSOP (44), bottom exposed pad	14 mm x 6.1 mm
DRV8462DDVR	HTSSOP (44), top exposed pad	14 mm x 6.1 mm

Figure 3-1. Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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5 Pin Configuration and Functions

Figure 5-1. DDW Package (44-Pin HTSSOP), Top View

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Figure 5-2. DDV Package (44-Pin HTSSOP), Top View

PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
VCP	1	22	Power	Charge pump output. Connect a X7R, 1-µF, 16-V ceramic capacitor to VM.
VM	2, 11, 12, 21	2, 11, 12, 21	Power	Power supply. Connect to motor supply voltage and bypass to PGNDA and PGNDB with two 0.01-µF ceramic capacitors (one for each pair of pins) plus a bulk capacitor rated for VM.
PGNDA	3, 10	13, 20	Power	Power ground. Connect to system ground.
PGNDB	13, 20	3, 10	Power	Power ground. Connect to system ground.
AOUT1	4, 5, 6	17, 18, 19	Output	Winding A output. Connect to motor winding.
AOUT2	7, 8, 9	14, 15, 16	Output	Winding A output. Connect to motor winding.
BOUT2	14, 15, 16	7, 8, 9	Output	Winding B output. Connect to motor winding.
BOUT1	17, 18, 19	4, 5, 6	Output	Winding B output. Connect to motor winding.
GND	22, 23	1, 44	Power	Device ground. Connect to system ground.
DVDD	24	43	Power	Internal LDO output. Connect a X7R, 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCC	25	42	Power	Supply voltage for internal logic blocks. When no separate supply voltage is available, tie the VCC pin to the DVDD output. When configured with SPI interface, the VCC pin also acts as the supply pin for SDO output.

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PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
nFAULT	26	41	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nHOME	27	40	Open Drain	Pulled logic low when indexer is at home position of step table. The nHOME pin outputs one low pulse per 360º electrical rotation (four fullsteps).
MODE	28	39	Input	MODE pin programs the device with either SPI or hardware (H/W) GPIO pin interface.
RSVD	29	38	-	Reserved. Leave unconnected.
RSVD	30	37	-	Reserved. Leave unconnected.
RSVD	31	36	-	Reserved. Leave unconnected.
RSVD	32	35	-	Reserved. Leave unconnected.
VREF	33	34	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
nSCS/M0	34	33	Input	With SPI interface, this pin acts as serial chip select. An active low on this pin enables the serial interface communications. With H/W interface, this pin programs the microstepping mode.
RSVD/TOFF	35	32	Input	This pin is not used with SPI interface. With H/W interface, this pin programs the OFF time for PWM current regulation.
SDO/ DECAY1	36	31	Push-Pull/Input	With SPI interface, this pin acts as serial data output. Data is shifted out on the rising edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SDI/DECAY0	37	30	Input	With SPI interface, this pin acts as serial data input. Data is captured on the falling edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SCLK/M1	38	29	Input	With SPI interface, this pin acts as serial clock input. Serial data is shifted out and captured on thecorresponding rising and falling edge on this pin. With H/W interface, this pin programs the microstepping mode.
STEP	39	28	Input	Step input. STEP active edge can be either rising edge or both rising and falling edge. An active edge causes the indexer to advance one step.
DIR	40	27	Input	Direction input. Logic level sets the direction of stepping.
ENABLE	41	26	Input	Logic low to disable device outputs; logic high to enable. When the device works with H/W interface, the ENABLE pin determines the type of OCP and OTSD response.
nSLEEP	42	25	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. An nSLEEP low pulse clears latched faults.
CPL	43	24	Power	Charge pump switching node. Connect a X7R, 0.1-µF, VM-rated ceramic capacitor from CPH to CPL.
CPH	44	23	Power	
PAD	-	-	-	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	65	V
Charge pump voltage (VCP, CPH)	-0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	-0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
Control pin voltage	–0.3	5.75	V
Reference input pin voltage (VREF)	–0.3	5.75	V
PGNDx to GND voltage	-0.3	1	V
Open drain output current (nFAULT, nHOME)	0	10	mA
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	Corner Pins	±750	
			Other Pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	60	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	500	kHz
I_{FS}	Motor full-scale current with DDW package (xOUTx)	0	5	A
I_{FS}	Motor full-scale current with DDV package (xOUTx)	0	10	A
I_{RMS}	Motor RMS current with DDW package (xOUTx)	0	3.5	A
I_{RMS}	Motor RMS current with DDW package (xOUTx)	0	7	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

over operating free-air temperature range (unless otherwise noted).

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6.4 Thermal Information

THERMAL METRIC		DDW	DDV	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.6	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.0	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.9	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	N/A	°C/W

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load, VCC = External 5V		3	5	mA
		ENABLE = 1, nSLEEP = 1, No motor load, VCC = DVDD		7	9	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	H/W interface, nSLEEP = 1 to output transition		0.8	1.2	ms
		SPI interface, nSLEEP = 1 to SPI ready		200	400	µs
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 60 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 60 V		V_{VM} + 5		V
f_{VCP}	Charge pump switching frequency	V_{VM} > UVLO ; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, MODE, nSCS, SCLK, SDI, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
$I_{IL(nSCS)}$	nSCS logic-low current	nSCS = 0V	8		12	µA
I_{IH}	Input logic-high current	V_{IN} = DVDD			100	µA
$I_{IH(nSCS)}$	nSCS logic-high current	nSCS = DVDD			500	nA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	5mA load, with respect to GND		30	60	Ω
$R_{PU,SDO}$	Internal pull-up resistance	5mA load, with respect to VCC		60	110	Ω

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SDO}	SDO Leakage Current	V_{VM} > 6 V, SDO = VCC and 0V	-1		1	µA
CONTROL OUTPUTS (nFAULT, nHOME)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		-1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -5 A		50	60	mΩ
		T_J = 125 °C, I_O = -5 A		75	90	mΩ
		T_J = 150 °C, I_O = -5 A		85	105	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		50	60	mΩ
		T_J = 125 °C, I_O = 5 A		75	90	mΩ
		T_J = 150 °C, I_O = 5 A		85	105	mΩ
t_{RF}	Output rise/fall time	H/W interface, I_O = 5 A, between 10% and 90%		100		ns
		SPI interface, SR = 0b, I_O = 5 A, between 10% and 90%		100		
		SPI interface, SR = 1b, I_O = 5 A, between 10% and 90%		50		
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns
PWM CURRENT CONTROL (VREF)						
VREF_INT	Internal Reference Voltage	VREF_INT_EN = 1b	3.12	3.3	3.48	V
K_V	Transimpedance gain	VREF = 3.3 V, DDW Package	0.625	0.66	0.695	V/A
		VREF = 3.3 V, DDV Package	0.313	0.33	0.347	
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			0.8	µA
t_{OFF}	PWM off-time	TOFF = 0 or TOFF = 00b		7		µs
		TOFF = 1 or TOFF = 01b		16		
		TOFF = Hi-Z or TOFF = 10b		24		
		TOFF = 330kΩ to GND or TOFF = 11b		32		
ΔI_{TRIP}	Current trip accuracy	10% to 20% full-scale current	-12		12	%
		20% to 40% full-scale current	-6		6	
		40% to 100% full-scale current	-5		5	
$I_{O,CH}$	AOUT and BOUT current matching	100% full-scale current	-2.5		2.5	%
t_{BLK}	Current regulation blanking time			1		µs
PROTECTION CIRCUITS						
VM_{UVLO}	VM UVLO lockout	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.35	4.45	
VCC_{UVLO}	VCC UVLO lockout	VCC connected to external voltage, VCC falling	2.7	2.8	2.9	V
		VCC connected to external voltage, VCC rising	2.8	2.9	3	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RST}	VM UVLO reset	VCC = DVDD, SPI interface, VM falling, device reset, no SPI communications			3.9	V
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET, DDW Package	8			A
		Current through any FET, DDV Package	16			A
t_{OCP}	Overcurrent detection delay	H/W Interface		2		µs
		SPI Interface, TOCP = 0b		1		
		SPI Interface, TOCP = 1b		2		
t_{RETRY}	Overcurrent retry time			4		ms
t_{OL}	Open load detection time	H/W Interface			50	ms
		SPI Interface, OL_T = 00b			25	
		SPI Interface, OL_T = 01b			50	
		SPI Interface, OL_T = 10b			100	
I_{OL}	Open load current threshold			150		mA
T_{OTW}	Overtemperature warning	SPI Interface, Die temperature T_J	135	150	165	°C
T_{HYS_OTW}	Overtemperature warning hysteresis	SPI Interface, Die temperature T_J		20		°C
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.5.1 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(READY)}$	SPI ready, VM > V_{RST}		1		ms
$t_{(CLK)}$	SCLK minimum period	100			ns
$t_{(CLKH)}$	SCLK minimum high time	50			ns
$t_{(CLKL)}$	SCLK minimum low time	50			ns
$t_{su(SDI)}$	SDI input setup time	20			ns
$t_{h(SDI)}$	SDI input hold time	30			ns
$t_{d(SDO)}$	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
$t_{su(nSCS)}$	nSCS input setup time	50			ns
$t_{h(nSCS)}$	nSCS input hold time	50			ns
$t_{(HI_nSCS)}$	nSCS minimum high time before active low			2	µs
$t_{dis(nSCS)}$	nSCS disable time, nSCS high to SDO high impedance		10		ns

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6.5.2 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500[(1)]	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

Figure 6-1. STEP and DIR Timing Diagram

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7 Detailed Description

7.1 Overview

The DRV8462 is an integrated motor-driver solution for bipolar stepper motors. The device provides the maximum integration by integrating two N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and a microstepping indexer. The DRV8462 is capable of supporting wide supply voltage of 4.5 V to 60 V. The device is available in two packages - a 44-pin HTSSOP (DDW) package with exposed pad on the bottom of the package; and another 44-pin HTSSOP (DDV) package with exposed pad on the top of the package. The DDW package provides an output current up to 8-A peak, 5-A full-scale, or 3.5-A root mean square (rms). When a heat sink with low thermal resistance is connected to the top of the DDV package, the DRV8462 can deliver an output current up to 16-A peak, 10-A full-scale, or 7-A root mean square (rms). The DDW package is pin-to-pin compatible with the DRV8452 driver, which is rated for 48 V maximum operating voltage and 5 A full-scale current. The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8462 uses an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. External power sense resistors can also be connected for implementing closed-loop algorithms such as Field Oriented Control. The current regulation set point is adjustedby the voltage at the VREF pin. For the SPI interface, a 6-bit register allows the controller to scale the output current without needing to scale the VREF voltage reference; and another 6-bit register allows configuration of the holding current level for the purpose of reducing power loss at motor standstill.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4,1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. The automatic microstepping mode interpolates the input step frequency to high resolution, thereby improving regulation and audible noise while running with a low frequency step input from the controller. The custom microstepping table allows adjusting the current waveform to a particular motor.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, like slow decay, mixed decay and fast decay. The DRV8462 also comes with smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme. Along with this seamless, effortless automatic smart tune, DRV8462 also provides a silent step decay mode for silent operation at standstill and low speeds of rotation.

The stall detection feature detects and reports to the controller when the motor is obstructed or has reached end-of-line. The auto-torque feature reduces power loss and improves efficiency by adjusting output current according to the load torque. Additionally, the standstill power saving mode reduces power loss when the motor is at holding position.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature minimizes the radiated emissions from the device. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

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7.2 Functional Block Diagram

Figure 7-1. DRV8462 Block Diagram with SPI Interface (MODE = 1)

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7.3 Functional Block Diagram

Figure 7-2. DRV8462 Block Diagram with Hardware Interface (MODE = 0)

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7.4 Feature Description

Table 7-1 lists the recommended external components for the DRV8462.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGNDA	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGNDB	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM3}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 6.3-V ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{nHOME}	DVDD or VCC	nHOME	10-kΩ resistor
R_{REF1}	VREF	DVDD or VCC	Resistor to set chopping current.
R_{REF2}	VREF	GND	

7.4.1 Operation Interface

The DRV8462 can operate with hardware (GPIO) or SPI interface.

The logic-level MODE pin latches the operating interface information at start-up. If the MODE pin is grounded at start-up, the device operates with hardware interface. If the MODE pin is logic high at start-up, the device operates with SPI interface. It is not recommended to change MODE pin logic level on the fly.

The functionality of five pins depend on the interface of operation, as shown below -

Table 7-2. Pin function, DDW package

Pin Number	MODE = 0, H/W interface	MODE = 1, SPI Interface
34	M0	nSCS
35	TOFF	Reserved
36	DECAY1	SDO
37	DECAY0	SDI
38	M1	SCLK

Table 7-3. Pin function, DDV package

Pin Number	MODE = 0, H/W interface	MODE = 1, SPI Interface
29	M1	SCLK
30	DECAY0	SDI
31	DECAY1	SDO
32	TOFF	Reserved
33	M0	nSCS

7.4.2 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

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7.4.2.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8462 in DDW package, the peak current rating is 8 A per bridge. For the DDV package, the peak current rating is 16 A per bridge.

7.4.2.2 RMS Current Rating

The RMS (average) current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8462 in DDW package, the RMS current rating is 3.5 A per bridge. For the DDV package, the RMS current rating is 7 A per bridge.

7.4.2.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

Figure 7-3. Full-Scale and RMS Current

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7.4.3 PWM Motor Drivers

The DRV8462 has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-4 shows the block diagram of the circuitry.

Figure 7-4. PWM Motor Driver Block Diagram

7.4.4 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The MICROSTEP_MODE bits in the SPI register or the M0 and M1 pins are used to configure the step mode as shown in Table 7-4.

Table 7-4. Microstepping Indexer Settings

MODE = 1	MODE = 0		
MICROSTEP_MODE	**M0**	**M1**	**STEP MODE**
0000b	0	0	Full step (2-phase excitation) with 100% current
0001b	0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
0010b	1	0	Non-circular 1/2 step

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Table 7-4. Microstepping Indexer Settings (continued)

MODE = 1	MODE = 0		
MICROSTEP_MODE	M0	M1	STEP MODE
0011b	Hi-Z	0	1/2 step
0100b	0	1	1/4 step
0101b	1	1	1/8 step
0110b	Hi-Z	1	1/16 step
0111b	0	Hi-Z	1/32 step
1000b	Hi-Z	330kΩ to GND	1/64 step
1001b	Hi-Z	Hi-Z	1/128 step
1010b	1	Hi-Z	1/256 step

Table 7-5 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

Depending on the STEP_EDGE bit, STEP active edge can be either rising edge or both rising and falling edge. At each active edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed.

Note

If the step mode is changed dynamically while stepping, the indexer advances to the next valid state for the new step mode setting at the active edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered immediately after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 7-5. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50

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Table 7-5. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-6 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-6. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 7-7 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-7. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

When the device operates with H/W interface and is programmed with silent step decay mode, the M0 and M1 pins also determine the compensation loop response.

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7.4.5 Automatic Microstepping Mode

When the device is operating with SPI interface (MODE = 1), automatic microstepping mode allows interpolating the input step pulses to generate a current waveform corresponding to higher resolution microstep. This results in smooth sinusoidal current for any step frequency. The EN_Autotrq bit must be '1' to enable the automatic microstepping mode.

Figure 7-5. Automatic Microstepping Interpolation

Figure 7-5 shows increment in motor angle with and without automatic microstepping. Without automatic microstepping (red plot), the motor angle increments by a large amount on every step input active edge. On the other hand, automatic microstepping (green plot) results in a much smoother change in motor angle.

The DRV8462 supports interpolation to 1/32, 1/64, 1/128 or 1/256 microstepping levels, configured by the RES_Auto bits. The interpolation setting can be changed on the fly.

Figure 7-6. Automatic Microstepping with Changing STEP Frequency

As shown in Figure 7-6, the interpolation is done based on the time between the two previous step pulses. The previous interval time is interpolated to equal divisions, depending on the RES_Auto bit setting.

When input step frequency reduces from previous interval (shown in segment '1'), the motor holds its position till the next STEP active edge occurs. Device will go to standstill power saving mode if the EN_STSL bit is '1', and the next active edge does not come within t_{STSL_DLY}. Standstill power saving mode is exited on the next STEP active edge.

When step frequency increases from previous interval (shown in segment '2'), the motor angle auto-corrects when the next STEP active edge comes, because the indexer moves to a position corresponding to the STEP input. In segment '3', the motor angle is incremented at faster rate, corresponding to the step frequency of segment '2'.

It should be ensured that the interpolated frequency does not fall in the resonant frequency band of the stepper motor.

7.4.6 Customizable Microstepping Table and Indexer Output

The DRV8462 supports a lookup table for customizing the microstepping current waveform. This allows tailoring the current waveform for the specific needs of a motor. When properly programmed, the customized current waveform ensures equally distanced microstep positions and therefore the best positional accuracy; and also minimizes the torque ripple, resulting in lower vibrations and noise.

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The EN_Custom bit enables the custom microstepping table feature. When the EN_Custom bit is '0', the lookup table is filled by values from the default microstepping indexer table, which is a good starting point for most stepper motors. When the EN_Custom bit is '1', the customizable lookup table is activated.

Figure 7-7. Customizable Microstepping

The user has to program the current values for only the first quadrant of coil A current waveform, corresponding to 0° to 90° electrical rotation. Those values are then repeated for the other three quadrants of coil A and again for the four quadrants of coil B current. The values must be entered by sequential writes to the lookup table.

A 10-bit INDEX_POS register indicates actual position in the microstep table for current in coil A. 8 bit CUR_A and CUR_B registers and associated sign bits output the microstep current for motor coil A and coil B for the position indicated by the INDEX_POS bits. When the microstep sequencer advances within the table through each possible value of the INDEX_POS bits, it calculates the actual current values for the motor coils with each microstep and stores them to the registers CUR_A and CUR_B. CUR_A and CUR_B become initialized to 0% and 100% full-scale current respectively whenever INDEX_POS passes zero.

Up to 7 unique current values, corresponding to 1/8 microstepping setting, can be programmed for the first quadrant of coil A current. The position for these current values correspond to the equidistant positions for the default microstepping indexer - at 11.25°, 22.5°, 33.75°, 45°, 56.25°, 67.5° and 78.75° electrical angles. The current values for 0° and 90° positions correspond to 0% and 100% full-scale current. For lower levels of microstepping, fewer current values have to be entered. For higher levels of microstepping, such as 1/256, the nine current values (including 0% and 100% full-scale current) are interpolated using a piecewise-linear approach to build the complete current waveform.

7.4.7 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC must not exceed 3.3 V.

Figure 7-8. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

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Figure 7-9. Controlling VREF With a PWM Resource

7.4.8 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for the OFF time to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

Figure 7-10. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. When the device is configured with H/W interface, the current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. When operating with SPI interface, two registers (TRQ_DAC and ISTSL) can further scale the reference current.

Use Equation 1 to calculate the full-scale regulation current for H/W interface.

$$I_{FS}\ (A) = VREF\ (V) / K_V\ (V/A) \quad (1)$$

For the SPI interface, the 8-bit TRQ_DAC register further scales the full-scale current as follows -

$$I_{FS}\ (A) = VREF\ (V) \times TRQ_DAC / K_V\ (V/A) \quad (2)$$

Table 7-8. TRQ_DAC Settings

TRQ_DAC	CURRENT SCALAR
11111111b	100%

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Table 7-8. TRQ_DAC Settings (continued)

TRQ_DAC	CURRENT SCALAR
11111110b	99.61%
11111101b	99.22%
11111100b	98.83%
.....	.....
00000000b	0.39%

Another 8-bit register ISTSL programs the holding current when the motor is being held at same position. Transitioning to a lower value of holding current reduces motor and driver power loss. See Standstill Power Saving Mode for details.

Table 7-9. ISTSL Settings

ISTSL	Holding Current Value
11111111b	TRQ_DAC
11111110b	0.9961 x TRQ_DAC
11111101b	0.9922 x TRQ_DAC
11111100b	0.9883 x TRQ_DAC
.....	.....
00000000b	0.0039 x TRQ_DAC

7.4.9 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-11, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in Figure 7-11, item 2. In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in Figure 7-11, Item 3.

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Figure 7-11. Decay Modes

The decay mode is selected by the DECAY register or the DECAY0 and DECAY1 pins, as shown in Table 7-10. The decay modes can be changed on the fly. After a decay mode change, the new decay mode is applied after a 2 µs de-glitch time. In full step and noncircular 1/2-step, the decay mode corresponding to decreasing steps is always used.

Table 7-10. Decay Mode Settings

SPI Interface	H/W Interface			
DECAY	DECAY0	DECAY1	INCREASING STEPS	DECREASING STEPS
000b	Hi-Z	1	Slow decay	Slow decay
001b	1	1	Slow decay	Mixed decay: 30% fast
010b	0	Hi-Z	Slow decay	Mixed decay: 60% fast
011b	1	Hi-Z	Slow decay	Fast decay
100b	1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
101b	Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
110b	0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
111b (default)	0	1	Smart tune Ripple Control	Smart tune Ripple Control
-	Hi-Z	Hi-Z	Silent step decay mode	

Figure 7-12 defines increasing and decreasing current.

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Figure 7-12. Definition of Increasing and Decreasing Steps

The DRV8462 also features the silent step decay mode for ultra-silent operation at low speed and standstill. See Silent step decay mode for details.

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7.4.9.1 Slow Decay for Increasing and Decreasing Current

Figure 7-13. Slow/Slow Decay Mode

During slow decay, both low-side MOSFETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly. If the current at the end of the off time is above the I_{TRIP} level, slow decay will be extended for multiple off time duration, until the current at the end of the cumulative off time is below the I_{TRIP} level.

When the winding current is held static for a long time (for example while no STEP input is present), or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. The motor current can rise rapidly, and may require an extremely long off-time. In some cases this could result in loss of current regulation. An aggressive decay mode is recommended in such cases.

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7.4.9.2 Slow Decay for Increasing Current, Fast Decay for Decreasing Current

Figure 7-14. Slow/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction. In this mode, fast decay only occurs during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

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7.4.9.3 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

Figure 7-15. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF}, followed by slow decay for the remainder of the t_{OFF} time. Mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This decay mode exhibits the same current ripple as slow decay mode does for increasing current, because for increasing current, only slow decay is used in this mode. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

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7.4.9.4 Mixed Decay for Increasing and Decreasing Current

Figure 7-16. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF} time, followed by slow decay for the remainder of t_{OFF} time. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

When the winding current is held static for a long time (for example while no STEP input is present) or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. In this case the motor current can rise rapidly and require an extremely long off-time to regulate the current. Increasing and decreasing current mixed decay mode allows the current to stay in regulation when no back-EMF is present across the motor windings.

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7.4.9.5 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

Figure 7-17. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

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7.4.9.6 Smart tune Ripple Control

Figure 7-18. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level along with the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to slow/slow decay where both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} is variable depending on the current level and operating parameters.

When the device operates with SPI interface, the ripple current is programmed by the RC_RIPPLE[1:0] bits.

Table 7-11. Current Ripple Settings

RC_RIPPLE	Current Ripple at a specific microstep level
00b	19mA + 1% of I_{TRIP}
01b	19mA + 2% of I_{TRIP}
10b	19mA + 4% of I_{TRIP}
11b	19mA + 6% of I_{TRIP}

When the device operates with H/W interface, the ripple current is programmed by the TOFF pin.

Table 7-12. Current Ripple Settings

TOFF	Current Ripple at a specific microstep level
0	19mA + 1% of ITRIP
1	19mA + 2% of ITRIP
Hi-Z	19mA + 4% of ITRIP
330kΩ to GND	19mA + 6% of ITRIP

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The ripple control method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve low current ripple with current regulation. Select a lowest possible ripple current setting that ensures the PWM frequency is above the audible range.

7.4.9.7 Silent step decay mode

The DRV8462 features the silent step decay mode. The silent step is a constant frequency average current regulation scheme which results in perfectly sinusoidal current waveform and minimizes audible noise at standstill and low speeds.

Conventional peak current mode control looks at instantaneous current in the sensing MOSFETs to determine drive and decay durations. As a result, the motor driver reacts to instantaneous inaccuracies in the system. This sudden changes in current causes audible noise. The silent step decay mode uses average of the coil current over multiple cycles to determine drive and decay durations. As a result, short term variations are filtered out. Also, silent step decay mode only uses slow decay, which minimizes the audible noise due to low current ripple.

With SPI interface, when EN_SILENTSTEP bit is 1b, the device operates with silent step decay mode at low speeds. At moderate to high speeds, the decay mode must be switched back to one of the conventional current-mode decay schemes to ensure proper current regulation. So, the DECAY bits in the SPI register must be populated with the bits corresponding to the chosen high speed decay mode, for example 111b for smart tune ripple control. The SILENTSTEP_CTRL bits program the loop compensation parameters of the average current regulation scheme. The SILENTSTEP_FREQ bits program the unity gain bandwidth of the compensation loop.

The speed at which silent step mode transitions to another decay mode also has to be programmed by the SPI register. The SILENTSTEP_THR bits program the transition speed. Transition from silent step to other decay modes is immediate, whereas the transition from other decay modes to silent step happens at the boundary of electrical half-cycles.

With H/W interface, making both DECAY0 and DECAY1 Hi-Z programs the device to operate with silent step decay mode. Once in silent step decay, the M0 and M1 pins program the loop compensation parameters, and the TOFF pin programs the loop unity gain bandwidth. To transition to another decay mode, all the five pins (DECAY0, DECAY1, M0, M1 and TOFF) have to change their values according to the intended decay mode, microstepping setting and PWM off time.

7.4.9.8 PWM OFF Time

The TOFF[1:0] bits or the TOFF pin configure the PWM OFF time for all decay modes except smart tune ripple control and silent step decay modes, as shown in Table 7-13. The OFF time settings can be changed dynamically. After a OFF time setting change, the new OFF time is applied after a 2 µs de-glitch time.

Table 7-13. OFF Time Settings

MODE = 1	MODE = 0	OFF Time
TOFF	TOFF	
00b	0	7 µs
01b	1	16 µs
10b	Hi-Z	24 µs
11b	330kΩ to GND	32 µs

7.4.9.9 Blanking Time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM.

When the device operates with hardware interface, the blanking time is fixed at 1 µs. When SPI interface is enabled, the blanking time can be programmed by the TBLANK_TIME bits to 1 µs, 1.5 µs, 2 µs or 2.5 µs, with a default value of 1 µs.

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7.4.10 Auto-torque Dynamic Current Adjustment

In a conventional stepper motor driver, the output current is always constant irrespective of the load torque. As a result, when the load torque is lower than nominal, there will be resistive power loss in the motor and the driver, as shown in Figure 7-19.

The auto-torque scheme implemented in the DRV8462 adapts the output current to the load torque demand. Whenever the load torque is low, the output current will reduce to restrict resistive loss; and when the load torque goes up, the output current increases immediately to prevent motor step loss. This is shown in Figure 7-20.

Figure 7-19. Power Loss with Conventional Stepper Driver

Figure 7-20. Power Saving with Auto-torque

The auto-torque algorithm implemented in the DRV8462 provides multiple options to optimize the closed-loop response time and the power saving.

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7.4.11 Standstill Power Saving Mode

When the motor is holding the same position and not receiving any step pulses, the DRV8462 can be configured to operate in standstill power saving mode. When this mode is enabled, the power dissipation of the system can be reduced by lowering the coil current from run current (TRQ_DAC) to holding current (ISTSL). After the last STEP pulse, the device waits for an amount of time programmed by the TSTSL_DLY register, after which the coil currents are ramped down from TRQ_DAC to ISTSL over a time period programmed by the TSTSL_FALL register. The STSL flag goes up to indicate that the device is in standstill power saving mode. Once the next STEP pulse is applied, the coil current immediately ramps up to TRQ_DAC.

The TRQ_DAC is programmed by the TRQ_DAC register and the holding current is programmed by the ISTSL register, as shown in Section 7.4.8.

Figure 7-21. Standstill Power Saving Mode

7.4.12 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

Figure 7-22. Charge Pump Block Diagram

7.4.13 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1 µF ceramic capacitor. The DVDD output is nominally 5-V.

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Figure 7-23. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.4.14 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3V and 5.5V. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8462. Bypass the VCC pin to ground using a 0.1 µF ceramic capacitor.

7.4.15 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

Figure 7-24. nFAULT Pin

7.4.16 nHOME Pin

When the microstepping indexer reaches the home state (electrical angle of 45°), corresponding to 71% of full-scale current in both coils, the open-drain nHOME output is pulled low. At all other times, the nHOME output will be pulled high. Thus, the nHOME output is low once within each electrical period. The nHOME output this way helps to detect a position with more precision than a mechanical stop switch can do.

Pull up the nHOME to a 5-V, 3.3-V or 1.8-V supply using a pull-up resistor. For a 5-V pullup, the nHOME pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

7.4.17 Spread Spectrum

Spread spectrum is the method to slightly vary the clock frequency over time so that the EMC signature of the driver is distributed over a band of frequencies and not concentrated at a single frequency. This helps to reduce radiated emissions and helps pass strict EMI standards.

The DRV8462 variants with SPI interfaces have the SSC bit to enable or disable the spread spectrum. The spread spectrum feature is disabled by default. Write '1' to the SSC bit to enable the feature. The spread spectrum in the DRV8462 has a triangular profile - the variation is ±10% from nominal frequency, and the

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variation occurs over 16 steps. Both the charge pump clock and the internal clock for digital blocks are varied for the purpose of spread spectrum.

7.4.18 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events. In addition, the device is protected against stall detection in the event of overload or end-of-line movement.

7.4.18.1 VM Undervoltage Lockout

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, all the outputs are disabled (High-Z), the charge pump (CP) is disabled and nFAULT is driven low. Normal operation resumes (motor driver and charge pump) when the VM voltage recovers above the UVLO rising threshold voltage.

For the device with SPI interface, when the voltage on the VM pin falls below the UVLO falling threshold voltage, but is above the V_{RST} or VCC UVLO; SPI communication is available, the digital core of the device is active, the FAULT and UVLO bits are made high in the SPI registers and the nFAULT pin is driven low, as shown below. From this condition, if the VM voltage recovers above the UVLO rising threshold voltage, nFAULT pin is released (is pulled-up to the external voltage), and the FAULT bit is reset, but the UVLO bit remains latched high until cleared through the CLR_FLT bit or an nSLEEP reset pulse.

Figure 7-25. Supply Voltage Ramp Profile

When the voltage on the VM pin falls below the V_{RST} or VCC UVLO; SPI communication is unavailable, the digital core is shutdown, the FAULT and UVLO bits are low and the nFAULT pin is high. During a subsequent power-up, when the VM voltage exceeds the V_{RST} voltage, the digital core comes alive, UVLO bit stays low but the FAULT bit is made high; and the nFAULT pin is pulled low, as shown below. When the VM voltage exceeds the VM UVLO rising threshold, FAULT bit is reset, UVLO bit stays low and the nFAULT pin is pulled high.

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Figure 7-26. Supply Voltage Ramp Profile

7.4.18.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. For the SPI version, the FAULT and CPUV bits are made high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

7.4.18.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold, all of the half-bridges are disabled and the charge pump is disabled. VCC UVLO is not reported on the nFAULT pin.

Normal motor-driver operation resumes when the VCC undervoltage condition is removed. When device operates with SPI interface, the NPOR bit is reset and latched low in the DIAG3 register once VCC goes above the UVLO threshold. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or nSLEEP reset pulse. After successfull wake up, the NPOR bit is automatically latched high once the CLR_FLT command is issued.

7.4.18.4 Overcurrent Protection (OCP)

An analog current-limit circuit on each MOSFET limits the current through the MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the MOSFETs in both H-bridges are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry. The operating modes can be changed on the fly.

For the SPI interface operation, the FAULT and OCP bits are latched high in the SPI registers. For xOUTy to VM short, corresponding OCP_LSy_x bit goes high in the DIAG Status 1 register. Similarly, for xOUTy to ground short, corresponding OCP_HSxy_x bit goes high. For example, for AOUT1 to VM short, OCP_LS1_A bit goes high; and for BOUT2 to ground short, the OCP_HS2_B bit goes high.

7.4.18.4.1 Latched Shutdown

To select latched shutdown mode, the ENABLE pin has to be made Hi-Z for the H/W interface option, or the OCP_MODE bit should be 0b for the SPI interface option. In this mode, once the OCP condition is removed, normal operation resumes after applying a CLR_FLT command, an nSLEEP reset pulse or a power cycling.

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7.4.18.4.2 Automatic Retry

To select automatic retry mode, the ENABLE pin has to be made HIGH (> 2.7 V) for the H/W interface option, or the OCP_MODE bit should be 1b for the SPI interface option. In this mode, normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.4.18.5 Stall Detection

The DRV8462 supports stall detection feature with the SPI interface.

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown below. As motor load approaches the torque capability of the motor for a given winding current, the back-EMF will move in phase with the winding current. By detecting back-emf phase shift between rising and falling current quadrants of the motor current, the DRV8462 can detect a motor overload stall condition or an end-of-line travel.

Figure 7-27. Stall Detection by Monitoring Motor Back-EMF

The Stall Detection algorithm works only when the device is programmed to operate in the smart tune Ripple Control decay mode. The EN_STL bit has to be '1' to enable stall detection. Additionally, if any fault condition exists (UVLO, OCP, OL, OTSD etc.), stall detection will be disabled.

The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a value represented by the 12-bit register TRQ_COUNT. The comparison is done in such a way that the TRQ_COUNT value is practically independent of motor current, ambient temperature and supply voltage. Full step mode of operation is supported by this algorithm.

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For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition. If at anytime TRQ_COUNT falls below the stall threshold (represented by the 12-bit STALL_TH register), the device will detect a stall and the STALL, STL and FAULT bits are latched high in the SPI register. To indicate stall detection fault on the nFAULT pin, the STL_REP bit must be '1'. When the STL_REP bit is '1', the nFAULT pin will be driven low when a stall is detected.

In the stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor ramps to its target speed. The nFAULT is released and the fault registers are cleared when a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

TRQ_COUNT is calculated as an average torque count of the most recent four electrical half-cycles of a spinning motor. The calculated value is updated within the next 100 ns. The registers are unchanged until the next update. Subsequent updates happen every electrical half-cycle.

High motor coil resistance can result in low TRQ_COUNT. The TRQ_SCALE bit allows scaling up low TRQ_COUNT values, for ease of further processing. If the initially calculated TRQ_COUNT value is less than 500 and the TRQ_SCALE bit is '1', then the TRQ_COUNT is multiplied by a factor of 8. If the TRQ_SCALE bit is '0', TRQ_COUNT retains the value originally calculated by the algorithm.

Stall threshold can be set in two ways – either the user can write the STALL_TH bits, or let the algorithm learn the stall threshold value using the stall learning process. The stall learning process is started by setting the STL_LRN bit to '1'. The motor is intentionally stalled briefly to allow the algorithm to learn the ideal stall threshold. At the end of a successful learning, the STALL_TH register is updated with the learnt stall threshold value. The STL_LRN_OK bit goes high after a successful learning.

A stall threshold learnt at one speed may not work well for another speed. It is recommended to re-learn the stall threshold every time the motor speed is changed considerably.

7.4.18.6 Open-Load Detection (OL)

If the winding current in any coil drops below the open load current threshold (I_{OL}) and the I_{TRIP} level set by the indexer, and if this condition persists for more than the open load detection time (t_{OL}), an open-load condition is detected and nFAULT is driven low.

When the device operates with H/W interface, if the ENABLE pin is connected to DVDD, the nFAULT line is released immediately after the open load condition is removed. When the ENABLE pin is Hi-Z, the nFAULT line is released after the open load condition is removed and a nSLEEP reset pulse has been applied.

When the device operates with the SPI interface, the EN_OL bit must be '1' to enable open load detection. When an open load fault is detected, the OL and FAULT bits are latched high. If the OL_A bit is high, it indicates an open load fault in winding A, between AOUT1 and AOUT2. Similarly, an open load fault between BOUT1 and BOUT2 causes the OL_B bit to go high. When the OL_MODE bit is '1', the nFAULT line is released immediately after an open load condition is removed. When the OL_MODE bit is '0', the nFAULT line is released after an open load condition is removed and a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

The open-load fault also clears when the device is power cycled or comes out of sleep mode.

7.4.18.7 Overtemperature Warning (OTW)

When operating with SPI interface, if the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}), the OTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. The charge pump remains active during this condition.

When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically.

The OTW bit can also be configured to report the fault on the nFAULT pin, as well as set the FAULT bit in the register, by setting the TW_REP bit to 1b.

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7.4.18.8 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}), all MOSFETs in the H-bridges are disabled, and the nFAULT pin is driven low. The charge pump is disabled during this condition. For the SPI interface, the FAULT, TF and OTS bits are latched high. The recovery from thermal shutdown protection can be in two different modes: latched shutdown and automatic retry. The recovery modes can be changed on the fly.

7.4.18.8.1 Latched Shutdown

To select latched shutdown mode, the ENABLE pin has to be made Hi-Z for H/W interface operation; or the OTSD_MODE bit should be 0b for SPI interface operation. In this mode, after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.4.18.8.2 Automatic Retry

To select automatic retry mode, the ENABLE pin has to be HIGH (>2.7V) or the OTSD_MODE bit should be 1b. In this mode, normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS_OTSD}$). When operating with SPI interface, the TF and OTS bits remain latched high indicating that a thermal event occurred until a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

7.4.18.9 Fault Condition Summary

Table 7-14. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT / SPI	Disabled	Disabled	Disabled	Reset	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	—	SPI	Disabled	Disabled	Disbaled	Reset	VCC > VCC_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	OCP_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OCP_MODE = 1b / ENABLE = 1	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	Default (H/W) / EN_OL = 1b (SPI)	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	CLR_FLT / nSLEEP
		STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	
Overtemperature Warning (OTW)	T_J > T_{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Automatic: T_J < T_{OTW} - T_{HYS_OTW}
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	OTSD_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OTSD_MODE = 1b / ENABLE = 1	SPI	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4.19 Device Functional Modes

7.4.19.1 Sleep Mode (nSLEEP = 0)

The DRV8462 device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep

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mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.19.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the half bridges in the device. When the ENABLE pin is low, the output drivers are disabled in the Hi-Z state. For operation with SPI interface, the EN_OUT bit can also be used to disable the output drivers. When the EN_OUT bit is '0', the output drivers are disabled in the Hi-Z state.

Table 7-15. Conditions to Enable or Disable Output Drivers with SPI

nSLEEP	ENABLE	EN_OUT	H-BRIDGE
0	Don't Care	Don't Care	Disabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

7.4.19.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.19.4 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

7.4.19.5 Functional Modes Summary

Table 7-16. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 60 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 60 V	nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

When configured to operate with SPI interface, the device SPI has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

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- One target device
- Multiple target devices in parallel connection
- Multiple target devices in series (daisy chain) connection

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W0 (bit 14)
- 6 address bits, A (bits 13 through 8)
- 8 data bits, D (bits 7 through 0)

The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 7-17. SDI Input Data Word Format

	R/W	ADDRESS						DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-18. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for a Single Target Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in target mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. Figure 7-28 shows the data sequence between the MCU and the SPI target driver.

Figure 7-28. SPI Transaction Between MCU and the device

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first.
- If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.

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- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

7.5.1.3 SPI for Multiple Target Devices in Daisy Chain Configuration

The device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. Figure 7-29 shows the topology when three devices are connected in series.

Figure 7-29. Three DRV8462 Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

Figure 7-30. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

Figure 7-31. SPI Data Sequence for Three Devices

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The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

Figure 7-32. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

Figure 7-33. Contents of Header, Status, Address, and Data Bytes for DRV8452

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 7-31, are the content of the register being accessed.

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Figure 7-34. SPI Transaction

7.5.1.4 SPI for Multiple Target Devices in Parallel Configuration

Figure 7-35. Three DRV8462 Devices Connected in Parallel Configuration

7.6 Register Maps

Table 7-19 lists the memory-mapped registers for the device. All register addresses not listed in Table 7-19 should be considered as reserved locations and the register contents must not be modified.

Table 7-19. Memory Map

Register	7	6	5	4	3	2	1	0	Type	Address
FAULT	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01

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Table 7-19. Memory Map (continued)

Register	7	6	5	4	3	2	1	0	Type	Address
DIAG2	STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A	R	0x02
DIAG3	SS_ON	NHOME	CNT_OFLW	CNT_UFLW	SS_ERROR	NPOR	RSVD		R	0x03
CTRL1	EN_OUT	SR	RSVD	TOFF [1:0]		DECAY [2:0]			RW	0x04
CTRL2	DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]				RW	0x05
CTRL3	CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP	RW	0x06
CTRL4	TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	RSVD	STEP_FREQ_TOL[1:0]		RW	0x07
CTRL5	STALL_TH [7:0]								RW	0x08
CTRL6	RC_RIPPLE[1:0]		EN_SSC	TRQ_SCALE	STALL_TH[11:8]				RW	0x09
CTRL7	TRQ_COUNT [7:0]								R	0x0A
CTRL8	REV_ID[3:0]				TRQ_COUNT[11:8]				R	0x0B
CTRL9	EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO	RW	0x0C
CTRL10	ISTSL[7:0]								RW	0x0D
CTRL11	TRQ_DAC[7:0]								RW	0x0E
CTRL12	EN_STSL	TSTSL_FALL[3:0]				RSVD			RW	0x0F
CTRL13	TSTSL_DLY[5:0]						RSVD		RW	0x10
INDEX1	CUR_A_POS[7:0]								R	0x11
INDEX2	CUR_A_SIGN	RSVD							R	0x12
INDEX3	CUR_B_POS[7:0]								R	0x13
INDEX4	CUR_B_SIGN	RSVD					INDEX_POS[9:8]		R	0x14
INDEX5	INDEX_POS[7:0]								R	0x15
CUSTOM_CTRL1	RSVD							EN_CUSTOM	RW	0x16
CUSTOM_CTRL2	CUSTOM_CURRENT1[7:0]								RW	0x17
CUSTOM_CTRL3	CUSTOM_CURRENT2[7:0]								RW	0x18
CUSTOM_CTRL4	CUSTOM_CURRENT3[7:0]								RW	0x19
CUSTOM_CTRL5	CUSTOM_CURRENT4[7:0]								RW	0x1A
CUSTOM_CTRL6	CUSTOM_CURRENT5[7:0]								RW	0x1B
CUSTOM_CTRL7	CUSTOM_CURRENT6[7:0]								RW	0x1C
CUSTOM_CTRL8	CUSTOM_CURRENT7[7:0]								RW	0x1D
CUSTOM_CTRL9	CUSTOM_CURRENT8[7:0]								RW	0x1E
ATQ_CTRL1	ATQ_CNT[7:0]								R	0x1F
ATQ_CTRL2	ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]			RW	0x20
ATQ_CTRL3	ATQ_LRN_CONST1[7:0]								RW	0x21
ATQ_CTRL4	ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]			RW	0x22
ATQ_CTRL5	ATQ_LRN_CONST2[7:0]								RW	0x23
ATQ_CTRL6	ATQ_UL[7:0]								RW	0x24
ATQ_CTRL7	ATQ_LL[7:0]								RW	0x25
ATQ_CTRL8	KP[7:0]								RW	0x26
ATQ_CTRL9	KI[3:0]				KD[3:0]				RW	0x27
ATQ_CTRL10	ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]			RW	0x28
ATQ_CTRL11	ATQ_TRQ_MIN[7:0]								RW	0x29
ATQ_CTRL12	ATQ_TRQ_MAX[7:0]								RW	0x2A

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Table 7-19. Memory Map (continued)

Register	7	6	5	4	3	2	1	0	Type	Address
ATQ_CTRL13	RSVD								RW	0x2B
ATQ_CTRL14	RSVD								RW	0x2C
ATQ_CTRL15	RSVD				ATQ_LRN_STEP[1:0]		ATQ_LRN_CYCLE-SELECT[1:0]		RW	0x2D
ATQ_CTRL16	ATQ_TRQ_DAC[7:0]								R	0x2E
ATQ_CTRL17	RSVD	VM_SCALE	RSVD						RW	0x2F
ATQ_CTRL18	RSVD		VREF_INT_EN	RSVD					RW	0x30
SS_CTRL1	RSVD				SS_PWM_FREQ[1:0]		RSVD	EN_SS	RW	0x31
SS_CTRL2	SS_KP[7:0]								RW	0x32
SS_CTRL3	SS_KI[7:0]								RW	0x33
SS_CTRL4	RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]			RW	0x34
SS_CTRL5	SS_THR[7:0]								RW	0x35

Complex bit access types are encoded to fit into small table cells. Table 7-20 shows the codes that are used for access types in this section.

Table 7-20. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers.

Table 7-21 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-21 should be considered as reserved locations and the register contents should not be modified.

Table 7-21. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT	Go
0x01	DIAG1	Go
0x02	DIAG2	Go
0x03	DIAG3	Go

7.6.1.1 FAULT (address = 0x00)

FAULT status is shown in Figure 7-36 and described in Table 7-22.

Read-only

Figure 7-36. FAULT Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL

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Figure 7-36. FAULT Register (continued)

R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-22. FAULT Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	FAULT bit is 1 when device has any fault condition. During normal operation, FAULT bit is 0. nFAULT pin is pulled down when FAULT bit is 1. nFAULT pin is released during normal operation.
6	SPI_ERROR	R	0b	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. Becomes high in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	Indicates an supply undervoltage lockout fault condition.
4	CPUV	R	0b	Indicates charge pump undervoltage fault condition.
3	OCP	R	0b	Indicates overcurrent fault condition
2	STL	R	0b	Indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning and overtemperature shutdown.
0	OL	R	0b	Indicates open-load condition.

7.6.1.2 DIAG1 (address = 0x01)

DIAG1 is shown in Figure 7-37 and described in Table 7-23.

Read-only

Figure 7-37. DIAG1 Register

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-23. DIAG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OCP_LS2_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in BOUT
6	OCP_HS2_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in BOUT
5	OCP_LS1_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in BOUT
4	OCP_HS1_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in BOUT
3	OCP_LS2_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in AOUT
2	OCP_HS2_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in AOUT
1	OCP_LS1_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in AOUT
0	OCP_HS1_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in AOUT

7.6.1.3 DIAG2 (address = 0x02)

DIAG2 is shown in Figure 7-38 and described in Table 7-24.

Read-only

Figure 7-38. DIAG2 Register

7	6	5	4	3	2	1	0
STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A

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Figure 7-38. DIAG2 Register (continued)

R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-24. DIAG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	STSL	R	0b	Indicates motor standstill.
6	OTW	R	0b	Indicates overtemperature warning.
5	OTS	R	0b	Indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	Indicates stall detection learning is successful
3	STALL	R	0b	Indicates motor stall condition
2	LRN_DONE	R	0b	Indicates auto torque learning is successful
1	OL_B	R	0b	Indicates open-load detection on BOUT
0	OL_A	R	0b	Indicates open-load detection on AOUT

7.6.1.4 DIAG3 (address = 0x03)

DIAG3 is shown in Figure 7-39 and described in Table 7-25.

Read-only

Figure 7-39. DIAG3 Register

7	6	5	4	3	2	1	0
SS_ON	NHOME	CNT_OFLW	CNT_UFLW	SS_ERROR	NPOR	RSVD	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

Table 7-25. DIAG3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SS_ON	R	0b	Indicates that device is working with silentstep decay mode
6	NHOME	R	0b	Indicates indexer is at home position of step table
5	CNT_OFLW	R	0b	Indicates ATQ_CNT is more than ATQ_UL
4	CNT_UFLW	R	0b	Indicates ATQ_CNT is less than ATQ_LL
3	SS_ERROR	R	0b	Indicates
2	NPOR	R	0b	Indicates a VCC UVLO event
1-0	RSVD	R	00b	Reserved

7.6.2 Control Registers

The IC control registers are used to configure the device. Control registers are read and write capable.

Table 7-26 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 7-26 should be considered as reserved locations and the register contents should not be modified.

Table 7-26. Control Registers Summary Table

Address	Register Name	Section
0x04	CTRL1	Go
0x05	CTRL2	Go
0x06	CTRL3	Go
0x07	CTRL4	Go
0x08	CTRL5	Go
0x09	CTRL6	Go

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Table 7-26. Control Registers Summary Table (continued)

Address	Register Name	Section
0x0A	CTRL7	Go
0x0B	CTRL8	Go
0x0C	CTRL9	Go
0x0D	CTRL10	Go
0x0E	CTRL11	Go
0x0F	CTRL12	Go
0x1A	CTRL13	Go

7.6.2.1 CTRL1 (address = 0x04)

CTRL1 is shown in Figure 7-40 and described in Table 7-27.

Read/Write

Figure 7-40. CTRL1 Control Register

7	6	5	4	3	2	1	0
EN_OUT	SR	RSVD	TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-0b	R/W-0b	R/W-01b		R/W-111b		

Table 7-27. CTRL1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OUT	R/W	0b	Write '1' to enable all outputs.
6	SR	R/W	0b	**0b = Output rise/fall time 100 ns** 1b = Output rise/fall time 50 ns
5	RSVD	R/W	0b	Reserved
4-3	TOFF [1:0]	R/W	01b	00b = 7 µs **01b = 16 µs** 10b = 24 µs 11b = 32 µs
2-0	DECAY [2:0]	R/W	111b	000b = Increasing SLOW, decreasing SLOW 001b = Increasing SLOW, decreasing MIXED 30% 010b = Increasing SLOW, decreasing MIXED 60% 011b = Increasing SLOW, decreasing FAST 100b = Increasing MIXED 30%, decreasing MIXED 30% 101b = Reserved 110b = Smart tune Dynamic Decay **111b = Smart tune Ripple Control**

7.6.2.2 CTRL2 (address = 0x05)

CTRL2 is shown in Figure 7-41 and described in Table 7-28.

Read/Write

Figure 7-41. CTRL2 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0110b			

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Table 7-28. CTRL2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIR	R/W	0b	Direction input. Logic '1' sets the direction of stepping, when SPI_DIR = 1.
6	STEP	R/W	0b	Step input. Logic '1' causes the indexer to advance one step, when SPI_STEP = 1. This bit is self-clearing, automatically becomes '0' after writing '1'.
5	SPI_DIR	R/W	0b	**0b = Outputs follow input pin for DIR** 1b = Outputs follow SPI registers DIR
4	SPI_STEP	R/W	0b	**0b = Outputs follow input pin for STEP** 1b = Outputs follow SPI registers STEP
3-0	MICROSTEP_MODE [3:0]	R/W	0110b	**0000b = Full step (2-phase excitation) with 100% current** 0001b = Full step (2-phase excitation) with 71% current 0010b = Non-circular 1/2 step 0011b = 1/2 step 0100b = 1/4 step 0101b = 1/8 step 0110b = 1/16 step 0111b = 1/32 step 1000b = 1/64 step 1001b = 1/128 step 1010b = 1/256 step 1011b to 1111b = Reserved

7.6.2.3 CTRL3 (address = 0x06)

CTRL3 is shown in Figure 7-42 and described in Table 7-29.

Read/Write

Figure 7-42. CTRL3 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP
R/W-0b	R/W-011b			R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 7-29. CTRL3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write '1' to this bit to clear all latched fault bits. This bit automatically resets after being written.
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x06h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
3	TOCP	R/W	1b	**1b = OCP deglitch time is 2 µs** 0b = OCP deglitch time is 1 µs
2	OCP_MODE	R/W	0b	**0b = Overcurrent condition causes a latched fault** 1b = Overcurrent condition causes an automatic retrying fault
1	OTSD_MODE	R/W	0b	**0b = Overtemperature condition will cause latched fault** 1b = Overtemperature condition will cause automatic recovery fault

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Table 7-29. CTRL3 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	TW_REP	R/W	0b	**0b = Overtemperature or undertemperature warning is not reported on the nFAULT line** 1b = Overtemperature or undertemperature warning is reported on the nFAULT line

7.6.2.4 CTRL4 (address = 0x07)

CTRL4 control is shown in Figure 7-43 and described in Table 7-30.

Read/Write

Figure 7-43. CTRL4 Control Register

7	6	5	4	3	2	1	0
TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	RSVD	STEP_FREQ_TOL[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-00b	

Table 7-30. CTRL4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	TBLANK_TIME[1:0]	R/W	00b	Controls the current sense blanking time. **00b = 1 µs blanking time** 01b = 1.5 µs blanking time 10b = 2 µs blanking time 11b = 2.5 µs blanking time
5	STL_LRN	R/W	0b	Write '1' to learn stall count for stall detection. This bit automatically returns to '0' when the stall learning process is complete.
4	EN_STL	R/W	0b	**0b = Stall detection is disabled** 1b = Stall detection is enabled
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT **1b = Stall detection is reported on nFAULT**
2	RSVD	R/W	0b	Reserved. Should always be '0'.
1-0	STEP_FREQ_TOL[1:0]	R/W	00b	Programs the filter setting on the STEP frequency input. **00b = No filtering** 01b = 2% filtering 10b = 4% filtering 11b = 6% filtering

7.6.2.5 CTRL5 (address = 0x08)

CTRL5 is shown in Figure 7-44 and described in Table 7-31.

Read/Write

Figure 7-44. CTRL5 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
R/W-00000011b							

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Table 7-31. CTRL5 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	STALL_TH [7:0]	R/W	00000011b	Lower 8-bits of stall threshold. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.6.2.6 CTRL6 (address = 0x09)

CTRL6 is shown in Figure 7-45 and described in Table 7-32.

Read/Write

Figure 7-45. CTRL6 Control Register

7	6	5	4	3	2	1	0
RC_RIPPLE[1:0]		EN_SSC	TRQ_SCALE	STALL_TH[11:8]			
R/W-00b		R/W-1b	R/W-0b	R/W-0000b			

Table 7-32. CTRL6 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RC_RIPPLE[1:0]	R/W	00b	Controls the current ripple in smart tune ripple control decay mode. **00b = 1% ripple** 01b = 2% ripple 10b = 4% ripple 11b = 6% ripple
5	EN_SSC	R/W	0b	**0b = spread-spectrum disabled** 1b = spread-spectrum enabled
4	TRQ_SCALE	R/W	0b	**0b = No torque count scaling is applied** 1b = Torque count is scaled up by a factor of 8
3-0	STALL_TH[11:8]	R/W	0000b	Upper 4-bits of stall threshold.

7.6.2.7 CTRL7 (address = 0x0A)

CTRL7 is shown in Figure 7-46 and described in Table 7-33.

Read-only

Figure 7-46. CTRL7 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT[7:0]							
R-11111111b							

Table 7-33. CTRL7 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_COUNT[7:0]	R	11111111b	Lower 8-bits of TRQ_COUNT. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.6.2.8 CTRL8 (address = 0x0B)

CTRL8 is shown in Figure 7-47 and described in Table 7-34.

Read-only

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Figure 7-47. CTRL8 Control Register

7	6	5	4	3	2	1	0
REV_ID[3:0]				TRQ_COUNT[11:8]			
R-0000b				R-1111b			

Table 7-34. CTRL8 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	REV_ID[3:0]	R	0000b	Silicon Revision Identification. 0000b indicates Production Revision.
3-0	TRQ_COUNT[11:8]	R	1111b	Upper 4-bits of TRQ_COUNT.

7.6.2.9 CTRL9 (address = 0x0C)

CTRL9 is shown in Figure 7-48 and described in Table 7-35.

Read/Write

Figure 7-48. CTRL9 Control Register

7	6	5	4	3	2	1	0
EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO
R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-00b		R/W-0b

Table 7-35. CTRL9 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OL	R/W	0b	Write '1' to enable open load detection
6	OL_MODE	R/W	0b	**0b = nFAULT is released after latched OL fault is cleared using CLR_FLT bit or nSLEEP reset pulse** 1b = nFAULT is released immediately after OL fault condition is removed
5-4	OL_T[1:0]	R/W	00b	Controls the open load fault detection time. **00b = 25 ms** 01b = 50 ms 10b = 100 ms 11b = Reserved
3	STEP_EDGE	R/W	0b	**0b = Active edge for STEP input is only rising edge** 1b = Active edge for STEP input is both rising and falling edges
2-1	RES_AUTO[1:0]	R/W	00b	Controls the microstepping resolution in automatic microstepping mode. **00b = 1/256** 01b = 1/128 10b = 1/64 11b = 1/32
0	EN_AUTO	R/W	0b	**0b = Automatic microstepping disabled** 1b = Automatic microstepping enabled

7.6.2.10 CTRL10 (address = 0x0D)

CTRL10 control is shown in Figure 7-49 and described in Table 7-36.

Read/Write

Figure 7-49. CTRL10 Control Register

7	6	5	4	3	2	1	0
ISTSL[7:0]							

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Figure 7-49. CTRL10 Control Register (continued)

R/W-10000000b

Table 7-36. CTRL10 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ISTSL[7:0]	R/W	10000000b	11111111b = 256/256 x TRQ_DAC 11111110b = 255/256 x TRQ_DAC 11111101b = 254/256 x TRQ_DAC 11111100b = 253/256 x TRQ_DAC ..... 00000000b = 1/256 x TRQ_DAC

7.6.2.11 CTRL11 (address = 0x0E)

CTRL11 control is shown in Figure 7-50 and described in Table 7-37.

Read/Write

Figure 7-50. CTRL11 Control Register

7	6	5	4	3	2	1	0
TRQ_DAC[7:0]							
R/W-11111111b							

Table 7-37. CTRL11 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_DAC[7:0]	R/W	11111111b	**11111111b = 256/256 x 100%** 11111110b = 255/256 x 100% 11111101b = 254/256 x 100% 11111100b = 253/256 x 100% ..... 00000000b = 1/256 x 100%

7.6.2.12 CTRL12 (address = 0x0F)

CTRL12 is shown in Figure 7-51 and described in Table 7-38.

Read/Write

Figure 7-51. CTRL12 Control Register

7	6	5	4	3	2	1	0
EN_STSL	TSTSL_FALL[3:0]				RSVD		
R/W-0b	R/W-0100b				R/W-000b		

Table 7-38. CTRL12 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_STSL	R/W	0b	**0b = Standstill power saving mode disabled** 1b = Standstill power saving mode enabled
6-3	TSTSL_FALL[3:0]	R/W	0100b	Controls the current fall time from IRUN to IHOLD after TSTSL_DLY 0000b: fall time = 0 0001b: fall time for each current step = 16 ms ..... 1111b: fall time for each current step = 240 ms

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Table 7-38. CTRL12 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2-0	RSVD	R/W	000b	Reserved

7.6.2.13 CTRL13 (address = 0x10)

CTRL13 is shown in Figure 7-52 and described in Table 7-39.

Read/Write

Figure 7-52. CTRL13 Control Register

7	6	5	4	3	2	1	0
TSTSL_DLY[5:0]						RSVD	
R/W-000100b						R/W-00b	

Table 7-39. CTRL13 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	TSTSL_DLY[5:0]	R/W	000100b	Controls the delay between last STEP pulse and activation of standstill power saving mode. 000000b: Delay = 0 000001b: Delay = 1 x 16 ms = 16 ms 000010b: Delay = 2 x 16 ms = 32 ms ..... 111111b: Delay = 63 x 16 ms = 1.008 s
1-0	RSVD	R/W	00b	Reserved

7.6.3 Indexer Registers

The indexer registers provide signed current values for coils A and B, and the position in the microstep table for the current in coil A. Indexer registers are read only.

Table 7-40 lists the memory-mapped registers for the indexer registers. All register offset addresses not listed in Table 7-40 should be considered as reserved locations and the register contents should not be modified.

Table 7-40. Indexer Registers Summary Table

Address	Register Name	Section
0x11	INDEX1	Go
0x12	INDEX2	Go
0x13	INDEX3	Go
0x14	INDEX4	Go
0x15	INDEX5	Go

7.6.3.1 INDEX1 (address = 0x11)

INDEX1 is shown in Figure 7-53 and described in Table 7-41.

Read only

Figure 7-53. INDEX1 Register

7	6	5	4	3	2	1	0
CUR_A[7:0]							
R-00000000b							

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Table 7-41. INDEX1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_A[7:0]	R	00000000b	Outputs the current of motor coil A for the position indicated by the INDEX_POS bits.

7.6.3.2 INDEX2 (address = 0x12)

INDEX2 is shown in Figure 7-54 and described in Table 7-42.

Read only

Figure 7-54. INDEX2 Register

7	6	5	4	3	2	1	0
CUR_A_SIGN	RSVD						
R-0b	R-0000000b						

Table 7-42. INDEX2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_A_SIGN	R	0b	Outputs the sign of coil A current for the position indicated by the INDEX_POS bits. **0b = Coil A current is positive** 1b = Coil A current is negative
6-0	RSVD	R	0000000b	Reserved

7.6.3.3 INDEX3 (address = 0x13)

INDEX3 is shown in Figure 7-55 and described in Table 7-43.

Read only

Figure 7-55. INDEX3 Register

7	6	5	4	3	2	1	0
CUR_B[7:0]							
R-00000000b							

Table 7-43. INDEX3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_B[7:0]	R	00000000b	Outputs the current of motor coil B for the position indicated by the INDEX_POS bits.

7.6.3.4 INDEX4 (address = 0x14)

INDEX4 is shown in Figure 7-56 and described in Table 7-44.

Read only

Figure 7-56. INDEX4 Register

7	6	5	4	3	2	1	0
CUR_B_SIGN	RSVD					INDEX_POS[9:8]	
R-0b	R-00000b					R-00b	

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Table 7-44. INDEX4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_B_SIGN	R	0b	Outputs the sign of coil B current for the position indicated by the INDEX_POS bits. **0b = Coil B current is positive** 1b = Coil B current is negative
6-2	RSVD	R	00000b	Reserved
1-0	INDEX_POS[9:8]	R	00b	Upper two MSBs of the indexer position

7.6.3.5 INDEX5 (address = 0x15)

INDEX5 is shown in Figure 7-57 and described in Table 7-45.

Read only

Figure 7-57. INDEX5 Register

7	6	5	4	3	2	1	0
INDEX_POS[7:0]							
R-00000000b							

Table 7-45. INDEX5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	INDEX_POS[7:0]	R	00000000b	Outputs the lower 8 bits of the indexer position

7.6.4 Custom Microstepping Registers

The custom microstep registers store the current values corresponding the first quadrant of coil A current. Custom microstep registers are read and write capable.

Table 7-46 lists the memory-mapped registers for the custom microstep registers. All register offset addresses not listed in Table 7-46 should be considered as reserved locations and the register contents should not be modified.

Table 7-46. Custom microstep Registers Summary Table

Address	Register Name	Section
0x16	CUSTOM_CTRL1	Go
0x17	CUSTOM_CTRL2	Go
0x18	CUSTOM_CTRL3	Go
0x19	CUSTOM_CTRL4	Go
0x1A	CUSTOM_CTRL5	Go
0x1B	CUSTOM_CTRL6	Go
0x1C	CUSTOM_CTRL7	Go
0x1D	CUSTOM_CTRL8	Go
0x1E	CUSTOM_CTRL9	Go

7.6.4.1 CUSTOM_CTRL1 (address = 0x16)

CUSTOM_CTRL1 is shown in Figure 7-58 and described in Table 7-47.

Read/Write

Figure 7-58. CUSTOM_CTRL1 Register

7	6	5	4	3	2	1	0

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Figure 7-58. CUSTOM_CTRL1 Register (continued)

RSVD	EN_CUSTOM
R/W-0000000b	R/W-0b

Table 7-47. CUSTOM_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	RSVD	R/W	0000000b	Reserved
0	EN_CUSTOM	R/W	0b	**0b = Custom microstepping table is disabled** 1b = Custom microstepping table is enabled

7.6.4.2 CUSTOM_CTRL2 (address = 0x17)

CUSTOM_CTRL2 is shown in Figure 7-59 and described in Table 7-48.

Read/Write

Figure 7-59. CUSTOM_CTRL2 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT1[7:0]							
R/W-00000000b							

Table 7-48. CUSTOM_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT1[7:0]	R/W	00000000b	Current value for position 1 in first quadrant

7.6.4.3 CUSTOM_CTRL3 (address = 0x18)

CUSTOM_CTRL3 is shown in Figure 7-60 and described in Table 7-49.

Read/Write

Figure 7-60. CUSTOM_CTRL3 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT2[7:0]							
R/W-00000000b							

Table 7-49. CUSTOM_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT2[7:0]	R/W	00000000b	Current value for position 2 in first quadrant

7.6.4.4 CUSTOM_CTRL4 (address = 0x19)

CUSTOM_CTRL4 is shown in Figure 7-61 and described in Table 7-50.

Read/Write

Figure 7-61. CUSTOM_CTRL4 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT3[7:0]							
R/W-00000000b							

Table 7-50. CUSTOM_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT3[7:0]	R/W	00000000b	Current value for position 3 in first quadrant

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7.6.4.5 CUSTOM_CTRL5 (address = 0x1A)

CUSTOM_CTRL5 is shown in Figure 7-62 and described in Table 7-51.

Read/Write

Figure 7-62. CUSTOM_CTRL5 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT4[7:0]							
R/W-00000000b							

Table 7-51. CUSTOM_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT4[7:0]	R/W	00000000b	Current value for position 4 in first quadrant

7.6.4.6 CUSTOM_CTRL6 (address = 0x1B)

CUSTOM_CTRL6 is shown in Figure 7-63 and described in Table 7-52.

Read/Write

Figure 7-63. CUSTOM_CTRL6 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT5[7:0]							
R/W-00000000b							

Table 7-52. CUSTOM_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT5[7:0]	R/W	00000000b	Current value for position 5 in first quadrant

7.6.4.7 CUSTOM_CTRL7 (address = 0x1C)

CUSTOM_CTRL7 is shown in Figure 7-64 and described in Table 7-53.

Read/Write

Figure 7-64. CUSTOM_CTRL7 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT6[7:0]							
R/W-00000000b							

Table 7-53. CUSTOM_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT6[7:0]	R/W	00000000b	Current value for position 6 in first quadrant

7.6.4.8 CUSTOM_CTRL8 (address = 0x1D)

CUSTOM_CTRL8 is shown in Figure 7-65 and described in Table 7-54.

Read/Write

Figure 7-65. CUSTOM_CTRL8 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT7[7:0]							
R/W-00000000b							

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Table 7-54. CUSTOM_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT7[7:0]	R/W	00000000b	Current value for position 7 in first quadrant

7.6.4.9 CUSTOM_CTRL9 (address = 0x1E)

CUSTOM_CTRL9 is shown in Figure 7-66 and described in Table 7-55.

Read/Write

Figure 7-66. CUSTOM_CTRL9 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT8[7:0]							
R/W-00000000b							

Table 7-55. CUSTOM_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT8[7:0]	R/W	00000000b	Current value for position 8 in first quadrant

7.6.5 Auto torque Registers

The auto torque registers control the auto torque feature. Auto torque registers are read and write capable.

Table 7-56 lists the memory-mapped registers for the auto torque registers. All register offset addresses not listed in Table 7-56 should be considered as reserved locations and the register contents should not be modified.

Table 7-56. Auto torque Registers Summary Table

Address	Register Name	Section
0x1F	ATQ_CTRL1	Go
0x20	ATQ_CTRL2	Go
0x21	ATQ_CTRL3	Go
0x22	ATQ_CTRL4	Go
0x23	ATQ_CTRL5	Go
0x24	ATQ_CTRL6	Go
0x25	ATQ_CTRL7	Go
0x26	ATQ_CTRL8	Go
0x27	ATQ_CTRL9	Go
0x28	ATQ_CTRL10	Go
0x29	ATQ_CTRL11	Go
0x2A	ATQ_CTRL12	Go
0x2B	ATQ_CTRL13	Go
0x2C	ATQ_CTRL14	Go
0x2D	ATQ_CTRL15	Go
0x2E	ATQ_CTRL16	Go
0x2F	ATQ_CTRL17	Go
0x30	ATQ_CTRL18	Go

7.6.5.1 ATQ_CTRL1 (address = 0x1F)

ATQ_CTRL1 is shown in Figure 7-67 and described in Table 7-57.

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Figure 7-67. ATQ_CTRL1 Register

7	6	5	4	3	2	1	0
ATQ_CNT[7:0]							
R-00000000b							

Table 7-57. ATQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_CNT[7:0]	R	00000000b	Indicates the 8 LSB bits of the ATQ_CNT output. ATQ_CNT is proportional to the mechanical load torque.

7.6.5.2 ATQ_CTRL2 (address = 0x20)

ATQ_CTRL2 is shown in Figure 7-68 and described in Table 7-58.

Read/Write

Figure 7-68. ATQ_CTRL2 Register

7	6	5	4	3	2	1	0
ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]		
R/W-000b			R/W-00b		R/W-000b		

Table 7-58. ATQ_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	ATQ_CNT[10:8]	R/W	000b	Indicates the 3 MSB bits of the ATQ_CNT output
4-3	RSVD	R/W	00b	Reserved
2-0	ATQ_LRN_CONST1[10:8]	R/W	000b	Indicates the 3 MSB bits of the Auto torque algorithm learn constant 1. This value is proportional to no load losses at current level 1.

7.6.5.3 ATQ_CTRL3 (address = 0x21)

ATQ_CTRL3 is shown in Figure 7-69 and described in Table 7-59.

Read/Write

Figure 7-69. ATQ_CTRL3 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST1[7:0]							
R/W-00000000b							

Table 7-59. ATQ_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST1[7:0]	R/W	00000000b	8 LSB bits of the Auto torque algorithm learn constant 1. This value is proportional to no load losses at current level 1.

7.6.5.4 ATQ_CTRL4 (address = 0x22)

ATQ_CTRL4 is shown in Figure 7-70 and described in Table 7-60.

Read/Write

Figure 7-70. ATQ_CTRL4 Register

7	6	5	4	3	2	1	0
ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]		

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Figure 7-70. ATQ_CTRL4 Register (continued)

R/W-00100b	R/W-000b

Table 7-60. ATQ_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-3	ATQ_LRN_MIN_CURRENT[4:0]	R/W	00100b	Initial current level for auto torque learning. Initial learning current = ATQ_LRN_MIN_CURRENT*8
2-0	ATQ_LRN_CONST2[10:8]	R/W	000b	3 MSB bits of the Auto torque algorithm learn constant 2

7.6.5.5 ATQ_CTRL5 (address = 0x23)

ATQ_CTRL5 is shown in Figure 7-71 and described in Table 7-61.

Read/Write

Figure 7-71. ATQ_CTRL5 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST2[7:0]							
R/W-00000000b							

Table 7-61. ATQ_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST2[7:0]	R/W	00000000b	8 LSB bits of the Auto torque algorithm learn constant 2

7.6.5.6 ATQ_CTRL6 (address = 0x24)

ATQ_CTRL6 is shown in Figure 7-72 and described in Table 7-62.

Read/Write

Figure 7-72. ATQ_CTRL6 Register

7	6	5	4	3	2	1	0
ATQ_UL[7:0]							
R/W-00000000b							

Table 7-62. ATQ_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_UL[7:0]	R/W	00000000b	Programs the upper limit of the auto torque hysterestic band. Upper band of desired operating region of ATQ_CNT.

7.6.5.7 ATQ_CTRL7 (address = 0x25)

ATQ_CTRL7 is shown in Figure 7-73 and described in Table 7-63.

Read/Write

Figure 7-73. ATQ_CTRL7 Register

7	6	5	4	3	2	1	0
ATQ_LL[7:0]							
R/W-00000000b							

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Table 7-63. ATQ_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LL[7:0]	R/W	00000000b	Programs the lower limit of the auto torque hysteresis band. Lower Band of desired operating region of ATQ_CNT.

7.6.5.8 ATQ_CTRL8 (address = 0x26)

ATQ_CTRL8 is shown in Figure 7-74 and described in Table 7-64.

Read/Write

Figure 7-74. ATQ_CTRL8 Register

7	6	5	4	3	2	1	0
KP[7:0]							
R/W-00000000b							

Table 7-64. ATQ_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	KP[7:0]	R/W	00000000b	Proportional constant for tuning the auto torque control loop.

7.6.5.9 ATQ_CTRL9 (address = 0x27)

ATQ_CTRL9 is shown in Figure 7-75 and described in Table 7-65.

Read/Write

Figure 7-75. ATQ_CTRL9 Register

7	6	5	4	3	2	1	0
KI[3:0]				KD[3:0]			
R/W-0000b				R/W-0000b			

Table 7-65. ATQ_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	KI[3:0]	R/W	0000b	Integral constant for tuning the auto torque control loop.
3-0	KD[3:0]	R/W	0000b	Differential constant for tuning the auto torque control loop.

7.6.5.10 ATQ_CTRL10 (address = 0x28)

ATQ_CTRL10 is shown in Figure 7-76 and described in Table 7-66.

Read/Write

Figure 7-76. ATQ_CTRL10 Register

7	6	5	4	3	2	1	0
ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]		
R/W-0b	R/W-0b	R/W-000b			R/W-000b		

Table 7-66. ATQ_CTRL10 Register Field Descriptions

Bit	Field	Type	Default	Description
7	ATQ_EN	R/W	0b	**0 = auto torque is disabled** 1 = auto torque is enabled
6	LRN_START	R/W	0b	Writing '1' to this bit enables the auto torque learning process. After learning is completed, the bit automatically goes to '0'.

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Table 7-66. ATQ_CTRL10 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-3	ATQ_FRZ[2:0]	R/W	001b	After any output current update, number of half cycles for which current update is frozen. Range 1 to 7. 1-Fastest response time,loop can be unstable 7-slowest response ,stable response
2-0	ATQ_AVG[2:0]	R/W	000b	Number of half cycles used for averaging in ATQ_COUNT calculation. 2 - 2 cycle average 4 - 4 cycle average 7 - 8 cycle average Others : no averaging

7.6.5.11 ATQ_CTRL11 (address = 0x29)

ATQ_CTRL11 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-77. ATQ_CTRL11 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MIN[7:0]							
R/W-00001010b							

Table 7-67. ATQ_CTRL11 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MIN[7:0]	R/W	00001010b	Auto torque minimum current limit.

7.6.5.12 ATQ_CTRL12 (address = 0x2A)

ATQ_CTRL12 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-78. ATQ_CTRL12 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MAX[7:0]							
R/W-11111111b							

Table 7-68. ATQ_CTRL12 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MAX[7:0]	R/W	11111111b	Auto torque maximum current limit.

7.6.5.13 ATQ_CTRL13 (address = 0x2B)

ATQ_CTRL13 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-79. ATQ_CTRL13 Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00000101b							

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Table 7-69. ATQ_CTRL13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00000101b	Reserved.

7.6.5.14 ATQ_CTRL14 (address = 0x2C)

ATQ_CTRL14 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-80. ATQ_CTRL14 Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00001111b							

Table 7-70. ATQ_CTRL14 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00001111b	Reserved.

7.6.5.15 ATQ_CTRL15 (address = 0x2D)

ATQ_CTRL15 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-81. ATQ_CTRL15 Register

7	6	5	4	3	2	1	0
RSVD				ATQ_LRN_STEP		ATQ_LRN_CYCLE_SELECT	
R/W-0000b				R/W-00b		R/W-00b	

Table 7-71. ATQ_CTRL15 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R/W	0000b	Reserved.
3-2	ATQ_LRN_STEP[1:0]	R/W	00b	Step increment in ATQ learn current **00b : 128** 01b : 64 10b : 32 11b : 16 Example : If ATQ_LRN_STEP= 10b and ATQ_LRN_MIN_CURRENT = 11000b, then Initial learn current level = 24 Final learn current level = 56 (24 + 32)
1-0	ATQ_LRN_CYCLE_SELECT[1:0]	R/W	00b	Applicable for learning. Number of sine half cycles in one current level before which the algorithm lets the current jump to the next level. **00b : 8** 01b : 16 10b : 24 11b : 32

7.6.5.16 ATQ_CTRL16 (address = 0x2E)

ATQ_CTRL16 is shown in Figure 7-77 and described in Table 7-67.

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Figure 7-82. ATQ_CTRL16 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_DAC[7:0]							
R-00000000b							

Table 7-72. ATQ_CTRL16 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_DAC[7:0]	R	00000000b	Auto torque current level readout.

7.6.5.17 ATQ_CTRL17 (address = 0x2F)

ATQ_CTRL17 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-83. ATQ_CTRL17 Register

7	6	5	4	3	2	1	0
RSVD	VM_SCALE	RSVD					
R/W-0b	R/W-0b	R/W-000000b					

Table 7-73. ATQ_CTRL17 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.
6	VM_SCALE	R/W	0b	Enables adaptability to supply voltage change. When supply voltage change is detected, the algorithm will scale ATQ_UL, ATQ_LL, ATQ_LRN_CONST1 and ATQ_LRN_CONST2.
5-0	RSVD	R/W	000000b	Reserved.

7.6.5.18 ATQ_CTRL18 (address = 0x30)

ATQ_CTRL18 is shown in Figure 7-77 and described in Table 7-67.

Read/Write

Figure 7-84. ATQ_CTRL18 Register

7	6	5	4	3	2	1	0
RSVD		VREF_INT_EN	RSVD				
R/W-00b		R/W-0b	R/W-00000b				

Table 7-74. ATQ_CTRL18 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RSVD	R/W	00b	Reserved.
5	VREF_INT_EN	R/W	0b	1b = Enables internal 3.3V reference voltage **0b = Device works with external reference voltage (VREF pin)**
4	RSVD	R/W	00000b	Reserved.

7.6.6 Silent Step Registers

The silent step registers control the silent step decay mode. Silent step registers are read and write capable.

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Table 7-75 lists the memory-mapped registers for the silent step registers. All register offset addresses not listed in Table 7-75 should be considered as reserved locations and the register contents should not be modified.

Table 7-75. Silent step Registers Summary Table

Address	Register Name	Section
0x31	SS_CTRL1	Go
0x32	SS_CTRL2	Go
0x33	SS_CTRL3	Go
0x34	SS_CTRL4	Go
0x35	SS_CTRL5	Go

7.6.6.1 SS_CTRL1 (address = 0x31)

SS_CTRL1 is shown in Figure 7-85 and described in Table 7-76.

Read/Write

Figure 7-85. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD				SS_PWM_FREQ[1:0]		RSVD	EN_SILENTSTEP
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 7-76. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R/W	0000b	Reserved
3-2	SS_PWM_FREQ[1:0]	R/W	00b	Silent step decay PWM frequency configuration **00b - 25KHz** 01b - 33KHz 10b - 42KHz 11b - 50KHz
1	RSVD	R/W	0b	Reserved
0	EN_SILENTSTEP	R/W	0b	**0b = silentstep decay mode is disabled** 1b = silentstep decay mode is enabled

7.6.6.2 SS_CTRL2 (address = 0x32)

SS_CTRL2 is shown in Figure 7-86 and described in Table 7-77.

Read/Write

Figure 7-86. SS_CTRL2 Register

7	6	5	4	3	2	1	0
SS_KP[7:0]							
R/W-00000000b							

Table 7-77. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SS_KP[7:0]	R/W	00000000b	Silent step decay mode proportional constant of the compensation loop. Range from 0 to 127.

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7.6.6.3 SS_CTRL3 (address = 0x33)

SS_CTRL3 is shown in Figure 7-87 and described in Table 7-78.

Read/Write

Figure 7-87. SS_CTRL3 Register

7	6	5	4	3	2	1	0
SS_KI[7:0]							
R/W-00000000b							

Table 7-78. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SS_KI[7:0]	R/W	00000000b	Silent step decay mode integral constant of the compensation loop. Range from 0 to 127.

7.6.6.4 SS_CTRL4 (address = 0x34)

SS_CTRL4 is shown in Figure 7-88 and described in Table 7-79.

Read/Write

Figure 7-88. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 7-79. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6-4	SS_KI_DIV_SEL[2:0]	R/W	000b	Silent step decay mode KI divider Actual KI = SS_KI/SS_KI_DIV_SEL **000b - SS_KI/32** 001b - SS_KI/64 010b - SS_KI/128 011b - SS_KI/256 100b - SS_KI/512 101b - SS_KI/16 110b - SS_KI
3-1	RSVD	R/W	0b	Reserved
0	SS_KP_DIV_SEL[2:0]	R/W	000b	Silent step decay mode KP divider Actual KP = SS_KP/SS_KP_DIV_SEL **000b - SS_KP/32** 001b - SS_KP/64 010b - SS_KP/128 011b - SS_KP/256 100b - SS_KP/512 101b - SS_KP/16 110b - SS_KP

7.6.6.5 SS_CTRL5 (address = 0x35)

SS_CTRL5 is shown in Figure 7-89 and described in Table 7-80.

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Read/Write

Figure 7-89. SS_CTRL5 Register

7	6	5	4	3	2	1	0
SS_THR[7:0]							
R/W-00000000b							

Table 7-80. SS_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SS_THR[7:0]	R/W	00000000b	Programs the frequency at which the device transitions from silent step decay mode to another decay mode programmed by the DECAY bits. 00000000b = 0 pps at 256 microstepping 00000001b = 2000 pps at 256 microstepping 00000010b = 4000 pps at 256 microstepping . . 11111111b = 510000 pps at 256 microstepping

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8 Power Supply Recommendations

The DRV8462 device is designed to operate from an input voltage supply (VM) range from 4.5 V to 60 V. A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of DRV8462. In addition, a bulk capacitor must be included on VM.

8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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Figure 8-1. Example Setup of Motor Drive System With External Power Supply

8.2 Power Supplies

To facilitate system design, the DRV8462 needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the H-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.
- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by built-in charge pump requiring external capacitors.

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Special attention should be paid to place all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. Furthermore, decoupling capacitors need a short ground path back to the device. It is recommended to follow the PCB layout of the DRV8462 EVM board.

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9 Layout

9.1 Layout Guidelines

The VM pins should be bypassed to PGND using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.

The VM pins must be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD of the DDW package must be connected to system ground.

Because of the power level of this device, it is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be easily made at bottom PCB layer. In order to minimize the impedance and inductance of ground traces, the traces from ground pins should keep as short and wide as possible before connected to bottom ground plane through vias. Multiple vias are suggested to reduce the impedance of vias. Try to clear the space around the device as much as possible especially at bottom PCB side to improve the heat spreading.

9.2 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. copper on both top and bottom layer is recommended for improved thermal performance (better heat sinking) and less noise susceptibility (lower PCB trace inductance).

9.3 Thermal Considerations

9.3.1 DDV Package

The thermally enhanced DDV package is designed to interface directly to a heat sink using a thermal interface compound in between,(e.g., Ceramique from Arctic Silver, TIMTronics 413, etc.). The heat sink absorbs heat from the DRV8462 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ of the DRV8462 DDV Package (thermal resistance from junction to exposed pad)
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

$R_{\theta JA} = R_{\theta JC}$ + thermal interface resistance + heat sink resistance

The thermal resistance of the thermal interface material can be determined from the manufacturer's value for the area thermal resistance (expressed in °Cmm^2/W) and the area of the exposed metal package. For example, a typical, white, thermal grease with a 0.0254 mm (0.001 inch) thick layer is approximately 4.52°C mm^2/W. The DRV8462 in the DDV package has an exposed area of 28.7 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the thermal grease. The thermal resistance of the thermal grease is 0.157°C/W.

Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured. The following are the various important parameters in selecting a heatsink.

1. Thermal resistance

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2. Airflow
3. Volumetric resistance
4. Fin density
5. Fin spacing
6. Width
7. Length

The thermal resistance is one parameter that changes dynamically depending on the airflow available.

Airflow is typically measured in linear feet per minute (LFM) or CFM (cubic feet per minute). LFM is a measure of velocity, whereas CFM is a measure of volume. Typically, fan manufacturers use CFM because fans are rated according to the quantity of air it can move. Velocity (speed) is more meaningful for heat removal at the board level, which is why the derating curves provided by most power converter manufacturers use this. Typically, airflow is either classified as natural or forced convection. Natural convection is a condition with no external induced flow and heat transfer depends on the air surrounding the heatsink. The effect of radiation heat transfer is very important in natural convection, as it can be responsible for approximately 25% of the total heat dissipation. Unless the component is facing a hotter surface nearby, it is imperative to have the heatsink surfaces painted to enhance radiation. Forced convection occurs when the flow of air is induced by mechanical means, usually a fan or blower.

Limited thermal budget and space make the choice of a particular type of heatsink very important. This is where the volume of the heatsink becomes relevant. The volume of a heatsink for a given flow condition can be obtained by using the following equation:

$Volume_{(heatsink)}$ = volumetric resistance (Cm^3 °C/W)/thermal resistance θ_{SA} (°C/W)

An approximate range of volumetric resistance is given in the following table:

Available Airflow (LFM)	Volumetric Resistance (Cm^3 °C/W)
NC	500 – 800
200	150 - 250
500	80 - 150
1000	50 - 80

The next important criterion for the performance of a heatsink is the width. It is linearly proportional to the performance of the heatsink in the direction perpendicular to the airflow. Considering an example, an increase in the width of a heatsink by a factor of two, three, or four increase the heat dissipation capability by a factor of two, three, or four. Similarly, the square root of the fin length used is approximately proportional to the performance of the heatsink in the direction parallel to the airflow. In case of an increase in the length of the heatsink by a factor of two, three, or four only increases the heat dissipation capability by a factor of 1.4, 1.7, or 2.

If the board has sufficient space, it is always beneficial to increase the width of a heatsink rather than the length of the heatsink. This is only the beginning of an iterative process before the correct and the actual heatsink design is achieved.

The heat sink must be supported mechanically at each end of the IC. This mounting ensures the correct pressure to provide good mechanical, thermal and electrical contact. The heat sink should be connected to GND or left floating.

9.3.2 DDW Package

Thermal pad of the DDW package is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet.

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OUTLINE

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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EXAMPLE BOARD LAYOUT

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

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EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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PACKAGE OUTLINE

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.

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PRODUCT PREVIEW

EXAMPLE BOARD LAYOUT

DDV0044E **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DDV0044E **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE

SOLDER PAPTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

4224779/A 01/2019

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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