DRV8424/25 Stepper Drivers With Integrated Current Sense, 1/256 Microstepping, STEP/DIR Interface and smart tune Technology

1 Features

- PWM Microstepping Stepper Motor Driver
  - Simple STEP/DIR Interface
  - Up to 1/256 Microstepping Indexer
- Integrated Current Sense Functionality
  - No Sense Resistors Required
  - ±5% Full-Scale Current Accuracy
- Smart tune decay technology, Fixed slow, and mixed decay options
- 4.5 to 33-V Operating Supply Voltage Range
- Low $R_{DS(ON)}$:
  - DRV8424: 330 mΩ HS + LS at 24 V, 25°C
  - DRV8425: 550 mΩ HS + LS at 24 V, 25°C
- High Current Capacity Per Bridge
  - DRV8424: 4A peak, 2.5A Full-Scale, 1.8A rms
  - DRV8425: 3.2A peak, 2A Full-Scale, 1.4A rms
- Configurable Off-Time PWM Chopping
  - 7-µs, 16-µs, 24-µs, or 32-µs.
- Supports 1.8-V, 3.3-V, 5.0-V Logic Inputs
- Low-Current Sleep Mode (2 µA)
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Small Package and Footprint
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Open Load Detection (OL)
  - Thermal Shutdown (OTSD)
  - Fault Condition Output (nFAULT)

2 Applications

- Printers and Scanners
- ATM and Money Handling Machines
- Textile Machines
- Stage Lighting Equipment
- Office and Home Automation
- Factory Automation and Robotics

3 Description

The DRV8424/25 are stepper motor drivers for industrial and consumer end equipment applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8424 is capable of driving up to 1.8-A rms output current; and the DRV8425 is capable of driving up to 1.4-A rms output current (dependent on PCB design).

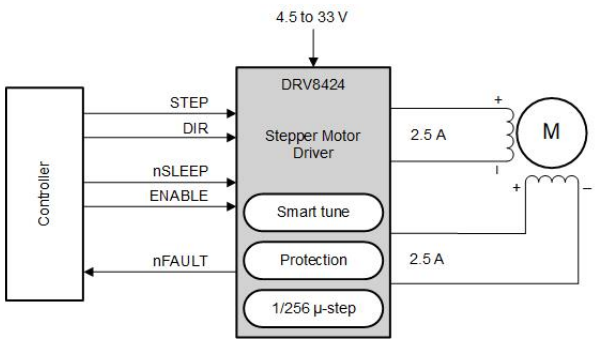
The DRV8424/25 use an internal current sense architecture to eliminate the need for two external power sense resistors, saving PCB area and system cost. The DRV8424/25 use an internal PWM current regulation scheme selectable between smart tune, fast, slow and mixed decay options. Smart tune decay technology automatically adjusts for optimal current regulation performance and compensates for motor variation and aging effects.

A simple STEP/DIR interface allows an external controller to manage the direction and step rate of the stepper motor. The device can be configured in different step modes ranging from full-step to 1/256 microstepping. A low-power sleep mode is provided for very low standby quiescent standby current using a dedicated nSLEEP pin. Protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, open load, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8424PWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8424RGER	VQFN (24)	4.0mm x 4.0mm
DRV8425PWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8425RGER	VQFN (24)	4.0mm x 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2020	*	Initial release

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5 Device Comparison Table

PART NUMBER	$R_{DS(ON)}$ (HS + LS) (mΩ)	Full-Scale Current Per Bridge (A)
DRV8424	330	2.5
DRV8425	550	2

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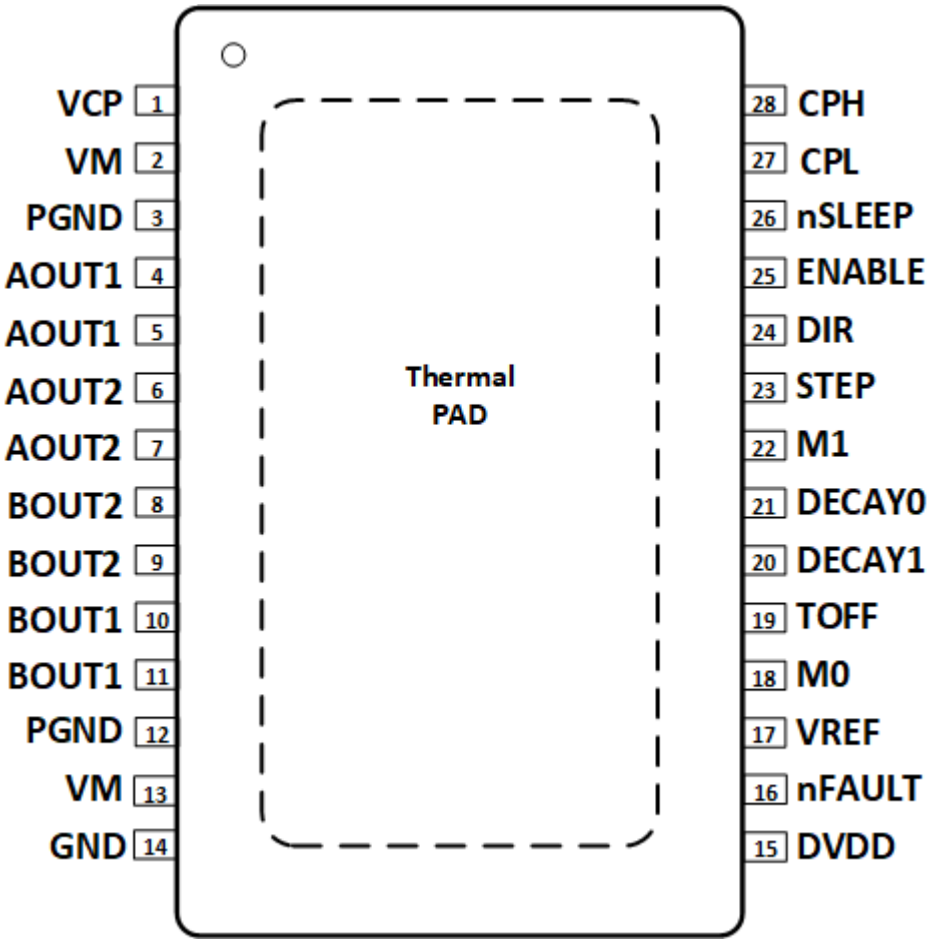
6 Pin Configuration and Functions

PWP PowerPAD™ Package
28-Pin HTSSOP
Top View



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RGE Package
24-Pin VQFN with Exposed Thermal PAD
Top View

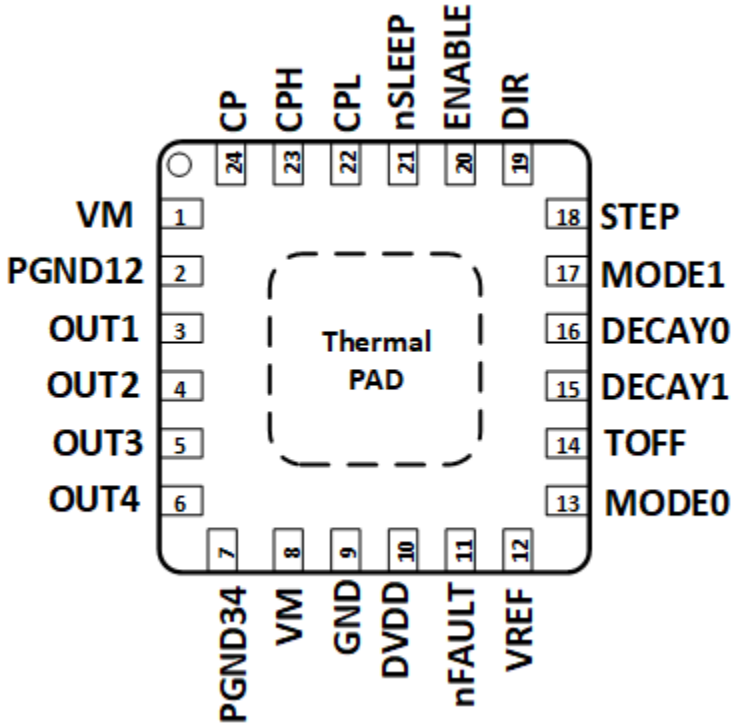

Table 1. Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	6	3	O	Output	Winding A output. Connect to stepper motor winding.
AOUT2	7	4	O	Output	Winding A output. Connect to stepper motor winding.
PGND	5, 10	2, 7	—	Power	Power ground. Connect to system ground.
BOUT2	8	5	O	Output	Winding B output. Connect to stepper motor winding
BOUT1	9	6	O	Output	Winding B output. Connect to stepper motor winding
CPH	2	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	1	22			
DIR	22	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
ENABLE	23	20	I	Input	Logic low to disable device outputs; logic high to enable; internal pullup to DVDD. Also determines the type of OCP and OTSD response.
DVDD	13	10		Power	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	12	9	—	Power	Device ground. Connect to system ground.
VREF	15	12	I	Input	Current set reference input. Maximum value 3.3 V for DRV8424 and 2.64V for DRV8425. DVDD can be used to provide VREF through a resistor divider.
M0	16	13	I	Input	Microstepping mode-setting pins. Sets the step mode; internal pulldown resistor.
M1	20	17			
DECAY0	19	16	I	Input	Decay-mode setting pins. Sets the decay mode (see the Decay Modes section).
DECAY1	18	15			

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Table 1. Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
STEP	21	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
VCP	3	24	—	Power	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	4, 11	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
TOFF	17	14	I	Input	Sets the Decay mode off time during current chopping; four level pin. Also sets the ripple current in smart tune ripple control mode.
nFAULT	14	11	O	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	24	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, DECAY0, DECAY1, TOFF, M0, M1)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	33	V
V_I	Logic level input voltage	0	5.5	V
V_{VREF}	VREF voltage (DRV8424)	0.05	3.3	V
V_{VREF}	VREF voltage (DRV8425)	0.05	2.64	V
f_{PWM}	Applied STEP signal (STEP)	0	100 (1)	kHz
I_{FS}	Motor full-scale current (xOUTx) (DRV8424)	0	2.5 (2)	A
I_{FS}	Motor full-scale current (xOUTx) (DRV8425)	0	2 (2)	A
I_{rms}	Motor RMS current (xOUTx) (DRV8424)	0	1.8 (2)	A
I_{rms}	Motor RMS current (xOUTx) (DRV8425)	0	1.4 (2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC (1)		DRV8424/25		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.2	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	18.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
V_{VM}	VM operating voltage	Supply voltage range for normal (DC) operation	4.5		33	V
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	75			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	18		35	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.6	0.9	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.6	0.9	ms
V_{DVDD}	Internal regulator voltage	No external load	4.5	5	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{CP}	VCP operating voltage			V_{VM} + 5		V
$f_{(CP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		400		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{IL}	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage	V_{VM} = 24 V	–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance (DRV8424)	V_{VM} = 24 V, T_J = 25 °C, I_O = -1 A		165	200	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = -1 A		250	300	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = -1 A		280	350	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (DRV8424)	V_{VM} = 24 V, T_J = 25 °C, I_O = 1 A		165	200	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = 1 A		250	300	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = 1 A		280	350	mΩ
$R_{DS(ONH)}$	High-side FET on resistance (DRV8425)	V_{VM} = 24 V, T_J = 25 °C, I_O = -1 A		275	330	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = -1 A		410	500	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = -1 A		460	580	mΩ

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Electrical Characteristics (continued)

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ONL)}$	Low-side FET on resistance (DRV8425)	V_{VM} = 24 V, T_J = 25 °C, I_O = 1 A		275	330	mΩ
		V_{VM} = 24 V, T_J = 125 °C, I_O = 1 A		410	500	mΩ
		V_{VM} = 24 V, T_J = 150 °C, I_O = 1 A		460	580	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain		1.254	1.32	1.386	V/A
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 2.5 A, 10% to 20% current setting	–15		15	%
		I_O = 2.5 A, 20% to 67% current setting	–10		10	
		I_O = 2.5 A, 68% to 100% current setting	–5		5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 2.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.15	4.25	4.35	V
		VM rising, UVLO rising	4.25	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET, DRV8424	4			A
I_{OCP}	Overcurrent protection	Current through any FET, DRV8425	3.2			A
t_{OCP}	Overcurrent deglitch time			1.25		µs
t_{RETRY}	Overcurrent retry time			4		ms
t_{OL}	Open load detection time				50	ms
I_{OL}	Open load current threshold			75		mA
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

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7.6 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500 (1)	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

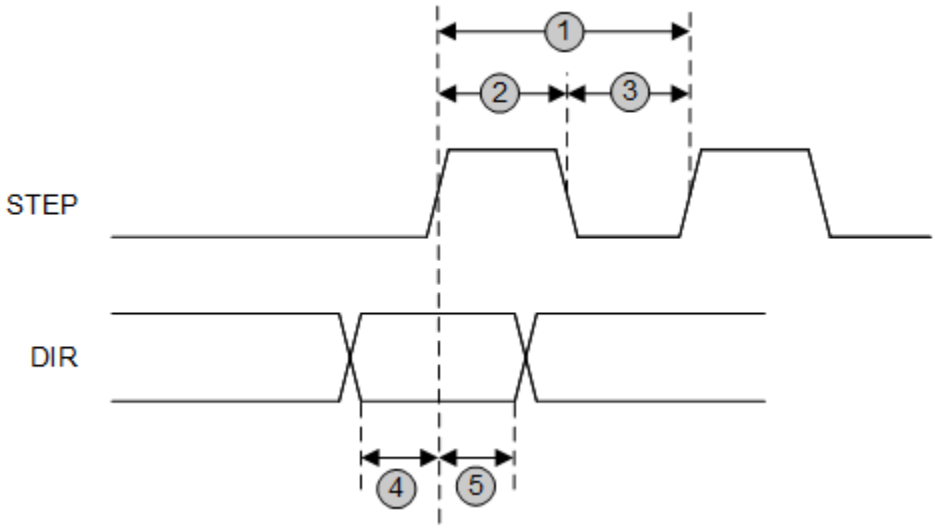


Figure 1. STEP and DIR Timing Diagram

8 Detailed Description

8.1 Overview

The DRV8424/25 devices are integrated motor-driver solutions for bipolar stepper motors. The devices integrate two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8424/25 devices can be powered with a supply voltage from 4.5 to 33 V. The DRV8424 is capable of providing an output current up to 4-A peak, 2.5-A full-scale, or 1.8-A root mean square (rms). The DRV8425 is capable of providing an output current up to 3.2-A peak, 2-A full-scale, or 1.4-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

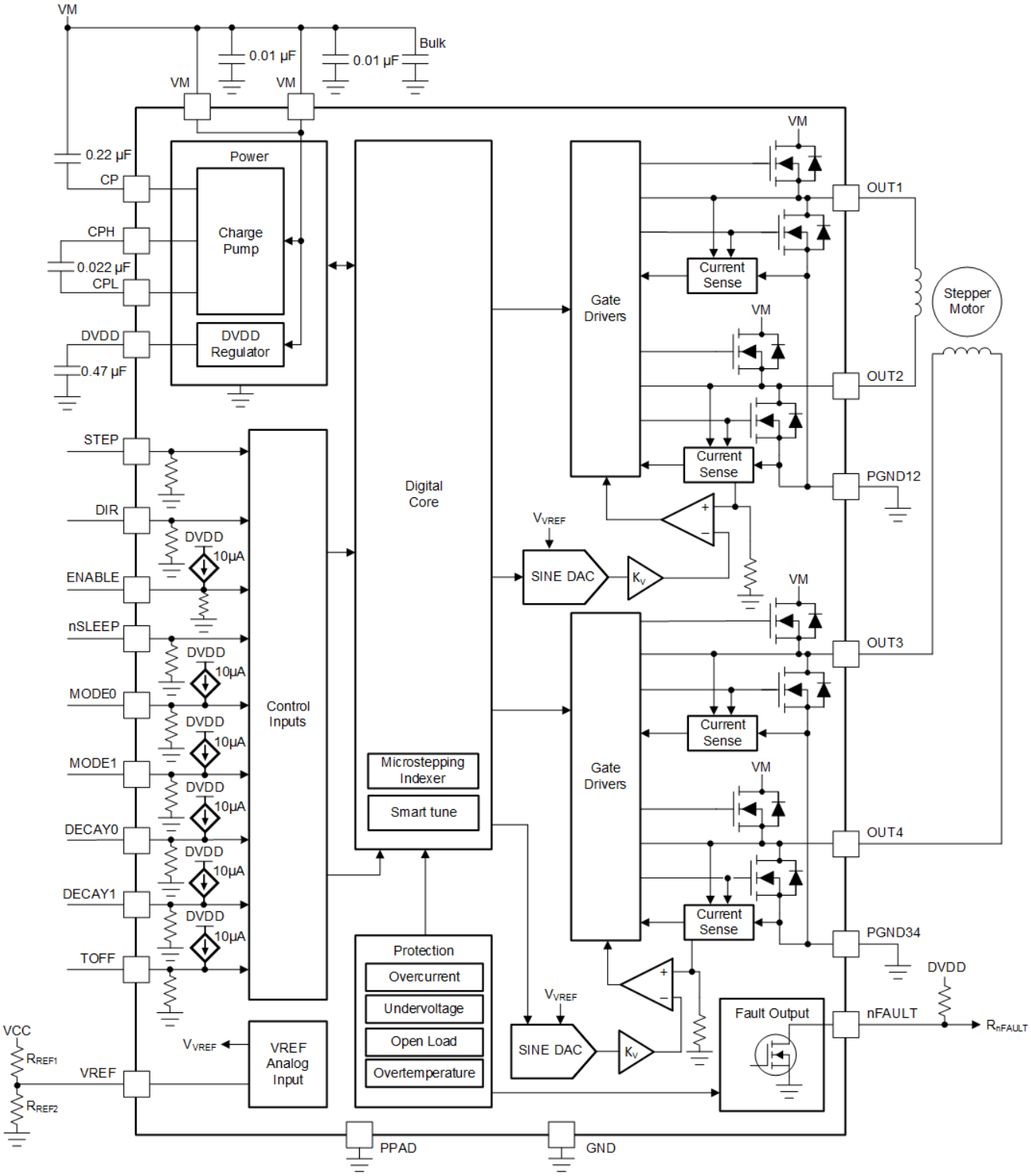
The DRV8424/25 devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin. This features reduces external component cost, board PCB size, and system power consumption.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. In addition to a standard half stepping mode, a non-circular half stepping mode is available for increased torque output at higher motor RPM.

The current regulation is configurable between several decay modes. The decay mode can be selected as a slow-mixed, mixed decay, smart tune Ripple Control, or smart tune Dynamic Decay current regulation scheme. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust for optimal current regulation performance and compensate for motor variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic decay percentage scheme to minimize distortion of the motor winding current while also minimizing frequency content.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

8.2 Functional Block Diagram



8.3 Feature Description

Table 2 lists the recommended external components for the DRV8424/25 devices.

Feature Description (continued)

Table 2. DRV8424/25 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{CP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the DRV8424/25 device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

8.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

8.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8424 device, the peak current rating is 4A per bridge. For the DRV8425 device, the peak current rating is 3.2A per bridge.

8.3.1.2 rms Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8424 device, the rms current rating is 1.8 A per bridge. For the DRV8425 device, the rms current rating is 1.4 A per bridge.

8.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$. For the DRV8424 device, the full-scale current rating is 2.5 A per bridge. For the DRV8425 device, the full-scale current rating is 2 A per bridge.

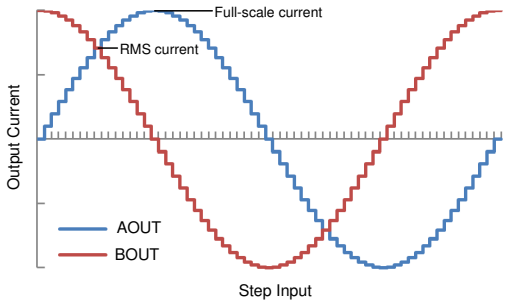


Figure 2. Full-Scale and RMS Current

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8.3.2 PWM Motor Drivers

The DRV8424/25 devices have drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 3 shows a block diagram of the circuitry.

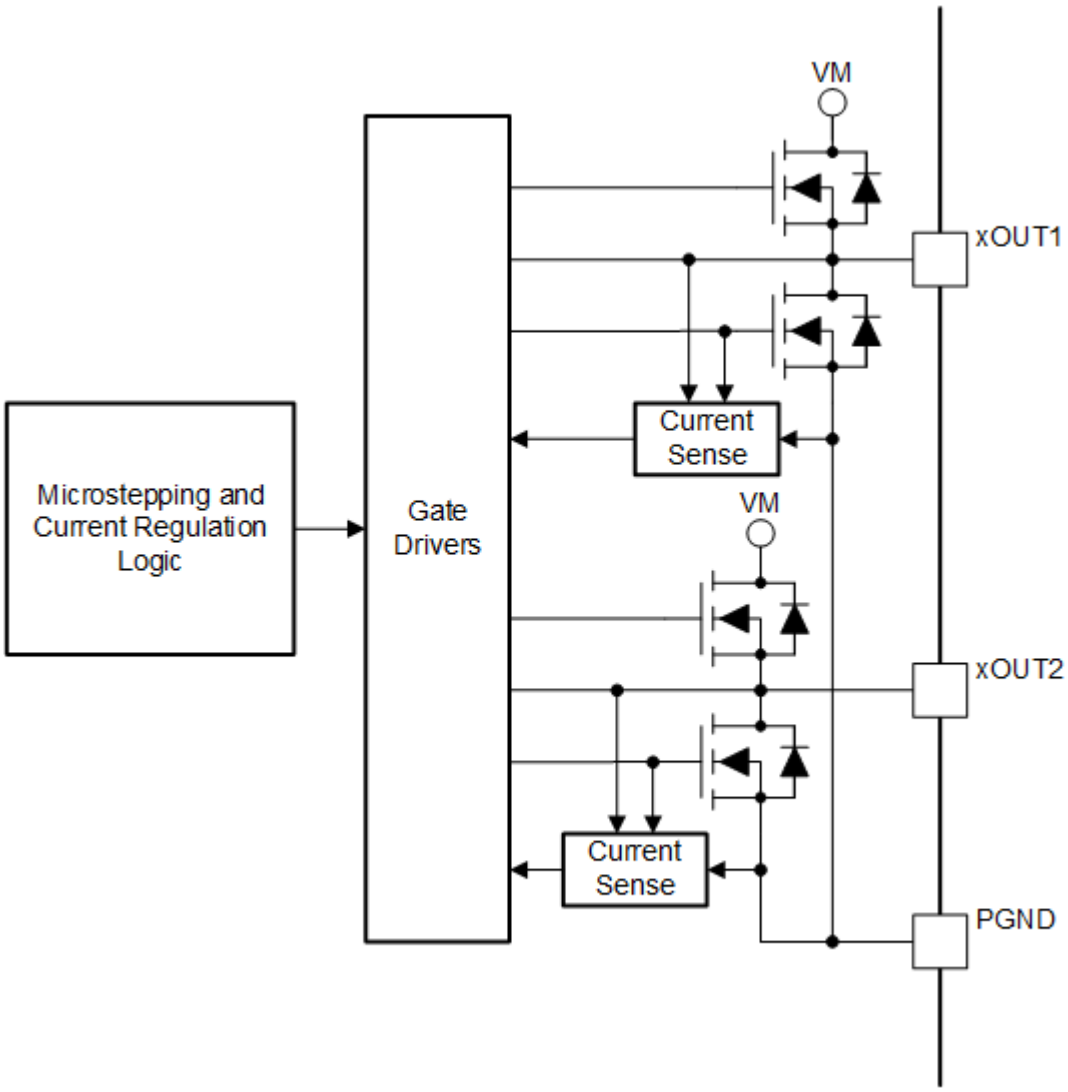

Figure 3. PWM Motor Driver Block Diagram

8.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8424/25 devices allow a number of different step modes. The M0 and M1 pins are used to configure the step mode as shown in Table 3. The settings can be changed on the fly.

Table 3. Microstepping Settings

M0	M1	STEP MODE
0	330kΩ to GND	Full step (2-phase excitation) with 100% current
0	0	Full step (2-phase excitation) with 71% current
Hi-Z	1	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step

Table 3. Microstepping Settings (continued)

M0	M1	STEP MODE
0	Hi-Z	1/8 step
1	0	1/16 step
1	1	1/32 step
Hi-Z	Hi-Z	1/64 step
1	330kΩ to GND	1/128 step
1	Hi-Z	1/256 step

Table 4 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

NOTE

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 4. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75

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Table 4. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 5 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 5. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	-100	100	135
3	-100	-100	225
4	100	–100	315

Table 6 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 6. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

8.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3V for DRV8424 and 2.64V for DRV8425.

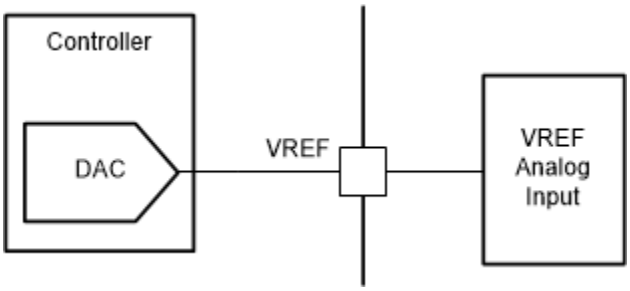

Figure 4. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

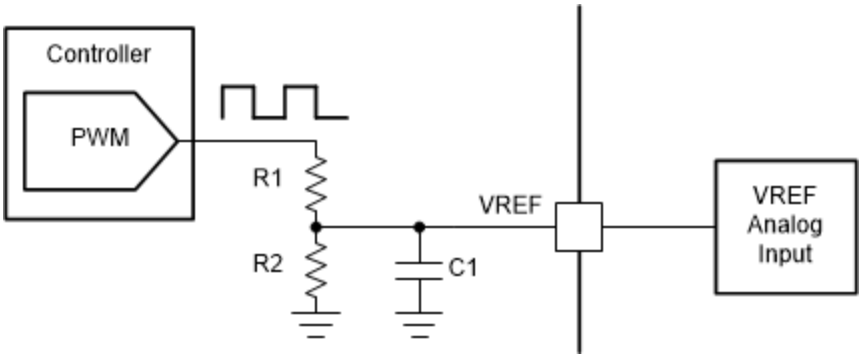

Figure 5. Controlling VREF With a PWM Resource

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8.3.5 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

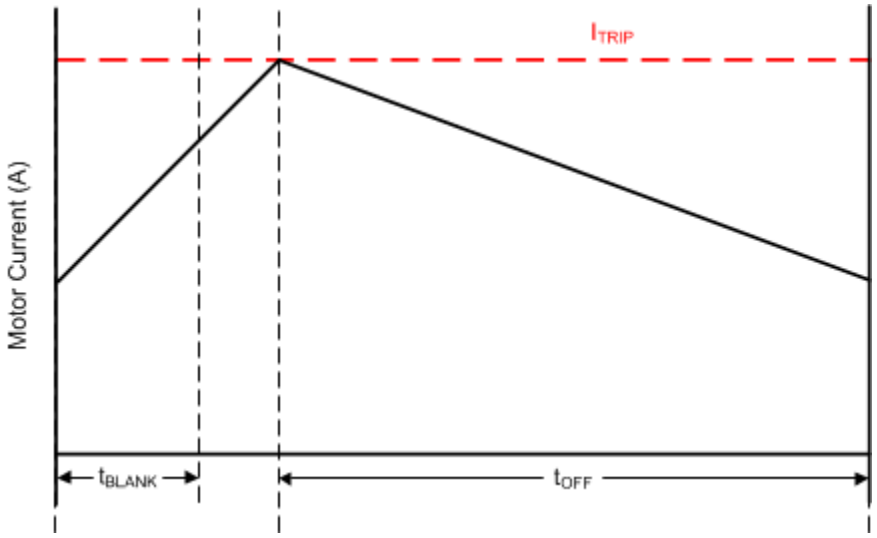

Figure 6. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin.

The full-scale regulation current (I_{FS}) can be calculated as I_{FS} (A) = V_{REF} (V) / K_V (V/A) = V_{REF} (V) / 1.32 (V/A).

8.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7, Item 3.

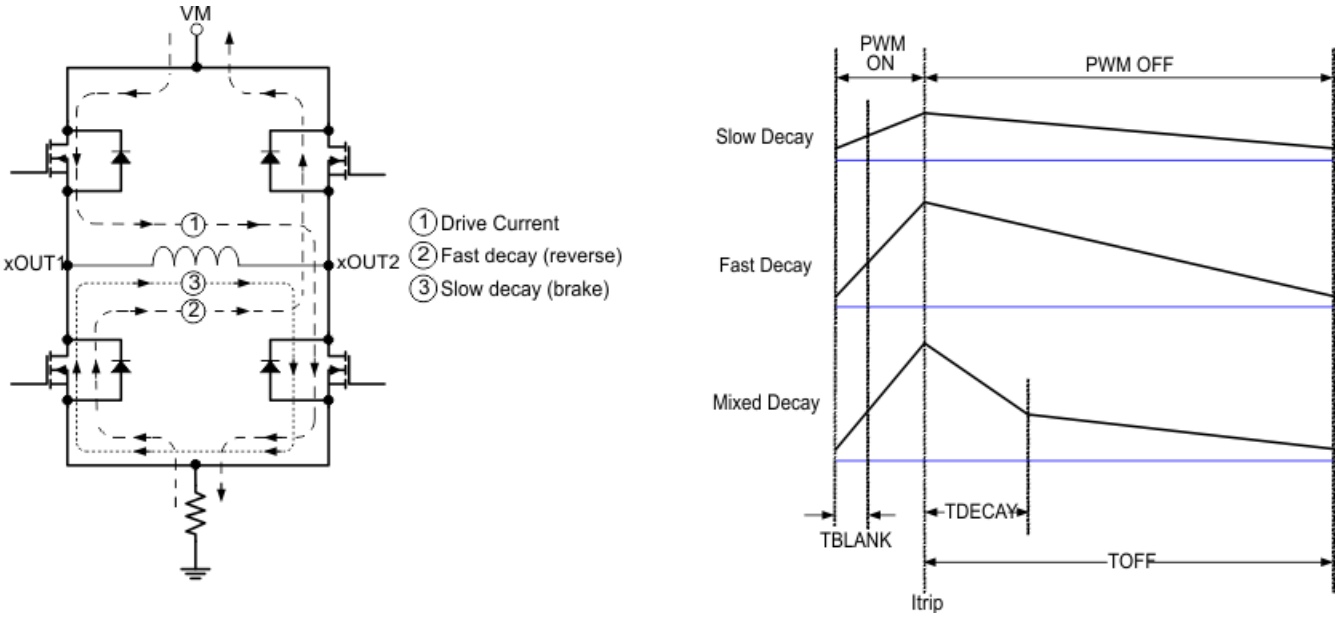

Figure 7. Decay Modes

The decay mode of the DRV8424/25 is selected by the DECAY0 and DECAY1 pins as shown in Table 7. If DECAY1 pin is Hi-Z, irrespective of the DECAY0 pin voltage, the decay mode will be smart tune dynamic decay. The decay modes can be changed on the fly. After a decay mode change, the new decay mode is applied after a 10 µs de-glitch time.

Table 7. Decay Mode Settings

DECAY0	DECAY1	INCREASING STEPS	DECREASING STEPS
0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
0	1	Smart tune Ripple Control	Smart tune Ripple Control
1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
1	1	Slow decay	Mixed decay: 30% fast
Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
Hi-Z	1	Slow decay	Slow decay

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Figure 8 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

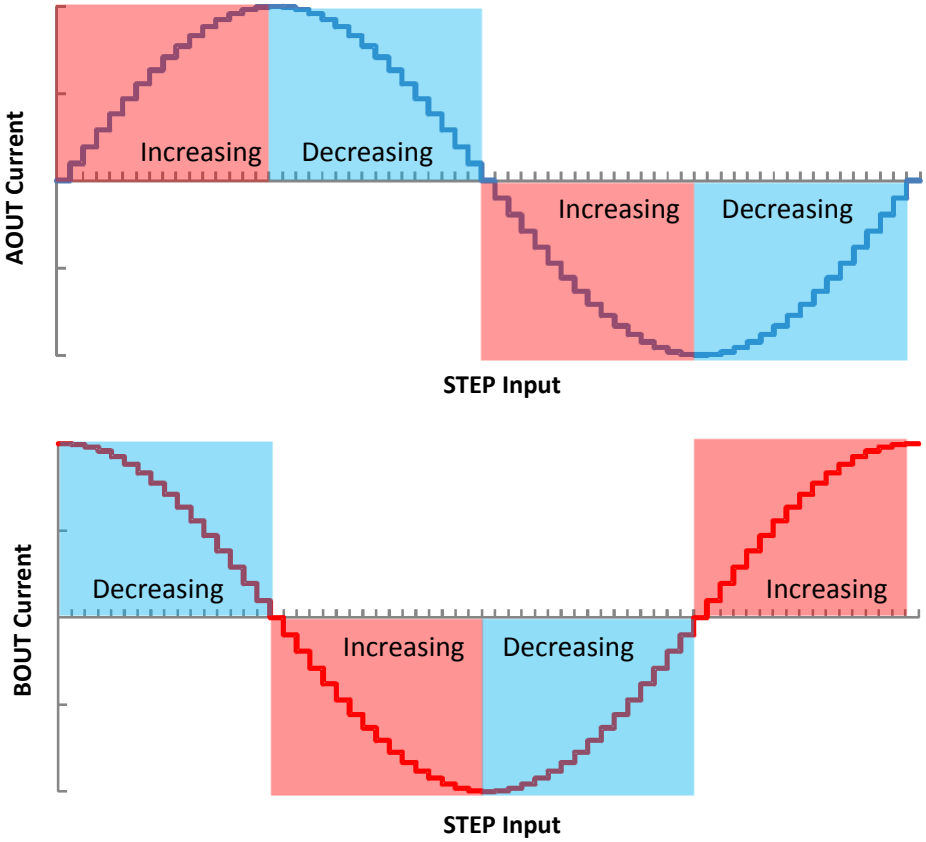

Figure 8. Definition of Increasing and Decreasing Steps

8.3.6.1 Slow Decay for Increasing and Decreasing Current

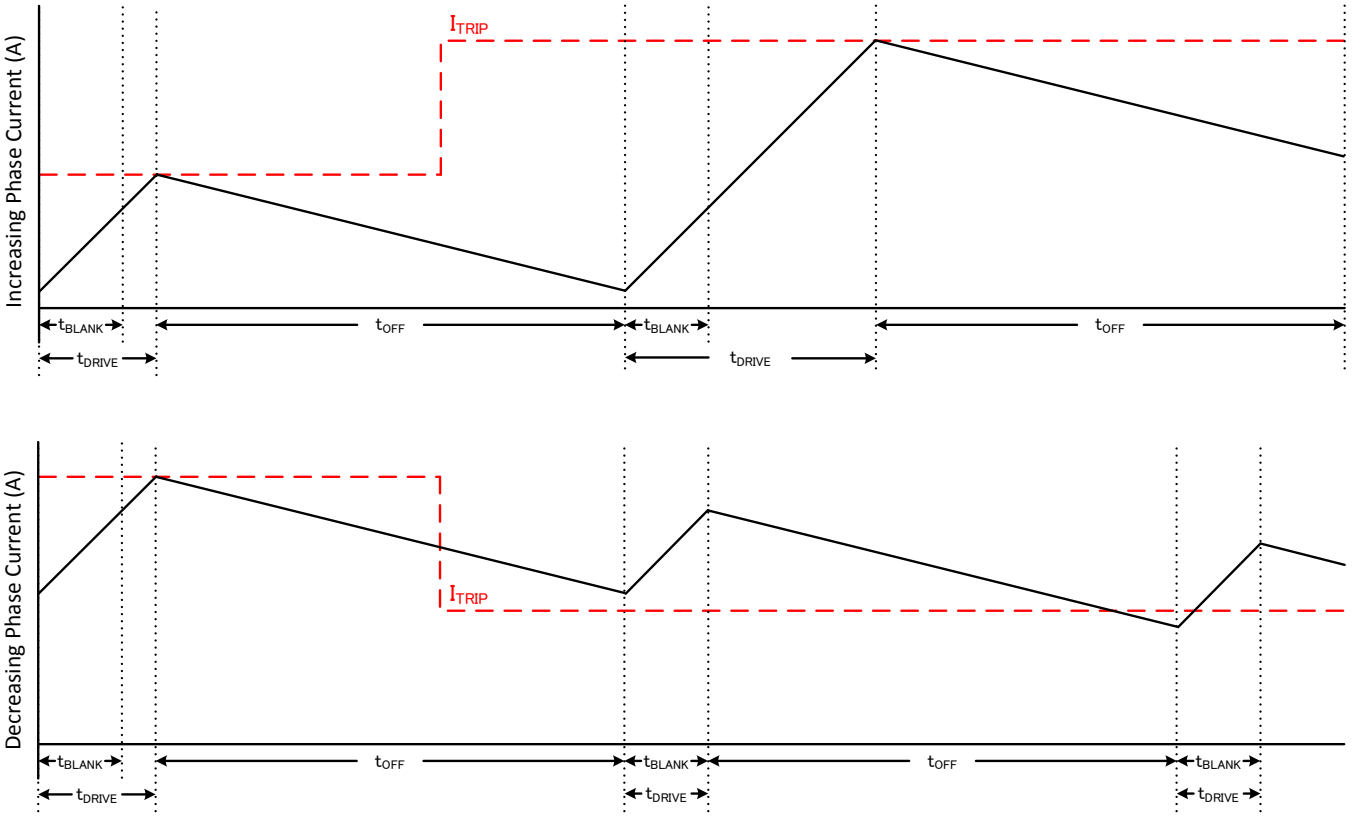

Figure 9. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new ITRIP level because the current decreases very slowly. If the current at the end of the off time is above the ITRIP level, slow decay will be extended for another off time duration and so on, till the current at the end of the off time is below ITRIP level.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

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8.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

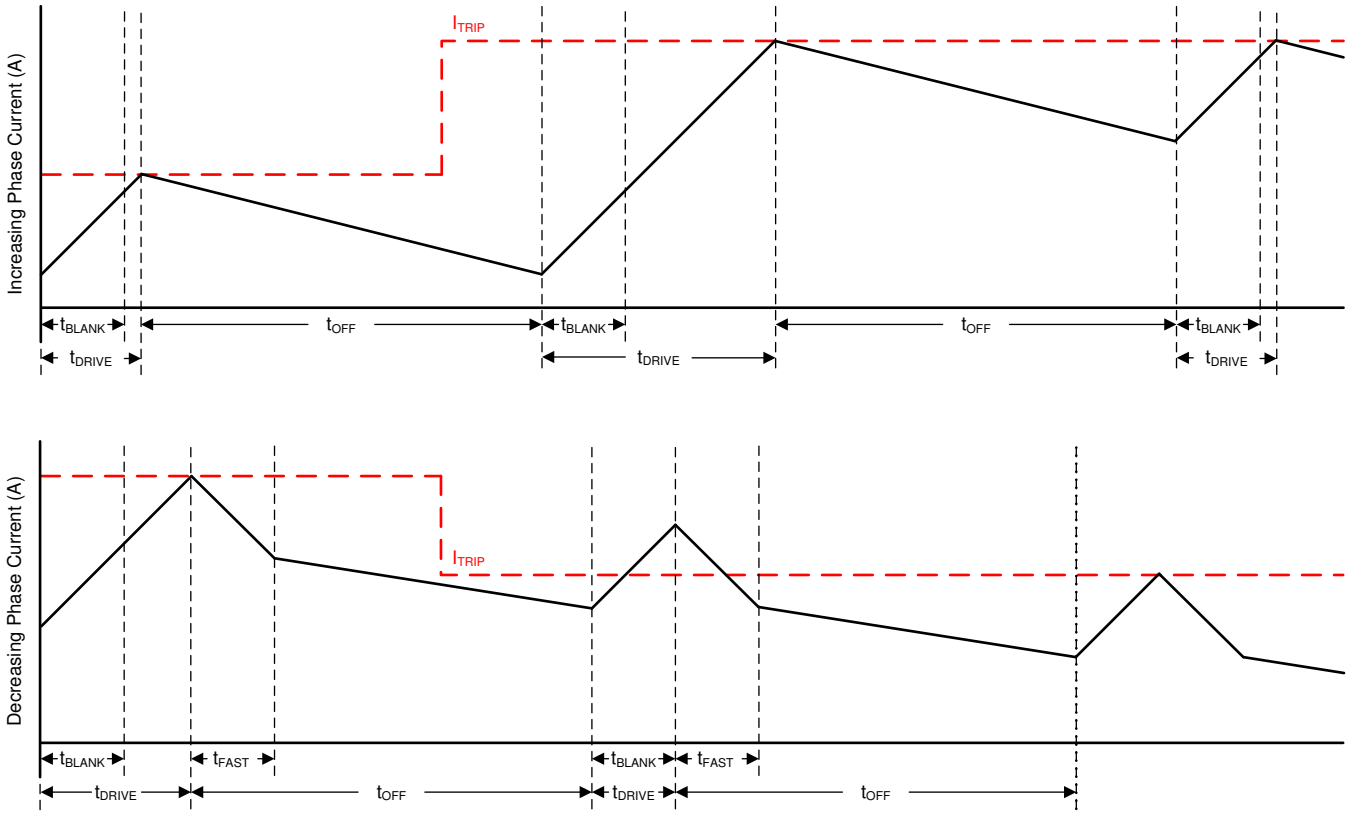

Figure 10. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

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8.3.6.3 Mixed Decay for Increasing and Decreasing Current

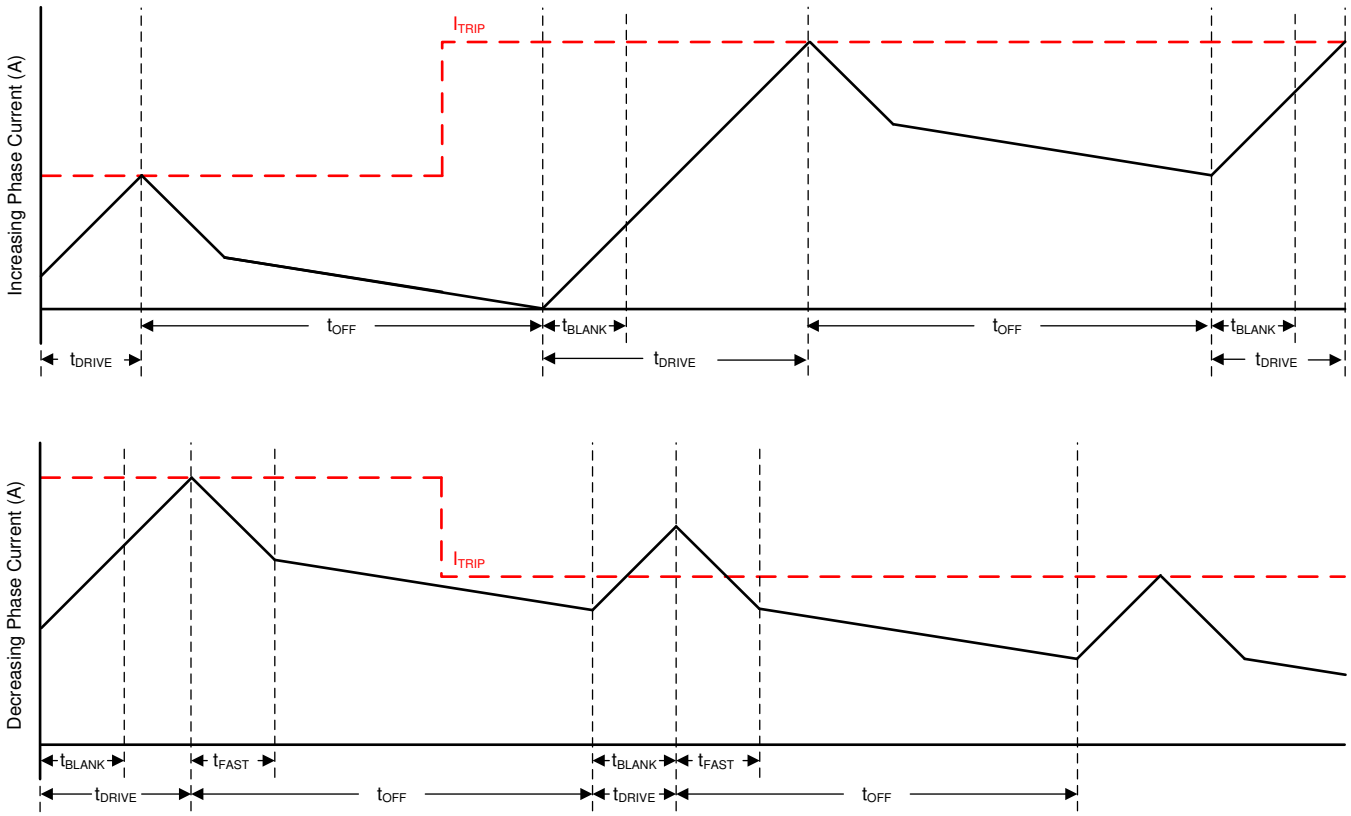

Figure 11. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

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8.3.6.4 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

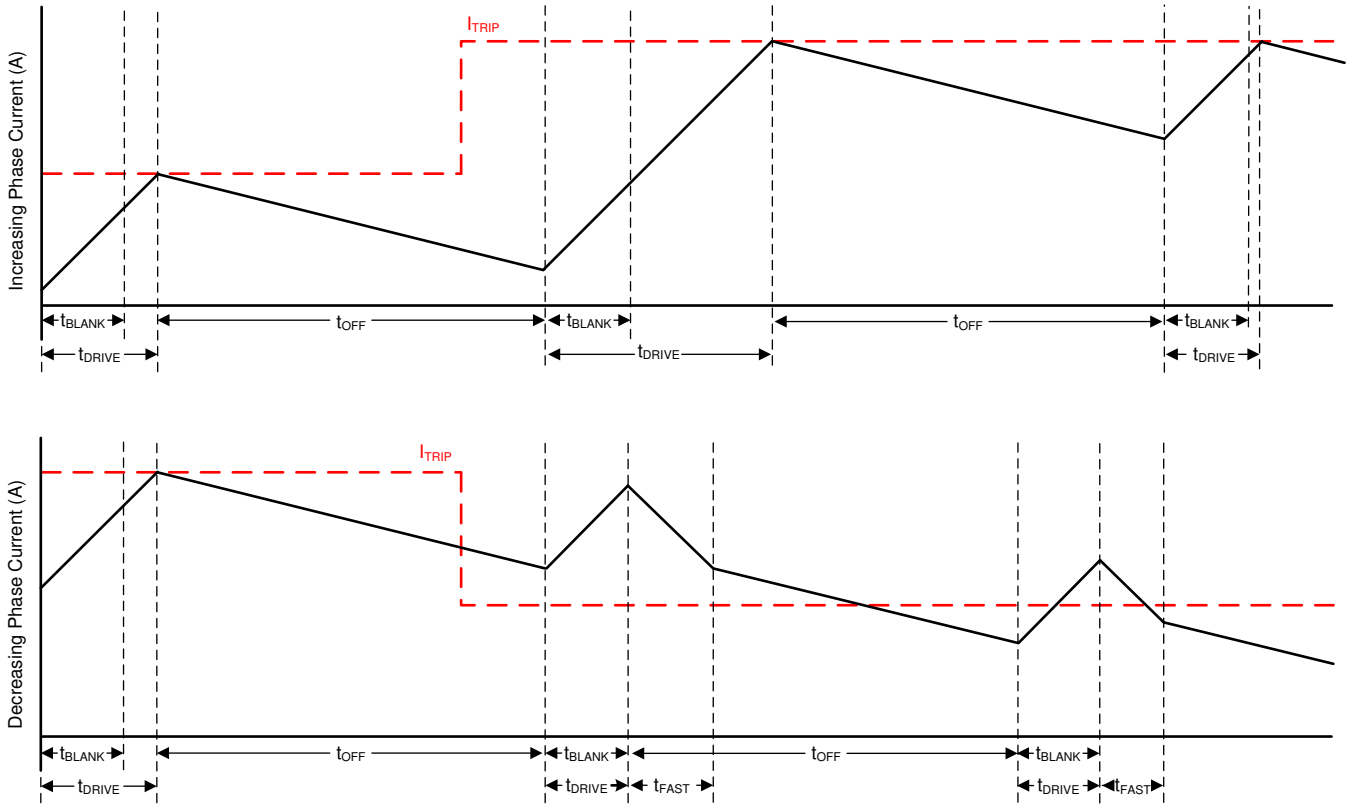

Figure 12. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

8.3.6.5 Smart tune Ripple Control

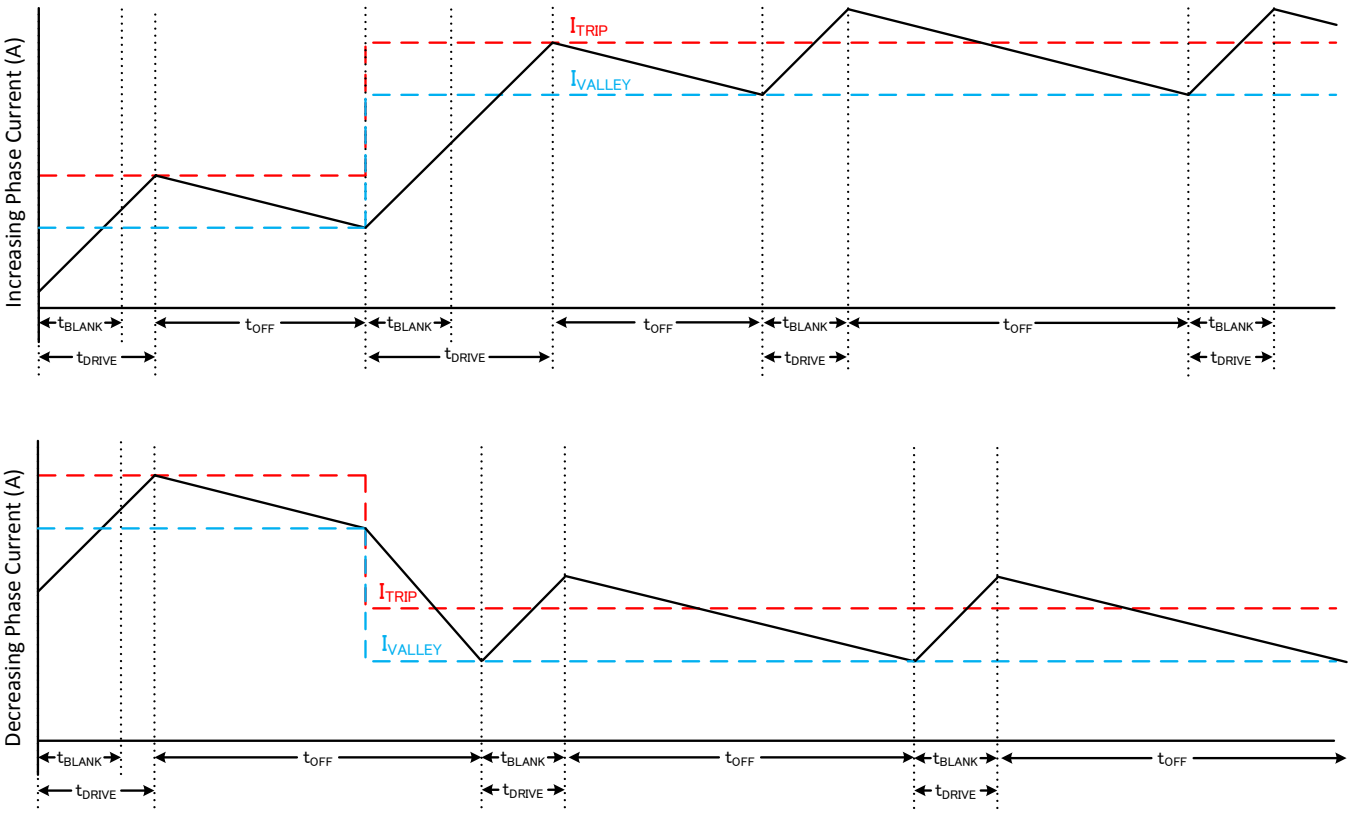

Figure 13. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

The ripple current in this decay mode is programmed by the TOFF pin. The ripple current is dependent on the ITRIP of a particular microstep level.

Table 8. Current Ripple Settings

TOFF	Current Ripple at a specific microstep level
0	11mA + 1% of ITRIP
1	11mA + 2% of ITRIP
Hi-Z	11mA + 4% of ITRIP
330kΩ to GND	11mA + 6% of ITRIP

The ripple control method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation. Select a low ripple current setting to ensure that the PWM frequency is not in the audible range.

8.3.6.6 PWM OFF Time

The TOFF pin configures the PWM OFF time, as shown in Table 7. The OFF time settings can be changed on the fly. After a OFF time setting change, the new OFF time is applied after a 10 µs de-glitch time.

Table 9. OFF Time Settings

TOFF	OFF Time
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

8.3.6.7 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

8.3.7 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

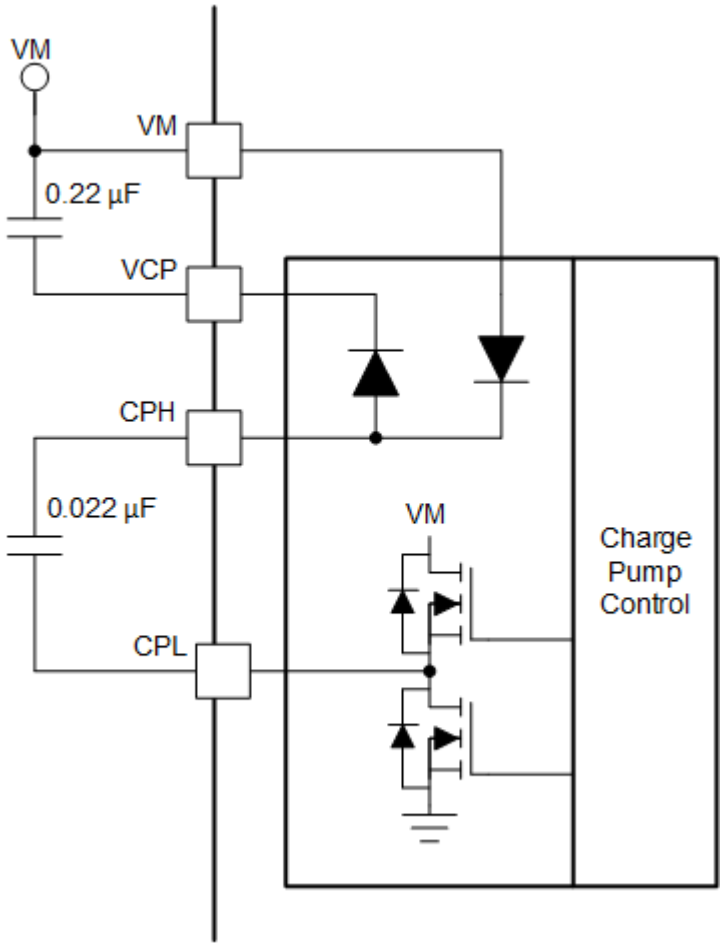

Figure 14. Charge Pump Block Diagram

8.3.8 Linear Voltage Regulators

A linear voltage regulator is integrated in the DRV8424/25 devices. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2mA, the output voltage drops significantly.

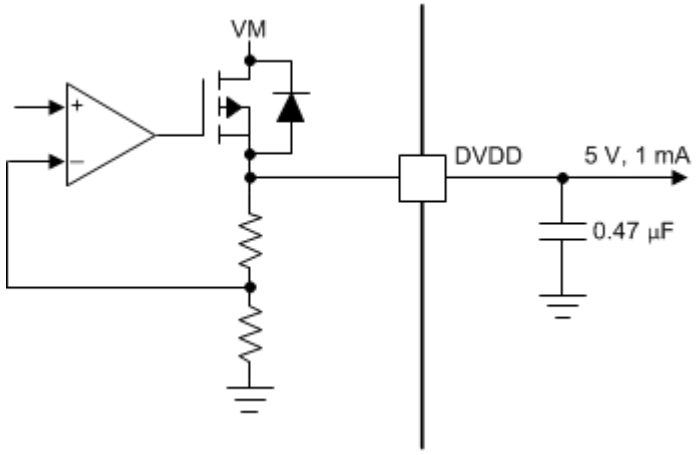

Figure 15. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, Mx, DECAYx or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

8.3.9 Logic Level, tri-level and quad-level Pin Diagrams

Figure 16 shows the input structure for M0, DECAY0, DECAY1 and ENABLE pins.

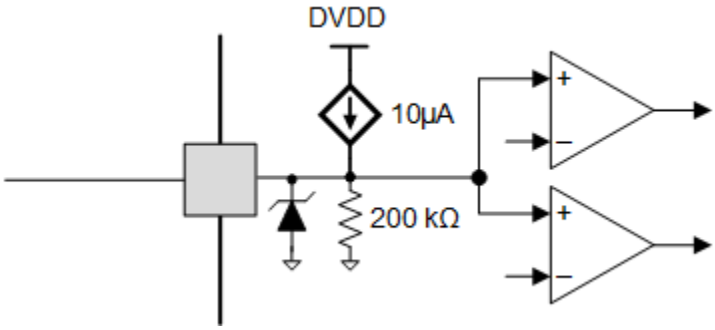

Figure 16. Tri-Level Input Pin Diagram

Figure 16 shows the input structure for M1 and TOFF pins.

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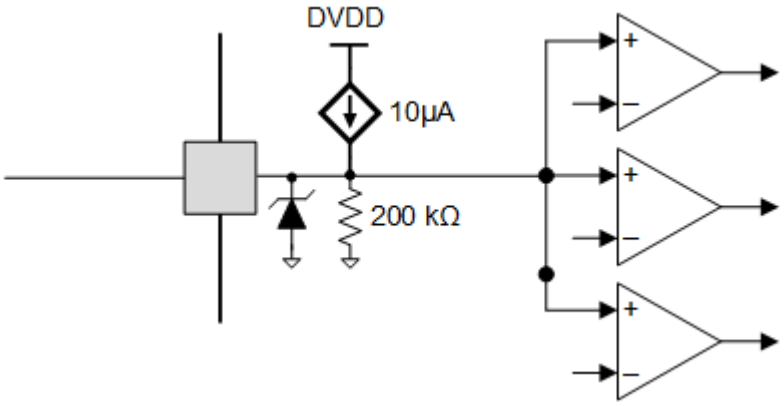

Figure 17. Quad-Level Input Pin Diagram

Figure 18 shows the input structure for STEP, DIR and nSLEEP pins.

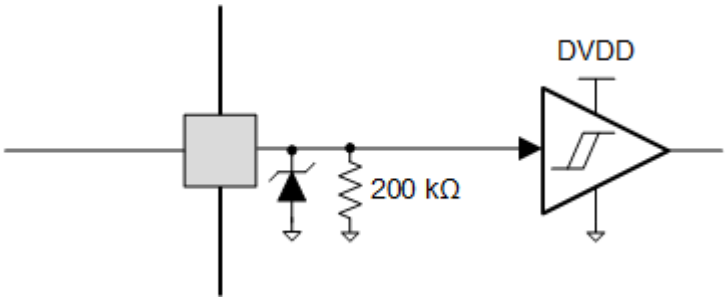

Figure 18. Logic-Level Input Pin Diagram

8.3.9.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V pullup, an external 3.3-V supply must be used.

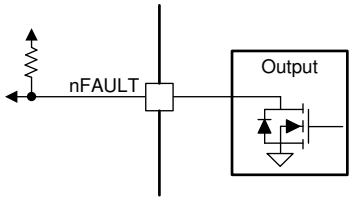

Figure 19. nFAULT Pin

8.3.10 Protection Circuits

The DRV8424/25 devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events.

8.3.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

8.3.10.2 CP Undervoltage Lockout (CPUV)

If at any time the voltage on the CP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the CP undervoltage condition is removed.

8.3.10.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in both H-bridges are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

8.3.10.3.1 Latched Shutdown

The ENABLE pin of the DRV8424/25 has to be made Hi-Z to select latched shutdown mode. In this mode, after an OCP event, the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes after nSLEEP cycling or a power cycling.

8.3.10.3.2 Automatic Retry

The ENABLE pin of the DRV8424/25 has to be connected to DVDD to select automatic retry mode. In this mode, after an OCP event the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

Errata: For the prototype samples, all output nodes are pulled high when the device enters sleep mode, until VCP discharges below V_{CPUV}. Ensure that the output nodes are not shorted to ground when nSLEEP is pulled low. This behavior will be corrected in the production samples – all output nodes will be Hi-Z when nSLEEP goes low.

8.3.10.4 Open-Load Detection (OL)

If the winding current in any coil drops below the open load current threshold (I_{OL}) and the I_{TRIP} level set by the indexer, and if this condition persists for more than the open load detection time (t_{OL}), an open-load condition is detected. Normal operation resumes and the nFAULT line is released when the open load condition is removed and a clear faults command has been issued through an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode.

8.3.10.5 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled during this condition. The thermal shutdown protection can operate in two different modes: latched shutdown and automatic retry.

8.3.10.5.1 Latched Shutdown

The ENABLE pin of the DRV8424/25 has to be made Hi-Z to select latched shutdown mode. In this mode, after an OTSD event, the relevant outputs are disabled and the nFAULT pin is driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after nSLEEP cycling or a power cycling.

8.3.10.5.2 Automatic Retry

The ENABLE pin of the DRV8424/25 has to be connected to DVDD to select automatic retry mode. In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

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Table 10. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
CP undervoltage (CPUV)	CP < V_{CPUV}	—	nFAULT	Disabled	Operating	Operating	Operating	CP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	ENABLE = Hi-Z	nFAULT	Disabled	Operating	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	—	nFAULT	Operating	Operating	Operating	Operating	Report only
Thermal Shutdown (OTSD)	T_J > T_{TSD}	ENABLE = Hi-Z	nFAULT	Disabled	Disabled	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

8.4 Device Functional Modes

8.4.1 Sleep Mode (nSLEEP = 0)

The DRV8424/25 device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the DRV8424/25 device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The DRV8424/25 device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

8.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the DRV8424/25 device. When the ENABLE pin is low, the output drivers are disabled in the Hi-Z state.

8.4.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

8.4.4 nSLEEP Reset Pulse

A latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 18 µs and shorter than 35 µs. If nSLEEP is low for longer than 35 µs but less than 75 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 20). This reset pulse does not affect the status of the charge pump or other functional blocks.

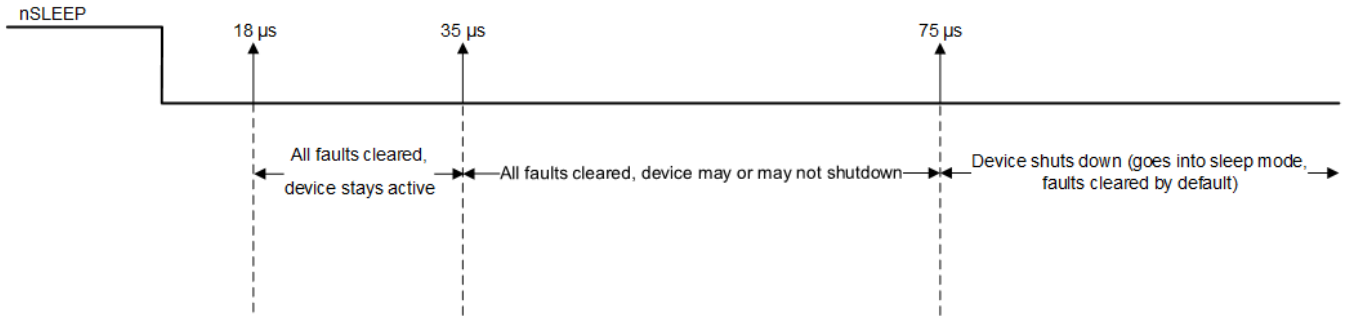

Figure 20. nSLEEP Reset Pulse

Table 11 lists a summary of the functional modes.

Device Functional Modes (continued)

Table 11. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 33 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 33 V	nSLEEP pin = 1 ENABLE pin = 1 or Hi-Z	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 33 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

9 Device and Documentation Support

9.1 Device Support (Optional)

9.1.1 Development Support (Optional)

9.1.2 Device Nomenclature (Optional)

9.2 Documentation Support (if applicable)

9.2.1 Related Documentation

For related documentation see the following:

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9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

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