**Digital Logic Design**

**Report (CSE20221-LAB NO 4)**

**2 March 2016**

**Submitted By -**

**Group 27**

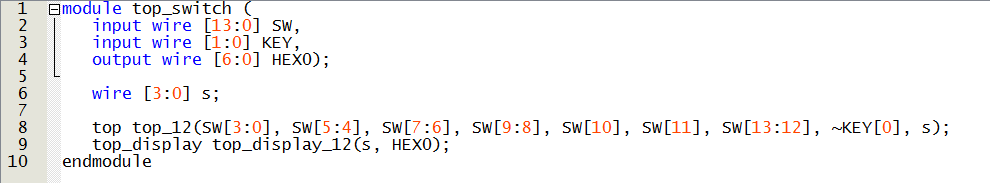
**Joseph P. Lacher**

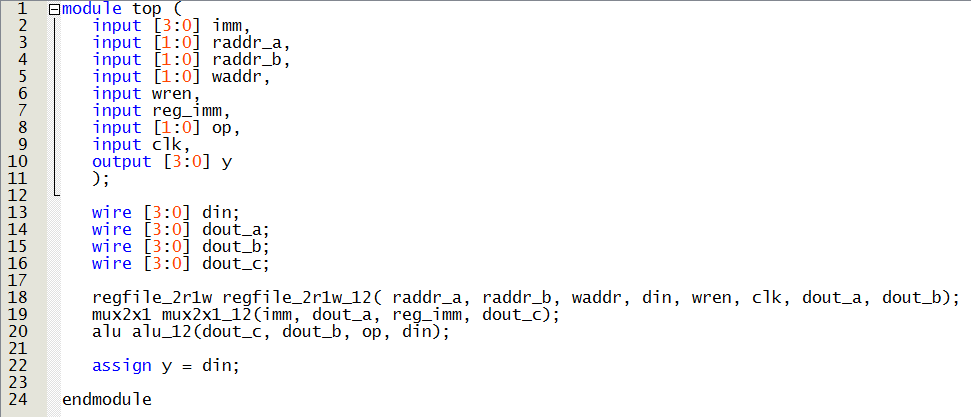
**Alex Brizius**

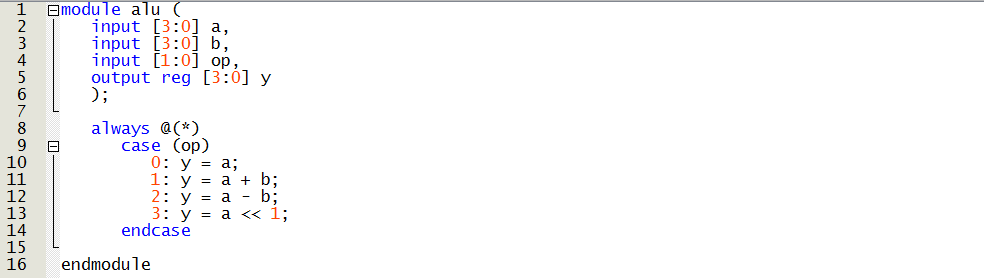
**Michael Burke**

**Terrence Clines**

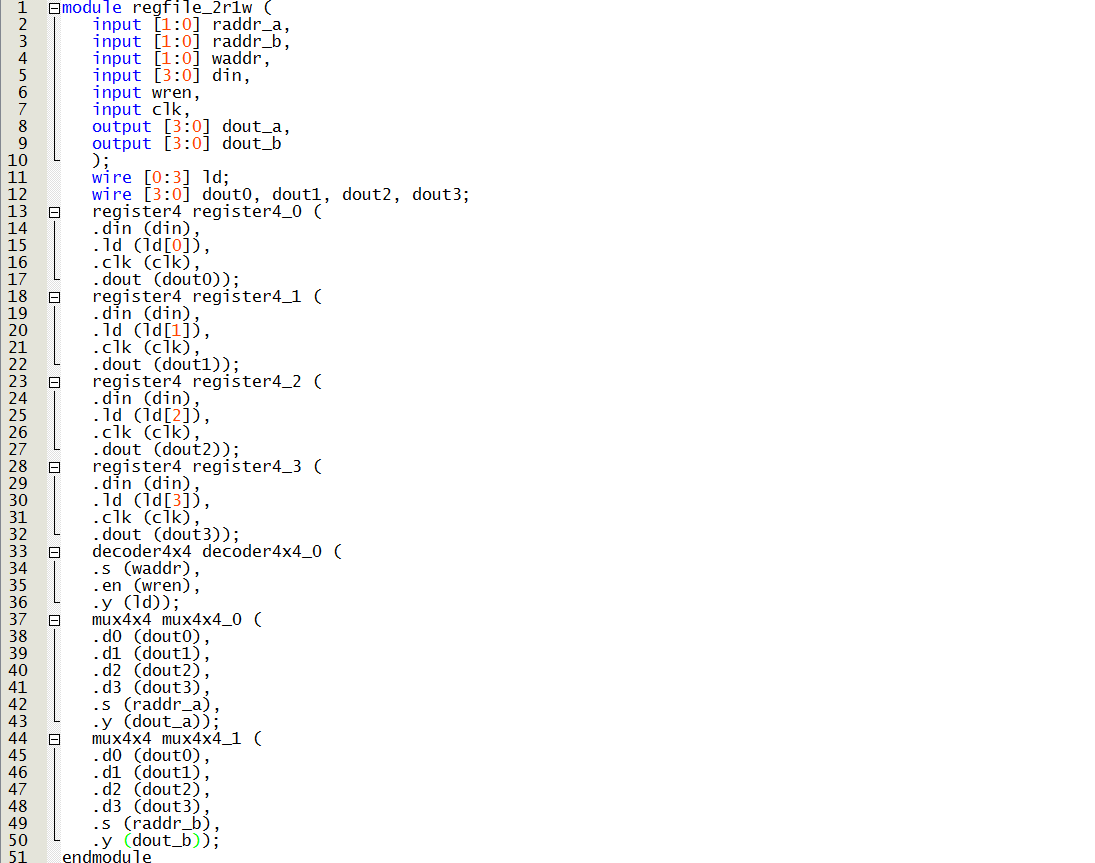
**Your complete code for Task 3:**



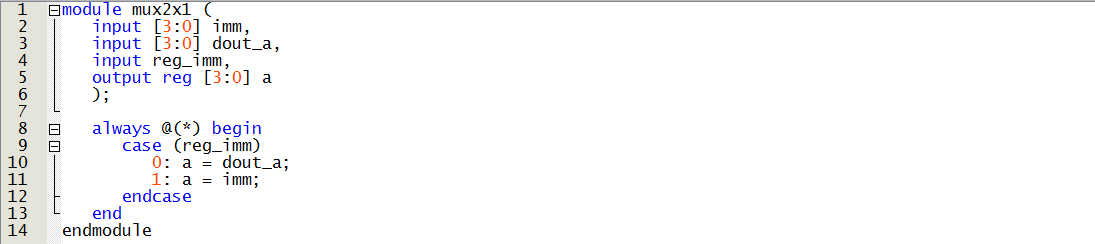


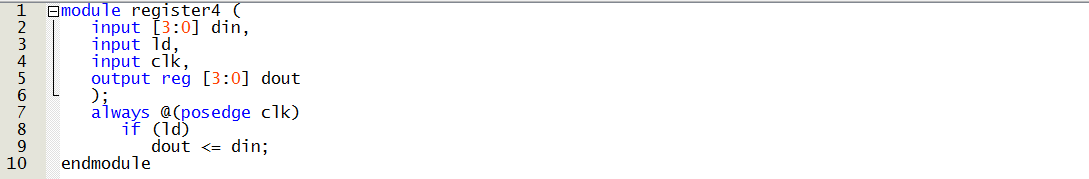


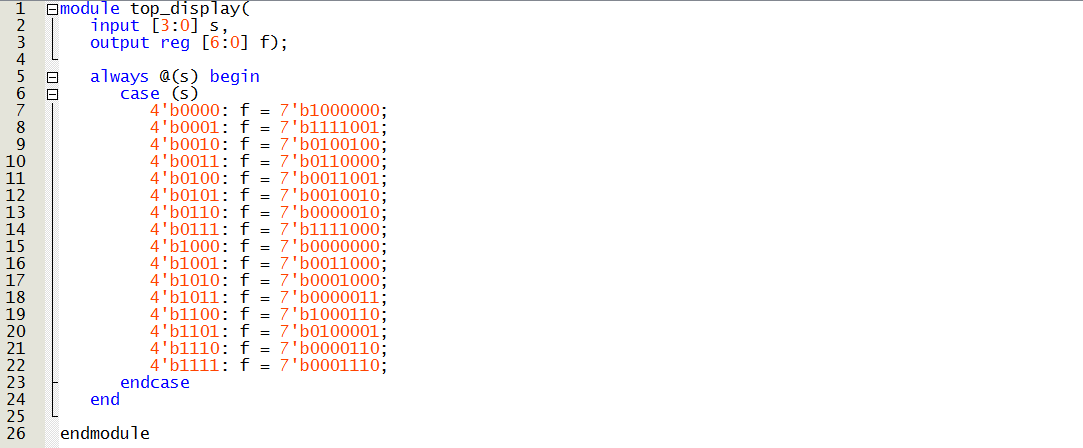


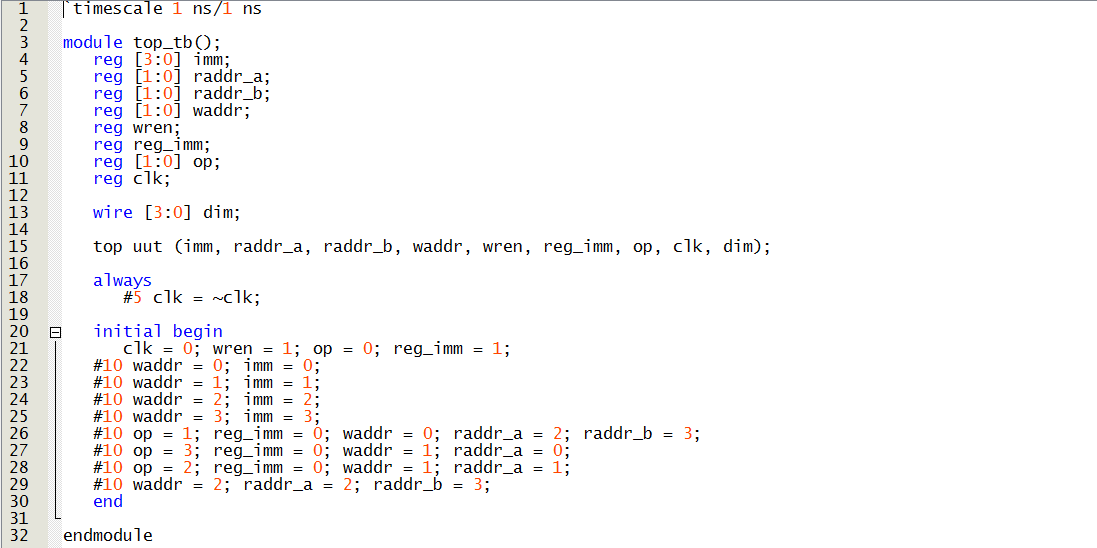












**Screenshot of simulation waveforms for Task 3:**

