**Digital Logic Design**

**Report (CSE20221-LAB NO 7)**

**31 March 2016**

**Submitted By -**

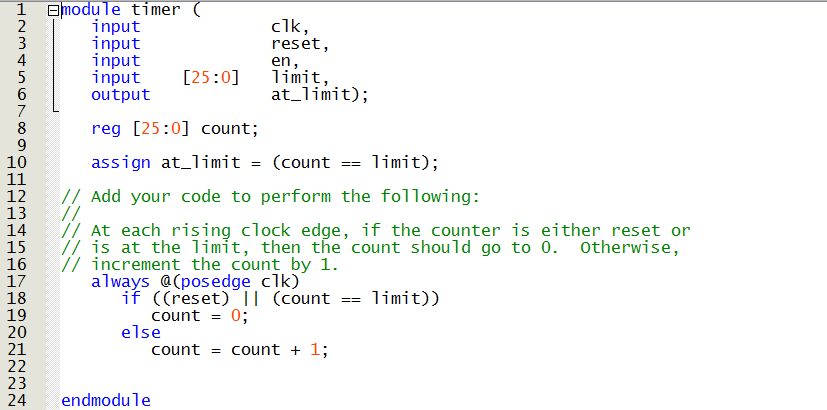
**Group 27**

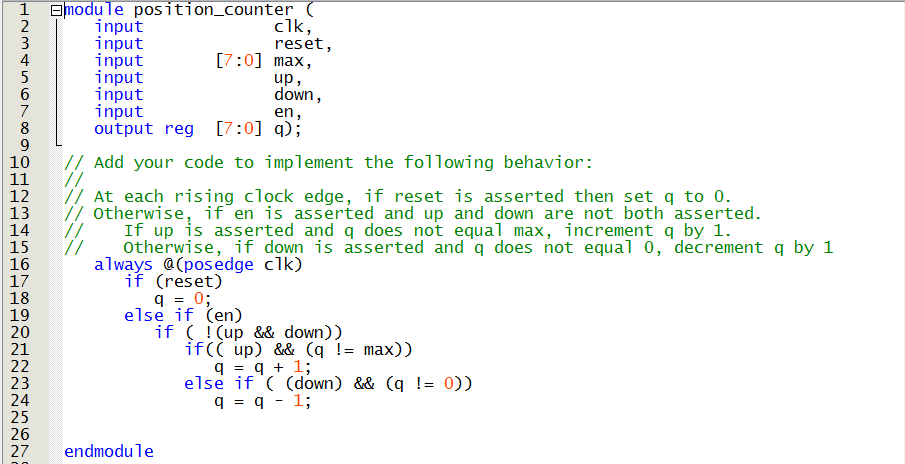
**Joseph P. Lacher**

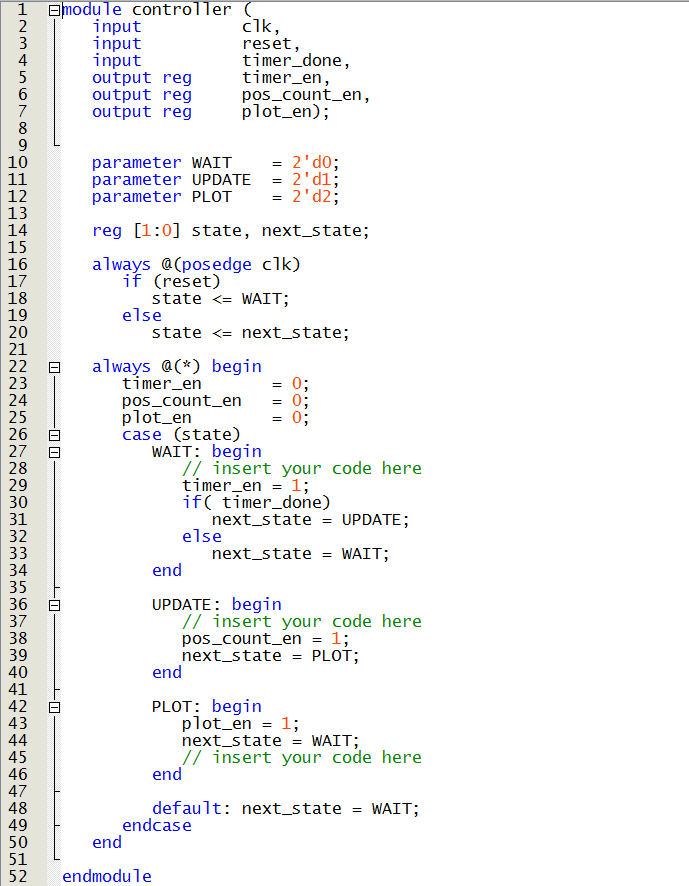
**Alex Brizius**

**Michael Burke**

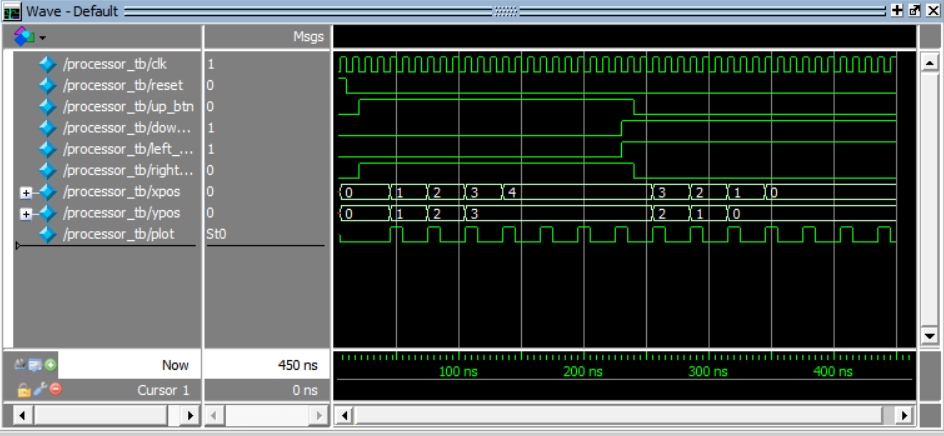
**Your complete code for Task 3:**







**Screenshot of simulation waveforms for Task 3:**



**Photo of Working Program:**

