**Digital Logic Design**

**Report (CSE20221-LAB NO 1)**

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**Submitted By -**

**Group 27**

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**Your complete code for Task 3:**

Task 3 called for the creation of a Verilog System to model the equation F = (1(1+2))’((1+2)+2) which simplifies to the equation F = a’b.

module nota\_b(

input a,

input b,

output f\_structural,

output f\_always);

nota\_b\_structural nota\_b\_structural\_0 (a, b, f\_structural);

nota\_b\_always nota\_b\_always\_0 (a, b, f\_always);

endmodule

module nota\_b\_structural (

input a,

input b,

output f

);

wire n0;

not(n0, a);

and(f, n0, b);

endmodule

module nota\_b\_always (

input a,

input b,

output reg f);

always @(a, b) begin

f = (~a & b);

end

endmodule

`timescale 1 ns/1 ns

module nota\_b\_all\_tb();

reg a;

reg b;

wire f\_structural;

wire f\_always;

nota\_b uut(a, b, f\_structural, f\_always);

initial begin

a = 0; b = 0;

#10 a = 0; b = 1;

#10 a = 1; b = 0;

#10 a = 1; b = 1;

#10;

end

endmodule

module nota\_b\_switch(

input wire SW0,

input wire SW1,

output LED\_RED0 );

nota\_b\_always nota\_b\_12(SW0, SW1, LED\_RED0);

endmodule

**Screenshot of simulation waveforms for Task 3**

