**Digital Logic Design**

**Report (CSE20221-LAB NO 2)**

**3 February 2016**

**Submitted By -**

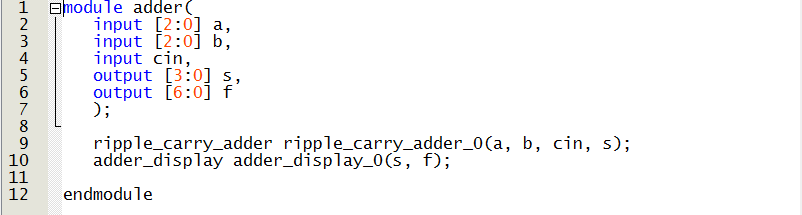
**Group 27**

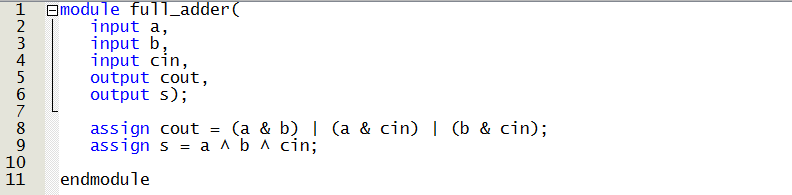
**Joseph P. Lacher**

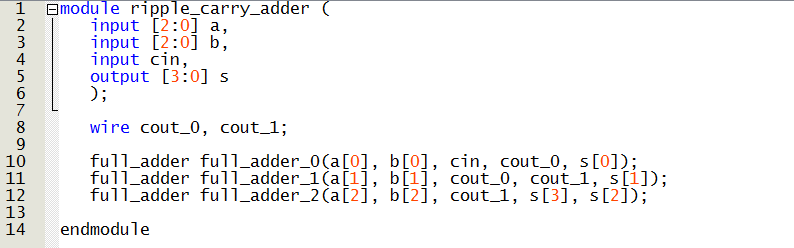
**Alex Brizius**

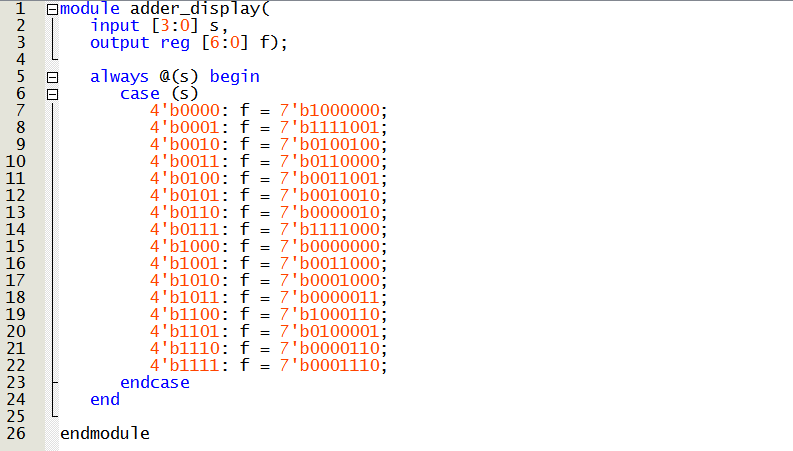
**Michael Burke**

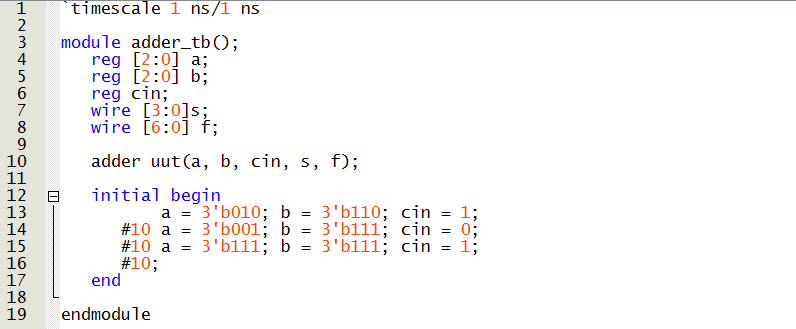
**Your complete code for Task 3:**

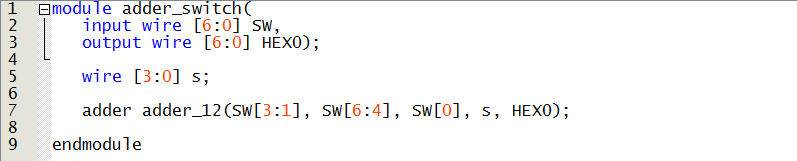












**Screenshot of simulation waveforms for Task 3**

