**Digital Logic Design**

**Report (CSE20221-LAB NO 3)**

**17 February 2016**

**Submitted By -**

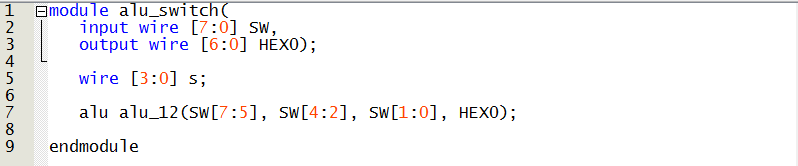
**Group27**

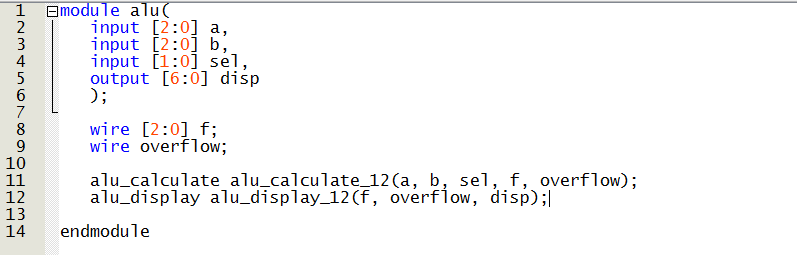
**J. Patrick Lacher**

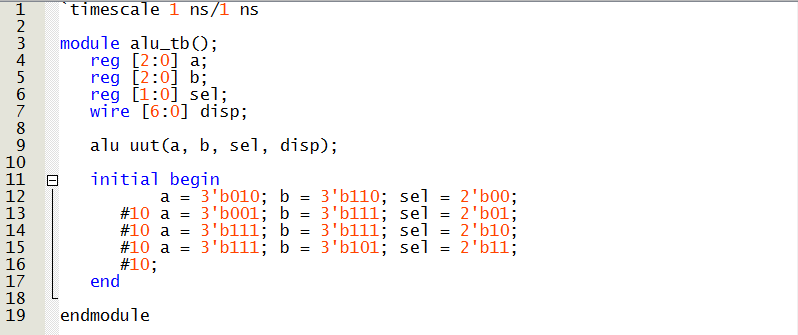
**Alex Brizius**

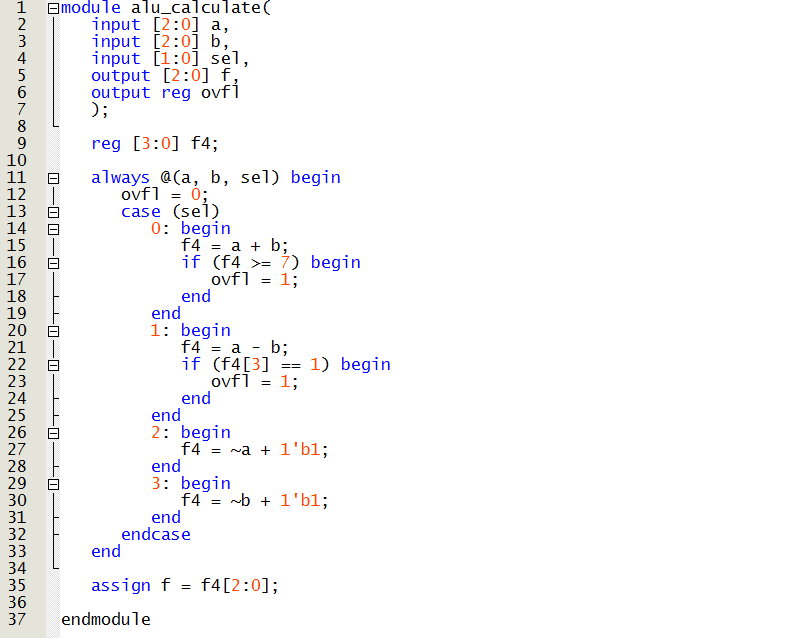
**Michael Burke**

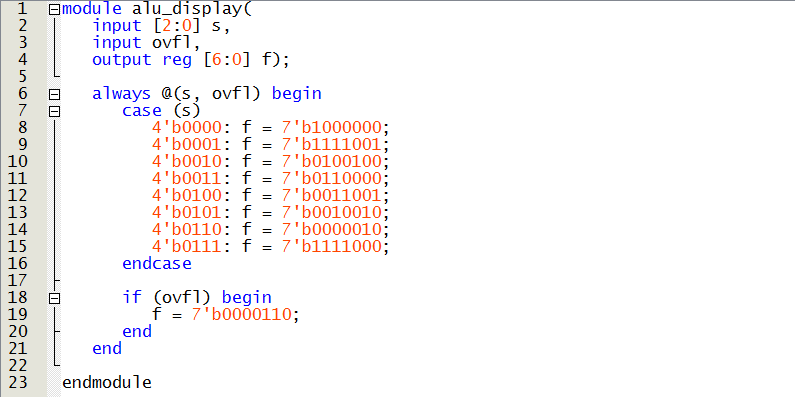
**Your complete code for Task 3:**











**Screenshot of simulation waveforms for Task 3**

