TECHNISCHE UNIVERSITÄT DRESDEN

Fakultät Informatik Institut für Systemarchitektur, Professur für Betriebssysteme

Master's Thesis Topic

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Topic:	Simulation of a Scheduling Algorithm for DAG-based Task Models

Driven by the trend towards manycores, an increasing number of applications is developed with parallelism in mind. Asynchronous programming paradigms based on lambdas are used to simplify the expression of parallelism within an algorithm. The dependencies between those individual work items allow the modeling of an application's parallel nature with a directed acyclic graph (DAG).

State-of-the art scheduling algorithms however still model parallelism with opaque threads and therefore cannot benefit from the additional insight available from a DAG-based task description. This thesis should explore DAG-based task scheduling by developing a simulator that allows to experiment with different DAG representations of tasks and corresponding scheduling algorithms.

As a first step, a survey of existing parallel applications should be conducted to analyze their parallel behavior and to extract relevant execution time parameters. Examples from cloud, high performance computing, and real-time workloads can be considered. This analysis should then inform the synthetic simulations performed within the simulator.

The simulator should be capable of operating on single and multiple concurrently running DAG-style applications. It should assign work to simulated CPU cores and thereby generate an execution trace that allows to judge scheduler efficiency, for example by the resulting CPU utilization and makespan.

Having full knowledge of the DAG available with all execution time parameters is an ideal scenario for scheduling, but not realistic in practice. Nevertheless, such a clairvoyant scheduler is useful for benchmarking. At least one additional scenario with a reduced, more coarse-grained representation of task behavior and a consequently less precise scheduling algorithm should be implemented and evaluated.

Dynamically changing the core count, heterogeneous hardware, or unforeseen code execution in applications, for example to recover from a fault, are potential future extensions, but outside the scope of this thesis.

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