RTL8019AS
RTL8019AS-LF

FULL-DUPLEX 10MBPS PLUG AND PLAY ETHERNET CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.1	2009/06/11	Added confidential marking.

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1. General Description

The RTL8019AS is a highly integrated 10Mbps Ethernet Controller providing a simple solution to implement a Plug and Play NE2000 compatible adapter with full-duplex and three-level power-down control features. The full-duplex function enables simultaneous transmission and reception on a twisted-pair link to a full-duplex Ethernet switching hub. This feature not only increases the channel bandwidth from 10 to 20Mbps, but also avoids performance degradation problems due to the channel contention characteristics of the Ethernet CSMA/CD protocol.

Plug and Play function relieves the user from setting up the adapter's resource configurations, e.g., IRQ, I/O, and memory address, etc. However, for special applications where the RTL8019AS will not be used as a Plug and Play compatible device, the RTL8019AS also supports jumper and proprietary jumperless options.

To offer a full Plug and Play solution, the RTL8019AS provides auto-detect capability between the integrated 10Base-T transceiver, BNC, and AUI interfaces. The 10Base-T transceiver can automatically correct polarity errors on its receiving pair. Furthermore, 8 IRQ lines and 16 I/O base address options are provided for resource configuration flexibility.

The RTL8019AS supports 16k, 32k, and 64k byte boot ROM and flash memory interface. It also offers the page mode function which can support up to 4M-byte boot ROM within only 16k-byte system memory space. A boot ROM disable command is provided to release the boot ROM memory space for other system usage (e.g. EMM386, etc.) after the boot ROM program is loaded.

The RTL8019AS features built-in 16K-byte SRAM, and is designed not only to provide more friendly functions, but also to eliminate the cost and effort of SRAM sourcing and inventory.

2. Features

- RTL8019 software compatible
- Supports PnP auto detect mode
- Compliant to Ethernet II and IEEE 802.3 10Base-5, 10Base-2, 10Base-T
- Software compatible with NE2000 on both 8 and 16-bit slots
- Supports both jumper and jumperless modes
- Supports Plug and Play configuration for jumperless mode
- Supports Full-Duplex Ethernet function to double the channel bandwidth
- Supports three-level power-down modes
  - Sleep
  - Power down with internal clock running
  - Power down with internal clock halted
- Built-in data prefetch function to improve performance
- Supports UTP, AUI, and BNC auto-detect
- Supports auto polarity correction for 10Base-T
- Support 8 IRQ lines
- Supports 16 I/O base address options
  - Plus extra I/O address fully decode mode
- Supports 16K, 32K, 64K and 16K-byte mode access to boot ROM (up to 256 pages with 16K bytes/page)
- Supports boot ROM disable command to release memory after remote boot
- Supports flash memory read/write
- Built-in 16k byte SRAM
- Uses 9346 (64*16-bit EEPROM) to store resource configurations and ID parameters
- Capable of programming blank 9346 on board for manufacturing convenience
- Supports 4 diagnostic LED pins with programmable outputs
- Package: 100-pin PQFP

3. Pin Assignments

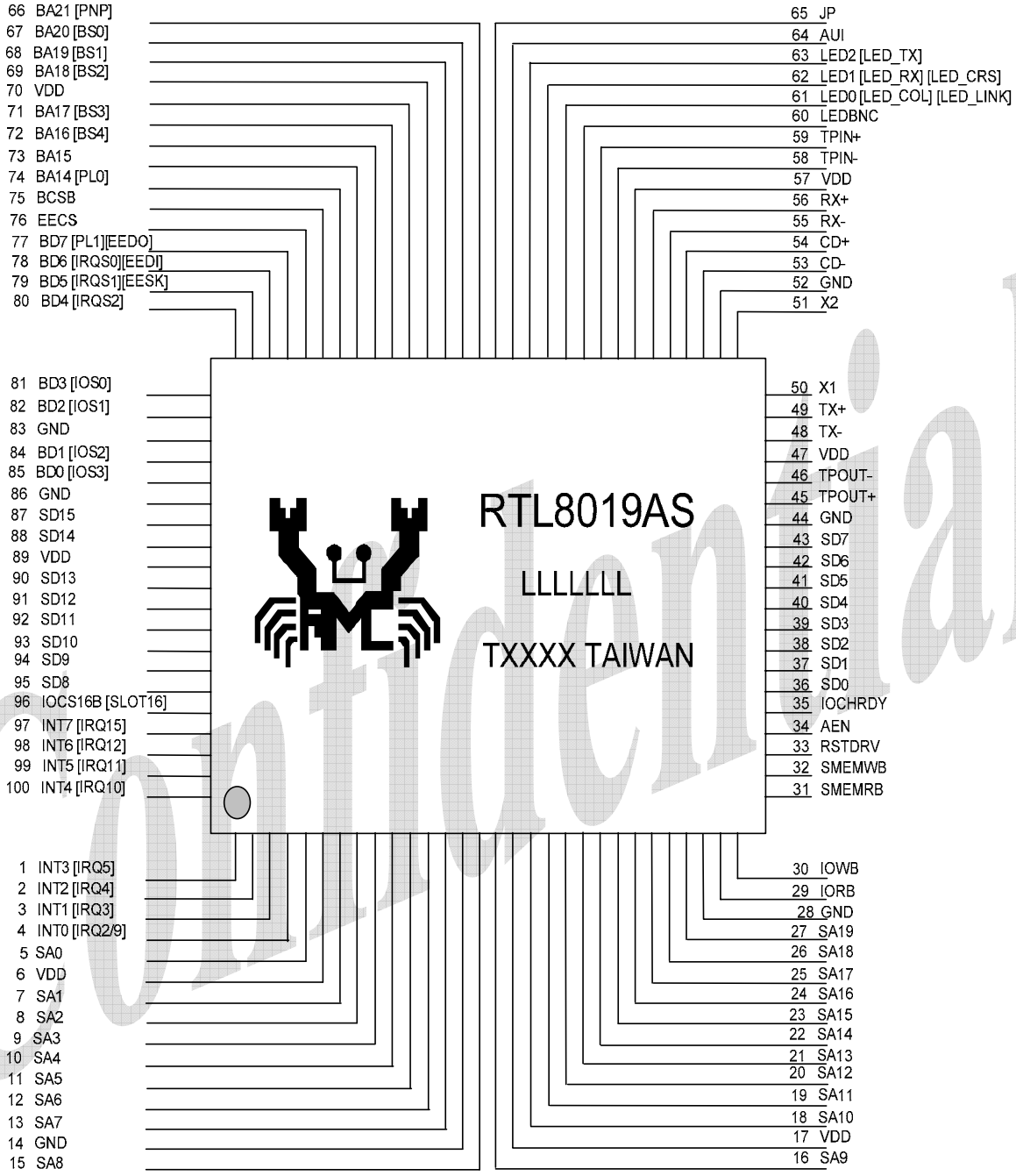


Figure 1. Pin Assignments

3.1. Package Identification

Lead-free package is indicated by an 'L' in the location marked 'T' in Figure 1.

4. Pin Descriptions

4.1. Power Pins

Table 1. Power Pins

No.	Name	Type	Description
6, 17, 47, 57, 70, 89	VDD	P	+5V DC Power.
14, 28, 44, 52, 83, 86	GND	P	Ground.

4.2. ISA Bus Interface Pins

Table 2. ISA Bus Interface Pins

No.	Name	Type	Descriptions
34	AEN	I	Address Enable. This ISA signal must be low for a valid I/O command.
97~100, 1~4	INT7~0	O	Interrupt Request Lines (mapped to IRQ15, IRQ12, IRQ11, IRQ10, IRQ5, IRQ4, IRQ3, IRQ2/9 respectively). Only one line is selected to reflect the interrupt requests at one time. All other lines are tri-stated. The RTL8019AS also uses these pins as inputs to monitor the actual state of the corresponding interrupt lines on the ISA bus. The result is recorded in the INTR register, which can be used by software to detect interrupt conflicts.
35	IOCHRDY	O	This ISA Signal is Driven Low to Insert Wait Cycles to Current Host Read/Write Command.
96	IOCS16B [SLOT16]	O	Upon Power-On Reset this pin acts as an input named SLOT16 and detects whether a 16-Bit or 8-Bit slot is in use. To do this, it is connected to a pull-down resistor (27KW) externally. At the falling edge of RSTDRV, the RTL8019AS senses this pin's state. If it is sensed high, the adapter is thought to be placed on a 16-bit slot where this pin is connected to the host's IOCS16B pin, which is typically pulled up by a 300W resistor on the mainboard. If it is sensed low, the adapter is thought to be placed on an 8-bit slot where this pin is pulled low by the 27KW resistor. After having latched the input state, this pin is switched as the IOCS16B signal, which is an open-drain output, and is driven low during a 16-bit host data transfer. It is decoded from AEN and SA9~0.
29	IORB	I	Host I/O Read Command.
30	IOWB	I	Host I/O Write Command.
33	RSTDRV	I	High Active Hardware Reset Signal from the ISA Bus. Pulses with high level less than 800ns are ignored.
27~18, 16~15, 13~7, 5	SA19~0	I	Host Address Bus. SA10 is added to implement the full decode of PnP ports, address 279h, and address A79h. SA10 should be 0 for a valid access to PnP ports.
87~88, 90~95, 43~36	SD15~0	I/O	Host Data Bus.
31	SMEMRB	I	Host Memory Read Command.
32	SMEMWB	I	Host Memory Write Command. This pin is added to decode the write command of a flash memory.

4.3. Memory Interface Pins (Including Boot ROM, EEPROM)

Table 3. Memory Interface Pins (Including Boot ROM, EEPROM)

No.	Name	Type	Description
75	BCSB	O	Boot ROM Chip Select. Active low signal, asserted when Boot ROM is read. The RTL8019AS drives this pin low when SA19~14 matches the selected Boot ROM memory base address and either of the 2 conditions below is met: (1) SMEMRB is low (2) SMEMWB is low and the RTL8019AS's flash memory write function is enabled.
76	EECS	O	9346 Chip Select. Active high signal. Asserted when the 9346 is read/write.
66~69, 71~74	BA21~14	O	Boot ROM Address*
77~82, 84~85	BD7~0	I/O	Boot ROM Data Bus.
[79]	[EESK]	O	9346 Serial Data Clock.
[78]	[EEDI]	O	9346 Serial Data Input.
[77]	[EEDO]	I	9346 Serial Data Output.
The Following Pins are Defined for Jumper Options. Their states are latched at the falling edge of RSTDRV, then they are changed to serve as the SRAM bus. Each of them is internally pulled down by a 100KW resistor. Therefore, the input will be low when left open, and high when pulled up by a 10K resistor externally.			
[66]	[PNP]	I	When High in Jumperless Mode (i.e., JP=low), the RTL8019AS is Forced into Plug and Play Mode Regardless of the Contents of the 9346. This pin is irrelevant in jumperless mode (JP=low).
[72~71, 69~67]	[BS4~0]	I	Select Boot ROM Size and Base Address. This pin is irrelevant in jumperless mode (JP=low).
[85~84, 82~81]	[IOS3~0]	I	Select I/O Base Address. This pin is irrelevant in jumperless mode (JP=low).
[77, 74]	[PL1~0]	I	Select Network Medium Type. This pin is irrelevant in jumperless mode (JP=low).
[80~78]	[IRQS2~0]	I	Select One Interrupt Line from INT7~0. This pin is irrelevant in jumperless mode (JP=low).
65	JP	I	When High, This Pin Selects Jumper Mode. When low, it selects jumperless modes (including RT jumperless and Plug and Play).

Note: After the RTL8019AS latches all jumper status upon power on reset, these pins **always** *reflect the value of the BPAGE register directly in Boot ROM page mode. In normal mode, BA16~21 are not used and BA14~15 act as:*

Boot ROM Size	BA14	BA15
16K	High	High
32K	SA14	High
64K	SA14	SA15

Note: The RTL8019AS does not drive BA14~21 until the SMEMRB goes from high to low.

4.3.1. Medium Interface Pins

Table 4. Medium Interface Pins

No.	Name	Type	Description
64	AUI	I	This Input is Used to Detect the Usage of an External MAU on the AUI Interface. The input should be driven low for embedded BNC and high for external MAU. When the input is high, the RTL8019AS sets the AUI bit (bit5) in CONFIG0 and drives LEDBNC low to disable the BNC. If this pin is not used, it should be connected to GND. See section 6.2, page 17 for more details.
54, 53	CD+, CD-	I	This AUI Collision Input Pair Carries the Differential Collision Input Signal from the MAU.
56, 55	RX+, RX-	I	This AUI Receive Input Pair Carries the Differential Receive Input Signal from the MAU.
49, 48	TX+, TX-	O	This AUI Transmit Output Pair Contains Differential Line Drivers that Send Manchester Encoded Data to the MAU. These outputs are source followers and require 270ohm pull-down resistors to GND.
59, 58	TPIN+, TPIN-	I	This TP Input Pair Receives 10Mbps Differential Manchester Encoded Data from the Twisted-Pair cable.
45, 46	TPOUT+, TPOUT-	O	This Pair Carries the Differential TP Transmit Output. The output Manchester encoded signals have been pre-distorted to prevent overcharge on the twisted-pair media and thus reduce jitter.
50	X1	I	20MHz Crystal or External Oscillator Input.
51	X2	O	Crystal Feedback Output. This output is used in crystal connection only. It must be left open when X1 is driven with an external oscillator.

4.3.2. LED Output Pins

Table 5. LED Output Pins

No.	Name	Type	Description
60	LEDBNC	O	This Pin Goes High when the RTL8019AS's Medium Type is Set to 10Base-2 Mode or Auto-Detect Mode with Link Test Failure. Otherwise, this pin is low. This pin can be used to control the power of the DC convertor for CX MAU, and can be connected to an LED to indicate the medium type used.
61	LED0	O	When LEDS0 Bit (in CONFIG3 Register of the RTL8019AS Page3) is 0, this pin acts as LED_COL. When LEDS0=1, it acts as LED_LINK.
62, 63	LED1, LED2	O	When LEDS1 Bit (in CONFIG3 Register of the RTL8019AS Page3) is 0, these 2 pins act as LED_RX & LED_TX respectively. When LEDS1=1, these pins act as LED_CRS & MCSB. See section 7.8, page 38 for details of the behavior of all LEDs.

5. Register Descriptions

The registers in the RTL8019AS can be roughly divided into two groups by their address and functions -- one for NE2000, the other for Plug and Play (PnP).

5.1. Group 1: NE2000 Registers

This group includes 4 pages of registers that are selected by bit PS0 & PS1 in the CR register. Each page contains 16 registers. As well as those registers compatible with NE2000, the RTL8019AS defines some registers for software configuration and feature enhancement.

Table 6. Register Table

No (Hex)	Page0		Page1	Page2	Page3	
	[R]	[W]	[RW]	[R]	[R]	[W]
00	CR	CR	CR	CR	***CR***	***CR***
01	CLDA0	PSTART	PAR0	PSTART	***9346CR***	***9346CR***
02	CLDA1	PSTOP	PAR1	PSTOP	***BPAGE***	***BPAGE***
03	BNRY	BNRY	PAR2	-	***CONFIG0***	-
04	TSR	TPSR	PAR3	TPSR	***CONFIG1***	***CONFIG1***
05	NCR	TBCR0	PAR4	-	***CONFIG2***	***CONFIG2***
06	FIFO	TBCR1	PAR5	-	***CONFIG3***	***CONFIG3***
07	ISR	ISR	CURR	-	-	***TEST***
08	CRDA0	RSAR0	MAR0	-	***CSNSAV***	-
09	CRDA1	RSAR1	MAR1	-	-	***HLTCLK***
0A	***8019ID0***	RBCR0	MAR2	-	-	-
0B	***8019ID1***	RBCR1	MAR3	-	***INTR***	-
0C	RSR	RCR	MAR4	RCR	-	***FMWP***
0D	CNTR0	TCR	MAR5	TCR	***CONFIG4***	-
0E	CNTR1	DCR	MAR6	DCR	-	-
0F	CNTR2	IMR	MAR7	IMR	-	-
10-17	Remote DMA Port					
18-1F	Reset Port					

Notes: '-' denotes reserved. Registers with names typed in **bold italic** *format are RTL8019AS defined registers and are not supported in a standard NE2000 adapter.*

5.2. Page 0 (PS1=0, PS0=0)

Table 7. Page 0 (PS1=0, PS0=0)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	RW	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	CLDA0	R	A7	A6	A5	A4	A3	A2	A1	A0
	PSTART	W	A15	A14	A13	A12	A11	A10	A9	A8
02H	CLDA1	R	A15	A14	A13	A12	A11	A10	A9	A8
	PSTOP	W	A15	A14	A13	A12	A11	A10	A9	A8
03H	BNRY	RW	A15	A14	A13	A12	A11	A10	A9	A8
04H	TSR	R	OWC	CDH	0	CRS	ABT	COL	-	PTX
	TPSR	W	A15	A14	A13	A12	A11	A10	A9	A8
05H	NCR	R	0	0	0	0	NC3	NC2	NC1	NC0
	TBCR0	W	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
06H	FIFO	R	D7	D6	D5	D4	D3	D2	D1	D0
	TBCR1	W	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
07H	ISR	RW	RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX
08H	CRDA0	R	A7	A6	A5	A4	A3	A2	A1	A0
	RSAR0	W	A7	A6	A5	A4	A3	A2	A1	A0
09H	CRDA1	R	A15	A14	A13	A12	A11	A10	A9	A8
	RSAR1	W	A15	A14	A13	A12	A11	A10	A9	A8
0AH	8019ID0	R	0	1	0	1	0	0	0	0
	RBCR0	W	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
0BH	8019ID1	R	0	1	1	1	0	0	0	0
	RBCR1	W	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
0CH	RSR	R	DFR	DIS	PHY	MPA	0	FAE	CRC	PRX
	RCR	W	-	-	MON	PRO	AM	AB	AR	SEP
0DH	CNTR0	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	TCR	W	-	-	-	OFST	ATD	LB1	LB0	CRC
0EH	CNTR1	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	DCR	W	-	FT1	FT0	ARM	LS	LAS	BOS	WTS
0FH	CNTR2	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	IMR	W	-	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

5.3. Page 1 (PS1=0, PS0=1)

Table 8. Page 1 (PS1=0, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	RW	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	PAR0	RW	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
02H	PAR1	RW	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
03H	PAR2	RW	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
04H	PAR3	RW	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
05H	PAR4	RW	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
06H	PAR5	RW	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40
07H	CURR	RW	A15	A14	A13	A12	A11	A10	A9	A8
08H	MAR0	RW	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
09H	MAR1	RW	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
0AH	MAR2	RW	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
0BH	MAR3	RW	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
0CH	MAR4	RW	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
0DH	MAR5	RW	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
0EH	MAR6	RW	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
0FH	MAR7	RW	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

5.4. Page 2(PS1=1, PS0=0)

Table 9. Page 2(PS1=1, PS0=0)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	RW	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	PSTART	R	A15	A14	A13	A12	A11	A10	A9	A8
02H	PSTOP	R	A15	A14	A13	A12	A11	A10	A9	A8
03H	-									
04H	TPSR	R	A15	A14	A13	A12	A11	A10	A9	A8
05H~ 0BH	-	-	-	-	-	-	-	-	-	-
0CH	RCR	R	-	-	MON	PRO	AM	AB	AR	SEP
0DH	TCR	R	-	-	-	OFST	ATD	LB1	LB0	CRC
0EH	DCR	R	-	FT1	FT0	ARM	LS	LAS	BOS	WTS
0FH	IMR	R	-	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

5.5. Page 3(PS1=1, PS0=1)

Table 10. Page 3(PS1=1, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	RW	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	9346CR	R	EEM1	EEM0	-	-	EECS	EESK	EEDI	EEDO
		W	EEM1	EEM0	-	-	EECS	EESK	EEDI	-
02H	BPAGE	RW	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
03H	CONFIG0	R	VerID1	VerID0	AUI	PNPJP	JP	BNC	0	0
04H	CONFIG1	R	IRQEN	IRQS2	IRQS1	IRQS0	IOS3	IOS2	IOS1	IOS0
		W*	IRQEN	-	-	-	-	-	-	-
05H	CONFIG2	R	PL1	PL0	BSELB	BS4	BS3	BS2	BS1	BS0
		W*	PL1	PL0	BSELB	-	-	-	-	-
06H	CONFIG3	R	PNP	FUDUP	LEDS1	LEDS0	-	SLEEP	PWRDN	ACTIVEB
		W*	-	-	-	-	-	SLEEP	PWRDN	-
07H	TEST	RW	Reserved, Do Not Write							
08H	CSNSAV	R	CSN7	CSN6	CSN5	CSN4	CSN3	CSN2	CSN1	CNS0
09H	HLTCLK	W	HLT7	HLT6	HLT5	HLT4	HLT3	HLT2	HLT1	HLT0
0AH	-	-	Reserved							
0BH	INTR	R	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
0CH	FMWP	W*	Flash Memory Write Protect							
0DH	CONFIG4	R	-	-	-	-	-	-	-	IOMS
0EH~ 0FH	-	-	Reserved							

Note: The registers marked with type='W' can be written only if bits EEM1=EEM0=1.*

6. Register Functions

6.1. NE2000 Compatible Registers

6.1.1. CR: Command Register (00H; Type=RW)

This register is used to select register pages, enable or disable remote DMA operation, and issue commands.

Table 11. NE2000 Compatible Registers

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7, 6</td><td>PS1, PS0</td><td>
<table>
<tr><th>PS1</th><th>PS0</th><th>Register Page</th><th>Remark</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NE2000 Compatible</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>NE2000 Compatible</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>NE2000 Compatible</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>RTL8019AS Configuration</td></tr>
</table>
</td></tr>
<tr><td>5~3</td><td>RD2~0</td><td>
<table>
<tr><th>RD2</th><th>RD1</th><th>RD0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Remote Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Remote Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Send Packet</td></tr>
<tr><td>1</td><td>*</td><td>*</td><td>Abort/Complete Remote DMA</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>TXP</td><td>This bit must be set to transmit a packet. It is internally reset either after the transmission is completed or aborted. Writing a 0 has no effect.</td></tr>
<tr><td>1</td><td>STA</td><td>The STA (status) bit controls nothing. It only reflects the value written to this bit. POWER UP=0.</td></tr>
<tr><td>0</td><td>STP</td><td>This bit is the STOP Command.
When it is set, no packets will be received or transmitted. POWER UP=1.
<table>
<tr><th>STA</th><th>STP</th><th>Function</th></tr>
<tr><td>1</td><td>0</td><td>Start Command</td></tr>
<tr><td>0</td><td>1</td><td>Stop Command</td></tr>
</table>
</td></tr>
</table>

6.1.2. ISR: Interrupt Status Register (07H; Type=RW in Page0)

This register reflects the NIC status. The host reads it to determine the cause of an interrupt. Individual bits are cleared by writing a 1 into the corresponding bit. This register must be cleared after power up.

Table 12. ISR: Interrupt Status Register (07H; Type=RW in Page0)

Bit	Symbol	Description
7	RST	This bit is set when the NIC enters the reset state, and is cleared when a start command is issued to the CR. It is also set when the receive buffer overflows, and is cleared when one or more packets have been read from the buffer.
6	RDC	Set when Remote DMA operation has been completed.
5	CNT	Set when the MSB of one or more of the network tally counters has been set.

Bit	Symbol	Description
4	OVW	This bit is set when the receive buffer has been exhausted.
3	TXE	Transmit error bit is set when a packet transmission is aborted due to excessive collisions.
2	RXE	This bit is set when a packet is received with one or more of the following errors: - CRC error - Frame alignment error - Missed packet
1	PTX	This bit indicates packet transmitted with no errors.
0	PRX	This bit indicates packet received with no errors.

6.1.3. IMR: Interrupt Mask Register (0FH; Type=W in Page0, Type=R in Page2)

All bits correspond to the bits in the ISR register. POWER UP=all 0s. Setting individual bits will enable the corresponding interrupts.

6.1.4. DCR: Data Configuration Register (0EH; Type=W in Page0, Type=R in Page2)

Table 13. DCR: Data Configuration Register (0EH; Type=W in Page0, Type=R in Page2)

Bit	Symbol	Description
7	-	Always 1.
6, 5	FT1, FT0	FIFO Threshold Select Bit 1 and 0.
4	ARM	Auto-Initialize Remote. 0: Send Packet Command not executed 1: Send Packet Command executed
3	LS	Loopback Select. 0: Loopback mode selected. Bits 1 and 2 of the TCR must also be programmed for Loopback operation 1: Normal Operation
2	LAS	This Bit Must be Set to Zero. The RTL8019AS only supports dual 16-bit DMA mode. POWER UP=1
1	BOS	Byte Order Select (Not Implemented). 0: MS byte placed on MD15~8 and LS byte on MD7~0 (32xxx,80x86) 1: MS byte placed on MD7~0 and LS byte on MD15~8 (680x0)
0	WTS	Word Transfer Select. 0: Byte-wide DMA transfer 1: Word-wide DMA transfer

6.1.5. TCR: Transmit Configuration Register (0DH; Type=W in Page0, Type=R in Page2)

Table 14. TCR: Transmit Configuration Register (0DH; Type=W in Page0, Type=R in Page2)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>-</td><td>Always 1.</td></tr>
<tr><td>6</td><td>-</td><td>Always 1.</td></tr>
<tr><td>5</td><td>-</td><td>Always 1.</td></tr>
<tr><td>4</td><td>OFST</td><td>Collision Offset Enable.</td></tr>
<tr><td>3</td><td>ATD</td><td>Auto Transmit Disable.
0: Normal operation
1: Reception of multicast address hashing to bit 62 disables transmitter.
Reception of multicast address hashing to bit 63 enables transmitter.</td></tr>
<tr><td>2~1</td><td>LB1, LB0</td><td><table><tr><th>LB1</th><th>LB0</th><th>Mode</th><th>Remark</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Normal Operation</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Internal Lookback</td></tr><tr><td>1</td><td>0</td><td>2</td><td>External Lookback</td></tr><tr><td>1</td><td>1</td><td>3</td><td>External Lookback</td></tr></table></td></tr>
<tr><td>0</td><td>CRC</td><td>The NIC CRC Logic Comprises a CRC Generator for the Transmitter and a CRC Checker for the Receiver. This bit controls the activity of the CRC logic. If this bit set, CRC is inhibited by the transmitter. Otherwise CRC is appended by the transmitter.<table><tr><th colspan="2">Conditions</th><th colspan="2">CRC Logic Activities</th></tr><tr><th>CRC Bit</th><th>Mode</th><th>CRC Generator</th><th>CRC Checker</th></tr><tr><td>0</td><td>Normal</td><td>Enabled</td><td>Enabled</td></tr><tr><td>1</td><td>Normal</td><td>Disabled</td><td>Enabled</td></tr><tr><td>0</td><td>Loopback</td><td>Enabled</td><td>Disabled</td></tr><tr><td>1</td><td>Loopback</td><td>Disabled</td><td>Enabled</td></tr></table></td></tr>
</table>

6.1.6. TSR: Transmit Status Register (04H; Type=R in Page0)

This register indicates the status of a packet transmission.

Table 15. TSR: Transmit Status Register (04H; Type=R in Page0)

Bit	Symbol	Description
7	OWC	Out of Window Collision. Set when a collision is detected after a slot time (51.2µs). Transmissions are rescheduled as in normal collisions.
6	CDH	CD Heartbeat. The NIC watches for a collision signal (i.e. CD Heartbeat signal) during the first 6.4µs of the inter-frame gap following a transmission. This bit is set if the transceiver fails to send this signal.
5	-	Always 1.
4	CRS	Carrier Sense Lost Bit is set when the carrier is lost during transmission of a packet.
3	ABT	Indicates the NIC aborted the transmission because of excessive collisions.
2	COL	Indicates the transmission collided with some other station on the network.
1	-	Always 1.
0	PTX	This bit indicates the transmission completed with no errors.

6.1.7. RCR: Receive Configuration Register (0CH; Type=W in Page0, Type=R in Page2)

Table 16. RCR: Receive Configuration Register (0CH; Type=W in Page0, Type=R in Page2)

Bit	Symbol	Description
7	-	Always 1.
6	-	Always 1.
5	MON	When monitor mode bit is set, received packets are checked for address match, good CRC, and frame alignment, but are not buffered to memory. Otherwise, packets will be buffered to memory.
4	PRO	If PRO=1, all packets with physical destination address accepted. If PRO=0, physical destination address must match the node address programmed in PAR0~5.
3	AM	If AM=1, packets with multicast destination address are accepted. If AM=0, packets with multicast destination address are rejected.
2	AB	If AB=1, packets with broadcast destination address are accepted. If AB=0, packets with broadcast destination address are rejected.
1	AR	If AR=1, packets with length fewer than 64 bytes are accepted. If AR=0, packets with length fewer than 64 bytes are rejected.
0	SEP	If SEP=1, packets with receive errors are accepted. If SEP=0, packets with receive errors are rejected.

6.1.8. RSR: Receive Status Register (0CH; Type=R in Page0)

Table 17. RSR: Receive Status Register (0CH; Type=R in Page0)

Bit	Symbol	Description
7	DFR	Deferring. Set when a carrier or a collision is detected.
6	DIS	Receiver Disabled. When the NIC enters the monitor mode, this bit is set and receiver is disabled. Reset when receiver is enabled after leaving the monitor mode.
5	PHY	PHY bit is set when the received packet has a multicast or broadcast destination address. It is reset when the received packet has a physical destination address.
4	MPA	Missed Packet bit is set when the incoming packet cannot be accepted by the NIC because of a lack of receive buffer, or if the NIC is in monitor mode. Increments the CNTR2 tally counter.
3	-	Always 1.
2	FAE	Frame Alignment Error bit reflects the incoming packet did not end on a byte boundary and the CRC did not match at the last byte boundary. Increments the CNTR0 tally counter.
1	CRC	CRC Error Bit Reflects Packet Received with CRC Error. This bit will also be set for FAE errors. Increment the CNTR1 tally counter.
0	PRX	This bit indicates packet received with no errors.

6.1.9. CLDA0, 1: Current Local DMA Registers (01H & 02H; Type=R in Page0)

These two registers can be read to get the current local DMA address.

6.1.10. PSTART: Page Start Register (01H; Type=W in Page0, Type=R in Page 2)

The Page Start register sets the start page address of the receive buffer ring.

PSTOP

Page Stop Register (02H; Type=W in Page0, Type=R in Page2)

The Page Stop register sets the stop page address of the receive buffer ring. In 8-bit mode the PSTOP register should not exceed 0x60, in 16-bit mode the PSTOP register should not exceed 0x80.

BNRY

Boundary Register (03H; Type=RW in Page0)

This register is used to prevent overwrite of the receive buffer ring. It is typically used as a pointer indicating the last receive buffer page the host has read.

TPSR

Transmit Page Start Register (04H; Type=W in Page0)

This register sets the start page address of the packet to be transmitted.

TBCR0, 1

Transmit Byte Count Registers (05H & 06H; Type=W in Page0)

These two registers set the byte counts of the packet to be transmitted.

NCR

Number of Collisions Register (05H; Type=R in Page0)

The register records the number of collisions a node experiences during a packet transmission.

FIFO

First In First Out Register (06H; Type=R in Page0)

This register allows the host to examine the contents of the FIFO after loopback.

CRDA0, 1

Current Remote DMA Address registers (08H & 09H; Type=R in Page0)

These two registers contain the current address of remote DMA.

RSAR0, 1

Remote Start Address Registers (08H & 09H; Type=W in Page0)

These two registers set the start address of remote DMA.

RBCR0, 1

Remote Byte Count Registers (0AH & 0BH; Type=W in Page0)

These two registers set the data byte counts of remote DMA.

CNTR0

Frame Alignment Error Tally Counter Register (0DH; Type=R in Page0)

CNTR1

CRC Error Tally Counter Register (0EH; Type=R in Page0)

CNTR2

Missed Packet Tally Counter Register (0FH; Type=R in Page0)

PAR0~5

Physical Address Registers (01H ~ 06H; Type=RW in Page1)

These registers contain the Ethernet node address and are used to compare the destination address of incoming packets for acceptation or rejection.

CURR

Current Page Register (07H; Type=RW in Page1)

This register points to the page address of the first receive buffer page to be used for packet reception.

6.1.11. MAR0~7: Multicast Address Register (08H ~ 0FH; Type=RW in Page1)

These registers provide filtering bits of multicast addresses hashed by the CRC logic.

6.2. RTL8019AS Defined Registers

6.2.1. Page 0 (PS1=0, PS0=0)

Two registers are defined to contain the RTL8019AS chip ID.

Table 18. Page 0 (PS1=0, PS0=0)

No.	Name	Type	Bit7~0
0AH	8019ID0	R	50H (ASCII Code of 'P')
0BH	8019ID1	R	70H (ASCII Code of 'p')

6.2.2. Page 3 (PS1=1, PS0=1)

Page3 Power Up Values before loading jumper states and 9346 contents.

Table 19. Page3 (PS1=1, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	RW	0	0	1	0	0	0	0	1
01H	9346CR	RW	0	0	*	*	*	*	*	*
02H	BPAGE	RW	0	0	0	0	0	0	0	0
03H	CONFIG0	RW	0	0	*	*	*	*	0	0
04H	CONFIG1	RW	1	*	*	*	*	*	*	*
05H	CONFIG2	RW	*	*	0	*	*	*	*	*
06H	CONFIG3	RW	*	*	*	*	*	0	0	1
07H	TEST	RW	-	-	-	-	-	-	-	-
08H	CSNSAV	R	0	0	0	0	0	0	0	0
09H	HLTCLK	W	1	1	1	1	1	1	1	1
0AH		-	-	-	-	-	-	-	-	-
0BH	INTR	R	*	*	*	*	*	*	*	*
0CH	FMWP	W	-	-	-	-	-	-	-	-
0DH	CONFIG4	R	-	-	-	-	-	-	-	*
0EH~ 0FH		-	-	-	-	-	-	-	-	-

*Note: * indicates user defined.*

6.2.3. Page3 Content Descriptions

9346CR: 9346 Command Register (01H; Type=RW except Bit0=R).

Table 20. Page3 Content Descriptions

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7~6</td><td>EEM1~0</td><td>These 2 Bits Select the RTL8019AS Operating Mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (DP8390 Compatible).</td></tr>
<tr><td>0</td><td>1</td><td>Auto-Load.
Entering this mode will force the RTL8019AS to load the contents of the 9346 as though the RSTDRV signal is asserted.
This auto-load operation will take about 2ms. After it is completed, the RTL8019AS goes back to the normal mode automatically (EEM1=EEM0 =0) and the CR register is reset to 21H.</td></tr>
<tr><td>1</td><td>0</td><td>9346 Programming.
In this mode, both the local & remote DMA operation of the RTL8019AS are disabled. The 9346 can be directly accessed via bit3~0 which now reflects the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config Register Write Enable.
Before writing to the Page3 CONFIG1-3 registers, the RTL8019AS must be placed in this mode. This will prevent the RTL8019AS’s configurations from being accidentally changed.</td></tr>
</table></td></tr>
<tr><td>5~4</td><td>-</td><td>Not Used.</td></tr>
<tr><td>3</td><td>EECS</td><td rowspan="4">These Bits Reflect the State of EECS, EESK, EEDI, & EEDO Pins in Auto-Load or 9346 Programming Mode.</td></tr>
<tr><td>2</td><td>EESK</td></tr>
<tr><td>1</td><td>EEDI</td></tr>
<tr><td>0</td><td>EEDO</td></tr>
</table>

6.2.4. BPAGE: Boot ROM Page Register (02H; Type=RW)

This register selects a boot ROM page to be read by the host. It can select a maximum of 256 pages with 16k bytes per page. Thus the maximum boot ROM size is 256*16k=4M bytes.

6.2.5. CONFIG0: RTL8019AS Configuration Register 0 (03H; Type=R Except Bit[7:6]=RW)

Table 21. CONFIG0: RTL8019AS Configuration Register 0 (03H; Type=R Except Bit[7:6]=RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-6</td><td>VERID</td><td>Version ID: These two bits are defined as below.
<table>
<tr><th>Bit7</th><th>Bit6</th><th>Type</th><th>Mode</th></tr>
<tr><td>1</td><td>1</td><td>R</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>R</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>RW</td><td>RTL8019AS, these two bits are all 0 when powered on, but can be written in the RTL8019AS’s config write enable mode (EEM0=EEM1=1). Software uses these differences to identify the chip.</td></tr>
</table></td></tr>
<tr><td>5</td><td>AUI</td><td>This Bit is Set when An External MAU is Used on the AUI Interface.
Therefore it is set when in 10Base-5 mode or when the AUI input pin is high.</td></tr>
<tr><td>4</td><td>PNPJP</td><td>This Bit is Set when the PnP Jumper Pin is Pulled High Externally.</td></tr>
<tr><td>3</td><td>JP</td><td>This Bit Reflects the State of JP Input. When set it indicates the RTL8019AS is in jumper mode.</td></tr>
<tr><td>2</td><td>BNC</td><td>When set, this bit indicates that the RTL8019AS is Using 10Base-2 Cable as Its Networking Medium. This bit will be set in the following 2 cases:
(1) PL1=PL0=0 (auto-detect) and link test fails
(2) PL1=PL0=1 (10 Base 2)</td></tr>
<tr><td>1~0</td><td>0</td><td>Always 0s.</td></tr>
</table>

The following table describes the behavior of bits and pins for cabling media.

Table 22. Cabling Media Behavior

Media Type	AUI Input	Selected Media	AUI Bit	BNC Bit	LEDBNC Output	Original BNC bit in 8019 (For Reference Only)
10Base-5	x	AUI	1	0	L	0
10Base-2	x	BNC	0	1	H	1
10Base-T Link Disabled	x	UTP	0	0	L	0
Auto Detect Link OK	x	UTP	0	0	L	0
Auto Detect Link Fail	L	BNC	0	1	H	1
Auto Detect Link Fail	H	AUI	1	0	L	1

6.2.6. CONFIG1: RTL8019AS Configuration Register 1 (04H; Type=R Except Bit7=RW)

Table 23. CONFIG1: RTL8019AS Configuration Register 1 (04H; Type=R Except Bit7=RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>IRQEN</td><td>IRQ Enable.
This bit controls the state of the interrupt request line selected by IRQS2~0. If this bit is set, the interrupt line goes high upon an interrupt request and will be low when there is no interrupt request.
The interrupt line will be forced to tri-state if this bit is reset.
This bit’s power-up initial value is 1 and may be modified by software if EEM1=EEM0=1 in the 9346CR register.</td></tr>
<tr><td>6-4</td><td>IRQS2~0</td><td>IRQ Select.
These 3 bits select one of INT7~0 to reflect the RTL8019AS’s interrupt request status. All unselected interrupt lines will be tri-stated.
<table>
<tr><th>IRQS2</th><th>IRQS1</th><th>IRQS0</th><th>Interrupt Line</th><th>Assigned ISA IRQ</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>INT0</td><td>IRQ2/9</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>INT1</td><td>IRQ3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>INT2</td><td>IRQ4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>INT3</td><td>IRQ5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>INT4</td><td>IRQ10</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>INT5</td><td>IRQ11</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>INT6</td><td>IRQ12</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>INT7</td><td>IRQ15</td></tr>
</table></td></tr>
<tr><td>3~0</td><td>IOS3~0</td><td>Select I/O Base Address.
<table>
<tr><th>IOS3</th><th>IOS2</th><th>IOS1</th><th>IOS0</th><th>I/O Base</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>300H</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>320H</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>340H</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>360H</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>380H</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3A0H</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>3C0H</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>3E0H</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>200H</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>220H</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>240H</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>260H</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>280H</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>2A0H</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>2C0H</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>2E0H</td></tr>
</table></td></tr>
</table>

6.2.7. CONFIG2: RTL8019AS Configuration Register 2 (05H; Type=R Except Bit[7:5]=RW)

Table 24. CONFIG2: RTL8019AS Configuration Register 2 (05H; Type=R Except Bit[7:5]=RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7~6</td><td>PL1~0</td><td>Select Network Medium Types.
<table>
<tr><th>PL1</th><th>PL0</th><th>Medium Type</th></tr>
<tr><td>0</td><td>0</td><td>TP/CX auto-detect (10Base-T link test is enabled)</td></tr>
<tr><td>0</td><td>1</td><td>10Base-T with link test disabled</td></tr>
<tr><td>1</td><td>0</td><td>10Base-5</td></tr>
<tr><td>1</td><td>1</td><td>10Base-2</td></tr>
</table></td></tr>
<tr><td>5</td><td>BSELB</td><td>This bit, when set, forces the Boot ROM Disabled Regardless of the Contents of BS4~0. Its power-up initial value is 0 and it can be modified by software if EEM1=EEM0=1 in the 9346CR register.</td></tr>
<tr><td>4~0</td><td>BS4~0</td><td>Select the Boot ROM Size and Memory Base Address.
<table>
<tr><th>BS4</th><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Boot ROM Base & Size</th></tr>
<tr><td>0</td><td>0</td><td>*</td><td>*</td><td>*</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>C000h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C800h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>D000h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>D800h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>C000h, 64K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>D000h, 64K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C000h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C400h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>C800h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>CC00h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>D000h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>D400h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>D800h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>DC00h, 16K</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>C000h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C400h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>C800h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>CC00h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>D000h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>D400h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>D800h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>DC00h, Page</td></tr>
</table>
The RTL8019AS supports a special boot ROM mode: page mode. In page mode, the boot ROM always occupies 16K-byte of host memory space. However the actual boot ROM size can be up to 4M bytes.
The boot ROM is divided into several 16K-byte pages. The power on boot page is set to page 0 and the program in page 0 is responsible for selecting the other pages from the BPAGE register and loading their programs.</td></tr>
</table>

Bit	Symbol	Description
		In page mode, bits BP7~0 of BPAGE register are mapped to the BA21-14 pins to select the proper boot ROM page. In other modes, BA21-16 are not used and the BA15-14 outputs are shown in the following table.

Boot ROM Size	BA14	BA15
16K	High	High
32K	SA14	High
64K	SA14	SA15

6.2.8. CONFIG3: RTL8019AS Configuration Register 3 (06H; Type=R Except Bit[2:1]=RW)

Table 25. CONFIG3: RTL8019AS Configuration Register 3 (06H; Type=R Except Bit[2:1]=RW)

Bit	Symbol	Description
7	PNP	This bit is irrelevant in Jumper Mode. In jumperless mode, when set, it indicates the RTL8019AS is operating in Plug and Play mode. This bit is set when the PnP pin is high or the PnP bit in the 9346 is set in jumperless mode.
6	FUDUP	When this bit is set, the RTL8019AS is set to full-duplex mode, which enables simultaneously transmission and reception on the twisted-pair link to a full-duplex Ethernet device. This feature not only increases the channel bandwidth from 10 to 20Mbps, but also avoids performance degradation problems due to the channel contention characteristics of the Ethernet CSMA/CD protocol.
5~4	LEDS1~0	These Two Bits Select the Outputs to LED2~0 Pins.

LEDS0	LED0 Pin
0	LED_COL
1	LED_LINK

LEDS1	LED1 Pin	LED2 Pin
0	LED_RX	LED_TX
1	LED_CRS	MCSB

		See section 7.8, page 38 for LED behavior details. The MCSB signal is defined to put the local buffer SRAM into standby mode while DMA is not in progress and thus save power. *Note: MCSB is not an LED signal.*
3	-	Reserved. Do not write a 1 to this bit.
2	SLEEP	This bit, when set, puts the RTL8019AS into Sleep Mode. In sleep mode, all LED signals except LEDBNC are forced high to turn off the LEDs (note that MCSB is not an LED signal). The RTL8019AS still handles the network transmission and reception as in normal mode. LEDBNC is not affected by this bit. This bit's power-up initial value is 0 and can be modified by software when EEM1=EEM0=1.

Bit	Symbol	Description
1	PWRDN	This bit, when set, puts the RTL8019AS into Power Down Mode. The RTL8019AS supports two types of power down mode, which are selected by the contents of the HLTCLK register: (1) Mode 1: Power down with clock running (2) Mode 2: Power down with clock halted In both power down modes, the RTL8019AS's serial network interface and transceiver are turned off. All network activities are ignored. All LED signals except LEDBNC are forced high. The LEDBNC is forced low to disable the DC convertor for coaxial transceiver. In power down mode2, the RTL8019AS stops its internal clock for minimal power consumption. Registers except HLTCLK are typically not accessible in this mode. This bit's initial value comes from the 9346 and can be modified if EEM1=EEM0=1 in the 9346CR register.
0	ACTIVEB	This bit is the inverse of Bit 0 in the PnP Activate Register (Index 30H). When the RTL8019AS is deactivated, all boot ROM memory read and I/O accesses to the Group1 registers except the HLTCLK register are ignored. The HLTCLK register and PnP logic work the same as when the RTL8019AS is active. *Note: The PnP logical device control register is the only way to activate the RTL8019AS. Therefore, the HLTCLK register is allowed to be written to prevent the RTL8019AS from dying when it is inactive in the clock-halted power-down mode.*

6.2.9. CONFIG4 RTL8019AS Configuration Register 4 (0DH; Type=R)

Table 26. CONFIG4 RTL8019AS Configuration Register 4 (0DH; Type=R)

Bit	Symbol	Description
7-1	-	Reserved
0	IOMS	When this bit is set, the RTL8019AS uses SA15~SA0 to decode the I/O address of NE2000 registers. When this bit is reset, the RTL8019AS decodes SA9~SA0. This mode is supported for applications which might require full decoding of I/O addresses. This bit is read-only and comes from the CONFIG4 byte (Offset 03H) of the 9346 (refer to section 7.6, page 35).

6.2.10. CSNSAV: CSN Save Register (08H; Type=R)

This register is provided to backup the CSN assigned to the PnP CSN register.

6.2.11. HLTCLK: Halt Clock Register (09H; Type=W)

This is the only active register of the Group1 registers when the RTL8019AS is inactivated.

Writing to this register is invalid if the RTL8019AS is not in power down mode (i.e. If PWRDN bit in CONFIG3 register is zero).

The data written to this register determines the RTL8019AS's power down mode.

Data	Power Down Mode
52H (ASCII Code of 'R')	Mode 1 - Clock Running
48H (ASCII Code of 'H')	Mode 2 - Clock Halted
Other Values	Ignored

6.2.12. INTR: Interrupt Register (0BH; Type=R)

This register reflects the ISA bus states of INT7~0 pins.

6.2.13. FMWP: Flash Memory Write Protect Register (0Ch, Type=W)

This register is write-only. A write to this register is valid only when EEM0=EEM1=1. Sequentially writing 2 bytes of data (57H then A8H) to this register enables the flash memory write operation. Writing other data to this register will reset the write sequence and disable the flash write. All flash memory write commands from the host are ignored if the write operation is not enabled.

6.3. Group 2: Plug and Play (PnP) Registers

6.3.1. Auto-Configuration Ports

Three 8-bit I/O ports are defined for the PnP read/write operations. They are called Auto-configuration ports and are listed below.

Table 27. Auto-Configuration Ports

Port Name	Type	Location
ADDRESS	W	279H (Printer Status Port).
WRITE_DATA	W	A79H (Printer Status Port + 800H).
READ_DATA	R	Re-Locatable in the Range 200H to 3FFH.

The Plug and Play registers are accessed by first writing the address of the desired register (called the 'Register Index' in the following paragraphs) to the ADDRESS port, followed by a read of data from the READ_DATA port, or a write of data to the WRITE_DATA port. A write to the ADDRESS port may be followed by any number of WRITE_DATA or READ_DATA accesses to the same indexed register without the need to write to the ADDRESS port before each access.

The Address port is also the write destination of the initiation key, which will be described later.

6.3.2. Plug and Play Registers

The Plug and Play registers can be divided into card registers and logical device registers. According to the Plug and Play specification, a PnP card may contain more than one logical device. The card registers are unique for each card. However, the logical device registers are repeated for each logical device on the card. Furthermore, all card registers are card control registers, while the logical device registers can be divided into logical device control registers and configuration registers. Although an RTL8019AS card contains only one logical device, the following paragraph still depicts the Plug and Play registers by the same PnP categorizing method.

Note: Those registers or bits not mentioned below are all read-only with value=0.

6.3.3. Card Control Registers

Table 28. Card Control Registers

Index	Name	Type	Definition
00H	Set RD_DATA Port	W	The Location of the READ_DATA Port is Determined by Writing to This Register. Bits[7:0] become ISA I/O read port address bits[9:2]. Address bits[1:0] of the READ_DATA port are always 1.
01H	Serial Isolation	R	A read to this register causes a PnP card in the isolation state to compare one bit of the card's serial ID. This process is described in more detail in section 7.5, page 29.
02H	Config Control	W	Bit[0]: Reset command Setting this bit will reset all logical devices and restore configuration registers to their power-up values. The Card Select Number (CSN) is preserved. Bit[1]: Wait for Key command. Setting this bit makes the PnP card return to the Wait for Key state. The CSN is preserved. Bit[2]: PnP Reset CSN command. Setting this bit will reset the NIC's CSN to 0. Both the CSN (index 06H) and CSNSAV (index F5H) registers are reset. *Note: The hardware will automatically clear the bits, so there is no need for software to clear them.*
03H	Wake[CSN]	W	A write to this register will cause all NICs that have a Card Select Number (CSN) that matches the write data[7:0] to go from the Sleep state to either the Isolation state if the write data for this command is zero, or the Config state if the write data is not zero.
04H	Resource Data	R	A read from this register reads the next byte of resource data. The Status register must be polled until bit[0] is set before this register may be read.
05H	Status	R	Bit[0] when set indicates it is okay to read the next data byte from the resource data register.
06H	Card Select Number (CSN)	RW	A write to this register sets a NIC's Card Select Number (CSN). The CSN is a value uniquely assigned to each ISA PnP card after the serial identification process so that each NIC may be individually selected during a Wake[CSN] command. The CSN value written to this register will also be recorded to the CSNSAV register located at PnP register index F5H and Group 1 Page3 offset 08H.
07H	Logical Device Number	R	00H (Only One Logical Device in the RTL8019AS).

6.3.4. Logical Device Control Registers

Table 29. Logical Device Control Registers

Index	Name	Type	Definition
30H	Activate	RW	For each logical device there is one Activate register that controls whether or not the logical device is active on the ISA bus. Bit[0], if set, activates the logical device. Before a logical device is activated, I/O range check must be disabled.
31H	I/O Range Check	RW	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device. Bit[1]: This bit, when set, enables I/O range check. I/O range check is only valid when the logical device is inactive. Bit[0]: If set, this bit forces the logical device to respond to I/O reads of the logical device's assigned I/O range with a 55H when an I/O range check is in operation. If clear, the logical device drives AAH.

6.3.5. Logical Device Configuration Registers

Table 30. Memory Configuration Registers

Index	Name	Type	Definition
40H	Boot ROM Base Address Bits[23:16]	RW	Bits[23:20] and Bit[17] are Read Only with Values=0. All other bits are read/write bits.
41H	Boot ROM Base Address Bits[15:0]	RW	Bits[13:8] are Read Only with Values=0. All other bits are read/write bits.
42H	Memory Control	R	00H (Only 8-Bit Operation is Supported for Boot ROM)

Note: The boot ROM size of the TL8019AS is determined by the 9346 contents but not the memory configuration registers.

Table 31. I/O Configuration Registers

Index	Name	Type	Definition
60H	I/O Base Address Bits[15:8]	RW	Bits[15:10] are Read Only with Values=0. All other bits are read/write bits.
61H	I/O Base Address Bits[7:0]	RW	Bits[4:0] are Read Only with Values=0. All other bits are read/write bits.

Table 32. Interrupt Configuration Registers

Index	Name	Type	Definition
70H	IRQ Level	RW	Read/Write Value Indicating a Selected Interrupt Level. Bits[3:0] select which ISA interrupt level is used. One selects IRQ1, fifteen selects IRQ15. IRQ0 is not a valid interrupt selection and represents no interrupt selection.
71H	IRQ Type	R	Read/Write Value Indicating which Type of Interrupt is Used for the IRQ Selected Above. Bit[1]: Level, 1=high, 0=low Bit[0]: Type, 1=level, 0=edge For the RTL8019AS, this register is read-only with value=02H.

Table 33. DMA Configuration Registers

Index	Name	Type	Definition
74H	DMA Channel Select 0	R	04H (Indicating No DMA Channel is Needed)
75H	DMA Channel Select 1	R	04H (Indicating No DMA Channel is Needed)

Table 34. Vendor Defined Registers

Index	Name	Type	Definition
F0H	CONFIG0	R	Direct Mapping of the Page3 CONFIG0 Register.
F1H	CONFIG1	R	Direct Mapping of the Page3 CONFIG1 Register.
F2H	CONFIG2	R	Direct Mapping of the Page3 CONFIG2 Register.
F3H	CONFIG3	R	Direct Mapping of the Page3 CONFIG3 Register.
F4H	-	-	Reserved
F5H	CSNSAV	R	Direct Mapping of the Page3 CSNSAV Register.
F6H	Vendor Control	W	Bit[2]: RT Reset CSN Command. Setting this bit will reset the card's CSN in the CSN register (index 06H) to 0. The CSNSAV register is not affected. This bit is cleared by hardware automatically.

7. Functional Descriptions

7.1. RTL8019AS Configuration Modes

The RTL8019AS supports three configuration modes: Jumper, RT Jumperless, and PnP.

Table 35. RTL8019AS Configuration Modes

JP Pin	PnP Pin	9346 Content		Mode	CONFIG0		CONFIG3	
		PNP	ACTIVEB		JP	PNPJP	PNP	ACTIVEB
H	H L	x	x	Jumper	1	1 0	0	0
L	H	x	a (a=0or1)	PnP	0	1	1	a
L	L	1	a (a=0or1)	PnP	0	0	1	a
L	L	0	x	RT Jmpless	0	0	0	0

Note: 'x' denotes irrelevant.

The RTL8019AS's resource configuration information such as I/O base address, boot ROM memory base address, and interrupt request line, etc., are stored in the CONFIG3~0 registers in Group1 Page3, as well as in the PnP logical device configuration registers. Their power-up default values may come from the states of jumper pins in jumper mode, or the contents of the 9346 in PnP and RT jumperless mode. Their values can be modified by software via the logical device configuration registers in all three modes. The updated values will also be recorded to the CONFIG3~0 registers. This new configuration is only valid temporarily and will be lost after an auto-load command, an active RSTDRV, or PC power-off. Permanent changes of configuration must be done by changing the jumper states or the contents of the 9346. Note that the boot ROM size cannot be modified temporarily.

The Plug and Play logic can work in all three configuration modes, except that a Realtek defined initiation key, named the RT initiation key, should be used instead of the PnP initiation key. In other words, the RT initiation key is supported in all configuration modes while the PnP initiation key is only supported in PnP mode. By using the RT initiation key, the software can put the RTL8019AS into the PnP Config state and access the logical device configuration registers, even in the jumper and RT jumperless modes.

Power-up Default ACTIVE State

In the RTL8019AS, the ACTIVEB bit in the 9346 is ignored when the RTL8019AS is in jumper or RT jumperless mode. The adapter's power-up status is always 'ACTIVE' in RT jumperless mode. However, the active status can be changed via the PnP Activate register.

The differences between the three configuration modes are shown in the following table.

Table 36. Configuration Mode Differences

Configuration Mode	Resource Power-Up Value	Supported Initiation Key
Jumper	Jumper Pins	RT Initiation Key
RT Jumperless	9346	RT Initiation Key
Plug and Play	9346	RT and PnP Initiation Key

7.2. Initial Values of CONFIG1 Register after RSTDRV or Auto-Load Command

Table 37. Initial Values of CONFIG1 Register after RSTDRV or Auto-Load Command

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRQEN	IRQS2	IRQS1	IRQS0	IOS3	IOS2	IOS1	IOS0
Jumper	1	Jumper	Jumper	Jumper	Jumper	Jumper	Jumper	Jumper
RT Jumperless Plug and Play	1	9346	9346	9346	9346	9346	9346	9346

7.3. Initial Values of CONFIG2 Register after RSTDRV or Auto-Load Command

Table 38. Initial Values of CONFIG2 Register after RSTDRV or Auto-Load Command

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PL1	PL0	BSELB	BS4	BS3	BS2	BS1	BS0
Jumper	Jumper	Jumper	0	Jumper	Jumper	Jumper	Jumper	Jumper
RT Jumperless Plug and Play	9346	9346	0	9346	9346	9346	9346	9346

7.4. Initial Values of CONFIG3 Register after RSTDRV or Auto-Load Command

Table 39. Initial Values of CONFIG3 Register after RSTDRV or Auto-Load Command

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PNP	FUDUP	LEDS1	LEDS0	-	SLEEP	PWRDN	ACTIVEB
Jumper	0	9346	9346	9346	-	0	9346	9346
RT Jumperless Plug and Play	0 1	9346	9346	9346	-	0	9346	9346

7.5. Plug and Play

7.5.1. Initiation Keys

The Plug and Play logic is inactive on power up and must be enabled by software. This is done by a predefined series of writes (32 I/O writes) to the ADDRESS port, which is called the initiation key. The write sequence is decoded by the RTL8019AS. If the correct series of I/O writes is detected, then the Plug and Play auto-configuration ports are enabled. The write sequence will be reset and must be issued from the beginning if any data mismatch occurs. The exact sequence for the initiation key is listed below in hexadecimal notation.

PnP Initiation Key

Table 40. PnP Initiation Key

6A	B5	DA	ED	F6	FB	7D	BE
DF	6F	37	1B	0D	86	C3	61
B0	58	2C	16	8B	45	A2	D1
E8	74	3A	9D	CE	E7	73	39

RT Initiation Key

Table 41. RT Initiation Key

DA	6D	36	1B	8D	46	23	91
48	A4	D2	69	34	9A	4D	26
13	89	44	A2	51	28	94	CA
65	32	19	0C	86	43	A1	50

7.5.2. Isolation Protocol

A simple algorithm is used to isolate each Plug and Play card. This algorithm uses the signals on the ISA bus and requires lock-step operation between the Plug and Play hardware and the isolation software.

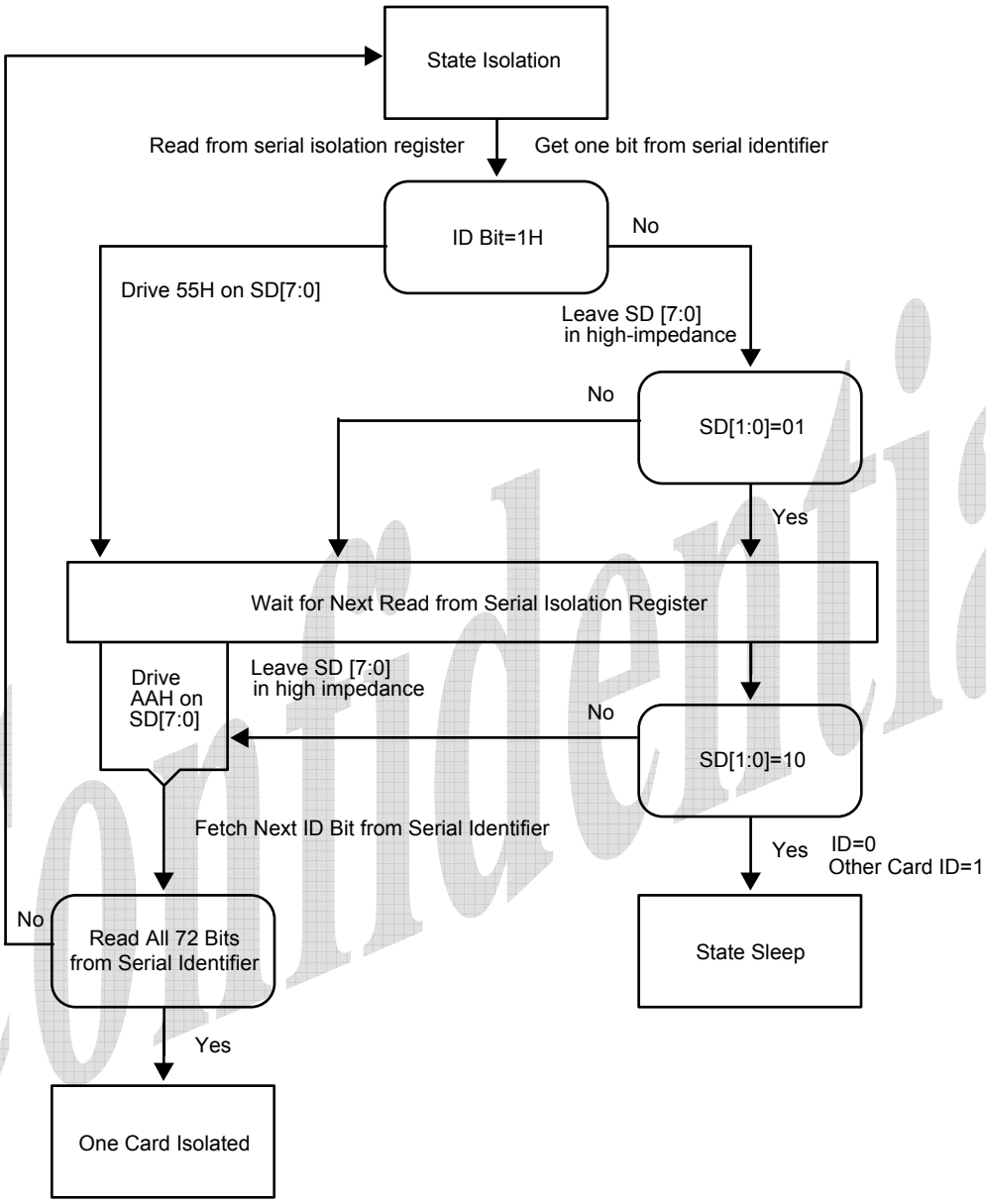


Figure 2. Plug and Play ISA Card Isolation Algorithm

Serial Identifier

The key element of the Plug and Play isolation protocol is that each card contains a unique number, known as a Serial Identifier. The serial identifier is a 72-bit unique, non-zero number composed of two 32-bit fields and an 8-bit checksum. The first 32-bit field is a vendor identifier. The other 32-bits can be any value, for example, a serial number, part of a LAN address, or a static number, as long as there are never two cards in a single system with the same 64-bit number. The serial identifier is accessed bit-serially by the isolation logic and is used to differentiate the cards.

Table 42. Shifting of Serial Identifier

Checksum	Serial Number				Vendor ID				
Byte 0	**Byte 3**	**Byte 2**	**Byte 1**	**Byte 0**	**Byte 3**	**Byte 2**	**Byte 1**	**Byte 0**	
7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0	***Shift***

The shift order for all Plug and Play serial isolation and resource data is defined as bit[0], bit[1], and so on through bit[7].

Hardware Protocol

The isolation protocol can be invoked by the Plug and Play software at any time. The initiation key described earlier puts all cards into configuration mode. The hardware on each card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value of each bit of the serial identifier, which is examined one bit at a time in the sequence shown in Figure 2, page 30.

If the current bit of the serial identifier is a 1, then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is 0, then the card puts its data bus driver into high impedance. All cards in high impedance will check the data bus during the I/O read cycle to sense whether another card is driving SD[1:0] to '01'. During the second I/O read, the card(s) that drove 55H will now drive AAH. All high impedance cards will check the data bus to sense whether another card is driving SD[1:0] to '10'.

If a high impedance card senses another card driving the data bus with the appropriate data during both cycles, then that card ceases to participate in the current iteration of card isolation. Such cards will participate in future iterations of the isolation protocol.

NOTE: During each read cycle, the Plug and Play hardware drives the entire 8-bit data bus, but only checks the lower 2 bits.

If a card is driving the bus, or if a card is in high impedance and does not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit and uses the shifted bit to decide its response.

The above sequence is repeated for the entire 72-bit serial identifier.

At the end of this process, one card remains. This card is assigned a handle referred to as the Card Select Number (CSN) that will be used later to select the card. Cards that have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. Cards must be assigned a CSN before they will respond to other PnP commands.

It should be noted that the protocol permits the 8-bit checksum to be stored in non-volatile memory on the card, or generated by the on-card logic in real-time. The checksum algorithm is implemented as a Linear Feedback Shift Register (LFSR), which is shown in Figure 3, page 32.

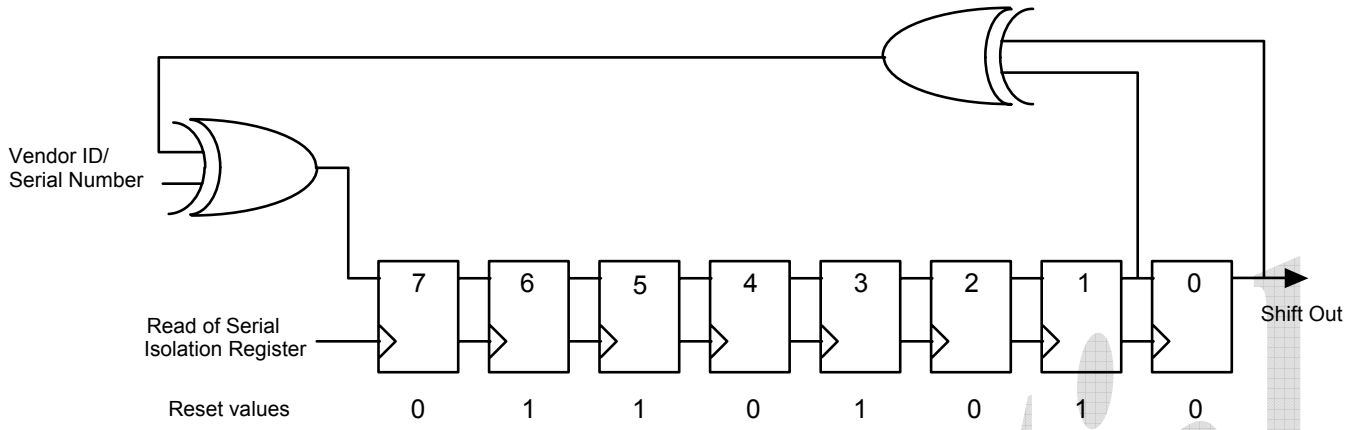


Figure 3. Checksum LFSR

The LFSR resets to 6AH upon receiving the Wake[CSN] command. The next shift value for the LFSR is calculated as LFSR[1] XOR LFSR[0] XOR Serial Data. The LFSR is shifted right one bit at the conclusion of each pair of reads to the Serial Isolation register. LFSR[7] is assigned the next shift value described above.

After the first 64 pairs of reads of the Serial Isolation register, the LFSR will have the value of serial identifier checksum.

Plug and Play cards must not drive the IOCHRDY signal during serial isolation. However, cards may drive IOCHRDY at any other time.

Software Protocol

The Plug and Play software sends the initiation key to all Plug and Play cards to place them into configuration mode. The software is then ready to perform the isolation protocol.

The Plug and Play software generates 72 pairs of I/O read cycles from the READ_DATA port. The software checks the data returned from each pair of I/O reads for 55H or AAH driven by the hardware. If either 55H or AAH are read back, then the software assumes that the hardware had a 1 bit in that position. All other results are assumed to be a 0.

During the first 64 bits, software generates a checksum using the received data. The checksum is compared with the checksum read back in the last 8 bits of the sequence.

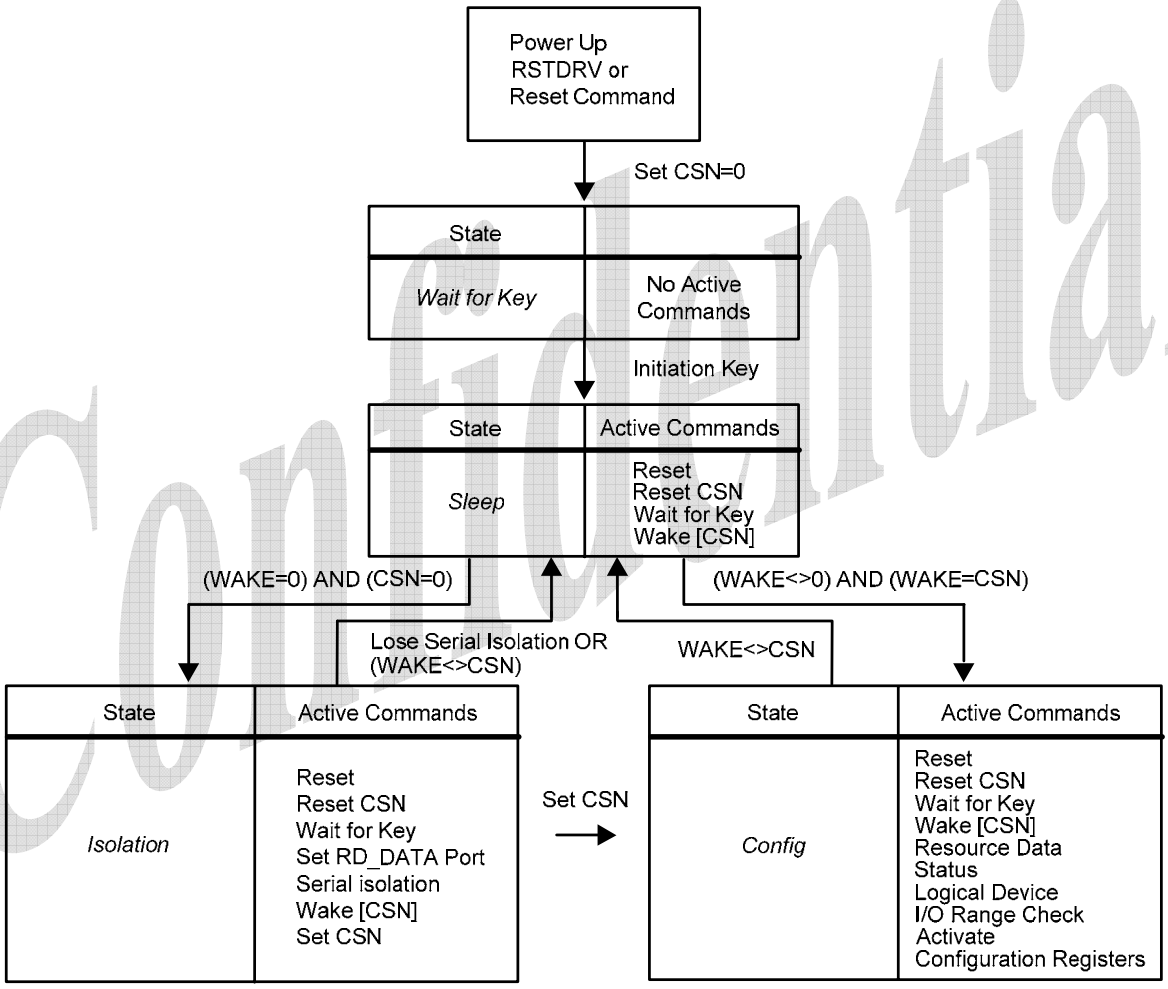
There are two other special considerations for the software protocol. During an iteration it is possible that the 55H and AAH combination is never detected. It is also possible that the checksum does not match. If either of these cases occurs on the first iteration, it must be assumed that the READ_DATA port is in conflict. If a conflict is detected, then the READ_DATA port is relocated. The above process is repeated until a non-conflicting location for the READ_DATA port is found. The entire range between 200H and 3FFH is available, however in practice it is expected that only a few locations will be tried before software determines that no Plug and Play cards are present.

During subsequent iterations, the occurrence of either of these two special cases should be interpreted as the absence of any further Plug and Play cards (i.e., the last card was found in the previous iteration). This terminates the isolation protocol.

NOTE: The software must delay 1 msec prior to starting the first pair of isolation reads, and must wait 250 msec between each subsequent pair of isolation reads. This delay gives the ISA card time to access information from possibly very slow storage devices.

7.5.3. Plug and Play Isolation Sequence

The Plug and Play isolation sequence is divided into four states: Wait for Key, Sleep, Isolation, and Config states. The state transitions for the Plug and Play ISA card are shown below.



NOTES:
1. CSN= Card Select Number
2. RSTDRV causes a state transition from the current state to Wait for Key and sets all CSNs to zero
3. The Wait for Key command causes a state transition from the current state to Wait for Key
4. The Reset CSN commands include PnP Reset CSN and RT Reset CSN commands. The former sets all ISA PnP cards' CSNs to zero while the latter only sets RTL8019 PnP cards' CSNs to zero. Both commands do not cause a state transition.

Figure 4. Plug and Play ISA Card State Transitions

On power up, all PnP cards detect RSTDRV, set their CSN to 0, and enter the Wait for Key state. There is a required 2 msec delay from either a RSTDRV or a PnP Reset command to any Plug and Play port access to allow a card to load initial configuration information from a non-volatile device, which is the 9346 in the case of the RTL8019AS.

Cards in the Wait for Key state do not respond to any access to their auto-configuration ports until the initiation key is detected. Cards ignore all ISA accesses to their Plug and Play interface.

When the cards have received the initiation key, they enter the Sleep state. In this state, the cards listen for a Wake[CSN] command with the write data set to 00H. This wake[CSN] command will send all cards to the Isolation state and reset the serial identifier/resource data pointer to the beginning.

The first time the cards enter the Isolation state it is necessary to set the READ_DATA port address using the Set RD_DATA port command. The software should then verify the selected READ_DATA port address is not in conflict with any other devices via the isolation protocol.

Next, 72 pairs of reads are performed to the Serial Isolation register to isolate a card as described previously. If the checksum read from the card is valid, then this means one card has been isolated. The isolated card remains in the Isolation state until all other cards have failed the isolation protocol and have returned to the Sleep state. The CSN on this card is set to a unique number. Writing this value causes this card to transition to the Config state. Sending a Wake[0] command causes this card to transition back to Sleep state and all cards with a CSN value of zero to transition to the Isolation state. This entire process is repeated until no Plug and Play cards are detected.

7.5.4. Reading Resource Data

Each PnP card supports a resource data structure stored in a non-volatile device (e.g. 9346) to describe the resources supported and those requested by the functions on the card. The Plug and Play resource management software will arbitrate resources and setup the logical device configuration registers according to the resource data.

Card resource data may only be read from cards in the Config state. A card may get to the Config state by one of two different methods. A card enters the Config state in response to the card ‘winning’ the serial isolation protocol and having a Card Select Number (CSN) assigned. The card also enters the Config state in response to receiving a Wake[CSN] command that matches the card’s CSN.

As described above, all Plug and Play cards function as if their serial identifier and their resource data both come from the same serial device. As also stated above, the pointer to the serial device is reset in response to any Wake[CSN] command. This implies that if a card enters the Config state directly in response to a Wake[CSN] command, the 9-byte serial identifier must be read first before the card resource data is accessed. The Vendor ID and Unique Serial Number is valid; however, the checksum byte, when read in this way, is not valid. A card that enters the Config state after the isolation protocol has been run has already accessed all 72 bits of the serial identifier and the first read of the Resource Data register will return resource data.

Card resource data is read by first polling the Status register and waiting for bit[0] to be set. When this bit is set it means that one byte of resource data is ready to be read from the Resource Data register. After the Resource Data register is read, the Status register must be polled before reading the next byte of resource data. This process is repeated until all resource data is read. The format of resource data is described in the following section.

The above operation implies that the hardware is responsible for accumulating 8 bits of data in the Resource Data register. When this operation is complete, the status bit[0] is set. When a read is performed on the Resource Data register, the status bit[0] is cleared, eight more bits are shifted into the Resource Data register, then the status bit[0] is set again.

7.5.5. PnP Auto Detect Mode

When using the RTL8019AS, the user needs to setup the card to PnP or jumperless mode according to the host environments. The typical operating modes of a RTL8019AS card include:

(1) When used in a non-PnP PC, set the card to RT jumperless mode & power-on active

(2) When used in a PnP PC:

(2.1) If boot ROM disabled, set the card to PnP mode & power-on inactive

(2.2) If boot ROM enabled, set the card to PnP mode & power-on active

If a card in mode (2.1) is put in a non-PnP PC, the drivers will fail to initialize the card. RTL8019AS supports a PnP auto-detect mode to solve the problem. The card may be set to a default state: PnP mode & power-on active with boot ROM disabled. If the card is in a non-PnP PC, it will work like a normal jumperless card. If the card is in a PnP PC which requires the card to be powered-on inactive, the RTL8019AS will put itself into inactive state the first time a PnP init key is detected.

7.6. 9346 Contents

The 9346 is a 1k-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.

Table 43. 9346 Contents

Bytes		Contents	Comments
00H~03H	(4 Bytes) 00H 01H 02H 03H	 CONFIG1 CONFIG2 CONFIG3 CONFIG4	Power-up initial value of Page3 and PnP logical device configuration registers.
04H~11H	(14 Bytes) 04H~09H 0AH~11H	 Ethernet ID 0-5 Product ID 0-7	NE2000 IDPROM. Ethernet node address. Assigned by card makers; negligible.
12H~1AH	(9 Bytes) 12H~15H 16H~19H 1AH	 Vendor ID 0-3 Serial Number 0-3 Serial ID Checksum	Plug and Play Serial Identifier.
1BH~7FH	(101 Bytes)	-	Plug and Play Resource Data.

7.6.1. Detail Values of 9346 CONFIG1-3 Bytes

Table 44. Detail Values of 9346 CONFIG1-3 Bytes

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG1	*	IRQS2	IRQS1	IRQS0	IOS3	IOS2	IOS1	IOS0
CONFIG2	PL1	PL0	*	BS4	BS3	BS2	BS1	BS0
CONFIG3	PNP	FUDUP	LEDS1	LEDS0	*	*	PWRDN	ACTIVEB

Note: '' denotes irrelevant.*

Example: Plug and Play Resource Data for RTL8019AS (Total 73+5 bytes)

TAG	Plug and Play Version Number Item Byte: 0AH PnP Version: 10H Vendor Version: 10H	Length: Fixed	3 Bytes
TAG	ANSI Identifier String Item Byte: 82H Length Bits 7~0: 22H Length Bits 15~8: 00H Identifier String: 'REALTEK PLUG & PLAY ETHERNET CARD', 00H	Length: Variable	37 Bytes
TAG	Logical Device ID Item Byte: 16H Logical Device ID0~3: 4AH, 8CH, 80H, 19H Flag 0: 02H or 03H (Use 03H when Boot ROM is Enabled) Flag 1: 00H	Length: Fixed	7 Bytes
TAG	Compatible Device ID (NE2000 Compatible) Item Byte: 1CH Compatible ID0-3: 41H, D0H, 80H, D6H	Length: Fixed	5 Bytes If Given
TAG	I/O Format Item Byte: 47H I/O Information: 00H Min. I/O Base Bits 7~0: 20H Min. I/O Base Bits 15~8: 02H Max. I/O Base Bits 7~0: 80H Max. I/O Base Bits 15~8: 03H Base Alignment: 20H Range Length: 20H	Length: Fixed	8 Bytes
TAG	IRQ Format Item Byte: 23H IRQ Mask Bits 7~0: 38H IRQ Mask Bits 15~8: 9EH IRQ Mask Bits 15~8: 9EH IRQ Information: 01H	Length: Fixed	4 Bytes

TAG	Memory Format (Optional) Item Byte: 81H (This Example Uses 16k-Byte Boot ROM) Length Bits 7~0: 09H Length Bits 15~8: 00H Memory Information: 40H Min. Base Bits 15~8: 00H Min. Base Bits 23~16: 0CH Max. Base Bits 15~8: C0H Max. Base Bits 23~16: 0DH Base Alignment Bits 7~0: 00H Base Alignment Bits 15~8: 40H Range Length Bits 15~8: 40H Range Length Bits 23~16: 00H	Length: Fixed	12 Bytes
TAG	END Tag Item Byte: 79H Checksum: 2's complement of the sum of all the above resource data, i.e., 2's complement of (0AH+10H+10H+.....+79H).	Length: Fixed	2 Bytes

7.7. Boot ROM

Whether an EPROM or flash memory is used as the boot ROM, the RTL8019AS's boot ROM read operation is still the same as the RTL8019AS's. The supported boot ROM size is the same, too.

The write operation of a flash memory is much like the read except that a SMEMWB command is issued instead of SMEMRB. The block diagram below shows the application when an 128k*8bit flash memory (e.g. 29F010) is used as the boot ROM.

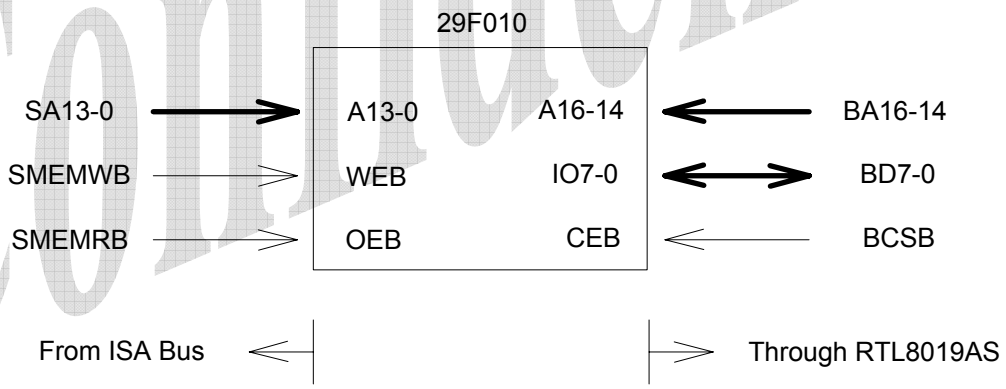


Figure 5. 128k*8bit Flash Memory (e.g. 29F010) used as the Boot ROM

In this case, the boot ROM page mode is used. Before either reading or writing boot ROM, the appropriate ROM page must be set in the BPAGE (page3, offset 02h) register first. The RTL8019AS will always reflect the content of BPAGE onto the BA14-21 bus. When the RTL8019AS decodes a valid boot ROM read or write command, it asserts BCSB low. Note the flash memory write must be enabled through the RTL8019AS's FMWP register before the host's flash write command.

7.8. LED Behavior

This section describes the lighting behavior of the LED output signals (selected by LEDS1 and LEDS0 bits in the Page3 CONFIG3 register).

Note: It is assumed that the LED is on when the signal goes low.

(1) LED_TX: Tx LED

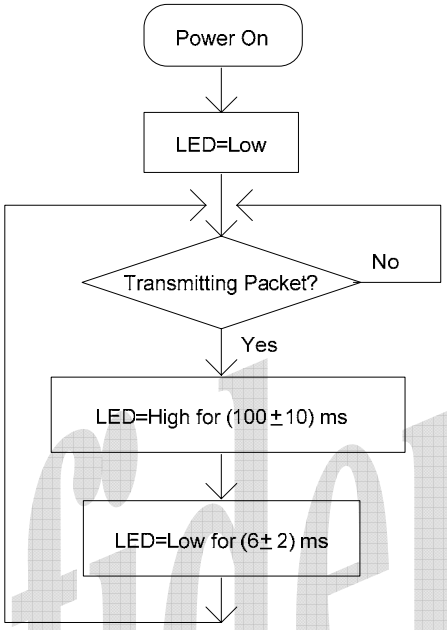


Figure 6. LED_TX: Tx LED

(2) LED_RX: Rx LED

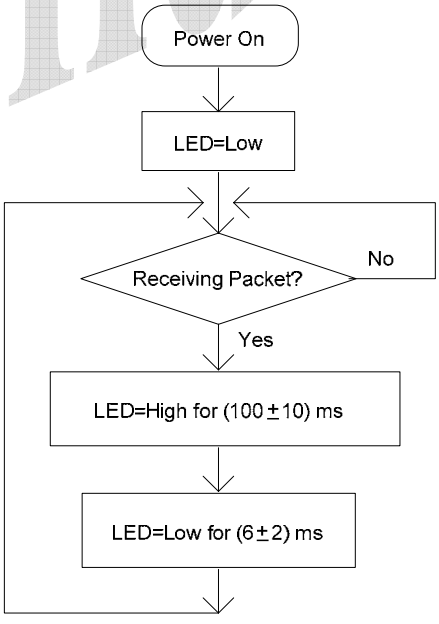


Figure 7. LED_RX: Rx LED

(3) LED_CRS=LED_TX+LED_RX: Carrier Sense LED

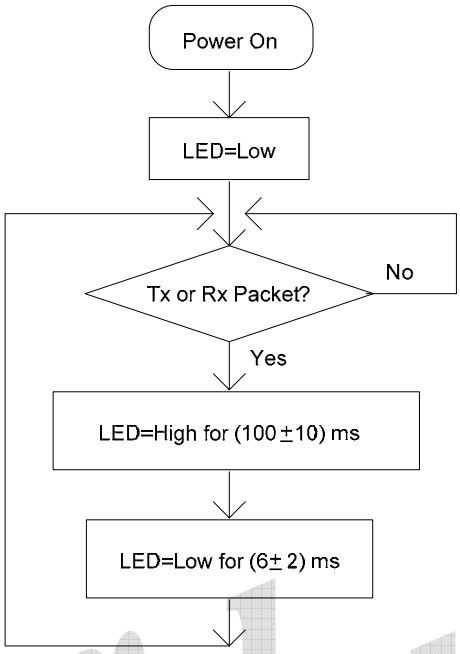


Figure 8. LED_CRS=LED_TX+LED_RX: Carrier Sense LED

(4) LED_COL: Collision LED

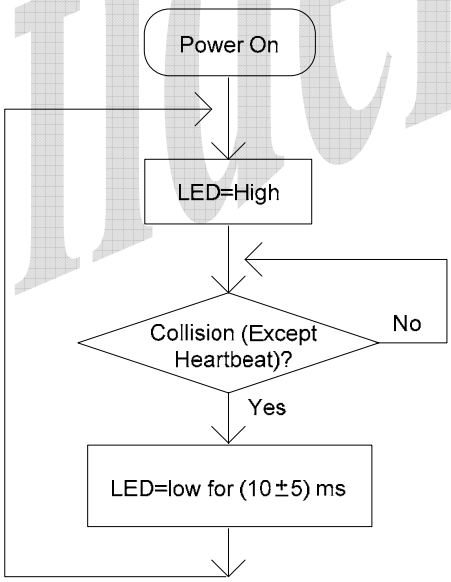


Figure 9. LED_COL: Collision LED

LED1 (LED_RX or LED_CRS)

The RTL8019AS's LED_RX or LED_CRS LED sometimes blinks continually when the media type of a 2-in-1 (UTP+BNC) LAN adapter is set to auto-detect and both UTP and coaxial cables are not connected. In the case, the RTL8019AS is actually using BNC, as the UTP link test failed. Some switches will falsely detect a carrier when the BNC interface is not properly terminated (e.g. coaxial cable is not connected). That carrier sense will then cause the RTL8019AS's LED_RX or LED_CRS to blink. Not all switches cause this LED blinking, which makes the phenomenon very ambiguous. Considering the phenomenon normally appears upon power on, we changed the RTL8019AS's original function to solve the problem to some extent.

The new specification is:

The LED_RX or LED_CRS does not reflect the carrier sense when the CR register bit 0 is set (in stop mode). Thus, the false carrier due to cabling problem upon power on will not cause the LED1 to blink anymore.

Table 45. LED Output States in Power Down Modes

LED Output	Normal Mode/Idle	Sleep Mode	Power Down Mode
LEDBNC	-	-	Low
LED_LINK	-	High	High
LED_COL	High	High	High
LED_TX	Low	High	High
LED_RX	Low	High	High
LED_CRS	Low	High	High

7.9. Loopback Diagnostic Operation

7.9.1. Loopback Operation

The RTL8019AS provides 3 loopback modes. Via a loopback test, we can verify the integrity of the data path, CRC logic, address recognition logic, and cable connection status.

Mode 1: Loopback through the NIC (LB1=0, LB0=1 in TCR)

The NRZ data is not transmitted to the SNI but instead is loopbacked to the NIC's Rx deserializer. The traffic on the cable is ignored.

Mode 2: Loopback through the SNI (LB1=1, LB0=0 in TCR)

The Manchester encoded data is not transmitted to the MAU. It is loopbacked through the SNI to the NIC. The traffic on the cable is ignored.

Mode 3: Loopback through the cable (LB1=1, LB0=1 in TCR)

The packets are transmitted via the MAU onto the network. The RTL8019AS receives all incoming packets (not only the MAU-loopbacked Tx data).

Alignment of the Reception FIFO

The reception FIFO is an 8-byte ring structure. The first received byte is put at location zero. When the location pointer gets to the end of the FIFO, it wraps to the beginning of the FIFO and overwrites the previous data. At the end of the packet reception, the FIFO contents are in the order (from the ring structure's view) as shown below.

(1) CRC Enabled (CRC bit in TCR=0)

- 1-byte received packet data
- 4-byte CRC
- 1-byte lower byte count
- 1-byte upper byte count
- 1-byte upper byte count

(2) CRC Disabled (CRC bit in TCR=1)

- 5-byte received packet data
- 1-byte lower byte count
- 1-byte upper byte count
- 1-byte upper byte count

7.9.2. Implement a Loopback Test

(1) Verify the integrity of the data path

- Set RCR=00h to accept physical packets
- Set PAR0~5 to accept packets
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Set TCR=02h, 04h, 06h to do loopback tests 1, 2, 3 respectively
- Set CRC enabled (CRC=0 in TCR)
- Clear ISR
- Tx a packet and check ISR
- Check FIFO after loopback

Note: Loopback mode 3 is sensitive to network traffic, so the values in the FIFO may not be correct.

(2) Verify CRC logic: Select a loopback mode (e.g., mode 2) to test

A. To test the CRC generator

- Set RCR=00h to accept physical packets
- Set PAR0~5 to accept packets
- Set TCR=04h (CRC enabled)
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Clear ISR
- Tx a packet
- Check CRC bytes in FIFO after loopback

B. Test the CRC checker

- Set RCR=00h to accept physical packets
- Set PAR0~5 to accept packets
- Set TCR=05h (CRC disabled)
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Clear ISR
- Tx a packet with good or bad CRC appended by program
- Check FIFO, ISR & RSR after loopback
  For bad CRC, expected: ISR=06h, RSR=02h (Tx: OK, Rx: CRC error)
  For good CRC, expected: ISR=02h, RSR=01h (Tx:OK, Rx: OK)

Note: In loopback mode, the received packets are not stored in SRAM, so the PRX bit in ISR is not set.

(3) Verify the Address Recognition Function: Select a loopback mode (e.g. mode 2) to test

A. Test Correct Physical Destination Address

- Set RCR=00h to accept physical packets
- Set PAR0~5 to accept packets
- Set TCR=04h (CRC enabled)
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Clear ISR
- Tx a packet
- Check ISR after loopback
  Expected: ISR=06h (packets accepted, Rx CRC error)

B. Test Incorrect Physical Destination Address

- Set RCR=00h to accept physical packets
- Set PAR0~5 to reject packets
- Set TCR=04h (CRC enabled)
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Clear ISR
- Tx a packet
- Check ISR after loopback
  Expected: ISR=02h (packets rejected, Rx no response)

(4) Test Cable Connection

There are four physical medium types in the RTL8019AS.

Perform Loopback Mode 3 to test the cable connection status:

- Set RCR=00h to accept physical packets
- Set PAR0~5 to accept packets
- Set TCR=06h (CRC enabled)
- Set DCR=40h (8-bit slot) or 43h (16-bit slot)
- Clear ISR
- Tx a packet
- Check TSR after loopback

A. 10Base-2

- If cable OK, get TSR=03h (Tx OK)
- If cable FAIL, get TSR=0Eh (Collision and Tx aborted)

B. 10Base-5

- If cable OK, get TSR=03h (Tx OK)
- If MAU connected but cable FAIL, get TSR=0Eh (Tx collision and Tx aborted)
- If MAU not connected, get TSR=53h (Carrier sense is lost during transmission and CD heartbeat fails)

C. 10Base-T with Link Test Disabled

The RTL8019AS disables the link test in this case, so cable OK or FAIL does not affect TSR; get TSR=03h.

D. Auto-detection (10Base-T with Link Test Enabled)

The RTL8019AS automatically switches from 10Base-T to 10Base-2 if the twisted-pair cable is not connected (10Base-T link test fails).

If twisted-pair cable is OK, get TSR=03h (Tx OK) & BNC=0 in CONFIG2

If twisted-pair cable FAILs but the coaxial cable is OK, get TSR=03h (Tx OK) & BNC=1 in CONFIG2

Otherwise, get TSR=0Eh (same as 10Base-2 connection fail).

8. Electrical Specifications and Timings

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 46. Absolute Maximum Ratings

Description	Ratings
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 140°C
All Outputs and Supply Voltages, with Respect to Ground	-0.5V to 7V
Power Dissipation	-

8.2. D.C. Characteristics (Tc=0°C to 70°C, Vcc=5V+5%)

Table 47. D.C. Characteristics (Tc=0°C to 70°C, Vcc=5V+5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vil	Input Low Voltage	-	-	0.8	V	-
Vih	Input Low Voltage	2.0	-		V	-
Vol1	Output Low Voltage 1	-	0.4	0.6	V	Iol=16mA, Note 1
Voh1	Output High Voltage 1	3.0	3.5		V	Ioh=8mA, Note 1
Vol2	Output Low Voltage 2	-	0.4	0.6	V	Iol=4mA, Note 2
Voh2	Output High Voltage 2	3.5	4.0	-	V	Ioh=4mA, Note 2
Vol3	Output Low Voltage 3	-	-	0.6	V	Iol=24mA, Note 3
Rpull-low	Internal Pull-Low Resistance	50	100	150	KW	-
II	Input Leakage Current	-10	-	10	mA	-

Note 1: Applies only to INT7 ~ INT0, SD15 ~ SD0.
Note 2: Applies only to MD7 ~ MD0, MA13 ~ MA0, LED Pins, EECS, MWRB, MRDB, BCSB.
Note 3: Applies only to IOCHRDY, IOCS16B.

8.3. A.C. Timing Characteristics

8.3.1. ISA I/O Read/Write

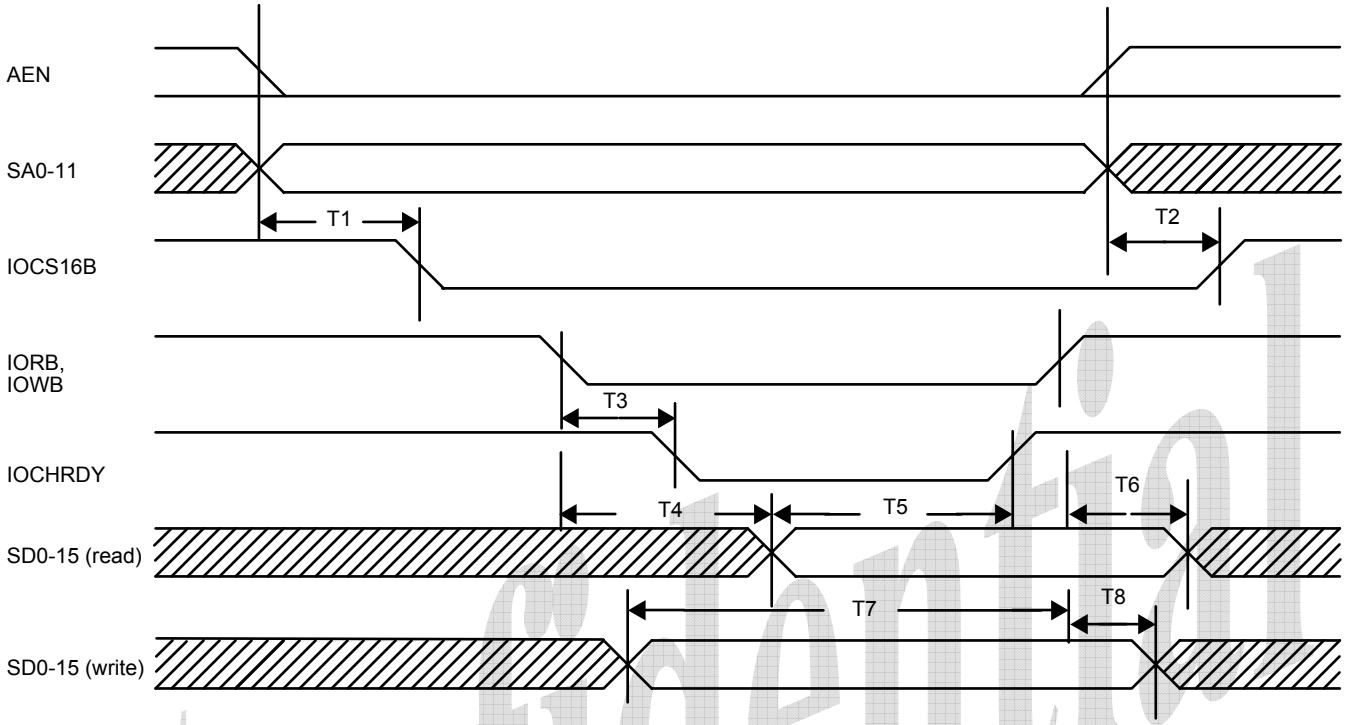


Table 48. ISA I/O Read/Write

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Host Address Valid to IOCS16B Low	8	20	20	ns
T2	Host Address Invalid to IOCS16B High	4	30	-	ns
T3	IOCHRDY Goes Low from Falling Edge of IORB or IOWB when Wait State Insertion is Needed	-	50	50	ns
T4	Read Data Valid from Falling Edge of IORB or IOWB when No Wait State Insertion is Needed	-	50	60	ns
T5	Read Data Valid to IOCHRDY High when Wait State is Needed	25	-	-	ns
T6	Read Data Hold after IORB Rising Edge	10	30	30	ns
T7	Write Data Setup to IOWB Rising Edge	10	10	-	ns
T8	Write Data Hold from IOWB Rising Edge	10	10	-	ns

8.3.2. Boot ROM Read

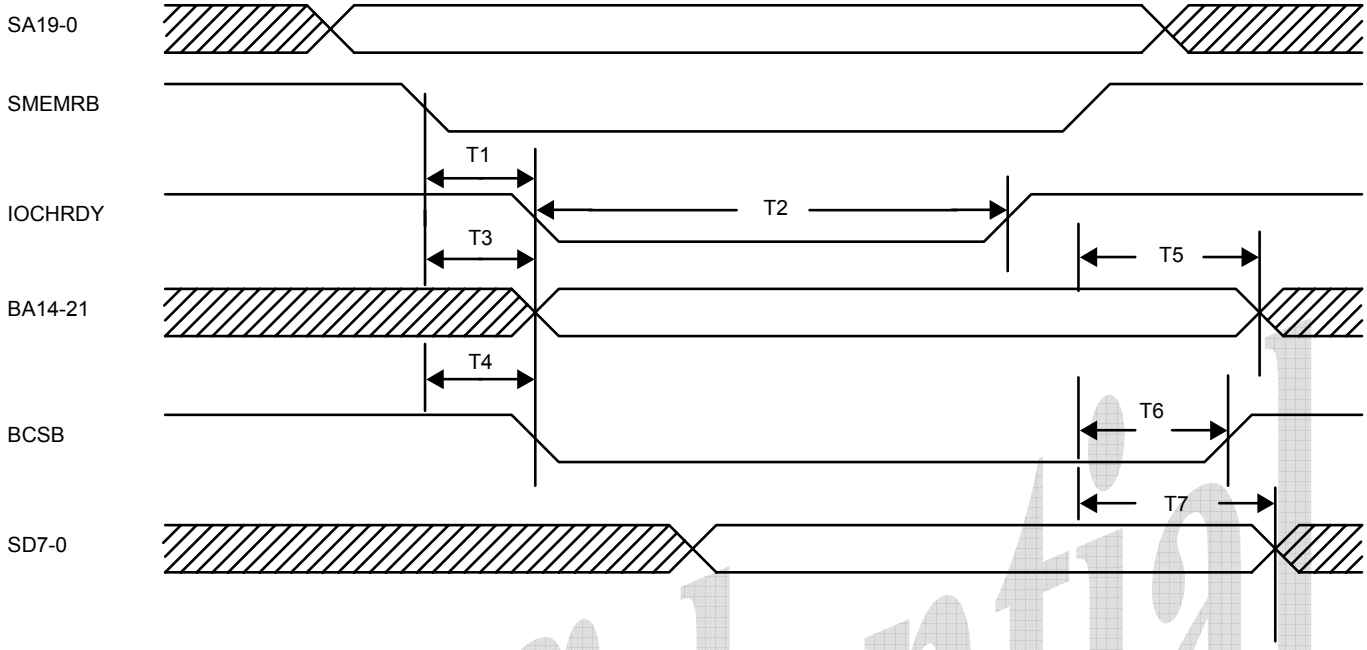
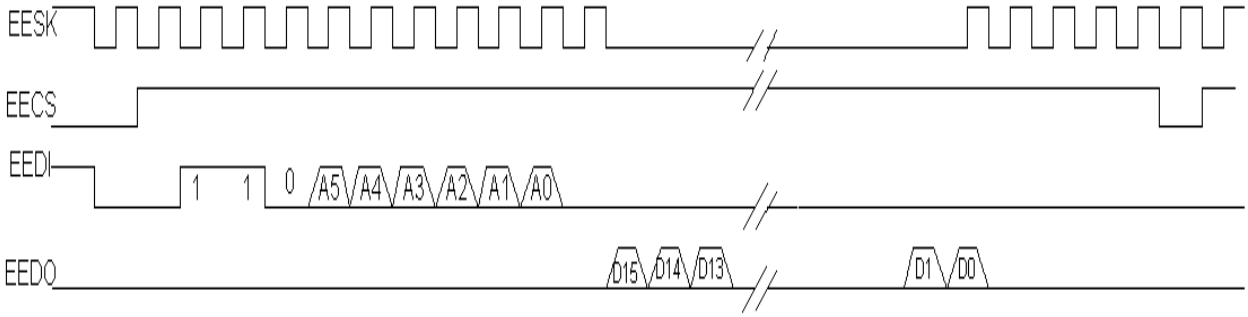


Table 49. Boot ROM Read

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SMEMRB Low to IOCHRDY Low	-	-	30	ns
T2	IOCHRDY Low Width	125	200	350	ns
T3	SMEMRB Low to BA14-21 Valid	-	-	30	ns
T4	SMEMRB Low to BCSB Valid	-	-	30	ns
T5	BA14-21 Hold from SMEMRB Rising Edge	-	-	30	ns
T6	BCSB Hold from SMEMRB Rising Edge	-	-	30	ns
T7	Read Data Hold from SMEMRB Rising Edge	-	-	30	ns

8.3.3. Serial EEPROM (9346) Auto-Load



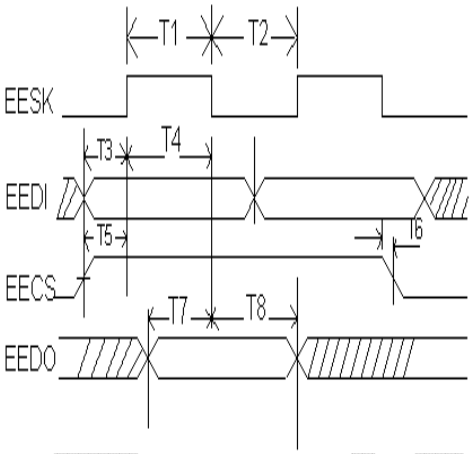
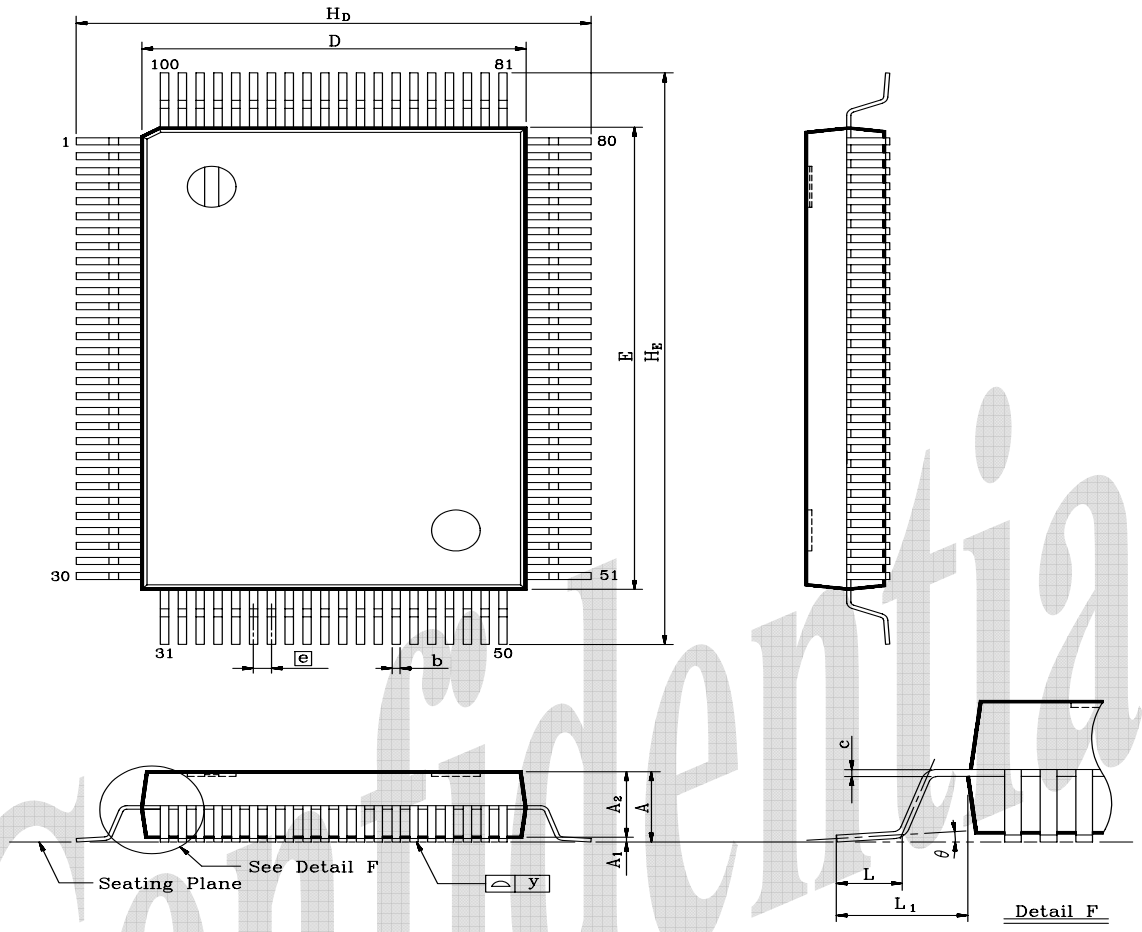


Table 50. Serial EEPROM (9346) Auto-Load

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EESK High Width	-	3.2	-	ms
T2	EESK Low Width	-	3.2	-	ms
T3	EEDI Setup to EESK Rising Edge	3.0	-	-	ms
T4	EEDI Hold from EESK Rising Edge	3.0	-	-	ms
T5	EECS Goes High to EESK Rising Edge	3.0	-	-	ms
T6	EECS Goes Low from EESK Falling Edge	-	0	-	ns
T7	EEDO Setup to EESK Falling Edge	20	-	-	ns
T8	EEDO Hold from EESK Falling Edge	10	-	-	ns

9. Mechanical Dimensions



Symbol	Dimension in mil			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	106.3	118.1	129.9	2.70	3.00	3.30
A_1	4.3	20.1	35.8	0.11	0.51	0.91
A_2	102.4	112.2	122.0	2.60	2.85	3.10
b	7.1	11.8	16.5	0.18	0.30	0.42
c	1.6	5.9	10.2	0.04	0.15	0.26
D	541.3	551.2	561.0	13.75	14.00	14.25
E	777.6	787.4	797.2	19.75	20.00	20.25
e	19.7	25.6	31.5	0.50	0.65	0.80
H_D	726.4	740.2	753.9	18.45	18.80	19.15
H_E	962.6	976.4	990.2	24.45	24.80	25.15
L	39.4	47.2	55.1	1.00	1.20	1.40
L_1	88.6	94.5	104.3	2.25	2.40	2.65
y	-	-	3.9	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 100PQFP (14x20 mm2) FOOTPRINT 4.8 mm			
PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
APPROVE		DWG NO.	
		REV NO.	
		SCALE	
CHECK	Ricardo Chen	DATE	
		SHT NO.	1 OF
REALTEK SEMICONDUCTOR CORP.			

10. Ordering Information

Table 51. Ordering Information

Part Number	Package	Status
RTL8019AS	100-Pin PQFP	MP
RTL8019AS-LF	RTL8019AS in Lead (Pb)-Free Package	MP

Note: See page 3 for package identification information.

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