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RTL8401-GR
PCI EXPRESS FAST ETHERNET CONTROLLER WITH INTEGRATED 1-LUN CARD READER CONTROLLER

RTL8401P-GR
PCI EXPRESS FAST ETHERNET CONTROLLER WITH INTEGRATED SWITCHING REGULATOR & 1-LUN CARD READER CONTROLLER

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the RTL8401(P) Ethernet controller.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/11/27	First release.

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1. Introduction

The Realtek RTL8401-GR and RTL8401P-GR Fast Ethernet controllers (hereafter referred to as RTL8401(P)) combine a 10/100M IEEE 802.3 compliant Media Access Controller (MAC) with a 10/100M Ethernet transceiver, PCI Express bus controller, and embedded One-Time-Programmable (OTP) memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8401(P) offers 10/100M transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, and timing recovery are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.1 bus interface for host communications with power management and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8401(P).

The RTL8401(P) is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The device also features next-generation interconnect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8401(P) is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8401(P). Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8401(P).

(3) Simplify the task of routing signal traces.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8401(P), good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV peak-to-peak)
- Keep power and ground noise levels below 100mV peak-to-peak
- Verify that critical components such as the clock source and transformer meet application requirements
- Use bulk capacitors (10µF~22µF) between the power and ground planes
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep de-coupling capacitors as close as possible to the RTL8401(P) (within 200 mils)
- Provide termination on all high-speed switching signals
- Route the signal trace as short as possible
- Use a smaller package for the capacitor to reduce the package inductance

Use the following signal integrity techniques to reduce crosstalk.

- Shorter parallel routes
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane

PCI Express TX/RX differential pairs should comply with the following requirements:

- Differential Return Loss ≥ 10dB (measured within a 50MHz~1.25GHz range)
- Common Mode Return Loss ≥ 6dB (measured within a 50MHz~1.25GHz range)
- Differential Impedance should be limited from 80 to 120ohms (100ohm recommended)
- Only PCB traces are allowed for signal routing (do not use flat/shielded cable)

2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location
- Avoid vias and layer changes if possible
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane if possible
- 0.1µF common mode noise filter capacitors should be placed near the RTL8401(P) chip
- Ninety-degree trace angles should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts

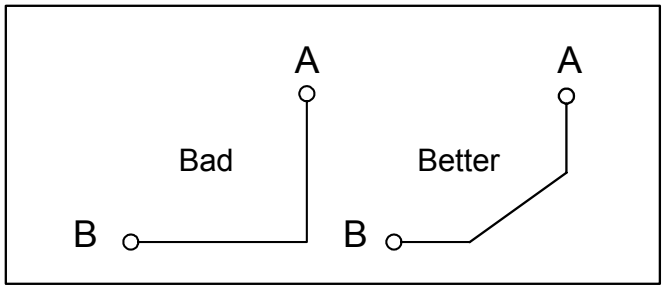

Figure 1. Signal Trace Angles

2.3. Placing the RTL8401(P)

- The RTL8401(P) should be placed as close as possible to the magnetics

2.4. Magnetics

- The 10/100M magnetics should be placed as close as possible to the RJ-45 connector
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other

2.5. Crystal

- The Crystal should be placed away from I/O ports, important or high frequency signal traces (Tx, Rx, power), magnetics, and board edges
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI
- The retaining straps of the OSC, if any, need good grounding

2.6. Ferrite Beads and De-Coupling Capacitors

Each PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

3. Signal and Trace Routing

Noise, ringing, and data lines should be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Traces routed from the RTL8401(P) to the 10/100M magnetics, and to the RJ-45 connector, should be as short as possible. The 20cm maximum length between the RTL8401(P) and magnetics is achievable only when there is no interference. It is also very important to keep all two differential pair signal traces (MDI0+/-, MDI1+/-) equal in length. The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. The width of D1 should be calculated to have 100Ω impedance (Figure 2).

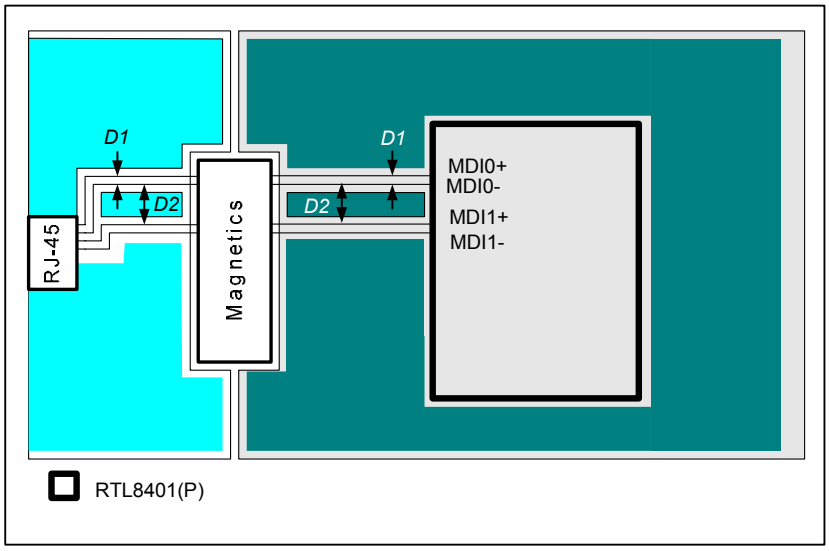

Figure 2. Signal & Trace Routing

- We suggest that there should be a minimum of 30-mil spacing between different differential pairs to minimize cross-talk coupled from other pairs (D2 in Figure 2). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, we recommend not to use vias on the four differential pairs
- Avoid right angle signal traces. Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1 , page 3. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.
- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them.
- It is important to separate Digital Signals (e.g., BOOTROM, Flash, EEPROM) from Analog Signals (e.g., MDI0+/-, MDI1+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles.
- The power into the RTL8401(P) digital power pins can be improved with de-coupling capacitors. The Power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8401(P) need to be de-coupled with a capacitor. The de-coupling capacitors should be placed as close to the IC as possible and the traces should be kept short.
- The PCI-Express signal differential pairs should be 5 mils wide, with a spacing of 7 mils between them (REFCLK+ & REFCLK-, HSOP & HSON, HSIP & HSIN). The length difference of the signals in a pair should not exceed 5 mils. For example, if HSON is 900 mils and HSOP is 890 mils, it may result in data transmit error.

4. Ground and Power Plane Layout

4.1. Ground Plane Layout

There is only one ground plane for analog power (HV33 in the RTL8401; HV/HV33_2 in the RTL8401P), digital power (DVDD3 in the RTL8401; DVDD33 in the RTL8401P), and PCI-Express power (EVDD3). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 3.8mm x 3.8mm. The PCB layout requires 9 vias to connect the EPAD to the lower layer ground plane (see Figure 3).

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

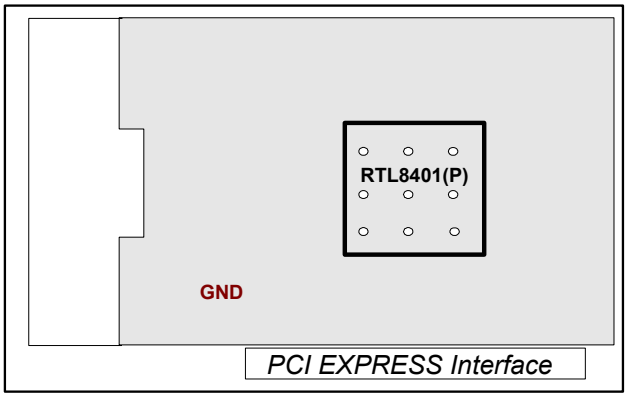

Figure 3. Ground Plane Layout-1

To achieve better ground plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 4 illustrates a not so good (left) and a good ground plane layout (right).

Figure 4. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 5).

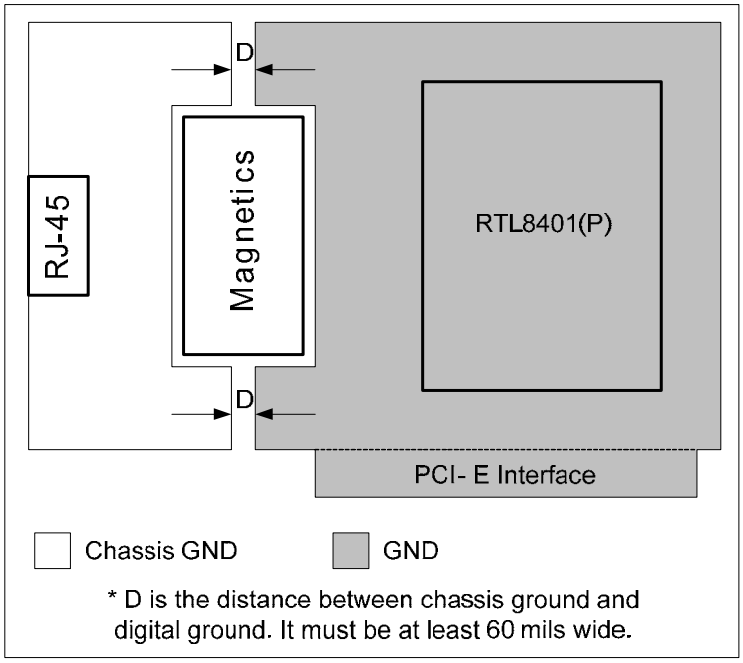

Figure 5. Ground Plane Separation

The Chassis Ground as shown in Figure 5 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is also important to keep the gap (D in Figure 5) between Chassis GND and System GND wider than 60 mils for better isolation.

4.2. Power Plane Layout

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. We recommend to use at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8401(P). If it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

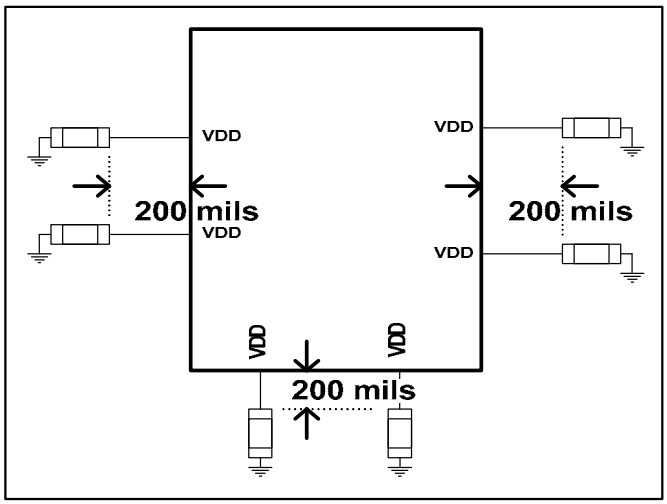

Figure 6. Decoupled Capacitor Example

(b) Use a Ferrite Bead or 0 ohm Resistor to connect Digital and Analog Power

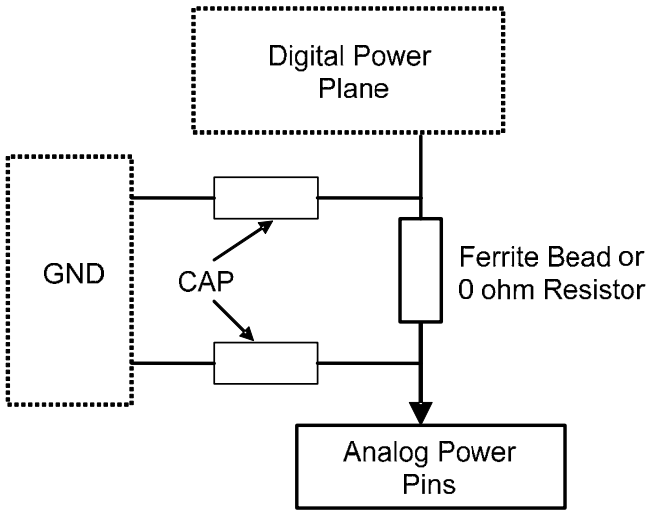

Figure 7. Power Plane

To further improve the performance of the power plane, try to keep the contact area between the RTL8401(P) VDD pins and power plane as large as possible rather than using small narrow traces (Figure 8).

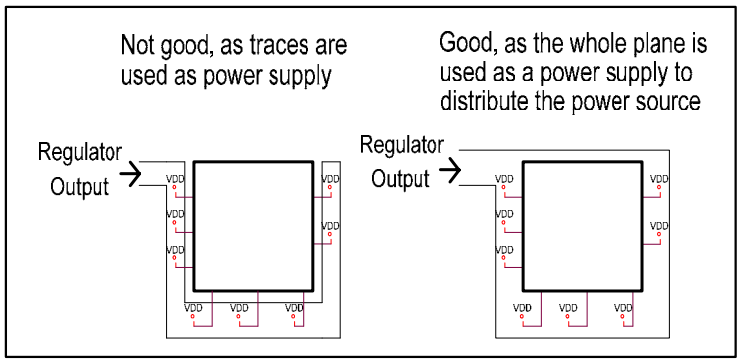

Figure 8. Power Source Distribution

- Keep power noise levels below 100mV peak-to-peak
- All 3.3V/1.2V decoupling capacitors shown in the reference schematic should be used in all designs
- Keep the analog power (1.2V) plane as whole and as large as possible

4.3. Four-Layer Board Plane Layout

1. Signal 1 (top layer)

2. GND

3. Power

4. Signal 2 (bottom)

4.3.1. Signal 1 Plane Layout (Top Layer)

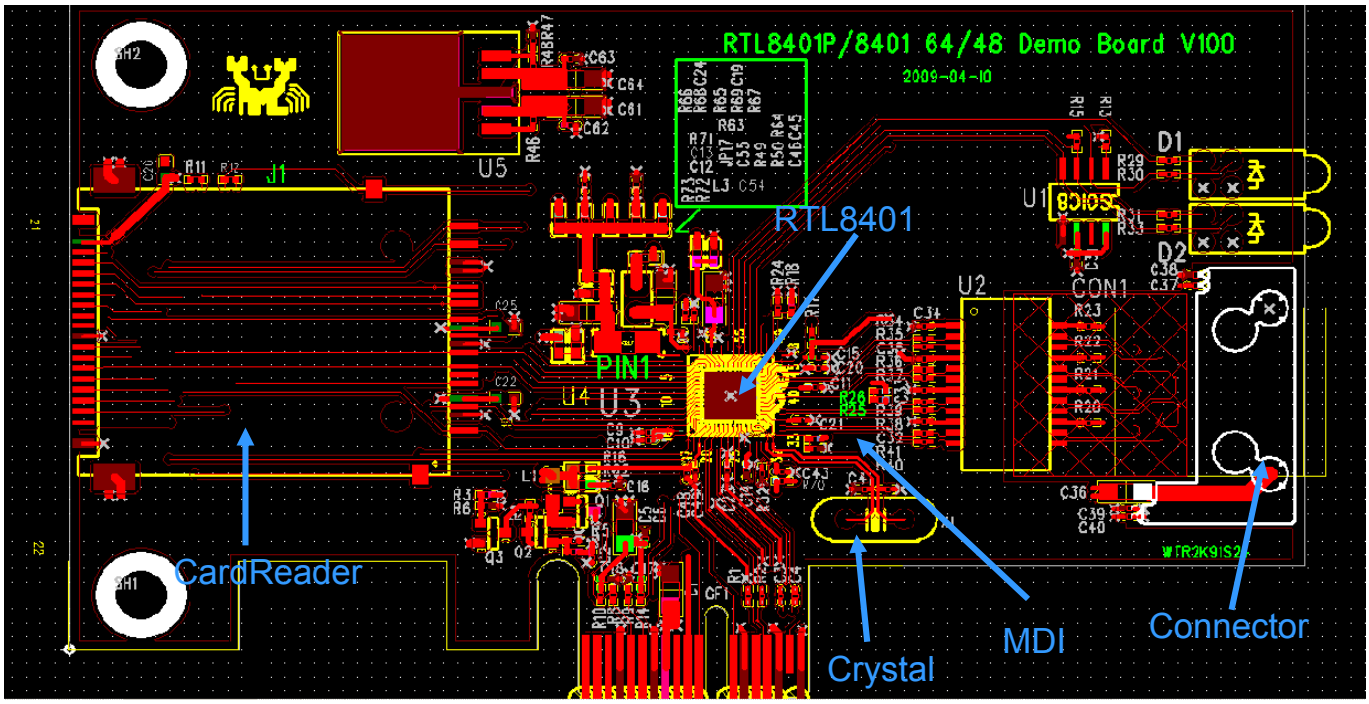

Figure 9. Signal 1 Plane Layout (Top Layer)

4.3.2. Ground Plane Layout (Layer 2)

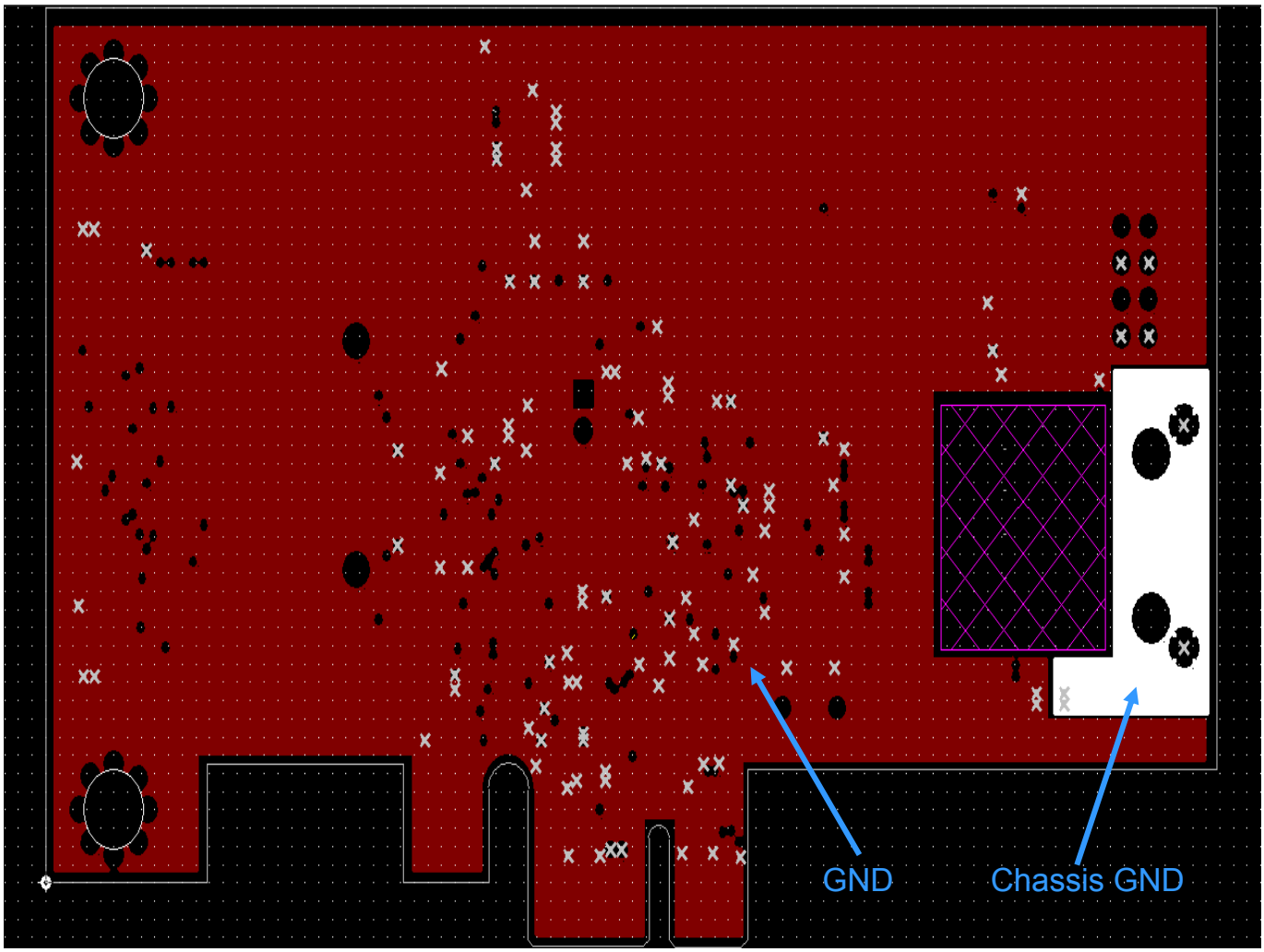

Figure 10. Ground Plane Layout (Layer 2)

4.3.3. Power Plane Layout (Layer 3)

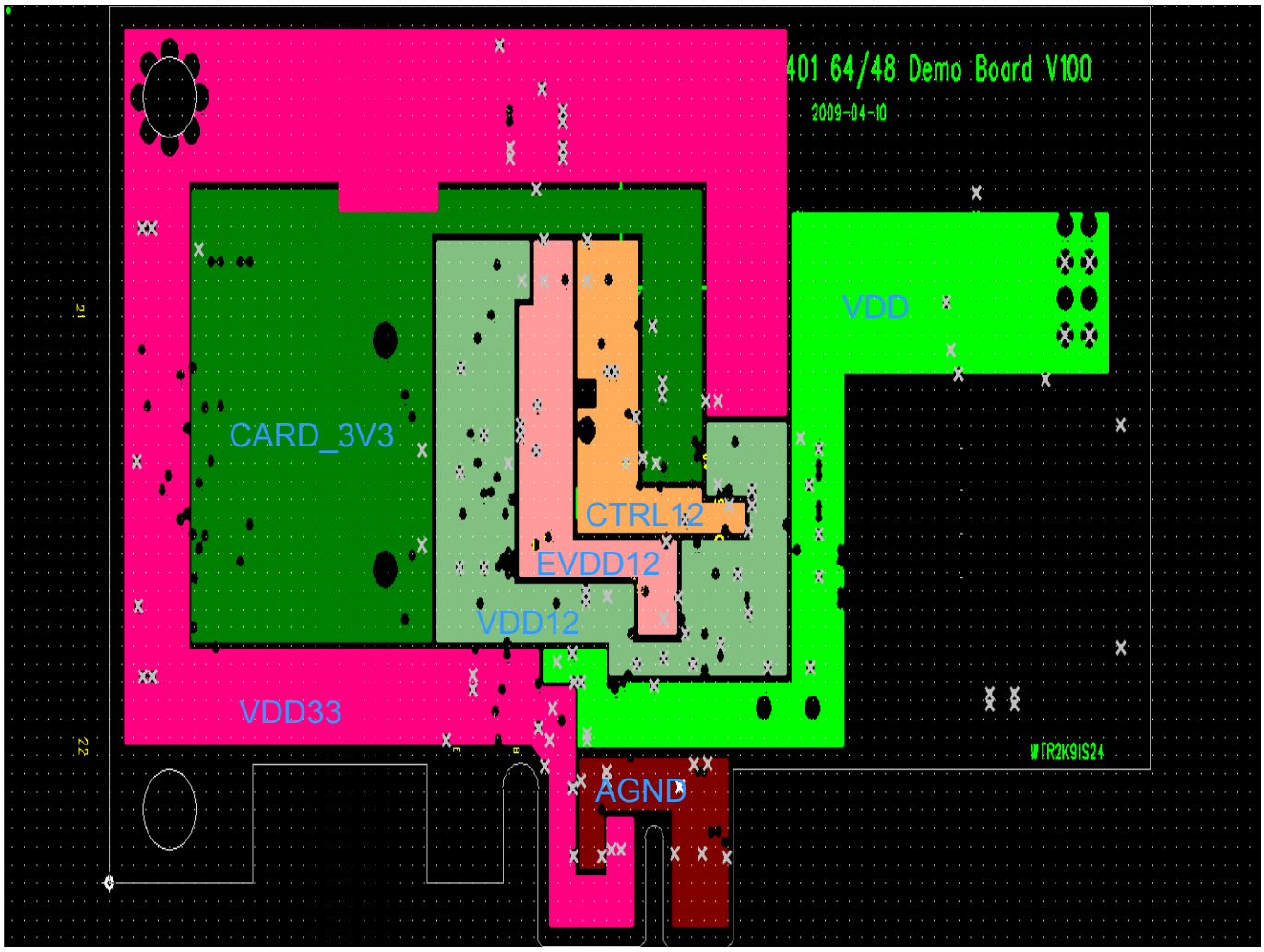

Figure 11. Power Plane Layout (Layer 3)

4.3.4. Signal 2 Plane Layout (Bottom Layer)

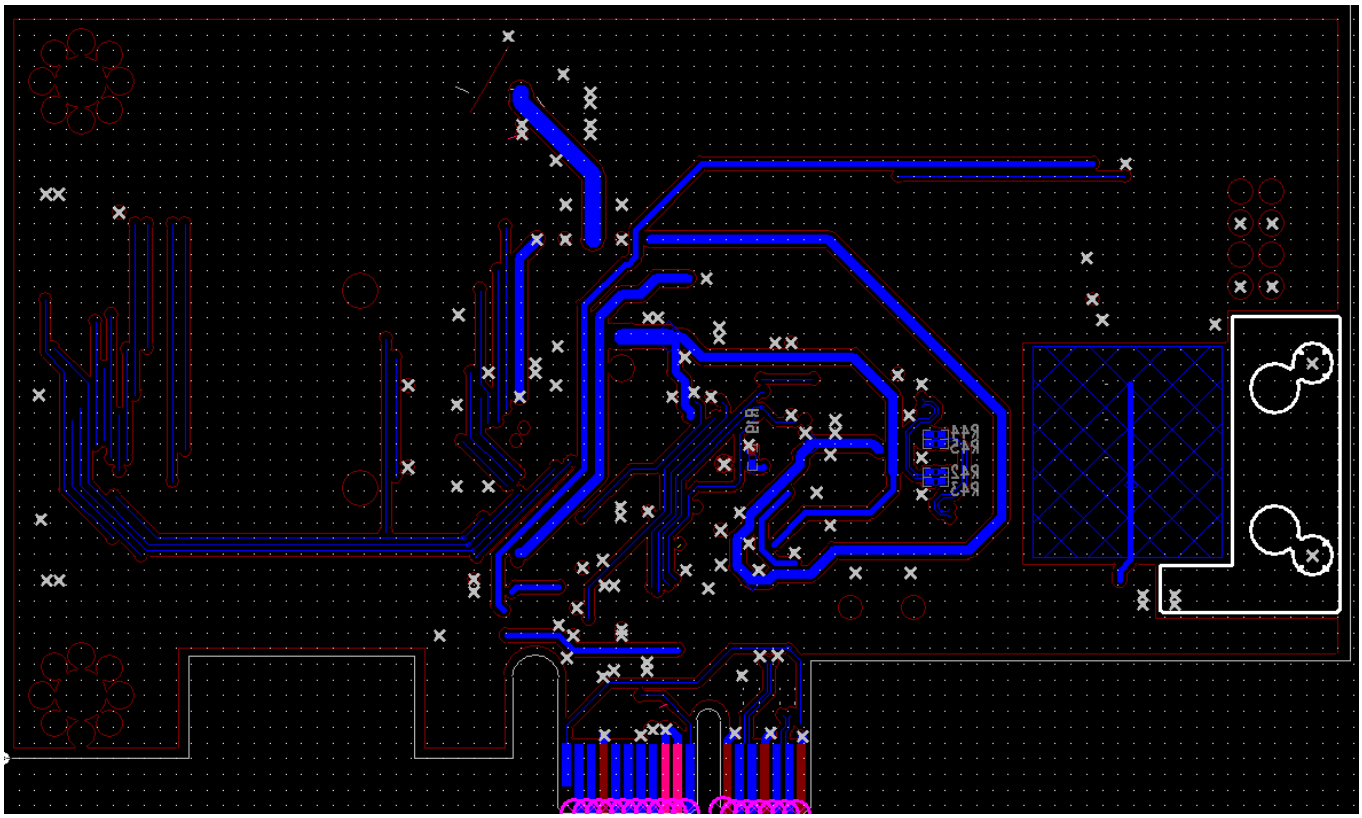

Figure 12. Signal 2 Plane Layout (Bottom Layer)

5. Center-Tapping

- A center-tapped fine-tuned capacitor (C1 Value: 0.1µF~10pF) can improve EMI for single tone noise. The capacitor default is NC
- Changing the R1 resistor to a capacitor (Value: 0.1µF~10pF), and fine-tuning the connection to GND can improve EMI for single tone noise. The resistor default is 0 ohm

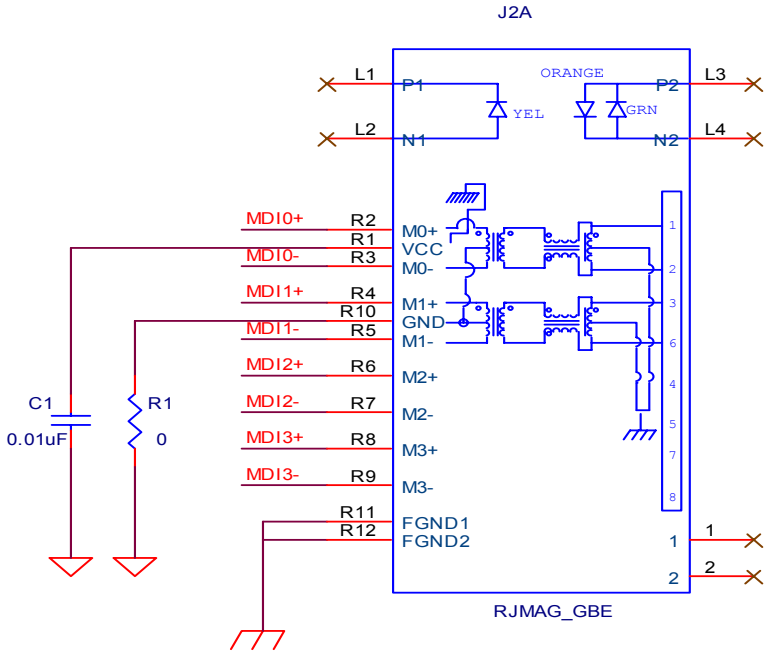

Figure 13. Center-Tapping

- When using a separate transformer, the center-tap MUST be aggregated (C35 Value: 0.1µF~50pF) (see Figure 14)

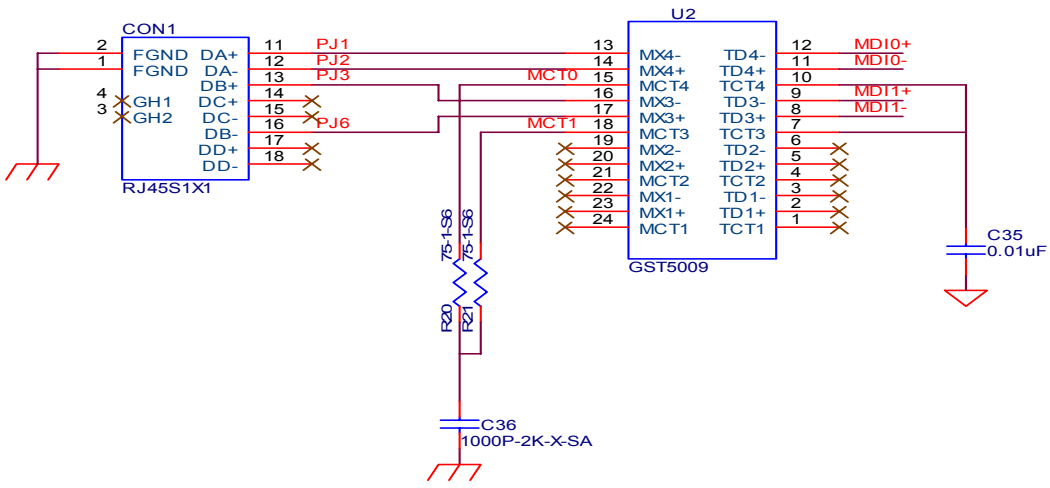

Figure 14. Separate Transformer

6. Switching Regulator (RTL8401P Only)

The RTL8401P incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.2V output pin (REGOUT) must be connected only to CTRL12D, CTRL12A, and VDDTX (do not provide this power source to other devices).

6.1. Inductor and Capacitor Parts List

Table 1. Inductor and Capacitor Parts List

Inductor Type	Inductance	ESR at 1MHz (mΩ)	Max IDC (mA)	Variation	Output Ripple (mV)
4R7GTSD32	4.7µH	712	1100	≤ 20%	12.6
6R8GTSD32	6.8µH	784	900	≤ 20%	12
6R8GTSD53	6.8µH	737	1510	≤ 20%	10.4

Note 1: The ESR is equivalent to RDC or DCR. Lower ESR inductor values will promote a higher-efficiency switching regulator.

Note 2: The power inductor used by the switching regulator should be able to withstand 600mA of current.

Note 3: Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 6.3 Efficiency Measurement, page 21.

Capacitor Type	Capacitance	ESR at 1MHz (mΩ)	Output Ripple (mV)
22µF 1210 TDK	21.5µF	33.53	9.6
22µF 1210 X5R	22.15µF	34.11	10.4

Note: Capacitors (C18 & C82) are must be ceramic due to their low ESR value. Lower ESR values will yield lower output voltage ripple.

6.2. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at VDDREG pin, not at the capacitor. In order to reduce the input voltage overshoot, C82 and C83 must be placed close to VDDREG pin. The following figures show what a good input voltage and a bad one look like.

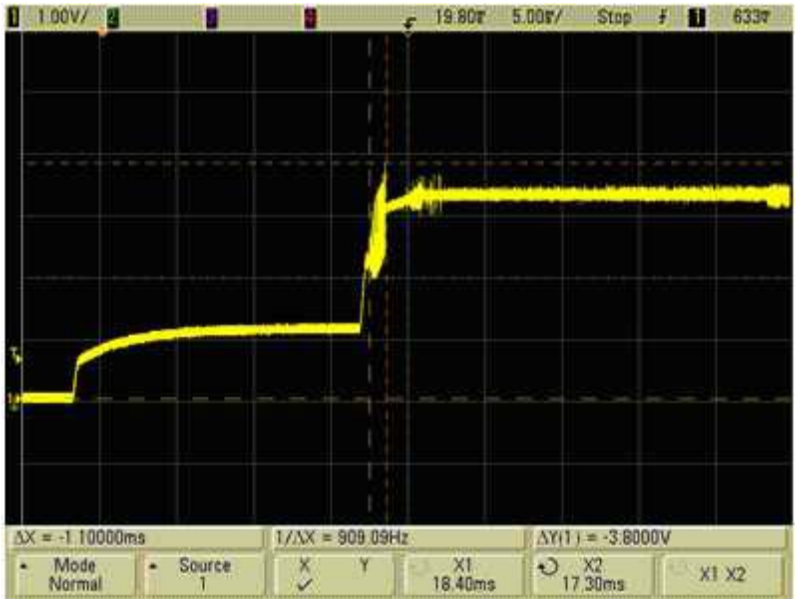

Figure 15. Input Voltage Overshoot <4V (Good)

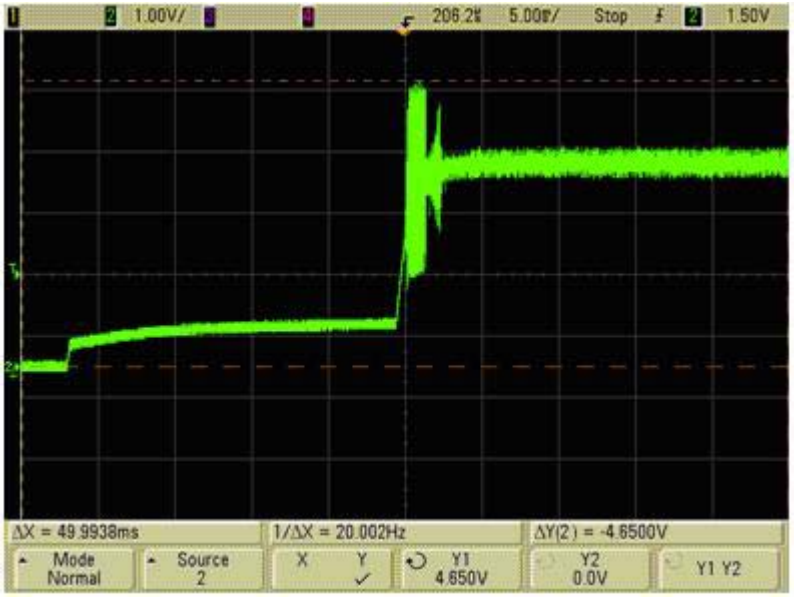

Figure 16. Input Voltage Overshoot >4V (Bad)

From the output side measured at Pin 1, the voltage ripple must be within 100mV. Choosing different types and values of output capacitor (C18, C19) and power inductor (L1) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of REGOUT pin before the power inductor (L1). The yellow signal (second row) is measured after the power inductor (L1), and shows there is a voltage ripple. The green signal (lower row) is the current.

Figure 17. Ceramic 22µF 1210(X5R) (Good)

Figure 18. Ceramic 22µF 0805(Y5V) (Bad)

A ceramic 22µF (X5R) will have a lower voltage ripple compared to an electrolytic 100µF. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 22µF 0805 (Y5V) in this case will cause malfunction of the switching regulator. Placing several Electrolytic capacitors in parallel will help lower the output voltage ripple.

Figure 19. Electrolytic 100µF (Ripple Too High)

The following figures show how different inductors affect the PIN 1 output waveform. The typical waveform should look like Figure 20, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 21, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system.

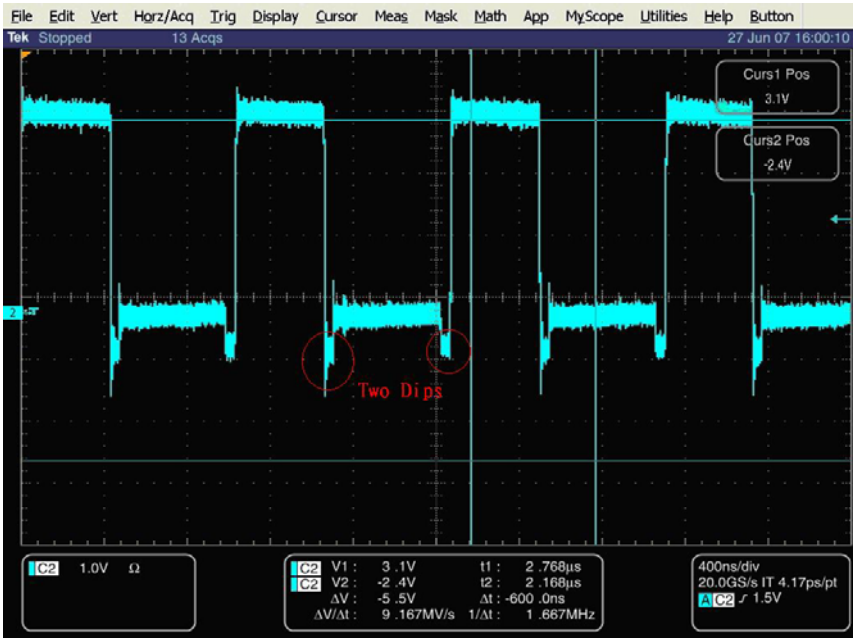

Figure 20. 4R7GTSD32 (Good)

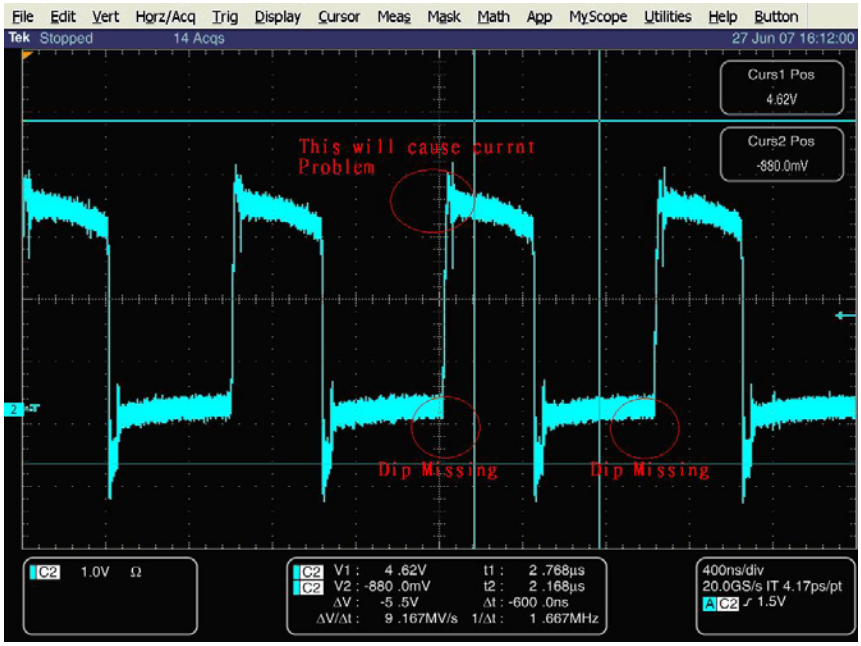

Figure 21. 1µH Bead (Bad)

6.3. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in 100M traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher-efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 22, page 22, shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

Efficiency = Vcpb*Icpb / Vcpa*Icpa

Where Vcpb is 1.2V; Vcpa is 3.3V. The measurements should be performed in 100M traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

- The ESR value @ 1MHz is approximately 0.712ohm
- The measured Icpa is 127mA at CP_A
- The measured Icpb is 54mA at CP_B

These values are measured in 100M traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

Efficiency = (1.2V*127mA) / (3.3V*54mA) = 0.86 = 86%.

We strongly recommend that when choosing an inductor for the switching regulator, the efficiency should be measured, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability in the long run.

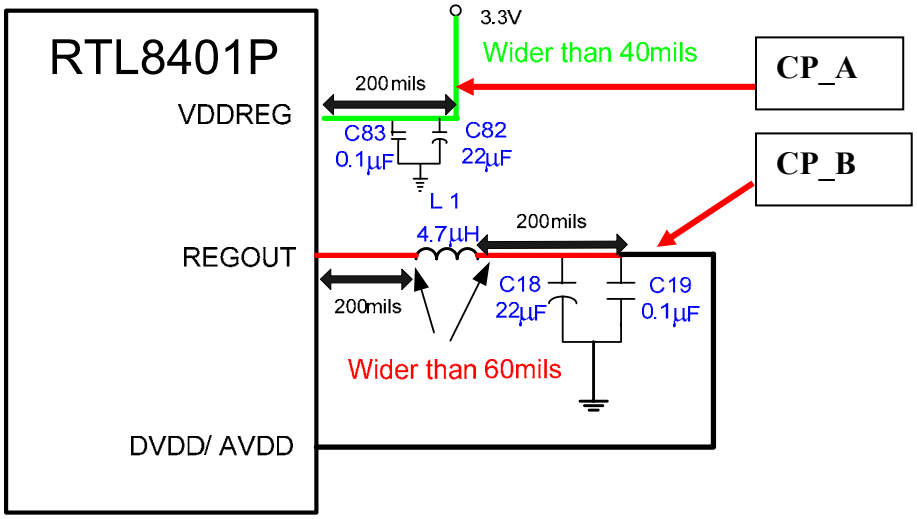

Figure 22. Switching Regulator Efficiency Measurement Checkpoint

6.4. PCB Layout

- The input 3.3V power trace connected to VDDREG pin should be wider than 40 mils
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200 mils (0.5cm) of VDDREG pin to prevent input voltage overshoot
- The output power trace out of REGOUT pin should be wider than 60 mils
- Keep L1 within 200 mils (0.5cm) of REGOUT pin
- Keep C18 and C19 within 200 mils (0.5cm) of L1 to ensure stable output power and better power efficiency
- For switching regulator stability, the capacitor C18 and C82 must be a ceramic (X5R) capacitor. C19 and C83 are recommended to be ceramic capacitors
- Place L1 and C82 on the same layout as the RTL8401P. Do not use vias on VDDREG and REGOUT traces

Note: Violation of the above rules will damage the IC.

6.5. Power Sequence

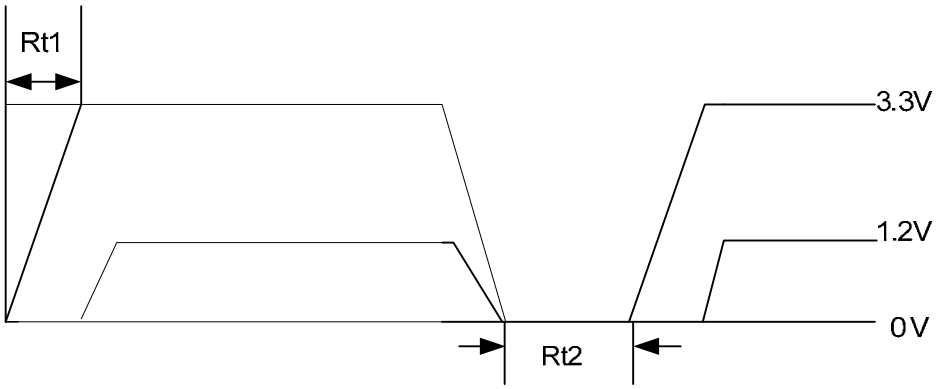

Figure 23. Power Sequence

Table 2. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	1	-	100	ms
Rt2	3.3V Off Time	200	-	-	ms

Note 1: The RTL8401P does not support fast 3.3V rising. The 3.3V rise time must be controlled over 1ms. If the rise time is too short it will induce a peak voltage in the VDDREG pin, which may cause permanent damage to the switching regulator.

Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the designer must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.2V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 200ms.

7. Parts Recommendations

7.1. 10/100M Magnetic

Turn Ratio Tx/Rx: 1:1

Primary Inductance: 350µH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Pulse H5007 or similar

7.2. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to CKXTAL1 pin and CKXTAL2 pin. Shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz
Temperature Stability	±10ppm
Duty Cycle	50%±10%
Tolerance	±50ppm
ESR	Max 30Ω
Broadband Peak-to-Peak Jitter*	Max 150ps
Aging	5ppm/year, max.

Note: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

7.3. Resistors

Resistors that have tolerance requirements within 1%, are strongly recommended. Refer to the provided BOM for suggested schematics.

7.4. Capacitors (RTL8401P Only)

For switching regulator power filtering, use X5R Ceramic capacitors for the power circuit. See section 6.1 Inductor and Capacitor Parts List, page 16, for the recommended parts list.

7.5. Ferrite Bead

The ferrite bead used should be of at least 100Ω@100MHz impedance with a rated current of 300mA or higher.

7.6. Power Inductor (RTL8401P Only)

The power inductor used by the switching regulator should be able to withstand 600mA of current, and the resistance value should be as small as possible to achieve the expected switching regulator efficiency which must be higher than 75%.

Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 6.3 Efficiency Measurement, page 21.

7.7. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

7.8. MS_CLK and SD_CLK Trace Routing

- Keep trace routing length as short as possible
- Avoid via and layer changes
- When the MS_CLK/SD_CLK traces run parallel to other signal trace edges, maintain at least an air gap of double MS_CLK/SD_CLK trace width to the edge of the other signal traces (Figure 24)
- Use a guard ground to isolate MS_CLK/SD_CLK trace is recommended (Figure 25)
- Do not route other signals under MS_CLK/SD_CLK traces
- Characteristic impedance of traces should be 50±15%
- Trace width: 4 mils (minimum)
- Via usage: No more than 2 vias is recommended
- Trace length: 4 inches (maximum); Via size: Pad ≤25 mils; Finished hole ≤14 mils

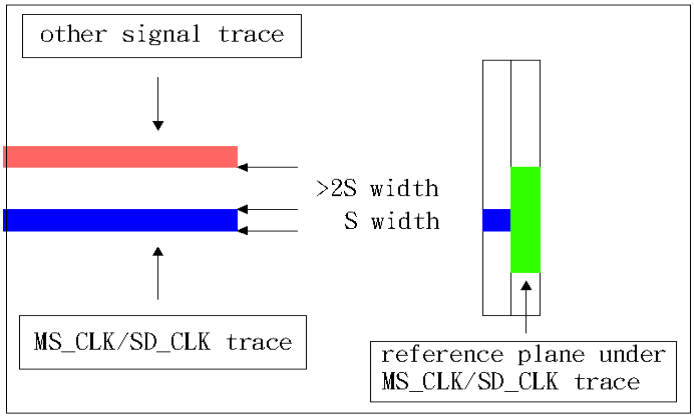

Figure 24. MS_CLK/SD_CLK Traces

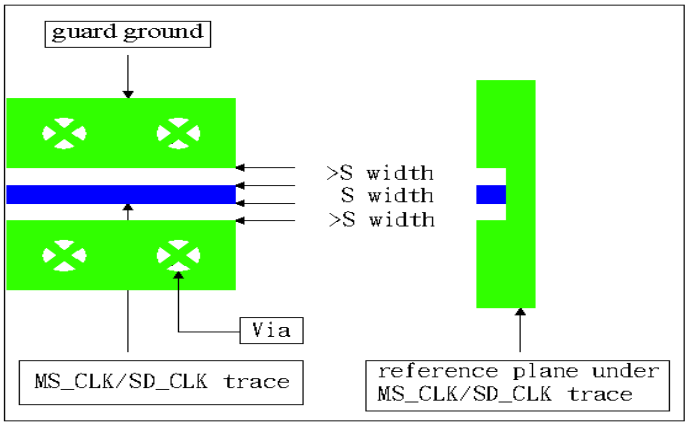

Figure 25. Use a Guard Ground to Isolate MS_CLK/SD_CLK Traces (Recommended)

7.9. Flash Card Signal Trace Routing

- Characteristic impedance of traces is 50Ω±15%
- Trace width: 4 mils (minimum)
- Trace length: 4 inches (maximum)
- Via usage: No more than 2 vias are recommended (signal quality impact from vias is more severe than longer trace lengths)
- If possible, do not route signal traces parallel to, near to, or under D+/D-/XTLI/XTLO/ MS_CLK/SD_CLK signal traces
- Flash card signal traces should have the same routing rule, length, width, and shape if possible
- We recommend not to route signal traces under the RTL8401(P) IC or flash memory card socket
- Avoid placing signal traces in the GND or POWER layers
- Follow the 3-W rule for reduced crosstalk affect
- Via size: Pad ≤ 25 mils; Finished hole ≤ 4 mils

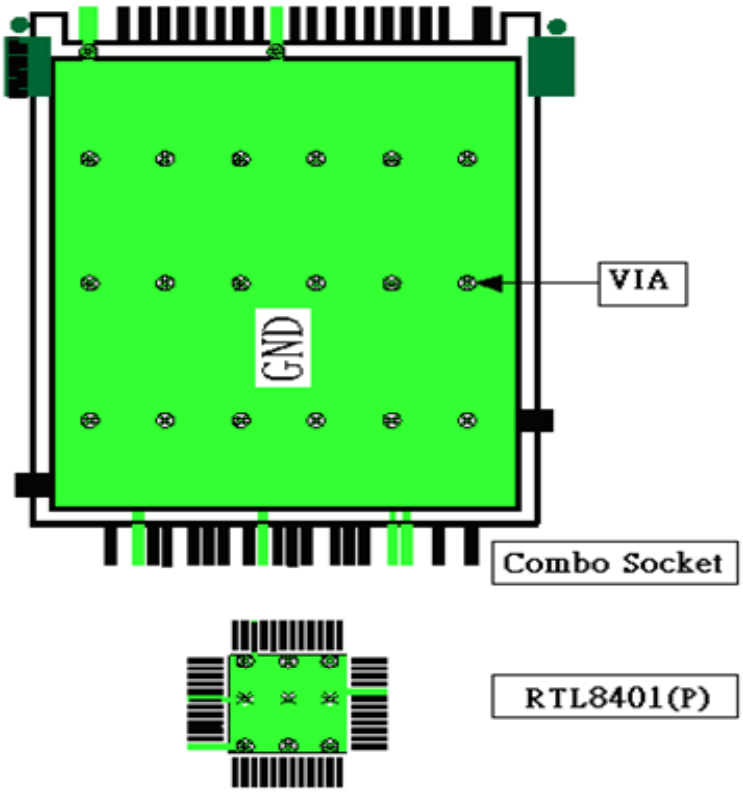

Figure 26. Signal Traces of Flash Memory Card Socket

8. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for Fast Ethernet applications.

- If it is found that there is a serious EMI issue, de-coupling capacitors (0.01µF, 10µF) can be added between the system GND and power planes
- When using the oscillator as the clock source for 25MHz, avoid connecting any capacitors to the clock circuitry
- To achieve proper skew rate requirements, the digital bus traces for BOOTROM and EEPROM should have lengths as equal as possible
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions
- The RTL8401(P) incorporates a state-of-the-art linear regulator. If the linear regulator is implemented, the 1.2V output pins must not be provided to other devices

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