RTL8218E-CG

INTEGRATED OCTAL 10/100/1000M ETHERNET TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 0.1
29 July 2020

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8218E IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.1	2020/07/29	First Draft.

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1. General Description

The RTL8218E-CG integrates octal independent 10/100/1000M Ethernet transceivers into a single IC, and performs all the physical layer (PHY) functions for 1000Base-T, 100Base-TX, and 10Base-T Ethernet on category 5 UTP cable except 1000Base-T half-duplex. 10Base-T functionality can also be achieved on standard category 3 or 4 cable.

This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The RTL8218E also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the four independent transceivers features an innovative XSGMII / QSGMII / O-USGMII for reduced PCB traces. All transceivers can communicate with the MAC simultaneously through the same XSGMII.

2. Features

- Octal-port integrated 10/100/1000M Ethernet transceiver
- Each port supports full duplex in 10/100/1000M mode (half duplex is only supported in 10/100M mode)
- Supports XSGMII (Ten-Gigabit Serial Media Independent Interface) , QSGMII (Quad Serial Gigabit Media Independent Interface) and O-USGMII (Octagon Universal Serial Gigabit Media Independent Interface) in 10/100/1000M mode
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports crossover detection and auto correction in 10Base-T/100Base-T
- Auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports Realtek's Cable Test (RTCT)
- Supports one interrupt output to external CPU for notification
- Low power consumption
- Easy layout, good EMI, and good thermal performance
- 25MHz crystal or 3.3V OSC input
- 3.3V and 0.9V power supply
- LQFP-128 E-PAD package

3. System Applications

3.1. 24-Ports Gigabit Ethernet Switch

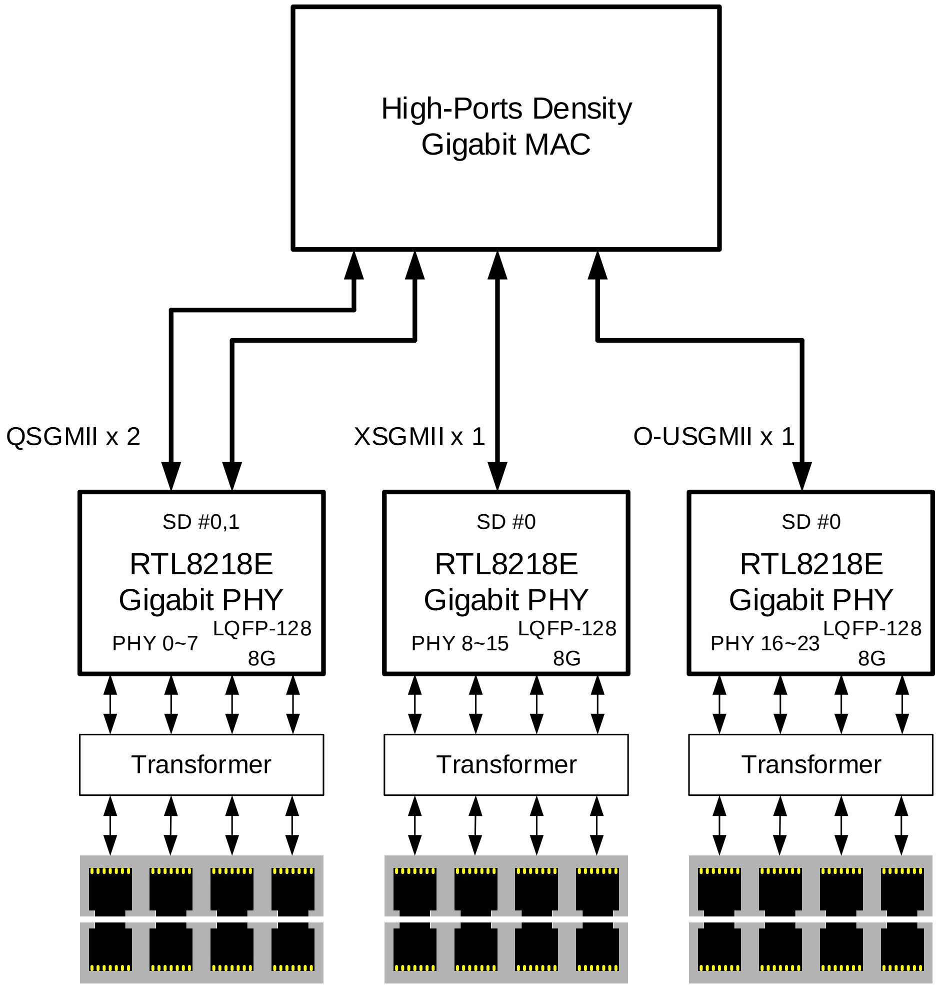


Figure 1. 24-Port Gigabit Ethernet Switch (QSGMII & XSGMII & O-USGMII Interface)

4. Block Diagram

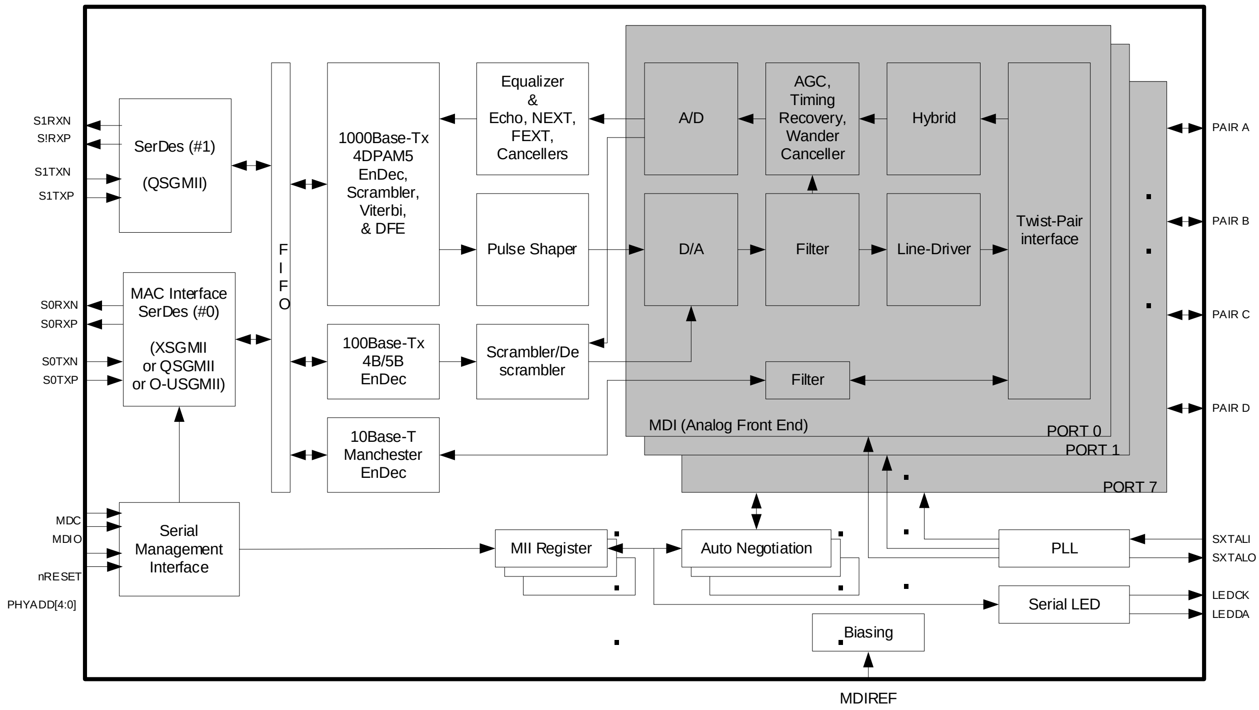


Figure 2. Block Diagram

5. Pin Assignments

5.1. Pin Assignments

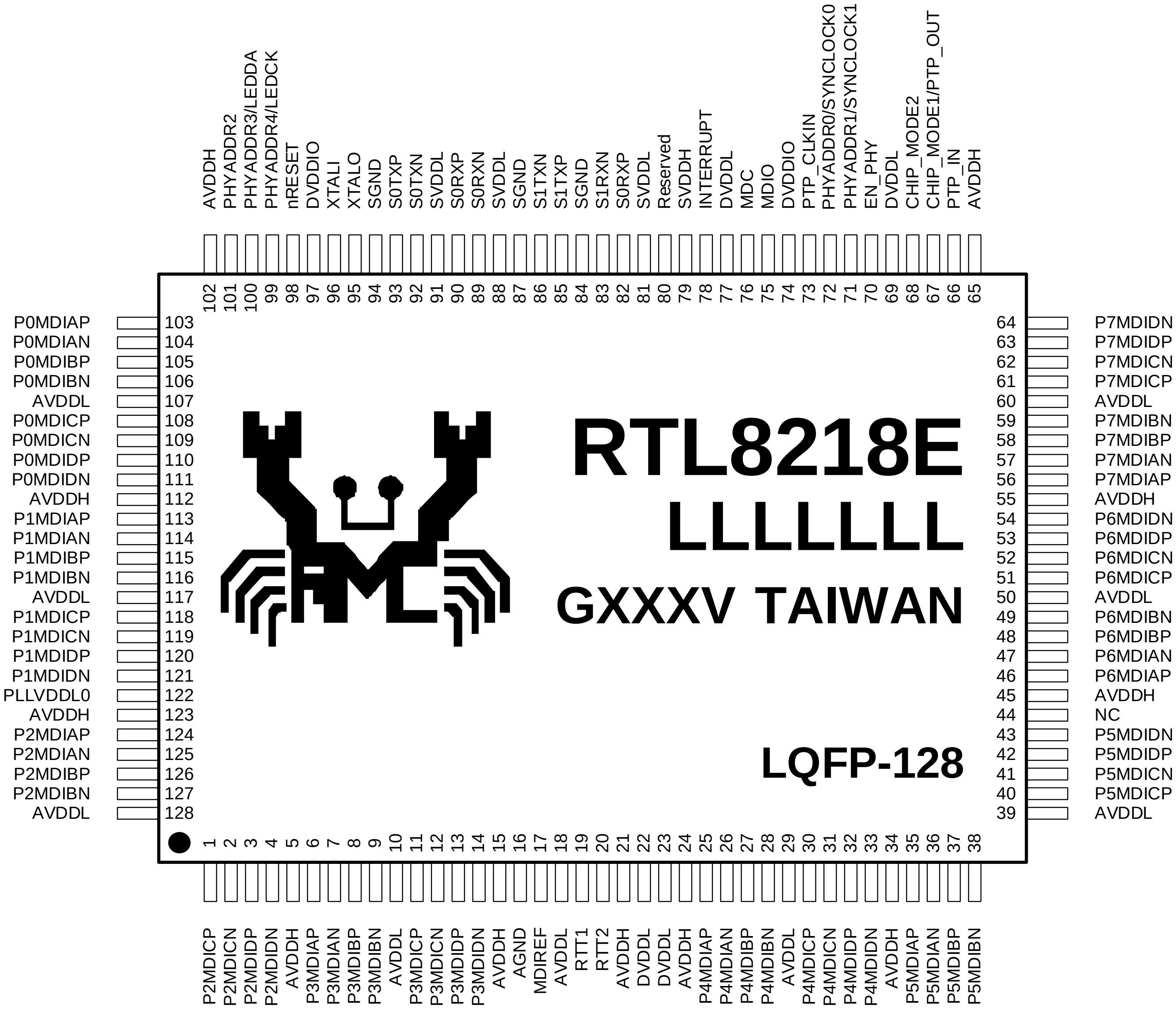


Figure 3. Pin Assignments

5.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 3). The version number is shown in the location marked 'V'.

5.3. Pin Assignment Tables

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PD}: Input Pin With Pull-Down Resistor

I_{PU}: Input Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

SP: SerDes Power Pin

I_S: Schmitt Trigger Input Pin

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

A: Analog Pin

O_{PU}: Output Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

SG: SerDes Ground Pin

Table 1. Pin Assignments Table

Pin Name	Pin No.	Type	Pin Name	Pin No.	Type
P2MDICP	1	AI/O	DVDDL	22	P
P2MDICN	2	AI/O	DVDDL	23	P
P2MDIDP	3	AI/O	AVDDH	24	AP
P2MDIDN	4	AI/O	P4MDIAP	25	AI/O
AVDDH	5	AP	P4MDIAN	26	AI/O
P3MDIAP	6	AI/O	P4MDIBP	27	AI/O
P3MDIAN	7	AI/O	P4MDIBN	28	AI/O
P3MDIBP	8	AI/O	AVDDL	29	AP
P3MDIBN	9	AI/O	P4MDICP	30	AI/O
AVDDL	10	AP	P4MDICN	31	AI/O
P3MDICP	11	AI/O	P4MDIDP	32	AI/O
P3MDICN	12	AI/O	P4MDIDN	33	AI/O
P3MDIDP	13	AI/O	AVDDH	34	AP
P3MDIDN	14	AI/O	P5MDIAP	35	AI/O
AVDDH	15	AP	P5MDIAN	36	AI/O
AGND	16	AG	P5MDIBP	37	AI/O
MDIREF	17	AO	P5MDIBN	38	AI/O
AVDDL	18	AP	AVDDL	39	AP
RTT1	19	AO	P5MDICP	40	AI/O
RTT2	20	AO	P5MDICN	41	AI/O
AVDDH	21	AP	P5MDIDP	42	AI/O

Pin Name	Pin No.	Type
P5MDIDN	43	AI/O
NC	44	-
AVDDH	45	AP
P6MDIAP	46	AI/O
P6MDIAN	47	AI/O
P6MDIBP	48	AI/O
P6MDIBN	49	AI/O
AVDDL	50	AP
P6MDICP	51	AI/O
P6MDICN	52	AI/O
P6MDIDP	53	AI/O
P6MDIDN	54	AI/O
AVDDH	55	AP
P7MDIAP	56	AI/O
P7MDIAN	57	AI/O
P7MDIBP	58	AI/O
P7MDIBN	59	AI/O
AVDDL	60	AP
P7MDICP	61	AI/O
P7MDICN	62	AI/O
P7MDIDP	63	AI/O
P7MDIDN	64	AI/O
AVDDH	65	AP
PTP_IN	66	I/O_{PU}
CHIP_MODE1/PTP_OUT	67	I_{PU}
CHIP_MODE2	68	I_{PU}
DVDDL	69	P
EN_PHY	70	I/O_{PU}
PHYADDR1/SYNCLOCK1	71	I/O_{PD}
PHYADDR0/SYNCLOCK0	72	I/O_{PD}
PTP_CLKIN	73	I/O_{PD}
DVDDIO	74	P
MDIO	75	I/O_{PU}
MDC	76	I
DVDDL	77	P
INTERRUPT	78	I/O_{PU}
SVDDH	79	SP
NC	80	-
SVDDL	81	SP
S1RXP	82	AO
S1RXN	83	AO
SGND	84	SG
S1TXP	85	AI
S1TXN	86	AI

Pin Name	Pin No.	Type
SGND	87	SG
SVDDL	88	SP
S0RXN	89	AO
S0RXP	90	AO
SVDDL	91	SP
S0TXN	92	AI
S0TXP	93	AI
SGND	94	SG
XTALO	95	AO
XTALI	96	AI
DVDDIO	97	P
nRESET	98	I_{PU}
PHYADDR4/LEDCK	99	I/O_{PD}
PHYADDR3/LEDDA	100	I/O_{PD}
PHYADDR2	101	I_{PD}
AVDDH	102	AP
P0MDIAP	103	AI/O
P0MDIAN	104	AI/O
P0MDIBP	105	AI/O
P0MDIBN	106	AI/O
AVDDL	107	AP
P0MDICP	108	AI/O
P0MDICN	109	AI/O
P0MDIDP	110	AI/O
P0MDIDN	111	AI/O
AVDDH	112	AP
P1MDIAP	113	AI/O
P1MDIAN	114	AI/O
P1MDIBP	115	AI/O
P1MDIBN	116	AI/O
AVDDL	117	AP
P1MDICP	118	AI/O
P1MDICN	119	AI/O
P1MDIDP	120	AI/O
P1MDIDN	121	AI/O
PLLVDDL0	122	AP
AVDDH	123	AP
P2MDIAP	124	AI/O
P2MDIAN	125	AI/O
P2MDIBP	126	AI/O
P2MDIBN	127	AI/O
AVDDL	128	AP
GND	EPAD	G

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Description
P0MDIAP P0MDIAN P0MDIBP P0MDIBN P0MDICP P0MDICN P0MDIDP P0MDIDN	103 104 105 106 108 109 110 111	AI/O	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P1MDIAP P1MDIAN P1MDIBP P1MDIBN P1MDICP P1MDICN P1MDIDP P1MDIDN	113 114 115 116 118 119 120 121	AI/O	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P2MDIAP P2MDIAN P2MDIBP P2MDIBN P2MDICP P2MDICN P2MDIDP P2MDIDN	124 125 126 127 1 2 3 4	AI/O	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P3MDIAP P3MDIAN P3MDIBP P3MDIBN P3MDICP P3MDICN P3MDIDP P3MDIDN	6 7 8 9 11 12 13 14	AI/O	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P4MDIAP P4MDIAN P4MDIBP P4MDIBN P4MDICP P4MDICN P4MDIDP P4MDIDN	25 26 27 28 30 31 32 33	AI/O	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.

Pin Name	Pin No.	Type	Description
P5MDIAP P5MDIAN P5MDIBP P5MDIBN P5MDICP P5MDICN P5MDIDP P5MDIDN	35 36 37 38 40 41 42 43	AI/O	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P6MDIAP P6MDIAN P6MDIBP P6MDIBN P6MDICP P6MDICN P6MDIDP P6MDIDN	46 47 48 49 51 52 53 54	AI/O	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P7MDIAP P7MDIAN P7MDIBP P7MDIBN P7MDICP P7MDICN P7MDIDP P7MDIDN	56 57 58 59 61 62 63 64	AI/O	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.

6.2. XSGMII Pins

Table 3. XSGMII Pins

Pin Name	Pin No.	Type	Description
S0RXP S0RXN	90 89	AO	If CHIP_MODE[2:1] = 2’b01 XSGMII Differential Output. 10.3125GHz serial interfaces to transfer data from an External device that supports the XSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXP S0TXN	93 92	AI	If CHIP_MODE[2:1] = 2’b01 XSGMII Differential Input. 10.3125GHz serial interfaces to receive data from an External device that supports the XSGMII interface. Differential pairs have an internal 100ohm termination resistor.
Reserved	82 83	AO	Reserved. Can be left floating
Reserved	85 86	AI	Reserved. Require either a 1K ohm resister to GND.

6.3. O-USGMII Pins

Table 4. O-USGMII Pins

Pin Name	Pin No.	Type	Description
S0RXP S0RXN	90 89	AO	If CHIP_MODE[2:1] = 2’b00 O-USGMII Differential Output. 10GHz serial interfaces to transfer data from an External device that supports the O-USGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXP S0TXN	93 92	AI	If CHIP_MODE[2:1] = 2’b00 O-USGMII Differential Input. 10GHz serial interfaces to receive data from an External device that supports the O-USGMII interface. Differential pairs have an internal 100ohm termination resistor.
Reserved	82 83	AO	Reserved. Can be left floating
Reserved	85 86	AI	Reserved. Require either a 1K ohm resister to GND.

6.4. QSGMII Pins

Table 5. QSGMII Pins

Pin Name	Pin No.	Type	Description
S0RXP S0RXN S1RXP S1RXN	90 89 82 83	AO	If CHIP_MODE[2:1] = 2’b10 QSGMII Differential Output. 5GHz serial interfaces to transfer data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXP S0TXN S1TXP S1TXN	93 92 85 86	AI	If CHIP_MODE[2:1] = 2’b10 QSGMII Differential Input. 5GHz serial interfaces to receive data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.

6.5. Serial LED Pins

Table 6. Serial LED Pins

Pin Name	Pin No.	Type	Description
LEDCK	99	I/O_{PD}	Serial LED Clock Output
LEDDA	100	I/O_{PD}	Serial LED Data Output

6.6. Configuration Pins

Table 7. Configuration Pins

Pin Name	Pin No.	Type	Description
PHYADDR0 / SYNCLOCK0	72	I/O_{PD}	PHYADDR0, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR1 / SYNCLOCK1	71	I/O_{PD}	PHYADDR1, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR2	101	I_{PD}	PHYADDR2, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR3 / LEDDA	100	I/O_{PD}	PHYADDR3, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR4 / LEDCK	99	I/O_{PD}	PHYADDR4, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
EN_PHY	70	I/O_{PU}	Enable PHY Power 1: Power up all ports 0: Power down all ports and set the MII register 0.11 power down as 1 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
CHIP_MODE2	68	I_{PU}	MAC Interface Configuration: CHIP_MODE[2:1] = 01: XSGMII 10: QSGMII 11: Reserved for Internal use 00: O-USGMII
CHIP_MODE1 / PTP_OUT	67	I_{PU}	Reference CHIP_MODE2

6.7. Miscellaneous Pins

Table 8. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
MDC	76	I	MII Management Interface Clock Input. The clock reference for the MII management interface. The maximum frequency support is 12.5MHz.
MDIO	75	I/O_{PU}	MII Management Interface Data Input/Output. MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.
INTERRUPT	78	I/O_{PU}	Interrupt output when Interrupt even occurs. Active High by pull-down to GND via a 1K resistor. Active Low by pull-up to DVDDIO via a 4.7K resistor.
nRESET	98	I_{PU}	Hardware Reset (Active Low Reset Signal). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
MDIREF	17	AO	MDI Bias Resistor. Adjusts the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.
NC	44	-	We suggest NC pins are left floating.
Reserved	80	I/O_{PU}	This pin must connect to DVDDIO via a 4.7k ohm resistor or left floating.
XTALI	96	AI	25MHz Crystal Clock Input. 25MHz±50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
XTALO	95	AO	25MHz Crystal Clock Output. 25MHz±50ppm tolerance crystal output. Refer to XTALI.

6.8. Power and GND Pins

Table 9. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	5, 15, 21, 24, 34, 45, 55, 65, 102, 112,123	AP	Analog High Voltage Power
AVDDL	10, 18, 29, 39, 50, 60, 107, 117, 128	AP	Analog Low Voltage Power
PLLVDD0	122	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2µF shunt capacitors to ground
SVDDH	79	SP	QSGMII / RSGMII-Plus SerDes High Voltage Power
SVDDL	81, 88, 91	SP	QSGMII / RSGMII-Plus SerDes Low Voltage Power
DVDDIO	74, 97	P	Digital I/O Power
DVDDL	22, 23, 69, 77	P	Digital Low Voltage Power
AGND	16	AG	Analog Ground
SGND	84, 87, 94	SG	QSGMII/RSGMII-Plus SerDes Ground
GND	EPAD	G	Digital/Analog Ground

6.9. Test Pins

Table 10. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	19	AO	Sync E Reference Clock Output. Must be Left Floating or pulled-up to to DVDDIO via 4.7K resistor.
RTT2	20	AO	Sync E Reference Clock Output. Must be Left Floating or pulled-up to to DVDDIO via 4.7K resistor.
PHYADDR0 / SYNCLOCK0	72	I/O_{PD}	SYNCLOCK signal to inform the external DPLL or MAC can begin to output the reference Sync E clock. *Note. This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR1 / SYNCLOCK1	71	I/O_{PD}	SYNCLOCK signal to inform the external DPLL or MAC can begin to output the reference Sync E clock. *Note. This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PTP_IN	66	I/O_{PU}	PTP module input used to start/stop/latch global timer. Must be Left Floating or pulled-up to to DVDDIO via 4.7K resistor.
CHIP_MODE / PTP_OUT	67	I_{PU}	PTP module trigger pulse or periodic clock generate output.
PTP_CLKIN	73	I/O_{PD}	External PTP clock input. Must be tied to GND via a 1K resistor for normal operation

7. Function Description

7.1. MDI Interface

The RTL8218E embeds octal 10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100M links and during auto-negotiation, only pairs A and B are used.

7.2. 1000Base-T Transmit Function

The 1000Base-T pcs layer receives data bytes from GMII interface and performs the generation of continuous code groups through 4D-PAM5 encoding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8218E obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8218E advertises full capabilities (1000full, 100full, 100half, 10full, 10half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8218E automatically determines whether or not it needs to crossover between pairs, so that an external crossover cable is not required. When connecting to a device that does not perform MDI crossover, the RTL8218E automatically switches its pin pairs to communicate with the remote device. When connecting to a device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The RTL8218E is set to MDI Crossover by default. The pin mapping in MDI and MDI Crossover mode is given below.

Table 11. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8218E automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when 10Base-T links up. The polarity becomes unlocked when the link is down.

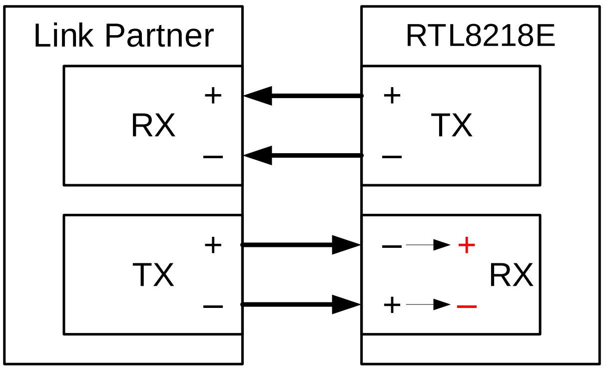


Figure 4. Conceptual Example of Polarity Correction

7.11. MDC/MDIO Interface

The RTL8218E supports the IEEE compliant Management Data Input/Output (MDIO) Interface. This is the only method for the MAC to acquire the status of the PHY. The Media Independent Interface Management (MIIM) registers are written and read serially, using the MDC/MDIO pins. Data transferred to and from the MDIO pins is synchronized with the MDC clock. All transfers are initiated by the MAC. A clock of up to 12MHz must drive the MDC pin of the RTL8218E.

The MII register is a block of 32 registers, each 16 bits wide. Certain registers are defined by IEEE 802.3 and are required for compliance (0~10, 15).

The MDIO frame structure starts with a 32-bit preamble, which is required by the RTL8218E. The following data includes a start-of-frame marker, an op-code, a 10-bit address field, and a 16-bit data field. The address field is divided into two 5-bit segments. The first segment identifies the PHY address and the second identifies the register being accessed.

The 5-bits of the PHY address are determined by the hardware strapping values during power up. The MDIO protocol provides both read and write operations. During a write operation, the MAC drives the MDIO line for the entire frame. For a read operation, a turn-around time is inserted in the frame to allow the PHY to drive back to the MAC. The MDIO pin of the MAC must be put in high-impedance during these bit times. Figure 5 and Figure 6 depict the MDIO read and write frame format respectively.

The RTL8218E is permanently programmed for preamble suppression. A preamble of 32 ‘1’ bits is required only for the first read or write. The management preamble may be as short as 1 bit.

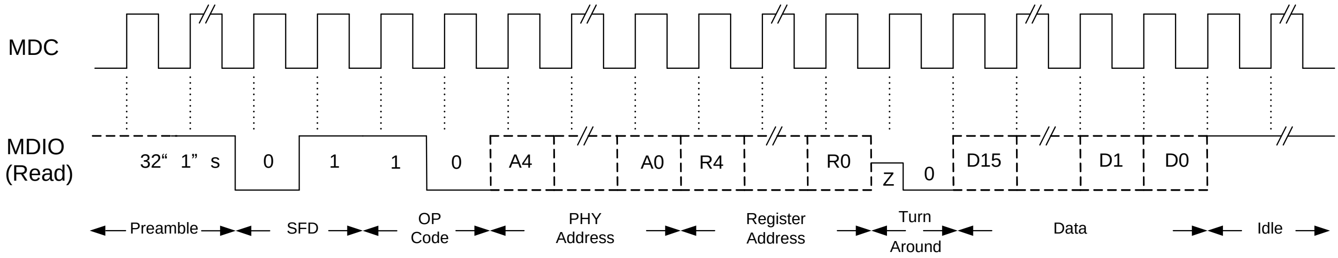


Figure 5. MDIO Read Frame Format

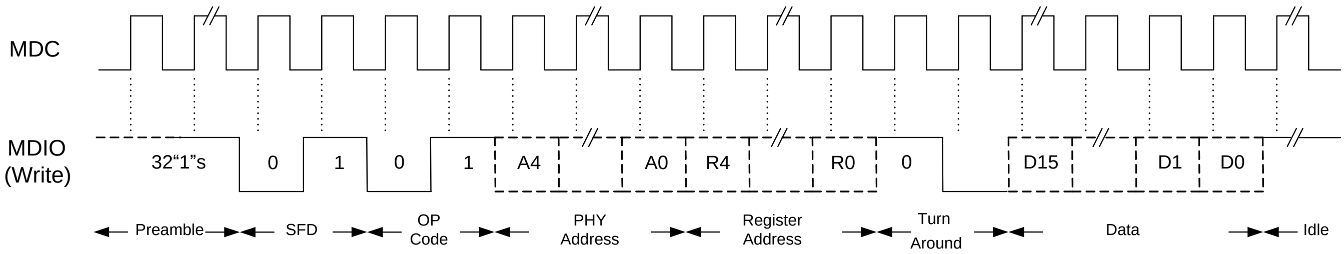


Figure 6. MDIO Write Frame Format

7.12. Ten-Gigabit Media Independent Interface (XSGMII)

The XSGMII (Ten-Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 10.3125 Gbps serial interface provides MAC to PHY communication path. XSGMII can carry the full duplex gigabit Ethernet data streams of 8 ports simultaneously, using only 4 pins.

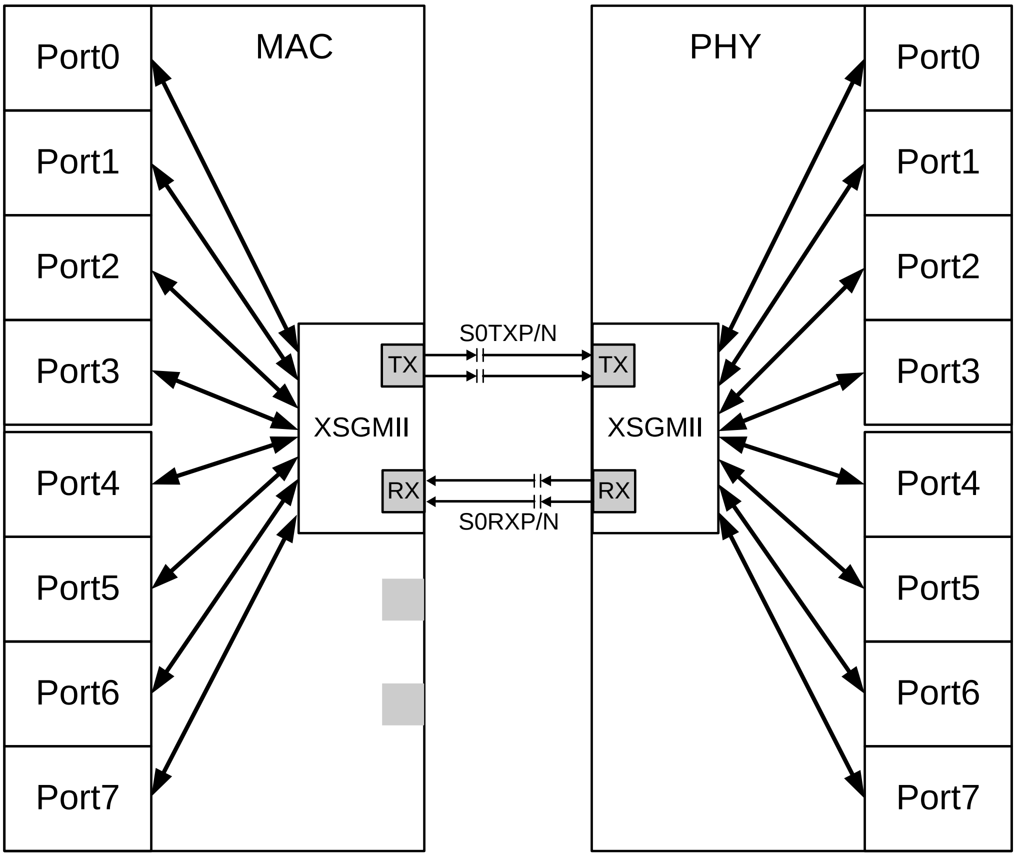


Figure 7. XSGMII Interconnection Diagram

7.13. Quad Serial Gigabit Media Independent Interface

(QSGMII)

The QSGMII (Quad Serial Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 5Gbps serial interface provides a MAC to PHY communication path. QSGMII can carry the full duplex gigabit Ethernet data streams of four ports simultaneously, using only 4 pins.

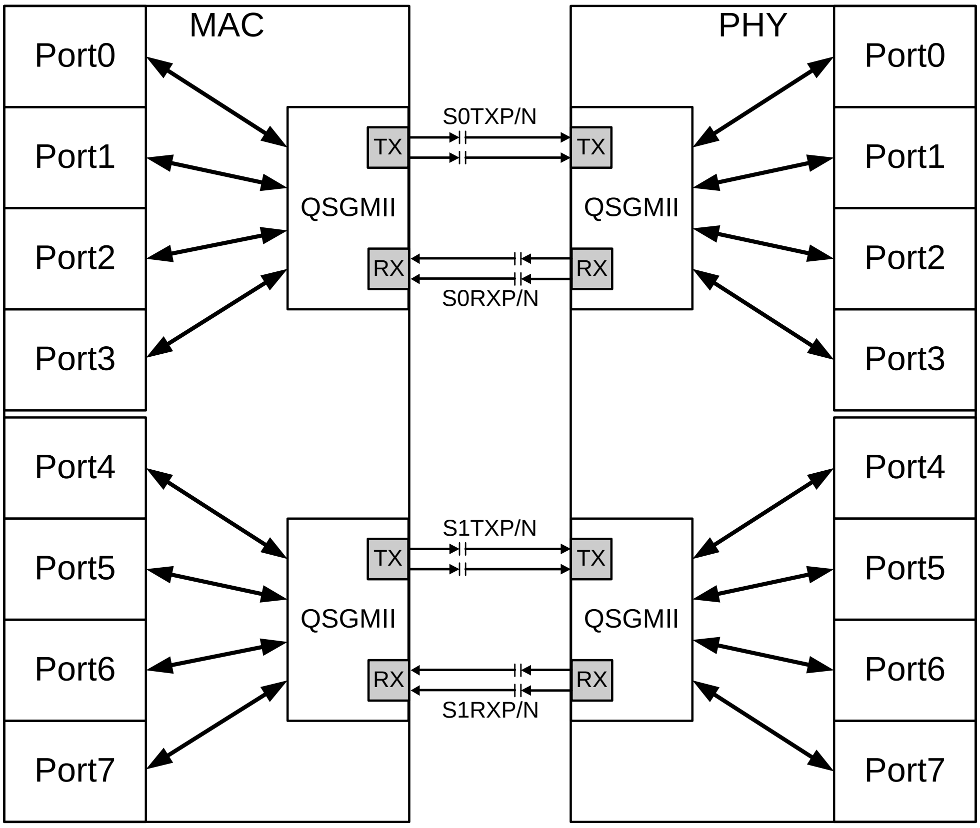


Figure 8. QSGMII Interconnection Diagram

7.14. Octagon Universal Serial Gigabit Media Independent Interface (O-USGMII)

The O-USGMII (Octagon Universal Serial Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 10 Gbps serial interface provides MAC to PHY communication path. O-USGMII can carry the full duplex gigabit Ethernet data streams of 8 ports simultaneously, using only 4 pins.

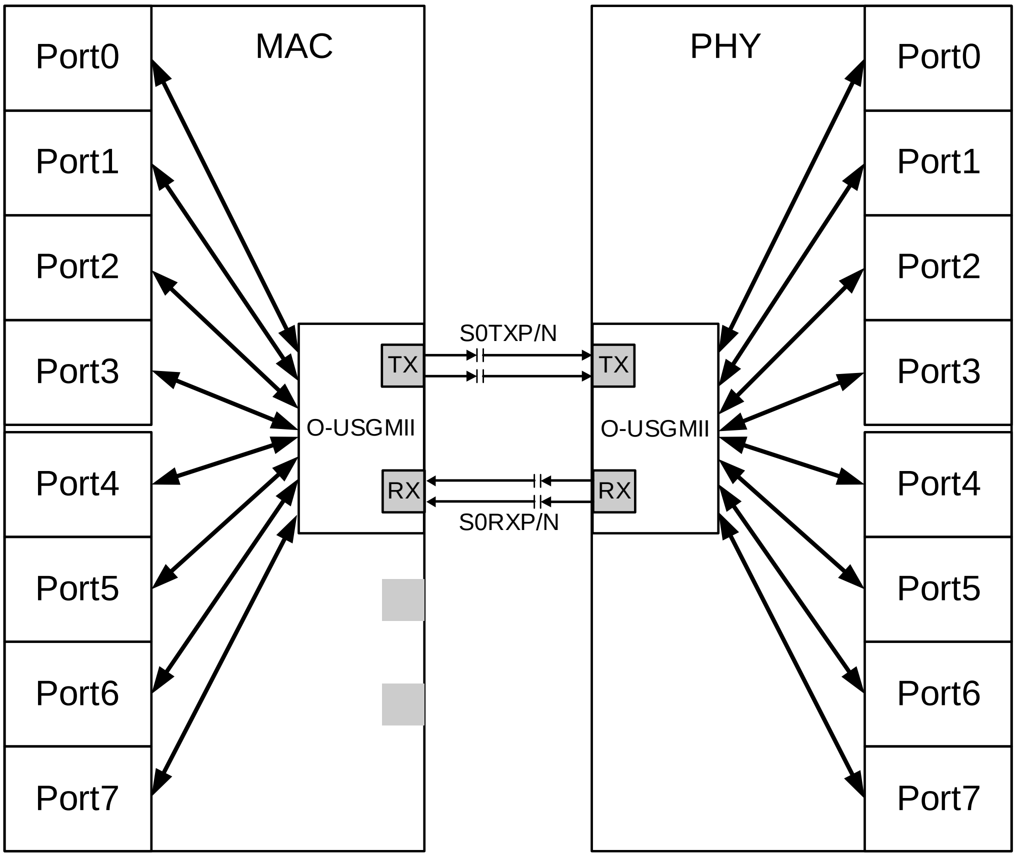


Figure 9. O-USGMII Interconnection Diagram

7.14.1. XSGMII Interface

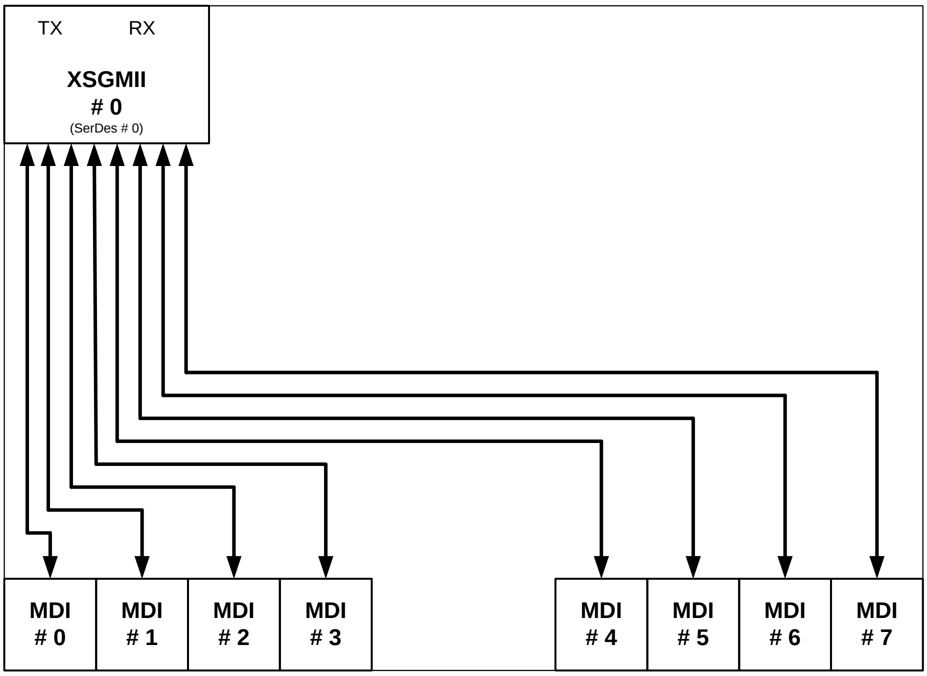


Figure 10. [MDI x 8] + [XSGMII x 1]

7.14.2. QSGMII Interface

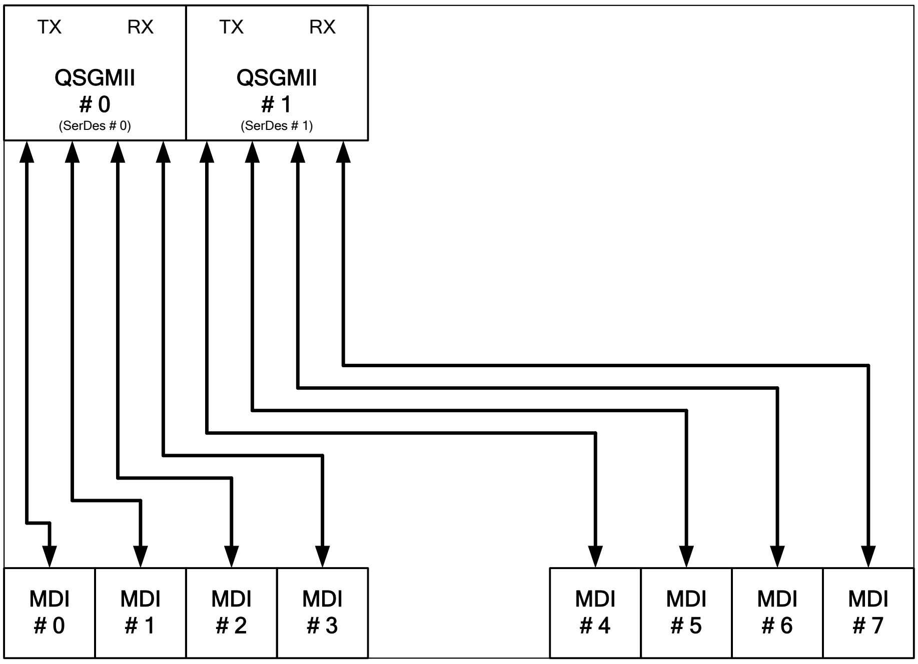


Figure 11. [MDI x 8] + [QSGMII x 2]

7.14.3. O-USGMII Interface

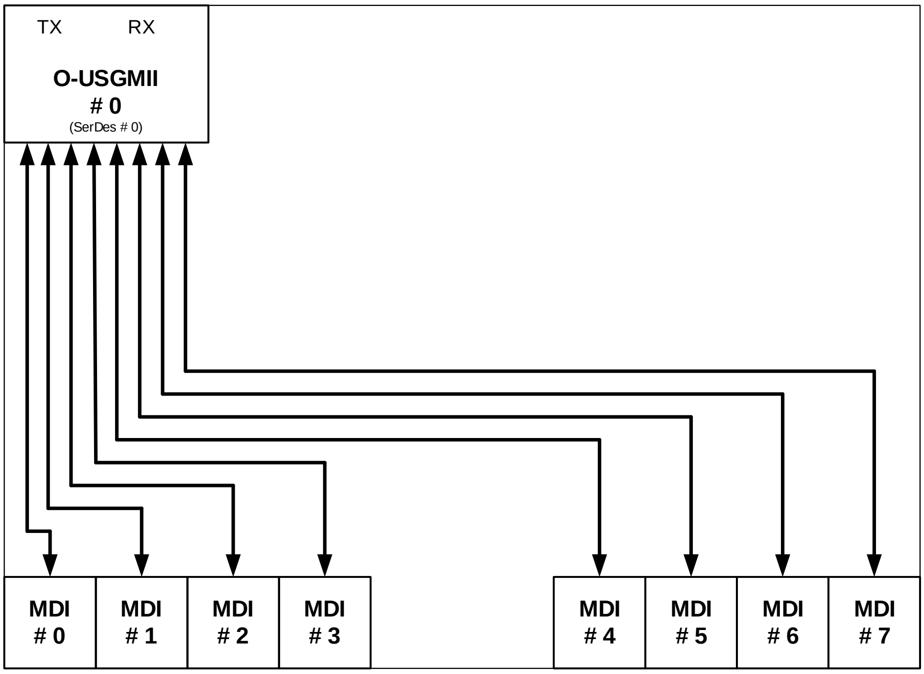


Figure 12. [MDI x 8] + [O-USGMII x 1]

7.15. Serial LED

7.15.1. Port Status Indicator

The RTL8218E supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins. Each MDI port has three indicator symbols and each fiber port has three indicator symbols. Each symbol may have different indicator information

7.15.2. LED Configuration

Table 12. Serial LED Per-LED Control

PHY0, Reg.30 = 8, Reg.=31=0x281

Reg.bit	Name	Mode	Description	Default
18.[15:12]	LED_00_Mode	RW	Assign LEDn to Port. 0000: MDI0 0001: MDI1 0010: MDI2 0011: MDI3 0100: MDI4 0101: MDI5 0110: MDI6 0111: MDI7 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100~1110: Reserved 1111: Disable	0x0
18.11		RW	1000M Speed Indicator.	0x0
18.10		RW	100M Speed Indicator.	0x0
18.9		RW	10M Speed Indicator.	0x0
18.8		RW	Reserved	0x0
18.7		RW	1000M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.6		RW	100M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.5		RW	10M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.4		RW	Reserved	0x0
18.3		RW	Duplex Indicator.	0x0
18.2		RW	Collision Indicator. Blinking when a collision occurs.	0x0
18.1		RW	Tx Activity Indicator. Blinking when the corresponding port is transmitting.	0x0
18.0		RW	Rx Activity Indicator. Blinking when the corresponding port is receiving.	0x0
19[15:0]	LED_01_Mode	RW	Same as LED_00_Mode	-
20[15:0]	LED_02_Mode	RW	Same as LED_00_Mode	-
21[15:0]	LED_03_Mode	RW	Same as LED_00_Mode	-

Reg.bit	Name	Mode	Description	Default
22[15:0]	LED_04_Mode	RW	Same as LED_00_Mode	-
23[15:0]	LED_05_Mode	RW	Same as LED_00_Mode	-

PHY0, Reg.29 = 8, Reg.=31=0x282

Reg.bit	Name	Mode	Description	Default
16[15:0]	LED_06_Mode	RW	Same as LED_00_Mode	-
17[15:0]	LED_07_Mode	RW	Same as LED_00_Mode	-
18[15:0]	LED_08_Mode	RW	Same as LED_00_Mode	-
19[15:0]	LED_09_Mode	RW	Same as LED_00_Mode	-
20[15:0]	LED_10_Mode	RW	Same as LED_00_Mode	-
21[15:0]	LED_11_Mode	RW	Same as LED_00_Mode	-
22[15:0]	LED_12_Mode	RW	Same as LED_00_Mode	-
23[15:0]	LED_13_Mode	RW	Same as LED_00_Mode	-

PHY0, Reg.29 = 8, Reg.=31=0x283

Reg.bit	Name	Mode	Description	Default
16[15:0]	LED_14_Mode	RW	Same as LED_00_Mode	-
17[15:0]	LED_15_Mode	RW	Same as LED_00_Mode	-
18[15:0]	LED_16_Mode	RW	Same as LED_00_Mode	-
19[15:0]	LED_17_Mode	RW	Same as LED_00_Mode	-
20[15:0]	LED_18_Mode	RW	Same as LED_00_Mode	-
21[15:0]	LED_19_Mode	RW	Same as LED_00_Mode	-
22[15:0]	LED_20_Mode	RW	Same as LED_00_Mode	-
23[15:0]	LED_21_Mode	RW	Same as LED_00_Mode	-

PHY0, Reg.29 = 8, Reg.=31=0x284

Reg.bit	Name	Mode	Description	Default
16[15:0]	LED_22_Mode	RW	Same as LED_00_Mode	-
17[15:0]	LED_23_Mode	RW	Same as LED_00_Mode	-
18[15:0]	LED_24_Mode	RW	Same as LED_00_Mode	-
19[15:0]	LED_25_Mode	RW	Same as LED_00_Mode	-
20[15:0]	LED_26_Mode	RW	Same as LED_00_Mode	-
21[15:0]	LED_27_Mode	RW	Same as LED_00_Mode	-
22[15:0]	LED_28_Mode	RW	Same as LED_00_Mode	-
23[15:0]	LED_29_Mode	RW	Same as LED_00_Mode	-

PHY0, Reg.29 = 8, Reg.=31=0x285

Reg.bit	Name	Mode	Description	Default
16[15:0]	LED_30_Mode	RW	Same as LED_00_Mode	-
17[15:0]	LED_31_Mode	RW	Same as LED_00_Mode	-

Reg.bit	Name	Mode	Description	Default
18[15:0]	LED_32_Mode	RW	Same as LED_00_Mode	-
19[15:0]	LED_33_Mode	RW	Same as LED_00_Mode	-
20[15:0]	LED_34_Mode	RW	Same as LED_00_Mode	-
21[15:0]	LED_35_Mode	RW	Same as LED_00_Mode	-

Table 13. Serial LED Mode Configuration (Per-Port 3 LEDs)

of Per-LED Register	LED_MODE [1:0]=11	LED_MODE [1:0]=10	LED_MODE [1:0]=01	LED_MODE [1:0]=00
LED35	0x0FF0	0x0880	0x0880	0x0FF0
LED34	0x1FF0	0x1880	0x1880	0x1FF0
LED33	0x2FF0	0x2880	0x2880	0x2FF0
LED32	0x3FF0	0x3880	0x3880	0x3FF0
LED31	0x4FF0	0x4880	0x4880	0x4FF0
LED30	0x5FF0	0x5880	0x5880	0x5FF0
LED29	0x6FF0	0x6880	0x6880	0x6FF0
LED28	0x7FF0	0x7880	0x7880	0x7FF0
LED27	0x0800	0x0440	0x0660	0xF000
LED26	0x1800	0x1440	0x1660	0xF000
LED25	0x2800	0x2440	0x2660	0xF000
LED24	0x3800	0x3440	0x3660	0xF000
LED23	0x4800	0x4440	0x4660	0xF000
LED22	0x5800	0x5440	0x5660	0xF000
LED21	0x6800	0x6440	0x6660	0xF000
LED20	0x7800	0x7440	0x7660	0xF000
LED19	0x0400	0x0220	0xF000	0xF000
LED18	0x1400	0x1220	0xF000	0xF000
LED17	0x2400	0x2220	0xF000	0xF000
LED16	0x3400	0x3220	0xF000	0xF000
LED15	0x4400	0x4220	0xF000	0xF000
LED14	0x5400	0x5220	0xF000	0xF000
LED13	0x6400	0x6220	0xF000	0xF000
LED12	0x7400	0x7220	0xF000	0xF000
LED11	0xF000	0xF000	0xF000	0xF000
LED10	0xF000	0xF000	0xF000	0xF000
LED09	0xF000	0xF000	0xF000	0xF000
LED08	0xF000	0xF000	0xF000	0xF000
LED07	0xF000	0xF000	0xF000	0xF000
LED06	0xF000	0xF000	0xF000	0xF000
LED05	0xF000	0xF000	0xF000	0xF000
LED04	0xF000	0xF000	0xF000	0xF000
LED03	0xF000	0xF000	0xF000	0xF000
LED02	0xF000	0xF000	0xF000	0xF000
LED01	0xF000	0xF000	0xF000	0xF000
LED00	0xF000	0xF000	0xF000	0xF000

of Per-LED Register	LED_MODE [1:0]=11	LED_MODE [1:0]=10	LED_MODE [1:0]=01	LED_MODE [1:0]=00

Notes:
LED_MODE [1:0]=11
MDI: [Link/Act] [SPD1000] [SPD100]
FX: [Link/Act] [SPD1000] [SPD100]

LED_MODE [1:0]=10
MDI: [SPD1000/Act] [SPD100/Act] [SPD10/Act]
FX: [SPD1000/Act] [SPD100/Act] [Disable]

LED_MODE [1:0]=01
MDI: [SPD1000/Act] [SPD100(10)/Act]
FX: [SPD1000/Act] [SPD100/Act]

LED_MODE [1:0]=00
MDI: [Link/Act]
FX: [Link/Act]

7.15.3. Serial LED Configuration Register

Table 14. Serial LED Configuration Register

PHY0, Reg.29 = 8, Reg.=31=0x280

Reg.bit	Name	Mode	Description	Default
16[15:14]	Reserved	RW	Reserved	00
16[13:12]	cfg_led_mode	RW	00: LED_Mode0. Per-Port 2 LEDs 01: LED_Mode1. Per-Port 2 LEDs 10: LED_Mode2. Per-Port 3 LEDs 11: LED_Mode3. Per-Port 3 LEDs	11
16[11]	Reserved	RW	Reserved	0
16[10:8]	Serial Blink Rate	RW	LED Blink Rate Configuration. 000: 32ms 001: 64ms 010: 128ms 011: 256ms 100: 512ms 101: 1024ms 110: 48ms 111: 96ms	000
16[7:6]	serial led burst cycle	RW	2'b00: 8 (ms) 2'b01: 16 2'b10: 32 2'b11: 64	10
16[5:4]	serial led clock cycle	RW	2'b00: 32 (ns) 2'b01: 64 2'b10: 96 2'b11: 192	11

Reg.bit	Name	Mode	Description	Default
16[3]	led_seri_active_low	RW	Serial LED active LOW 0: LED status active high 1: LED status active low	1
16[2]	led_seri_disable	RW	Disable Serial LED. 1: Disable 0: Enable Default by strapping option (pin-30)	
16[1]	led_data_e_b	RW	Serial LED DATA_EN	
16[0]	led_clk_e_b	RW	Serial LED CLK_EN	

Note: Upon reset, the RTL8218E supports chip diagnostics and LED functions by blinking all LEDs once via the LED_PowerOn_Light strapping pin configuration.

7.15.4. Serial LED Timing Definitions

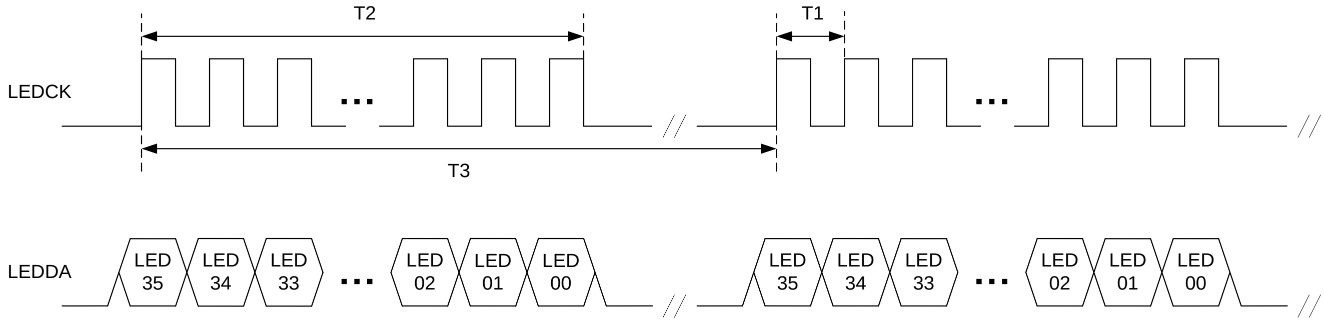


Figure 13. Serial LED Timing Definitions

7.16. Realtek Cable Test (RTCT)

The RTL8218E physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function could be used to detect short, open, crossed, or impedance mismatch in each differential pair. The RTL8218E supports inter-pair short detection.

7.17. IEEE 802.3az Energy Efficient Ethernet (EEE)

The RTL8218E supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL8218E also supports PHY-mode EEE.

7.18. Interrupt Pin for External CPU

The RTL8218E provides one Interrupt output pin to interrupt an external CPU for 10/100/1000Base-T ports. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8218E will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

7.19. Reg.0.11 Power Down Mode

The RTL8218E implements power down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8218E to enter power down mode.

7.20. Reg.0.14 PHY Digital Loopback Return to Internal

The digital loopback mode of the PHY (return to MAC) may be enabled on a per-port basis by setting MII Reg.0.14 to 1. In digital loopback mode, the TXD of the PHY is transferred directly to the RXD of the PHY, with TXEN changed to CRS_DV, and returns to the MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium, and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps, 100Mbps, and 1000Mbps in full duplex mode. This function is useful for diagnostic purposes.

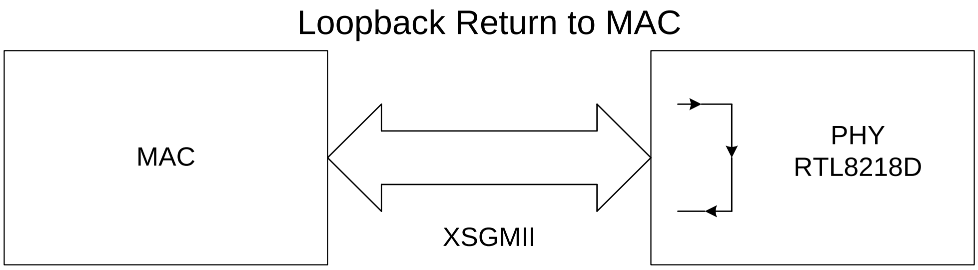


Figure 14. Reg.0.14 PHY Digital Loopback

As the RTL8218E only supports digital loopback in full duplex mode, PHY Reg.0.8 for each port will be always kept to 1 when digital loopback is enabled. In loopback mode, the link LED of the loopback port should be always turned on, and the speed combined with the duplex LED will reflect the link status (1000full/100full/10full) correctly regardless of what the previous status of this loopback port was.

8. Register Descriptions

Registers 0~15 of the MII are defined by the MII specification. Other registers are defined by Realtek Semiconductor Corp. for internal use and are reserved.

The following abbreviations are used in this section:

RW: Read/Write RO: Read Only SC: Self Clearing

LL: Latch Low until clear LH: Latch High until clear

Table 15. Register Descriptions

Page	Register	Description	Default
0	0	Control	0x1140
	1	Status	0x7989
	2	PHY Identifier 1	0x001C
	3	PHY Identifier 2	0xC984
	4	Auto-Negotiation Advertisement	0x05E1
	5	Auto-Negotiation Link Partner Ability	0x0000
	6	Auto-Negotiation Expansion	0x0064
	7	Auto-Negotiation Next Page Transmit	0x2001
	8	Auto-Negotiation Link Partner Next Page Ability	0x0000
	9	1000Base-T Control	0x0E00
	10	1000Base-T Status	0x0000
	11~14	Reserved	0x0000
	13	1000Base-T MMD Access Control	0x0000
	14	1000Base-T MMD Access Address Data	0x0000
	15	Extended Status	0x2000
	16~30	ASIC Control	-

8.1. Register 0: Control

Table 16. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing.	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback (this will loopback TXD to RXD and ignore all activity on the cable media) 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6, 0.13] Speed Selection [1:0]. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps This bit can be set through SMI (Read/Write).	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	1
0.11	Power Down	RW	1: Power down (all functions will be disabled except SMI function) 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from QGMII (PHY still responds to MDC/MDIO) 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation This bit can be set through SMI (Read/Write).	1
0.7	Collision Test	RO	1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	0
0.6	Speed Selection[1]	RW	See Bit 13.	1
0.[5:0]	Reserved	RO	Reserved.	000000

8.2. Register 1: Status

Table 17. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0: No 100Base-T4 capability The RTL8218E does not support 100Base-T4 mode, and this bit should always be 0.	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1
1.10	100Base-T2-FD	RO	0: No 100Base-T2 full duplex capability The RTL8218E does not support 100Base-T2 mode, and this bit should always be 0.	0
1.9	100Base-T2-HD	RO	0: No 100Base-T2 half duplex capability The RTL8218E does not support 100Base-T2 mode, and this bit should always be 0.	0
1.8	Extended Status	RO	1: Extended status information in Register 15 The RTL8218E always supports Extended Status Register.	1
1.7	Reserved	RO	Reserved.	1
1.6	MF Preamble Suppression	RO	The RTL8218E will accept management frames with preamble suppressed.	0
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/ LH	1: Remote fault indication from link partner has been detected 0: No remote fault indication detected This bit will remain set until it is cleared by reading register 1 via the management interface.	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable (permanently=1) 0: No Auto-negotiation capability	1
1.2	Link Status	RO/ LL	1: Link has not failed since previous read 0: Link has failed since previous read If the link fails, this bit will be set to 0 until this bit is read.	0
1.1	Jabber Detect	RO/ LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	0
1.0	Extended Capability	RO	1: Extended register capable (permanently=1) 0: Not extended register capable	1

8.3. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY part of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 18. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI), Respectively.	0x001C

8.4. Register 3: PHY Identifier 2

Table 19. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th Bits of the OUI.	110010
3.[9:4]	Model Number	RO	Manufacturer's Model Number.	011000
3.[3:0]	Revision Number	RO	Manufacturer's Revision Number.	0011

8.5. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8218E is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 20. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0.	0
4.13	Remote Fault	RW	1: Advertises that the RTL8218E has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved.	0
4.11	Asymmetric Pause	RW	1: Advertises that the RTL8218E has asymmetric flow control capability 0: No asymmetric flow control capability	0
4.10	Pause	RW	1: Advertises that the RTL8218E has flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	1: 100Base-T4 capable 0: Not 100Base-T4 capable (permanently=0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1

Reg.bit	Name	Mode	Description	Default
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	00001: IEEE 802.3	00001

Note 1: This Register 4 setting has no effect unless auto-negotiation is restarted or link down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

8.6. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 21. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Technology Ability Field. Received code word bit 12.	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (Read only).	0
5.10	Pause	RO	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (Read only).	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	00001: IEEE 802.3	00000

8.7. Register 6: Auto-Negotiation Expansion

Table 22. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:7]	Reserved	RO	Ignore On Read.	0
6.6	Receive Next Page Location Able	RO	1: Received next page storage location is specified by bit (6.5) 0: Received next page storage location is not specified by bit (6.5)	1
6.5	Received Next Page Storage Location	RO	1: Link Partner next pages are stored in Register 8 0: Link Partner next pages are stored in Register 5	1
6.4	Parallel Detection Fault	RO/LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	1: RTL8218E is Next Page able	1
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is Enabled, this bit means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

8.8. Register 7: Auto-Negotiation Next Page Transmit

Table 23. Register 7: Auto-Negotiation Next Page Transmit

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1: Another next page desired 0: No other next page to send	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
7.13	Message Page	RW	1: Message page	1
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0
7.11	Toggle	RO	Toggle Bit.	0
7.[10:0]	Message/Unformatted Field	RW	Content of Message/Unformatted Page.	000000 00001

8.9. Register 8: Auto-Negotiation Link Partner Next Page Ability

Table 24. Register 8: Auto-Negotiation Link Partner Next Page Ability

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15.	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14.	0
8.13	Message Page	RO	Received Link Code Word Bit 13.	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12.	0
8.11	Toggle	RO	Received Link Code Word Bit 11.	0
8.[10:0]	Message/Unformatted Field	RO	Received Link Code Word Bit 10:0.	0

8.10. Register 9: 1000Base-T Control

Table 25. Register 9: 1000Base-T Control

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select. 000: Normal mode 001: Test mode 1–Transmit waveform test 010: Test mode 2–Transmit jitter test in MASTER mode 011: Test mode 3–Transmit jitter test in SLAVE mode 100: Test mode 4–Transmitter distortion test 101, 110, 111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full-Duplex	RW	1: Advertise PHY is 1000Base-T Full-Duplex capable 0: Advertise PHY is not 1000Base-T Full-Duplex capable	1
9.8	1000Base-T Half-Duplex	RW	1: Advertise PHY is 1000Base-T Half-Duplex capable 0: Advertise PHY is not 1000Base-T Half-Duplex capable	0
9.[7:0]	Reserved	RW	Reserved.	0

8.11. Register 10: 1000Base-T Status

Table 26. Register 10: 1000Base-T Status

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full-Duplex	RO	1: Link partner is capable of 1000Base-T Full-Duplex 0: Link partner is not capable of 1000Base-T Full-Duplex	0
10.10	1000Base-T Half-Duplex	RO	1: Link partner is capable of 1000Base-T Half-Duplex 0: Link partner is not capable of 1000Base-T Half-Duplex	0
10.[9:8]	Reserved	RO	Reserved.	0
10.[7:0]	Idle Error Count	RO/SC	Idle Error Counter. The counter stops automatically when it reaches 0xFF.	0

8.12. Register 13: MMD Access Control Register

Table 27. Register 13: MMD Access Control Register

Reg.bit	Name	Mode	Description	Default
13.[15:14]	Function	RW	13.[15:14] 00: Address 01: Data, no post increment 10: Data, post increment on read and writes 11: Data, post increment on writes only	0
13.[13:5]	Reserved	RW	Write as 0, ignore on read	0
13.[4:0]	MMD DEVAD	RW	Device address	0

8.13. Register 14: MMD Access Address Data Register

Table 28. Register 14: MMD Access Address Data Register

Reg.bit	Name	Mode	Description	Default
13.[15:10]	MMD Address Data	RW	If 13.[15:14] = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the content of its address register	0

8.14. Register 15: Extended Status

Table 29. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000Base-X Full-Duplex	RO	1: 1000Base-X Full-Duplex capable 0: Not 1000Base-X Full-Duplex capable	0
15.14	1000Base-X Half-Duplex	RO	1: 1000Base-X Half-Duplex capable 0: Not 1000Base-X Half-Duplex capable	0
15.13	1000Base-T Full-Duplex	RO	1: 1000Base-T Full-Duplex capable 0: Not 1000Base-T Full-Duplex capable	1
15.12	1000Base-T Half-Duplex	RO	1: 1000Base-T Half-Duplex capable 0: Not 1000Base-T Half-Duplex capable	0
15.[11:0]	Reserved	RO	Reserved.	0

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability may be affected. All voltages are specified reference to GND unless otherwise specified.

Table 30. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, AVDDH Supply Voltage Referenced to GND	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Referenced to GND	GND-0.3	+0.99	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

9.2. Operating Range

Table 31. Operating Range

Parameter	Min	Typ	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDIO, AVDDH Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Range	0.855	0.9	0.945	V

9.3. Power Consumption

Table 32. XSGMII Mode Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
System Idle (All ports are in link-down state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
1000Base-T Active (8 1000base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	519	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	686	-	mA
EEE 1000Base-T Linkup (8 1000base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
100Base-TX Active (8 100base-TX Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
EEE 100Base-TX Linkup (8 100base-TX Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
10Base-T Active (8 10base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
DVDDIO=3.3V					
TTL Input High Voltage	V_{IH}	2.0	-	-	V
TTL Input Low Voltage	V_{IL}	-	-	0.7	V
Output High Voltage	V_{OH}	2.7	-	-	V
Output Low Voltage	V_{OL}	-	-	0.6	V

Note: DVDDIO=3.3V, AVDDH=3.3V, DVDDL=0.9V, AVDDL=0.9V, SVDDL=0.9V.

Table 33.QSGMII Mode Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
System Idle (All ports are in link-down state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
1000Base-T Active (8 1000base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	521	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	634	-	mA
EEE 1000Base-T Linkup (8 1000base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
100Base-TX Active (8 100base-TX Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
EEE 100Base-TX Linkup (8 100base-TX Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
10Base-T Active (8 10base-T Ports are in link-up state)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	TBD	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	TBD	-	mA
DVDDIO=3.3V					
TTL Input High Voltage	V_{IH}	2.0	-	-	V
TTL Input Low Voltage	V_{IL}	-	-	0.7	V
Output High Voltage	V_{OH}	2.7	-	-	V
Output Low Voltage	V_{OL}	-	-	0.6	V

Note: DVDDIO=3.3V, AVDDH=3.3V, DVDDL=0.9V, AVDDL=0.9V, SVDDL=0.9V.

9.4. IEEE 10/100/1000Base-T Specifications

Table 34. IEEE 10/100/1000Base-T Specifications

Parameter	Min	Typ	Max	Units
1000Base-T				
Peak Voltage of Point A	670	724.5	820	mV
Peak Voltage of Point B	670	726.0	820	mV
Difference between the Peak Voltage of Point A and Point B	-	0.467	1	%
Difference between the Peak Voltage of Point C and 0.5 Times the Average of the Peak Voltage of Points A and B	-	0.47	2	%
Difference between the Peak Voltage of Point D and 0.5 Times the Average of the Peak Voltage of Points A and B	-	0.66	2	%
Droop off Point G	73.1	85.4	-	%
Droop off Point J	73.1	826	-	%
Transmitter Distortion	-	8.5	10	mV
Common Mode Output Voltage	-	46.4	50	mV
100Base-TX				
Peak Voltage (+Vout)	950	1017	1050	mV
Peak Voltage (-Vout)	-950	-1017	-1050	mV
Amplitude Symmetry	0.98	1.001	1.02	-
Rise Time (+Vout)	3	3.56	5	ns
Rise Time (-Vout)	3	3.51	5	ns
Fall Time (+Vout)	3	3.54	5	ns
Fall Time (-Vout)	3	3.48	5	ns
Rise/Fall Symmetry (+Vout)	-	70.2	500	ps
Rise/Fall Symmetry (-Vout)	-	70.1	500	ps
Overshoot (+Vout)	-	0.8	5	%
Overshoot (-Vout)	-	1.1	5	%
Transmit Jitter (+Vout)	-	0.62	1.4	ns
Transmit Jitter (-Vout)	-	0.61	1.4	ns
Distortion (Duty Cycle)	-	80	500	ps
10Base-T				
Link Pulse Timing	8	16	24	ms
Differential Voltage	2.2	2.57	2.8	V
Peak-to-Peak Normal Jitter with Cable	-	1.7	11	ns
Peak-to-Peak 8.0 BT Jitter with Cable	-	8.2	22	ns
Peak-to-Peak 8.5 BT Jitter with Cable	-	11.73	22	ns
Peak-to-Peak Normal Jitter without Cable	-	0.9	16	ns
Peak-to-Peak 8.0 BT Jitter without Cable	-	1.2	40	ns
Peak-to-Peak 8.5 BT Jitter without Cable	-	1.3	40	ns
Common Mode Output Voltage	-	23.55	50	mV

9.5. XSGMII Characteristics

9.5.1. XSGMII Differential Transmitter Characteristics

Table 35. XSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	97	-	ps	-
$V_{TX\text{-}DIFFp\text{-}p}$	Output Differential Voltage	400	-	1200	mV	-
T_J	Output Jitter	-	-	0.28	UI	-
R_{TX}	Differential Resistance	-	100	-	ohm	-

9.5.2. XSGMII Differential Receiver Characteristics

Table 36. QSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	97	-	ps	-
$V_{RX\text{-}DIFFp\text{-}p}$	Input Differential Voltage	200	-	950	mV	-
R_{RX}	Differential Resistance	-	100	-	ohm	-

9.5.3. QSGMII Differential Transmitter Characteristics

Table 37 QSGMII Differential Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Unit Interval	UI	199.94	200	200.06	ps
Output Offset Voltage	VTX-OFFSET	600	800	1000	mV
Output Differential Voltage	VTX-DIFFp-p	400	700	1200	mV
Output Total Jitter	T_TJ	-	-	0.35	UI

9.5.4. QSGMII Differential Receiver Characteristics

Table 38 QSGMII Differential Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Unit Interval	UI	199.94	200	200.06	ps
Input Differential Voltage	$V_{RX\text{-}DIFFp\text{-}p}$	200	-	950	mV
Differential Resistance	R_{RX}	-	100	-	ohm

9.6. XTALI Clock Characteristics

Table 39. Crystal Clock Characteristics

Parameter	Min	Typ	Max	Units
Frequency of XTALI	-	25	-	MHz
Frequency Tolerance of XTALI	-50	-	+50	ppm
Duty Cycle of XTALI	40	-	60	%
Equivalent Series Resistance Note1	-	-	Note1	ohm
Input High Level (Vih)	2.2	-	-	V
Input Low Level (Vil)	-	-	0.8	V

Note1:
Shunt Capacitance (C0)=3pF, the maximum value =50 Ω
Shunt Capacitance (C0)=5pF, the maximum value =40 Ω
Shunt Capacitance (C0)=7pF, the maximum value =30 Ω

Table 40. XTALI External Input Clock Characteristics

Parameter	Min	Typ	Max	Units
Frequency of XTALI	-	25	-	MHz
Frequency Tolerance of XTALI	-50	-	+50	ppm
Duty Cycle of XTALI	40	-	60	%
Rise Time of XTALI (10% ~ 90%)	-	-	4	ns
Fall Time of XTALI (10% ~ 90%)	-	-	4	ns
Jitter(Rms) Note1	-	-	1	ps
Phase Noise Note1	-	-	1	ps
Input High Level (Vih)	2.2	-		V
Input Low Level (Vil)	-	-	0.8	V

Note1 :BW 12KHz~10MHz

9.7. Power and Reset Characteristics

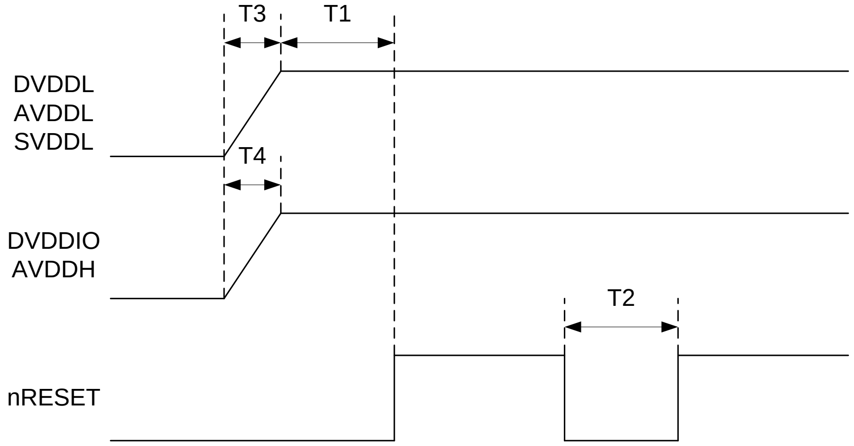


Figure 15. Power and Reset Characteristics

Table 41. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Delay Time	t1	The duration from 'all power steady' to the reset signal released to high	I	10	-	-	ms
Reset Low Time	t2	The duration of reset signal remaining low time before issuing a reset to the RTL8218E	I	10	-	-	ms
VDDL Power Rise Settling Time	t3	DVDDL, AVDDL, and SVDDL power rise settling time	I	0.5	-	-	ms
VDDH Power Rise Settling Time	t4	DVDDIO, and AVDDH power rise settling time	I	0.5	-	-	ms

9.8. MDC/MDIO Interface Characteristics

The RTL8218E supports the IEEE compliant Management Data Input/Output (MDIO) Interface. This is the only method for the MAC to acquire the status of the PHY. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the master sources the MDIO signal. In a read command, the slave sources the MDIO signal.

- The timing characteristics t1, t2, and t3 (Figure 16) of the Master (MAC) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics t4 (Figure 17) of the Slave (RTL8218E) are provided by the RTL8218E when the RTL8218E sources the MDIO signal (Read command)

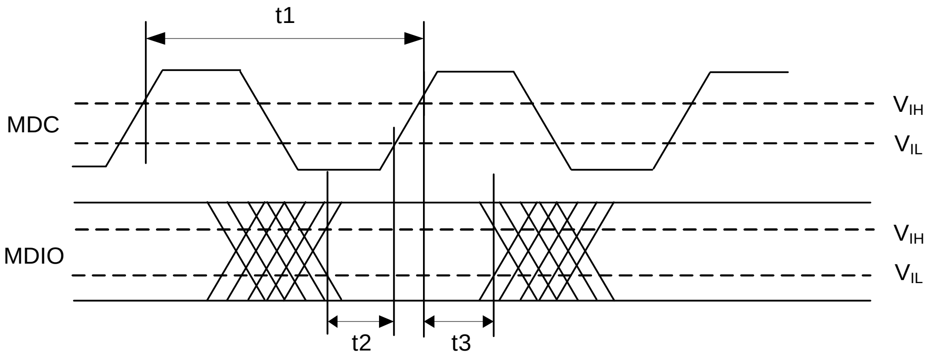


Figure 16. MDIO Sourced by Master (MAC)

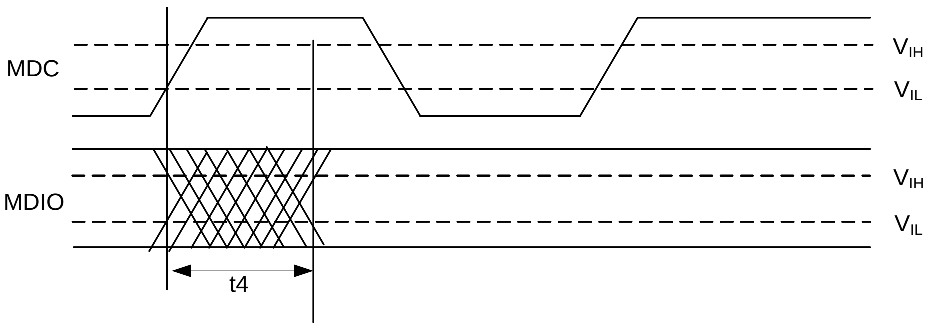


Figure 17. MDIO Sourced by RTL8218E (Slave)

Table 42. MDIO Timing Characteristics and Requirement

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	80	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	10	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	10	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	48	ns

9.9. LED Characteristics

9.9.1. Serial LED Timing

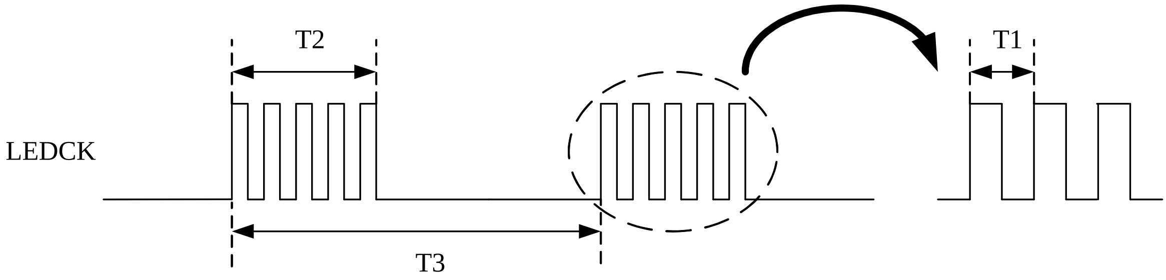


Figure 18. Serial LED Timing

Table 43. Serial LED Timing

Symbol	Description	Min	Typ	Max	Units
T1	Serial LED Clock Cycle Time	-	192	-	ns
T2	Serial LED Clock On/Off Duration	-	6.82	-	us
T3	Serial LED Burst Cycle Time	-	32	-	ms

10. Thermal Characteristics

10.1. Assembly Description

Table 44. Assembly Description

Package	Type	E-Pad LQFP-128
	Dimension (L×W)	14×20mm
	Thickness	1.4mm
PCB	PCB Dimension (L×W)	76.2×114.3mm
	PCB Thickness	1.6mm
	Number of Cu Layer-PCB	4-Layer (2S2P)
Heat Sink	-	35.8 x 35 x 28 mm^3

10.2. Material Properties

Table 45. Material Properties

Item		**Material**	**Thermal Conductivity K (W/m-k)**
Package	Die	Si	147
	Silver Paste	1033BF	1.0
	Lead Frame	CDA7025	168
	Mold Compound	G631	0.9
PCB		Cu	400
		FR4	0.2

10.3. Simulation Conditions

Table 46. Simulation Conditions

Input Power	2.6W
Test Board (PCB)	4L (2S2P)
Control Condition	Air Flow = 0m/s

10.4. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convention

Table 47. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convention

PCB Layer	θ_{JA}	θ_{JC}	Ψ_{JT}
4L PCB	25.7	12.3	0.89

.

10.5. Thermal Performance of E-Pad LQFP-128 with External Heat-Sink on PCB under Natural Convention

External Heat-Sink size: 35.8 x 35 x 28 mm^3

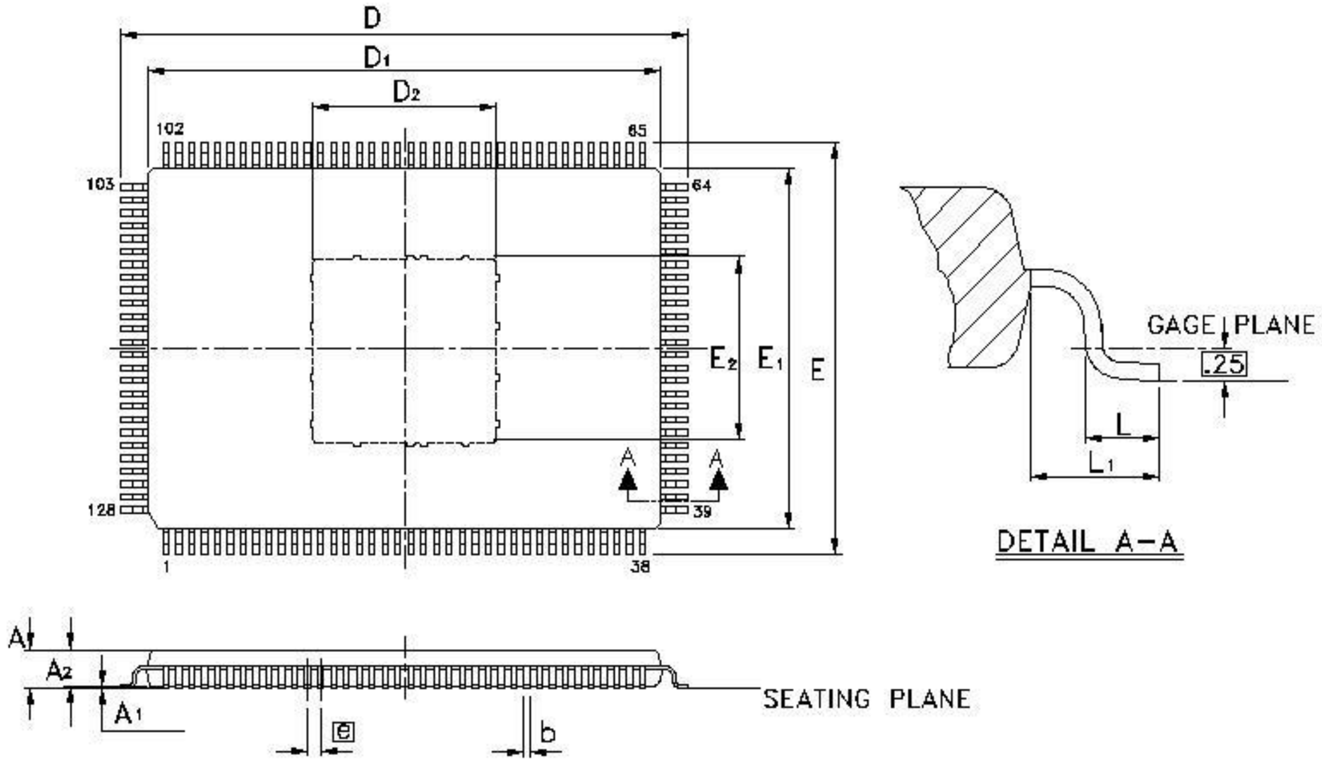
Table 48. Thermal Performance of E-Pad LQFP-128 with External Heat-Sink on PCB under Natural Convention

PCB Layer	θ_{JA}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	16.8	-	10.7	11.0

Note:
θ_{JA}: Junction to ambient thermal resistance.
Ψ_{JT}: Junction to top center of package thermal characterization.
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization.

11. Mechanical Dimensions

11.1. LQFP-128 E-PAD Package



11.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D	21.90	22.00	22.10	0.862	0.866	0.870
D_1	19.90	20.00	20.10	0.783	0.787	0.791
D_2/E_2	—	5.6	—	—	0.220	—
E	15.90	16.00	16.10	0.626	0.630	0.634
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

12. Ordering Information

Table 49. Ordering Information

Part Number	Package	Status
RTL8218E-CG	LQFP-128 EPAD Green Package	Mass Production

Note: See page 5 for package identification information.

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