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**RTL8212F-GR  
RTL8212G-GR**

**INTEGRATED DUAL 10/100/1000BASE-T  
AND 1000BASE-X/100BASE-FX GIGABIT  
ETHERNET TRANSCEIVER**

**DATASHEET**  
**(CONFIDENTIAL: Development Partners Only)**

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## USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8212F/RTL8212G IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/05/08	First release.



## Table of Contents

1. GENERAL DESCRIPTION.....	1
2. FEATURES.....	1
3. SYSTEM APPLICATIONS.....	2
4. BLOCK DIAGRAM.....	3
5. PIN ASSIGNMENTS .....	4
5.1. RTL8212F (LQFP128) PIN ASSIGNMENTS .....	4
5.2. GREEN PACKAGE AND VERSION IDENTIFICATION .....	4
5.3. RTL8212G (LQFP164) PIN ASSIGNMENTS .....	5
5.4. GREEN PACKAGE AND VERSION IDENTIFICATION .....	5
5.5. PIN ASSIGNMENT CODES .....	6
5.6. RTL8212F (LQFP128) PIN ASSIGNMENTS TABLE .....	6
5.7. RTL8212G (LQFP164) PIN ASSIGNMENTS TABLE .....	8
6. PIN DESCRIPTIONS.....	10
6.1. MEDIA DEPENDENT INTERFACE PINS.....	10
6.2. SERDES INTERFACE PINS .....	10
6.3. RGMII INTERFACE PINS .....	11
6.4. GMII/MII INTERFACE PINS (RTL8212G ONLY).....	12
6.5. SGMII INTERFACE PINS.....	13
6.6. LED INTERFACE PINS .....	13
6.7. SERIAL MANAGEMENT INTERFACE PINS .....	14
6.8. MISCELLANEOUS PINS .....	14
6.9. CONFIGURATION PINS.....	15
6.10. POWER AND GROUND PINS .....	17
7. FUNCTIONAL DESCRIPTION.....	18
7.1. OPERATION MODE .....	18
7.1.1. Copper to RGMII/GMII/MII.....	18
7.1.2. Fiber to RGMII/GMII/MII.....	18
7.1.3. Copper to SGMII.....	19
7.2. INTEGRATED GIGABIT PHY .....	20
7.2.1. MDI Interface.....	20
7.2.2. 1000Base-T Transmit Function.....	20
7.2.3. 1000Base-T Receive Function.....	20
7.2.4. 100Base-TX Transmit Function.....	20
7.2.5. 100Base-TX Receive Function.....	21
7.2.6. 10Base-T Transmit Function.....	21
7.2.7. 10Base-T Receive Function.....	21
7.2.8. Auto-Negotiation Function.....	21
7.2.9. PHY Register.....	21
7.2.10. Crossover Detection and Auto Correction.....	21
7.2.11. Polarity Correction.....	22
7.2.12. Green Ethernet .....	22
7.3. INTEGRATED SERDES.....	23
7.3.1. 1000Base-X Mode .....	23
7.3.2. 100Base-FX Mode .....	24
7.3.3. SGMII Mode.....	25
7.4. RESET .....	25
7.5. MAC INTERFACE .....	26





7.5.1.	GMII/MII (RTL8212G Only) .....	26
7.5.2.	RGMII.....	27
7.5.3.	SGMII .....	29
7.5.4.	Serial Management Interface (SMI) .....	29
7.6.	BACKWARD COMPATIBLE MODE .....	31
7.7.	LED FUNCTION.....	31
7.7.1.	Status Indication.....	31
7.7.2.	LED Mode Settings.....	34
7.7.3.	Bi-Color LED .....	35
<b>8.</b>	<b>REGISTER DESCRIPTIONS.....</b>	<b>36</b>
8.1.	REGISTER LIST .....	36
8.2.	PORT 0~1 REGISTER 0: CONTROL .....	37
8.3.	PORT 0~1 REGISTER 1: STATUS.....	38
8.4.	PORT 0~1 REGISTER 2: PHY IDENTIFIER 1 .....	39
8.5.	PORT 0~1 REGISTER 3: PHY IDENTIFIER 2.....	39
8.6.	PORT 0~1 REGISTER 4: 1000BASE-T AUTO-NEGOTIATION ADVERTISEMENT.....	39
8.7.	PORT 0~1 REGISTER 4: 1000BASE-X AUTO-NEGOTIATION ADVERTISEMENT .....	40
8.8.	PORT 0~1 REGISTER 5: 1000BASE-T AUTO-NEGOTIATION LINK PARTNER ABILITY .....	40
8.9.	PORT 0~1 REGISTER 5: 1000BASE-X AUTO-NEGOTIATION LINK PARTNER ABILITY .....	41
8.10.	PORT 0~1 REGISTER 6: 1000BASE-T AUTO-NEGOTIATION EXPANSION.....	42
8.11.	PORT 0~1 REGISTER 6: 1000BASE-X AUTO-NEGOTIATION EXPANSION .....	42
8.12.	PORT 0~1 REGISTER 7: 1000BASE-T AND 1000BASE-X AUTO-NEGOTIATION PAGE TRANSMIT REGISTER .....	43
8.13.	PORT 0~1 REGISTER 8: 1000BASE-T AND 1000BASE-X AUTO-NEGOTIATION LINK PARTNER NEXT PAGE REGISTER 43	43
8.14.	PORT 0~1 REGISTER 9: 1000BASE-T CONTROL REGISTER.....	44
8.15.	PORT 0~1 REGISTER 10: 1000BASE-T STATUS REGISTER .....	44
8.16.	PORT 0~1 REGISTER 15: EXTENDED STATUS .....	45
8.17.	PORT 0~1 REGISTER 31: PAGE SELECTION .....	45
<b>9.</b>	<b>CHARACTERISTICS.....</b>	<b>46</b>
9.1.	ABSOLUTE MAXIMUM RATINGS .....	46
9.2.	OPERATING RANGE.....	46
9.3.	DC CHARACTERISTICS .....	46
9.3.1.	Digital IO DC Characteristics .....	46
9.3.2.	Power Consumption for RGMII Application .....	47
9.3.3.	Power Consumption for GMII/MII Application (RTL8212G Only) .....	49
9.3.4.	Power Consumption for SGMII Application .....	51
9.4.	AC CHARACTERISTICS .....	52
9.4.1.	SerDes Transmitter Signal Electrical Characteristics .....	52
9.4.2.	SerDes Receiver Signal Electrical Characteristics .....	52
9.4.3.	RGMII Timing .....	53
9.4.4.	GMII/MII Timing (RTL8212G Only) .....	55
9.4.5.	SMI Timing .....	56
9.4.6.	Serial LED Timing .....	57
<b>10.</b>	<b>DESIGN AND LAYOUT.....</b>	<b>58</b>
10.1.	GENERAL GUIDELINES .....	58
10.2.	ETHERNET MDI DIFFERENTIAL SIGNAL LAYOUT GUIDELINES .....	58
10.3.	POWER PLANES.....	58
10.4.	GROUND PLANE .....	58
10.5.	TRANSFORMER OPTIONS .....	59
<b>11.</b>	<b>MECHANICAL DIMENSIONS.....</b>	<b>60</b>
11.1.	RTL8212F-GR: LQFP-128 E-PAD PACKAGE.....	60





## RTL8212F & RTL8212G Datasheet

11.2. MECHANICAL DIMENSIONS NOTES FOR RTL8212F-GR LQFP-128 (14*20MM) .....	61
11.3. RTL8212G-GR: LQFP-164 E-PAD PACKAGE .....	62
11.4. MECHANICAL DIMENSIONS NOTES FOR RTL8212G-GR LQFP-164 (20*20MM) .....	63
<b>12. ORDERING INFORMATION .....</b>	<b>64</b>



## List of Tables

TABLE 1. RTL8212F (LQFP128) PIN ASSIGNMENTS TABLE .....	6
TABLE 2. RTL8212G (LQFP164) PIN ASSIGNMENTS TABLE .....	8
TABLE 3. MEDIA DEPENDENT INTERFACE PINS .....	10
TABLE 4. SERDES INTERFACE PINS .....	10
TABLE 5. RGMII INTERFACE PINS .....	11
TABLE 6. GMII/MII INTERFACE PINS (RTL8212G ONLY) .....	12
TABLE 7. SGMII INTERFACE PINS .....	13
TABLE 8. LED INTERFACE PINS .....	13
TABLE 9. SERIAL MANAGEMENT INTERFACE PINS .....	14
TABLE 10. MISCELLANEOUS PINS .....	14
TABLE 11. CONFIGURATION PINS .....	15
TABLE 12. POWER AND GND PINS .....	17
TABLE 13. MAPPING OF TWISTED-PAIR OUTPUTS TO RJ-45 CONNECTORS .....	20
TABLE 14. MEDIA DEPENDENT INTERFACE PIN MAPPING .....	22
TABLE 15. RESISTANCE SELECTION VS. 1X9 FIBER TRANSCEIVER VCC .....	24
TABLE 16. CONFIGURATION AND DATA RATES SUPPORTED FOR EACH INTERFACE .....	26
TABLE 17. GMII/MII (RTL8212G ONLY) .....	26
TABLE 18. TX_ER AND TX_EN ENCODING .....	28
TABLE 19. RX_ER AND RX_DV ENCODING .....	28
TABLE 20. RGMII TIMING MODES .....	28
TABLE 21. SMI READ/WRITE CYCLES .....	30
TABLE 22. LED DEFAULT SETTINGS .....	31
TABLE 23. LED DEFINITIONS .....	32
TABLE 24. LED MAPPING CODE .....	33
TABLE 25. AVAILABLE LED SIGNAL PAIRS FOR BI-COLOR LED .....	35
TABLE 26. BI-COLOR LED TRUTH TABLE FOR PARALLEL LED MODE .....	35
TABLE 27. REGISTER LIST .....	36
TABLE 28. PORT 0~1 REGISTER 0: CONTROL .....	37
TABLE 29. PORT 0~1 REGISTER 1: STATUS .....	38
TABLE 30. PORT 0~1 REGISTER 2: PHY IDENTIFIER 1 .....	39
TABLE 31. PORT 0~1 REGISTER 3: PHY IDENTIFIER 2 .....	39
TABLE 32. PORT 0~1 REGISTER 4: 1000BASE-T AUTO-NEGOTIATION ADVERTISEMENT .....	39
TABLE 33. PORT 0~1 REGISTER 4: 1000BASE-X AUTO-NEGOTIATION ADVERTISEMENT .....	40
TABLE 34. PORT 0~1 REGISTER 5: 1000BASE-T AUTO-NEGOTIATION LINK PARTNER ABILITY .....	40
TABLE 35. PORT 0~1 REGISTER 5: 1000BASE-X AUTO-NEGOTIATION LINK PARTNER ABILITY .....	41
TABLE 36. PORT 0~1 REGISTER 6: 1000BASE-T AUTO-NEGOTIATION EXPANSION .....	42
TABLE 37. PORT 0~1 REGISTER 6: 1000BASE-X AUTO-NEGOTIATION EXPANSION .....	42
TABLE 38. PORT 0~1 REGISTER 7: AUTO-NEGOTIATION PAGE TRANSMIT REGISTER .....	43
TABLE 39. PORT 0~1 REGISTER 8: AUTO-NEGOTIATION LINK PARTNER NEXT PAGE REGISTER .....	43
TABLE 40. PORT 0~1 REGISTER 9: 1000BASE-T CONTROL REGISTER .....	44
TABLE 41. PORT 0~1 REGISTER 10: 1000BASE-T STATUS REGISTER .....	44
TABLE 42. PORT 0~1 REGISTER 15: EXTENDED STATUS .....	45
TABLE 43. PORT 0~1 REGISTER 31: PAGE SELECTION .....	45
TABLE 44. ABSOLUTE MAXIMUM RATINGS .....	46
TABLE 45. OPERATING RANGE .....	46
TABLE 46. DIGITAL IO DC CHARACTERISTICS .....	46
TABLE 47. POWER CONSUMPTION FOR RGMII APPLICATION .....	47
TABLE 48. POWER CONSUMPTION FOR GMII/MII APPLICATION (RTL8212G ONLY) .....	49
TABLE 49. POWER CONSUMPTION FOR SGMII APPLICATION .....	51
TABLE 50. SERDES DIFFERENTIAL TRANSMITTER OUTPUT PARAMETERS .....	52
TABLE 51. SERDES DIFFERENTIAL RECEIVER INPUT PARAMETERS .....	52
TABLE 52. RGMII TIMING PARAMETERS .....	54



TABLE 53. GMII/MII TIMING PARAMETERS (RTL8212G ONLY).....	55
TABLE 54. SMI TIMING PARAMETERS .....	56
TABLE 55. SERIAL LED TIMING PARAMETERS.....	57
TABLE 56. ORDERING INFORMATION.....	64

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## List of Figures

FIGURE 1. GMII/RGMII APPLICATION (GMII FOR LQFP-164 PACKAGE ONLY).....	2
FIGURE 2. SGMII APPLICATION.....	2
FIGURE 3. BLOCK DIAGRAM .....	3
FIGURE 4. RTL8212F (LQFP128) PIN ASSIGNMENTS.....	4
FIGURE 5. RTL8212G (LQFP164) PIN ASSIGNMENTS .....	5
FIGURE 6. COPPER TO RGMII/GMII/MII MODE .....	18
FIGURE 7. FIBER TO RGMII/GMII/MII .....	19
FIGURE 8. COPPER TO SGMII.....	19
FIGURE 9. CONCEPTUAL EXAMPLE OF POLARITY CORRECTION .....	22
FIGURE 10. SERDES WITH SFP FIBER TRANSCEIVER .....	23
FIGURE 11. SERDES WITH 1X9 FIBER TRANSCEIVER .....	23
FIGURE 12. RESET.....	25
FIGURE 13. GMII/MII SIGNAL DIAGRAM .....	27
FIGURE 14. RGMII SIGNAL DIAGRAM .....	27
FIGURE 15. SGMII SIGNAL DIAGRAM .....	29
FIGURE 16. DUAL SMI APPLICATION .....	30
FIGURE 17. HIGH ACTIVE AND LOW ACTIVE LED PIN FOR SINGLE-COLOR LED .....	34
FIGURE 18. SERIAL LED SIGNAL .....	34
FIGURE 19. SIGNAL ON 74164 .....	34
FIGURE 20. BI-COLOR LED IN PARALLEL LED MODE .....	35
FIGURE 21. RGMII TIMING .....	53
FIGURE 22. GMII/MII TIMING (RTL8212G ONLY).....	55
FIGURE 23. SMI TIMING .....	56
FIGURE 24. SERIAL LED TIMING .....	57

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## 1. General Description

The RTL8212F/RTL8212G integrates dual independent gigabit Ethernet transceivers (PHY) and dual gigabit SerDes into a single IC. The device performs all the physical layer functions for 1000Base-T, 100Base-TX, and 10Base-T Ethernet on category 5 UTP cable, except 1000Base-T half duplex. 10Base-T functionality can also be achieved over standard category 3 or 4 cable.

With gigabit SerDes, the RTL8212F/RTL8212G also supports 1000Base-X/100Base-FX and it can be connected directly to a fiber-optical transceiver. The RTL8212F/RTL8212G supports fiber/copper dual media for combo link applications.

This device perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. An integrated internal hybrid allows the use of inexpensive 1:1 transformer modules. Each of the two independent transceivers features an industrial standard SGMII/RGMII/GMII/MII for glueless connection with Ethernet MACs. The two SerDes, acting as 1000Base-X/100Base-FX fiber ports, support SGMII/RGMII (RTL8212F) and SGMII/RGMII/GMII/MII (RTL8212G).

The RTL8212F/RTL8212G adopts mixed mode  $0.13\mu\text{m}$  CMOS technology and analog line driver architecture, and is offered in thermally-enhanced 128/164-pin LQFP-EPAD packages. Enhanced ‘Green’ power-saving features allow very low power consumption.

## 2. Features

- Dual integrated 10/100/1000Base-T Gigabit Ethernet transceiver
- Dual integrated Gigabit SerDes supporting SGMII and 1000Base-X/100Base-FX
- RTL8212F supports RGMII/SGMII. RTL8212G supports RGMII/SGMII/GMII/MII
- Supports full duplex in 10/100/1000 speed and half duplex in 10/100 speed
- Crossover detection and auto correction in all speeds
- Physical layer Polarity Detection and Correction function
- Line driver architecture with low power dissipation
- Supports Realtek’s Green Ethernet power saving mode
- Supports cable diagnostic function
- Supports serial and parallel LED mode
- Supports jumbo packets up to 16KB
- 3.3V and 1.2V power supply
- $0.13\mu\text{m}$  CMOS process
- Packages:
  - ◆ RTL8212F-GR: LQFP-128 E-PAD
  - ◆ RTL8212G-GR: LQFP-164 E-PAD

### 3. System Applications

- Gigabit Ethernet switch
- Gigabit Ethernet routers
- Copper/Fiber combo links

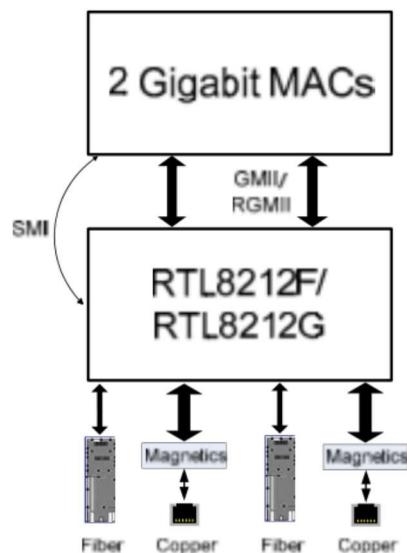


Figure 1. GMII/RGMII Application (GMII for LQFP-164 Package Only)

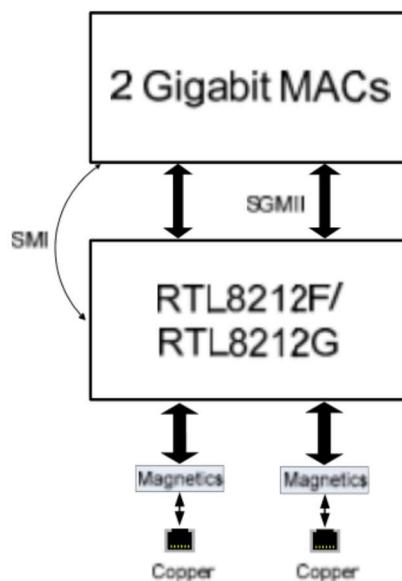


Figure 2. SGMII Application

## 4. Block Diagram

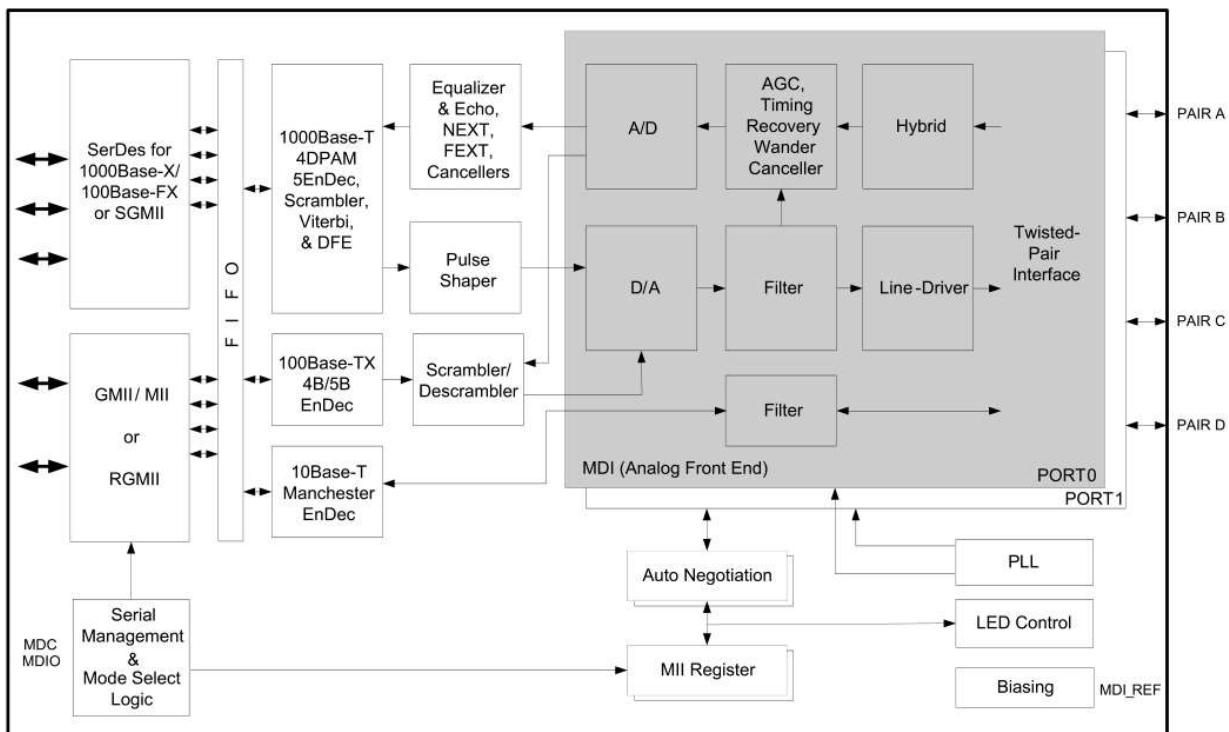


Figure 3. Block Diagram



## 5. Pin Assignments

### 5.1. RTL8212F (LQFP128) Pin Assignments

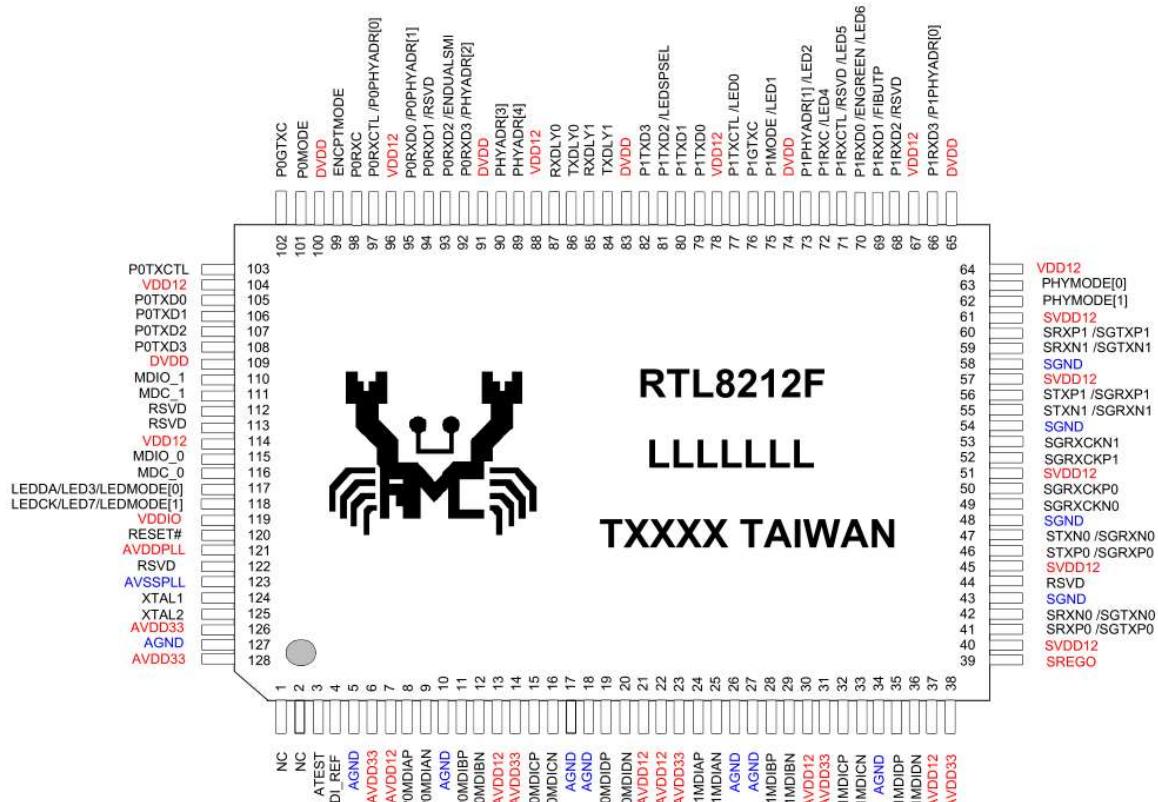


Figure 4. RTL8212F (LQFP128) Pin Assignments

### 5.2. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 4.

### 5.3. RTL8212G (LQFP164) Pin Assignments

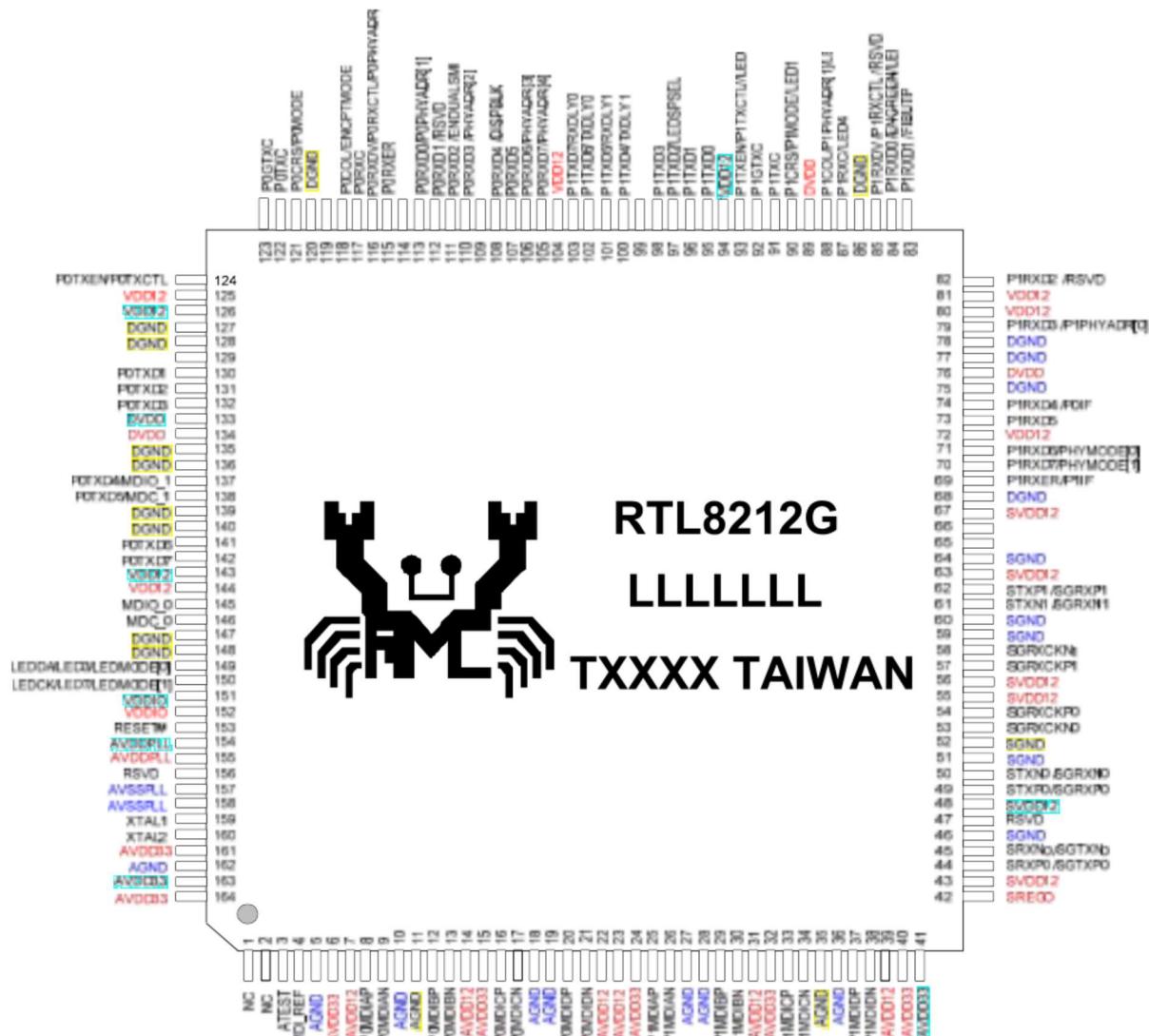


Figure 5. RTL8212G (LQFP164) Pin Assignments

### 5.4. Green Package and Version Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 5.





## 5.5. Pin Assignment Codes

I: Input pin

AI: Analog input pin

O: Output pin

AO: Analog output pin

I/O: Bi-direction input/output pin

AI/O: Analog Bi-direction input/output pin

P: Digital power pin

AP: Analog power pin

G: Digital ground pin

AG: Analog ground pin

I<sub>PD</sub>: Internal with pull-down resistor

SP: SerDes power pin

I<sub>PU</sub>: Internal with pull-up resistor

SG: SerDes ground pin

NC: Not Connected

## 5.6. RTL8212F (LQFP128) Pin Assignments Table

See Table 2, page 8, for RTL8212G (LQFP164) Assignments.

**Table 1. RTL8212F (LQFP128) Pin Assignments Table**

Pin No.	Name	Type
1	NC	-
2	NC	-
3	ATEST	AO
4	MDI_REF	AO
5	AGND	AG
6	AVDD33	AP
7	AVDD12	AP
8	P0MDIAP	AI/O
9	P0MDIAN	AI/O
10	AGND	AG
11	P0MDIBP	AI/O
12	P0MDIBN	AI/O
13	AVDD12	AP
14	AVDD33	AP
15	P0MDICP	AI/O
16	P0MDICN	AI/O
17	AGND	AG
18	AGND	AG
19	P0MDIDP	AI/O
20	P0MDIDN	AI/O
21	AVDD12	AP

Pin No.	Name	Type
22	AVDD12	AP
23	AVDD33	AP
24	P1MDIAP	AI/O
25	P1MDIAN	AI/O
26	AGND	AG
27	AGND	AG
28	P1MDIBP	AI/O
29	P1MDIBN	AI/O
30	AVDD12	AP
31	AVDD33	AP
32	P1MDICP	AI/O
33	P1MDICN	AI/O
34	AGND	AG
35	P1MDIDP	AI/O
36	P1MDIDN	AI/O
37	AVDD12	AP
38	AVDD33	AP
39	SREGO	O
40	SVDD12	SP
41	SRXP0/SGTXP0	AI
42	SRXN0/SGTXN0	AI



# RTL8212F & RTL8212G Datasheet

Pin No.	Name	Type
43	SGND	SG
44	RSVD	-
45	SVDD12	SP
46	STXP0/SGRXP0	AO
47	STXN0/SGRXN0	AO
48	SGND	SG
49	SGRXCKN0	AO
50	SGRXCKP0	AO
51	SVDD12	SP
52	SGRXCKP1	AO
53	SGRXCKN1	AO
54	SGND	SG
55	STXN1/SGRXN1	AO
56	STXP1/SGRXP1	AO
57	SVDD12	SP
58	SGND	SG
59	SRXN1/SGTXN1	AI
60	SRXP1/SGTXP1	AI
61	SVDD12	SP
62	PHYMODE[0]	I (I <sub>PD</sub> )
63	PHYMODE[1]	I (I <sub>PD</sub> )
64	VDD12	P
65	DVDD	P
66	P1RXD3/P1PHYADR[0]	I/O (I <sub>PD</sub> )
67	VDD12	P
68	P1RXD2/RSVD	O (I <sub>PD</sub> )
69	P1RXD1/FIBUTP	I/O (I <sub>PD</sub> )
70	P1RXD0/ENGREEN/LED6	I/O (I <sub>PD</sub> )
71	P1RXCTL/RSVD/LED5	I/O (I <sub>PD</sub> )
72	P1RXC/LED4	O (I <sub>PD</sub> )
73	P1PHYADR[1]/LED2	I/O (I <sub>PD</sub> )
74	DVDD	P
75	P1MODE/LED1	I/O (I <sub>PD</sub> )
76	P1GTXC	I (I <sub>PD</sub> )
77	P1TXCTL/LED0	I/O (I <sub>PD</sub> )
78	VDD12	P
79	P1TXD0	I (I <sub>PD</sub> )
80	P1TXD1	I (I <sub>PD</sub> )
81	P1TXD2/LEDSPSEL	I (I <sub>PD</sub> )
82	P1TXD3	I (I <sub>PD</sub> )
83	DVDD	P
84	TXDLY1	I (I <sub>PD</sub> )
85	RXDLY1	I (I <sub>PD</sub> )
86	TXDLY0	I (I <sub>PD</sub> )

Pin No.	Name	Type
87	RXDLY0	I (I <sub>PD</sub> )
88	VDD12	P
89	PHYADR[4]	I (I <sub>PD</sub> )
90	PHYADR[3]	I (I <sub>PD</sub> )
91	DVDD	P
92	P0RXD3 /PHYADR[2]	I/O (I <sub>PD</sub> )
93	P0RXD2/ENDUALSMI	I/O (I <sub>PD</sub> )
94	P0RXD1/RSVD	I/O (I <sub>PD</sub> )
95	P0RXD0/P0PHYADR[1]	I/O (I <sub>PD</sub> )
96	VDD12	P
97	P0RXCTL/P0PHYADR[0]	I/O (I <sub>PD</sub> )
98	P0RXC	O (I <sub>PD</sub> )
99	ENCPTMODE	I (I <sub>PD</sub> )
100	DVDD	P
101	P0MODE	I (I <sub>PD</sub> )
102	P0GTXC	I (I <sub>PD</sub> )
103	P0TXCTL	I (I <sub>PD</sub> )
104	VDD12	P
105	P0TXD0	I (I <sub>PD</sub> )
106	P0TXD1	I (I <sub>PD</sub> )
107	P0TXD2	I (I <sub>PD</sub> )
108	P0TXD3	I (I <sub>PD</sub> )
109	DVDD	P
110	MDIO_1	I/O (I <sub>PD</sub> )
111	MDC_1	I (I <sub>PD</sub> )
112	RSVD	-
113	RSVD	-
114	VDD12	P
115	MDIO_0	I/O (I <sub>PU</sub> )
116	MDC_0	I (I <sub>PU</sub> )
117	LEDDA/LED3/LEDMODE[0]	I/O (I <sub>PU</sub> )
118	LEDCK/LED7/LEDMODE[1]	I/O (I <sub>PU</sub> )
119	VDDIO	P
120	RESET#	I
121	AVDDPLL	AP
122	RSVD	-
123	AVSSPLL	AG
124	XTAL1	AI
125	XTAL2	AO
126	AVDD33	AP
127	AGND	AG
128	AVDD33	AP
EPAD	DGND	G





## 5.7. RTL8212G (LQFP164) Pin Assignments Table

Table 2. RTL8212G (LQFP164) Pin Assignments Table

Pin No.	Name	Type
1	NC	-
2	NC	-
3	ATEST	AO
4	MDI_REF	AO
5	AGND	AG
6	AVDD33	AP
7	AVDD12	AP
8	P0MDIAP	AI/O
9	P0MDIAN	AI/O
10	AGND	AG
11	AGND	AG
12	P0MDIBP	AI/O
13	P0MDIBN	AI/O
14	AVDD12	AP
15	AVDD33	AP
16	P0MDICP	AI/O
17	P0MDICN	AI/O
18	AGND	AG
19	AGND	AG
20	P0MDIDP	AI/O
21	P0MDIDN	AI/O
22	AVDD12	AP
23	AVDD12	AP
24	AVDD33	AP
25	P1MDIAP	AI/O
26	P1MDIAN	AI/O
27	AGND	AG
28	AGND	AG
29	P1MDIBP	AI/O
30	P1MDIBN	AI/O
31	AVDD12	AP
32	AVDD33	AP
33	P1MDICP	AI/O
34	P1MDICN	AI/O
35	AGND	AG
36	AGND	AG
37	P1MDIDP	AI/O
38	P1MDIDN	AI/O
39	AVDD12	AP
40	AVDD33	AP
41	AVDD33	AP

Pin No.	Name	Type
42	SREGO	O
43	SVDD12	SP
44	SRXP0/SGTXP0	AI
45	SRXN0/SGTXN0	AI
46	SGND	SG
47	RSVD	-
48	SVDD12	SP
49	STXP0/SGRXP0	AO
50	STXN0/SGRXN0	AO
51	SGND	SG
52	SGND	SG
53	SGRXCKN0	AO
54	SGRXCKP0	AO
55	SVDD12	SP
56	SVDD12	SP
57	SGRXCKP1	AO
58	SGRXCKN1	AO
59	SGND	SG
60	SGND	SG
61	STXN1/SGRXN1	AO
62	STXP1/SGRXP1	AO
63	SVDD12	SP
64	SGND	SG
65	SRXN1/SGTXN1	AI
66	SRXP1/SGTXP1	AI
67	SVDD12	SP
68	DGND	G
69	P1RXER/P1IF	I/O (I <sub>PD</sub> )
70	P1RXD7/PHYMODE[1]	I/O (I <sub>PD</sub> )
71	P1RXD6/PHYMODE[0]	I/O (I <sub>PD</sub> )
72	VDD12	P
73	P1RXD5	O (I <sub>PD</sub> )
74	P1RXD4/P0IF	O (I <sub>PD</sub> )
75	DGND	G
76	DVDD	P
77	DGND	G
78	DGND	G
79	P1RXD3/P1PHYADR[0]	I/O (I <sub>PD</sub> )
80	VDD12	P
81	VDD12	P
82	P1RXD2/RSVD	I/O (I <sub>PD</sub> )





# RTL8212F & RTL8212G Datasheet

Pin No.	Name	Type
83	P1RXD1/FIBUTP	I/O (I <sub>PD</sub> )
84	P1RXD0/ENGREEN/LED6	I/O (I <sub>PD</sub> )
85	P1RXDV/P1RXCTL/RSVD/ LED5	I/O (I <sub>PD</sub> )
86	DGND	G
87	P1RXC/LED4	O (I <sub>PD</sub> )
88	P1COL/P1PHYADR[1]/LED2	I/O (I <sub>PD</sub> )
89	DVDD	P
90	P1CRS/P1MODE/LED1	I/O (I <sub>PD</sub> )
91	P1TXC	I (I <sub>PD</sub> )
92	P1GTXC	I (I <sub>PD</sub> )
93	P1TXEN/P1TXCTL/LED0	I/O (I <sub>PD</sub> )
94	VDD12	P
95	P1TXD0	I (I <sub>PD</sub> )
96	P1TXD1	I (I <sub>PD</sub> )
97	P1TXD2/LEDSPSEL	I (I <sub>PD</sub> )
98	P1TXD3	I (I <sub>PD</sub> )
99	DVDD	P
100	P1TXD4/TXDLY1	I (I <sub>PD</sub> )
101	P1TXD5/RXDLY1	I (I <sub>PD</sub> )
102	P1TXD6/TXDLY0	I (I <sub>PD</sub> )
103	P1TXD7/RXDLY0	I (I <sub>PD</sub> )
104	VDD12	P
105	P0RXD7/PHYADR[4]	I/O (I <sub>PD</sub> )
106	P0RXD6/PHYADR[3]	I/O (I <sub>PD</sub> )
107	P0RXD5	O (I <sub>PD</sub> )
108	P0RXD4/DISPBLK	I/O (I <sub>PD</sub> )
109	DVDD	P
110	P0RXD3/PHYADR[2]	I/O (I <sub>PD</sub> )
111	P0RXD2/ENDUALSMI	I/O (I <sub>PD</sub> )
112	P0RXD1/RSVD	I/O (I <sub>PD</sub> )
113	P0RXD0/P0PHYADR[1]	I/O (I <sub>PD</sub> )
114	VDD12	P
115	P0RXER	O (I <sub>PD</sub> )
116	P0RXDV/P0RXCTL/ P0PHYADR[0]	I/O (I <sub>PD</sub> )
117	P0RXC	O (I <sub>PD</sub> )
118	P0COL/ENCPTMODE	I/O (I <sub>PD</sub> )
119	DVDD	P
120	DGND	G
121	P0CRS/P0MODE	I/O (I <sub>PD</sub> )
122	P0TXC	I (I <sub>PD</sub> )
123	P0GTXC	I (I <sub>PD</sub> )

Pin No.	Name	Type
124	P0TXEN/P0TXCTL	I (I <sub>PD</sub> )
125	VDD12	P
126	VDD12	P
127	DGND	G
128	DGND	G
129	P0TXD0	I (I <sub>PD</sub> )
130	P0TXD1	I (I <sub>PD</sub> )
131	P0TXD2	I (I <sub>PD</sub> )
132	P0TXD3	I (I <sub>PD</sub> )
133	DVDD	P
134	DVDD	P
135	DGND	G
136	DGND	G
137	P0TXD4/MDIO_1	I/O (I <sub>PD</sub> )
138	P0TXD5/MDC_1	I/O (I <sub>PD</sub> )
139	DGND	G
140	DGND	G
141	P0TXD6	I (I <sub>PD</sub> )
142	P0TXD7	I (I <sub>PD</sub> )
143	VDD12	P
144	VDD12	P
145	MDIO_0	I/O (I <sub>PU</sub> )
146	MDC_0	I (I <sub>PU</sub> )
147	DGND	G
148	DGND	G
149	LEDDA/LED3/LEDMODE[0]	I/O (I <sub>PU</sub> )
150	LEDCK/LED7/LEDMODE[1]	I/O (I <sub>PU</sub> )
151	VDDIO	P
152	VDDIO	P
153	RESET#	I
154	AVDDPLL	AP
155	AVDDPLL	AP
156	RSVD	-
157	AVSSPLL	AG
158	AVSSPLL	AG
159	XTAL1	AI
160	XTAL2	AO
161	AVDD33	AP
162	AGND	AG
163	AVDD33	AP
164	AVDD33	AP
EPAD	DGND	G



## 6. Pin Descriptions

I: Input pin	AI: Analog input pin
O: Output pin	AO: Analog output pin
I/O: Bi-direction input/output pin	AI/O: Analog Bi-direction input/output pin
P: Digital power pin	AP: Analog power pin
G: Digital ground pin	AG: Analog ground pin
I <sub>PD</sub> : Internal with pull-down resistor	SP: SerDes power pin
I <sub>PU</sub> : Internal with pull-up resistor	SG: SerDes ground pin

### 6.1. Media Dependent Interface Pins

Table 3. Media Dependent Interface Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
8, 9	8, 9	P0MDIAP/N	AI/O	Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100Ω termination resistor.
12, 13	11, 12	P0MDIBP/N		
16, 17	15, 16	P0MDICP/N		
20, 21	19, 20	P0MDIDP/N		
25, 26	24, 25	P1MDIAP/N		
29, 30	28, 29	P1MDIBP/N		
33, 34	32, 33	P1MDICP/N		
37, 38	35, 36	P1MDIDP/N		

### 6.2. SerDes Interface Pins

Table 4. SerDes Interface Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
66, 44	60, 41	SRXP[1:0]	AI	SerDes Receive Pair. Differential serial input for fiber application. The differential pair has an internal 100ohm termination resistor.
65, 45	59, 42	SRXN[1:0]		
62, 49	56, 46	STXP[1:0]	AO	SerDes Transmit Pair. Differential serial output for fiber application. The differential pair has an internal 100ohm termination resistor.
61, 50	55, 47	STXN[1:0]		



Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
42	39	SREGO	AO	Internal Regulator's Output. When SerDes is not used as SGMII interface, this pin is the internal regulator's output. The internal regulator is used by SerDes circuit. It is strongly recommended to place a 10uF capacitor and a 0.1uF capacitor between this pin and GND. The voltage of this pin output is in the range of 1.2V~1.5V. When SerDes is used as SGMII interface, this pin is a SerDes 1.2V power pin and should be connected with SVDD12 power supplier.

### 6.3. RGMII Interface Pins

Table 5. RGMII Interface Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
123 92	102 76	P0GTXC P1GTXC	I (I <sub>PD</sub> )	RGMII Transmit Clock. All transmit inputs must be synchronized to this clock. Its frequency depends upon the link speed. 1000M: 125MHz      100M: 25MHz      10M: 2.5MHz
132 131 130 129 98 97 96 95	108 107 106 105 82 81 80 79	P0TXD3 P0TXD2 P0TXD1 P0TXD0 P1TXD3 P1TXD2 P1TXD1 P1TXD0	I (I <sub>PD</sub> )	RGMII Transmit Data Bus. In RGMII 1000Base-T mode, TXD[3:0] runs at a double data rate with bits[3:0] presented on the rising edge of the GTXC and bits[7:4] presented on the falling edge of the GTXC. TXD[7:4] are ignored in this mode. In RGMII 10/100Base-T modes, the transmitted data nibble is presented on TXD[3:0] on the rising edge of GTXC and duplicated on the falling edge of GTXC.
124 93	103 77	P0TXCTL P1TXCTL	I (I <sub>PD</sub> )	RGMII Transmit Control. The TXCTL indicates TXEN at rising of GTXC and the logical derivative of TXER and TXEN at the falling edge of GTXC.
117 87	98 72	P0RXC P1RXC	O (I <sub>PD</sub> )	RGMII Receive Clock. All RGMII receive outputs must be synchronized to this clock. Its frequency (with +/-50ppm tolerance) depends upon the link speed. 1000M: 125MHz      100M: 25MHz      10M: 2.5MHz
110 111 112 113 79 82 83 84	92 93 94 95 66 68 69 70	P0RXD3 P0RXD2 P0RXD1 P0RXD0 P1RXD3 P1RXD2 P1RXD1 P1RXD0	O (I <sub>PD</sub> )	RGMII Receive Data Bus. In RGMII 1000Base-T mode, RXD[3:0] runs at a double data rate with bits[3:0] presented on the rising edge of the RXC and bits[7:4] presented on the falling edge of the RXC. RXD[7:4] are ignored in this mode. In RGMII 10/100Base-T modes, the received data nibble is presented on RXD[3:0] on the rising edge of RXC and duplicated on the falling edge of RXC.
116 85	97 71	P0RXCTL P1RXCTL	O (I <sub>PD</sub> )	RGMII Receive Control. The RXCTL indicates RXDV at rising of RXC and the logical derivative of RXER and RXDV at the falling edge of RXC.



## 6.4. GMII/MII Interface Pins (RTL8212G Only)

**Table 6. GMII/MII Interface Pins (RTL8212G Only)**

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
123/92	-	P0GTXC/P1GTXC	I ( $I_{PD}$ )	GMII Transmit Clock. 125MHz transmit clock. All transmit data must be synchronized to this clock during 1000Base-T operation.
122/91	-	P0TXC/P1TXC	O ( $I_{PD}$ )	MII Transmit Clock. All transmit must be synchronized to this clock during 10/100 operation. It provides 25MHz clock reference in 100Base-TX mode, and 2.5MHz clock reference in 10Base-T.
124/93	-	P0TXEN/P1TXEN	I ( $I_{PD}$ )	GMII/MII Transmit Enable. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to GTXC in 1000Base-T mode and synchronous to TXC in 10/100Base-T mode.
142/141 138/137 132/131 130/129 103/102 101/100 98/97 96/95	-	P0TXD7/P0TXD6 P0TXD5/P0TXD4 P0TXD3/P0TXD2 P0TXD1/P0TXD0 P1TXD7/P1TXD6 P1TXD5/P1TXD4 P1TXD3/P1TXD2 P1TXD1/P1TXD0	I ( $I_{PD}$ )	GMII/MII Transmit Data Bus. The width of this synchronous input bus varies with the speed mode. 1000M: TXD[7:0] are used 10/100M: TXD[3:0] are used; TXD[7:4] are ignored TXD[7:0] is synchronous to GTXC in 1000Base-T mode and synchronous to TXC in 10/100Base-TX mode.
117/87	-	P0RXC/P1RXC	O ( $I_{PD}$ )	GMII/MII Receive Clock. The MII/GMII Receive output clock is used to synchronize received signals. Its frequency depends upon the link speed. 1000M: 125MHz    100M: 25MHz    10M: 2.5MHz
116/85	-	P0RXDV/P1RXDV	O ( $I_{PD}$ )	GMII/MII Receive Data Valid. This synchronous output is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
121/90	-	P0CRS/P1CRS	O ( $I_{PD}$ )	MII Carrier Sense. This asynchronous output is asserted when non-idle condition is detected at the twisted-pair interface and de-asserted when idle or a valid end of stream delimiter is detected. In 10/100Base-T half duplex, CRS is also asserted during transmitted. CRS is asynchronous to TXC, and RXC.
118/88	-	P0COL/P1COL	O ( $I_{PD}$ )	MII Collision. This asynchronous output is asserted when a collision is detected in half-duplex modes. In full duplex mode, this signal is forced low. COL is asynchronous to TXC and RXC.
115, 69	-	P0RXER P1RXER	O ( $I_{PD}$ )	GMII/MII Receive Error. When RXER and RXDV are both asserted, the symbol indicates an error symbol is detected on the cable. Since the RTL8212F/RTL8212G does not support 1000Base-T half-duplex mode, carrier-extension receive symbol (RXER is asserted with RXDV deasserted) is not valid. RXER is synchronous to RXC.



Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
105/106	-	P0RXD7/P0RXD6	O (I <sub>PD</sub> )	GMII/MII Receive Data Bus. The width of this synchronous input bus varies with the speed mode.
107/108		P0RXD5/P0RXD4		1000M: RXD[7:0] are used
110/111		P0RXD3/P0RXD2		10/100M: RXD[3:0] are used; RXD[7:4] are ignored
112/113		P0RXD1/P0RXD0		RXD[7:0] is synchronous to RXC.
70/71		P1RXD7/P1RXD6		
73/74		P1RXD5/P1RXD4		
79/82		P1RXD3/P1RXD2		
83/84		P1RXD1/P1RXD0		

## 6.5. SGMII Interface Pins

Table 7. SGMII Interface Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
66, 44	60, 41	SGTXP[1:0]	AI	SGMII Transmit Pair. 1.25GHz differential serial input.
65, 45	59, 42	SGTXN[1:0]		The differential pair has an internal 100ohm termination resistor.
62, 49	56, 46	SGRXP[1:0]	AO	SGMII Receive Pair. 1.25GHz differential serial output.
61, 50	55, 47	SGRXN[1:0]		The differential pair has an internal 100ohm termination resistor.
57, 54	52, 50	SGRXCKP[1:0]	AO	SGMII 625MHz Transmit Clock Pair.
58, 53	53, 49	SGRXCKN[1:0]		

## 6.6. LED Interface Pins

Table 8. LED Interface Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
150	118	LEDCK	O (I <sub>PU</sub> )	Serial LED Clock. Reference output clock for serial LED interface. The frequency of the serial LED clock is 12.5MHz. Data is latched on the rising edge of LEDCK.
149	117	LEDDA	O (I <sub>PU</sub> )	Serial LED Data Output. The serial data bit of the link information presents on the rising edge of LEDCK.
150, 84, 85, 87, 149, 88, 90, 93	118, 70, 71, 72, 117, 73, 75, 77	LED[7:0]	O (I <sub>PD</sub> )	Parallel LED 7~0.



## 6.7. Serial Management Interface Pins

**Table 9. Serial Management Interface Pins**

<b>Pin No.</b>		<b>Pin Name</b>	<b>Type</b>	<b>Description</b>
<b>LQFP164</b>	<b>LQFP128</b>			
146	116	MDC_0	I (I <sub>P</sub> U)	Management Data Clock for SMI0. This pin is the clock reference for the serial management interface driven by an external management device. When dual SMI is disabled (ENDUALSMI = 0), MDC_0/MDIO_0 is used to access the two ports. When dual SMI is enabled (ENDUALSMI = 1), MDC_0/MDIO_0 is used to access the 1 <sup>st</sup> Port (Port0).
145	115	MDIO_0	I/O (I <sub>P</sub> U)	Management Data IO for SMI0. MDIO transfers the serial data stream in and out of the device synchronous to the rising edge of MDC.
138	111	MDC_1	I (I <sub>P</sub> D)	Management Data Clock for SMI1. This pin is the clock reference for the serial management interface driven by an external management device. MDC_1/MDIO_1 is available only when dual SMI is enabled (ENDUALSMI = 1). It is used to access the 2 <sup>nd</sup> Port.
137	110	MDIO_1	I/O (I <sub>P</sub> D)	Management Data IO for SMI1. MDIO transfers the serial data stream in and out of the device synchronous to the rising edge of MDC.

## 6.8. Miscellaneous Pins

**Table 10. Miscellaneous Pins**

<b>Pin No.</b>		<b>Pin Name</b>	<b>Type</b>	<b>Description</b>
<b>LQFP164</b>	<b>LQFP128</b>			
159	124	XTAL1	AI	25MHz Crystal Clock Input. 25MHz ±50ppm tolerance crystal reference or oscillator input. When a crystal is used, a loading capacitor should be connected between this pin and ground. When used as oscillator input, this pin is connected with an oscillator or driven by an external 25MHz clock from another device and the XTAL2 pin should be left floating. The maximum XTAL1 input voltage is 3.3V.
160	125	XTAL2	AO	25MHz Crystal Clock Output. When a crystal is used, a loading capacitor should be connected between this pin and ground.
153	120	RESET#	I	Chip Reset. An active low signal. To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
4	4	MDI_REF	AO	MDI Bias Resistor. Used to adjust the reference current for the gigabit PHY. A 2.49KΩ±1% resistor should be connected between this pin and ground.



Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
3	3	ATEST	AO	Analog Test Pin. Reserved for internal analog debugging. It should be connected to ground through a 1KΩ resistor. If debug is not important and there are board space constrains, this pin can be left floating.
1, 2	1, 2	NC	-	These pins should be left floating.
156	122	RSVD	-	This pin should be left floating.
47	44	RSVD	-	This pin should be pulled low with a 1KΩ resistor.

## 6.9. Configuration Pins

Table 11. Configuration Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
70, 71	62, 63	PHYMODE[1:0]	I (I <sub>PD</sub> )	PHY Interface Mode Selection. These are strapping pins (i.e., this pin's state is latched upon reset* for configuration function use. After reset, this pin acts as an output pin for other functions, or as a non-used pin). 00: GMII/RGMII mode (default) 01: Reserved 10: SGMII mode 11: Reserved <i>Note: 'Upon Reset' is defined as a short time after the rising edge of the hardware reset signal. 'After Reset' is defined as the time after the specified 'Upon Reset' time.</i>
74 69	-	P0IF P1IF	I (I <sub>PD</sub> )	Interface Mode Select. These are strapping pins. GMII/MII and RGMII mode selection for Port0 and Port1 respectively. These pins are irrelevant if the PHYMODE[1:0] is not '00'. 0: RGMII (default) 1: GMII/MII <i>Note: This is only available for the RTL8212G.</i>
82	68	RSVD	I (I <sub>PD</sub> )	Reserved for Internal Use. This is a strapping pin. 0: Disable internal use mode (default) 1: Enable internal use mode This pin is recommended to be '0' in usual usage.
83	69	FIBUTP	I (I <sub>PD</sub> )	Fiber and Copper (UTP) Port Selection. When the strapping value of Pin 112 on the 164-pin package, or Pin 94 on the 128-pin package is '0', this pin is used to determine which media, fiber or copper, is selected for both Port0 and Port1. When the strapping value of the Pin112 on 164-pin package or Pin94 on 128-pin package is '1', this pin is irrelevant. 0: Copper (default) 1: Fiber If SGMII is used as the PHY interface, copper is selected and this pin is irrelevant.


**RTL8212F & RTL8212G  
Datasheet**

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
84	70	ENGREEN	I (I <sub>PD</sub> )	Enable Green Feature. It is a strapping pin. 0: Disable green feature (default) 1: Enable green feature
85	71	RSVD	I (I <sub>PD</sub> )	Reserved for Internal Function. It is a strapping pin. It is recommended to be '0'.
88, 79	73, 66	P1PHYADR[1:0]	I (I <sub>PD</sub> )	PHY Address for Port1. These are strapping pins. P1PHYADR[1:0] sets the least two bits of the Port1 5-bit PHY address upon reset.
97	81	LEDSPSEL	I (I <sub>PD</sub> )	LED Serial and Parallel Mode Selection. It is a strapping pin. This pin can be used when PHYMODE[1:0] is not '00'. If the PHYMODE[1:0]='00', the serial LED is selected and this pin is irrelevant. 0: Serial LED (default) 1: Parallel LED
102 100	86 84	TXDLY0 TXDLY1	I (I <sub>PD</sub> )	GTXC Clock Delay Select. These are strapping pins. Enable GTXC input delay in RGMII mode for port0 and port1 respectively. 0: No delay (default) 1: Add delay to GTXC
103 101	87 85	RXDLY0 RXDLY1	I (I <sub>PD</sub> )	RXC Clock Delay Select. These are strapping pins. Enable RXC output delay in RGMII mode for port0 and port1 respectively. 0: No delay (default) 1: Add delay to RXC
105, 106, 110	89, 90, 92	PHYADR[4:2]	I (I <sub>PD</sub> )	PHY Address for Port0 and Port1. These are strapping pins. PHYADR[4:2] sets the bit 4, bit3, bit2 of the 5-bit PHY address upon reset for both of the two ports.
108	-	DISPBLK	I (I <sub>PD</sub> )	Disable Power on Blinking. 0: Enable LED power on blinking. After hardware reset, LED will blink for diagnoses (default) 1: Disable LED power on blinking
111	93	ENDUALSMI	I (I <sub>PD</sub> )	Enable Dual SMI (MDC/Mdio). This is a strapping pin. 0: Disable dual SMI mode (default). Only MDC_0/Mdio_0 can be used. 1: Enable dual SMI mode. Two sets of SMI, MDC_0/Mdio_0 and MDC_1/Mdio_1, can be used to access each PHY correspondingly. In GMII mode, dual SMI can not be used due to the sharing pins of the MDC_1/Mdio_1 and GMII and this pin should be '0'.
112	94	RSVD	I (I <sub>PD</sub> )	Reserved for Internal Function. 0: Disable the internal function (default) 1: Enable the internal function If SGMII is used as the MAC interface, this pin is irrelevant.
113, 116	95, 97	P0PHYADR[1:0]	I (I <sub>PD</sub> )	PHY Address. These are strapping pins. PHYADR[1:0] sets the least two bits of the Port0 5-bit PHY address upon reset.





Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
118	99	ENCPTMODE	I (I <sub>PD</sub> )	Enable Backward Compatible Mode. It is a strapping pin. 0: Disable backward compatible mode (default) 1: Enable backward compatible mode. This mode supports the MACs which do not support fibers when fiber media is selected.
121 90	101 75	P0MODE P1MODE	I (I <sub>PD</sub> )	Auto-Negotiation Mode Configuration. These are strapping pins. P0/P1MODE preset each Port's MASTER/SLAVE preference for 1000Base-T. 0: Prefer MASTER (default) 1: Prefer SLAVE
150, 149	118, 117	LEDMODE[1:0]	I (I <sub>PU</sub> )	LED Mode Select. These are strapping pins. These pins are used to configure LED operation mode. There are four LED display modes. 00: Mode 3 01: Mode 2 10: Mode1 11: Mode0 (default)

Note: 'Upon Reset' is defined as a short time after the rising edge of the hardware reset signal. 'After Reset' is defined as the time after the specified 'Upon Reset' time.

## 6.10. Power and Ground Pins

Table 12. Power and GND Pins

Pin No.		Pin Name	Type	Description
LQFP164	LQFP128			
6, 15, 24, 32, 40, 41, 161, 163, 164	6, 14, 23, 31, 38, 126, 128	AVDD33	AP	Analog Power 3.3V.
76, 89, 99, 109, 119, 133, 134	65, 74, 83, 91, 100, 109	DVDD	P	Digital Power 3.3V/2.5V for Digital IO. The 2.5V power may be used in 2.5V RGMII applications.
7, 14, 22, 23, 31, 39	7, 13, 21, 22, 30, 37	AVDD12	AP	Analog Power 1.2V.
43, 48, 55, 56, 63, 67	40, 45, 51, 57, 61	SVDD12	SP	Analog Power 1.2V.
72, 80, 81, 94, 104, 114, 125, 126, 143, 144	64, 67, 78, 88, 96, 104, 114	VDD12	P	Digital Core Power 1.2V.
154, 155	121	AVDDPLL	AP	PLL Power 1.2V.
151, 152	119	VDDIO	P	Digital Power 3.3V/2.5V for Digital IO.
5, 10, 11, 18, 19, 27, 28, 35, 36, 162	5, 10, 17, 18, 26, 27, 34, 127	AGND	AG	Analog Ground.
157, 158	123	AVSSPLL	AG	PLL Ground.
46, 51, 52, 59, 60, 64	58, 54, 48, 43	SGND	SG	SerDes Ground.
68, 75, 77, 78, 86, 120, 127, 128, 135, 136, 139, 140, 147, 148, E-PAD	E-PAD	DGND	G	Digital Ground.



## 7. Functional Description

### 7.1. Operation Mode

#### 7.1.1. Copper to RGMII/GMII/MII

When PHYMODE[1:0]=00 and FIBUTP=0 (refer to Table 11, page 15), the RTL8212F/RTL8212G will operate in copper to RGMII mode (RTL8212F) or RGMII/GMII/MII mode (RTL8212G). In this mode, RGMII/GMII/MII is used as the MAC interface and communicates with the copper media interface – the Gigabit Ethernet transceiver. SerDes is powered down in this mode.

For the RTL8212G, the value of P0IF/P1IF (refer to Table 11, page 15) will determine whether the MAC interface is RGMII or GMII/MII.

*Note: The RTL8212F will only operate in RGMII mode.*

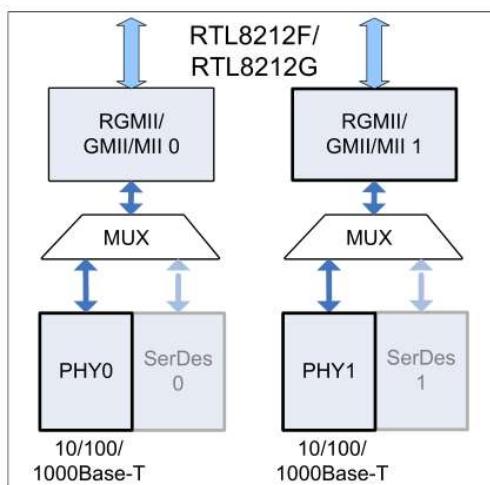


Figure 6. Copper to RGMII/GMII/MII Mode

#### 7.1.2. Fiber to RGMII/GMII/MII

When Pin PHYMODE[1:0]=00 and Pin FIBUTP=1 (refer to Table 11, page 15), the RTL8212F/RTL8212G will operate in Fiber to RGMII mode (RTL8212F) or RGMII/GMII/MII mode (RTL8212G). In this mode, RGMII/GMII/MII is used as the MAC interface and the SerDes connecting with fiber transceiver is used as the media interface. The SerDes in this mode supports 1000Base-X and 100Base-FX. 1000Base-X is selected by default and 100Base-FX should be selected via register setting (SerDes page register 0=0x2100, refer to Table 28, page 37).

The Gigabit Ethernet transceiver (PHY0/PHY1) is powered down in this mode. For the RTL8212G, the value of P0IF/P1IF (refer to Table 11, page 15) will determine whether the MAC interface is RGMII or GMII/MII.

*Note: The RTL8212F will only operate in RGMII mode.*

With support for copper and fiber media to the MAC interface transmission, the RTL8212F/RTL8212G meets the requirement of combo link applications.

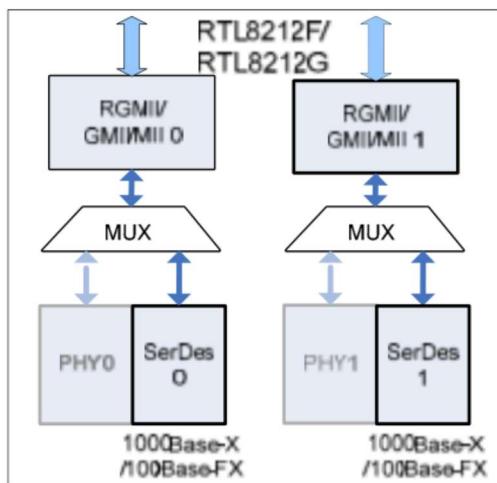


Figure 7. Fiber to RGMII/GMII/MII

### 7.1.3. Copper to SGMII

When Pin PHYMODE[1:0]=10 (refer to Table 11, page 15), the RTL8212F/RTL8212G is in the copper to SGMII mode. In this mode, the SerDes work as SGMII and can be connected with MACs that support SGMII. The SerDes connects with the Gigabit Ethernet transceivers internally in this mode. RGMII/GMII/MII is not used.

Both parallel and serial mode LEDs are supported in this mode.

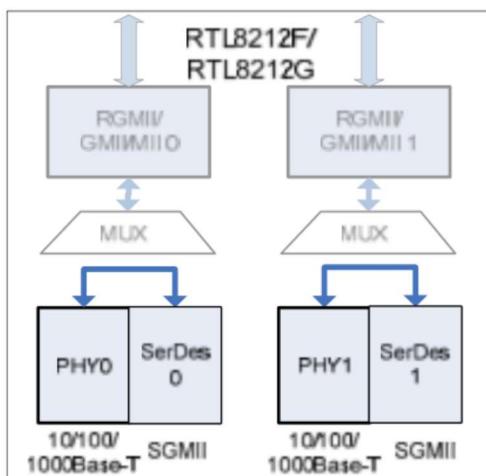


Figure 8. Copper to SGMII



## 7.2. Integrated Gigabit PHY

### 7.2.1. MDI Interface

The RTL8212F/RTL8212G embeds two Gigabit Ethernet PHYs in one chip. Each PHY uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs: A, B, C, and D (refer to Table 3, page 10). Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors to reduce BOM cost and PCB complexity.

For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used. Table 13 shows the mapping between the pairs and the RJ-45 signals.

**Table 13. Mapping of Twisted-Pair Outputs to RJ-45 Connectors**

Pairs	RJ-45 Pin
A	1 and 2
B	3 and 6
C	4 and 5
D	7 and 8

### 7.2.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

### 7.2.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz.

### 7.2.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.



## 7.2.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

## 7.2.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

## 7.2.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

## 7.2.8. Auto-Negotiation Function

The RTL8212F/RTL8212G obtains the states of duplex, speed, and flow control ability for each port through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8212F/RTL8212G advertises full capabilities (1000Full, 100Full/Half, 10Full/Half) together with flow control ability. The MASTER/SLAVE mode preference, which is used in 1000Base-T auto-negotiation, can be configured by strapping pins (P0MODE/P1MODE, refer to Table 11, page 15). When the P0MODE (P1MODE) is ‘0’, the Port0 (Port1) MASTER/SLAVE Configuration Value will be MASTER and the Port Type will be Multi-port device (refer to Table 40, page 44). Otherwise, the MASTER/SLAVE Configuration Value will be SLAVE and the Port Type will be Single-port device.

## 7.2.9. PHY Register

Each Gigabit PHY within the RTL8212F/RTL8212G contains a set of PHY registers in compliance with the IEEE 802.3 specifications. All of the PHY registers can be accessed through the MDC and MDIO signals (refer to section 7.5.4 Serial Management Interface (SMI), page 29).

## 7.2.10. Crossover Detection and Auto Correction

The RTL8212F/RTL8212G automatically determines whether or not it needs to crossover between pairs (see Table 14, page 22) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8212F/RTL8212G automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The RTL8212F/RTL8212G is set to MDI Crossover by default. The pin mapping in MDI and MDI Crossover mode is given in Table 14, page 22.

**Table 14. Media Dependent Interface Pin Mapping**

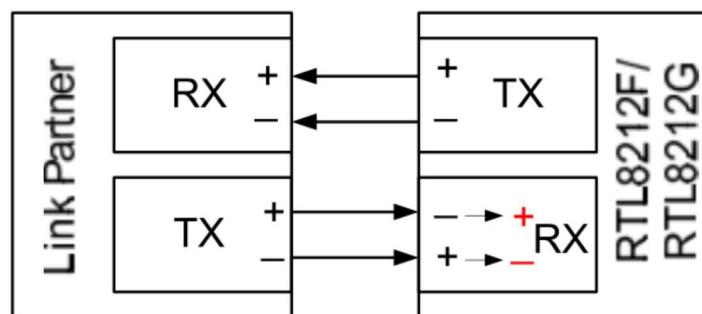
Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

### 7.2.11. Polarity Correction

The RTL8212F/RTL8212G automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-Tx mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

**Figure 9. Conceptual Example of Polarity Correction**

### 7.2.12. Green Ethernet

#### 7.2.12.1 Link-On and Cable Length Power Saving

The RTL8212F/RTL8212G provides link-on and dynamic detection of the copper cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

#### 7.2.12.2 Link-Down Power Saving

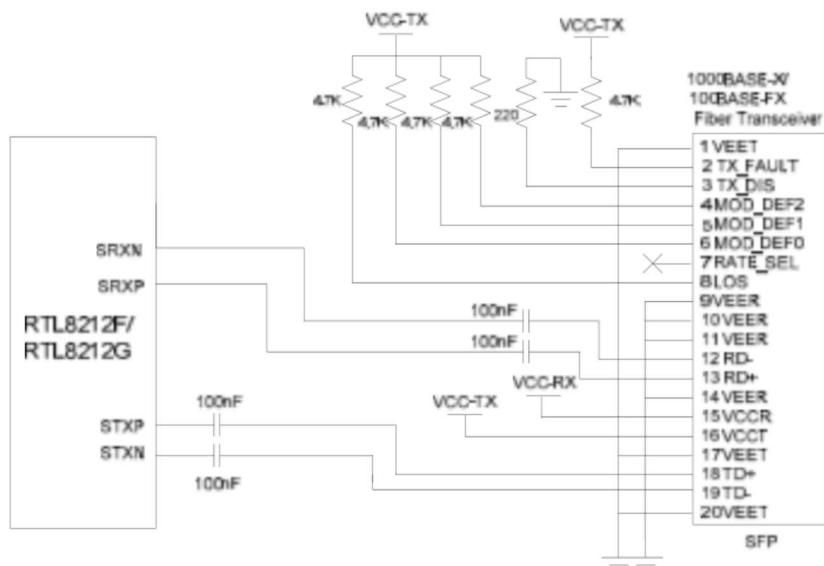
The RTL8212F/RTL8212G implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.



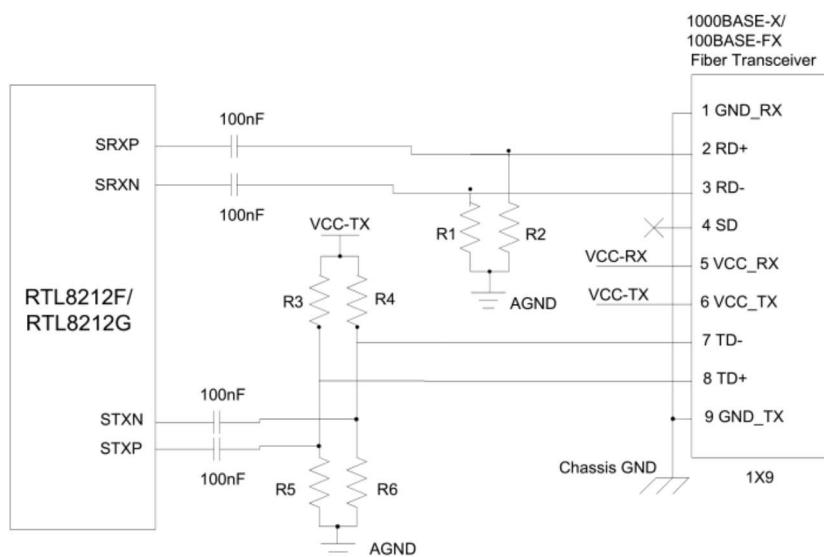
### 7.3. Integrated SerDes

#### 7.3.1. 1000Base-X Mode

The SerDes in the RTL8212F/RTL8212G supports 1000Base-X/100Base-FX when fiber media interface is used. The SerDes transmit and receive serial data differentially at 1.25G/125M baud, which complies with IEEE 802.3, and can directly connect with SFP (Small Form-Factor) or 1X9 fiber transceivers (Refer to Figure 10 and Figure 11).



**Figure 10. SerDes with SFP Fiber Transceiver**



**Figure 11. SerDes with 1X9 Fiber Transceiver**



The resistance value in Figure 11, page 23 varies according to the 1X9 fiber transceiver's supply power voltage. The typical supply power voltage and the resistance selection are shown in Table 15.

**Table 15. Resistance Selection vs. 1x9 Fiber Transceiver VCC**

Resistance	VCC_TX=VCC_RX=5V	VCC_TX=VCC_RX=3.3V
R1, R2	270ohm	200ohm
R3, R4	68ohm	82ohm
R5, R6	180ohm	130ohm

The PCS and PMA layers specified in IEEE 802.3, Clauses 36 and 37 are implemented in the RTL8212F/RTL8212G SerDes. The PCS provides services of encoding of GMII data octets to ten-bit code-groups (8B/10B), and decoding of GMII data octets from ten-bit code-groups (8B/10B) for communication with the underlying PMA. The PCS also manages the Auto-Negotiation process. The PMA serializes (or deserializes) code-groups for transmission (or reception) on the serial differential TX (or RX) pins and uses integrated CDR circuit to recover clock from the 8B/10B-coded RX data.

The RTL8212F/RTL8212G provides a built-in Signal Detect block that can generate the SD (Signal Detect) signal by monitoring RX+/- signals from the fiber transceiver (SD signals from the fiber transceiver are not required). This is useful in reducing pin count and PCB layout effort.

The RTL8212F/RTL8212G supports 1000Base-X auto-negotiation as described in IEEE-802.3, Clause 37. The duplex and Pause abilities are advertised, but speed ability is not. The IEEE-802.3 specified '1000Base-X Auto-Negotiation Advertisement Register' and '1000Base-X Auto-Negotiation Link Partner Ability Register' are both implemented.

The RTL8212F/RTL8212G also supports an enhanced auto-negotiation mode for 1000Base-X. With this enhanced auto-negotiation ability, the RTL8212F/RTL8212G will establish a link even when the link partner has no auto-negotiation ability. The enhanced auto-negotiation mode can be selected via register setting.

### 7.3.2. 100Base-FX Mode

The SerDes of the RTL8212F/RTL8212G can work in 100Base-FX mode (described in IEEE 802.3, Clause 24) via register configuration.

In 100Base-FX transmission, 4-bit TX data are encoded to 5-bit codes (4B/5B) and serialized into a data stream that is driven out as NRZI signals to the fiber transceiver in differential form. In reception, Signals received from the fiber transceiver are passed to a clock recovery circuit for clock recovery and then deserialized and decoded into MII data nibbles.

The RTL8212F/RTL8212G provides a built-in Signal Detect block that can generate the SD (Signal Detect) signal by monitoring RX+/- signals from the fiber transceiver (SD signals from the fiber transceiver are not required). This is useful in reducing pin count and PCB layout effort.

The RTL8212F/RTL8212G provides a FEFI (Far-End-Fault-Indication) function for the 100Base-FX SerDes. When the FEFI function is enabled, the RTL8212F/RTL8212G will transmit a special FEFI pattern when a physical error condition is sensed on the receive channel. The FEFI is an in-band signaling that is composed of 84 consecutive 1's followed by one 0. PHY Reg.1.4 (Remote Fault) indicates whether a FEFI has been detected. When the RTL8212F/RTL8212G has detected 3 consecutive FEFI's, Reg.1.4



will be set. After being set, Reg.1.4 will always be latched high until it is read. The FEFI mechanism is used in 100Base-FX only and can be disabled by register setting.

In 100Base-FX mode, the two SerDes can also directly connect with SFP or 1X9 fiber transceivers (Refer to Figure 10, page 23 and Figure 11, page 23). Half duplex is not supported in the RTL8212F/RTL8212G 100Base-FX mode.

### 7.3.3. SGMII Mode

When Pin PHYMODE[1:0]=10, the SerDes are used as SGMII interface circuits. This serial interface can carry a full duplex 10/100/1000M Ethernet data stream from a copper port, and recover clock from the data rather than use the dedicated clock. This feature helps to reduce pin count, PCB layout effort, and EMI. The SGMII interface runs at 1.25Gbps in 10M/100M/1000Mbps modes. The encoding/decoding and Serialization/De-serialization mechanism of SGMII is identical to that of 1000Base-X. As a 1.25Gbps data rate is excessive for interfaces operating at 10M/100Mbps. In these conditions, each code-word of data is repeated 10 times for 100Mbps, and 100 times for 10Mbps, through a rate adaptation block.

The auto-negotiation mechanism of SGMII mode is similar to that of 1000Base-X mode, except that the link timer is reduced to about 1.6ms and the configuration code-word is changed to reflect the copper ports link, duplex, and speed. Whenever the copper port link changes, SGMII auto-negotiation is restarted with the current copper port link information.

The connection of the RTL8212F/RTL8212G and MAC though the SGMII interface is described in section 7.5.3, page 29.

## 7.4. Reset

In a power-on reset or pin reset (RESET# pin pulled low for at least 10ms), an internal reset pulse is generated and the RTL8212F/RTL8212G will start the reset initialization procedures for the whole system. It will take about 50ms to complete the initialization procedures after the rising edge of the hardware reset signal (see Figure 12).

The hardware reset signal is inactive only when all of the following conditions are met:

1. AVDD33 and VDD12 power is ready
2. RESET# pin is on logic high

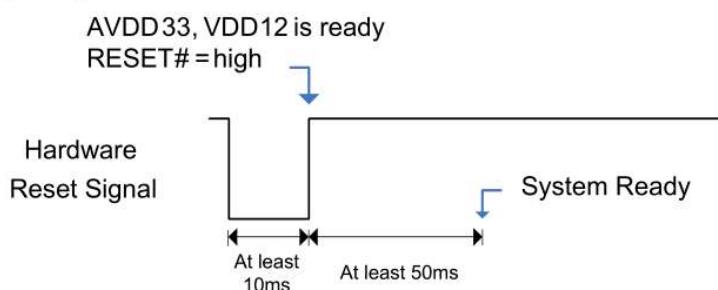


Figure 12. Reset



## 7.5. MAC Interface

The RTL8212F/RTL8212G MAC interface supports SGMII/RGMII (RTL8212F) and SGMII/RGMII/GMII/MII (RTL8212G). The MAC interface selection is set by P0IF, P1IF, and PHYMODE[1:0] pins (refer to Table 11, page 15). Table 16 shows the configuration and data rates supported for each interface.

**Table 16. Configuration and Data Rates Supported for Each Interface**

PHYMODE[1:0]	P0IF/P1IF	MAC Interface	10Base-T	100Base-TX	1000Base-T	1000Base-X	100Base-FX
00	1	GMII	-	-	√	√	-
00	1	MII	√	√	-	-	√
00	0	RGMII	√	√	√	√	√
10	Do not Care	SGMII	√	√	√	-	-

### 7.5.1. GMII/MII (RTL8212G Only)

Table 17 indicates the signal mapping of the RTL8212G to the Gigabit Media Independent Interface (GMII/MII).

MII signaling to support 100Base-TX/100Base-FX, and 10Base-T modes is implemented by sharing pins of the GMII interface. The unused pins for MII or GMII in Table 17 will not be driven and can be left floating.

GMII mode does not support carrier extension and packet concatenation in both the transmit and the receive directions, due to not having a TXER pin. The RTL8212G will auto select GMII or MII according to the speed (GMII for 1000M, MII for 10/100M) of the copper or fiber port. The timing characteristics for GMII/MII are described in section 9.4.4 and 9.4.5, page 55 and 56.

*Note: GMII/MII is only available for the RTL8212G.*

**Table 17. GMII/MII (RTL8212G Only)**

RTL8212G Pins	MII	GMII
GTXC	-	GTX_CLK
TXC	TXC	-
TXEN	TX_EN	TX_EN
TXD[7:4]	-	TXD[7:4]
TXD[3:0]	TXD[3:0]	TXD[3:0]
RXC	RX_CLK	RX_CLK
RXER	RX_ER	RX_ER
RXDV	RX_DV	RX_DV
RXD[7:4]	-	RXD[7:4]
RXD[3:0]	RXD[3:0]	RXD[3:0]
CRS	CRS	-
COL	COL	-

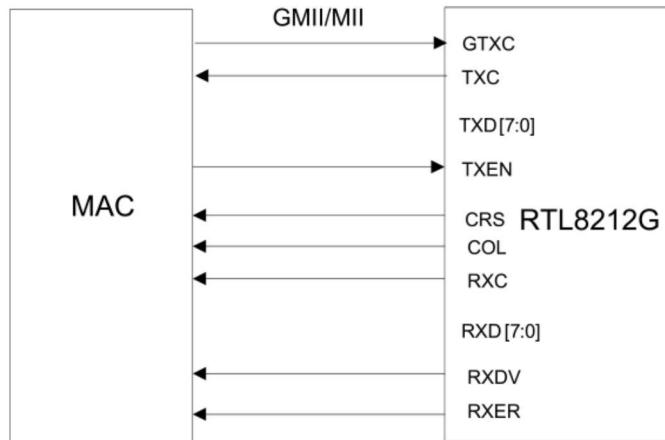


Figure 13. GMII/MII Signal Diagram

### 7.5.2. RGMII

The Reduced Gigabit Media Independent Interface (RGMII) needs less pin count than GMII. It supports 1000M, 100M, and 10M speeds. The RTL8212F/RTL8212G supports the RGMII Rev. 2.0 specification. This interface reduces the interconnection between the MAC and the PHY to 12 pins. In order to accomplish this, the data paths and all associated control signals are reduced, control signals are multiplexed together, and both edges of the clock are used.

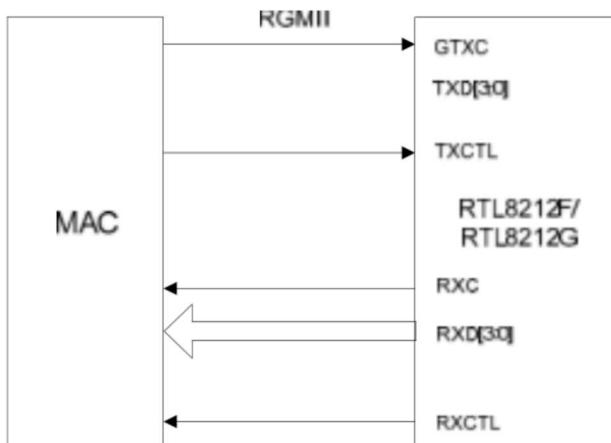


Figure 14. RGMII Signal Diagram

For Gigabit operation, the transmit and receive clocks will operate at 125MHz, and for 10/100M operation, the clocks will operate at 2.5MHz or 25MHz respectively. In all three speeds, transmit control is presented on both clock edges of GTXC and receive control (RX\_CTL) is presented on both clock edges of RXC.



## RTL8212F & RTL8212G Datasheet

To reduce power of this interface, TX\_ER and RX\_ER of GMII are encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. The TX\_ERR signal appears on the falling edge of GTXC and RX\_ERR appears on the falling edge of RXC.

$$\text{TX\_ERR} \leftarrow \text{GMII\_TX\_ER} (\text{XOR}) \text{ GMII\_TX\_EN}$$

$$\text{RX\_ERR} \leftarrow \text{GMII\_RX\_ER} (\text{XOR}) \text{ GMII\_RX\_DV}$$

As the RTL8212F/RTL8212G does not support Half-Duplex in 1000Base-T, and the GMII\_TX\_ER signal is always tied to logic low, carrier extend and transmit errors never appear at the transmitting and receiving end. The following tables show the available encoding of the RX\_CTL and TX\_CTL.

**Table 18. TX\_ER and TX\_EN Encoding**

TX_CTL	GMII_TX_EN	GMII_TX_ER	Description
0, 0	0	0	Normal Inter-Frame
1, 1	1	0	Normal Data Transmission

**Table 19. RX\_ER and RX\_DV Encoding**

RX_CTL	GMII_RX_DV	GMII_RX_ER	Description
0, 0	0	0	Normal Inter-Frame
0, 1	0	1	Carrier Sense
1, 1	1	0	Normal Data Reception
1, 0	1	1	Data Reception Error

*Note 1: The MAC is designed to acquire the link status, speed, and duplex mode of the PHY via MDC/MDIO polling, so the RTL8212F/RTL8212G does not implement specific code onto RXD[3:0] to inform the MAC of the PHY status during normal inter-frame.*

*Note 2: In addition to the encoding of RX\_DV and RX\_ER as shown in the above table, a value of 'FF' also exists on the RXD[7:0] simultaneously when Carrier Sensing occurs.*

The RTL8212F/RTL8212G supports four timing modes of operation. The per-port strapping pins, TXDLY and RXDLY, can be used to adjust the delays of data with respect to clock edges.

**Table 20. RGMII Timing Modes**

Mode	TXDLY	RXDLY	PHY Input GTXC vs. Data	PHY Output RXC vs. Data
Mode 0	0	0	No Delay	No Delay
Mode 1	0	1	No Delay	Add Delay to RXC
Mode 2	1	0	Add Delay to GTXC	No Delay
Mode 3	1	1	Add Delay to GTXC	Add Delay to RXC

For RGMII pin descriptions and timing information, see Table 5, page 11, and section 9.4.3, page 53.

### 7.5.3. SGMII

The RTL8212F/RTL8212G SGMII supplies a differential 625MHz clock via the SGRXCKP/N pins which synchronize the 1.25G baud data on SGRXP/N pins. The RTL8212F/RTL8212G does not need the input clock since it provides clock recovery on the SGMII input data. Figure 15 shows the signal diagram of the SGMII. All SGMII pins of the RTL8212F/RTL8212G include on-chip 100ohm differential termination resistors. They connect with the MAC via AC coupling. The typical value of the coupling capacitor is 100nF.

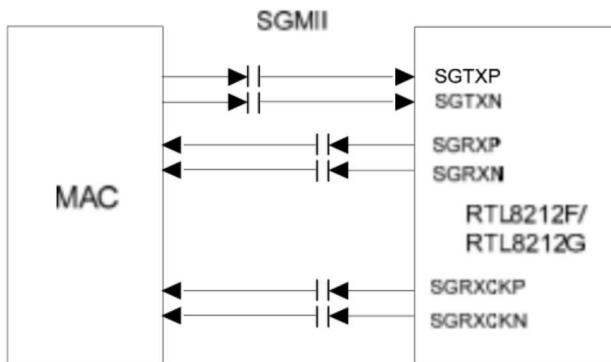


Figure 15. SGMII Signal Diagram

### 7.5.4. Serial Management Interface (SMI)

The SMI is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control and acquire the state of the PHY registers. MDIO is a bi-directional connection used to write data to, or read data from the RTL8212F/RTL8212G. Data transferred to and from the MDIO pins is synchronized with the MDC clock. The clock can run from DC to 2.5MHz.

The RTL8212F/RTL8212G register implementation is in compliance with the IEEE-802.3 standard registers defined for 1000Base-T and 1000Base-X/100Base-FX (refer to section 8 Register Descriptions, page 36). In addition, the RTL8212F/RTL8212G defines ‘Page Selection’ in register 31(refer to Table 43, page 45) to select which kind of registers is shown in registers 0~15 (the registers for 1000Base-T or the registers for 1000Base-X/100Base-FX), as some 1000Base-X register definitions are different from those of 1000Base-T.

When the media is selected, the ‘Page Selection’ register will automatically switch to the corresponding standard registers. The standard registers for 100Base-FX and 1000Base-X are also different.

- Registers 0~15 are for 1000Base-X if 1000Base-X is selected (SerDes register 0=0x1140, refer to Table 28, page 37).
- Registers 0~15 are for 100Base-FX if 100Base-FX is selected (SerDes register 0=0x2100, refer to Table 28, page 37).

The MDIO frame starts with a 32-bit preamble, which is required by the RTL8212F/RTL8212G. The rest of the frame includes a start-of-frame marker, an op-code, a 10-bit address field, and a 16-bit data field. The address field is divided into two 5-bit segments. The first segment identifies the PHY address and the Integrated Dual 10/100/1000Base-T and 1000Base-X/100Base-FX Gigabit Ethernet Transceiver

second identifies the register being accessed (refer to Table 21, page 30). The 5-bits PHY address are determined by the hardware strapping values during power up. The most significant 3 bits of the two port's PHY address is determined by the same 3 pins, pin PHYADR[4:2]. The least significant 2 bits of the two ports' PHY address can be configured independently. Pins P0PHYADR[1:0] are used for port 0 configuration and Pins P1PHYADR[1:0] are used for port 1 configuration (refer to Table 11, page 15). When dual SMIs are not used, the identical PHY address cannot be configured for the two ports.

**Table 21. SMI Read/Write Cycles**

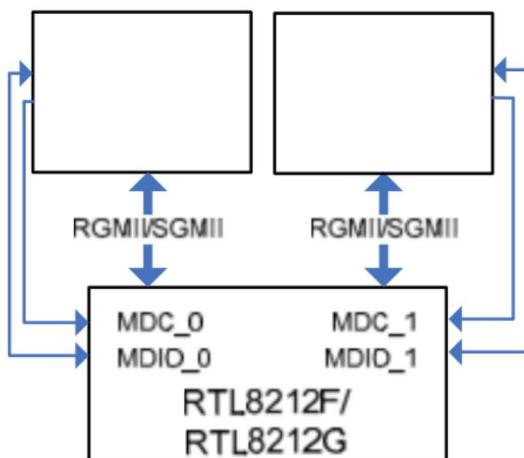
	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1.....1	01	10	A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	Z0	D <sub>15</sub> .....D <sub>0</sub>	Z*
Write	1.....1	01	01	A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	10	D <sub>15</sub> .....D <sub>0</sub>	Z*

Note: Z\*: High-impedance.

The SMI timing description is shown in section 9.4.5 SMI Timing, page 56.

The RTL8212F/RTL8212G can support two MDC/Mdio interfaces by setting strapping pin ENDUALSMI (refer to Table 11, page 15) to high. The dual SMIs mean the two ports can be treated as totally independent ports that can be controlled by two different master devices. In Dual SMI interface mode, the MDIO\_0 and MDC\_0 pins are used for Port 0, and the MDIO\_1 and MDC\_1 pins are used for Port 1. The PHY address of the two ports can be the same. The registers of the two ports can be accessed simultaneously.

In GMII mode, the dual SMIs cannot be used for sharing pins.



**Figure 16. Dual SMI Application**



## 7.6. Backward Compatible Mode

Some older switch MAC controllers were designed to work with copper media only and are not able to connect with 1000Base-X fiber media because they have no ability to access the 1000Base-X transceiver registers.

The RTL8212F/RTL8212G provides the strapping pin ENCPTMODE (refer to Table 11, page 15) to enable backward compatible ability supporting these old MAC controllers to employ the 1000Base-X fiber media. When enabling the backward compatible ability, the RTL8212F/RTL8212G will rearrange the link information registers (in register 0~15) of 1000Base-X to comply with the 1000Base-T, which makes the old MAC controller access 1000Base-X registers properly.

## 7.7. LED Function

### 7.7.1. Status Indication

The RTL8212F/RTL8212G provides the ability to show various link statuses of PHY0, PHY1, SD0 and SD1 (PHY0 and PHY1 indicate the two gigabit Ethernet transceivers; SD0 and SD1 indicate the two SerDes). Both parallel mode and serial mode LED indicators are implemented. The RTL8212F/RTL8212G supports 8 LED indicators. The default LED settings are shown in Table 22. They are determined by LEDMODE[1:0] and LEDSPSEL pins (Refer to Table 11, page 15).

**Table 22. LED Default Settings**

Mode	LED0	LED1	LED2	LED3	LED4	LED5	LED6	LED7
Serial Mode 0	PHY0 Spd1000Link/ Act	PHY0 Spd100/ 10Link/Act	PHY0 Dup/Col	SD0 Link/Act	PHY1 Spd1000Link/ Act	PHY1 Spd100/ 10Link/Act	PHY1 Dup/Col	SD1 Link/Act
Serial Mode 1	PHY0 Link/Act	PHY0 Spd100	PHY0 Spd10	PHY 0 Dup/Col	PHY1 Link/Act	PHY1 Spd100	PHY1 Spd10	PHY 1 Dup/Col
Serial Mode 2	PHY0 Spd1000	PHY0 Spd100	PHY0 Link/Act	PHY0 Dup	SD1 Link/Act	Reserved	Reserved	Reserved
Serial Mode 3	PHY0 Link/RxAct	PHY0 Link/TxAct	SD0 Link/RxAct	SD0 Link/TxAct	PHY1 Link/RxAct	PHY1 Link/TxAct	SD1 Link/RxAct	SD1 Link/TxAct
Parallel Mode 0	PHY0 Spd1000Link/ Act	PHY0 Spd100Link/Act	PHY0 Spd10Link/Act	PHY0 Dup/Col	PHY1 Spd1000Link/ Act	PHY1 Spd100Link/Act	PHY1 Spd10Link/Act	PHY1 Dup/Col
Parallel Mode 1	PHY0 Spd1000Link/ Act	PHY0 Spd100Link/Act	PHY0 Dup/Col	SD0 Link/Act	PHY1 Spd1000Link/ Act	PHY1 Spd100Link/Act	PHY1 Dup/Col	SD1 Link/Act
Parallel Mode 2	PHY0 Spd1000	PHY0 Spd100	PHY0 Link/Act	PHY0 Dup	SD1 Link/Act	Reserved	Reserved	Reserved
Parallel Mode 3	SD1 Link/Act	Reserved	PHY1 Spd1000Link/Act	PHY1 Spd100Link/ Act	PHY1 Dup	PHY0 Spd1000Link/Act	PHY0 Spd100Link/Act	PHY0 Dup

Information or status that each of the LEDs may indicate is defined in Table 23. Each of the LEDs can be configured to indicate the information listed in the table by register setting. Each of the LEDs can be forced on or off to show customized information. When the code listed in Table 24, page 33 is written into an LED definition register, the corresponding LED will change to indicate the information that the code represents.





## RTL8212F & RTL8212G Datasheet

Table 23. LED Definitions

LED Definition	Description
Link/Act	PHY or SerDes Link/Activity Indicator. LED is lit when link is established and no traffic is detected. LED blinks when traffic is transmitted or received.
Link	PHY or SerDes Link Indicator. LED is lit when link is established.
Act	PHY or SerDes Activity Indicator. LED blinks when traffic is transmitted or received. LED is unlit when no traffic is detected.
Dup/Col	PHY Collision/Full Duplex Indicator. LED blinks when collision occurs. When there is no collision, an unlit LED means half duplex mode, and a lit LED means full duplex mode.
Dup	PHY Full Duplex Indicator. An unlit LED means half duplex mode, and a lit LED means full duplex mode.
Col	PHY Collision Indicator. LED blinks when collision occurs.
Spd1000	PHY 1000Mbps Speed Indicator. LED is lit only when link speed is 1000Mbps.
Spd100	PHY 100Mbps Speed Indicator. LED is lit only when link speed is 100Mbps.
Spd10	PHY 10Mbps Speed Indicator. LED is lit only when link speed is 10Mbps.
Spd1000Link/Act	PHY 1000Mbps Speed Link/Activity Indicator. LED is lit when link is established at 1000Mbps speed and no traffic is detected. LED blinks when traffic is transmitted or received at 1000Mbps speed.
Spd100Link/Act	PHY 100Mbps Speed Link/Activity Indicator. LED is lit when link is established at 100Mbps speed and no traffic is detected. LED blinks when traffic is transmitted or received at 100Mbps speed.
Spd10Link/Act	PHY 10Mbps Speed Link/Activity Indicator. LED is lit when link is established at 10Mbps speed and no traffic is detected. LED blinks when traffic is transmitted or received at 10Mbps speed.
Spd100(10)Link/Act	PHY 10/100Mbps Speed Link/Activity Indicator. LED is lit when link is established at 10/100Mbps speed and no traffic is detected. LED blinks when traffic is transmitted or received at 10/100Mbps speed.
Link/RxAct	PHY or SerDes Link/RX Activity Indicator. LED is lit when link is established and no traffic is received. LED blinks when traffic is received.
Link/TxAct	PHY or SerDes Link/TX Activity Indicator. LED is lit when link is established and no traffic is transmitted. LED blinks when traffic is transmitted.
Fault	PHY or SerDes Auto-Negotiation Fault Indicator. LED is lit when auto-negotiation fault is detected.
Master	PHY Link on Master Indicator. LED is lit when local device links in 1000M master mode.
Spd1000Link/Act_Bicolor	PHY 1000Mbps Speed/Link/Activity Indicator for Bi-Color LED. Only used in parallel mode LED 1 and LED 5 signals. If assigned to LED1, LED2 is set as Spd100Link/Act automatically. LED1 and LED2 are used to control a Bi-color LED. If assigned to LED5, LED6 is set as Spd100Link/Act automatically. LED5 and LED6 are used to control a Bi-color LED.
Spd100Link/Act_Bicolor	PHY 100Mb/s Speed/Link/Activity Indicator for Bi-Color LED. It is only used in parallel mode LED 1 and LED 5 signal. If assigned to LED1, LED2 is set as Spd10Link/Act automatically. LED1 and LED2 are used to control a Bi-color LED. If assigned to LED5, LED6 is set as Spd10Link/Act automatically. LED5 and LED6 are used to control a Bi-color LED.

Note 1: Receive activity, transmit activity, and collision are indicated by LED blinking. The blinking period is 43ms or 120ms and is configurable.

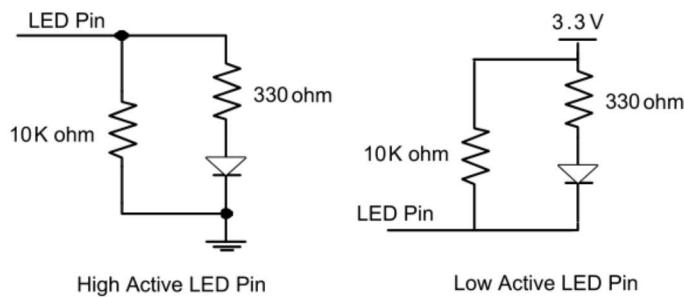
Note 2: After hardware reset, if DISPBLK=0, all LEDs will flash once simultaneously to indicate that the reset occurred.


**Table 24. LED Mapping Code**

<b>Code</b>	<b>LED Definition</b>	<b>Code</b>	<b>LED Definition</b>
000000	LED Off	111111	LED Force
000001	PHY0 Link/Act	100001	PHY1 Link/Act
000010	PHY0 Link	100010	PHY1 Link
000011	PHY0 Act	100011	PHY1 Act
000100	PHY0 Dup/Col	100100	PHY1 Dup/Col
000101	PHY0 Dup	100101	PHY1 Dup
000110	PHY0 Col	100110	PHY1 Col
000111	PHY0 Spd1000	100111	PHY1 Spd1000
001000	PHY0 Spd100	101000	PHY1 Spd100
001001	PHY0 Spd10	101001	PHY1 Spd10
001010	PHY0 Spd1000Link/Act	101010	PHY1 Spd1000Link/Act
001011	PHY0 Spd100Link/Act	101011	PHY1 Spd100Link/Act
001100	PHY0 Spd10Link/Act	101100	PHY1 Spd10Link/Act
001101	PHY0 Spd100(10)Link/Act	101101	PHY1 Spd100(10)Link/Act
001110	PHY0 Link/RxAct	101110	PHY1 Link/RxAct
001111	PHY0 Link/TxAct	101111	PHY1 Link/TxAct
010000	PHY0 Fault	110000	PHY1 Fault
010010	PHY0 Master	110010	PHY1 Master
010011	SD0 Link/Act	110011	SD1 Link/Act
010100	SD0 Link	110100	SD1 Link
010101	SD0 Fault	110101	SD1 Fault
010110	SD0 Link/RxAct	110110	SD1 Link/RxAct
010111	SD0 Link/TxAct	110111	SD1 Link/TxAct
011010	PHY0 Spd1000Link/Act_Bicolor	111010	PHY1 Spd1000Link/Act_Bicolor
011011	PHY0 Spd100Link/Act_Bicolor	111011	PHY1 Spd100Link/Act_Bicolor

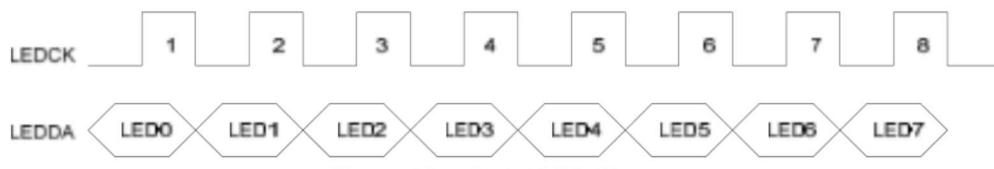
### 7.7.2. LED Mode Settings

Parallel or serial LED mode is determined by the LEDSPSEL pin (see Table 11, page 15). The Parallel LED is available only when PHYMODE[1:0] is not ‘00’. If the PHYMODE[1:0]=‘00’, the serial LED is selected. In parallel mode, 8 LED indication signals are represented by 8 LED pins correspondingly (see Table 8, page 13). These LED pins can be high active or low active pins (determined by the strapped value of these pins). When the strapped value is high, the LED pin will be low active, and vice versa (see Figure 17). The default strapped value of LED3 and LED7 are high. For the other LED pins, it is low.

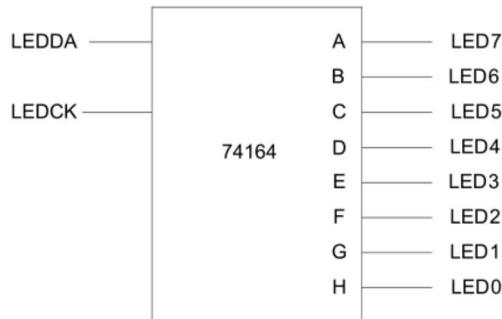


**Figure 17. High Active and Low Active LED Pin for Single-Color LED**

The RTL8212F/RTL8212G implements LEDCK and LEDDA pins as serial LED interface pins (see Table 8, page 13). These 8 LED signals are encapsulated within a shift sequence on the LEDDA pin. The LEDCK provides a 12.5MHz clock to synchronize the sequence. These two pins provide data and clock to enable an external shift register to capture the LED status indications from the RTL8212F/RTL8212G for each port (see Figure 18 and Figure 19).



**Figure 18. Serial LED Signal**



**Figure 19. Signal On 74164**

*Note: LED indication signals in serial mode are all low active.*

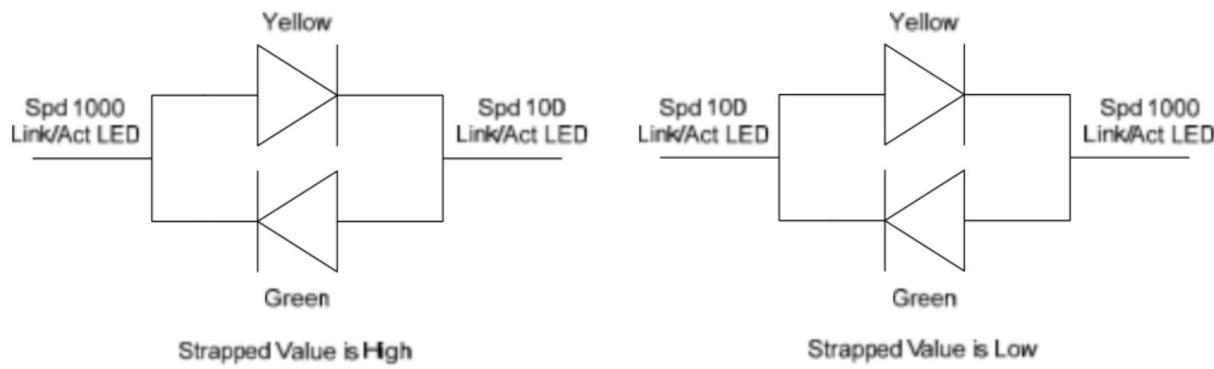
### 7.7.3. Bi-Color LED

A Bi-color LED is a single LED package with two LEDs connected in parallel with opposite polarities. It is controlled by two LED signals. In parallel mode, only LED1 and LED2, or LED5 and LED6 can be configured to be bi-color LEDs. The strapped value of the LED1 or LED5 pin determines the connection and the active high/low setting of the signals. Figure 20 and Table 26 show examples. The LED signal pairs that can compose a bi-color LED are shown below.

**Table 25. Available LED Signal Pairs for Bi-Color LED**

Pair	LED1 or LED5	LED2 or LED6
1	Spd1000Link/Act	Spd100Link/Act
2	Spd100Link/Act	Spd10Link/Act

Note: In serial LED mode, any of the 8 LEDs can be configured with another to compose a bi-color LED.



**Figure 20. Bi-Color LED in Parallel LED Mode**

**Table 26. Bi-Color LED Truth Table for Parallel LED Mode**

Indication	Bi-Color State	The Strapped Value of Spd1000Link/Act LED Pin is High		The Strapped Value of Spd1000Link/Act LED Pin is Low	
		Spd1000Link/Act (LED1 or LED5)	Spd100Link/Act (LED2 or LED6)	Spd1000Link/Act (LED1 or LED5)	Spd100Link/Act (LED2 or LED6)
No Link	Both Off	1	1	0	0
1000M Link	Green On	0	1	1	0
100M Link	Yellow On	1	0	0	1
1000M Act	Green Flash	Flash	1	Flash	0
100M Act	Yellow Flash	1	Flash	0	Flash



## 8. Register Descriptions

1000Base-T, 1000Base-X, and 100Base-FX registers are described in this section. Registers that have the same definitions in 1000Base-T, 1000Base-X, and 100Base-FX are described without distinction.

Registers for GPHY and SerDes are located in various register pages that are determined by register 31 (see Table 43, page 45). On the SerDes page, the registers are for 1000Base-X by default. They are used for 100Base-FX when register 0 is written to 0x2100.

### 8.1. Register List

In this section the following abbreviations are used:

RO: Read Only

LH: Latch High until clear

RW: Read/Write

SC: Self Clearing

LL: Latch Low until clear

**Table 27. Register List**

<b>PORT</b>	<b>Page</b>	<b>Register</b>	<b>Register Description</b>	<b>Default</b>
0~1	Copper (0x40)	0	Control Register	0x1140
		1	Status Register	0x7949
		2	PHY Identifier 1	0x001C
		3	PHY Identifier 2	0xC960
		4	Auto-Negotiation Advertisement Register	0x0DE1
		5	Auto-Negotiation Link Partner Ability Register	0x0000
		6	Auto-Negotiation Expansion Register	0x0004
		7	Auto-Negotiation Page Transmit Register	0x2001
		8	Auto-Negotiation Link Partner Next Page Register	0x0000
		9	1000Base-T Control Register	0x0E00
		10	1000Base-T Status Register	0x0000
		15	Extended Status	0x2000
		31	ASIC Control Register	0x0040
0~1	Fiber (0x50)	0	Control Register	0x1140
		1	Status Register	0x0109
		2	PHY Identifier 1	0x001C
		3	PHY Identifier 2	0xC960
		4	Auto-Negotiation Advertisement Register	0x01A0
		5	Auto-Negotiation Link Partner Ability Register	0x0000
		6	Auto-Negotiation Expansion Register	0x0004
		7	Auto-Negotiation Page Transmit Register	0x0004
		8	Auto-Negotiation Link Partner Next Page Register	0x0000
		15	Extended Status	0x2000
		31	ASIC Control Register	0x0050



## 8.2. Port 0~1 Register 0: Control

Table 28. Port 0~1 Register 0: Control

Reg.bit	Name	Mode	Description	1000 Base-T Default	1000 Base-X Default	100 Base-FX Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing.	0	0	0
0.14	Loopback (Digital Loopback)	RW	1: Enable loopback This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation	0	0	0
0.13	Speed Selection[0]	RW	[0.6, 0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	0	0	1
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process	1	1	0
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0	0	0
0.10	Isolate	RW	1: Electrically isolates the PHY The PHY is still able to respond to MDC/MDIO. 0: Normal operation	0	0	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0	0	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation	1	1	1
0.7	Reserved	RO	Reserved	0	0	0
0.6	Speed Selection[1]	RW	See Bit 13	1	1	0
0.[5:0]	Reserved	RO	Reserved	000000	000000	000000



### 8.3. Port 0~1 Register 1: Status

Table 29. Port 0~1 Register 1: Status

Reg.bit	Name	Mode	Description	1000 Base-T Default	1000 Base-X Default	100 Base-FX Default
1.15	100Base-T4	RO	0: No 100Base-T4 capability This bit should always be 0.	0	0	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1	0	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1	0	0
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1	0	0
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1	0	0
1.10	100Base-T2-FD	RO	0: No 100Base-T2 full duplex capability This bit should always be 0.	0	0	0
1.9	100Base-T2-HD	RO	0: No 100Base-T2 half duplex capability This bit should always be 0.	0	0	0
1.8	Extended Status	RO	1: Extended status info in Register 15 1: No extended status information	1	1	0
1.7	Reserved	RO	Reserved	0	0	0
1.6	MF Preamble Suppression	RO	1: Accept management frames with preamble suppressed 0: Not accept management frames with preamble suppressed	0	0	0
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0	0	0
1.4	Remote Fault	RO/LH	1: Remote fault indication from link partner has been detected 0: No remote fault indication detected This bit will remain set until it is cleared by reading register 1 via management interface.	0	0	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable	1	1	0
1.2	Link Status	RO/LL	1: Link has never failed since previous read 0: Link has failed since previous read If link fails, this bit will be set to 0 until bit is read.	0	0	0
1.1	Jabber Detect	RO/LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	0	0	0
1.0	Extended Capability	RO	1: Extended register capable	1	1	0





## 8.4. Port 0~1 Register 2: PHY Identifier 1

Table 30. Port 0~1 Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3 <sup>rd</sup> to 18 <sup>th</sup> Bits of the Organizationally Unique Identifier (OUI), Respectively	0x001C

## 8.5. Port 0~1 Register 3: PHY Identifier 2

Table 31. Port 0~1 Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19 <sup>th</sup> through 24 <sup>th</sup> Bits of the Organizationally Unique Identifier (OUI)	110010
3.[9:4]	Model Number	RO	Manufacturer's Model number	010011
3.[3:0]	Revision Number	RO	Manufacturer's Revision number	0000

## 8.6. Port 0~1 Register 4: 1000Base-T Auto-Negotiation Advertisement

Table 32. Port 0~1 Register 4: 1000Base-T Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8212F/RTL8212G has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Asymmetric Pause	RW	1: Enable Asymmetric Pause 0: Disable Asymmetric Pause	1
4.10	Pause	RW	1: Advertises that the RTL8212F/RTL8212G possesses 802.3x flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	Technology not supported (Permanently=0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001



## **8.7. Port 0~1 Register 4: 1000Base-X Auto-Negotiation Advertisement**

**Table 33. Port 0~1 Register 4: 1000Base-X Auto-Negotiation Advertisement**

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RW	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Reserved	RO	Reserved	0
4.[13:12]	Remote Fault	RW	00: No error, link OK (default) 01: Link Failure 10: Offline 11: Auto-Negotiation Error	00
4.[11:9]	Reserved	RO	Reserved	0
4.8	Asymmetric Pause	RW	1: Advertises that the RTL8212F/RTL8212G has asymmetric flow control capability 0: No asymmetric flow control capability	1
4.7	Pause	RW	1: Advertises that the RTL8212F/RTL8212G has flow control capability 0: No flow control capability	1
4.6	Half Duplex	RW	1: Half Duplex capable 0: Not Half Duplex capable	0
4.5	Full Duplex	RW	1: Full Duplex capable 0: Not Full Duplex capable	1
4.[4:0]	Reserved	RO	Reserved	00000

Note: This register is not used in 100Base-FX.

## **8.8. Port 0~1 Register 5: 1000Base-T Auto-Negotiation Link Partner Ability**

**Table 34. Port 0~1 Register 5: 1000Base-T Auto-Negotiation Link Partner Ability**

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Reserved	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner	0
5.10	Pause	RO	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0



<b>Reg.bit</b>	<b>Name</b>	<b>Mode</b>	<b>Description</b>	<b>Default</b>
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	[00001]: IEEE 802.3	00000

## **8.9. Port 0~1 Register 5: 1000Base-X Auto-Negotiation Link Partner Ability**

**Table 35. Port 0~1 Register 5: 1000Base-X Auto-Negotiation Link Partner Ability**

<b>Reg.bit</b>	<b>Name</b>	<b>Mode</b>	<b>Description</b>	<b>Default</b>
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.[13:12]	Remote Fault	RO	00: No error, link OK (default) 01: Link Failure 10: Offline 11: Auto-Negotiation Error	00
5.[11:9]	Reserved	RO	Ignore On Read	0
5.8	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner. When auto-negotiation is enabled, this bit reflects Link Partner ability (Read only)	0
5.7	Pause	RO	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (Read only)	0
5.6	Half Duplex	RO	1: Half Duplex capable 0: Not Half Duplex capable	0
5.5	Full Duplex	RO	1: Full Duplex capable 0: Not Full Duplex capable	0
5.[4:0]	Selector Field	RO	[00001]: IEEE 802.3	00000

*Note: This register is not used in 100Base-FX.*

## 8.10. Port 0~1 Register 6: 1000Base-T Auto-Negotiation Expansion

Table 36. Port 0~1 Register 6: 1000Base-T Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore On Read	0
6.4	Parallel Detection Fault	RO/LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	1: Next Page able	1
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is Enabled, This Bit Means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

## 8.11. Port 0~1 Register 6: 1000Base-X Auto-Negotiation Expansion

Table 37. Port 0~1 Register 6: 1000Base-X Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:2]	Reserved	RO	Ignore On Read	0000 0000 0000 01
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Reserved	RO	Ignore On Read	0

Note: This register is not used in 100Base-FX.



## **8.12. Port 0~1 Register 7: 1000Base-T and 1000Base-X Auto-Negotiation Page Transmit Register**

Table 38. Port 0~1 Register 7: Auto-Negotiation Page Transmit Register

Reg.bit	Name	Mode	Description	1000 Base-T Default	1000 Base-X Default
7.15	Next Page	RW	1: Another next page desired 0: No other next page to send	0	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0	0
7.13	Message Page	RW	1: Message page	1	0
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0	0
7.11	Toggle	RO	Toggle Bit	0	0
7.[10:0]	Message/ Unformatted Field	RW	Content of Message/Unformatted Page	0000 0000 001	0000 0000 100

Note: This register is not used in 100Base-FX.

## **8.13. Port 0~1 Register 8: 1000Base-T and 1000Base-X Auto-Negotiation Link Partner Next Page Register**

Table 39. Port 0~1 Register 8: Auto-Negotiation Link Partner Next Page Register

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14	0
8.13	Message Page	RO	Received Link Code Word Bit 13	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12	0
8.11	Toggle	RO	Received Link Code Word Bit 11	0
8.[10:0]	Message/Unformatted Field	RO	Received Link Code Word Bit 10:0	0

Note: This register is not used in 100Base-FX.



## 8.14. Port 0~1 Register 9: 1000Base-T Control Register

Table 40. Port 0~1 Register 9: 1000Base-T Control Register

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select. 000: Normal mode 001: Test mode 1 – Transmit waveform test 010~111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full Duplex	RW	1: Advertise PHY is 1000Base-T full duplex capable 0: Advertise PHY is not 1000Base-T full duplex capable	1
9.8	1000Base-T Half Duplex	RW	1: Advertise PHY is 1000Base-T half duplex capable 0: Advertise PHY is not 1000Base-T half duplex capable	0
9.[7:0]	Reserved	RW	Reserved	0

Note: This register is not used in 100Base-FX and 1000Base-X.

## 8.15. Port 0~1 Register 10: 1000Base-T Status Register

Table 41. Port 0~1 Register 10: 1000Base-T Status Register

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH /SC	1: MASTER/SLAVE configuration fault detected 0: no MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full Duplex	RO	1: Link partner is capable of 1000Base-T full duplex 0: Link partner is not capable of 1000Base-T full duplex	0
10.10	1000Base-T Half Duplex	RO	1: Link partner is capable of 1000Base-T half duplex 0: Link partner is not capable of 1000Base-T half duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle error counter. The counter stops automatically when it reaches 0xFF	0

Note: This register is not used in 100Base-FX and 1000Base-X.



## **8.16. Port 0~1 Register 15: Extended Status**

**Table 42. Port 0~1 Register 15: Extended Status**

<b>Reg.bit</b>	<b>Name</b>	<b>Mode</b>	<b>Description</b>	<b>1000 Base-T Default</b>	<b>1000 Base-X Default</b>
15.15	1000Base-X Full Duplex	RO	1: 1000Base-X full duplex capable 0: Not 1000Base-X full duplex capable	0	1
15.14	1000Base-X Half Duplex	RO	1: 1000Base-X half duplex capable 0: Not 1000Base-X half duplex capable	0	0
15.13	1000Base-T Full Duplex	RO	1: 1000Base-T full duplex capable 0: Not 1000Base-T full duplex capable	1	0
15.12	1000Base-T Half Duplex	RO	1: 1000Base-T half duplex capable 0: Not 1000Base-T half duplex capable	0	0
15.[11:0]	Reserved	RO	Reserved	0	0

Note: This register is not used in 100Base-FX.

## **8.17. Port 0~1 Register 31: Page Selection**

**Table 43. Port 0~1 Register 31: Page Selection**

<b>Reg.bit</b>	<b>Name</b>	<b>Mode</b>	<b>Description</b>	<b>Default</b>
31.[15:7]	Reserved	-	Reserved	0
31.[6:0]	Page Selection	RW	Register Page Selection. 0x40: 10/100/1000Base-T register page. Registers 0~15 are the registers for copper. 0x50: 100Base-FX/1000Base-X register page. Registers 0~15 are the registers for fiber. Others: Reserved	0x40



## 9. Characteristics

### 9.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability may be affected. All voltages are specified reference to their corresponding ground unless otherwise specified.

**Table 44. Absolute Maximum Ratings**

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Supply Voltage Referenced to AGND, AVSSPLL, SGND, DGND: AVDD12, AVDDPLL, SVDD12, and VDD12	Ground-0.5	+1.32	V
Supply Voltage Referenced to AGND, DGND: AVDD33, DVDD, and VDDIO	Ground-0.5	+3.63	V
Digital Input Voltage	Ground-0.5	DVDD and VDDIO	V

### 9.2. Operating Range

**Table 45. Operating Range**

Parameter	Min	Max	Units
Ambient Operating Temperature for RTL8212F/RTL8212G	0	+70	°C
1.2V AVDD12, AVDDPLL, SVDD12, and VDD12 Supply Voltage Range	1.14	1.26	V
3.3V AVDD33 Supply Voltage Range	3.14	3.46	V
DVDD and VDDIO Supply Voltage Range	2.5	3.46	V

### 9.3. DC Characteristics

#### 9.3.1. Digital IO DC Characteristics

**Table 46. Digital IO DC Characteristics**

Parameter	SYM	Condition	Min	Typ	Max	Units
TTL Input Current	I <sub>in</sub>	-	-10	-	10	μA
TTL Input Capacitance	C <sub>in</sub>	-	-	3	-	pF
TTL Input High Voltage	V <sub>ih</sub>	Power Supply for Digital IO=3.3V	2.0	-	-	V
TTL Input Low Voltage	V <sub>il</sub>	Power Supply for Digital IO=3.3V	-	-	0.8	V
Output High Voltage	V <sub>oh</sub>	Power Supply for Digital IO=3.3V	2.4	-	-	V
Output Low voltage	V <sub>ol</sub>	Power Supply for Digital IO=3.3V	-	-	0.4	V
TTL Input High Voltage	V <sub>ih</sub>	Power Supply for Digital IO=2.5V	1.7	-	-	V
TTL Input Low Voltage	V <sub>il</sub>	Power Supply for Digital IO=2.5V	-	-	0.7	V
Output High Voltage	V <sub>oh</sub>	Power Supply for Digital IO=2.5V	2.0	-	-	V
Output Low voltage	V <sub>ol</sub>	Power Supply for Digital IO=2.5V	-	-	0.2	V
Output Three State Leakage Current	I <sub>OZ</sub>	-	-	-	10	μA



### 9.3.2. Power Consumption for RGMII Application

Test conditions for the following power consumption tests are:

1. Serial LED Mode.
2. AVDD33=DVDD=VDDIO=3.30V; AVDD12=AVDDPLL=SVDD12=VDD12=1.20V.
3. Random packet length and 100% loading traffic stream.

**Table 47. Power Consumption for RGMII Application**

Parameter	SYM	Condition	Min	Typ	Max	Units
<b>Two Copper Ports</b>						
Power Supply Current for Analog 1.2V	Icc	Link Down	-	28	-	mA
		10Base-T Idle	-	28	-	
		10Base-T Peak Continuous 100% Utilization	-	28	-	
		100Base-TX Idle	-	83	-	
		100Base-TX Peak Continuous 100% Utilization	-	83	-	
		1000Base-T Idle	-	250	-	
		1000Base-T Peak Continuous 100% Utilization	-	250	-	
Power Supply Current for Digital 1.2V	Icc	Link Down	-	84	-	mA
		10Base-T Idle	-	89	-	
		10Base-T Peak Continuous 100% Utilization	-	90	-	
		100Base-TX Idle	-	115	-	
		100Base-TX Peak Continuous 100% Utilization	-	117	-	
		1000Base-T Idle	-	357	-	
		1000Base-T Peak Continuous 100% Utilization	-	394	-	
Power Supply Current for SerDes 1.2V	Icc	Link Down	-	25	-	mA
		10Base-T Idle	-	25	-	
		10Base-T Peak Continuous 100% Utilization	-	25	-	
		100Base-TX Idle	-	25	-	
		100Base-TX Peak Continuous 100% Utilization	-	25	-	
		1000Base-T Idle	-	25	-	
		1000Base-T Peak Continuous 100% Utilization	-	25	-	
Power Supply Current for Analog 3.3V	Icc	Link Down	-	49	-	mA
		10Base-T Idle	-	104	-	
		10Base-T Peak Continuous 100% Utilization	-	183	-	
		100Base-TX Idle	-	98	-	
		100Base-TX Peak Continuous 100% Utilization	-	98	-	
		1000Base-T Idle	-	135	-	
		1000Base-T Peak Continuous 100% Utilization	-	135	-	
Power Supply Current for Digital 3.3V	Icc	Link Down	-	11	-	mA
		10Base-T Idle	-	11	-	
		10Base-T Peak Continuous 100% Utilization	-	12	-	
		100Base-TX Idle	-	16	-	
		100Base-TX Peak Continuous 100% Utilization	-	21	-	
		1000Base-T Idle	-	39	-	
		1000Base-T Peak Continuous 100% Utilization	-	98	-	



## RTL8212F & RTL8212G Datasheet

Parameter	SYM	Condition	Min	Typ	Max	Units
Total Power Consumption for All Ports	PS	Link Down	-	362.4	-	mW
		10Base-T Idle	-	549.9	-	
		10Base-T Peak Continuous 100% Utilization	-	815.1	-	
		100Base-TX Idle	-	643.8	-	
		100Base-TX Peak Continuous 100% Utilization	-	662.7	-	
		1000Base-T Idle	-	1332.6	-	
		1000Base-T Peak Continuous 100% Utilization	-	1571.7	-	
<b>Two Fiber Ports</b>						
Power Supply Current for Analog 1.2V	Icc	1000Base-X Link Down	-	24	-	mA
		100Base-FX Link Down	-	24	-	
		100Base-FX Idle	-	24	-	
		100Base-FX Peak Continuous 100% Utilization	-	24	-	
		1000Base-X Idle	-	25	-	
		1000Base-X Peak Continuous 100% Utilization	-	25	-	
Power Supply Current for Digital 1.2V	Icc	1000Base-X Link Down	-	95	-	mA
		100Base-FX Link Down	-	87	-	
		100Base-FX Idle	-	87	-	
		100Base-FX Peak Continuous 100% Utilization	-	86	-	
		1000Base-X Idle	-	112	-	
		1000Base-X Peak Continuous 100% Utilization	-	120	-	
Power Supply Current for SerDes 1.2V	Icc	1000Base-X Link Down	-	90	-	mA
		100Base-FX Link Down	-	83	-	
		100Base-FX Idle	-	92	-	
		100Base-FX Peak Continuous 100% Utilization	-	93	-	
		1000Base-X Idle	-	101	-	
		1000Base-X Peak Continuous 100% Utilization	-	102	-	
Power Supply Current for Analog 3.3V	Icc	1000Base-X Link Down	-	52	-	mA
		100Base-FX Link Down	-	52	-	
		100Base-FX Idle	-	52	-	
		100Base-FX Peak Continuous 100% Utilization	-	52	-	
		1000Base-X Idle	-	52	-	
		1000Base-X Peak Continuous 100% Utilization	-	52	-	
Power Supply Current for Digital 3.3V	Icc	1000Base-X Link Down	-	39	-	mA
		100Base-FX Link Down	-	16	-	
		100Base-FX Idle	-	16	-	
		100Base-FX Peak Continuous 100% Utilization	-	21	-	
		1000Base-X Idle	-	39	-	
		1000Base-X Peak Continuous 100% Utilization	-	98	-	
Total Power Consumption for All Ports	PS	1000Base-X Link Down	-	551.1	-	mW
		100Base-FX Link Down	-	457.2	-	
		100Base-FX Idle	-	468.0	-	
		100Base-FX Peak Continuous 100% Utilization	-	484.5	-	
		1000Base-X Idle	-	585.9	-	
		1000Base-X Peak Continuous 100% Utilization	-	791.4	-	



### 9.3.3. Power Consumption for GMII/MII Application (RTL8212G Only)

Test conditions for the following power consumption tests are:

1. Serial LED Mode.
2. AVDD33=DVDD=VDDIO=3.30V; AVDD12=AVDDPLL=SVDD12=VDD12=1.20V.
3. Random packet length and 100% loading traffic stream.

**Table 48. Power Consumption for GMII/MII Application (RTL8212G Only)**

Parameter	SYM	Condition	Min	Typ	Max	Units
<b>Two Copper Ports</b>						
Power Supply Current for Analog 1.2V	Icc	Link Down	-	28	-	mA
		10Base-T Idle	-	28	-	
		10Base-T Peak Continuous 100% Utilization	-	28	-	
		100Base-TX Idle	-	83	-	
		100Base-TX Peak Continuous 100% Utilization	-	83	-	
		1000Base-T Idle	-	250	-	
Power Supply Current for Digital 1.2V	Icc	Link Down	-	80	-	mA
		10Base-T Idle	-	90	-	
		10Base-T Peak Continuous 100% Utilization	-	90	-	
		100Base-TX Idle	-	115	-	
		100Base-TX Peak Continuous 100% Utilization	-	116	-	
		1000Base-T Idle	-	354	-	
Power Supply Current for SerDes 1.2V	Icc	Link Down	-	25	-	mA
		10Base-T Idle	-	25	-	
		10Base-T Peak Continuous 100% Utilization	-	25	-	
		100Base-TX Idle	-	25	-	
		100Base-TX Peak Continuous 100% Utilization	-	25	-	
		1000Base-T Idle	-	25	-	
Power Supply Current for Analog 3.3V	Icc	Link Down	-	49	-	mA
		10Base-T Idle	-	104	-	
		10Base-T Peak Continuous 100% Utilization	-	183	-	
		100Base-TX Idle	-	98	-	
		100Base-TX Peak Continuous 100% Utilization	-	98	-	
		1000Base-T Idle	-	135	-	
Power Supply Current for Digital 3.3V	Icc	Link Down	-	11	-	mA
		10Base-T Idle	-	11	-	
		10Base-T Peak Continuous 100% Utilization	-	14	-	
		100Base-TX Idle	-	21	-	
		100Base-TX Peak Continuous 100% Utilization	-	26	-	
		1000Base-T Idle	-	39	-	
		1000Base-T Peak Continuous 100% Utilization	-	89	-	



## RTL8212F & RTL8212G Datasheet

Parameter	SYM	Condition	Min	Typ	Max	Units
Total Power Consumption for All Ports	PS	Link Down	-	357.6	-	mW
		10Base-T Idle	-	551.1	-	
		10Base-T Peak Continuous 100% Utilization	-	821.7	-	
		100Base-TX Idle	-	660.3	-	
		100Base-TX Peak Continuous 100% Utilization	-	678.0	-	
		1000Base-T Idle	-	1329.0	-	
		1000Base-T Peak Continuous 100% Utilization	-	1538.4	-	
<b>Two Fiber Ports</b>						
Power Supply Current for Analog 1.2V	Icc	1000Base-X Link Down	-	24	-	mA
		100Base-FX Link Down	-	24	-	
		100Base-FX Idle	-	24	-	
		100Base-FX Peak Continuous 100% Utilization	-	24	-	
		1000Base-X Idle	-	25	-	
		1000Base-X Peak Continuous 100% Utilization	-	25	-	
Power Supply Current for Digital 1.2V	Icc	1000Base-X Link Down	-	96	-	mA
		100Base-FX Link Down	-	88	-	
		100Base-FX Idle	-	86	-	
		100Base-FX Peak Continuous 100% Utilization	-	85	-	
		1000Base-X Idle	-	106	-	
		1000Base-X Peak Continuous 100% Utilization	-	112	-	
Power Supply Current for SerDes 1.2V	Icc	1000Base-X Link Down	-	90	-	mA
		100Base-FX Link Down	-	82	-	
		100Base-FX Idle	-	92	-	
		100Base-FX Peak Continuous 100% Utilization	-	93	-	
		1000Base-X Idle	-	101	-	
		1000Base-X Peak Continuous 100% Utilization	-	102	-	
Power Supply Current for Analog 3.3V	Icc	1000Base-X Link Down	-	52	-	mA
		100Base-FX Link Down	-	52	-	
		100Base-FX Idle	-	52	-	
		100Base-FX Peak Continuous 100% Utilization	-	52	-	
		1000Base-X Idle	-	52	-	
		1000Base-X Peak Continuous 100% Utilization	-	52	-	
Power Supply Current for Digital 3.3V	Icc	1000Base-X Link Down	-	39	-	mA
		100Base-FX Link Down	-	21	-	
		100Base-FX Idle	-	21	-	
		100Base-FX Peak Continuous 100% Utilization	-	26	-	
		1000Base-X Idle	-	39	-	
		1000Base-X Peak Continuous 100% Utilization	-	89	-	
Total Power Consumption for All Ports	PS	1000Base-X Link Down	-	552.3	-	mW
		100Base-FX Link Down	-	473.7	-	
		100Base-FX Idle	-	483.3	-	
		100Base-FX Peak Continuous 100% Utilization	-	499.8	-	
		1000Base-X Idle	-	578.7	-	
		1000Base-X Peak Continuous 100% Utilization	-	752.1	-	



### 9.3.4. Power Consumption for SGMII Application

Test conditions for the following power consumption tests are:

1. Serial LED Mode.
2. AVDD33=DVDD=VDDIO=3.30V; AVDD12=AVDDPLL=SVDD12=VDD12=1.20V.
3. Random packet length and 100% loading traffic stream.

**Table 49. Power Consumption for SGMII Application**

Parameter	SYM	Condition	Min	Typ	Max	Units
Power Supply Current for Analog 1.2V	Icc	Link Down	-	28	-	mA
		10Base-T Idle	-	28	-	
		10Base-T Peak Continuous 100% Utilization	-	28	-	
		100Base-TX Idle	-	83	-	
		100Base-TX Peak Continuous 100% Utilization	-	83	-	
		1000Base-T Idle	-	245	-	
		1000Base-T Peak Continuous 100% Utilization	-	245	-	
Power Supply Current for Digital 1.2V	Icc	Link Down	-	101	-	mA
		10Base-T Idle	-	109	-	
		10Base-T Peak Continuous 100% Utilization	-	102	-	
		100Base-TX Idle	-	135	-	
		100Base-TX Peak Continuous 100% Utilization	-	128	-	
		1000Base-T Idle	-	371	-	
		1000Base-T Peak Continuous 100% Utilization	-	400	-	
Power Supply Current for SerDes 1.2V	Icc	Link Down	-	158	-	mA
		10Base-T Idle	-	164	-	
		10Base-T Peak Continuous 100% Utilization	-	164	-	
		100Base-TX Idle	-	164	-	
		100Base-TX Peak Continuous 100% Utilization	-	165	-	
		1000Base-T Idle	-	165	-	
		1000Base-T Peak Continuous 100% Utilization	-	165	-	
Power Supply Current for Analog 3.3V	Icc	Link Down	-	49	-	mA
		10Base-T Idle	-	104	-	
		10Base-T Peak Continuous 100% Utilization	-	183	-	
		100Base-TX Idle	-	98	-	
		100Base-TX Peak Continuous 100% Utilization	-	98	-	
		1000Base-T Idle	-	135	-	
		1000Base-T Peak Continuous 100% Utilization	-	135	-	
Power Supply Current for Digital 3.3V	Icc	Link Down	-	18	-	mA
		10Base-T Idle	-	18	-	
		10Base-T Peak Continuous 100% Utilization	-	18	-	
		100Base-TX Idle	-	18	-	
		100Base-TX Peak Continuous 100% Utilization	-	18	-	
		1000Base-T Idle	-	13	-	
		1000Base-T Peak Continuous 100% Utilization	-	13	-	
Total Power Consumption for All Ports	PS	Link Down	-	565.5	-	mW
		10Base-T Idle	-	763.8	-	
		10Base-T Peak Continuous 100% Utilization	-	1016.1	-	
		100Base-TX Idle	-	841.2	-	
		100Base-TX Peak Continuous 100% Utilization	-	834.0	-	
		1000Base-T Idle	-	1425.6	-	
		1000Base-T Peak Continuous 100% Utilization	-	1460.4	-	



## 9.4. AC Characteristics

### 9.4.1. SerDes Transmitter Signal Electrical Characteristics

Table 50. SerDes Differential Transmitter Output Parameters

Symbol	Parameter	Min	Typical	Max	Units
V <sub>TX-DIFFp-p</sub>	Differential Peak to Peak Output Voltage 1000Base-X and 100Base-FX SGMII	0.6 0.35	0.8 -	1.0 0.4	V V
T <sub>TX-MAXJITTER</sub>	TX TIE Jitter Peak to Peak 1000Base-X 100Base-FX SGMII	- - -	- - -	120 120 120	ps ps ps
T <sub>TX-RISE</sub> T <sub>TX-FALL</sub> (20%~80%)	Differential TX Output Rise/Fall Time 1000Base-X 100Base-FX	100 180	- -	200 400	ps ps
C <sub>TX</sub>	AC Coupling Capacitor	75	100	200	nF
L <sub>TX</sub>	Transmit Length in PCB	-	-	5	Inch

### 9.4.2. SerDes Receiver Signal Electrical Characteristics

Table 51. SerDes Differential Receiver Input Parameters

Symbol	Parameter	Min	Typical	Max	Units
V <sub>RX-DIFFp-p</sub>	Differential Input Peak to Peak Voltage	0.3	-	1.0	V
T <sub>RX-MAXJITTER</sub>	Maximum RX Jitter Tolerance 1000Base-X/SGMII Deterministic Jitter 1000Base-X/SGMII Total Jitter 100Base-FX Deterministic Jitter 100Base-FX Total Jitter	- - - -	- - - -	0.2 0.5 0.5 0.7	UI UI UI UI
C <sub>RX</sub>	AC Coupling Capacitor	75	100	200	nF

### 9.4.3. RGMII Timing

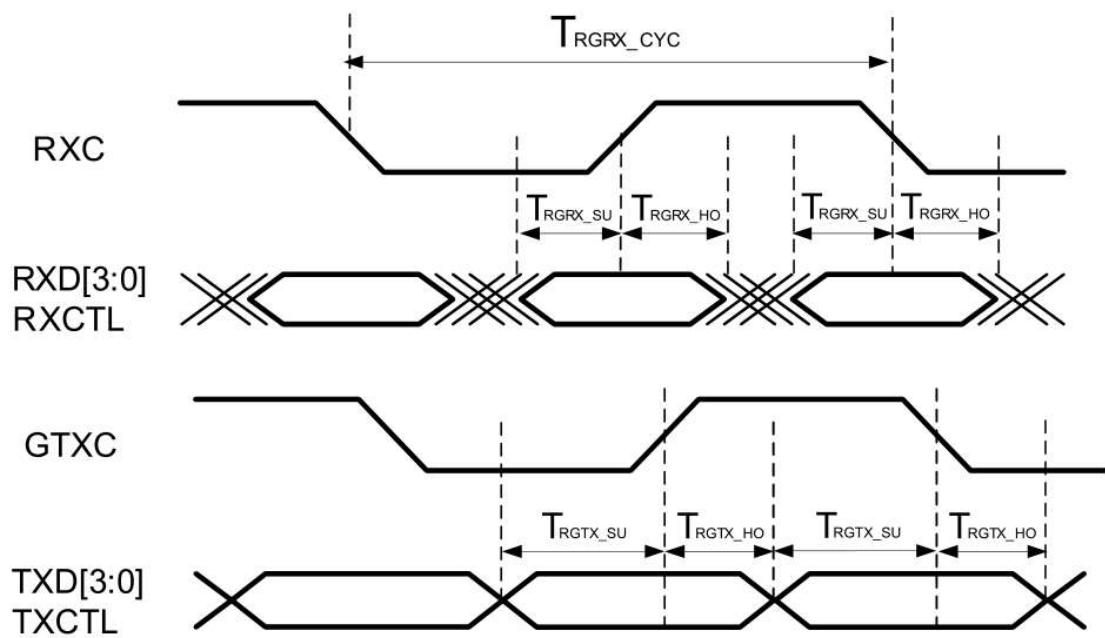


Figure 21. RGMII Timing

**Table 52. RGMII Timing Parameters**

<b>Parameter</b>	<b>SYM</b>	<b>Description</b>	<b>I/O</b>	<b>Min</b>	<b>Type</b>	<b>Max</b>	<b>Units</b>
1000/100/10Base-T RXC Output Cycle	T <sub>RGRx_cyc</sub>	RXC Clock 125M Output for 1000Base-T RXC Clock 25M Output for 100Base-TX RXC Clock 2.5M Output for 10Base-T	O	7.5 36 360	8.0 40 400	8.5 44 440	ns ns ns
RX Data to Clock Output Setup time	T <sub>RGRx_SU</sub>	RXD, RXCTL to RXC Output Setup (RXDLY=0): 1000M 100M 10M	O	-0.5 3 3	- - -	0.5	ns ns ns
		RXD, RXCTL to RXC Output Setup (RXDLY=1): 1000M 100M 10M	O	1.5 4 4	- - -	-	ns ns ns
RX Data to Clock Output Hold time	T <sub>RGRx_HO</sub>	RXD, RXCTL to RXC Output Hold (RXDLY=0): 1000M 100M 10M	O	3.0 10 150	- - -	-	ns ns ns
		RXD, RXCTL to RXC Output Hold (RXDLY=1): 1000M 100M 10M	O	1.0 8 140	- - -	-	ns ns ns
TX Data to Clock Input Setup time	T <sub>RGTX_SU</sub>	TXD, TXCTL to GTXC Input Setup for 1000/100/10M (TXDLY=0)	I	1.0	-	-	ns
		TXD, TXCTL to GTXC Input Setup for 1000/100/10M (TXDLY=1)		-500	-	-	ps
TX Data to Clock Input Hold time	T <sub>RGTX_HO</sub>	TXD, TXCTL to GTXC Input Hold for 1000/100/10M (TXDLY=0)	I	1.0	-	-	ns
		TXD, TXCTL to GTXC Input Hold for 1000/100/10M (TXDLY=1)		3.0	-	-	ns

#### 9.4.4. GMII/MII Timing (RTL8212G Only)

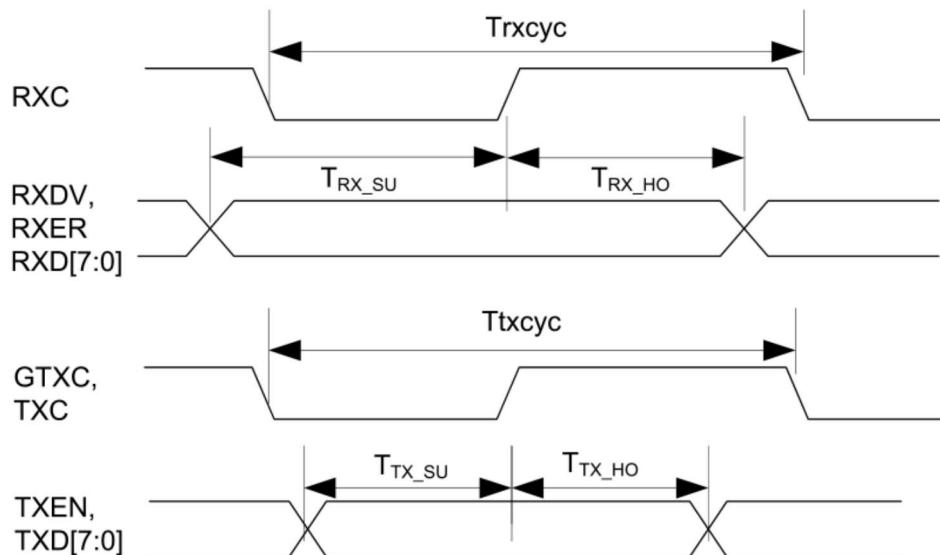


Figure 22. GMII/MII Timing (RTL8212G Only)

Table 53. GMII/MII Timing Parameters (RTL8212G Only)

Parameter	SYM	Description	I/O	Min	Type	Max	Units
<b>GMII</b>							
1000BaseT GTXC	T <sub>Txyc</sub>	GTXC 125MHz Clock Input	I	7.5	-	-	ns
1000BaseT RXC	T <sub>Rxyc</sub>	RXC 125MHz Clock Output	O	7.5	8.0	8.5	ns
RXD[7:0], RXDV, RXER to RXC Output Setup Time	T <sub>Rx_SU</sub>	RXD[7:0], RXDV, RXER to RXC Rising Edge Setup Time	O	3.5	-	-	ns
RXD[7:0], RXDV, RXER to RXC Output Hold Time	T <sub>Rx_HO</sub>	RXD[7:0], RXDV, RXER to RXC Rising Edge Hold Time	O	1.5	-	-	ns
TXD[7:0], TXEN to GTXC Input Setup Time	T <sub>Tx_SU</sub>	TXD[7:0], TXEN to GTXC Rising Edge Setup Time	I	2.0	-	-	ns
TXD[7:0], TXEN to GTXC Input Hold Time	T <sub>Tx_HO</sub>	TXD[7:0], TXEN to GTXC Rising Edge Hold Time	I	0.0	-	-	ns
<b>MII Timing</b>							
RXD[3:0], RXDV, RXER to RXC Output Setup Time	T <sub>Rx_SU</sub>	RXD[3:0], RXDV, RXER to RXC Rising Edge Setup Time	O	30	-	-	ns
RXD[3:0], RXDV, RXER to RXC Output Hold Time	T <sub>Rx_HO</sub>	RXD[3:0], RXDV, RXER to RXC Rising Edge Hold Time	O	4.5	-	-	ns
TXD[3:0], TXEN to TXC Input Setup Time	T <sub>Tx_SU</sub>	TXD[3:0], TXEN to TXC Rising Edge Setup Time	I	4.0	-	-	ns
TXD[3:0], TXEN to TXC Input Hold Time	T <sub>Tx_HO</sub>	TXD[3:0], TXEN to TXC Rising Edge Hold Time	I	2.0	-	-	ns

### 9.4.5. SMI Timing

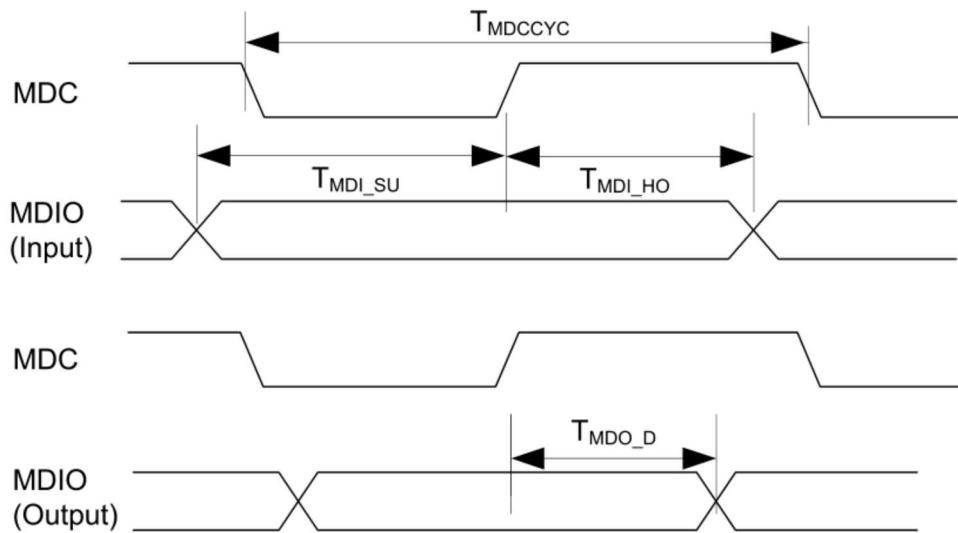


Figure 23. SMI Timing

Table 54. SMI Timing Parameters

Parameter	SYM	Description	I/O	Min	Typ	Max	Units
MDC	T <sub>MDCCYC</sub>	MDC Cycle Time Clock Cycle Time	I	400	-	-	ns
MDIO to MDC Output Delay	T <sub>MDO_D</sub>	MDIO to MDC Output Delay	O	2.8	-	7.8	ns
MDIO Input Setup Time	T <sub>MDI_SU</sub>	MDIO to MDC Rising Edge Setup Time	I	4	-	-	ns
MDIO Input Hold Time	T <sub>MDI_HO</sub>	MDIO to MDC Rising Edge Hold Time	I	2	-	-	ns

#### 9.4.6. Serial LED Timing

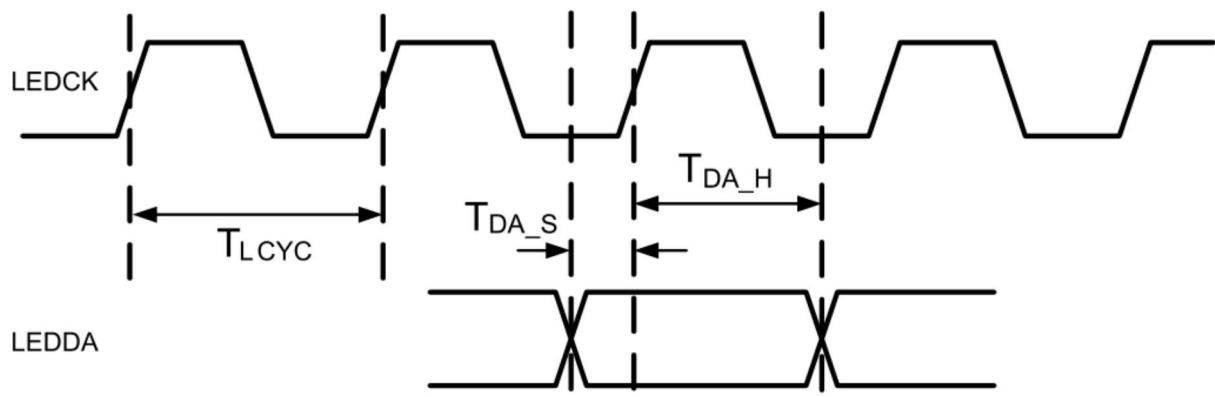


Figure 24. Serial LED Timing

Table 55. Serial LED Timing Parameters

Parameter	SYM	Description	Min	Typ	Max	Units
LEDCK Cycle Time	$T_{LCYC}$	LEDCK Output Clock Cycle Time	79	80	81	ns
LEDDA Setup Time	$T_{DA\_S}$	LEDDA to LEDCK Rising Output Setup Time	22	-	-	ns
LEDDA Hold Time	$T_{DA\_H}$	LEDDA to LEDCK Rising Output Hold Time	54	-	-	ns

## 10. Design and Layout

In order to achieve maximum performance using the RTL8212F/RTL8212G, good design attention is required throughout the design and layout process. The following are some suggestions to implement a high-performance system.

### 10.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV).
- Verify the ability of critical components, e.g., clock source and transformer, to meet application requirements.
- Use bulk capacitors (4.7 $\mu$ F-10 $\mu$ F) between the power and ground planes.
- Use 0.1 $\mu$ F de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8212F/RTL8212G (less than 200 mil).
- The transformer should be placed as close as possible to the RTL8212F/RTL8212G (less than 12cm).
- The RJ-45 jack should be placed as close as possible to the transformer.

### 10.2. Ethernet MDI Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other.

### 10.3. Power Planes

- Divide the power plane into 1.2V digital, 1.2V analog, 3.3V digital, and 3.3V analog.
- Use 0.1 $\mu$ F decoupling capacitors and bulk capacitors between each power plane and ground plane.

### 10.4. Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.



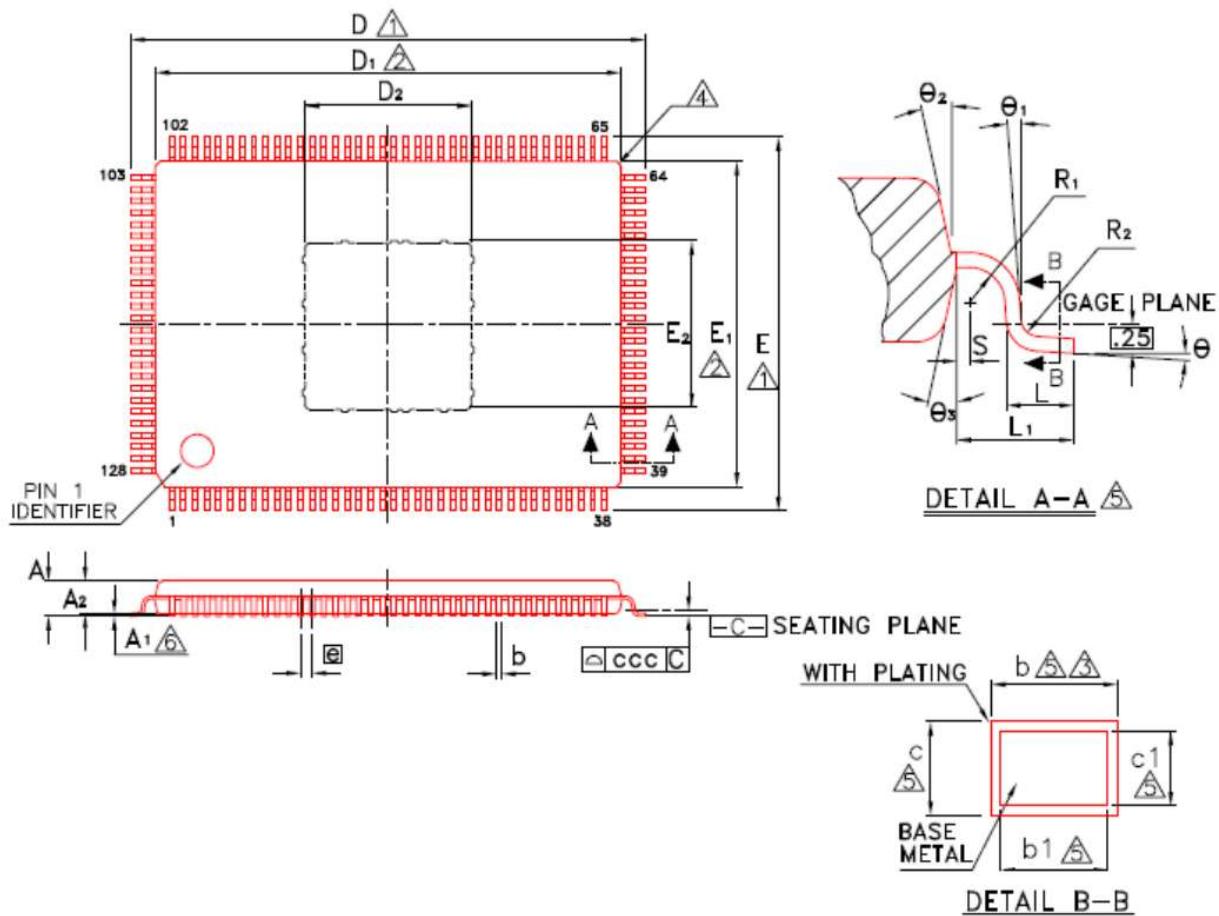
## 10.5. Transformer Options

The RTL8212F/RTL8212G uses a transformer with a 1:1 turn ratio. There are many vendors offering transformer designs that meet the RTL8212F/RTL8212G's requirement. Examples are:

Vendor	Type
FLY-CORE	FC1503NL
FLY-CORE	FC-202GYDNL

## 11. Mechanical Dimensions

### 11.1. RTL8212F-GR: LQFP-128 E-PAD Package



See the Mechanical Dimensions notes on the next page.



## 11.2. Mechanical Dimensions Notes for RTL8212F-GR LQFP-128 (14\*20mm)

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	-	0.20	0.004	-	0.008
c1	0.09	-	0.16	0.004	-	0.006
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
D2/E2	6.4	-	8.4	0.251	-	0.331
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
[e]	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.003	-	0.008
S	0.20	-	-	0.008	-	-
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	4° TYP			4° TYP		
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		
ccc	0.08			0.003		

Note1: To be determined at seating plan -C.

Note2: Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

Note3: Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius or the foot.

Note4: Exact shape of each corner is option.

Note5: These Dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Note6: A1 is defined as the distance from the seating plan to the lowest point of the package body.

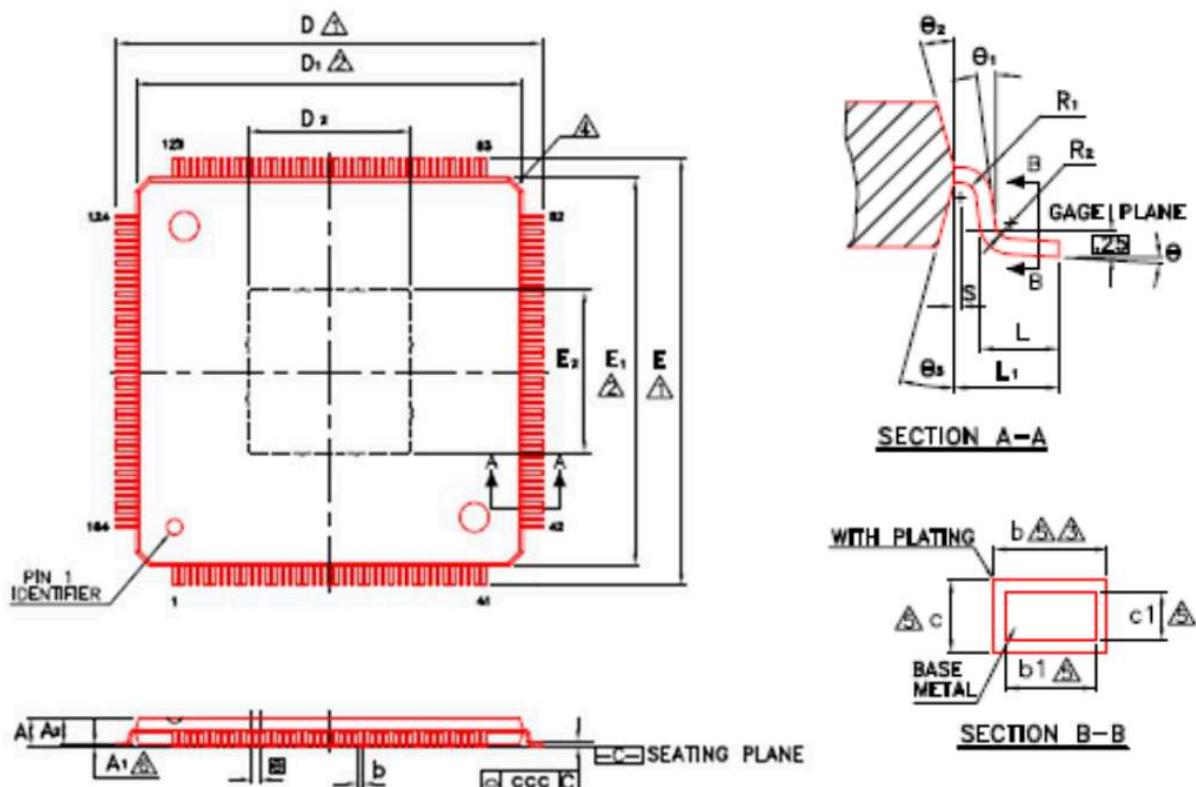
Note7: Controlling Dimension: Millimeter.

Note8: Reference document: JEDEC MS-026.

Note9: Special characteristics C class: ccc.



### 11.3. RTL8212G-GR: LQFP-164 E-PAD Package





## 11.4. Mechanical Dimensions Notes for RTL8212G-GR LQFP-164 (20\*20mm)

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	-	0.20	0.004	-	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D1	-	20.00	-	-	0.787	-
D2/E2	6.4	-	8.4	0.251	-	0.331
E	21.60	22.00	22.40	0.850	0.866	0.882
E1	-	20.00	-	-	0.787	-
[e]	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	-	1.00	-	-	0.039	-
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.003	-	-
S	0.20	-	-	0.008	-	-
$\theta$	$0^\circ$	$3.5^\circ$	$7^\circ$	$0^\circ$	$3.5^\circ$	$7^\circ$
$\theta_1$	$0^\circ$	-	-	$0^\circ$	-	-
$\theta_2$	$11^\circ$	$12^\circ$	$13^\circ$	$11^\circ$	$12^\circ$	$13^\circ$
$\theta_3$	$11^\circ$	$12^\circ$	$13^\circ$	$11^\circ$	$12^\circ$	$13^\circ$
ccc	0.08			0.003		

Note1: To be determined at seating plan -C.

Note2: Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

Note3: Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius or the foot.

Note4: Exact shape of each corner is option.

Note5: These Dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Note6: A1 is defined as the distance from the seating plan to the lowest point of the package body.

Note7: Controlling Dimension: Millimeter.

Note8: Reference document: JEDEC MS-026.

Note9: Special characteristics C class: ccc.



## 12. Ordering Information

Table 56. Ordering Information

Part Number	Package	Status
RTL8212F-GR	128-Pin LQFP with E-PAD, 'Green' Package	
RTL8212G-GR	164-Pin LQFP with E-PAD, 'Green' Package	

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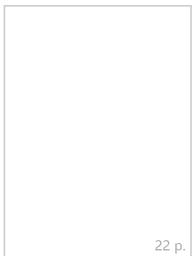
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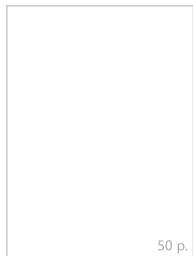
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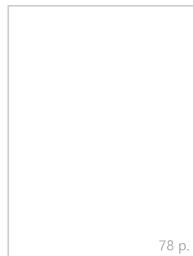
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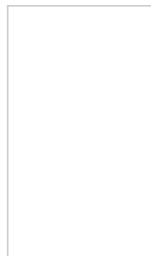
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