RTL8103E-GR
RTL8103EL-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

EEPROM & eFUSE DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.1
12 February 2009
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

LICENSE

This product is covered by one or more of the following patents: US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer's register information on the Realtek RTL8103E and RTL8103EL chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/11/21	First release.
1.1	2009/02/12	Added Table 4 9346CR: 93C46 (93C56) Command (Offset 0050h, RW), page 5.

Table of Contents

List of Tables

1. EEPROM (93C46/93C56) Contents

The RTL8103E(L) requires an external EEPROM. The 93C46/93C56 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8103E(L) to read from, and write data to, an external serial EEPROM device.

Note: The RTL8103EL only supports 93C46 EEPROM.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on reset, PCI reset, and software EEPROM auto-load command. The RTL8103E(L) will auto-load values from the EEPROM.

If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8103E(L) initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using 'bit-bang' accesses via the 9346CR Register, or using PCI VPD (Vital Product Data).

Although it is actually addressed by words, the EEPROM contents are listed in Table 1 below by bytes for convenience. After the power-on reset, PCI reset, and software EEPROM auto-load command in the 9346CR, the RTL8103E(L) performs a series of EEPROM read operations from the 93C46/93C56, Address 00h to 3Fh.

We recommend you obtain Realtek's approval before changing the default settings of the EEPROM.

Table 1. EEPROM (93C46/93C56) Contents

Bytes	Contents	Description
00h	29h	These 2 Bytes Contain ID Code Words for the RTL8103E(L).
01h	81h	The RTL8103E(L) will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are '10ECh' and '8136h'.
02h-03h	VID	PCI Vendor ID. PCI configuration space offset 00h-01h.
04h-05h	DID	PCI Device ID. PCI configuration space offset 02h-03h.
06h-07h	SVID	PCI Subsystem Vendor ID. PCI configuration space offset 2Ch-2Dh.
08h-09h	SMID	PCI Subsystem ID. PCI configuration space offset 2Eh-2Fh.
0Ah	BAR2	PCI BAR2[7:0]. PCI configuration space offset 18h. 04h for 64-bit MEM 00h for 32-bit MEM 0Ch for 64-bit prefetchable MEM
0Bh	BAR0	PCI BAR0[7:0]. PCI configuration space offset 10h. 01h for IO.
0Ch	CONFIG2	RTL8103E(L) Configuration Register 2. MAC register offset 53h.
0Dh	CONFIG3	RTL8103E(L) Configuration Register 3. MAC register offset 54h.
0Eh-13h	Ethernet ID	Ethernet ID. After an auto-load command or hardware reset, the RTL8103E(L) loads the Ethernet ID to IDR0-IDR5 of the RTL8103E(L)'s I/O registers.
14h	CONFIG0	RTL8103E(L) Configuration Register 0. MAC registers offset 51h.
15h	CONFIG1	RTL8103E(L) Configuration Register 1. MAC registers offset 52h.
16h-17h	PMC	Do Not Change This Field Without Realtek Approval. Power Management Capabilities. PCI configuration space addresses 42h and 43h.

Bytes	Contents	Description
18h	CONFIG4	RTL8103E(L) Configuration Register 5. MAC registers offset 55h.
19h	CONFIG5	Reserved. Do not change this field without Realtek approval. RTL8103E(L) Configuration register 4. MAC registers offset 56h.
1Ah	Express Device Capability	PCIE Configuration Space Offset 74h.
1Bh		PCIE Configuration Space Offset 75h.
1Ch	MSI Capability	PCIE Configuration Space Offset 52h.
1Dh	PCI Express Capability	PCIE Configuration Space Offset 73h.
1Eh	PCI Express Link Control	PCIE Configuration Space Offset 80h.
1Fh		PCIE Configuration Space Offset 81h.
20h	PCI Express Link Capability	PCIE Configuration Space Offset 7Ch.
21h		PCIE Configuration Space Offset 7Dh.
22h		PCIE Configuration Space Offset 7Eh.
23h		PCIE Configuration Space Offset 7Fh.
24h	PCI Express Link Device Control	PCIE Configuration Space Offset 78h.
25h		PCIE Configuration Space Offset 79h.
26h~2Bh	PCI Express Parameter	Realtek Internal Use. Do not change this field without Realtek approval.
2Ch	ROMBAR	PCIE Configuration Space Offset 30h.
2Dh~31h	PCI Express Parameter	Realtek Internal Use. Do not change this field without Realtek approval.
32h-33h	-	Reserved.
34h~3Eh	PCI Express Parameter	Realtek Internal Use. Do not change this field without Realtek approval.
3Fh	PXE_Para	Reserved. Do not change this field without Realtek approval. PXE ROM code parameter.
40h~49h	PCI Express Parameter	Realtek Internal Use. Do not change this field without Realtek approval.
4Ah-51h	PCI Express Serial Number registers	PCIE Configuration Space Offset 164h-16Bh.
52h-56h	PCI Express Parameter	Realtek Internal Use. Do not change this field without Realtek approval.

2. PG Tool eFUSE Configuration File Contents

The RTL8103E(L) features embedded configurable 2K-bit eFUSE One-Time-Programmable (OTP) memory. The eFUSE interface permits the RTL8103E(L) to read from, and write data to, an internal eFUSE.

Values in the internal eFUSE allow default fields in PCI configuration space and I/O space to be overridden. Following a power-on reset or software EEPROM/eFUSE auto-load command, the RTL8103E(L) will auto-load values from the eFUSE.

If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8103E(L) initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the eFUSE using 'bit-bang' accesses via the eFUSE Access Register.

We recommend you obtain Realtek's approval before changing the default settings of the eFUSE.

Table 2. eFUSE CFG Contents

Contents	Description
NODEID	Ethernet ID. After auto-load command or hardware reset, the RTL8103E(L) loads Ethernet ID to IDR0-IDR5 of the RTL8103E(L)'s I/O registers.
VID	PCI Vendor ID. PCI configuration space offset 00h-01h.
DID	PCI Device ID. PCI configuration space offset 02h-03h.
SVID	PCI Subsystem Vendor ID. PCI configuration space offset 2Ch-2Dh.
SMID	PCI Subsystem ID. PCI configuration space offset 2Eh-2Fh.
CONFIG0	RTL8103E(L) Configuration Register 0. MAC registers offset 51h.
CONFIG1	RTL8103E(L) Configuration Register 1. MAC registers offset 52h.
CONFIG2	RTL8103E(L) Configuration Register 2. MAC register offset 53h.
CONFIG3	RTL8103E(L) Configuration Register 3. MAC register offset 54h.
CONFIG4	RTL8103E(L) Configuration Register 5. MAC registers offset 55h.
CONFIG5	Reserved. Do not change this field without Realtek approval. RTL8103E(L) Configuration register 4: MAC registers offset 56h.
PMC	Reserved. Do not change this field without Realtek approval. Power Management Capabilities. PCI configuration space addresses 42h and 43h.
ROMBAR	PCIE Configuration Space Offset 30h.
ROMCONF	Reserved. Do not change this field without Realtek approval. PXE ROM code parameter. 20h for enable and 00h for disable PXE code.
LEDCFG	RTL8103E(L) LED Configuration Register. MAC registers offset 18h and 19h.
SN	PCIE Configuration Space Offset 164h-16Bh.

3. EEPROM & eFUSE Related Ethernet MAC Registers

Table 3. EEPROM & eFUSE Related Ethernet MAC Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0–IDR5	RW	-	-	-	-	-	-	-	-
51h	CONFIG0	R	-	-	-	-	-	BS2	BS1	BS0
		W	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	-	Speed_down	-	-	-	-
		W	LEDS1	LEDS0	-	Speed_down	-	-	-	-
53h	CONFIG2	R	-	-	-	-	-	led_lp_en	lanwake_dly_en	-
		W	-	-	-	-	-	led_lp_en	lanwake_dly_en	-
54h	CONFIG3	R	-	VPDSel	Magic	LinkUp	-	Jumbo_en0	-	-
		W	-	VPDSel	Magic	LinkUp	-	Jumbo_en0	-	-
55h	CONFIG4	R	-	-	-	-	-	-	Jumbo_en1	-
		W	-	-	-	-	-	-	Jumbo_en1	-
56h	CONFIG5	R	-	BWF	MWF	UWF	-	-	LANWake	-
		W	-	BWF	MWF	UWF	-	-	LANWake	-

3.1. 9346CR: 93C46 (93C56) Command (Offset 0050h, RW)

Table 4. 9346CR: 93C46 (93C56) Command (Offset 0050h, RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
<tr><td>7:6</td><td>EEM1-0</td><td>RW</td><td>Operating Mode: These 2 bits select the RTL8102E/RTL8102EL operating mode.
Note: The RTL8102EL supports only 93C46.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (RTL8102E/RTL8102EL network/host communication mode)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-Load.
Entering this mode will make the RTL8102E/RTL8102EL load the contents of the 93C46 (93C56) when the PCI RSTB signal is asserted. Autoload_en bit (9346CR bit5) must be ‘1’ before RTL8102E/RTL8102EL enters this mode, so set this byte to 60h when software auto-loads.
This auto-load operation will take about 2ms. After it is completed, the RTL8102E/RTL8102EL goes back to normal mode automatically (EEM1 = 0, EEM0 = 0) and all other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) Programming.
In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config Register Write Enable.
Before writing to CONFIGx and IDx registers, the RTL8102E/RTL8102EL must be placed in this mode. This will prevent RTL8102E/RTL8102EL configurations from being accidentally changed.</td></tr>
</table></td></tr>
<tr><td>5</td><td>Autoload_en</td><td>RW</td><td>Setting this bit to 1 when there is a software autoload action (EEM1 = 0, EEM0 = 1).</td></tr>
<tr><td>4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>EECS</td><td>RW</td><td rowspan="4">These bits reflect the state of the EECS, EESK, EEDI, and EEDO pins in auto-load or 93C46 (93C56) programming mode, and are valid only when the Flash bit is cleared.
Note: EESK, EEDI, and EEDO are valid after boot ROM complete.</td></tr>
<tr><td>2</td><td>EESK</td><td>RW</td></tr>
<tr><td>1</td><td>EEDI</td><td>RW</td></tr>
<tr><td>0</td><td>EEDO</td><td>R</td></tr>
</table>

3.2. CONFIG 0 (Offset 0051h, RW)

Table 5. CONFIG 0 (Offset 0051h, RW)

Bit	Symbol	RW	Description
7	Bootrom_pgact	RW	When set to 1, the SPI flash can be directly accessed via bit 6~3, which now reflects the states of SPICSB, SPISK, SPIDI, and SPIDO pins respectively.
6	P_SPICS	RW	These bits reflect the state of the SPICSB, SPISK, SPIDI and SPIDO pins when bootrom_pgact is set to 1.
5	P_SPISCK	RW	
4	P_SPISI	RW	
3	P_SPISO	R	
2:0	BS2, BS1, BS0	R	Select Boot ROM Size.

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	Reserved
1	1	1	Reserved

Note: Only the RTL8103E has this function.

3.3. CONFIG 1 (Offset 0052h, RW)

Table 6. CONFIG 1 (Offset 0052h, RW)

Bit	Symbol	RW	Description
7:6	LEDS1-0	RW	Refer to the RTL8103E(L) datasheet for a detailed LED pin description. The initial value of these bits comes from the 93C46/93C56.
5	-	-	Reserved.
4	Speed_down	RW	Speed Down Enable. 0: Link speed will stay at 100Mbps when the isolateb pin is low 1: Link speed changes from 100Mbps to 10Mbps when the isolateb pin is low
3	MEMMAP	R	Memory Mapping. The operational registers are mapped into PCI memory space. Always 1.
2	IOMAP	R	I/O Mapping. The operational registers are mapped into PCI I/O space. Always 1.
1	VPD	R	Vital Product Data. Set to enable Vital Product Data. Always 1.
0	PMEn	R	Power Management Enable. Always 1.

3.4. CONFIG 2 (Offset 0053h, RW)

Table 7. CONFIG 2 (Offset 0053h, RW)

Bit	Symbol	RW	Description
7:5	-	-	Reserved.
4	Aux_Status	R	Auxiliary Power Present Status. 1: Aux. Power is present 0: Aux. Power is absent The value of this bit is fixed after each PCI reset.
3	-	-	Reserved.
2	led_lp_en	RW	LED Low Power Enable. 1: LEDs are disabled except D0 state 0: LEDs are enabled in all power management states
1	lanwake_dly_en	RW	Lanwakeb Pin Delay Enable. 1: The lanwakeb pin is pulled low after 0.5s when the RTL8103E(L) receives a WOL packet 0: The lanwakeb pin is pulled low immediately the RTL8103E(L) receives a WOL packet
0	-	-	Reserved.

3.5. CONFIG 3 (Offset 0054h, RW)

Table 8. CONFIG 3 (Offset 0054h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved.
6	VPDSel	RW	Vital Product Data Offset Select. 1'b0 (default): VPD address start point = 60h 1'b1: VPD address start point = 00h
5	Magic	RW	Magic Packet. This bit is valid when the PMEn bit of the CONFIG1 register is set. The RTL8103E(L) will assert the PMEB signal to wakeup the operating system when a Magic Packet is received. Once the RTL8103E(L) has been enabled for Magic Packet wakeup, it scans all incoming packets addressed to the node for a specific data sequence that indicates to the controller that this is a Magic Packet. A Magic Packet must also meet the basic requirements of: Destination address + Source address + data + CRC. The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of a 6-byte ID register, with no breaks nor interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE MAC address match the address of the ID register. If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the Magic frame looks like the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4	LinkUp	RW	Link Up. This bit is valid when the PMEn bit of the CONFIG1 register is set. The RTL8103E(L), in an adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is reestablished.
3:0	-	-	Reserved.

3.6. CONFIG 4 (Offset 0055h, RW)

Table 9. CONFIG 4 (Offset 0055h, RW)

Bit	Symbol	RW	Description
7:5	-	-	Reserved.
4	Isolate_disable_LAN	RW	1: Enable 0: Disable
3:0	-	-	Reserved.

3.7. CONFIG 5 (Offset 0056h, RW)

Table 10. CONFIG 5 (Offset 0056h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved.
6	BWF	RW	Broadcast Wakeup Frame. 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF 0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only the DID field = FF FF FF FF FF FF The power-on default value of this bit is 0.
5	MWF	RW	Multicast Wakeup Frame. 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only the DID field, which is a multicast address The power-on default value of this bit is 0.
4	UWF	RW	Unicast Wakeup Frame. 1: Enable Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address The power-on default value of this bit is 0.
3:2	-	-	Reserved.
1	LANWake	RW	LANWake Signal Enable/Disable. 1: Enable LANWake signal 0: Disable LANWake signal
0	-	-	Reserved.

4. EEPROM & eFUSE Related Power Management Registers

Table 11. EEPROM & eFUSE Related Power Management Registers

Configuration Space Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

4.1. PCI Configuration Space Table

Table 12. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	IntDisable	0	SERREN
		W	-	-	-	-	-	IntDisable	-	SERREN
06h	Status	R	0	0	0	1	IntSt	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	0	0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	1	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	CLS7	CLS6	CLS5	CLS4	CLS3	CLS2	CLS1	CLS0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		RW	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		RW	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		RW	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h~17h	Reserved									
18h	MEM 64 BAR	R	MEM7	0	0	0	MEMPF	MEMLOC	MEMLOC	MEMIN
19h		RW	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
1Ah		RW	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
1Bh		RW	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
1Ch		RW	MEM39	MEM38	MEM37	MEM36	MEM35	MEM34	MEM33	MEM32
1Dh		RW	MEM47	MEM46	MEM45	MEM44	MEM43	MEM42	MEM41	MEM40
1Eh		RW	MEM55	MEM54	MEM53	MEM52	MEM51	MEM50	MEM49	MEM48
1Fh		RW	MEM63	MEM62	MEM61	MEM60	MEM59	MEM58	MEM57	MEM56

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h~27h	Reserved									
28h~2Bh	CISPtr	CardBus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		RW	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h~3Bh	Reserved									
3Ch	ILR	RW	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	1	0	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
45h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
46~4Fh	Reserved									
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	1	0	0	0	0
52h	Message Control	R	64-bit Address Capable	Multiple Message Enable			0	0	0	MSI Enable
		W	-	Multiple Message Enable			-	-	0	MSI Enable
53h		Reserved. Always return 0								
54h~57h	Message Address Low	RW	64-bit Interrupt Message Address Low							
58h~5Bh	Message Address High	RW	64-bit Interrupt Message Address High							
5Ch~5Dh	Message Data	RW	16-bit Message Data							
5E~6Fh	Reserved									
70h	PCIEID	R	0	0	0	1	0	0	0	0
71h	NextPtr	R	1	0	1	1	0	0	0	0
72h~73h	PCIE Cap.	R	0	0	0	Legacy	0	0	0	1
		R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74h~77h	Device Capability Register	R	L0s_acpt_latency[1]	L0s_acpt_latency[0]	Entend_tag_support	0	0	Max_payload_size_support		
		R	Role Base Error rpt	0	0	0	L1_acpt_latency[2]	L1_acpt_latency[1]	L1_acpt_latency[0]	L0s_acpt_latency[2]
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
78h~79h	Device Control Register	RW	Max_payload_size			Relaxed_ordering_en	Unsupport_rqst_rpt_en	Fatal_err_rpt_en	Non_fatal_err_rpt_en	Correct-able_err_rpt_en
		RW	0	Max_read_request_size			No_snoop_en	Auxpwr_PM_en	0	Entend_tag_en
7Ah	Device Status Register	R	0	0	Transaction_pending	AuxPwr_det	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correct-able_err_det
		W	0	0	-	-	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correct-able_err_det
7Bh		R	0	0	0	0	0	0	0	0
7Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
7Dh		R	L1_exit_lat[0]	L0s_exit_lat[2]	L0s_exit_lat[1]	L0s_exit_lat[0]	ASPM_support		0	0
7Eh		R	0	0	0	0	0	Clock_PM	L1_exit_lat[2]	L1_exit_lat[1]0
7Fh		R	0	0	0	0	0	0	0	0
80h	Link Control Register	R	Extended_sync	Common_clock	0	0	RCB	0	ASPM_control	
		W	Extended_sync	Common_clock	0	0	RCB	0	ASPM_control	
81h		R	0	0	0	0	0	0	0	Enable clock_PM
		W	0	0	0	0	0	0	0	Enable clock_PM
82h	Link Status Register	R	0	0	0	1	0	0	0	1
83h		R	0	0	0	Slot_clock_cfg	0	0	0	0
84h	Slot Capability Register	R	Slot power Limit[0]	Hot-Plug Capable	Hot-Plug Surprise	Power Indicator Present	Attn Indicator Present	MRL Sensor Present	Power Control Present	Attn Bottom Present
85h		R	Slot Power Limit scale[0]	Slot Power Limit[7]	Slot Power Limit[6]	Slot Power Limit[5]	Slot Power Limit[4]	Slot Power Limit[3]	Slot Power Limit[2]	Slot Power Limit[1]
86h		R	Physical Slot Number[4]	Physical Slot Number[3]	Physical Slot Number[2]	Physical Slot Number[1]	Physical Slot Number[0]	No Common Complete Support	Electromech-anical Interlock Present	Slot Power Limit Scale[1]
87h		R	Physical Slot Number[12]	Physical Slot Number[11]	Physical Slot Number[10]	Physical Slot Number[9]	Physical Slot Number[8]	Physical Slot Number[7]	Physical Slot Number[6]	Physical Slot Number[5]
88h	Slot Control Register	RW	Attn Indicator Control[1]	Attn Indicator Control[0]	Hot-Plug Interrupt Enable	Command Completed Interrupt Enable	Presence Detect Changed Enable	MRL Sensor Changed Enable	Power Fault Detected Enable	Attn Button Pressed Enable
89h		RW	-	-	-	Data Link Layer State Changed Enable	Electromecha nical Interlock Control	Power Controller Control	Power Indicator Control[1]	Power Indicator Control[0]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ah	Slot Status Register	R	Electro-mechanical Interlock Status	Presence Detect State	MRL Sensor State	Command Completed	Presence Detect Changed	MRL Sensor Changed	Power Fault Detected	Attn Button Pressed
8Bh		R	Reserved							Data Link Layer State Changed
8Ch~AFh	Reserved									
B0h	MSI-X ID	R	0	0	0	1	0	0	0	1
B1h	NextPtr	R	1	1	0	1	0	0	0	0
B2h		R	MSI-X Table _Size[7]	MSI-X Table _Size[6]	MSI-X Table _Size[5]	MSI-X Table _Size[4]	MSI-X Table _Size[3]	MSI-X Table _Size[2]	MSI-X Table _Size[1]	MSI-X Table _Size[0]
B3h		R	MSI-X Enable	Function Mask	Reserved			MSI-X Table _Size[10]	MSI-X Table _Size[9]	MSI-X Table _Size[8]
B4h	MSI-X Table Offset and BIR Register	R	Table Offset[4]	Table Offset[3]	Table Offset[2]	Table Offset[1]	Table Offset[0]	BIR[2]	BIR[1]	BIR[0]
B5h		R	Table Offset[12]	Table Offset[11]	Table Offset[10]	Table Offset[9]	Table Offset[8]	Table Offset[7]	Table Offset[6]	Table Offset[5]
B6h		R	Table Offset[20]	Table Offset[19]	Table Offset[18]	Table Offset[17]	Table Offset[16]	Table Offset[15]	Table Offset[14]	Table Offset[13]
B7h		R	Table Offset[28]	Table Offset[27]	Table Offset[26]	Table Offset[25]	Table Offset[24]	Table Offset[23]	Table Offset[22]	Table Offset[21]
B8h	MSI-X PBA Offset and BIR	R	PBA Table Offset[4]	PBA Table Offset[3]	PBA Table Offset[2]	PBA Table Offset[1]	PBA Table Offset[0]	PBA BIR[2]	PBA BIR[1]	PBA BIR[0]
B9h		R	PBA Table Offset[12]	PBA Table Offset[11]	PBA Table Offset[10]	PBA Table Offset[9]	PBA Table Offset[8]	PBA Table Offset[7]	PBA Table Offset[6]	PBA Table Offset[5]
BAh		R	PBA Table Offset[20]	PBA Table Offset[19]	PBA Table Offset[18]	PBA Table Offset[17]	PBA Table Offset[16]	PBA Table Offset[15]	PBA Table Offset[14]	PBA Table Offset[13]
BBh		R	PBA Table Offset[28]	PBA Table Offset[27]	PBA Table Offset[26]	PBA Table Offset[25]	PBA Table Offset[24]	PBA Table Offset[23]	PBA Table Offset[22]	PBA Table Offset[21]
BCh~CFH	Reserved									
D0h	VPDID	R	0	0	0	0	0	0	1	1
D1h	NextPTR	R	0	0	0	0	0	0	0	0
D2h	Flag VPD Address	RW	VPD ARRD7	VPD ARRD6	VPD ARRD5	VPD ARRD4	VPD ARRD3	VPD ARRD2	VPD ARRD1	VPD ARRD0
D3h		RW	Flag	VPD ARRD14	VPD ARRD13	VPD ARRD12	VPD ARRD11	VPD ARRD10	VPD ARRD9	VPD ARRD8
D4h	VPD Data	RW	VPD Data7	VPD Data6	VPD Data5	VPD Data4	VPD Data3	VPD Data2	VPD Data1	VPD Data0
D5h		RW	VPD Data15	VPD Data14	VPD Data13	VPD Data12	VPD Data11	VPD Data10	VPD Data9	VPD Data8
D6h		RW	VPD Data23	VPD Data22	VPD Data21	VPD Data20	VPD Data19	VPD Data18	VPD Data17	VPD Data16
D7h		RW	VPD Data31	VPD Data30	VPD Data29	VPD Data28	VPD Data27	VPD Data26	VPD Data25	VPD Data24
D8h~FFh	Reserved									

5. PXE Parameters

Table 13. PXE Parameters

Bit	Symbol	RW	Description
7-6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5-4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3	Show Config Message	RW	0: Enable 1: Disable
2	Shift+F10 Menu Entry	RW	0: Enable 1: Disable
1-0	Show Config Time	RW	00: 3 Seconds 01: 5 Seconds 10: 1 Second 11: 0 Seconds

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com