



REALTEK

RTL8393M-VC-CG

LAYER 2 + MANAGED 52 10/100/1000M-PORT SWITCH CONTROLLER

PRELIMINARY DATASHEET (CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8393M IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Table of Contents

| | |
|---|----|
| 1. GENERAL DESCRIPTION | 1 |
| 2. FEATURES | 2 |
| 3. BLOCK DIAGRAM | 5 |
| 3.1. RTL8393M (48G + 4G COMBO) BLOCK DIAGRAM | 5 |
| 3.2. RTL8393M (48G + 2 SGMII) BLOCK DIAGRAM | 6 |
| 4. SYSTEM APPLICATIONS | 7 |
| 4.1. 48 10/100/1000BASE-T + 4 COMBO 10/100/1000BASE-T/SFP | 7 |
| 4.2. 48 10/100/1000BASE-T + 2 SGMII (OR 100/1000BASE-FX) | 8 |
| 5. PIN ASSIGNMENTS | 9 |
| 5.1. RTL8393M (48G + 4G COMBO) PIN LAYOUT | 9 |
| 5.2. RTL8393M (48G + 2 SGMII) PIN LAYOUT | 10 |
| 5.3. RTL8393M (48G + 4G COMBO) PIN ASSIGNMENTS (TOP VIEW) | 11 |
| 5.4. RTL8393M (48G + 2 SGMII) PIN ASSIGNMENTS (TOP VIEW) | 13 |
| 5.5. PIN ASSIGNMENTS TABLE DEFINITIONS | 15 |
| 5.6. RTL8393M(48G + 4G COMBO) PIN ASSIGNMENTS TABLE | 15 |
| 5.7. RTL8393M(48G + 2 SGMII) PIN ASSIGNMENTS TABLE | 20 |
| 6. PIN DESCRIPTIONS | 25 |
| 6.1. DDR3 SDRAM INTERFACE | 25 |
| 6.2. SPI MASTER INTERFACE | 26 |
| 6.3. UART INTERFACE | 26 |
| 6.4. EJTAG INTERFACE | 27 |
| 6.5. GPIO INTERFACE | 27 |
| 6.6. SGMI INTERFACE | 28 |
| 6.7. 100/1000BASE-FX INTERFACE | 28 |
| 6.8. QSGMII INTERFACE | 29 |
| 6.9. LED INTERFACE | 29 |
| 6.10. SPI SLAVE INTERFACE | 29 |
| 6.11. EEPROM SMI SLAVE INTERFACE | 30 |
| 6.12. MISCELLANEOUS INTERFACE | 30 |
| 6.13. CONFIGURATION (PIN STRAPPING FUNCTION) | 31 |
| 6.14. POWER AND GND | 32 |
| 7. SWITCH FUNCTION DESCRIPTION | 34 |
| 7.1. HARDWARE RESET AND SOFTWARE RESET | 34 |
| 7.1.1. Hardware Reset | 34 |
| 7.1.2. Software Reset | 34 |
| 7.2. LAYER 2 LEARNING AND FORWARDING | 34 |
| 7.2.1. Forwarding | 34 |
| 7.2.2. Learning | 35 |
| 7.3. LAYER 2 LEARNING CONSTRAINT | 35 |
| 7.4. PORT ISOLATION | 35 |
| 7.5. LAYER 2 MULTICAST AND IP MULTICAST | 36 |
| 7.6. RESERVED MULTICAST ADDRESS | 36 |
| 7.7. IEEE 802.1Q AND Q-IN-Q VLAN | 37 |
| 7.8. INGRESS AND EGRESS VLAN TRANSLATION | 38 |
| 7.9. IEEE 802.3AD LINK AGGREGATION | 38 |
| 7.10. MIRRORING AND SAMPLING | 38 |

| | | |
|------------|--|-----------|
| 7.11. | ATTACK PREVENTION | 38 |
| 7.12. | PIE (PACKET INSPECTION ENGINE)..... | 39 |
| 7.12.1. | <i>Ingress ACL</i> | 39 |
| 7.12.2. | <i>Egress ACL</i> | 39 |
| 7.12.3. | <i>Log Counter</i> | 39 |
| 7.13. | TRAFFIC SUPPRESSION | 39 |
| 7.13.1. | <i>Input Bandwidth Control</i> | 39 |
| 7.13.2. | <i>ACL Policing</i> | 40 |
| 7.13.3. | <i>Storm Control</i> | 40 |
| 7.14. | PRIORITY DECISION | 40 |
| 7.15. | PACKET SCHEDULING | 41 |
| 7.16. | EGRESS PACKET REMARKING | 41 |
| 7.17. | IEEE 802.3X FLOW CONTROL | 41 |
| 7.18. | HALF DUPLEX BACKPRESSURE | 42 |
| 7.18.1. | <i>Collision-Based Backpressure (Jam Mode)</i> | 42 |
| 7.18.2. | <i>Carrier-Based Backpressure (Defer Mode)</i> | 43 |
| 7.19. | SRTCM/TRTCM (SINGLE/TWO RATE THREE COLOR MARKER)..... | 43 |
| 7.20. | SWRED (SIMPLE WEIGHTED RANDOM EARLY DETECTION)..... | 43 |
| 7.21. | MANAGEMENT INFORMATION BASE (MIB) | 44 |
| 7.22. | NIC AND CPU TAG FORWARDING | 45 |
| 7.23. | TABLE ACCESS | 45 |
| 7.24. | EXTERNAL PHY REGISTER ACCESS | 45 |
| 7.25. | OAM (OPERATION, ADMINISTRATION, MAINTENANCE)..... | 46 |
| 7.26. | IEEE 1588 PTP | 46 |
| 7.27. | EEE | 47 |
| 8. | CPU FUNCTION DESCRIPTION | 48 |
| 8.1. | MIPS-34KC | 48 |
| 8.2. | SPI FLASH CONTROLLER | 48 |
| 8.3. | DDR MEMORY CONTROLLER | 48 |
| 9. | ELECTRICAL AC/DC CHARACTERISTICS..... | 49 |
| 9.1. | ABSOLUTE MAXIMUM RATINGS | 49 |
| 9.2. | OPERATING RANGE..... | 49 |
| 9.3. | DC CHARACTERISTICS | 49 |
| 9.4. | AC CHARACTERISTICS | 50 |
| 9.4.1. | <i>Clock Characteristics</i> | 50 |
| 9.4.2. | <i>QSGMII Differential Transmitter Characteristics</i> | 51 |
| 9.4.3. | <i>QSGMII Differential Receiver Characteristics</i> | 52 |
| 9.4.4. | <i>DDR3 Characteristics</i> | 53 |
| 9.4.5. | <i>SPI Flash Controller Interface Characteristics</i> | 54 |
| 9.4.6. | <i>EJTAG Timing Characteristics</i> | 55 |
| 9.4.7. | <i>SMI (MDC/MDIO) Interface Characteristics</i> | 56 |
| 9.4.8. | <i>LED Timing Characteristics</i> | 57 |
| 9.4.9. | <i>Power and Reset Characteristics</i> | 58 |
| 10. | PACKAGE INFORMATION (EDHS-PBGA388 (27*27))..... | 59 |
| 11. | ORDERING INFORMATION | 60 |

List of Tables

| | |
|--|----|
| TABLE 1. RTL8393M(48G + 4G COMBO) PIN ASSIGNMENTS TABLE..... | 15 |
| TABLE 2. RTL8393M(48G + 2 SGMII) PIN ASSIGNMENTS TABLE | 20 |
| TABLE 3. DDR3 SDRAM INTERFACE PINS..... | 25 |
| TABLE 4. SPI MASTER INTERFACE PINS | 26 |
| TABLE 5. UART INTERFACE PINS | 26 |
| TABLE 6. EJTAG INTERFACE PINS | 27 |
| TABLE 7. GPIO INTERFACE PINS | 27 |
| TABLE 8. SGMII INTERFACE PINS | 28 |
| TABLE 9. 100/1000BASE-FX INTERFACE PINS..... | 28 |
| TABLE 10. QSGMII INTERFACE PINS..... | 29 |
| TABLE 11. LED INTERFACE PINS | 29 |
| TABLE 12. SPI SLAVE INTERFACE PINS..... | 29 |
| TABLE 13. EEPROM SMI SLAVE INTERFACE PINS | 30 |
| TABLE 14. MISCELLANEOUS INTERFACE PINS..... | 30 |
| TABLE 15. CONFIGURATION STRAPPING PINS | 31 |
| TABLE 16. POWER AND GND PINS..... | 32 |
| TABLE 17. ABSOLUTE MAXIMUM RATINGS | 49 |
| TABLE 18. RECOMMEND OPERATING RANGE..... | 49 |
| TABLE 19. DC CHARACTERISTICS FOR 48G+4G | 49 |
| TABLE 20. DC CHARACTERISTICS FOR 48G+2SGMII..... | 49 |
| TABLE 21. DC CHARACTERISTICS (DVDD33=3.3V)..... | 50 |
| TABLE 22. XTAL1 (XI) CHARACTERISTICS..... | 50 |
| TABLE 23. QSGMII DIFFERENTIAL TRANSMITTER CHARACTERISTICS..... | 51 |
| TABLE 24. QSGMII DIFFERENTIAL RECEIVER CHARACTERISTICS | 52 |
| TABLE 25. DDR3 TIMING CHARACTERISTICS | 53 |
| TABLE 26. SPI FLASH CONTROLLER INTERFACE TIMING CHARACTERISTICS..... | 54 |
| TABLE 27. EJTAG INTERFACE TIMING CHARACTERISTICS | 55 |
| TABLE 28. SMI_0 (MDC/MDIO) TIMING CHARACTERISTICS | 56 |
| TABLE 29. SMI_1 (MDC/MDIO) TIMING CHARACTERISTICS | 56 |
| TABLE 30. SERIAL LED TIMING CHARACTERISTICS | 57 |
| TABLE 31. SCAN BI-COLOR LED TIMING CHARACTERISTICS | 57 |
| TABLE 32. SCAN SINGLE-COLOR LED TIMING CHARACTERISTICS | 57 |
| TABLE 33. POWER AND RESET TIMING CHARACTERISTICS | 58 |
| TABLE 34. ORDERING INFORMATION | 60 |

List of Figures

| | |
|--|----|
| FIGURE 1. RTL8393M (48G + 4G COMBO) BLOCK DIAGRAM..... | 5 |
| FIGURE 2. RTL8393M (48G + 2 SGMII) BLOCK DIAGRAM | 6 |
| FIGURE 3. 48 10/100/1000BASE-T + 4 COMBO 10/100/1000BASE-T/SFP | 7 |
| FIGURE 4. 48 10/100/1000BASE-T + 2 SGMII (OR 100/1000BASE-FX) | 8 |
| FIGURE 5. RTL8393M (48G + 4G COMBO) PIN LAYOUT | 9 |
| FIGURE 6. RTL8393M (48G + 2 SGMII) PIN LAYOUT | 10 |
| FIGURE 7. RTL8393M (48G + 4G COMBO) PIN ASSIGNMENTS (TOP VIEW) | 11 |
| FIGURE 8. RTL8393M (48G + 4G COMBO) PIN ASSIGNMENTS (TOP VIEW) (CONTINUED) | 12 |
| FIGURE 9. RTL8393M (48G + 2 SGMII) PIN ASSIGNMENTS (TOP VIEW) | 13 |
| FIGURE 10. RTL8393M (48G + 2 SGMII) PIN ASSIGNMENTS (TOP VIEW) (CONTINUED) | 14 |
| FIGURE 11. PORT ISOLATION EXAMPLE | 35 |

| | |
|--|----|
| FIGURE 12. SPANNING TREE AND RAPID SPANNING TREE PORT STATES | 37 |
| FIGURE 13. TX PAUSE FRAME FORMAT..... | 42 |
| FIGURE 14. FLOW CONTROL STATE MACHINE | 42 |
| FIGURE 15. SWRED PACKET MARKING PROBABILITY OF DIFFERENT DROP PRECEDENCE | 44 |
| FIGURE 16. NIC ARCHITECTURE | 45 |
| FIGURE 17. OAM DYING GASP APPLICATION CIRCUIT | 46 |
| FIGURE 18. QSGMII DIFFERENTIAL TRANSMITTER EYE DIAGRAM | 51 |
| FIGURE 19. QSGMII DIFFERENTIAL RECEIVER EYE DIAGRAM | 52 |
| FIGURE 20. DDR3 TIMING ILLUSTRATIONS | 53 |
| FIGURE 21. SPI FLASH CONTROLLER INTERFACE TIMING ILLUSTRATIONS | 54 |
| FIGURE 22. EJTAG INTERFACE TIMING ILLUSTRATIONS | 55 |
| FIGURE 23. SMI (MDC/MDIO) TIMING ILLUSTRATIONS | 56 |
| FIGURE 24. LED TIMING ILLUSTRATIONS | 57 |
| FIGURE 25. POWER AND RESET TIMING ILLUSTRATIONS | 58 |

1. General Description

The RTL8393M is a 52-port 10/100/1000M Managed Ethernet MAC Switch Controller. It supports 13 pairs of 5Gbps QSGMII to connect to external 52 ports Gigabit Ethernet PHY transceivers. There are two mode selections in RTL8393M. One is 48 10/100/1000BASE-T + 4 combo 10/100/1000BASE-T/SFP the other one is 48 10/100/1000BASE-T + 2 SGMII (all of “SGMII” can be changed to 100/1000BASE-FX interface in RTL8393M).

The RTL8393M is embedded with a up to 700MHz MIPS-34Kc CPU. It supports a 32-bit data bus, 32M-Byte SPI flash (3-byte mode) or 64MB SPI flash (4-byte mode), and 256M-Byte DDR3 SDRAMs (maximum). It is also embedded a 96KB SRAM can be used for time-sensitive application. For connecting to an external CPU, it supports SGMII interface.

The RTL8393M has a 4K-entry VLAN table. It provides VLAN classification ability according to port-based, protocol-and-port-based, MAC-based, and Flow-based. It also supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning) for flexible network topology architecture. In access network application, it provides IEEE802.1ad (Q-in-Q) for double tag inserted and removed function. In addition, VLAN translation function is also supported for Metro Ethernet application.

RTL8393M supports 16K entries in L2 MAC table with 4-way hashing algorithm. An independent 4K-entry Multicast table is used to support the Multicast function, such as IGMP snooping.

The RTL8393M supports a 2K+256-entry ingress/egress Access Control List (ACL). The ACL function supports L2/L3/L4 in IPv4/Ipv6 protocol and performs configurable actions, such as Drop/ Permit/ Redirect/ Mirror/ Logging/ Policing/ Ingress VLAN conversion/ Egress VLAN conversion/ QoS remarking/ VLAN tag status assignment. The RTL8393M supports per-port ingress/egress bandwidth control and per-queue egress bandwidth control.

The RTL8393M provides three types of packet scheduling, including SP (Strict Priority), WFQ (Weighted Fair Queuing), and WRR (Weighted Round Robin). Each port has 8 physical queues and each queue provides a leaky-bucket to shape the incoming traffic into the average rate behavior. Broadcast/ Multicast/ Unknown-Multicast/ Unknown-Unicast storm suppression function can inhibit external and internal malicious attacks.

The RTL8393M also supports 4-set of port mirror configuration to mirror ingress and egress traffic. RSPAN, sFlow, and IPFIX are also supported for traffic monitor. For network management purposes, complete MIB counters are supported to provide forwarding statistics in real time. Link aggregation function enhanced link redundancy and increased bandwidth linearly.

2. Features

- Hardware Interface
 - ◆ RTL8393M is 104 Gbps switch capacity
 - ◆ RTL8393M supports 13 pairs of 5Gbps QSGMII to 52 ports 10/100/1000M Ethernet PHY
 - ◆ RTL8393M has two mode selections
 - 48 10/100/1000BASE-T + 4 combo 10/100/1000BASE-T/SFP
 - 48 10/100/1000BASE-T + 2 SGMII (SGMII can be changed to 100/1000BASE-FX interface)
 - ◆ Supports flexible interfaces for internal or external CPU, either one can be enabled
 - Maximum 32Mbyte SPI Flash (3-byte mode) or maximum 64Mbyte SPI Flash (4-byte mode) and maximum 256Mbytes DDR3 SDRAMs for internal MIPS-34Kc
 - SGMII (or 100/1000BASE-FX) for connecting external CPU
 - ◆ Supports flash-only solution
 - Single/Dual/Quad SPI flash
 - 96Kbyte SP-SRAM
 - ◆ Embedded MIPS-34Kc with MMU
 - MIPS32 instruction set and 9-stage pipeline
 - Up to 700MHz CPU clock rate
 - 32Kbyte I-Cache and 32Kbyte D-Cache
 - 32 TLB entry
 - Two UART interface to control internal CPU with Command Line Interface (CLI)
 - ◆ External CPU interface
 - Support SGMII interface as external CPU connection
 - Supports EEPROM SMI Slave/SPI interface for external CPU to access internal register
- L2 VLAN Function
 - ◆ Supports IVL, SVL, and IVL/SVL
 - ◆ Supports IEEE 802.1Q VLAN and Q-in-Q VLAN
 - 4K-entry VLAN Table
 - Supports 256 Filtering Database
 - Supports up to 256 spanning tree instances for MSTP (IEEE 802.1s), RSTP, and STP
 - Forwarding bases on inner or outer VLAN
 - Ingress/Egress VLAN filtering per-port based
 - VLAN keep content mode per-ingress-egress-port based
 - ◆ Port-based/Port-and-protocol-based /MAC-based/IP-Subnet-based/Flow-based VLAN
 - ◆ VLAN Conversion Table
 - 1K ingress and 1K egress table
 - Specific VLAN or a VLAN range to convert
 - Shift operation is supported
 - Selective Q-in-Q
- L2 MAC Function
 - ◆ 16K-entry L2 MAC table
 - ◆ 4-way hashing algorithm
 - ◆ 2 hash algorithm selection for L2 table searching/learning
 - ◆ Source/Destination MAC filtering
 - ◆ Per port enables aging
 - ◆ Independent 4K entry Multicast table for L2/IP multicast function
 - ◆ 12Mbit SRAM Packet Buffer
 - ◆ Jumbo frame up to 12KB
 - ◆ Supports IGMPv1/2/3 & MLDv1/2 snooping

- ◆ Supports 48 Reserved Multicast Addresses processing
- ◆ Limited learned L2 MAC entry on Port/VLAN/System
- ◆ MAC address Aging-out and New-learn notification
- L2 Miscellaneous Functions
 - ◆ Supports broadcast/ multicast/ unknown-multicast/ unicast/ unknown-unicast packet suppression control in pps/bps mode
 - ◆ Supports Port Mirroring/Sampling
 - Supports 4 sets of mirror configuration
 - Supports good packet, bad packet, unicast packet, and multicast packet mirror filter
 - Support flow-based mirror
 - RSPAN mirror
 - sFlow and IPFIX
 - ◆ Supports Link Aggregation (IEEE 802.3ad) for 16 groups of link aggregators with up to 8 ports per group
 - Hardware trunk fail-over
 - Distribution algorithm can base on SPA/DMAC/SMAC/ DIP/SIP/DPORT/SPORT
 - Known multicast/flooding packet can be separated
 - ◆ Port isolation function to enhance port security
 - ◆ Attack Prevention
 - LAND attack
 - Blat attack
 - TCP control flag attack
 - Ping attack
 - Packet length attack
 - ◆ OAM
 - 802.3ah OAM loopback
 - 802.3ah Dying Gasp
 - 802.1ag CFM fault detection
 - Y.1731 Ethernet delay measurement
- L3 Function
 - ◆ Ipv4/Ipv6 unicast routing
 - ◆ Layer 3 VPN – Ipv4/Ipv6 over MPLS
- Access Control List (ACL) Function
 - ◆ Supports 2K+256 shared entry for ingress and egress ACL
 - ◆ Supports L2/L3/L4 format and user defined field
 - ◆ Supports 512 leaky-buckets for traffic policing/srTCM/trTCM
 - ◆ Supports 2K 32-bit packet-based or 1K 64-bit byte-based log counters to enhance MIB counter
 - ◆ Supports action to Drop/ Permit/ Redirect/ Mirror/ Logging/ Policing/ Ingress VLAN conversion/ Egress VLAN conversion/ QoS remarking/ VLAN tag status assignment
 - ◆ Range Check
 - VLAN
 - Ipv4/Ipv6 SIP/DIP
 - L4 SPORT/DPORT
 - Packet Length
- QoS Functions
 - ◆ 8 physical queues each port
 - ◆ Priority Assignment based on IEEE 802.1P priority, DSCP value, physical port number, DMAC-based, SMAC-based, Ether-Type-based, CVID, SVID, Ipv4 SIP, Ipv4 DIP, Ipv4/Ipv6 TOS field, Ipv6 Flow Label, TCP/UDP source/destination port
 - ◆ Strict Priority (SP) and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
 - ◆ QoS remarking for 802.1p and DSCP (includes Ipv4/Ipv6)

- ◆ Supports average packet rate control leaky-bucket per queue with 16Kbps steps from 16Kbps to 1Gbps
- ◆ Supports ingress and egress port bandwidth control with 16Kbps steps from 16Kbps to 1Gbps
- ◆ Simple Weighted Random Early Drop (SWRED) to prevent TCP Global Synchronization
- ◆ Ethernet AV
 - IEEE 1588v2 supported by RTL8218B
 - IEEE 802.1Qav
- Power Saving Function
 - ◆ Support IEEE 802.3az EEE
- MIB Functions
 - ◆ MIB-II (RFC 1213)
 - ◆ Ethernet-like MIB (RFC 3635)
 - ◆ Interface Group MIB (RFC 2863)
 - ◆ RMON (RFC 2819)
 - ◆ Bridge MIB (RFC 1493)
 - ◆ Bridge MIB Extension (RFC 2674)
- Others
 - ◆ 55nm CMOS process
 - ◆ 3.3V/1.1V power input
 - ◆ 1.5V for DDR3
 - ◆ EDHS-PBGA 388 package

3. Block Diagram

3.1. *RTL8393M (48G + 4G combo) Block Diagram*

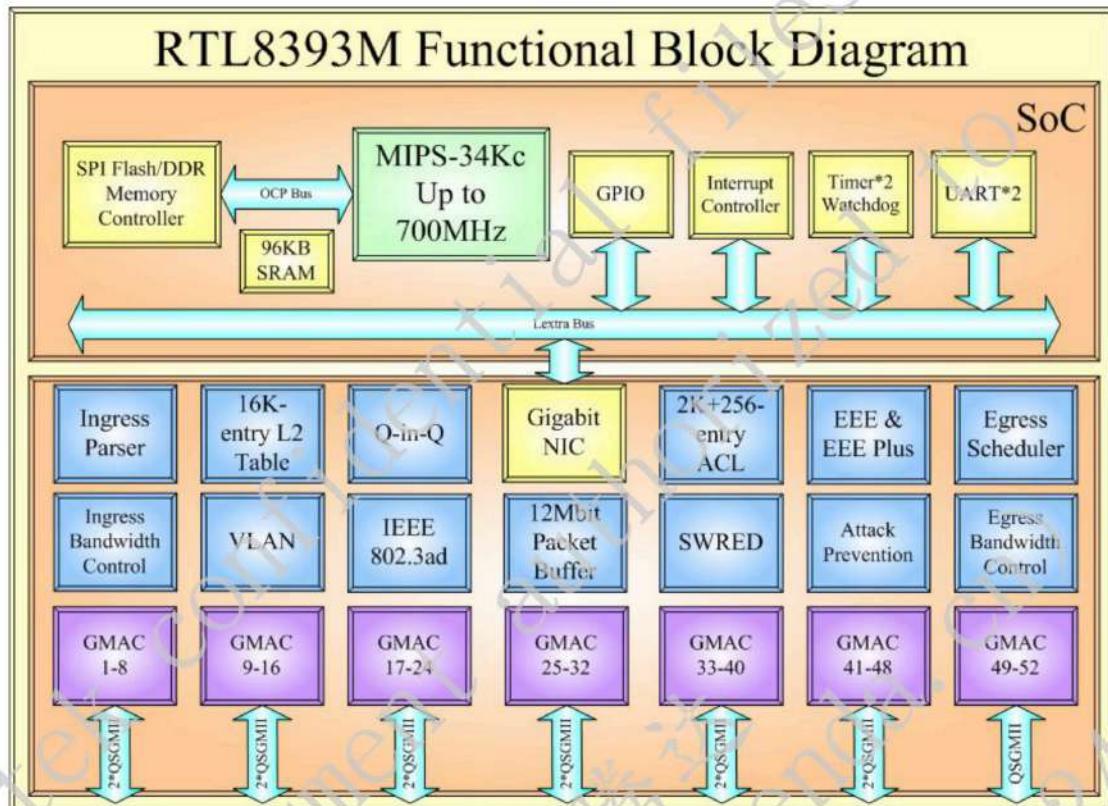


Figure 1. **RTL8393M (48G + 4G combo) Block Diagram**

3.2. RTL8393M (48G + 2 SGMII) Block Diagram

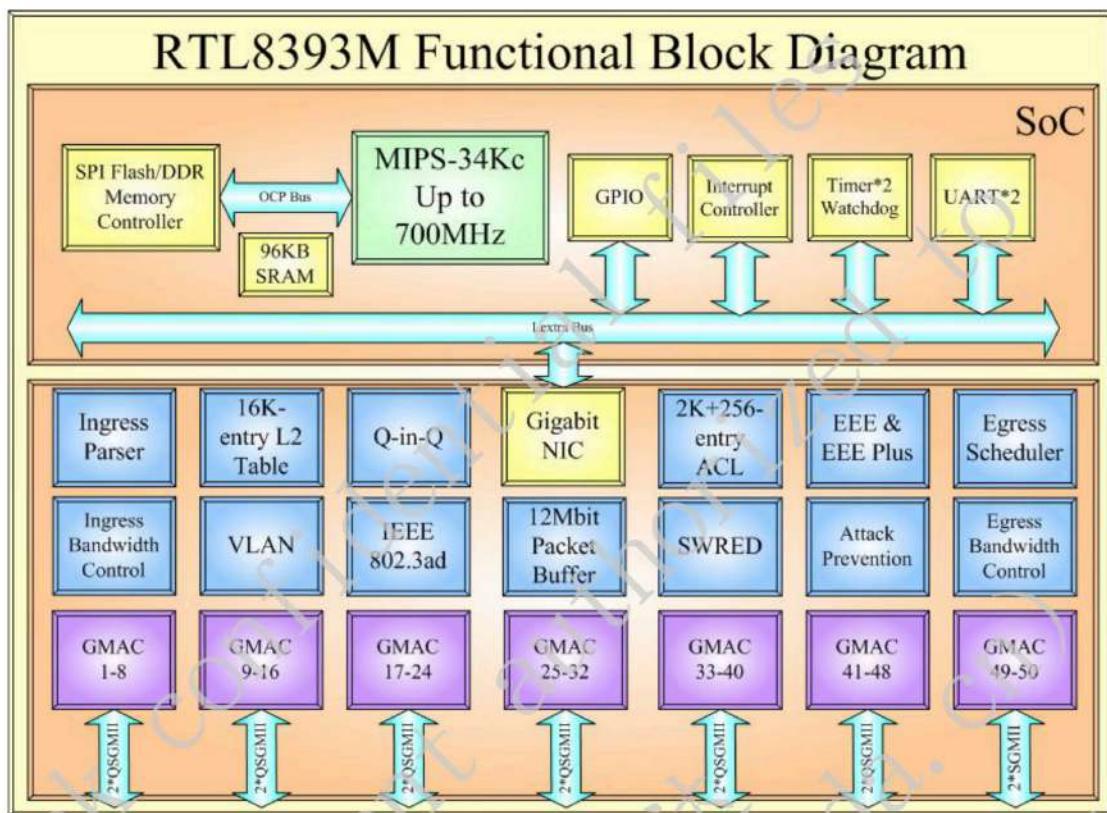


Figure 2. RTL8393M (48G + 2 SGMII) Block Diagram

4. System Applications

4.1. 48 10/100/1000BASE-T + 4 combo 10/100/1000BASE-T/SFP

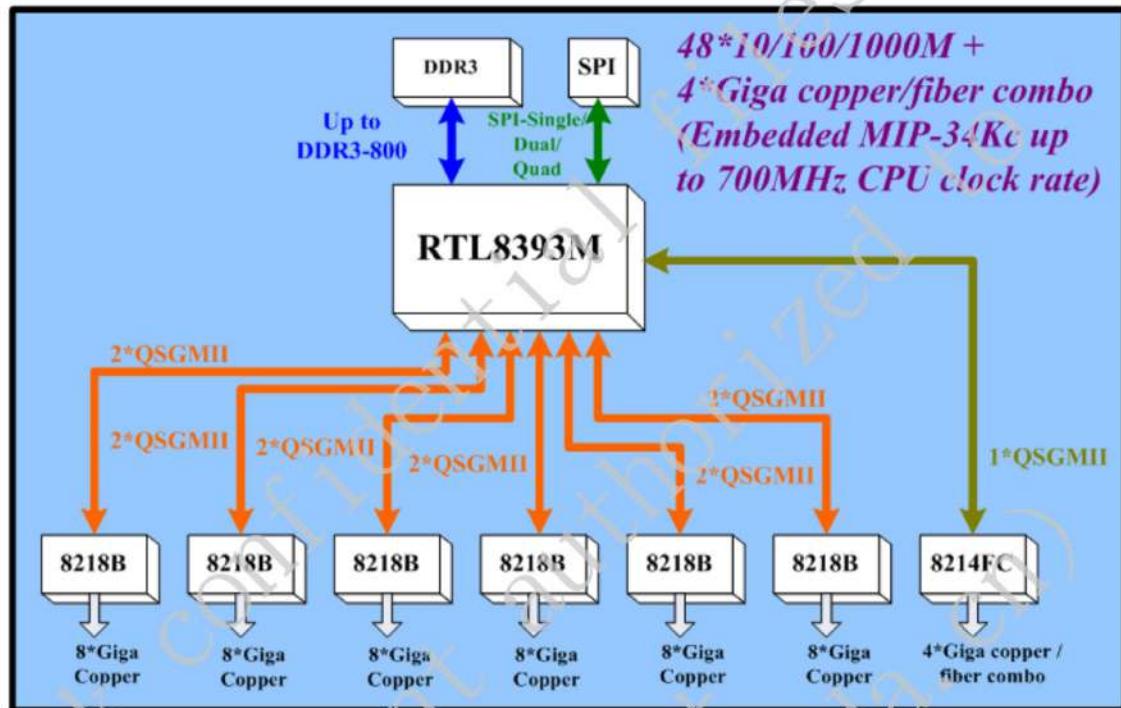


Figure 3. 48 10/100/1000BASE-T + 4 combo 10/100/1000BASE-T/SFP

4.2. 48 10/100/1000BASE-T + 2 SGMII (or 100/1000BASE-FX)

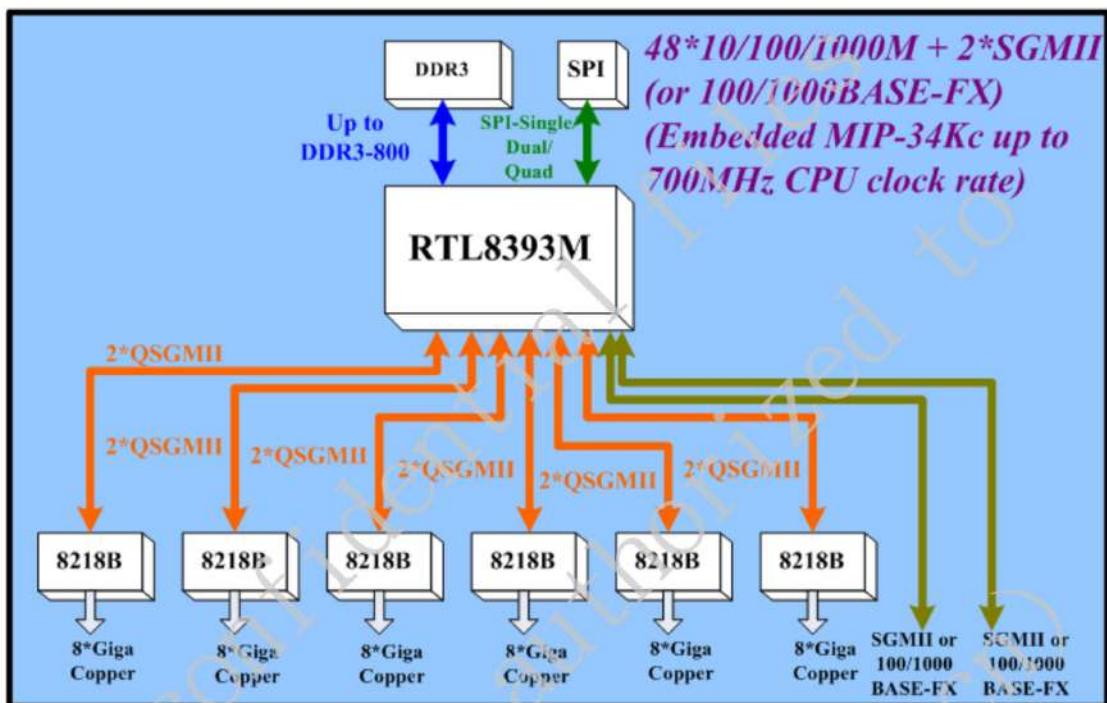


Figure 4. 48 10/100/1000BASE-T + 2 SGMII (or 100/1000BASE-FX)

5. Pin Assignments

5.1. RTL8393M (48G + 4G combo) Pin Layout

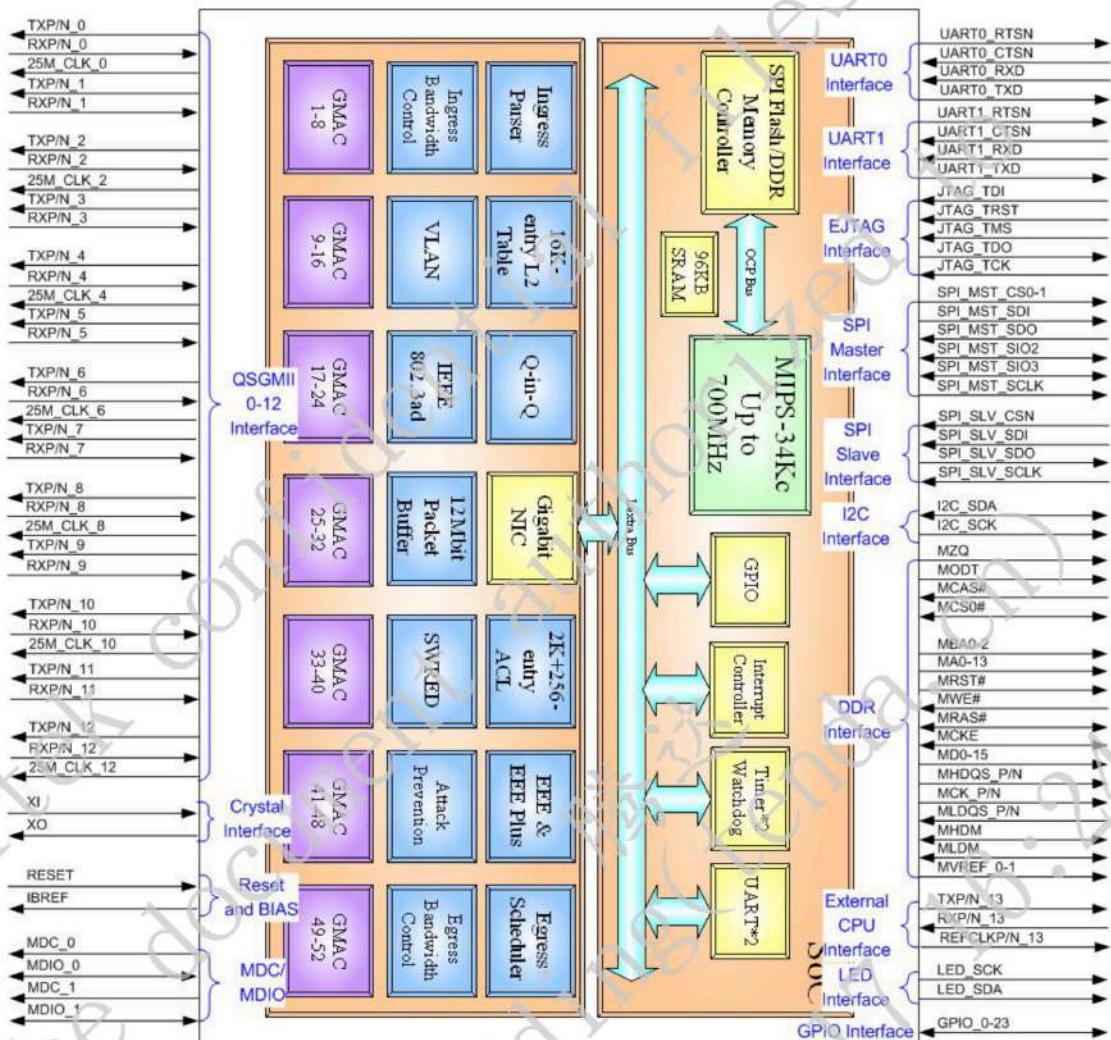


Figure 5. RTL8393M (48G + 4G combo) Pin Layout

5.2. RTL8393M (48G + 2 SGMII) Pin Layout

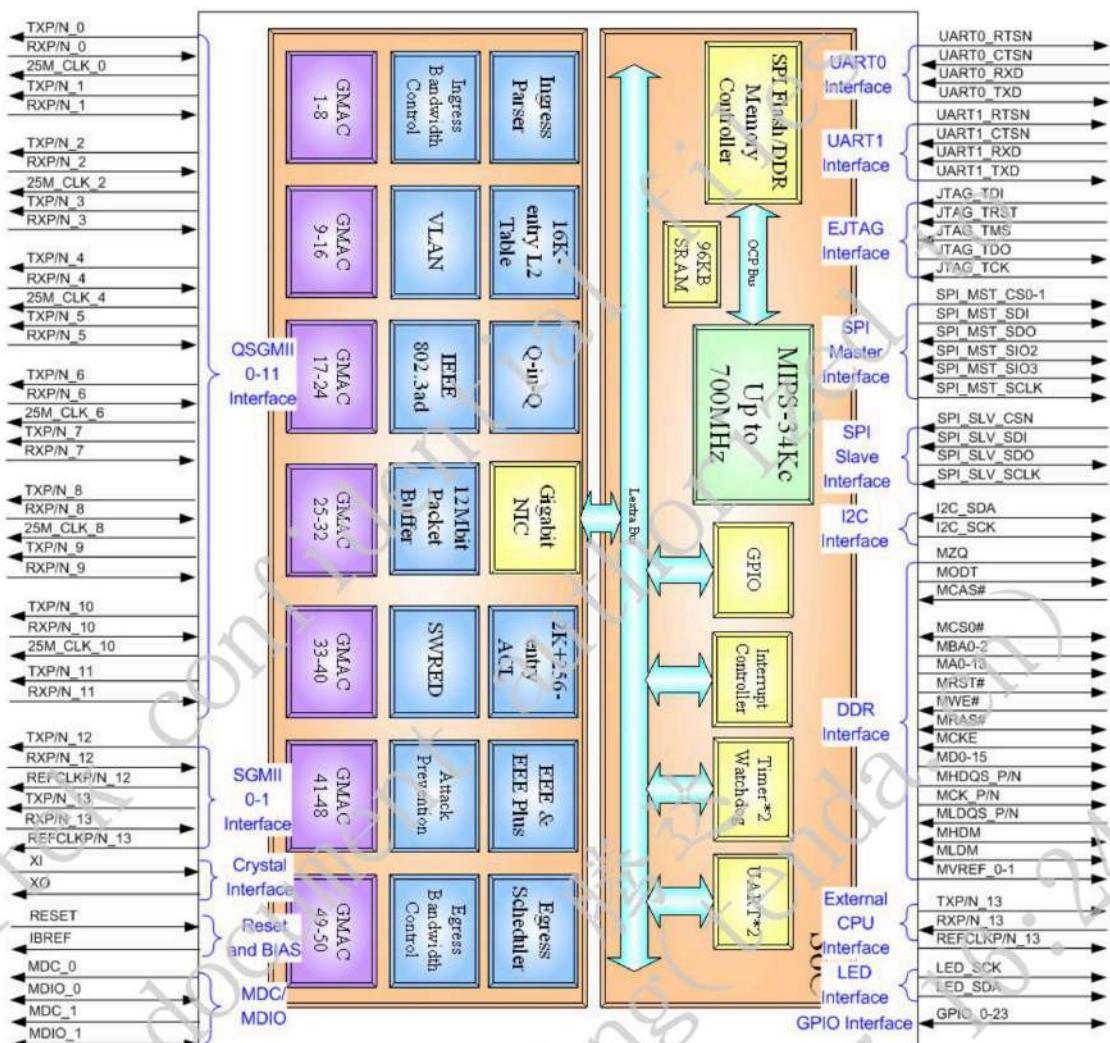


Figure 6. RTL8393M (48G + 2 SGMII) Pin Layout

5.3. RTL8393M (48G + 4G combo) Pin Assignments (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|----|----------------|--------------|------------|---------------|-----------|-----------|-----------|------------|-----------|---------------|---------------|----------------|--------------|
| A | GPIO_1_9 | GPIO_2_0 | GPIO_2_2 | GPIO_2_3 | JTAG_TDI | JTAG_TMS | JTAG_TCK | UART0_RTSN | UART0_RXD | SPI_MS_T_SIO3 | SPI_MS_T_SDO | SPI_MS_T_SDIN | SPI_MS_T_CS1 |
| B | GPIO_1_7 | GPIO_1_8 | GPIO_2_1 | INT | JTAG_TST | JTAG_TDO | RESER_VED | UART0_CTSN | UART0_RXD | SPI_MS_T_CS0 | SPI_MS_T_SIO2 | SPI_MS_T_SCL_K | GPIO_8 |
| C | GPIO_1_5 | GPIO_1_6 | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | MDVD_D |
| D | GPIO_1_3 | GPIO_1_4 | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | MDVD_D |
| E | RESER_VED | RESER_VED | RESER_VED | RESER_VED | | | | | | | | | |
| F | GPIO_1 | GPIO_2 | RESER_VED | RESER_VED | | | | | | | | | |
| G | LED_S_ck | GPIO_0 | RESER_VED | RESER_VED | | | | | | | | | |
| H | GPIO_1_2 | LED_S_DA | RESER_VED | RESER_VED | | | | | | | | | |
| J | SPI_SL_V_SDO | SPI_SL_V_CSN | LED_SF_SEL | LED_SF_SEL | | | | | | | | | |
| K | SPI_SL_V_SCL_K | SPI_SL_V_SDI | MODS_SEL | SPI_MS_ODESEL | | | | | | | | | |
| L | MDC_0 | MDIO_0 | DGND | DGND | | | | | | | | | |
| M | DGND | DGND | DGND | DGND | | | | | | | | | |
| N | DGND | DGND | DGND | DGND | | | | | | | | | |
| P | RESER_VED | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| R | RESER_VED | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| T | 25M_C_LK_0 | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| U | TXP_0 | TXN_0 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| V | RXN_0 | RXP_0 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| W | TXN_1 | TXP_1 | RESER_VED | SVDD3_3 | | | | | | | | | |
| Y | RXN_1 | RXP_1 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| AA | 25M_C_LK_2 | SGND | SGND | SVDD3_3 | | | | | | | | | |
| AB | TXP_2 | TXN_2 | SGND | SGND | | | | | | | | | |
| AC | RXP_2 | RXN_2 | SGND | SGND | SGND | SGND | AVDD3_3 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 |
| AD | RESER_VED | RESER_VED | 25M_C_LK_4 | SGND | SGND | SGND | SGND | AVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 |
| AE | TXN_3 | TXP_3 | TXN_4 | RXN_4 | SGND | TXP_5 | RXP_5 | SGND | AGND | AGND | SGND | SVDD1_0 | TXN_6 |
| AF | RXN_3 | RXP_3 | TXP_4 | RXP_4 | RESER_VED | TXN_5 | RXN_5 | SGND | XI | XO | SGND | 25M_C_LK_6 | TXP_6 |

Figure 7. RTL8393M (48G + 4G combo) Pin Assignments (Top View)

| 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|---|---------------|----------------|---------------|---------------|-----------------|---------------|--------------|-----------------|-----------------|----------------|-------------|----------------|
| GPIO_9 | MZQ/ RSVD | MCS#/ /MBA2 | MCS0#/ MA3 | MA3/ MA7 | MA7/ MA12 | MA9/ MA1 | MA2/ MCKE | MBA2/ /MRAS# | MRAS#/ /MA11 | MA1/ MA8 | MA8/ MA4 | MA6/ MA2 |
| MDVD/ D | MDOT/ MBA0 | MCS1#/ MA10 | MBA0/ MA5 | MA5/ MA9 | MRST#/ /RSVD | MA13/ MBA1 | MA0/ MWE# | MCAS# | MA12/ MA13 | MA11/ MA6 | MA4/ MA9 | MBA1/ MCS0# |
| MDVD/ D | MDVD/ D | MDVD/ D | MDVD/ D | MDVD/ D | DGND | DGND | DGND | DGND | DGND | DGND | MD7/ MD5 | MD5/ MD2 |
| MDVD/ D | MDVD/ D | MDVD/ D | MDVD/ D | MDVD/ D | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND |
| 14 15 16 | | | | | | | | | | | | |
| L M N P R T | | | | | | | | | | | | |
| DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 |
| DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 |
| DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 | DVDD1_0 |
| DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND |
| DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND |
| DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND |
| 14 15 16 | | | | | | | | | | | | |
| SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD3_3 | SVDD3_3 | SVDD3_3 | SVDD3_3 | SVDD3_3 |
| SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | RESER VED | RESER VED | SGND | RESER VED | RESER VED | RESER VED | TXP_11 | TXN_1_1 |
| RXN_6 | SGND | TXP_7 | RXP_7 | SGND | TXN_8 | RXN_8 | SGND | TXP_9 | RXP_9 | SGND | RXN_1_0 | RXP_10 |
| RXP_6 | RESER VED | TXN_7 | RXN_7 | 25M_C LK_S | TXP_8 | RXP_8 | RESER VED | TXN_9 | RXN_9 | 25M_C LK_10 | TXN_1_0 | TXP_10 |
| 14 15 16 17 18 19 20 21 22 23 24 25 26 | | | | | | | | | | | | |
| A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF | | | | | | | | | | | | |

Figure 8. RTL8393M (48G + 4G combo) Pin Assignments (Top View) (Continued)

5.4. RTL8393M (48G + 2 SGMII) Pin Assignments (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|----|----------------|--------------|------------|---------------|-----------|-----------|-----------|------------|-----------|---------------|---------------|----------------|--------------|
| A | GPIO_1_9 | GPIO_2_0 | GPIO_2_2 | GPIO_2_3 | JTAG_TDI | JTAG_TMS | JTAG_TCK | UART0_RTSN | UART0_RXD | SPI_MS_T_SIO3 | SPI_MS_T_SDO | SPI_MS_T_SDIN | SPI_MS_T_CS1 |
| B | GPIO_1_7 | GPIO_1_8 | GPIO_2_1 | INT | JTAG_TST | JTAG_TDO | RESER_VED | UART0_CTSN | UART0_RXD | SPI_MS_T_CS0 | SPI_MS_T_SIO2 | SPI_MS_T_SCL_K | GPIO_8 |
| C | GPIO_1_5 | GPIO_1_6 | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | MDVD_D |
| D | GPIO_1_3 | GPIO_1_4 | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | RESER_VED | MDVD_D |
| E | RESER_VED | RESER_VED | RESER_VED | RESER_VED | | | | | | | | | |
| F | GPIO_1 | GPIO_2 | RESER_VED | RESER_VED | | | | | | | | | |
| G | LED_S_ck | GPIO_0 | RESER_VED | RESER_VED | | | | | | | | | |
| H | GPIO_1_2 | LED_S_DA | RESER_VED | RESER_VED | | | | | | | | | |
| J | SPI_SL_V_SDO | SPI_SL_V_CSN | LED_SF_SEL | LED_SF_SEL | | | | | | | | | |
| K | SPI_SL_V_SCL_K | SPI_SL_V_SDI | MODS_SEL | SPI_MS_ODESEL | | | | | | | | | |
| L | MDC_0 | MDIO_0 | DGND | DGND | | | | | | | | | |
| M | DGND | DGND | DGND | DGND | | | | | | | | | |
| N | DGND | DGND | DGND | DGND | | | | | | | | | |
| P | RESER_VED | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| R | RESER_VED | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| T | 25M_C_LK_0 | DVDD3_3 | DVDD3_3 | DVDD3_3 | | | | | | | | | |
| U | TXP_0 | TXN_0 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| V | RXN_0 | RXP_0 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| W | TXN_1 | TXP_1 | RESER_VED | SVDD3_3 | | | | | | | | | |
| Y | RXN_1 | RXP_1 | SVDD3_3 | SVDD3_3 | | | | | | | | | |
| AA | 25M_C_LK_2 | SGND | SGND | SVDD3_3 | | | | | | | | | |
| AB | TXP_2 | TXN_2 | SGND | SGND | | | | | | | | | |
| AC | RXP_2 | RXN_2 | SGND | SGND | SGND | SGND | AVDD3_3 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 |
| AD | RESER_VED | RESER_VED | 25M_C_LK_4 | SGND | SGND | SGND | SGND | AVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 | SVDD1_0 |
| AE | TXN_3 | TXP_3 | TXN_4 | RXP_4 | SGND | TXP_5 | RXP_5 | SGND | AGND | AGND | SGND | SVDD1_0 | TXN_6 |
| AF | RXN_3 | RXP_3 | TXP_4 | RXP_4 | RESER_VED | TXN_5 | RXN_5 | SGND | XI | XO | SGND | 25M_C_LK_6 | TXP_6 |

1 2 3 4 5 6 7 8 9 10 11 12 13

Figure 9. RTL8393M (48G + 2 SGMII) Pin Assignments (Top View)

| 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|---------------------------|---------------|-----------------|----------------------------|-------------|----------------|----------------|---------------|----------------|----------------|--------------|-----------------|----------------|
| GPIO_9 | MZQ/ RSVD | MCAS0#/ MBA2 | MCS0#/ MA3 | MA3/ MA7 | MA7/ MA12 | MA9/ MA1 | MA2/ MCKE | MB2A#/ MA11 | MRAS#/ MA11 | MA1/ MA8 | MAS/ MA4 | MA6/ MA7 |
| MDVD_D | MDDT/ MBA0 | MCS1#/ MA10 | MBA0/ MA5 | MA5/ MA9 | MRST#/ RSVD | MA13#/ MBA1 | MA0#/ MWE# | MWE#/ MCAS# | MA12#/ MA13 | MA11/ MA6 | MA4/ MA0 | MBA1/ MCS0# |
| MDVD_D | MDVD_D | MDVD_D | MDVD_D | MDVD_D | DGND | DGND | DGND | DGND | DGND | DGND | MD10#/ MCS1# | MCKE/ MDT |
| MDVD_D | MDVD_D | MDVD_D | MDVD_D | MDVD_D | DGND | DGND | DGND | DGND | DGND | DGND | MD7#/ MD5 | MD5#/ MD2 |
| Document generated by EDR | | | | | | | | | | | | |
| 14 | 15 | 16 | L M N P K T | | | | | | | | | |
| DVDDI_0 | DVDDI_0 | DVDDI_0 | RESER_VED | | | | | | | | | |
| DVDDI_0 | DVDDI_0 | DVDDI_0 | RESER_VED | | | | | | | | | |
| DVDDI_0 | DVDDI_0 | DVDDI_0 | DDR_C_LK_SE_L2 | | | | | | | | | |
| DGND | DGND | DGND | RESER_VED | | | | | | | | | |
| DGND | DGND | DGND | RESER_VED | | | | | | | | | |
| DGND | DGND | DGND | RESER_VED | | | | | | | | | |
| 14 | 15 | 16 | AGND | | | | | | | | | |
| SVDDI_0_1 | SVDDI_0_1 | SVDDI_0_1 | SVDDI_0_1 | SVDDI_0 | SVDDI_0 | RESER_VED | RESER_VED | SGND | RESER_VED | RESER_VED | TXP_I_1 | TXN_I_1 |
| SVDDI_0_1 | SVDDI_0_1 | SVDDI_0_1 | SVDDI_0_1 | SVDDI_0 | RESER_VED | RESER_VED | RESER_VED | SGND | RESER_VED | RESER_VED | TXP_I_2 | TXN_I_2 |
| RXN_6 | SGND | TXP_I_7 | RXP_I_7 | SGND | TXN_I_8 | RXN_I_8 | SGND | TXP_I_9 | RXP_I_9 | SGND | RXN_I_0 | RXP_I_0 |
| RXP_6 | RESER_VED | TXN_I_7 | RXXN_I_7 | 25M_C_LK_8 | TXP_I_8 | RXP_I_8 | RESER_VED | TXN_I_9 | RXXN_I_9 | TXN_I_0 | 25M_C_LK_10 | TXN_I_0 |
| 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |

Figure 10. RTL8393M (48G + 2 SGMII) Pin Assignments (Top View) (Continued)

5.5. Pin Assignments Table Definitions

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified ‘Upon Reset’ time.

I: Input Pin

AI: Analog Input Pin

O: Output Pin

AO: Analog Output Pin

I/O: Bi-Direction Input/Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

DP: Digital Power Pin

AP: Analog Power Pin

DG: Digital Ground Pin

AG: Analog Ground Pin

SP: SERDES Power Pin

SG: SERDES Ground Pin

MP: DDR Power Pin

RP: Reference voltage for data for DDR SDRAM

IPU: Input Pin With Pull-Up Resistor;
 (Typical Value = 75KΩ)

OPU: Output Pin With Pull-Up Resistor;
 (Typical Value = 75KΩ)

IPD: Input Pin With Pull-Down Resistor;
 (Typical Value = 75KΩ)

OPD: Output Pin With Pull-Down Resistor;
 (Typical Value = 75KΩ)

5.6. RTL8393M(48G + 4G combo) Pin Assignments Table

Table 1. RTL8393M(48G + 4G combo) Pin Assignments Table

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| GPIO_19 | A1 | I/O _{PD} |
| GPIO_20 | A2 | I/O _{PD} |
| GPIO_22 | A3 | I/O _{PD} |
| GPIO_23 | A4 | I/O _{PD} |
| JTAG_TDI/UART1_RXD/GPIO_6 | A5 | I/O _{PD} |
| JTAG_TMS/UART1_RTSN/GPIO_3 | A6 | I/O _{PU} |
| JTAG_TCK/UART1_CTSN/GPIO_4 | A7 | I/O _{PU} |
| UART0_RTSN | A8 | O _{PD} |
| UART0_RXD | A9 | I _{PD} |
| SPI_MST_SIO3/GPIO_11 | A10 | I/O _{PD} |
| SPI_MST_SDO/SIO_1 | A11 | I/O _{PD} |
| SPI_MST_SD/SDI/SIO_0 | A12 | I/O _{PD} |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| SPI_MST_CS1 | A13 | O |
| GPIO_9 | A14 | I/O _{PU} |
| MZQ/RSVD | A15 | I |
| MCAS#/MBA2 | A16 | O |
| MCS#/#MA3 | A17 | O |
| MA3/MA7 | A18 | O |
| MA7/MA12 | A19 | O |
| MA9/MA1 | A20 | O |
| MA2/MCKE | A21 | O |
| MBA2/MRAS# | A22 | O |
| MRAS#/MA11 | A23 | O |
| MA1/MA8 | A24 | O |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| MA8/MA4 | A25 | O |
| MA6/MA2 | A26 | O |
| GPIO_17 | B1 | I/O _{PD} |
| GPIO_18 | B2 | I/O _{PD} |
| GPIO_21 | B3 | I/O _{PD} |
| INT | B4 | O _{PD} |
| JTAG_TRST/GPIO_5 | B5 | I/O _{PD} |
| JTAG_TDO/UART1_TXD/GPIO_7 | B6 | I/O _{PD} |
| RESERVED | B7 | |
| UART0_CTSN | B8 | I _{PU} |
| UART0_RXD | B9 | O _{PU} |
| SPI_MST_CS0 | B10 | O |
| SPI_MST_SIO2/GPIO_10 | B11 | I/O _{PD} |
| SPI_MST_SCLK | B12 | O |
| GPIO_8 | B13 | I/O _{PU} |
| MDVDD | B14 | MP |
| MODT/MBA0 | B15 | O |
| MCS1#/MA10 | B16 | O |
| MBA0/MA5 | B17 | O |
| MA5/MA9 | B18 | O |
| MRST#/RSVD | B19 | O |
| MA13/MBA1 | B20 | O |
| MA0/MWE# | B21 | O |
| MWE#/MCAS# | B22 | O |
| MA12/MA13 | B23 | O |
| MA11/MA6 | B24 | O |
| MA4/MA0 | B25 | O |
| MBA1/MCS0# | B26 | O |
| GPIO_15 | C1 | I/O _{PD} |
| GPIO_16 | C2 | I/O _{PD} |
| RESERVED | C3 | |
| RESERVED | C4 | |
| RESERVED | C5 | |
| RESERVED | C6 | |
| RESERVED | C7 | |
| RESERVED | C8 | |
| RESERVED | C9 | |
| RESERVED | C10 | |
| RESERVED | C11 | |
| RESERVED | C12 | |
| MDVDD | C13 | MP |
| MDVDD | C14 | MP |
| MDVDD | C15 | MP |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| MDVDD | C16 | MP |
| MDVDD | C17 | MP |
| MDVDD | C18 | MP |
| DGND | C19 | DG |
| DGND | C20 | DG |
| DGND | C21 | DG |
| DGND | C22 | DG |
| DGND | C23 | DG |
| DGND | C24 | DG |
| MA10/MCS1# | C25 | O |
| MCKE/MODT | C26 | O |
| GPIO_13 | D1 | I/O _{PD} |
| GPIO_14 | D2 | I/O _{PD} |
| RESERVED | D3 | |
| RESERVED | D4 | |
| RESERVED | D5 | |
| RESERVED | D6 | |
| RESERVED | D7 | |
| RESERVED | D8 | |
| RESERVED | D9 | |
| RESERVED | D10 | |
| RESERVED | D11 | |
| RESERVED | D12 | |
| MDVDD | D13 | MP |
| MDVDD | D14 | MP |
| MDVDD | D15 | MP |
| MDVDD | D16 | MP |
| MDVDD | D17 | MP |
| MDVDD | D18 | MP |
| MDVDD | D19 | MP |
| DGND | D20 | DG |
| DGND | D21 | DG |
| DGND | D22 | DG |
| DGND | D23 | DG |
| DGND | D24 | DG |
| MD7/MD5 | D25 | I/O |
| MD5/MD2 | D26 | I/O |
| RESERVED | E1 | |
| RESERVED | E2 | |
| RESERVED | E3 | |
| RESERVED | E4 | |
| DGND | E23 | DG |
| DGND | E24 | DG |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| MD3/MD0 | E25 | I/O |
| MD1/MD7 | E26 | I/O |
| GPIO_1/GPIO_MDC | F1 | I/O _{PU} |
| GPIO_2/GPIO_MDIO | F2 | I/O _{PU} |
| RESERVED | F3 | |
| RESERVED | F4 | |
| DGND | F23 | DG |
| DGND | F24 | DG |
| MLDM/MLDM | F25 | O |
| MD8/MD13 | F26 | I/O |
| LED_SCK/LED_MDC | G1 | O _{PD} |
| GPIO_0/SYS_LED | G2 | I/O _{PD} |
| RESERVED | G3 | |
| RESERVED | G4 | |
| DGND | G23 | DG |
| DGND | G24 | DG |
| MD10/MD10 | G25 | I/O |
| MD14/MD8 | G26 | I/O |
| GPIO_12/1588_OUTPUT | H1 | I/O _{PD} |
| LED_SDA/LED_MDIO | H2 | I/O _{PU} |
| RESERVED | H3 | |
| RESERVED | H4 | |
| DGND | H23 | DG |
| DGND | H24 | DG |
| MD12/MD15 | H25 | I/O |
| MHDQS_N/MHDQS_N | H26 | I/O |
| SPI_SLV_SDO | J1 | O _{PD} |
| SPI_SLV_CSN | J2 | I _{PU} |
| LED_IF_SEL_1 | J3 | I _{PU} |
| LED_IF_SEL_0 | J4 | I _{PU} |
| RESERVED | J23 | |
| MVREF | J24 | RP |
| MHDQS_P/MHDQS_P | J25 | I/O |
| MCK_P/MLDQS_P | J26 | I/O |
| SPI_SLV_SCLK/I2C_SCK | K1 | I _{PU} |
| SPI_SLV_SDI/I2C_SDA | K2 | I/O _{PU} |
| MODE_SEL | K3 | I _{PU} |
| SPI_MODE_SEL | K4 | I _{PU} |
| RESERVED | K23 | |
| MVREF | K24 | RP |
| MCK_N/MLDQS_N | K25 | I/O |
| MLDQS_N/MCK_N | K26 | I/O |
| MDC_0 | L1 | O _{PD} |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| MDIO_0 | L2 | I/O _{PU} |
| DGND | L3 | DG |
| DGND | L4 | DG |
| DVDD10 | L11 | DP |
| DVDD10 | L12 | DP |
| DVDD10 | L13 | DP |
| DVDD10 | L14 | DP |
| DVDD10 | L15 | DP |
| DVDD10 | L16 | DP |
| RESERVED | L23 | |
| LED_EN | L24 | I _{PU} |
| MLDQS_P/MCK_P | L25 | I/O |
| MHDM/MHDM | L26 | O |
| DGND | M1 | DG |
| DGND | M2 | DG |
| DGND | M3 | DG |
| DGND | M4 | DG |
| DVDD10 | M11 | DP |
| DVDD10 | M12 | DP |
| DVDD10 | M13 | DP |
| DVDD10 | M14 | DP |
| DVDD10 | M15 | DP |
| RESERVED | M23 | |
| RESERVED | M24 | |
| MD15/MD14 | M25 | I/O |
| MD13/MD9 | M26 | I/O |
| DGND | N1 | DG |
| DGND | N2 | DG |
| DGND | N3 | DG |
| DGND | N4 | DG |
| DVDD10 | N11 | DP |
| DVDD10 | N12 | DP |
| DVDD10 | N13 | DP |
| DVDD10 | N14 | DP |
| DVDD10 | N15 | DP |
| DVDD10 | N16 | DP |
| DDR_CLK_SEL_2 | N23 | I _{PU} |
| RESERVED | N24 | |
| MD11/MD11 | N25 | I/O |
| MD9/MD12 | N26 | I/O |
| RESERVED | P1 | |
| DVDD33 | P2 | DP |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|------|
| DVDD33 | P3 | DP |
| DVDD33 | P4 | DP |
| DVDD10 | P11 | DP |
| DVDD10 | P12 | DP |
| DGND | P13 | DG |
| DGND | P14 | DG |
| DGND | P15 | DG |
| DGND | P16 | DG |
| RESERVED | P23 | |
| PWRMON | P24 | AI |
| MD0/MD6 | P25 | I/O |
| MD2/MD1 | P26 | I/O |
| RESERVED | R1 | |
| DVDD33 | R2 | DP |
| DVDD33 | R3 | DP |
| DVDD33 | R4 | DP |
| DGND | R11 | DG |
| DGND | R12 | DG |
| DGND | R13 | DG |
| DGND | R14 | DG |
| DGND | R15 | DG |
| DGND | R16 | DG |
| RESERVED | R23 | |
| IBREF | R24 | AI/O |
| MD6/MD3 | R25 | I/O |
| MD4/MD4 | R26 | I/O |
| 25M_CLK_0 | T1 | AO |
| DVDD33 | T2 | DP |
| DVDD33 | T3 | DP |
| DVDD33 | T4 | DP |
| DGND | T11 | DG |
| DGND | T12 | DG |
| DGND | T13 | DG |
| DGND | T14 | DG |
| DGND | T15 | DG |
| DGND | T16 | DG |
| AGND | T23 | AG |
| RESERVED | T24 | |
| RESERVED | T25 | |
| RESERVED | T26 | |
| TXP_0 | U1 | AO |
| TXN_0 | U2 | AO |
| SVDD33 | U3 | SP |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|-------------------|
| SVDD33 | U4 | SP |
| AVDD10 | U23 | AP |
| RESET | U24 | AI |
| MDIO_1 | U25 | I/O _{PU} |
| MDC_1 | U26 | O _{PD} |
| RXP_0 | V1 | AI |
| RXN_0 | V2 | AI |
| SVDD33 | V3 | SP |
| SVDD33 | V4 | SP |
| AVDD33 | V23 | AP |
| REFCLKP_13 | V24 | AO |
| RXP_13 | V25 | AI |
| RXN_13 | V26 | AI |
| TXN_1 | W1 | AO |
| TXP_1 | W2 | AO |
| RESERVED | W3 | |
| SVDD33 | W4 | SP |
| RESERVED | W23 | |
| REFCLKN_13 | W24 | AO |
| TXP_13 | W25 | AO |
| TXN_13 | W26 | AO |
| RXN_1 | Y1 | AI |
| RXP_1 | Y2 | AI |
| SVDD33 | Y3 | SP |
| SVDD33 | Y4 | SP |
| RESERVED | Y23 | |
| RESERVED | Y24 | |
| RXN_12 | Y25 | AI |
| RXP_12 | Y26 | AI |
| 25M_CLK_2 | AA1 | AO |
| SGND | AA2 | SG |
| SGND | AA3 | SG |
| SVDD33 | AA4 | SP |
| SVDD33 | AA23 | SP |
| RESERVED | AA24 | |
| TXN_12 | AA25 | AO |
| TXP_12 | AA26 | AO |
| TXP_2 | AB1 | AO |
| TXN_2 | AB2 | AO |
| SGND | AB3 | SG |
| SGND | AB4 | SG |
| SVDD33 | AB23 | SP |
| SGND | AB24 | SG |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|------|
| SGND | AB25 | SG |
| 25M_CLK_12 | AB26 | AO |
| RXP_2 | AC1 | AI |
| RXN_2 | AC2 | AI |
| SGND | AC3 | SG |
| SGND | AC4 | SG |
| SGND | AC5 | SG |
| SGND | AC6 | SG |
| AVDD33 | AC7 | AP |
| SVDD10 | AC8 | SP |
| SVDD10 | AC9 | SP |
| SVDD10 | AC10 | SP |
| SVDD10 | AC11 | SP |
| SVDD10 | AC12 | SP |
| SVDD10 | AC13 | SP |
| SVDD10 | AC14 | SP |
| SVDD10 | AC15 | SP |
| SVDD10 | AC16 | SP |
| SVDD10 | AC17 | SP |
| SVDD10 | AC18 | SP |
| SVDD10 | AC19 | SP |
| SVDD33 | AC20 | SP |
| SVDD33 | AC21 | SP |
| SVDD33 | AC22 | SP |
| SVDD33 | AC23 | SP |
| SGND | AC24 | SG |
| RXP_11 | AC25 | AI |
| RXN_11 | AC26 | AI |
| RESERVED | AD1 | |
| RESERVED | AD2 | |
| 25M_CLK_4 | AD3 | AO |
| SGND | AD4 | SG |
| SGND | AD5 | SG |
| SGND | AD6 | SG |
| SGND | AD7 | SG |
| AVDD10 | AD8 | AP |
| SVDD10 | AD9 | SP |
| SVDD10 | AD10 | SP |
| SVDD10 | AD11 | SP |
| SVDD10 | AD12 | SP |
| SVDD10 | AD13 | SP |
| SVDD10 | AD14 | SP |
| SVDD10 | AD15 | SP |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|------|
| SVDD10 | AD16 | SP |
| SVDD10 | AD17 | SP |
| SVDD10 | AD18 | SP |
| RESERVED | AD19 | |
| RESERVED | AD20 | |
| SGND | AD21 | SG |
| RESERVED | AD22 | |
| RESERVED | AD23 | |
| TXP_11 | AD25 | AO |
| TXN_11 | AD26 | AO |
| TXN_3 | AE1 | AO |
| TXP_3 | AE2 | AO |
| TXN_4 | AE3 | AO |
| RXN_4 | AE4 | AI |
| SGND | AE5 | SG |
| TXP_5 | AE6 | AO |
| RXP_5 | AE7 | AI |
| SGND | AE8 | SG |
| AGND | AE9 | AG |
| AGND | AE10 | AG |
| SGND | AE11 | SG |
| SVDD10 | AE12 | SP |
| TXN_6 | AE13 | AO |
| RXN_6 | AE14 | AI |
| SGND | AE15 | SG |
| TXP_7 | AE16 | AO |
| RXP_7 | AE17 | AI |
| SGND | AE18 | SG |
| TXN_8 | AE19 | AO |
| RXN_8 | AE20 | AI |
| SGND | AE21 | SG |
| TXP_9 | AE22 | AO |
| RXP_9 | AE23 | AI |
| SGND | AE24 | SG |
| RXN_10 | AE25 | AI |
| RXP_10 | AE26 | AI |
| RXN_3 | AF1 | AI |
| RXP_3 | AF2 | AI |
| TXP_4 | AF3 | AO |
| RXP_4 | AF4 | AI |
| RESERVED | AF5 | |
| TXN_5 | AF6 | AO |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|------|
| RXN_5 | AF7 | AI |
| SGND | AF8 | SG |
| XI | AF9 | AI |
| XO | AF10 | AO |
| SGND | AF11 | SG |
| 25M_CLK_6 | AF12 | AO |
| TXP_6 | AF13 | AO |
| RXP_6 | AF14 | AI |
| RESERVED | AF15 | |
| TXN_7 | AF16 | AO |

| RTL8393M(48G+4G combo) Pin Name | Pin No. | Type |
|---------------------------------|---------|------|
| RXN_7 | AF17 | AI |
| 25M_CLK_8 | AF18 | AO |
| TXP_8 | AF19 | AO |
| RXP_8 | AF20 | AI |
| RESERVED | AF21 | |
| TXN_9 | AF22 | AO |
| RXN_9 | AF23 | AI |
| 25M_CLK_10 | AF24 | AO |
| TXN_10 | AF25 | AO |
| TXP_10 | AF26 | AO |

5.7. RTL8393M(48G + 2 SGMII) Pin Assignments Table

Table 2. RTL8393M(48G + 2 SGMII) Pin Assignments Table

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|-------------------|
| GPIO_19 | A1 | I/O _{PD} |
| GPIO_20 | A2 | I/O _{PD} |
| GPIO_22 | A3 | I/O _{PD} |
| GPIO_23 | A4 | I/O _{PD} |
| JTAG_TDI/UART1_RXD/GPIO_6 | A5 | I/O _{PD} |
| JTAG_TMS/UART1_RTSN/GPIO_3 | A6 | I/O _{PU} |
| JTAG_TCK/UART1_CTSN/GPIO_4 | A7 | I/O _{PU} |
| UART0_RTSN | A8 | O _{PD} |
| UART0_RXD | A9 | I _{PD} |
| SPI_MST_SIO3/GPIO_11 | A10 | I/O _{PD} |
| SPI_MST_SDO/SIO_1 | A11 | I/O _{PD} |
| SPI_MST_SDI/SIO_0 | A12 | I/O _{PD} |
| SPI_MST_CS1 | A13 | O |
| GPIO_9 | A14 | I/O _{PU} |
| MZQ/RSVD | A15 | I |
| MCAS#/MBA2 | A16 | O |
| MCS0#/MA3 | A17 | O |
| MA3/MA7 | A18 | O |
| MA7/MA12 | A19 | O |
| MA9/MA1 | A20 | O |
| MA2/MCKE | A21 | O |
| MBA2/MRAS# | A22 | O |
| MRAS#/MA11 | A23 | O |
| MA1/MA8 | A24 | O |
| MA8/MA4 | A25 | O |
| MA6/MA2 | A26 | O |
| GPIO_17 | B1 | I/O _{PD} |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|-------------------|
| GPIO_18 | B2 | I/O _{PD} |
| GPIO_21 | B3 | I/O _{PD} |
| INT | B4 | O _{PD} |
| JTAG_TRST/GPIO_5 | B5 | I/O _{PD} |
| JTAG_TDO/UART1_TXD/GPIO_7 | B6 | I/O _{PD} |
| RESERVED | B7 | |
| UART0_CTSN | B8 | I _{PU} |
| UART0_RXD | B9 | O _{PU} |
| SPI_MST_CS0 | B10 | O |
| SPI_MST_SIO2/GPIO_10 | B11 | I/O _{PD} |
| SPI_MST_SCLK | B12 | O |
| GPIO_8 | B13 | I/O _{PU} |
| MDVDD | B14 | MP |
| MODT/MBA0 | B15 | O |
| MCS1#/MA10 | B16 | O |
| MBA0/MA5 | B17 | O |
| MA5/MA9 | B18 | O |
| MRST#/RSVD | B19 | O |
| MA13/MBA1 | B20 | O |
| MA0/MWE# | B21 | O |
| MWE#/MCAS# | B22 | O |
| MA12/MA13 | B23 | O |
| MA11/MA6 | B24 | O |
| MA4/MA0 | B25 | O |
| MBA1/MCS0# | B26 | O |
| GPIO_15 | C1 | I/O _{PD} |
| GPIO_16 | C2 | I/O _{PD} |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|-------------------|
| RESERVED | C3 | |
| RESERVED | C4 | |
| RESERVED | C5 | |
| RESERVED | C6 | |
| RESERVED | C7 | |
| RESERVED | C8 | |
| RESERVED | C9 | |
| RESERVED | C10 | |
| RESERVED | C11 | |
| RESERVED | C12 | |
| MDVDD | C13 | MP |
| MDVDD | C14 | MP |
| MDVDD | C15 | MP |
| MDVDD | C16 | MP |
| MDVDD | C17 | MP |
| MDVDD | C18 | MP |
| DGND | C19 | DG |
| DGND | C20 | DG |
| DGND | C21 | DG |
| DGND | C22 | DG |
| DGND | C23 | DG |
| DGND | C24 | DG |
| MA10/MCS1# | C25 | O |
| MCKE/MODT | C26 | O |
| GPIO_13 | D1 | I/O _{PD} |
| GPIO_14 | D2 | I/O _{PD} |
| RESERVED | D3 | |
| RESERVED | D4 | |
| RESERVED | D5 | |
| RESERVED | D6 | |
| RESERVED | D7 | |
| RESERVED | D8 | |
| RESERVED | D9 | |
| RESERVED | D10 | |
| RESERVED | D11 | |
| RESERVED | D12 | |
| MDVDD | D13 | MP |
| MDVDD | D14 | MP |
| MDVDD | D15 | MP |
| MDVDD | D16 | MP |
| MDVDD | D17 | MP |
| MDVDD | D18 | MP |
| MDVDD | D19 | MP |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|-------------------|
| DGND | D20 | DG |
| DGND | D21 | DG |
| DGND | D22 | DG |
| DGND | D23 | DG |
| DGND | D24 | DG |
| MD7/MD5 | D25 | I/O |
| MD5/MD2 | D26 | I/O |
| RESERVED | E1 | |
| RESERVED | E2 | |
| RESERVED | E3 | |
| RESERVED | E4 | |
| DGND | E23 | DG |
| DGND | E24 | DG |
| MD3/MD0 | E25 | I/O |
| MD1/MD7 | E26 | I/O |
| GPIO_1/GPIO_MDC | F1 | I/O _{PU} |
| GPIO_2/GPIO_MDIO | F2 | I/O _{PU} |
| RESERVED | F3 | |
| RESERVED | F4 | |
| DGND | F23 | DG |
| DGND | F24 | DG |
| MLDM/MLDM | F25 | O |
| MD8/MD13 | F26 | I/O |
| LED_SCK/LED_MDC | G1 | O _{PD} |
| GPIO_0/SYS_LED | G2 | I/O _{PD} |
| RESERVED | G3 | |
| RESERVED | G4 | |
| DGND | G23 | DG |
| DGND | G24 | DG |
| MD10/MD10 | G25 | I/O |
| MD14/MD8 | G26 | I/O |
| GPIO_12/1588_OUTPUT | H1 | I/O _{PD} |
| LED_SDA/LED_MDIO | H2 | I/O _{PU} |
| RESERVED | H3 | |
| RESERVED | H4 | |
| DGND | H23 | DG |
| DGND | H24 | DG |
| MD12/MD15 | H25 | I/O |
| MHDQS_N/MHDQS_N | H26 | I/O |
| SPI_SLV_SDO | J1 | O _{PD} |
| SPI_SLV_CSN | J2 | I _{PU} |
| LED_IF_SEL_1 | J3 | I _{PU} |
| LED_IF_SEL_0 | J4 | I _{PU} |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|---|----------------|-------------------|
| RESERVED | J23 | |
| MVREF | J24 | RP |
| MHDQS_P/MHDQS_P | J25 | I/O |
| MCK_P/MLDQS_P | J26 | I/O |
| SPI_SLV_SCLK/I2C_SCK | K1 | I _{PU} |
| SPI_SLV_SD/I2C_SDA | K2 | I/O _{PU} |
| MODE_SEL | K3 | I _{PU} |
| SPI_MODE_SEL | K4 | I _{PU} |
| RESERVED | K23 | |
| MVREF | K24 | RP |
| MCK_N/MLDQS_N | K25 | I/O |
| MLDQS_N/MCK_N | K26 | I/O |
| MDC_0 | L1 | O _{PD} |
| MDIO_0 | L2 | I/O _{PU} |
| DGND | L3 | DG |
| DGND | L4 | DG |
| DVDD10 | L11 | DP |
| DVDD10 | L12 | DP |
| DVDD10 | L13 | DP |
| DVDD10 | L14 | DP |
| DVDD10 | L15 | DP |
| DVDD10 | L16 | DP |
| RESERVED | L23 | |
| LED_EN | L24 | I _{PU} |
| MLDQS_P/MCK_P | L25 | I/O |
| MHDM/MHDM | L26 | O |
| DGND | M1 | DG |
| DGND | M2 | DG |
| DGND | M3 | DG |
| DGND | M4 | DG |
| DVDD10 | M11 | DP |
| DVDD10 | M12 | DP |
| DVDD10 | M13 | DP |
| DVDD10 | M14 | DP |
| DVDD10 | M15 | DP |
| DVDD10 | M16 | DP |
| RESERVED | M23 | |
| RESERVED | M24 | |
| MD15/MD14 | M25 | I/O |
| MD13/MD9 | M26 | I/O |
| DGND | N1 | DG |
| DGND | N2 | DG |
| DGND | N3 | DG |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|---|----------------|-----------------|
| DGND | N4 | DG |
| DVDD10 | N11 | DP |
| DVDD10 | N12 | DP |
| DVDD10 | N13 | DP |
| DVDD10 | N14 | DP |
| DVDD10 | N15 | DP |
| DVDD10 | N16 | DP |
| DDR_CLK_SEL_2 | N23 | I _{PU} |
| RESERVED | N24 | |
| MD11/MD11 | N25 | I/O |
| MD9/MD12 | N26 | I/O |
| RESERVED | P1 | |
| DVDD33 | P2 | DP |
| DVDD33 | P3 | DP |
| DVDD33 | P4 | DP |
| DVDD10 | P11 | DP |
| DVDD10 | P12 | DP |
| DGND | P13 | DG |
| DGND | P14 | DG |
| DGND | P15 | DG |
| DGND | P16 | DG |
| RESERVED | P23 | |
| PWRMON | P24 | AI |
| MD0/MD6 | P25 | I/O |
| MD2/MD1 | P26 | I/O |
| RESERVED | R1 | |
| DVDD33 | R2 | DP |
| DVDD33 | R3 | DP |
| DVDD33 | R4 | DP |
| DGND | R11 | DG |
| DGND | R12 | DG |
| DGND | R13 | DG |
| DGND | R14 | DG |
| DGND | R15 | DG |
| DGND | R16 | DG |
| RESERVED | R23 | |
| IBREF | R24 | AI/O |
| MD6/MD3 | R25 | I/O |
| MD4/MD4 | R26 | I/O |
| 25M_CLK_0 | T1 | AO |
| DVDD33 | T2 | DP |
| DVDD33 | T3 | DP |
| DVDD33 | T4 | DP |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|-------------------|
| DGND | T11 | DG |
| DGND | T12 | DG |
| DGND | T13 | DG |
| DGND | T14 | DG |
| DGND | T15 | DG |
| DGND | T16 | DG |
| AGND | T23 | AG |
| RESERVED | T24 | |
| RESERVED | T25 | |
| RESERVED | T26 | |
| TXP_0 | U1 | AO |
| TXN_0 | U2 | AO |
| SVDD33 | U3 | SP |
| SVDD33 | U4 | SP |
| AVDD10 | U23 | AP |
| RESET | U24 | AI |
| MDIO_1 | U25 | I/O _{PU} |
| MDC_1 | U26 | O _{PD} |
| RXP_0 | V1 | AI |
| RXN_0 | V2 | AI |
| SVDD33 | V3 | SP |
| SVDD33 | V4 | SP |
| AVDD33 | V23 | AP |
| REFCLKP_13 | V24 | AO |
| RXP_13 | V25 | AI |
| RXN_13 | V26 | AI |
| TXN_1 | W1 | AO |
| TXP_1 | W2 | AO |
| RESERVED | W3 | |
| SVDD33 | W4 | SP |
| RESERVED | W23 | |
| REFCLKN_13 | W24 | AO |
| TXP_13 | W25 | AO |
| TXN_13 | W26 | AO |
| RXN_1 | Y1 | AI |
| RXP_1 | Y2 | AI |
| SVDD33 | Y3 | SP |
| SVDD33 | Y4 | SP |
| RESERVED | Y23 | |
| REFCLKP_12 | Y24 | AO |
| RXN_12 | Y25 | AI |
| RXP_12 | Y26 | AI |
| 25M_CLK_2 | AA1 | AO |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|------|
| SGND | AA2 | SG |
| SGND | AA3 | SG |
| SVDD33 | AA4 | SP |
| SVDD33 | AA23 | SP |
| REFCLKN_12 | AA24 | AO |
| TXN_12 | AA25 | AO |
| TXP_12 | AA26 | AO |
| TXP_2 | AB1 | AO |
| TXN_2 | AB2 | AO |
| SGND | AB3 | SG |
| SGND | AB4 | SG |
| SVDD33 | AB23 | SP |
| SGND | AB24 | SG |
| SGND | AB25 | SG |
| RESERVED | AB26 | |
| RXP_2 | AC1 | AI |
| RXN_2 | AC2 | AI |
| SGND | AC3 | SG |
| SGND | AC4 | SG |
| SGND | AC5 | SG |
| SGND | AC6 | SG |
| AVDD33 | AC7 | AP |
| SVDD10 | AC8 | SP |
| SVDD10 | AC9 | SP |
| SVDD10 | AC10 | SP |
| SVDD10 | AC11 | SP |
| SVDD10 | AC12 | SP |
| SVDD10 | AC13 | SP |
| SVDD10_1 | AC14 | SP |
| SVDD10_1 | AC15 | SP |
| SVDD10_1 | AC16 | SP |
| SVDD10_1 | AC17 | SP |
| SVDD10 | AC18 | SP |
| SVDD10 | AC19 | SP |
| SVDD33 | AC20 | SP |
| SVDD33 | AC21 | SP |
| SVDD33 | AC22 | SP |
| SVDD33 | AC23 | SP |
| SGND | AC24 | SG |
| RXP_11 | AC25 | AI |
| RXN_11 | AC26 | AI |
| RESERVED | AD1 | |
| RESERVED | AD2 | |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|------|
| 25M_CLK_4 | AD3 | AO |
| SGND | AD4 | SG |
| SGND | AD5 | SG |
| SGND | AD6 | SG |
| SGND | AD7 | SG |
| AVDD10 | AD8 | AP |
| SVDD10 | AD9 | SP |
| SVDD10 | AD10 | SP |
| SVDD10 | AD11 | SP |
| SVDD10 | AD12 | SP |
| SVDD10 | AD13 | SP |
| SVDD10_1 | AD14 | SP |
| SVDD10_1 | AD15 | SP |
| SVDD10_1 | AD16 | SP |
| SVDD10_1 | AD17 | SP |
| SVDD10 | AD18 | SP |
| RESERVED | AD19 | |
| RESERVED | AD20 | |
| SGND | AD21 | SG |
| RESERVED | AD22 | |
| RESERVED | AD23 | |
| RESERVED | AD24 | |
| TXP_11 | AD25 | AO |
| TXN_11 | AD26 | AO |
| TXN_3 | AE1 | AO |
| TXP_3 | AE2 | AO |
| TXN_4 | AE3 | AO |
| RXN_4 | AE4 | AI |
| SGND | AE5 | SG |
| TXP_5 | AE6 | AO |
| RXP_5 | AE7 | AI |
| SGND | AE8 | SG |
| AGND | AE9 | AG |
| AGND | AE10 | AG |
| SGND | AE11 | SG |
| SVDD10 | AE12 | SP |
| TXN_6 | AE13 | AO |
| RXN_6 | AE14 | AI |

| RTL8393M(48G + 2 SGMII) Pin Name | Pin No. | Type |
|----------------------------------|---------|------|
| SGND | AE15 | SG |
| TXP_7 | AE16 | AO |
| RXP_7 | AE17 | AI |
| SGND | AE18 | SG |
| TXN_8 | AE19 | AO |
| RXN_8 | AE20 | AI |
| SGND | AE21 | SG |
| TXP_9 | AE22 | AO |
| RXP_9 | AE23 | AI |
| SGND | AE24 | SG |
| RXN_10 | AE25 | AI |
| RXP_10 | AE26 | AI |
| RXN_3 | AF1 | AI |
| RXP_3 | AF2 | AI |
| TXP_4 | AF3 | AO |
| RXP_4 | AF4 | AI |
| RESERVED | AF5 | |
| TXN_5 | AF6 | AO |
| RXN_5 | AF7 | AI |
| SGND | AF8 | SG |
| XI | AF9 | AI |
| XO | AF10 | AO |
| SGND | AF11 | SG |
| 25M_CLK_6 | AF12 | AO |
| TXP_6 | AF13 | AO |
| RXP_6 | AF14 | AI |
| RESERVED | AF15 | |
| TXN_7 | AF16 | AO |
| RXN_7 | AF17 | AI |
| 25M_CLK_8 | AF18 | AO |
| TXP_8 | AF19 | AO |
| RXP_8 | AF20 | AI |
| RESERVED | AF21 | |
| TXN_9 | AF22 | AO |
| RXN_9 | AF23 | AI |
| 25M_CLK_10 | AF24 | AO |
| TXN_10 | AF25 | AO |
| TXP_10 | AF26 | AO |

6. Pin Descriptions

6.1. DDR3 SDRAM Interface

Table 3. DDR3 SDRAM Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-----------------------|---|---|------|---------------|---|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | | |
| MD[15:0] | M25, G26, M26, H25, N25, G25, N26, F26, D25, R25, D26, R26, E25, P26, E26, P25 | M25, G26, M26, H25, N25, G25, N26, F26, D25, R25, D26, R26, E25, P26, E26, P25 | I/O | | Data Input/Output: Bi-directional data bus. These pins must be floating when not used. |
| MA[13:0] | B20, B23, B24, C25, A20, A25, A19, A26, B18, B25, A18, A21, A24, B21 | B20, B23, B24, C25, A20, A25, A19, A26, B18, B25, A18, A21, A24, B21 | O | | Address Outputs. |
| MBA[2:0] | A22, B26, B17 | A22, B26, B17 | O | | Bank Address Outputs. |
| MLDM | F25 | F25 | O | | Data Masks for lower-byte. |
| MHDM | L26 | L26 | O | | Data Masks for upper-byte. |
| MRAS#, MCAS#, MWE# | A23, A16, B22 | A23, A16, B22 | O | | Command Outputs: MRAS#, MCAS#, MWE# (along with MCS#) define the command being entered. |
| MCS0# | A17 | A17 | O | | Chip Select: MCS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. |
| MCK_P, MCK_N | J26 K25 | J26 K25 | O | | Clock: MCK_P and MCK_N are differential clock outputs. |
| MCKE | C26 | C26 | O | | Clock Enable: MCKE HIGH activates. |
| MLDQS_P, MLDQS_N | L25 K26 | L25 K26 | I/O | | Lower byte data strobe. These pins must be floating when not used. |
| MHDQS_P MHDQS_N | J25 H26 | J25 H26 | I/O | | Upper byte data strobe. These pins must be floating when not used. |
| MRST# | B19 | B19 | O | | Active Low Reset. |
| MODT | B15 | B15 | O | | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. |
| MZQ | A15 | A15 | I | | External reference ball for output drive calibration. This pin must be floating when not used. |

6.2. SPI Master Interface

Table 4. SPI Master Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-----------------|----------------------------|--------------------------|------|---------------|--|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| SPI_MST_CS[1:0] | A13, B10 | A13, B10 | O | | Chip select 1-0. |
| SPI_MST_SCLK | B12 | B12 | O | | Clock output. |
| SPI_MST_SDI | A12 | A12 | I/O | | Serial data output (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O). This pin must be floating when not used. |
| SPI_MST_SDO | A11 | A11 | I/O | | Serial data input (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O). This pin must be floating when not used. |
| SPI_MST_SIO2 | B11 | B11 | I/O | | Serial data input & output (for 4Xi/O). This pin must be floating when not used. |
| SPI_MST_SIO3 | A10 | A10 | I/O | | Serial data input & output (for 4Xi/O). This pin must be floating when not used. |

6.3. UART Interface

Table 5. UART Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|------------|----------------------------|--------------------------|------|---------------|--|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| UART0_TXD | B9 | B9 | O | | UART0 Interface Transmit Data. |
| UART0_RXD | A9 | A9 | I | | UART0 Interface Receive Data. This pin must be pulled high with a 10K ohm resistor when not used. |
| UART0_RTSN | A8 | A8 | O | | UART0 Interface Request to Send. |
| UART0_CTSN | B8 | B8 | I | | UART0 Interface Clear to Send. This pin must be pulled low with a 1K ohm resistor when not used. |
| UART1_TXD | B6 | B6 | O | | UART1 Interface Transmit Data. |
| UART1_RXD | A5 | A5 | I | | UART1 Interface Receive Data. This pin must be pulled high with a 10K ohm resistor when not used. |
| UART1_RTSN | A6 | A6 | O | | UART1 Interface Request to Send. |

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|------------|----------------------------|--------------------------|------|---------------|---|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| UART1_CTSN | A7 | A7 | I | | UART1 Interface Clear to Send. This pin must be pulled low with a 1K ohm resistor when not used. |

6.4. EJTAG Interface

Table 6. EJTAG Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-----------|----------------------------|---------------------------|------|---------------|---|
| | RTL8393M(48G+ 4G Combo) | RTL8393M(48G+ 2 SGMII) | | | |
| JTAG_TMS | A6 | A6 | I | | JTAG Test Mode Select. This pin must be floating when not used. |
| JTAG_TCK | A7 | A7 | I | | JTAG Test Clock Input. This pin must be floating when not used. |
| JTAG_TRST | B5 | B5 | I | | JTAG Test Reset. <i>Note: The pin must be external pulled down via a 1Kohm resistor.</i> This pin must be floating when not used. |
| JTAG_TDI | A5 | A5 | I | | JTAG Test Data Input. This pin must be floating when not used. |
| JTAG_TDO | B6 | B6 | O | | JTAG Test Data Output. |

6.5. GPIO Interface

Table 7. GPIO Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|------------|---|---|------|---------------|--|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| GPIO[23:0] | A4, A3, B3, A2, A1, B2, B1, C2, C1, D2, D1, H1, A10, B11, A14, B13, B6, A5, B5, A7, A6, F2, F1, G2 | A4, A3, B3, A2, A1, B2, B1, C2, C1, D2, D1, H1, A10, B11, A14, B13, B6, A5, B5, A7, A6, F2, F1, G2 | I/O | | General Purpose Input/Output. Provides configurable I/O ports that can be configured for either input or output. These pins must be floating when not used. GPIO[5] can't connect with internal pull high device. |

6.6. SGMII Interface

Table 8. SGMII Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|---------------------------|----------------------------|--------------------------|------|---------------|---|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| TXP_13/ TXN_13 | W25 W26 | W25 W26 | AO | | SGMII 1 (1.25G) Transmit Data Differential Output Pair. |
| RXP_13/ RXN_13 | V25 V26 | V25 V26 | AI | | SGMII 1 (1.25G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |
| REFCLKP_13/ REFCLKN_13 | V24 W24 | V24 W24 | AO | | Reference Clock (625M) output for SGMII 1 Interface. |
| TXP_12/ TXN_12 | - - | AA26 AA25 | AO | | SGMII 0 (1.25G) Transmit Data Differential Output Pair. |
| RXP_12/ RXN_12 | - - | Y26 Y25 | AI | | SGMII 0 (1.25G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |
| REFCLKP_12/ REFCLKN_12 | - | Y24 AA24 | AO | | Reference Clock (625M) output for SGMII 0 Interface. |

6.7. 100/1000BASE-FX Interface

Table 9. 100/1000BASE-FX Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-------------------|----------------------------|--------------------------|------|---------------|---|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| TXP_13/ TXN_13 | W25 W26 | W25 W26 | AO | | 100/1000BASE-FX 1 (1.25G) Transmit Data Differential Output Pair. |
| RXP_13/ RXN_13 | V25 V26 | V25 V26 | AI | | 100/1000BASE-FX 1 (1.25G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |
| TXP_12/ TXN_12 | - - | AA26 AA25 | AO | | 100/1000BASE-FX 0 (1.25G) Transmit Data Differential Output Pair. |
| RXP_12/ RXN_12 | - - | Y26 Y25 | AI | | 100/1000BASE-FX 0 (1.25G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |

6.8. QSGMII Interface

Table 10. QSGMII Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-------------------------|---|---|------|---------------|---|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| TXP[11:0]/ TXN[11:0] | AD25, AF26, AE22, AF19, AE16, AF13, AE6, AF3, AE2, AB1, W2, U1/ AD26, AF25, AF22, AE19, AF16, AE13, AF6, AE3, AE1, AB2, W1, U2 | AD25, AF26, AE22, AF19, AE16, AF13, AE6, AF3, AE2, AB1, W2, U1/ AD26, AF25, AF22, AE19, AF16, AE13, AF6, AE3, AE1, AB2, W1, U2 | AO | | QSGMII[11:0] (5G) Transmit Data Differential Output Pair. |
| RXP[11:0]/ RXN[11:0] | AC25, AE26, AE23, AF20, AE17, AF14, AE7, AF4, AF2, AC1, Y2, V1/ AC26, AE25, AF23, AE20, AF17, AE14, AF7, AE4, AF1, AC2, Y1, V2 | AC25, AE26, AE23, AF20, AE17, AF14, AE7, AF4, AF2, AC1, Y2, V1/ AC26, AE25, AF23, AE20, AF17, AE14, AF7, AE4, AF1, AC2, Y1, V2 | AI | | QSGMII[11:0] (5G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |
| TXP_12/ TXN_12 | AA26/ AA25 | - - | AO | | QSGMII_12 (5G) Transmit Data Differential Output Pair. |
| RXP_12/ RXN_12 | Y26/ Y25 | - - | AI | | QSGMII_12 (5G) Receive Data Differential Input Pair. These pins must be tied to ground when not used. |

6.9. LED Interface

Table 11. LED Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|----------|----------------------------|--------------------------|------|---------------|---------------------------------------|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| LED_SCK | G1 | G1 | O | | Controller Clock for Serial LED Mode. |
| LED_SDA | H2 | H2 | O | | Controller Data for Serial LED Mode. |
| SYS_LED | G2 | G2 | O | | System LED. |

6.10. SPI Slave Interface

Table 12. SPI Slave Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|-------------|----------------------------|--------------------------|------|---------------|--|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | | |
| SPI_SLV_CSN | J2 | J2 | I | | Chip select. This pin must be floating when not used. |

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|--------------|------------------------|-----------------------|------|------------|--|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | | |
| SPI_SLV_SCLK | K1 | K1 | I | | Clock input. This pin must be floating when not used. |
| SPI_SLV_SDI | K2 | K2 | I | | Serial data input. This pin must be floating when not used. |
| SPI_SLV_SDO | J1 | J1 | O | | Serial data output. |

6.11. EEPROM SMI Slave Interface

Table 13. EEPROM SMI Slave Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|----------|------------------------|-----------------------|------|------------|--|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | | |
| I2C_SCK | K1 | K1 | I | | Clock input. This pin must be floating when not used. |
| I2C_SDA | K2 | K2 | I/O | | Data input/output. This pin must be floating when not used. |

6.12. Miscellaneous Interface

Table 14. Miscellaneous Interface Pins

| Pin Name | Pin No. | | Type | Drive (Ma) | Description |
|----------|------------------------|-----------------------|------|------------|--|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | | |
| MDC_0 | L1 | L1 | O | | MII 0 Management Interface Clock Pin. |
| MDIO_0 | L2 | L2 | I/O | | MII 0 Management Interface Data Pin. This pin must be floating when not used. |
| MDC_1 | U26 | U26 | O | | MII 1 Management Interface Clock Pin. |
| MDIO_1 | U25 | U25 | I/O | | MII 1 Management Interface Data Pin. This pin must be floating when not used. |
| XI | AF9 | AF9 | AI | | 25MHz Crystal Clock Input Pin. |
| XO | AF10 | AF10 | AO | | 25MHz Crystal Clock Output Pin. |
| RESET | U24 | U24 | AI | | System Pin Reset Input. |
| IBREF | R24 | R24 | AI/O | | Reference Resistor for BG. A 3KΩ (1%) resistor should be connected between IBREF and GND. |
| PWRMON | P24 | P24 | AI | | For power monitor used. This pin must be floating when not used. |
| INT | B4 | B4 | O | | Interrupt. |

| Pin Name | Pin No. | | Type | Drive (mA) | Description |
|-----------------------------|--|---|------|------------|--|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | | |
| 25M_CLK [10, 8, 6, 4, 2, 0] | AF24, AF18, AF12, AD3, AA1, T1 | AF24, AF18, AF12, AD3, AA1, T1 | AO | | 25M clock output. |
| 25M_CLK_12 | AB26 | - | AO | | 25M clock output. |
| RESERVE_D | B7, J23, K23, P1, R1, T24, Y23, AD2, C3-C12, D3-D12, E3, E4, F3, F4, G3, G4, H3, H4, E1, W3, AD1, AF5, AF15, AF21, AD24, W23, AD19, AD20, AD22, AD23, Y24, AA24, R23, T25, T26 | B7, J23, K23, P1, R1, T24, Y23, AD2, C3-C12, D3-D12, E3, E4, F3, F4, G3, G4, H3, H4, E1, W3, AD1, AF5, AF15, AF21, AD24, AB26, W23, AD19, AD20, AD22, AD23, R23, T25, T26 | | | Reserved. Must be floating in normal operation. |
| RESERVE_D | N24, P23 | N24, P23 | | | Reserved. Must be pulled low with a 1K ohm resistor in normal operation. |
| RESERVE_D | L23 | L23 | | | Reserved. Must be pulled high with a 10K ohm resistor in normal operation. |
| RESERVE_D | E2 | E2 | | | Reserved. Must be floating in normal operation. |

6.13. Configuration (Pin Strapping Function)

Table 15. Configuration Strapping Pins

| Pin Name | Pin No. | | Default | Description |
|-------------------|------------------------|-----------------------|---------|---|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | |
| DDR_CLK_SEL[2:0] | N23, U26, L1 | N23, U26, L1 | 0b000 | Select DDR clock frequency. 0b00: Disable DDR clock output 0b001: 175MHz 0b010: 275MHz 0b011: 375MHz 0b100: 50MHz 0b101: 100MHz 0b110: 133MHz 0b111: 193MHz |
| DDR_TYPE_SEL[1:0] | G1, J1 | G1, J1 | 0b00 | Select DDR type. 0b00: Reserved 0b01: Reserved 0b10: DDR3 0b11: Reserved |
| EXT_CPU_EN | B4 | B4 | 0b0 | Enable external CPU. 0b0: Disable 0b1: Enable |

| Pin Name | Pin No. | | Default | Description |
|-----------------|-------------------------|-----------------------|---------|--|
| | RTL8393M(48G+4 G Combo) | RTL8393M(48G+2 SGMII) | | |
| SYS_LED_EN | B9 | B9 | 0b1 | Enable system LED. 0b0: Disable 0b1: Enable |
| REG_IF_SEL | A8 | A8 | 0b0 | Select Register Access Interface. 0b0: Register can only be accessed by EEPROM SMI Slave interface 0b1: Register can only be accessed by SPI Slave interface |
| LED_EN | L24 | L24 | 0b0 | Enable LED. 0b0: Disable 0b1: Enable |
| SPI_MODE_SEL | K4 | K4 | 0b0 | SPI flash mode selection. 0b0: 3-byte mode 0b1: 4-byte mode |
| MODE_SEL | K3 | K3 | 0b0 | Chip mode selection. 0b0: 48G+4G 0b1: 48G+2SGMII |
| LED_IF_SEL[1:0] | J3, J4 | J3, J4 | 0b00 | LED interface selection. 0b00: Serial LED 0b01: Single color scan LED 0b10: Bi-color scan LED 0b11: Reserved |

6.14. Power and GND

Table 16. Power and GND Pins

| Pin Name | Pin No. | | Type | Description |
|----------|---|--|------|--|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | |
| SVDD33 | U3, U4, V3, V4, W4, Y3, Y4, AA4, AA23, AB23, AC20, AC21, AC22, AC23 | U3, U4, V3, V4, W4, Y3, Y4, AA4, AA23, AB23, AC20, AC21, AC22, AC23 | SP | 3.3V Power for SERDES. |
| SVDD10 | AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AE12 | AC8, AC9, AC10, AC11, AC12, AC13, AC18, AC19, AD9, AD10, AD11, AD12, AD13, AD18, AE12 | SP | 1.1V Power for SERDES. |
| SVDD10_1 | NA | AC14, AC15, AC16, AC17, AD14, AD15, AD16, AD17 | SP | 1.1V Power for SGMII or 100/1000Base-FX |
| AVDD33 | V23, AC7 | V23, AC7 | AP | 3.3V Power for Analog. |
| AVDD10 | U23, AD8 | U23, AD8 | AP | 1.1V Power for Analog. |
| DVDD33 | P2, P3, P4, R2, R3, R4, T2, T3, T4 | P2, P3, P4, R2, R3, R4, T2, T3, T4 | DP | 3.3V Digital Power for I/O Pins |
| DVDD10 | L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12 | L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12 | DP | 1.1V Digital Power for Digital Core Voltage. |

| Pin Name | Pin No. | | Type | Description |
|----------|---|---|------|---|
| | RTL8393M(48G+4G Combo) | RTL8393M(48G+2 SGMII) | | |
| MDVDD | B14, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, D19 | B14, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, D19 | MP | Power for DDR SDRAM. |
| MVREF | J24, K24 | J24, K24 | RP | Reference voltage for data for DDR SDRAM. |
| DGND | C19, C20, C21, C22, C23, C24, D20, D21, D22, D23, D24, E23, E24, F23, F24, G23, G24, H23, H24, L3, L4, M1, M2, M3, M4, N1, N2, N3, N4, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16 | C19, C20, C21, C22, C23, C24, D20, D21, D22, D23, D24, E23, E24, F23, F24, G23, G24, H23, H24, L3, L4, M1, M2, M3, M4, N1, N2, N3, N4, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16 | DG | Digital Ground. |
| SGND | AA2, AA3, AB3, AB4, AB24, AB25, AC3, AC4, AC5, AC6, AC24, AD4, AD5, AD6, AD7, AD21, AE5, AE8, AE11, AE15, AE18, AE21, AE24, AF8, AF11 | AA2, AA3, AB3, AB4, AB24, AB25, AC3, AC4, AC5, AC6, AC24, AD4, AD5, AD6, AD7, AD21, AE5, AE8, AE11, AE15, AE18, AE21, AE24, AF8, AF11 | SG | SERDES Ground. |
| AGND | T23, AE9, AE10 | T23, AE9, AE10 | AG | Analog Ground. |

7. Switch Function Description

7.1. Hardware Reset and Software Reset

7.1.1. Hardware Reset

Hardware reset forces the RTL8393M to start the initial power-on sequence. At first hardware will strap pins to give all default values when the ‘RESET’ signal terminates. Next the configuration is cleared to chip default, and then the complete SRAM BIST (Built-In Self Test) process is run. Finally the packet buffer descriptors are initialized and internal registers can be accessed by internal /external CPU.

7.1.2. Software Reset

The RTL8393M supports three software resets, CPU&Memory reset, Software NIC reset, and Software Switch reset. Reset sources are the signals that will trigger the reset command to the chip. All reset signals are low active.

- CPU & Memory reset: Resets MIPS 34Kc + Memory Controller + Peripheral + LXB + NIC.
- Software NIC reset: Resets NIC interface between CPU and Switch.
- Software Switch reset: Resets whole switch core.

7.2. Layer 2 Learning and Forwarding

The RTL8393M has a 4K-entry VLAN table which is used by 802.1Q and Q-in-Q VLAN. It supports 256 FID (Filtering Database ID) in total. IVL (Individual VLAN Learning), SVL (Shared VLAN learning) and IVL/SVL mixed mode are supported and per VLAN basis can specify the VLAN learning mode for unicast/broadcast and L2/IP multicast traffic respectively.

7.2.1. Forwarding

IP multicast data packets involve L2 and multicast group table lookup. If the L2 table lookup returns a hit, the data packet is forwarded to all member ports and router ports retrieved from multicast group table. If the multicast address is not stored in the address table (i.e., lookup miss), the packet is broadcast to all ports of the broadcast domain. The VLAN Frame Forwarding Rules are defined as follows:

- The received unknown unicast/unknown multicast/broadcast frame will be flooded to VLAN member ports and the source port is excluded.
- The received known unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

7.2.2. Learning

The RTL8393M features a 16K-entry Layer 2 table. It uses a 4-way hash structure to store L2 entries. Each entry can be recorded in three formats, L2 Unicast, L2 Multicast, and IP Multicast. The L2 Unicast and Multicast hash key is (FID/VID, MAC) and the IP Multicast hash key is (SIP, GIP) or (FID/VID, GIP).

The learnt unicast entries are aged out after the specified aging period. The RTL8393M per port supports a configuration to disable the aging out function.

7.3. Layer 2 Learning Constraint

The RTL8393M supports system-based, port-based, and VLAN-based layer 2 learning constraint. The function is to limit the number of learnt MAC address on the system, particular port and particular VLAN.

For system-based learning constraint, there is configuration for user to define the MAC address number that the system can learn. For port-based learning constraint, each port has a configuration to define the MAC address number that the port can learn. For VLAN-based learning constraint, there are 32 configurations supported to define the MAC address number that the particular VLAN can learn.

The packets are dropped, forwarded, or trapped to the CPU when the learnt L2 entries number reaches the limited number. Three learning constraint functions can work simultaneously and the action priority is VLAN-based > Port-based > System-based if the learning constraint actions are triggered at the same time.

7.4. Port Isolation

Port Isolation function is used to control whether the hosts can communicate with each other or not.

If we set the register to cut the connection between hosts, all packets from a host (downlink port) cannot be transmitted to another host directly. These packets can only be transmitted by passing through the router (uplink port) as below illustration.

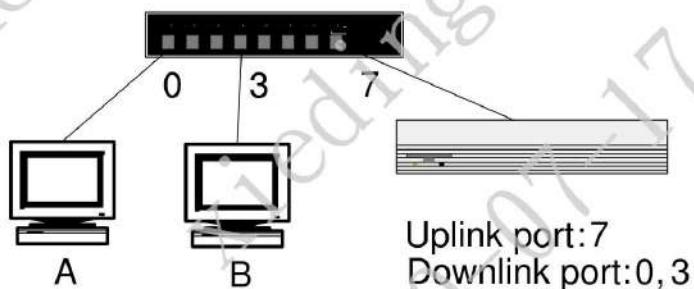


Figure 11. Port Isolation Example

Port-based port isolation is archived by providing a port mask configuration for each ingress port. The port mask is used to indicate the ports that allow forwarding the traffic.

The Mirroring function is not limited by the port isolation port mask, that is, mirroring port doesn't have to be within the port mask.

In addition to port-based port isolation, there are 16 VLAN-based port isolation configurations supported in RTL8393M. Each configuration can specify the VLAN ID, Port Mask, and the enable state. The port mask definition of VLAN-based port isolation is different from port-based port isolation. Ports configured as 1 in this port mask could communicate with all ports belonging to the same specified VLAN while ports configured as 0 could only communicate with ports configured as 1 belonging to the same specified VLAN.

7.5. Layer 2 Multicast and IP Multicast

There are two IP multicast frame types supported in RTL8393M: IPv4 multicast and IPv6 multicast.

An IPv4 multicast frame must satisfy two conditions:

- The type must be IPv4
- DMAC =01-00-5E-XX-XX-XX

An IPv6 multicast frame must satisfy two conditions:

- The type must be IPv6
- DMAC =0x33-33-XX-XX-XX-XX

A packet is deemed a L2 multicast packet if it is not an IP multicast packet and DMAC [40]=1.

The RTL8393M supports IGMPv1/2/3 and MLDv1/2. IGMP/MLD control packets can be trapped to CPU for software to insert an IP multicast entry into the L2 table.

7.6. Reserved Multicast Address

There are some Reserved Multicast Address (RMA) definitions in the IEEE 802.1 standard. The RTL8393M includes 01-80-C2-00-00-00~01-80-C2-00-00-2F and two user defined RMA support. For each RMA, the actions include: Table lookup, Drop, and Trap to CPU. Some of them have options to bypass ingress VLAN filtering and ingress spanning tree filtering if the action is set to "Trap to CPU".IEEE 802.1d/1w/1s (STP/RSTP/MSTP)

There are 256 spanning tree instances supported by the RTL8393M. The CPU will create a different Port State for different spanning tree instances at each port. The RTL8393M assigns a VID for a received packet, and look up the VLAN table to retrieve the Multiple Spanning Tree Instances (MSTI). Then it follows the port's MSTI state to complete its corresponding ingress/egress check. The Spanning Tree and Rapid Spanning Tree port states are shown in Figure 12.

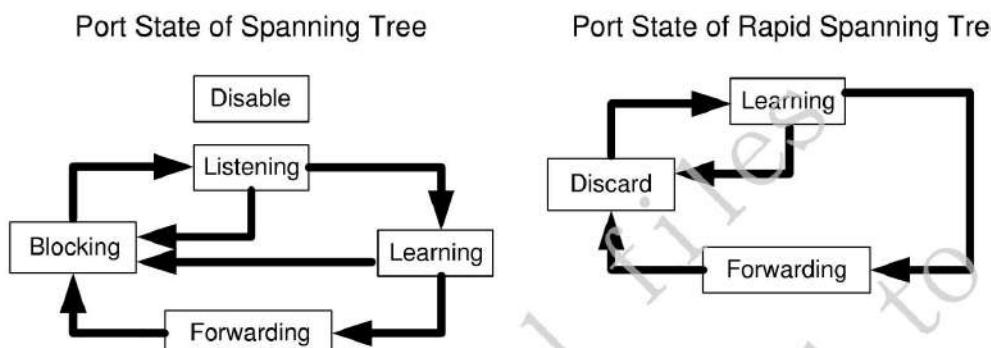


Figure 12. Spanning Tree and Rapid Spanning Tree Port States

When using IEEE 802.1D/1w/1s, the RTL8393M supports four states for each port per instance:

- Disabled

Except for software forwarding, the port will not transmit/receive packets, and will not perform learning.

- Blocking/Listening

Except for software forwarding, the port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

- Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

- Forwarding

The port will transmit/receive all packets, and will perform learning.

7.7. IEEE 802.1Q and Q-in-Q VLAN

The RTL8393M has a 4K-entry VLAN table which is used by 802.1Q and Q-in-Q VLAN. Up to three layer VLAN tags (Outer Tag, Inner Tag, Extra Tag) are supported for Q-in-Q applications. The device supports four outer TPIDs, four inner TPIDs and one extra TPID which are all configurable and per port has a TPID mask to select the recognized TPID. For VLAN tag manipulation, VLAN untag set and the egress port tag status configurations are coordinated for determining the tag status for a packet.

Per ingress port can specify the forwarding VLAN is either from inner tag or outer tag. Forwarding VLAN is used for doing VLAN table lookup and ingress/egress VLAN filtering. In Q-in-Q application, outer VLAN ID is used as forwarding VLAN ID for both downlink and uplink ports as well as the inner VLAN ID is used in traditional VLAN application.

The RTL8393M also supports eight protocol-based, 1K MAC-based/IP-subnet-based, and application-based VLANs.

7.8. Ingress and Egress VLAN Translation

The RTL8393M supports 1K ingress and 1K egress VLAN translation table. They are used to support the 1:1 and port-based N:1 VLAN translation. For MAC-based N:1 VLAN translation, per egress port has a configuration to enable the function. In addition to the dedicated VLAN translation tables, VLAN translation can also be done by ACL.

7.9. IEEE 802.3ad Link Aggregation

The RTL8393M supports 802.3ad (Link Aggregation) for 16 groups of link aggregators with up to 8 ports per-group. Link aggregation group frames are sent to an aggregation port of the link aggregation group according to a distribution algorithm. Four trunk distribution algorithms are supported and per group can bind to a specific distribution algorithm. The parameters of the distribution algorithm are: Source port, SMAC, DMAC, SIP, DIP, L4 source port, L4 destination port, Source port&SMAC.

Each trunk group can optionally separate the known multicast and flooding traffic to the MSB port. Besides, H/W fail-over is also supported to prevent forwarding traffic to a link down port.

7.10. Mirroring and Sampling

There are four mirror configurations supported in RTL8393M. Each mirror configuration can specify the ingress and egress mirrored ports, mirroring port, isolation state, and enable state. Normal forwarding packet can't be forwarded to mirroring port if isolation state is enabled. The mirrored traffic can across VLAN, that is, mirrored port and mirroring port can reside in different VLANs.

If multiple mirrored ports are matched for a multiple egress port packet, the packet transmitted through the lowest mirrored port ID is duplicated to the mirroring port. The mirroring port drops the mirrored traffic instead of triggering the flow control if it is congested.

The RTL8393M supports ingress and egress port sFlow sampling. Each ingress and egress port can specify the sample rate for packet sampling and a corresponding trap reason is carried when the packet is sampled to CPU.

Flow-based mirroring and sampling can be supported by ACL.

7.11. Attack Prevention

Most common attacks can be blocked by RTL8393M includes LAND attack, UDP Blat attack, TCP Blat attack, Ping of Death attack, Smurf attack, TCP NULL scan and so on. The attack prevention function is per port enabled and each attack type is globally enabled. Each attack type packet can be selected to drop or trap to CPU for further processing.

7.12. PIE (Packet Inspection Engine)

PIE is a 2K+256-entry search engine that is divided into 18 blocks (block numbers are 0~17). Each block contains 128 entries. There is a register to indicate whether these 18 blocks are ingress or egress ACL. If the block number is smaller than the register value, then the block is an ingress ACL block. If the block number is larger than or equal to the register value, then this block is an egress ACL block. For example: if the register value is 3, then blocks 0~2 are ingress ACL blocks, and blocks 3~17 are egress ACL blocks.

7.12.1. Ingress ACL

The ingress ACL function supports packet drop/permit/redirect/copy to CPU, log, mirror, policing, ingress inner VLAN assignment, ingress outer VLAN assignment, priority assignment, and bypass functionalities. When a PIE memory block is configured to ingress ACL, it will execute the corresponding actions when a packet hits the entry.

Each ingress ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries match), these matched actions will be divided into different action groups. Each group will then execute the lowest address entry corresponding action.

7.12.2. Egress ACL

The egress ACL function supports packet drop/permit/redirect/copy to CPU, log, mirror, policing, egress inner VLAN assignment, egress outer VLAN assignment, priority assignment, QoS remarking and egress tag status assignment functionalities. When a PIE memory block is configured to egress ACL, it will execute the corresponding actions when a packet hits the entry.

Each egress ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries match), these matched actions will be divided into different action groups. Each group will then execute the lowest address entry corresponding action.

7.12.3. Log Counter

The RTL8393M supports 1K 64-bit byte counters or 2K 32-bit packet counters which are divided into 16 blocks. Counters belong to different blocks can be increased concurrently, thus, up to 16 counters can be increased concurrently. One limitation is that ingress and egress ACL can't share the same counter block.

7.13. Traffic Suppression

The priority sequence for traffic suppression is:

1. Ingress bandwidth control
2. ACL policing
3. Storm control

7.13.1. Input Bandwidth Control

The RTL8393M supports ingress bandwidth control configuration for each port. The bandwidth setting ranges from 16Kbps~1Gbps. The granularity is 16Kbps, and each port has a 16-bit register to control the bandwidth. If the receiving packet rate is faster than the bandwidth setting, it can optionally send a ‘Pause

ON' packet to slow the link partner transmissions. For out of profile detection, per port supports a EXCEED flag to indicate whether the traffic rate ever over the bandwidth setting.

7.13.2. ACL Policing

The RTL8393M supports 512 policers which are divided into 16 blocks. Policers belong to different blocks can be executed concurrently, thus, up to 16 policers can be executed concurrently to support hierarchy policing. The policer is flow controlled via leaky bucket. The rate ranges from 16Kbps~1Gbps with 16Kbps granularity and each policer entry has a 16-bit register to control the rate value.

Each ACL entry has an index to point to 512 ACL policers. One limitation is that ingress and egress ACL can't share the same policer block.

7.13.3. Storm Control

The per-port L2 storm filtering control mechanism suppresses the flow rate of storm packets. The RTL8393M supports five control types: Unknown Unicast, Unicast, Unknown Multicast, Multicast and Broadcast Storm. The definitions of five traffic types are:

- Unknown Unicast : If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet. The failure in L2 unicast table DA look-up is what called "Unknown Unicast".
- Unicast : If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet.
- Unknown Multicast : If the I/G bit of DMAC address (DMAC[40]) is 1, it is a multicast packet. The failure in L2 multicast table DA look-up is what called "Unknown Multicast".
- Multicast : The success of in L2 multicast table DA look-up for a multicast packet is called the "Known Multicast". System's Multicast Storm Filtering Control includes Unknown and Known Multicast.
- Broadcast : DMAC = FF-FF-FF-FF-FF-FF is called the "Broadcast packet".

The traffic rate for these five types can be set on a per-port basis and per port per control type supports a EXCEED flag to indicate whether the traffic rate ever overran. Besides, PPS (Packet-Per-Second) or BPS (Bit-Per-Second) counting mode can be selected system-wise.

7.14. Priority Decision

There are seven types of priority decision source for the RTL8393M:

- Port
- Ingress ACL
- DSCP
- Inner Tag
- Outer Tag

- MAC-based/IP-subnet-based VLAN
- Protocol-VLAN

For each receiving packet it will be given an internal priority, and the packet is then en-queued to the output queue according to its internal priority. The internal priority is from one of the seven priority source. Each priority source has a weight configuration; the priority source with larger weight is taken as the internal priority.

7.15. Packet Scheduling

The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL8393M scheduling algorithm is divided into Weighted Fair-Queuing (WFQ) and Weighted Round-Robin (WRR). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Weighted Fair-Queuing (WFQ): Byte-count
- Weighted Round-Robin (WRR): Packet-count

WFQ and WRR cannot exist at the same time. Both WFQ and WRR are round robin, from large queue ID to small.

7.16. Egress Packet Remarketing

RTL8393M Remarketing can be divided into inner 1p, outer 1p and DSCP Remarketing. Per egress port per type supports a configuration to turn on the remarking function. For inner 1p Remarketing, the remarking source can be either from internal priority or original inner 1p priority. For outer 1p Remarketing, the remarking source can be either from internal priority or original outer 1p priority. For DSCP Remarketing, the remarking source can be either from internal priority or original DSCP value.

7.17. IEEE 802.3x Flow Control

The RTL8393M supports IEEE 802.3x full duplex flow control. If the packet buffer used by a port is over the pause threshold, a pause-on frame is sent to indicate the link partner to stop the transmission. When the frame buffer used by a port drops below the pause threshold, it sends a pause-off frame. The PAUSE frame format is shown in Figure 13.

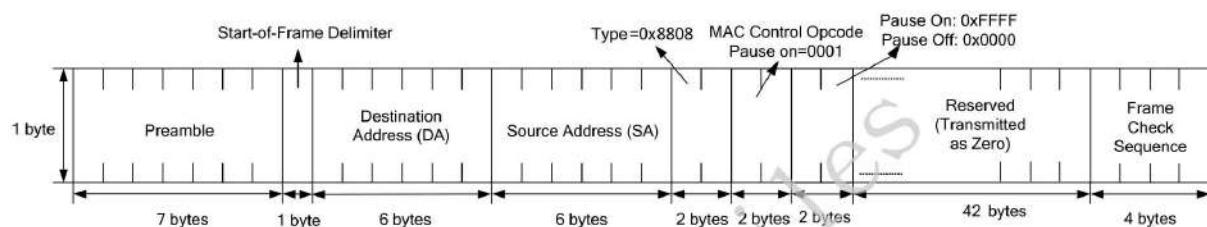


Figure 13. Tx Pause Frame Format

The flow control mechanism of the RTL8393M is implemented on the Ingress side. It counts the received pages on the Ingress side in order to determine on which port it should send out pause on/off packets.

Figure 14 shows the flow control state machine.

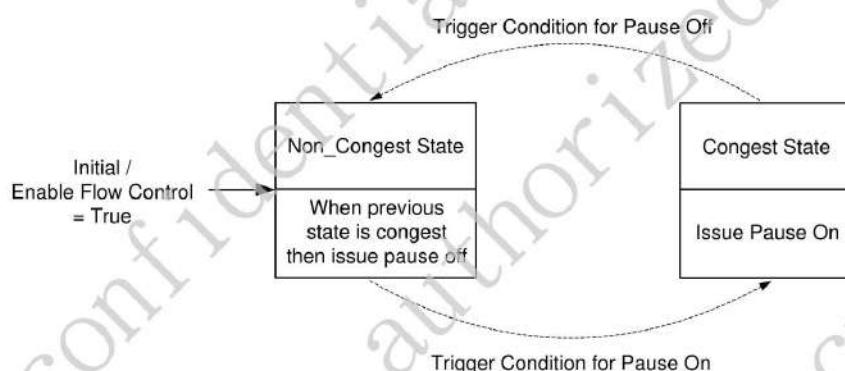


Figure 14. Flow Control State Machine

The first flow control state is ‘Non_Congest’. This is continuously monitored for the pause-on trigger condition, at which point it enters the ‘Congest’ state. In the congest state, it is continuously monitored for the pause-off trigger condition, at which point it re-enters the ‘Non_Congest’ state.

7.18. Half Duplex Backpressure

There are two mechanisms for half duplex backpressure: Collision-Based and Carrier-Based.

7.18.1. Collision-Based Backpressure (Jam Mode)

If the packet buffer used by a ingress port over the configured threshold, this mechanism forces a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- When the link partner detects the collision, it waits for a random backoff time. The RTL8393M will handle packets that are in the packet buffer during this time.
- RXDV and TXEN will be driven high. The RTL8393M will send a 4-byte Jam signal (pattern is 0xAA). Then the RTL8393M will drive TXEN low.
- When the link partner receives the Jam signal, it will feedback a 4-byte Jamming signal.
- The link partner waits for a random backoff time then re-sends the packet.

7.18.2. Carrier-Based Backpressure (Defer Mode)

If the packet buffer used by an ingress port over the configured threshold, this mechanism will send a 2k-bytes defer signal (pattern is 0xAA) to defer the other station's transmission. The RTL8393M will continuously send the defer signal until the packet buffer usage is under the threshold.

7.19. srTCM/trTCM (Single/Two Rate Three Color Marker)

The RTL8393M supports 512 ACL policers which can also be used as srTCM (Single Rate Three Color Marker) and trTCM (Two Rate Three Color Marker).

The srTCM meters a traffic stream and marks its packets according to three traffic parameters, Committed Information Rate (CIR), Committed Burst Size (CBS), and Excess Burst Size (EBS), to be either green, yellow, or red. A packet is marked green if it doesn't exceed the CBS, yellow if it does exceed the CBS, but not the EBS, and red otherwise.

The trTCM meters a traffic stream and marks its packets based on two rates, Peak Information Rate (PIR) and Committed Information Rate (CIR), and their associated burst sizes to be either green, yellow, or red. A packet is marked red if it exceeds the PIR. Otherwise it is marked either yellow or green depending on whether it exceeds or doesn't exceed the CIR.

The 512 ACL policers are divided into 16 blocks. Each block can specify the counting mode to be either PPS (Packet-Per-Second) or BPS (Bit-Per-Second) and each entry supports configurations includes policer type, PIR rate, CIR rate, and color aware mode.

The packet is marked a color by srTCM/trTCM and the color is then referenced by SWRED to perform egress random dropping for congestion avoidance.

7.20. SWRED (Simple Weighted Random Early Detection)

When SWRED is not configured, output buffers fill during periods of congestion. When the buffers are full, tail drop occurs; all additional packets are dropped. Since the packets are dropped all at once, global synchronization of TCP hosts can occur as multiple TCP hosts reduce their transmission rates. The congestion clears, and the TCP hosts increase their transmission rates, resulting in waves of congestion followed by periods where the transmission link is not fully used.

SWRED reduces the chances of tail drop by selectively dropping packets when the output interface begins to show signs of congestion. By dropping some packets early rather than waiting until the buffer is full, SWRED avoids dropping large numbers of packets at once and minimizes the chances of global synchronization. Thus, SWRED allows the transmission line to be used fully at all times.

The RTL8393M SWRED provides separate thresholds and weights for different drop precedence (0: Green, 1: Yellow, 2: Red), allowing you to provide different qualities of service for different traffic. It simplifies the calculation of packet marking probability as Figure 15.

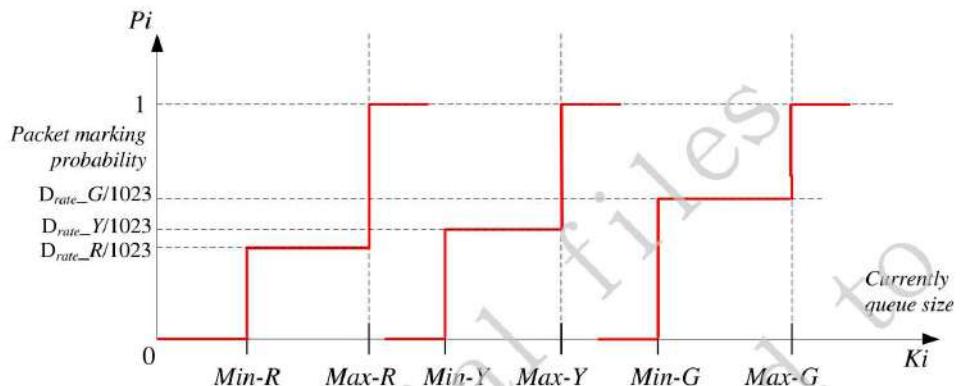


Figure 15. SWRED Packet Marking Probability of Different Drop Precedence

7.21. Management Information Base (MIB)

The supported MIB (Management Information Base) counters include:

- Ethernet-like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (Remote Network Monitoring) MIB (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

7.22. NIC and CPU Tag Forwarding

NIC interface is used for receiving packets from the CPU, or transmitting packets to the CPU. The architecture is shown in Figure 16.

When a packet is sent from the switch core to the CPU port, the CPU tag can carry status information. The CPU tag can be divided into a transmit CPU tag, and a receive CPU tag. Transmit CPU Tag can force the egress port mask while receive CPU Tag indicates the ingress port the packet came from and the reason why it is sent to CPU. If no transmit CPU tag is attached, normal L2 table lookup is taken to forward the packet.

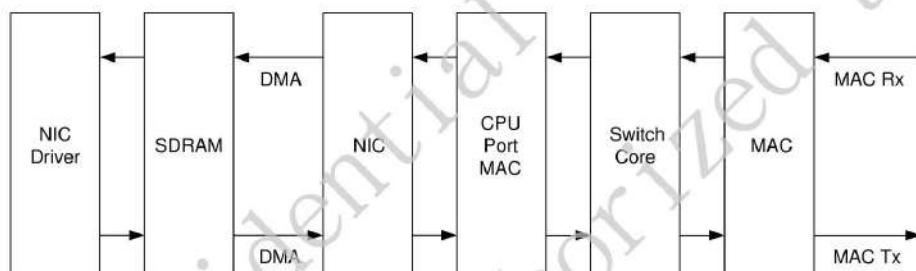


Figure 16. NIC Architecture

7.23. Table Access

The RTL8393M employs an indirect method to set the control register and the data register to complete Layer 2/VLAN/ACL Table Access:

1. Set the register to determine which table and which entry is to be accessed.
2. Determines the read or write operation.
3. Hardware executes table access.

Read: After the control register setup has been completed by software, hardware starts accessing and retrieves the data into the data register. Software then reads this data from the data register.

Write: Software puts the data in the data register and indicates the write operation in the control register. Then hardware writes the data from data register to the table.

7.24. External PHY Register Access

The RTL8393M supports PHY access control registers to indirectly access an external PHY via the MDC/MDIO interface.

7.25. OAM (Operation, Administration, Maintenance)

802.3ah OAM provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions.

The OAM loopback function supported by RTL8393M is wire-speed guaranteed and the source/destination MAC address can be swapped for the loopback packet.

When the system power is lower than a pre-defined voltage, an OAM Dying Gasp message is sent to administrator for fault indication. Hardware based Dying Gasp is sent within a very short time, thus, a large volume capacitance can be omitted to save the system cost. The OAM dying gasp application circuit is shown in Figure 17.

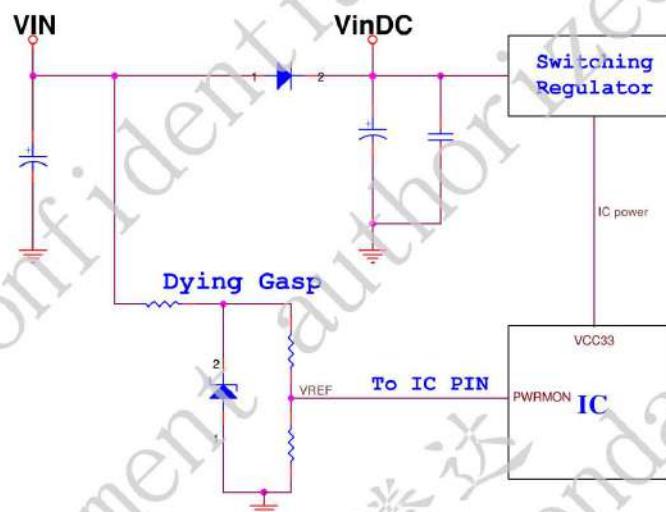


Figure 17. OAM Dying Gasp Application Circuit

The RTL8393M also supports Y.1731 ETH-DM (Ethernet Delay Measurement) to measure frame delay and frame delay variation between peers.

7.26. IEEE 1588 PTP

The Precision Time Protocol (PTP) is a protocol used to synchronize clocks throughout a computer network. On a local area network it achieves clock accuracy in the sub-microsecond range, making it suitable for measurement and control systems.

The RTL8393M supports PTPv1 and PTPv2. A hardware system time clock is provided for synchronizing the time with grandmaster clock. The transmitting and receiving timestamp of Delay Measurement and Time Synchronization packets are latched by hardware to minimize the variation. The transmitting and receiving timestamp can be retrieved from registers.

7.27. EEE

EEE proposes a low power idle (LPI) mode that MAC and PHY can shut down part of electric circuits to reduce the power consumption. If there is no traffic to be transmitted, the TX part of a port can enter LPI mode to sleep. If the link partner enters TX LPI mode, the connected port can enter RX LPI mode.

The RTL8393M per port can enable the TX/RX EEE function separately for different link speed (excludes 10Mbps).

8. CPU Function Description

8.1. MIPS-34Kc

- CPU Core
 - Up to 700MHz
 - 9-stage pipeline
 - MIPS32 and additional MIPS16e instruction set support
- Cache Configuration
 - 32KB I-Cache
 - 32KB D-Cache
- MMU Configuration
 - 4-entry ITLB
 - 4-entry DTLB
 - 32-entry JTLB

8.2. SPI Flash Controller

The RTL8393M supports serial/dual/quad SPI Flash access with below specification.

- Up to 100MHz in serial SPI Flash
- Two chip select with up to 32MB (3-byte mode), 64MB (4-byte mode)
- Programmed I/O interface and memory-mapped I/O interface for read operation is supported
- Cached read access

8.3. DDR Memory Controller

DDR3 are supported with below specification.

- 8/16 bit bus width
- Low speed DDR3 up to 400MHz (DDR3-800)
- Up to 256MB

9. Electrical AC/DC Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified referenced to GND unless otherwise specified.

Table 17. Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|--|------|------|-------|
| Junction Temperature (T _j) | - | +125 | °C |
| Storage Temperature | -45 | +125 | °C |
| DVDD33, AVDD33, SVDD33 Supply Referenced to DGND, AGND, and SGND | 2.97 | 3.63 | V |
| DVDD10, AVDD10, SVDD10, SVDD10_1 Supply Referenced to DGND, AGND, and SGND | 0.9 | 1.2 | V |
| MDVDD Supply Referenced to DGND (for DDR3) | 1.35 | 1.65 | V |

9.2. Operating Range

Table 18. Recommend Operating Range

| Parameter | Min | Typical | Max | Units |
|---|-------|---------|-------|-------|
| Ambient Operating Temperature (T _a) | 0 | - | 70 | °C |
| DVDD33, AVDD33, SVDD33 Supply Voltage Range | 3.135 | 3.3 | 3.465 | V |
| DVDD10, AVDD10, SVDD10 Supply Voltage Range | 1.05 | 1.1 | 1.15 | V |
| SVDD10_1 Supply Voltage Range (for 48G+2 SGMII) | 1.05 | 1.1 | 1.15 | V |
| MDVDD Supply Voltage Range (for DDR3) | 1.425 | 1.5 | 1.575 | V |

9.3. DC Characteristics

Table 19. DC Characteristics for 48G+4G

| Symbol | Parameter | Min | Typical | Max | Units |
|---------------------|---------------------------------------|-----|---------|-----|-------|
| I _{SVDD33} | Power Supply Current for SVDD33 | - | 116 | - | mA |
| I _{SVDD10} | Power Supply Current for SVDD10 | - | 976 | - | mA |
| I _{AVDD33} | Power Supply Current for AVDD33 | - | 22 | - | mA |
| I _{AVDD10} | Power Supply Current for AVDD10 | - | 27 | - | mA |
| I _{DVDD33} | Power Supply Current for DVDD33 | - | 10 | - | mA |
| I _{DVDD10} | Power Supply Current for DVDD10 | - | 2110 | - | mA |
| I _{MDVDD} | Power Supply Current for MDVDD | - | 48 | - | mA |
| PS | Total Power Consumption for All Ports | - | 3984.7 | - | mW |

Table 20. DC Characteristics for 48G+2SGMII

| Symbol | Parameter | Min | Typical | Max | Units |
|-----------------------|-----------------------------------|-----|---------|-----|-------|
| I _{SVDD33} | Power Supply Current for SVDD33 | - | 125 | - | mA |
| I _{SVDD10} | Power Supply Current for SVDD10 | - | 489 | - | mA |
| I _{SVDD10_1} | Power Supply Current for SVDD10_1 | - | 690 | - | mA |

| Symbol | Parameter | Min | Typical | Max | Units |
|---------------------|---------------------------------------|-----|---------|-----|-------|
| I _{AVDD33} | Power Supply Current for AVDD33 | - | 22 | - | mA |
| I _{AVDD10} | Power Supply Current for AVDD10 | - | 27 | - | mA |
| I _{DVDD33} | Power Supply Current for DVDD33 | - | 10 | - | mA |
| I _{DVDD10} | Power Supply Current for DVDD10 | - | 2110 | - | mA |
| I _{MDVDD} | Power Supply Current for MDVDD | - | 48 | - | mA |
| PS | Total Power Consumption for All Ports | - | 4272.2 | - | mW |

Table 21. DC Characteristics (DVDD33=3.3V)

| Symbol | Parameter | Min | Typical | Max | Units |
|-----------------|--------------------------|-----|---------|-----|-------|
| V _{IH} | LVTTL Input-High Voltage | 2.0 | - | - | V |
| V _{IL} | LVTTL Input-Low Voltage | - | - | 0.8 | V |
| V _{OH} | Output-High Voltage | 2.4 | - | - | V |
| V _{OL} | Output-Low Voltage | - | - | 0.4 | V |

9.4. AC Characteristics

9.4.1. Clock Characteristics

Table 22. XTALI (X!) Characteristics

| Parameter | Min | Typ | Max | Units |
|------------------------------|-----|-----|------|-------|
| Frequency of XTALI | - | 25 | - | MHz |
| Frequency Tolerance of XTALI | -50 | - | +50 | ppm |
| Duty Cycle of XTALI | 40 | - | 60 | % |
| Rise Time of XTALI | - | - | 12.5 | ns |
| Fall Time of XTALI | - | - | 12.5 | ns |
| Jitter of XTALI | - | - | 200 | ps |

9.4.2. QSGMII Differential Transmitter Characteristics

Table 23. QSGMII Differential Transmitter Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|-------------------------|-----------------------------|--------|-----|--------|-------|--|
| UI | Unit Interval | 199.94 | 200 | 200.06 | ps | $200\text{ps} \pm 300\text{ppm}$ |
| T_X1 | Eye Mask | - | - | 0.175 | UI | - |
| T_X2 | Eye Mask | - | - | 0.4 | UI | - |
| T_Y1 | Eye Mask | 200 | - | - | mV | - |
| T_Y2 | Eye Mask | - | - | 450 | mV | - |
| V _{TX-OFFSET} | Output Offset Voltage | 600 | 800 | 1000 | mV | - |
| V _{TX-DIFFp-p} | Output Differential Voltage | 400 | 700 | 900 | mV | - |
| T _{TX-EYE} | Minimum TX Eye Width | 0.65 | - | - | UI | - |
| T _{TX-JITTER} | Output Jitter | - | - | 0.35 | UI | $T_{TX-JITTER-MAX} = 1 - T_{TX-EYE-MIN} = 0.35\text{UI}$ |
| T _{TX-RISE} | Output Rise Time | 0.15 | - | - | UI | 20% ~ 80% |
| T _{TX-FALL} | Output Fall Time | 0.15 | - | - | UI | 20% ~ 80% |
| R _{TX} | Differential Resistance | 80 | 100 | 120 | ohm | - |
| C _{TX} | AC Coupling Capacitor | 80 | 100 | 120 | nF | - |
| L _{TX} | Transmit Length in PCB | - | - | 10 | inch | - |

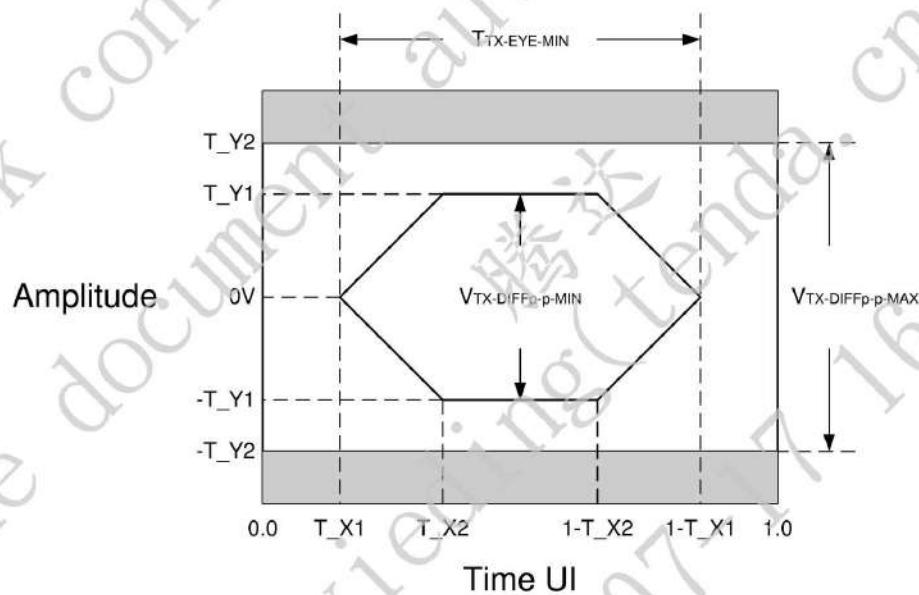


Figure 18. QSGMII Differential Transmitter Eye Diagram

9.4.3. QSGMII Differential Receiver Characteristics

Table 24. QSGMII Differential Receiver Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--------------|----------------------------|--------|-----|--------|-------|---|
| UI | Unit Interval | 199.94 | 200 | 200.06 | ps | $200\text{ps} \pm 300\text{ppm}$ |
| R_X1 | Eye Mask | - | - | 0.3 | UI | - |
| R_Y1 | Eye Mask | 100 | - | - | mV | - |
| R_Y2 | Eye Mask | - | - | 600 | mV | - |
| V_RX-DIFFp-p | Input Differential Voltage | 200 | - | 1200 | mV | - |
| TRX-EYE | Minimum RX Eye Width | 0.4 | - | - | UI | - |
| TRX-JITTER | Input Jitter Tolerance | - | - | 0.6 | UI | $\text{TRX-JITTER-MAX} = 1 - \text{TRX-EYE-MIN} = 0.6\text{UI}$ |
| R_RX | Differential Resistance | 80 | 100 | 120 | ohm | - |

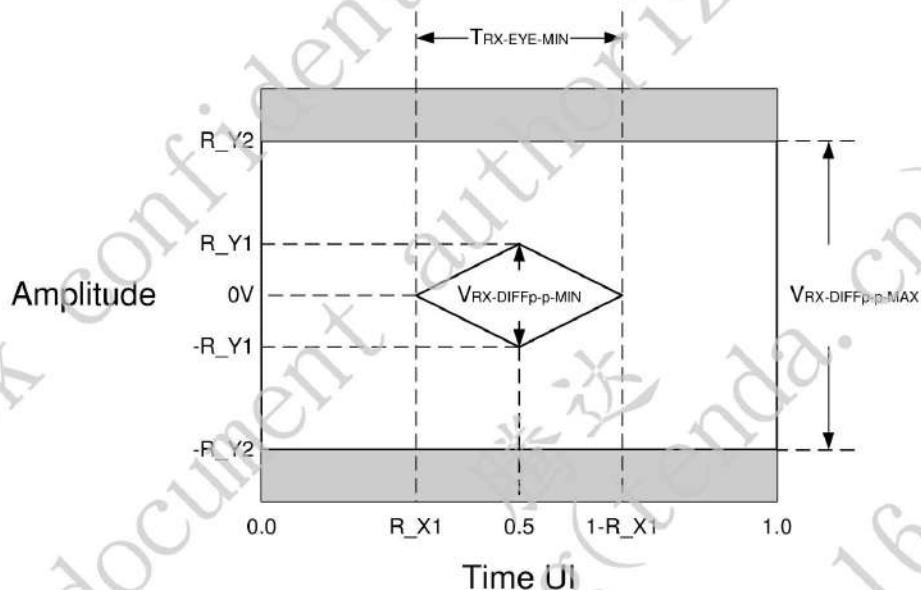


Figure 19. QSGMII Differential Receiver Eye Diagram

9.4.4. DDR3 Characteristics

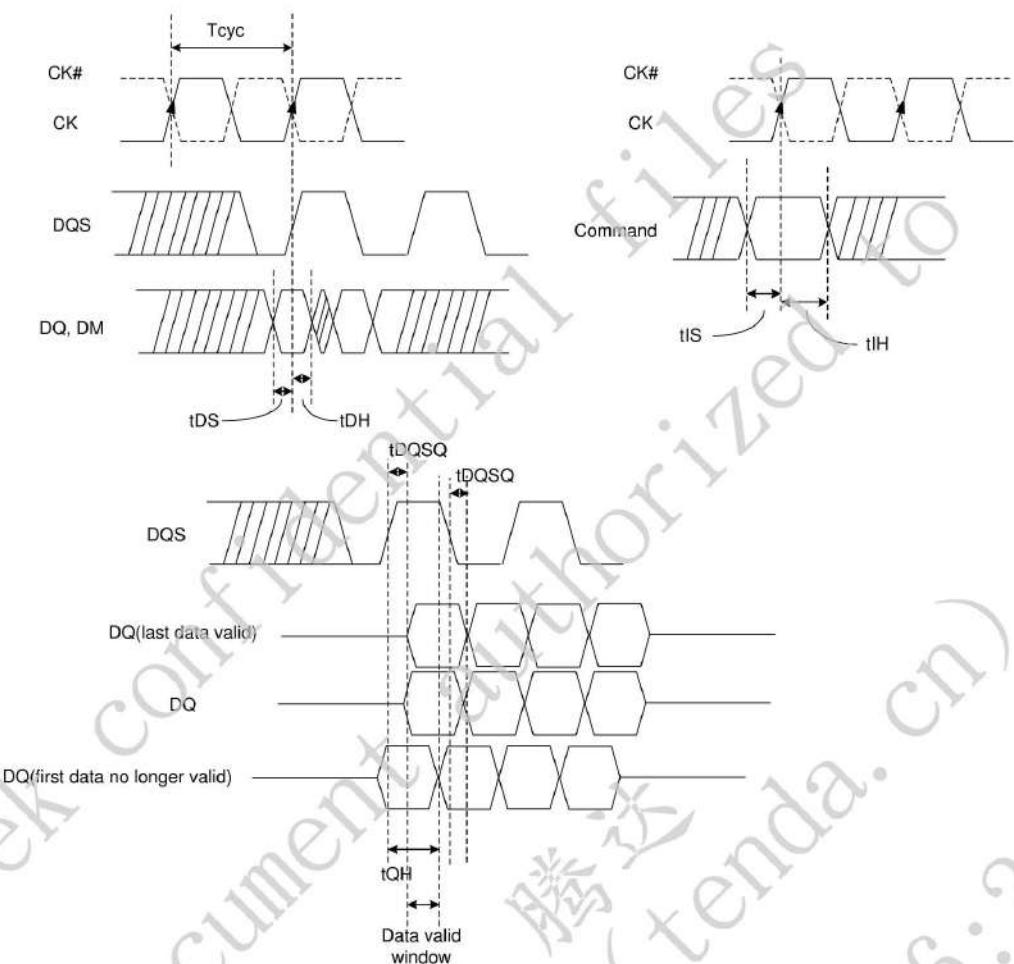


Figure 20. DDR3 Timing Illustrations

Table 25. DDR3 Timing Characteristics

| Symbol | Description | I/O | Min | Typ | Max | Units |
|--------------------|--|-----|-----|-----|-----|-------|
| $f_{CK}, f_{CK\#}$ | Clock Frequency of the CK and CK# | O | - | 400 | - | MHz |
| Duty | Duty Cycle of the CK and CK# | O | - | 50 | - | % |
| t_{DS} | DQ and DM Output Setup Time | O | 270 | - | - | ps |
| t_{DH} | DQ and DM Output Hold Time | O | 370 | - | - | ps |
| t_{IS} | Address and Control Output Setup Time | O | 692 | - | - | ps |
| t_{IH} | Address and Control Output Hold Time | O | 731 | - | - | ps |
| t_{DQSQ} | Input DQS-DQ Skew, DQS to Last DQ Valid | I | - | - | 200 | ps |
| t_{QH} | Input DQ-DQS Hold. DQS to first DQ to Go Non-Valid | I | 300 | - | - | ps |

9.4.5. SPI Flash Controller Interface Characteristics

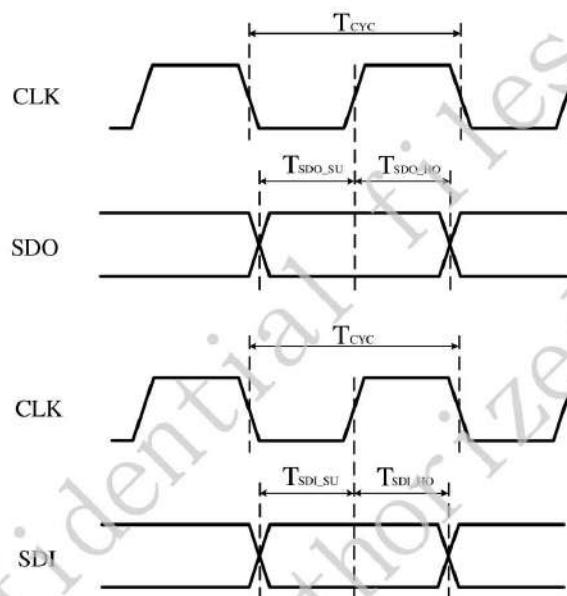


Figure 21. SPI Flash Controller Interface Timing Illustrations

Table 26. SPI Flash Controller Interface Timing Characteristics

| Symbol | Parameter | I/O | Min | Typical | Max | Units | Note |
|---------------------|-----------------------|-----|-----|---------|-----|-------|-------------------------|
| T _{CYC} | CLK Output Cycle Time | O | - | 40 | - | ns | 25MHz |
| T _{SDO_SU} | SDO Setup Time | O | - | 11.2 | - | ns | Write Command operation |
| T _{SDO_HO} | SDO Hold Time | O | - | 29.6 | - | ns | Write Command operation |
| T _{SDILSU} | SDI Setup Time | I | 5 | - | - | ns | Read Command operation |
| T _{SDILHO} | SDI Hold Time | I | 1 | - | - | ns | Read Command operation |

9.4.6. EJTAG Timing Characteristics

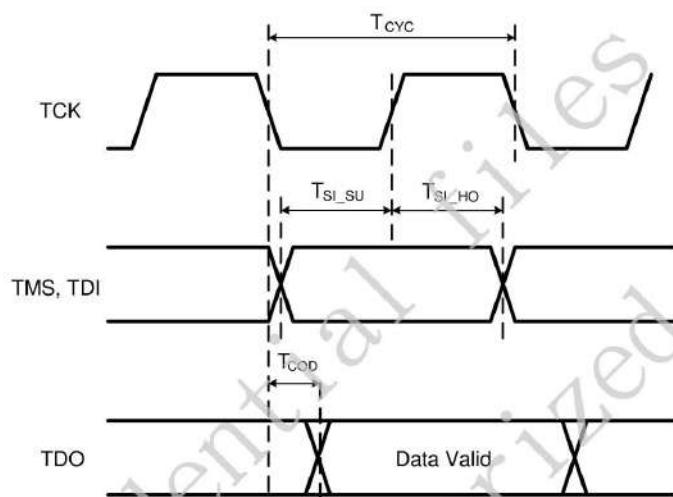


Figure 22. EJTAG Interface Timing illustrations

Table 27. EJTAG Interface Timing Characteristics

| Symbol | Parameter | I/O | Min | Typical | Max | Units |
|--------------|-------------------------|-----|-----|---------|-----|-------|
| T_{CYC} | CLK Input Cycle Time | I | 20 | | | ns |
| T_{SI_SU} | TMS and TDI Setup Times | I | 5 | | | ns |
| T_{SI_HO} | TMS and TDI Hold Times | I | 1 | | | ns |
| T_{COD} | TDO Output Delay | O | | 10.4 | | ns |

9.4.7. SMI (MDC/MDIO) Interface Characteristics

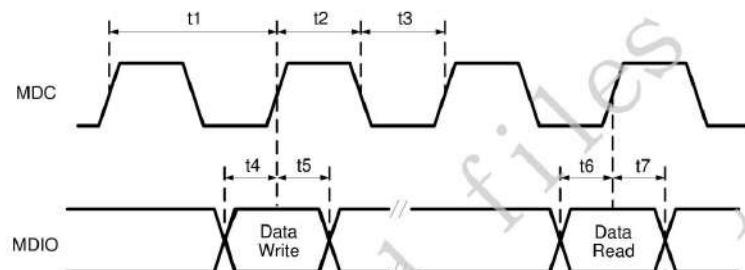


Figure 23. SMI (MDC/MDIO) Timing Illustrations

Table 28. SMI_0 (MDC/MDIO) Timing Characteristics

| Symbol | Description | Min | Typ | Max | Units |
|--------|--|-----|-----|-----|-------|
| t1 | MDC Clock Period | - | 400 | - | ns |
| t2 | MDC High Time | - | 200 | - | ns |
| t3 | MDC Low Time | - | 200 | - | ns |
| t4 | MDIO to MDC Rising Setup Time (Write Data) | - | 200 | - | ns |
| t5 | MDIO to MDC Rising Hold Time (Write Data) | - | 200 | - | ns |
| t6 | MDIO to MDC Rising Setup Time (Read Data) | 20 | - | - | ns |
| t7 | MDIO to MDC rising hold time (Read Data) | 0 | - | - | ns |

Table 29. SMI_1 (MDC/MDIO) Timing Characteristics

| Symbol | Description | Min | Typ | Max | Units |
|--------|--|-----|-----|-----|-------|
| t1 | MDC Clock Period | - | 400 | - | ns |
| t2 | MDC High Time | - | 200 | - | ns |
| t3 | MDC Low Time | - | 200 | - | ns |
| t4 | MDIO to MDC Rising Setup Time (Write Data) | - | 200 | - | ns |
| t5 | MDIO to MDC Rising Hold Time (Write Data) | - | 200 | - | ns |
| t6 | MDIO to MDC Rising Setup Time (Read Data) | 20 | - | - | ns |
| t7 | MDIO to MDC rising hold time (Read Data) | 0 | - | - | ns |

9.4.8. LED Timing Characteristics

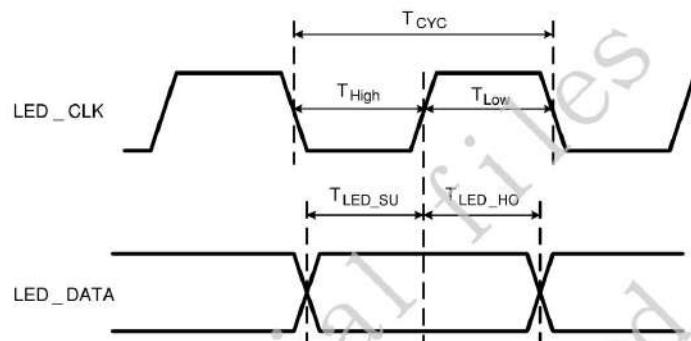


Figure 24. LED Timing Illustrations

Table 30. Serial LED Timing Characteristics

| Symbol | Description | I/O | Min | Typical | Max | Units |
|------------|---------------------------------------|-----|-----|---------|-----|-------|
| T_{CYC} | LED Clock Period | O | - | 96 | - | ns |
| T_{High} | LED High Time | O | - | 48 | - | ns |
| T_{Low} | LED Low Time | O | - | 48 | - | ns |
| T_{OSU} | LED_DATA to LED_CLK Rising Setup Time | O | - | 48 | - | ns |
| T_{OH} | LED_DATA to LED_CLK Rising Hold Time | O | - | 48 | - | ns |

Table 31. Scan Bi-Color LED Timing Characteristics

| Symbol | Description | I/O | Min | Typical | Max | Units |
|------------|---------------------------------------|-----|-----|---------|-----|-------|
| T_{CYC} | LED Clock Period | O | - | 384 | - | ns |
| T_{High} | LED High Time | O | - | 192 | - | ns |
| T_{Low} | LED Low Time | O | - | 192 | - | ns |
| T_{OSU} | LED_DATA to LED_CLK Rising Setup Time | O | - | 189 | - | ns |
| T_{OH} | LED_DATA to LED_CLK Rising Hold Time | O | - | 195 | - | ns |

Table 32. Scan Single-Color LED Timing Characteristics

| Symbol | Description | I/O | Min | Typical | Max | Units |
|------------|---------------------------------------|-----|-----|---------|-----|-------|
| T_{CYC} | LED Clock Period | O | - | 384 | - | ns |
| T_{High} | LED High Time | O | - | 192 | - | ns |
| T_{Low} | LED Low Time | O | - | 192 | - | ns |
| T_{OSU} | LED_DATA to LED_CLK Rising Setup Time | O | - | 189 | - | ns |
| T_{OH} | LED_DATA to LED_CLK Rising Hold Time | O | - | 195 | - | ns |

9.4.9. Power and Reset Characteristics

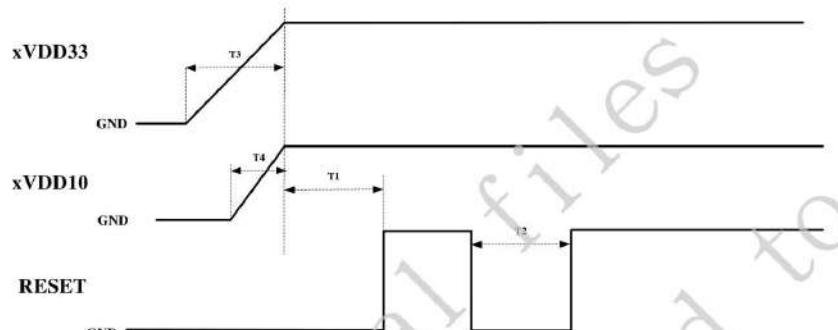
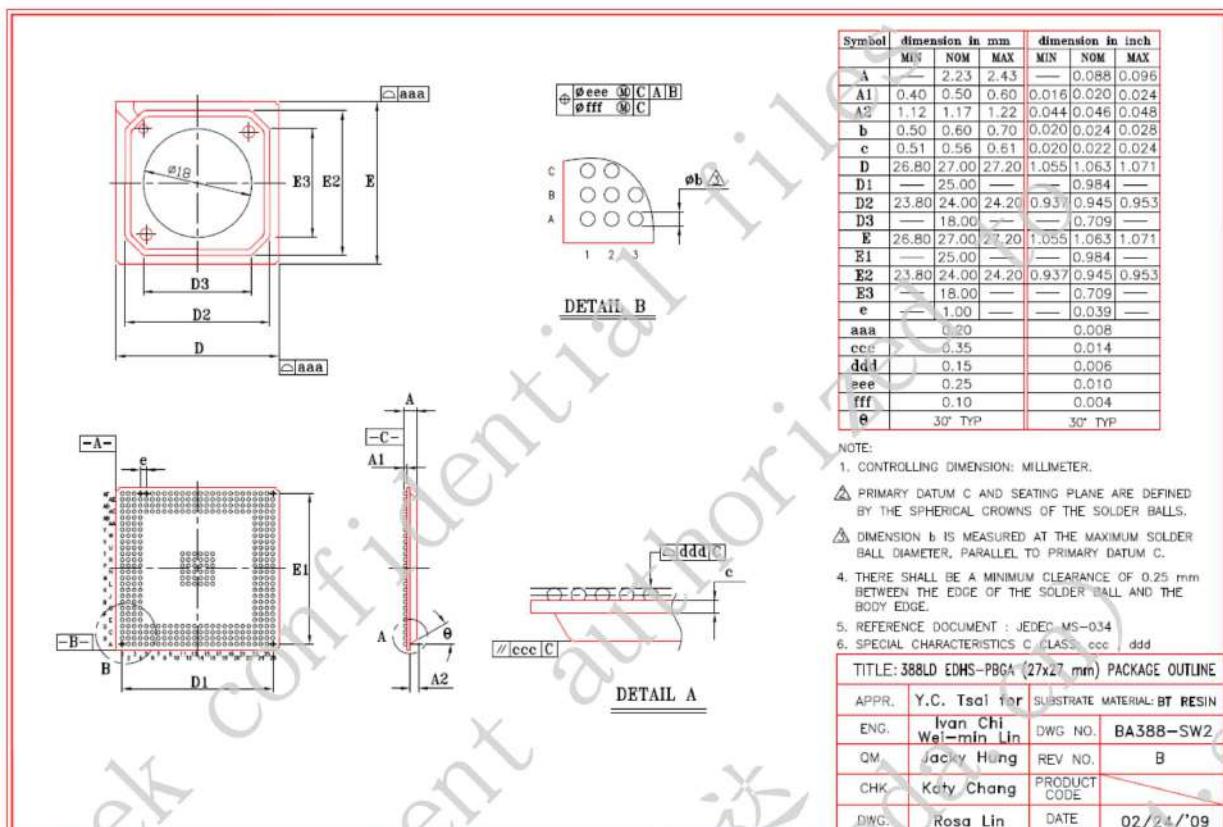


Figure 25. Power and Reset Timing Illustrations

Table 33. Power and Reset Timing Characteristics

| Symbol | Description | Min | Typ | Max | Units |
|--------|--|-----|-----|-----|-------|
| T1 | The duration from all of VDD33 and all of VDD10 power steady to reset signal release to high | 10 | - | - | ms |
| T2 | The duration of reset signal remain low timing | 10 | - | - | ms |
| T3 | All of VDD33 power rising time | 1 | - | - | ms |
| T4 | All of VDD10 power rising time | 1 | - | - | ms |

10. Package Information (EDHS-PBGA388 (27*27))



11. Ordering Information

Table 34. Ordering Information

| Part Number | Package | Status |
|----------------|--------------------------|--------|
| RTL8393M-VC-CG | EDHS-PBGA388 (27mm*27mm) | |
| | | |

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