

REALTEK

RTL8261N

INTEGRATED 100M/1G/2.5G/5G/10G ETHERNET TRANSCEIVER

Brief DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8261N IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

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0.2	2022/05/31	Modify HSIP PIN NO Modify AVDDH Voltage spec
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1. Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A			RSET			XTAL_N		XTAL_P		SYNCECLK		DNC		DNC		DNC		PTP_XTAL_N
B																		
C																		
D	NC																	
E			NC				AVDDH_LL		DNC		AVDDH_LL		AVDDL_LL		AVDDL_LL		DGND	
F	AGND_PHY																	
G			NC															
H	AGND_PHY																	
J			AGND_PHY															
K	AVDDHPHY																	
L			AGND_PHY															
M	MDIDP																	
N			AVDDHPHY															
P	MDIDN																	
R			AVDDLPHY															
T	AVDDLPHY																	
U			AVDDHPHY															
V	MDICN																	
W			AVDDLPHY															
Y	MDICP																	
AA			AVDDHPHY															
AB	AVDDLPHY																	
AC			AVDDLPHY															
AD	MDIBP																	
AE			AVDDLPHY															
AF	MDIBN																	
AG			AVDDHPHY															
AH	AVDDLPHY																	
AJ			AGND_PHY															
AK	MDIAN																	
AL			AGND_PHY															
AM	MDIAP																	
AN			AGND_PHY															
AP	AGND_PHY																	
AR																		
AT																		
AU			AGND_PHY			AGND_PHY		LED3		LED1		LED4		LED2		LED5		LED6

Figure 1. Pin Assignments (Top View)

Figure 2. Pin Assignments (Top View) (Continued)

1.1. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified ‘Upon Reset’ time.

I: Input Pin

AI: Analog Input Pin

O: Output Pin

AO: Analog Output Pin

I/O: Bi-Directional Input/Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

P: Digital Power Pin
 G: Digital Ground Pin
 I_{PU}: Input Pin With Pull-Up Resistor
 I_{XT}: Input Crystal Pin
 O_{OD}: Open Drain Output Pin
 O_{PU}: Output Pin With Pull-Up Resistor;
 I_{ST}: Schmitt trigger input

AP: Analog Power Pin
 AG: Analog Ground Pin
 SP: SerDes Power Pin
 SG: SerDes Ground Pin
 O_{PD}: Output Pin With Pull-Down Resistor
 ISOR: Input sampled on reset

Table 1. Pin Assignments Table

Name	Pin No.	Type
RSET	A4	AO
XTAL_N	A6	I _{XT}
XTAL_P	A8	I _{XT}
SYNCECLK	A10	AO
DNC	A12	AO
DNC	A14	AO
DNC	A16	AO
PTP_XTAL_N	A18	I _{XT}
PTP_XTAL_P	A20	I _{XT}
DVDDL	A22	P
DNC	A24	I _{PU} , SOR
INT	A26	O _{OD}
PTP_IN0	A28	I _{PD}
CLK_SEL	A30	I _{PU} , SOR
CHIP_MODE	A32	I _{PU} , SOR
DVDDL	A34	P
NC	D1	-
NC	D37	-
NC	E4	-
AVDDH_PLL	E7	AP
DNC	E9	I _{PU} , SOR
AVDDH_PLL	E11	AP
AVDDL_PLL	E13	AP
AVDDL_PLL	E15	AP
DGND	E17	G
DVDDL	E19	P
DVDDL	E21	P
DVDDIO	E23	P
DVDDIO	E25	P

Name	Pin No.	Type
DGND	E27	G
DGND	E29	G
DVDDL	E31	P
DGND	E34	G
AGND_PHY	F1	AG
SGND	F37	SG
NC	G4	-
DVDDL	G34	P
AGND_PHY	H1	AG
SGND	H37	SG
AGND_PHY	J4	AG
SGND	J34	SG
AVDDH_PHY	K1	AP
HSON	K37	AO
AGND_PHY	L4	AG
SVDDL_CK	L34	SP
MDIDP	M1	AI/O
HSOP	M37	AO
AVDDH_PHY	N4	AP
MDIDN	P1	AI/O
SGND	P37	SG
AVDDL_PHY	R4	AP
SGND	R34	SG
AVDDL_PHY	T1	AP
HSIN	T37	AI
AVDDH_PHY	U4	AP
SVDDL_TR	U34	SP
MDICN	V1	AI/O
HSIP	V37	AI

Name	Pin No.	Type
AVDDL_PHY	W4	AP
DGND	W34	G
MDICP	Y1	AI/O
SGND	Y37	SG
AVDDH_PHY	AA4	AP
DVDDL	AA34	P
AVDDL_PHY	AB1	AP
PHYAD0	AB37	I _{PU, SOR}
AVDDL_PHY	AC4	AP
DVDDIO	AC34	P
MDIBP	AD1	AI/O
PHYAD1	AD37	I _{PU, SOR}
AVDDL_PHY	AE4	AP
PHYAD3	AE34	I _{PU, SOR}
MDIBN	AF1	AI/O
PHYAD2	AF37	I _{PU, SOR}
AVDDH_PHY	AG4	AP
DNC	AG34	I _{PU, SOR}
AVDDL_PHY	AH1	AP
PHYAD4	AH37	I _{PU, SOR}
AGND_PHY	AJ4	AG
LED_AUTOP_DIS	AJ34	I _{PU, SOR}
MDIAN	AK1	AI/O
POB_DIS	AK37	I _{PU, SOR}
AGND_PHY	AL4	AG
MDI_ORDER	AL34	I _{PD, SOR}
MDIAP	AM1	AI/O
PHY_DIS	AM37	I _{PD, SOR}
AGND_PHY	AN4	AG
AGND_PHY	AN7	AG
AGND_PHY	AN9	AG
DVDDIO	AN11	P

Name	Pin No.	Type
DVDDIO	AN13	P
DVDDIOLED	AN15	P
DGND	AN17	G
DVDDL	AN19	P
DVDDL	AN21	P
DVDDIO	AN23	P
DVDDL	AN25	P
DGND	AN27	G
DVDDIO	AN29	P
DGND	AN31	G
DVDDL	AN34	P
AGND_PHY	AP1	AG
DVDDL	AP37	P
AGND_PHY	AU4	AG
AGND_PHY	AU6	AG
LED3	AU8	O _{PD}
LED1	AU10	O _{PD}
LED4	AU12	O _{PD}
LED2	AU14	O _{PD}
LED5	AU16	O _{PD}
LED6	AU18	O _{PD}
SYNCELOCK	AU20	O _{PD}
DNC	AU22	I _{PU, SOR}
PTP_IN1_OUT	AU24	I/O _{PD}
NRESET	AU26	I _{PU, ST}
DVDDL	AU28	P
MDIO	AU30	I/O _{PU}
MDC	AU32	I _{PD}
DNC	AU34	I _{PU, SOR}
EPAD-AGND_PHY	V13	AG
EPAD-DGND_PHY	V25	G

2. Pin Descriptions

2.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
MDIAP	AM1	AI/O	-	Media Dependent Interface A~D. For 10GBase-T, 5GBase-T, 2.5GBase-T, 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100Ω termination resistor.
MDIAN	AK1	AI/O	-	
MDIBP	AD1	AI/O	-	
MDIBN	AF1	AI/O	-	
MDICP	Y1	AI/O	-	
MDICN	V1	AI/O	-	
MDIDP	M1	AI/O	-	
MDIDN	P1	AI/O	-	

2.2. XSGMII Interface Pins

Table 3. XSGMII Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
HSIP	V37	AI	-	USXGMII/XFI/5000base-X/2500BASE-X/SGMII Receive Serial Data. Serdess differential input data. Externally AC coupled.
HSIN	T37	AI	-	
HSOP	M37	AO	-	USXGMII/XFI/5000base-X/2500BASE-X/SGMII Transmit Serial Data. Serdess differential output data. Externally AC coupled.
HSON	K37	AO	-	

2.3. LED Pins

Table 4. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED1	AU10	OPD	4/8	Status LED1. Active-Low or auto polarity (see LED_AUTOP pin) by pin's strapping value. Its indication can be defined via register. It's 3.3V voltage tolerance. The default indication is: On=master, OFF=Slave.
LED2	AU14	OPD	4/8	Status LED2. Active-Low or auto polarity by pin's strapping value. Its indication can be defined via register. It's 3.3V voltage tolerance. The default indication is: Blink=Tranning, 2.5G/5GE ON=Linup, 2.5G/5GE OFF=Linkdown.
LED3	AU8	OPD	4/8	Status LED3. Active-Low or auto polarity by pin's strapping value. Its indication can be defined via register. It's 3.3V voltage tolerance. The default indication is: Copper Act, BLINK =Traffic, OFF=No Traffic.
LED4	AU12	OPD	4/8	Status LED4. Active-Low or auto polarity by pin's strapping value. Its indication can be defined via register. It's 3.3V voltage tolerance. The default indication is: Copper Link UP= ON. Copper Link Down= OFF.

Pin Name	Pin No.	Type	Drive (mA)	Description
LED5	AU16	OPD	4/8	Status LED5. Active-Low or auto polarity by pin's strapping value. Its indication can be defined via register. It's 3.3V voltage tolerance. The default indication is: 2.5G/5GE/10G ON=Linkup,2.5G/5GE/10G OFF=Linkdown.
LED6	AU18	OPD	4/8	Reserved. Default Disable. Enable by register configuration.

2.4. Configuration Strapping Pins

Table 5. Configuration Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
CLK_SEL	A30	I _{PU} , SOR	-	Reference Clock Source Select. 0b1: the XTAL_P/N inputs are configured to accept differential 50 MHz input reference clock. (default) 0b0: the XTAL_P/N applies 50 MHz single-end to generate reference clock.
POB_DIS	AK37	I _{PU} , SOR	-	Enable/Disable LED power on Blinking. 0b1: the function is disabled. (default) 0b0: all LED blink once simultaneously according predefined timing before they indication the PHY status.
CHIP_MODE	A32	I _{PU} , SOR	-	Chip mode select. 0b1: chip is on the media converter mode. (default) 0b0: chip is on the USXGMII mode.
LED_AUTOP_DIS	AJ34	I _{PU} , SOR	-	LED auto polarity strap. 0b1: LED auto polarity is disabled and all LEDs are active low. (default) 0b0: each LED pin's polarity determined by the pin's strapping value during reset. The LED pin's polarity is opposite to the strapping value. For example, LED1's strap value is 0 (1), then LED1 is active high (low). This function is used to avoid LED lighting unexpectedly during power on.
MDI_ORDER	AL34	I _{PD} , SOR	-	MDI order strap. Pair ordering of the port, 0b1: pair order swap to DCBA 0b0: no swap, pair order is ABCD as the MDI pin name(default)
PHY_DIS	AM37	I _{PD} , SOR	-	PHY disable strap. 0b1: PHY function is disabled after reset and should be enabled via register 0b0: PHY function is enabled by default. (default)
PHYAD0	AB37	I _{PU} , SOR	-	PHYAD[4:0]. Port Address or PHY Address. Using these pins the user set the Port Address values. (default 5b11111)
PHYAD1	AD37	I _{PU} , SOR	-	
PHYAD2	AF37	I _{PU} , SOR	-	
PHYAD3	AE34	I _{PU} , SOR	-	
PHYAD4	AH37	I _{PU} , SOR	-	

2.5. Management Interface Pins

Table 6. Management Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
MDC	AU32	I _{PD}	4/8	Management Data Clock for Port. The MDC clock input must be provided to allow MII management functions.
MDIO	AU30	I/O _{PU}	4/8	Management Data I/O for Port. This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
NRESET	AU26	I _{PU, ST}	-	Reset. Active low, NRESET is Schmitt Trigger Input. The NRESET signal resets the PHY chip. The PHY requires a hardware reset prior to normal operation. Configuration settings obtained via Hardware Strap Option pins are latched on the rising edge of NRESET. Latched on the rising edge of NRESET.
RSET	A4	AO	-	Bias Resistors. Adjusts the reference current of the chip. A 2.49 k ±1% resistor is connected between this pin and AGND.

2.6. Miscellaneous Pins

Table 7. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
XTAL_P	A8	I _{XT}	-	50MHz±50ppm tolerance crystal reference or external clock input. A continuous differential 50MHz reference clock must be supplied to these pins. When CLK_SEL pin is low, apply a 50 MHz crystal oscillator. XTAL_P is XI pin and XTAL_N is XO pin for the crystal oscillator circuit. External single end clock should be fed on the XTAL_P pin.
XTAL_N	A6	I _{XT}	-	
SYNCECLK	A10	AO	-	Synchronous Ethernet Recovered Clock. This pin provides a 25 MHz recovered clock signal which is synchronous to the incoming Ethernet signal of the device. It's 1.9v only. These pins reference to the AVDDH_PLL voltage Level.
SYNCELOCK	AU20	O _{PD}	4/8	Synchronous Ethernet Lock. These pins reference to the DVDDIO voltage Level.
PTP_XTAL_N	A18	I _{XT}	-	PTP Clock Input
PTP_XTAL_P	A20	I _{XT}	-	
PTP_IN0	A28	I _{PD}	-	PTP Input 0. This is the PTP0 input signal used in IEEE 1588.
PTP_IN1_OUT	AU24	I/O _{PD}	4/8	Bidirectional I/O signal: {PTP Input 1 or PTP Output} This pin can be provisioned (via register writes) as the PTP_IN1 signal, or as the PTP_Out output signal used in IEEE 1588. After reset, this pin is set as input (PTP_IN1).
INT	A26	O _{OD}	4/8	Dedicated Interrupt Pin. Indicates an interrupt on the port. It can be configured as Tristateable Output or open drain output. The active polarity can be configured. It's active low and open drain by default.

Pin Name	Pin No.	Type	Drive (mA)	Description
DNC	A12, A14, A16, A24, E9, AG34, AU22, AU34	-	-	Internal used. These pins must be floated.
NC	D1, D37, E4, G4	-	-	No Connection.

2.7. Power and GND Pins

Table 8. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDL	A22, A34, E19, E21, E31, G34, AA34, AN19, AN21, AN25, AN34, AP37, AU28	P	Digital Low Voltage Power. Connect to 1.0V +/- 3% power source. Ripple & noise must under 30mV pk-pk, can't exceed the operating Voltage tolerance.
DVDDIOLE_D	AN15	P	Digital IO power for all LED pins. Operating Voltage SPEC & power noise level as below. 3.3v(+/- 5) or 2.5v(+/- 5%) : Keep power noise below 100mV(pk-pk), can't exceed the operating voltage tolerance. 1.9v(+/- 3%) or 1.8v(+/- 5%) : Keep power noise below 50mV(pk-pk), can't exceed the operating voltage tolerance.
DVDDIO	E23, E25, AC34, AN11, AN13, AN23	P	Digital IO power for the digital IO signal pins except the MDC/MDIO pins and LED pins. Connect it to 1.9v(+/- 3%) power source, and keep power noise below 50mV(pk-pk), can't exceed the operating voltage tolerance.
DVDDIOM	AN29	P	Digital IO power for MDC/MDIO pin. Operating Voltage SPEC & power noise level as below. 3.3v(+/- 5%)or 2.5v(+/- 5%) : Keep power noise below 100mV(pk-pk), can't exceed the operating voltage tolerance. 1.9v(+/- 3%) or 1.8v(+/- 5%) or 1.2v(+/- 5%): keep power noise below 50mV(pk-pk), can't exceed the operating voltage tolerance
AVDDH_PH_Y	K1, N4, U4, AA4, AG4	AP	Analog High Voltage Power for transceiver . Connect to 1.9V+/- 3% power source. Ripple & noise must under 20mV pk-pk, can't exceed the operating Voltage tolerance.

Pin Name	Pin No.	Type	Description
AVDDL_PH_Y	R4, T1, W4, AB1, AC4, AE4, AH1	AP	Analog Low Voltage Power 2 for transceiver . Connect to 1.0V +/- 3% power source Ripple & noise must under 20mV pk-pk, can't exceed the operating Voltage tolerance.
AVDDH_PLL	E7, E11,	AP	Analog High Voltage Power for PLL. Connect to 1.9V +/- 3% power. Ripple & noise must under 20mV pk-pk, can't exceed the operating Voltage tolerance.
AVDDL_PLL	E13, E15,	AP	Analog Low Voltage Power for PLL . Connect to 1.0V +/- 3% power source Ripple & noise must under 20mV pk-pk, can't exceed the operating Voltage tolerance.
SVDDL_TR	U34	SP	SerDes Low Voltage Power for transceiver. Connect to 1.0V +/- 3% power source.
SVDDL_CK	L34	SP	SerDes Low Voltage Power for clock. Connect to 1.0V +/- 3% power source. Ripple & noise must under 20mV(pk-pk) (Bandwidth: 0~400MHz), can't exceed the operating Voltage tolerance.
DGND	E17, E27, E29, E34, W34, V25, AN17, AN27, AN31	G	Digital Ground.
AGND_PHY	F1, H1, J4, L4, V13, AJ4, AL4, AN4, AN7, AN9, AP1, AU4, AU6	AG	Analog Ground for transceiver.
SGND	F37, H37, J34, P37, R34, Y37	SG	SerDes Ground.

3. General Function Description

3.1. Chip Mode

The RTL8261N supports MAC Interface: USXGMII/10GBase-R/5GBase-R/5000Base-X/2500Base-X/1000Base-X/SGMII ; UTP speed : 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX.

3.1.1.USXGMII mode

When the UTP operate at 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX.

The SDS mode is USXGMII.

3.1.2.Media Converter mode

Media converter mode is used for convert copper interface to fiber interface. The support UTP speed: 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX; the SDS mode support speed:10GBase-R/5GBase-R/5000Base-X/2500Base-X/1000Base-X and SGMII.

In media converter mode the speed of the SDS mode is determined by the UTP port speed the phy

The Chip mode /UTP speed/SDS speed relations list is given below.

Table 9. SDS speed v.s UTP speed

Chip mode	UTP Speed	SDS Speed
10G-SXGMII	10G	10G-SXGMII
	5G	10G-SXGMII
	2.5G	10G-SXGMII
	1G	10G-SXGMII SGMII
	100M	10G-SXGMII SGMII
Media Convert	10G	10GBase-R
	5G	5GBase-R 5000Base-X
	2.5G	2500Base-X
	1G	SGMII 1000Base-X (default)
	100M	SGMII

3.2. Parallel LED

The RTL8261N only support parallel mode LED, per port can support 6 LEDs.

The LED pin also supports pin strapping configuration functions.

3.2.1. Power On Blinking

RTL8261N provides power on LED blinking function. Power on blinking time setting depend on PWR_ON_BLINK_SEL[1:0]. The duration of STP1_PWR_ON_LED[5:0] is set by register PWR_ON_BLINK_SEL[1:0]; if the power on blinking time is 400ms means 400ms on and 400ms off. The duration of STP2_PWR_ON_LED[5:0] also follow the selection of PWR_ON_BLINK_SEL[1:0].

Two power on blinking status can be configured individually by STP1_PWR_ON_LED[5:0] and STP2_PWR_ON_LED[5:0].

Table 10. Power On Blinking LED Configuration

Bits	Name	Description	Mode	Default
n.[15]	POB_EN	enable parallel LED power on blinking(from strap pin) 1'b1: enable parallel LED power on blinking 1'b0: disable parallel LED power on blinking strap pin POB_DIS Low: enable parallel LED power on blinking High: disable parallel LED power on blinking	RO	1'b0
n.[14:13]	PWR_ON_BLINK_SEL[1:0]	Select power on blinking time (T). 2'b00: disable 2'b01: 400ms 2'b10: 800ms 2'b11: 1600ms	R/W	2'b01
n.[12]	reserve	reserve	reserve	reserve
n.[11:6]	STP2_PWR_ON_LED[5:0]	Select power on blinking LED[5:0] in step 2 power on duration. “1” = LED on, “0” = LED off.	R/W	6'b101010
n[5:0]	STP1_PWR_ON_LED[5:0]	Select power on blinking LED[5:0] in step 1 power on duration. “1” = LED on, “0” = LED off.	R/W	6'b010101

3.2.2. Parallel LED Mode

Each of parallel LED I/O enable or disable can be set by register . The each of LED polarity can be set individually by register .

Table 11.Per port Parallel LED I/O Configuration Register Table

Bits	Name	Description	Mode	Default
n.[15:14]	Reserve	Reserve	Reserve	Reserve
n.13	P0_LED5_ACTIVE_L	Select P0_LED[5] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1

Bits	Name	Description	Mode	Default
n.12	P0_LED4_ACTIVE_L	Select P0_LED[4] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1
n.11	P0_LED3_ACTIVE_L	Select P0_LED[3] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1
n.10	P0_LED2_ACTIVE_L	Select P0_LED[2] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1
n.9	P0_LED1_ACTIVE_L	Select P0_LED[1] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1
n.8	P0_LED0_ACTIVE_L	Select P0_LED[0] is high active or low active. Strapping pin, combined with LED_AUTOP_DIS = 0. 0: High active 1: Low active	R/W	1'b1
n.[7:6]	Reserve	Reserve	Reserve	Reserve
n.5	P0_LED5_PARA_EN	Select LED P0_LED[5] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1
n.4	P0_LED4_PARA_EN	Select LED P0_LED[4] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1
n.3	P0_LED3_PARA_EN	Select LED P0_LED[3] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1
n.2	P0_LED2_PARA_EN	Select LED P0_LED[2] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1
n.1	P0_LED1_PARA_EN	Select LED P0_LED[1] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1
n.0	P0_LED0_PARA_EN	Select LED P0_LED[0] is output enable or disable: 0: Disable 1: Enable	R/W	1'b1

3.3. Realtek Cable Test (RTCT)

The RTL8261N physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function could be used to detect short, open, crossed, or impedance mismatch in each differential pair.

3.4. SyncE

The RTL8261N syncE recovery clock can supports 25MHz/50MHz clock.

3.5. Power Down Mode

The RTL8261N implements power down mode on a per-port basis. Setting MMD1.0.11 forces the corresponding port of the RTL8261N to enter power down mode.

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4. Register Descriptions

4.1. Register Access Types

Table 12. Register Access Types

Type	Description
LH	Latch high. If the status is high, this field is set to ‘1’ and remains set.
RC	Read-cleared. The register field is cleared after read.
RO	Read only.
WO	Write only.
RW	Read and Write
SC	Self-cleared. Writing a ‘1’ to this register field causes the function to be activated immediately, and then the field will be automatically cleared to ‘0’.

4.2. MMD Register Mapping and Definition

Table 13. MMD Register Mapping and Definition

Device	MMD Name	Description
1	PMA/PMD	PMA/PMD Control Register.
3	PCS	PCS Control Register.
7	Auto-Negotiation	Auto-Negotiation Register.
30	Vendor specific 1	SERDES Control Register
31	Vendor specific 2	PHY Control Register
Otherwise	Reserved	Reserved

4.3. PMA/PMD MMD Mapping and Definition

Table 14. PMA/PMD MMD Register Mapping and Definitions

Register Address	Register Name	Subclause
1.0x0000	PMA/PMD control 1	45.2.1.1
1.0x0001	PMA/PMD status 1	45.2.1.2
1.0x0002	PMA/PMD device identifier 1	45.2.1.3
1.0x0003	PMA/PMD device identifier 2	45.2.1.3
1.0x0004	PMA/PMD speed ability	45.2.1.4
1.0x000B	PMA/PMD extended ability	45.2.1.10
1.0x0015	2.5G PMA/PMD extended ability	45.2.1.14
1.0x0081	Multi-GBASE-T status	45.2.1.62
1.0x0082	Multi-GBASE-T pair swap and polarity	45.2.1.63
1.0x0083	Multi-GBASE-T TX power backoff and PHY short reach setting	45.2.1.64
1.0x0084	Multi-GBASE-T test mode	45.2.1.65
1.0x0091	Multi-GBASE-T skew delay 1	45.2.1.78
1.0x0092	Multi-GBASE-T skew delay 2	45.2.1.78
1.0x0093	Multi-GBASE-T fast retrain status and control	45.2.1.79
Otherwise	Reserved	Reserved

4.3.1. PMA/PMD Control 1 Register MMD 1.0x0000)

Table 15. PMA/PMD Control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0000 0.15	Reset	RW, SC	0	Reset. 1: PMA/PMD reset 0: Normal operation This action may change the internal PHY state and the state of the physical link associated with the PHY.

Bit	Name	Type	Default	Description															
1.0x000 0.14	Reserved	RO	0	Value always 0															
1.0x000 0.13	Speed selection (LSB)	RW	1	<p>Speed Select Bit 0</p> <p>In forced mode, i.e., when Auto-Negotiation is disabled, bits 0.6 and 0.13 could be used to determine device speed selection. See mmd 31.0.0 for detailed description.</p> <table border="1"> <thead> <tr> <th>1.0.6</th> <th>1.0.13</th> <th>Speed Enabled</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Bits 5:2 select speed</td> </tr> <tr> <td>1</td> <td>0</td> <td>1000Mbps</td> </tr> <tr> <td>0</td> <td>1</td> <td>100Mbps</td> </tr> <tr> <td>0</td> <td>0</td> <td>10Mbps</td> </tr> </tbody> </table>	1.0.6	1.0.13	Speed Enabled	1	1	Bits 5:2 select speed	1	0	1000Mbps	0	1	100Mbps	0	0	10Mbps
1.0.6	1.0.13	Speed Enabled																	
1	1	Bits 5:2 select speed																	
1	0	1000Mbps																	
0	1	100Mbps																	
0	0	10Mbps																	
1.0x000 0.12	Reserved	RO	0	Value always 0															
1.0x000 0.11	Low power	RW	0	<p>Power Down.</p> <p>1: Power down (only Management Interface and logic are active; link is down)</p> <p>0: Normal operation</p>															
1.0x000 0.10:7	Reserved	RO	4'b0	Value always 0															
1.0x000 0.6	Speed selection (MSB)	RW, SC	1	<p>Speed Select Bit 1</p> <p>In forced mode, i.e., when Auto-Negotiation is disabled, the bits 0.6 and 0.13 can be used to determine device speed selection. See mmd 31.0.0 for a detailed description.</p> <table border="1"> <thead> <tr> <th>1.0.6</th> <th>1.0.13</th> <th>Speed Enabled</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Bits 5:2 select speed</td> </tr> <tr> <td>1</td> <td>0</td> <td>1000Mbps</td> </tr> <tr> <td>0</td> <td>1</td> <td>100Mbps</td> </tr> <tr> <td>0</td> <td>0</td> <td>10Mbps</td> </tr> </tbody> </table>	1.0.6	1.0.13	Speed Enabled	1	1	Bits 5:2 select speed	1	0	1000Mbps	0	1	100Mbps	0	0	10Mbps
1.0.6	1.0.13	Speed Enabled																	
1	1	Bits 5:2 select speed																	
1	0	1000Mbps																	
0	1	100Mbps																	
0	0	10Mbps																	
1.0x000 0.5:2	Speed selection	RW	4'b0	<p>5 4 3 2</p> <p>0 1 1 1: 5Gb/s</p> <p>0 1 1 0: 2.5Gb/s</p> <p>0 0 0 0: 10Gb/s</p> <p>Otherwise: Reserved</p>															
1.0x000 0.1	PMA remote loopback	RW	0	<p>1: Enable PMA remote loopback mode</p> <p>0: Disable PMA remote loopback mode</p>															
1.0x000 0.0	PMA local loopback	RW	0	<p>1: Enable PMA local loopback mode</p> <p>0: Disable PMA local loopback mode</p>															

Note 1: To make bits speed selection bits effective, 1.0x000.13 & 1.0x000.6 or 1.0x000.5:2 must have consistent setting, i.e., only one speed could be set among these bits.

4.3.2. PMA/PMD Status 1 Register (MMD 1.0x0001)

Table 16. PMA/PMD Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0001.15:8	Reserved	RO	8'b 0	Value always 0
1.0x0001.7	PMA Fault	RO	0	1: Fault condition detected 0: Fault condition not detected
1.0x0001.6:3	Reserved	RO	4'b 0	Value always 0
1.0x0001.2	Receive link status	RO, LL	0	1: PMA/PMD receive link up 0: PMA/PMD receive link down
1.0x0001.1	Low-power ability	RO	0	1: PMA/PMD supports low-power mode 0: PMA/PMD does not support low-power mode
1.0x0001.0	Reserved	RO	0	Value always 0

4.3.3. PMA/PMD Device Identifier 1 Register (MMD 1.0x0002)

Table 17. PMA/PMD Device Identifier 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0002.15:0	Realtek OUI [21:6]	RO	0x1C	Realtek OUI, bit 21 to bit 6

4.3.4. PMA/PMD Device Identifier 2 Register (MMD 1.0x0003)

Table 18. PMA/PMD Device Identifier 2 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0003.15:10	Realtek OUI [5:0]	RO	0x32	Realtek OUI, bit 5 to bit 0
1.0x0003.9:4	Model number	RO	0x2f	Value always 0x2f for RTL8261N
1.0x0001.3:0	Revision number	RO	0x3	Revision number

4.3.5. PMA/PMD Speed Ability Register (MMD 1.0x0004)

Table 19. PMA/PMD Speed Ability Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0004.15	Reserved	RO	0	Value always 0
1.0x0004.14	5G capable	RO	0	1: PMA/PMD is capable of operating at 5 Gb/s 0: PMA/PMD is not capable of operating at 5 Gb/s
1.0x0004.13	2.5G capable	RO	1	1: PMA/PMD is capable of operating at 2.5 Gb/s 0: PMA/PMD is not capable of operating at 2.5 Gb/s
1.0x0004.12:10	Reserved	RO	3'b 0	Value always 0
1.0x0004.9	Reserved	RO	0	Reserved
1.0x0004.8	Reserved	RO	0	Reserved
1.0x0004.7	Reserved	RO	0	Reserved
1.0x0004.6	10M capable	RO	1	1: PMA/PMD is capable of operating at 10 Mb/s 0: PMA/PMD is not capable of operating at 10 Mb/s

Bit	Name	Type	Default	Description
1.0x0004.5	100M capable	RO	1	1: PMA/PMD is capable of operating at 100 Mb/s 0: PMA/PMD is not capable of operating at 100 Mb/s
1.0x0004.4	1000M capable	RO	1	1: PMA/PMD is capable of operating at 1000 Mb/s 0: PMA/PMD is not capable of operating at 1000 Mb/s
1.0x0004.3	Reserved	RO	0	Value always 0
1.0x0004.2	10PASS-TS capable	RO	0	1: PMA/PMD is capable of operating at 10PASS-TS 0: PMA/PMD is not capable of operating at 10PASS-TS
1.0x0004.1	2BASE-TL capable	RO	0	1: PMA/PMD is capable of operating at 2BASE-TL 0: PMA/PMD is not capable of operating at 2BASE-TL
1.0x0004.0	10G capable	RO	1	1: PMA/PMD is capable of operating at 10 Gb/s 0: PMA/PMD is not capable of operating at 10 Gb/s

4.3.6. PMA/PMD Extended Ability Register (MMD 1.0x000B)

Table 20. PMA/PMD Extended Ability Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x000B.15	Reserved	RO	0	Value always 0
1.0x000B.14	2.5G extended abilities	RO	1	1: PMA/PMD has 2.5G extended abilities listed in register 1.21 0: PMA/PMD does not have 2.5G extended abilities
1.0x000B.13:11	Reserved	RO	3'b 0	Value always 0
1.0x000B.10	Reserved	RO	0	Reserved
1.0x000B.9	P2MP ability	RO	0	1: PMA/PMD has P2MP abilities listed in register 1.12 0: PMA/PMD does not have P2MP abilities
1.0x000B.8	10BASE-Te ability	RO	1	1: PMA/PMD is able to perform 10BASE-Te 0: PMA/PMD is not able to perform 10BASE-Te
1.0x000B.7	100BASE-TX ability	RO	1	1: PMA/PMD is able to perform 100BASE-TX 0: PMA/PMD is not able to perform 100BASE-TX
1.0x000B.6	Reserved	RO	0	Reserved
1.0x000B.5	1000BASE-T ability	RO	1	1: PMA/PMD is able to perform 1000BASE-T 0: PMA/PMD is not able to perform 1000BASE-T
1.0x000B.4:3	Reserved	RO	0	Reserved
1.0x000B.2	10GBASE-T ability	RO	0	1: PMA/PMD is able to perform 10GBASE-T 0: PMA/PMD is not able to perform 10GBASE-T
1.0x000B.1:0	Reserved	RO	0	Reserved

4.3.7. 2.5G PMA/PMD Extended Ability Register (MMD 1.0x0015)

Table 21. 2.5G/5G PMA/PMD Extended Ability Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0015.15:2	Reserved	RO	14'b 0	Value always 0
1.0x0015.1	5GBASE-T ability	RO	1	1: PMA/PMD is able to perform 5GBASE-T 0: PMA/PMD is not able to perform 5GBASE-T
1.0x0015.0	2.5GBASE-T ability	RO	1	1: PMA/PMD is able to perform 2.5GBASE-T 0: PMA/PMD is not able to perform 2.5GBASE-T

4.3.8. Multi-GBASE-T Status Register (MMD 1.0x0081)

Table 22. Multi-GBASE-T Status Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0081.15:1	Reserved	RO	15'b 0	Value always 0
1.0x0081.0	LP information valid	RO	0	1: Link partner information is valid in 10G/ 5G/ 2.5GBASE-T 0: Link partner information is invalid in 10G/ 5G/ 2.5GBASE-T

4.3.9. Multi-GBASE-T Pair Swap and Polarity Register (MMD 1.0x0082)

Table 23. Multi-GBASE-T Pair Swap and Polarity Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0082.15:12	Reserved	RO	4'b 0	Value always 0
1.0x0082.11	Pair D polarity	RO	0	1: Polarity of pair D is reversed 0: Polarity of pair D is not reversed
1.0x0082.10	Pair C polarity	RO	0	1: Polarity of pair C is reversed 0: Polarity of pair C is not reversed
1.0x0082.9	Pair B polarity	RO	0	1: Polarity of pair B is reversed 0: Polarity of pair B is not reversed
1.0x0082.8	Pair A polarity	RO	0	1: Polarity of pair A is reversed 0: Polarity of pair A is not reversed
1.0x0082.7:2	Reserved	RO	6'b 0	Value always 0
1.0x0082.1:0	MDI/MDI-X connection	RO	2'b 0	bit1 bit0 1 1: No crossover 1 0: Reserved 0 1: Reserved 0 0: Pair A/B and pair C/D crossover

4.3.10. Multi-GBASE-T TX Power Backoff and PHY Short Reach Setting Register (MMD 1.0x0083)

Table 24. Multi-GBASE-T TX Power Backoff and PHY Short Reach Setting Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0083.15:13	Link partner TX power backoff setting	RO	3'b 0	15 14 13 1 1 1: 14 dB 1 1 0: 12 dB 1 0 1: 10 dB 1 0 0: 8 dB 0 1 1: 6 dB 0 1 0: 4 dB 0 0 1: 2 dB 0 0 0: 0 dB
1.0x0083.12:10	TX power backoff setting	RO	3'b 0	12 11 10 1 1 1: 14 dB 1 1 0: 12 dB 1 0 1: 10 dB 1 0 0: 8 dB 0 1 1: 6 dB 0 1 0: 4 dB 0 0 1: 2 dB 0 0 0: 0 dB
1.0x0083.9:1	Reserved	RO	9'b 0	Value always 0
1.0x0083.0	Short reach mode	RW	4'b 0	1: PHY is operating in short reach mode 0: PHY is not operating in short reach mode

4.3.11. Multi-GBASE-T Test Mode Register (MMD 1.0x0084)

Table 25. Multi-GBASE-T Test Mode Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0084.15:13	Test mode control	RW	3'b0	15 14 13 1 1 1: Test mode 7 1 1 0: Test mode 6 1 0 1: Test mode 5 1 0 0: Test mode 4 0 1 1: Test mode 3 0 1 0: Test mode 2 0 0 1: Test mode 1 0 0 0: Normal operation

Bit	Name	Type	Default	Description
1.0x0084.12:10	Transmitter test frequencies	RW	3'b001	12 11 10 1 1 1: Reserved 1 1 0: Dual tone 5 1 0 1: Dual tone 4 1 0 0: Dual tone 3 0 1 1: Reserved 0 1 0: Dual tone 2 0 0 1: Dual tone 1 0 0 0: Reserved
1.0x0084.9:0	Reserved	RO	10'b 0	Value always 0

4.3.12. Multi-GBASE-T Skew Delay 1 Register (MMD 1.0x0091)

Table 26. Multi-GBASE-T Skew Delay 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0091.15	Reserved	RO	0	Value always 0
1.0x0091.14:8	Skew delay B	RO	7'b 0	Skew delay for pair B
1.0x0091.7:0	Reserved	RO	8'b 0	Value always 0

4.3.13. Multi-GBASE-T Skew Delay 2 Register (MMD 1.0x0092)

Table 27. Multi-GBASE-T Skew Delay 2 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0092.15	Reserved	RO	0	Value always 0
1.0x0092.14:8	Skew delay D	RO	7'b0	Skew delay for pair D
1.0x0092.7	Reserved	RO	0	Value always 0
1.0x0092.6:0	Skew delay C	RO	7'b0	Skew delay for pair C

4.3.14. Multi-GBASE-T Fast Retrain Status and Control Register (MMD 1.0x0093)

Table 28. Multi-GBASE-T Fast Retrain Status and Control Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0093.15:11	LP fast retrain count	RO, LH, RC	5'b0	Counts the number of fast retrains requested by the link partner
1.0x0093.10:6	LD fast retrain count	RO, LH, RC	5'b0	Counts the number of fast retrains requested by the local device
1.0x0093.5	Reserved	RO	0	Value always 0
1.0x0093.4	Fast retrain ability	RO	0	1: Fast retrain capability is supported 0: Fast retrain capability is not supported
1.0x0093.3	Fast retrain negotiated	RO	0	1: Fast retrain capability was negotiated 0: Fast retrain capability was not negotiated

Bit	Name	Type	Default	Description
1.0x0093.2:1	Fast retrain signal type	RW	2'b 01	11: Reserved 10: PHY signals Link Interruption during fast retrain 01: PHY signals Local Fault during fast retrain 00: PHY signals IDLE during fast retrain
1.0x0093.0	Fast retrain enable	RW	1	1: Fast retrain capability is enabled 0: Fast retrain capability is disabled

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4.4. PCS Registers

Table 29. PCS Registers Mapping and Definitions

Register Address	Register Name	Subclause
3.0x0000	PCS control 1	45.2.3.1
3.0x0001	PCS status 1	45.2.3.2
3.0x0004	PCS speed ability	45.2.3.4
3.0x0014	EEE control and capability	45.2.3.9
3.0x0015	EEE control and capability 2	45.2.3.9
3.0x0016	EEE wake error counter	45.2.3.10
Otherwise	Reserved	Reserved

4.4.1. PCS Control 1 Register (MMD 3.0x0000)

Table 30. PCS control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0000.15	Reset	RW	0	1: PCS reset 0: Normal operation
3.0x0000.14	Loopback	RW	0	1: Enable loopback mode 0: Disable loopback mode
3.0x0000.13	Speed selection	RO	1	13:6 1: Bits 5:2 select speed 0: Unspecified x: Unspecified
3.0x0000.12	Reserved	RO	0	Value always 0
3.0x0000.11	Low power	RW	0	1: Low-power mode 0: Normal operation
3.0x0000.10	Clock stop enable	RW	0	1: The PHY may stop the clock during LPI 0: Clock not stoppable
3.0x0000.9:7	Reserved	RO	3'b 0	Value always 0
3.0x0000.6	Speed selection	RO	1	13:6 1: Bits 5:2 select speed 0: Unspecified x: Unspecified
1.0x0000.5:2	Speed selection	RO	4'b 0	5:4:3:2 0: 1Gb/s 1: 2.5Gb/s 0: 5Gb/s 0: 10Gb/s Otherwise: Reserved
1.0x0000.1:0	Reserved	RO	2'b 0	Reserved

Note 1: 3.0x0000.13 & 3.0x0000.6 or 3.0x0000.5:2 will have no effect when Auto-Negotiation is 0. That is, they are unlike 1.0x0000.13 & 1.0x0000.6 or 1.0x0000.5:2.

4.4.2. PCS Status 1 Register (MMD 3.0x0001)

Table 31. PCS Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0001.15:12	Reserved	RO	4'b 0	Value always 0
3.0x0001.11	Tx LPI received	RO, LH	0	1: Tx PCS has received LPI 0: LPI not received
3.0x0001.10	Rx LPI received	RO, LH	0	1: Rx PCS has received LPI 0: LPI not received
3.0x0001.9	Tx LPI indication	RO	0	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
3.0x0001.8	Rx LPI indication	RO	0	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
3.0x0001.7	Fault	RO	0	1: Fault condition detected 0: No fault condition detected
3.0x0001.6	Clock stop capable	RO	0	1: The MAC may stop the clock during LPI 0: Clock not stoppable
3.0x0001.5:3	Reserved	RO	0	Value always 0
3.0x0001.2	PCS receive link status	RO, LL	0	1: PCS receive link up 0: PCS receive link down
3.0x0001.1	Low-power ability	RO	0	1: PCS supports low-power mode 0: PCS does not support low-power mode
3.0x0001.0	Reserved	RO	0	Value always 0

4.4.3. PCS Speed Ability Register (MMD 3.0x0004)

Table 32. PCS Speed Ability Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0004.15:8	Reserved	RO	8'b 0	Value always 0
3.0x0004.7	5G capable	RO	1	1: PCS is capable of operating at 5 Gb/s 0: PCS is not capable of operating at 5 Gb/s
3.0x0004.6	2.5G capable	RO	1	1: PCS is capable of operating at 2.5 Gb/s 0: PCS is not capable of operating at 2.5 Gb/s
3.0x0004.5:1	Reserved	RO	0	Reserved
3.0x0004.0	10G capable	RO	0	1: PCS is capable of operating at 10 Gb/s 0: PCS is not capable of operating at 10 Gb/s

4.4.4. EEE Control and Capability Register (MMD 3.0x0014)

Table 33. EEE Control and Capability Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0014.15:5	Reserved	RO	0	Value always 0
3.0x0014.6	10GBASE-KR EEE	RO	0	1: EEE is supported for 10GBASE-KR 0: EEE is not supported for 10GBASE-KR
3.0x0014.5	10GBASE-KX4 EEE	RO	0	1: EEE is supported for 10GBASE-KX4 0: EEE is not supported for 10GBASE-KX4
3.0x0014.4	1000BASE-KX EEE	RO	0	1: EEE is supported for 1000BASE-KX 0: EEE is not supported for 1000BASE-KX
3.0x0014.3	10GBASE-T EEE	RO	0	1: EEE is supported for 10GBASE-T 0: EEE is not supported for 10GBASE-T
3.0x0014.2	1000BASE-T EEE	RO	1	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
3.0x0014.1	100BASE-TX EEE	RO	1	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
3.0x0014.0	Reserved	RO	0	Value always 0

4.4.5. EEE Control and Capability 2 Register (MMD 3.0x0015)

Table 34. EEE Control and Capability 2 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0015.15:1	Reserved	RO	15'b 0	Value always 0
3.0x0015.1	5GBASE-T EEE	RO	0	1: EEE is supported for 5GBASE-T 0: EEE is not supported for 5GBASE-T
3.0x0015.0	2.5GBASE-T EEE	RO	0	1: EEE is supported for 2.5GBASE-T 0: EEE is not supported for 2.5GBASE-T

4.4.6. EEE Wake Error Counter (MMD 3.0x0016)

Table 35. EEE Wake Error Counter Bit Definitions

Bit	Name	Type	Default	Description
3.0x0016.15:0	EEE wake time fault counter	RO, SC	16'b0	Count EEE wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type

4.4.7. BASE-R and Multi-GBASE-T PCS Status 1 Register (MMD 3.0x0020)

Table 36. BASE-R and Multi-GBASE-T PCS Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0020.15:12	Reserved	RO	4'b0	Value always 0
3.0x0020.11:2	Reserved	RO	10'b0	Value always 0
3.0x0020.1	BASE-R and 10GBASE-T PCS high BER	RO	0	1: BASE-R or 10GBASE-T PCS reporting a high BER 0: BASE-R or 10GBASE-T PCS not reporting a high BER
3.0x0020.0	BASE-R and 10GBASE-T PCS block lock	RO	0	1: BASE-R or 10GBASE-T PCS locked to received blocks 0: BASE-R or 10GBASE-T PCS not locked to received blocks

4.4.8. BASE-R and Multi-GBASE-T PCS Status 2 Register (MMD 3.0x0021)

Table 37. BASE-R and Multi-GBASE-T PCS Status 2 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0021.15	Latched block lock	RO, LL	0	1: BASE-R or 10GBASE-T PCS has block lock 0: BASE-R or 10GBASE-T PCS does not have block lock
3.0x0021.14	Latched high BER	RO, LH	0	1: BASE-R or 10GBASE-T PCS has reported a high BER 0: BASE-R or 10GBASE-T PCS has not reported a high BER
3.0x0021.13:8	BER	RO, RC	6'b0	BER counter
3.0x0021.7:0	Errored blocks	RO, RC	8'b0	Errored blocks counter

4.5. Auto-Negotiation Registers

Table 38. Auto-Negotiation Registers Mapping and Definitions

Register Address	Register Name	Subclause
7.0x0000	AN control	45.2.7.1
7.0x0001	AN status	45.2.7.2
7.0x0010	AN advertisement	45.2.7.6
7.0x0013	AN LP base page ability register	45.2.7.7
7.0x0016 through 7.0x0018	AN XNP transmit	45.2.7.8
7.0x0020	Multi-GBASE-T AN control	45.2.7.10
7.0x0021	Multi-GBASE-T AN status	45.2.7.11
7.0x003C	EEE advertisement	45.2.7.13
7.0x003D	EEE LP ability	45.2.7.14
7.0x003E	EEE advertisement 2	45.2.7.14
7.0x003F	EEE link partner ability 2	45.2.7.14
7.0x0040	Multi-GBASE-TBASE-T AN control 2	45.2.7.14
7.0x0041	Multi-GBASE-TBASE-T AN status 2	45.2.7.14
otherwise	Reserved	Reserved

4.5.1. AN Control Register (MMD 7.0x0000)

Table 39. AN Control Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0000.15	AN reset	RW	0	1: AN reset 0: AN normal operation
7.0x0000.14	Reserved	RO	0	Value always 0
7.0x0000.13	Extended Next Page control	RW	1	1: Extended Next Pages are enabled 0: Extended Next Pages are disabled
7.0x0000.12	Auto-Negotiation enable	RW	1	1: Enable Auto-Negotiation process 0: Disable Auto-Negotiation process
7.0x0000.11:10	Reserved	RO	0	Value always 0
7.0x0000.9	Restart Auto-Negotiation	RW, SC	0	1: Restart Auto-Negotiation process 0: Auto-Negotiation in process, disabled, or not supported
7.0x0000.8:0	Reserved	RO	0	Value always 0

4.5.2. AN Status Register (MMD 7.0x0001)

Table 40. AN Status Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0001.15:10	Reserved	RO	6'b 0	Value always 0
7.0x0001.9	Reserved	RO	0	Value always 0
7.0x0001.8	Reserved	RO	0	Value always 0

Bit	Name	Type	Default	Description
7.0x0001.7	Extended Next Page status	RO	0	1: Extended Next Page format is used 0: Extended Next Page is not allowed
7.0x0001.6	Page received	RO	0	1: A page has been received 0: A page has not been received
7.0x0001.5	Auto-Negotiation complete	RO	0	1: Auto-Negotiation process completed 0: Auto-Negotiation process not completed
7.0x0001.4	Remote fault	RO	0	1: remote fault condition detected 0: no remote fault condition detected
7.0x0001.3	Auto-Negotiation ability	RO	1	1: PHY is able to perform Auto-Negotiation 0: PHY is not able to perform Auto-Negotiation
7.0x0001.2	Link status	RO	0	1: Link is up 0: Link is down
7.0x0001.1	Reserved	RO	0	Value always 0
7.0x0001.0	Link partner Auto-Negotiation ability	RO	0	1: LP is able to perform Auto-Negotiation 0: LP is not able to perform Auto-Negotiation

4.5.3. AN Advertisement Register (MMD 7.0x0010)

Table 41. AN Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0010.15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
7.0x0010.14	Reserved	RO	0	Value always 0
7.0x0010.13	Remote fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
7.0x0010.12	XNP	RW	1	1: Extended Next Page format is used 0: Extended Next Page is not allowed
7.0x0010.11	Asymmetric PAUSE	RW	0	1: Advertise support of asymmetric pause 0: No support of asymmetric pause
7.0x0010.10	PAUSE	RW	1	1: Advertise support of pause frames 0: No support of pause frames
7.0x0010.9	100BASE-T4	RO	0	1: 100BASE-T4 support 0: 100BASE-T4 not supported
7.0x0010.8	100BASE-TX (Full)	RW	1	1: Advertise support of 100BASE-TX full-duplex mode 0: Not advertised
7.0x0010.7	100BASE-TX (Half)	RW	1	1: Advertise support of 100BASE-TX half-duplex mode 0: Not advertised
7.0x0010.6	10BASE-T (Full)	RW	1	1: Advertise support of 10BASE-T full-duplex mode 0: Not advertised
7.0x0010.5	10BASE-T (Half)	RW	1	1: Advertise support of 10BASE-T half-duplex mode 0: Not advertised
7.0x0010.4:0	Selector field	RO	5'b00001	Indicates the RTL8261N supports IEEE 802.3

4.5.4. AN LP Base Page Ability Register (MMD 7.0x0013)

Table 42. AN LP Base Page Ability Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0013.15	Next Page	RO	0	1: Link partner support for transmission and reception of additional link coed word encodings. 0: No additional next pages exchange desired
7.0x0013.14	Acknowledge	RO	0	1: Link partner has successfully received Link Code Word.
7.0x0013.13	Remote fault	RO	0	1: Link partner Indicate to local device that a fault condition has occurred
7.0x0013.12	XNP	RO	0	1: Link partner supports Extended Next Page 0: Extended Next Page is not supported
7.0x0013.11	Asymmetric PAUSE	RO	0	1: Link partner support Asymmetric PAUSE operation for full duplex links 0: No support of asymmetric pause
7.0x0013.10	PAUSE	RO	0	1: Link partner support PAUSE operation for full duplex links 0: No support of pause frames
7.0x0013.9	100BASE-T4	RO	0	1: Link partner support 100BASE-T4 capability 0: 100BASE-T4 not supported
7.0x0013.8	100BASE-TX (Full)	RO	0	1: Link partner support 100BASE-TX full duplex capability 0: Not advertised
7.0x0013.7	100BASE-TX (Half)	RO	0	1: Link partner support 100BASE-TX half duplex capability. 0: Not advertised
7.0x0013.6	10BASE-Te (Full)	RO	0	1: Link partner support 10BASE-Te full duplex capability. 0: Not advertised
7.0x0013.5	10BASE-Te (Half)	RO	0	1: Link partner support 10BASE-Te half duplex capability 0: Not advertised
7.0x0013.4:0	Selector field	RO	5'b00000	Indicates the link partner supports IEEE 802.3

4.5.5. AN XNP Transmit Register (MMD 7.0x0016~7.0x0018)

Table 43. AN XNP Transmit Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0016.15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
7.0x0016.14	Reserved	RO	0	1: Link partner has successfully received Link Code Word.
7.0x0016.13	Message Page	RW	0	1: XNP message page coding 0: XNP unformatted page coding
7.0x0016.12	Acknowledge 2	RW	0	1: Will comply with message 0: Cannot comply with message
7.0x0016.11	Toggle	RO	0	1: Previous value of the transmitted link codeword equaled 1 0: Previous value of the transmitted link codeword equaled 0
7.0x0016.10:0	Message/Unform atted Code Field	RW	11'b 0	If 7.0x0016.13 is 1, then these bits are random seed used for master/slave decision and is RO. Otherwise these bits should be self-defined.
7.0x0017.15:0	Unformatted Code Field 1	RW	16'b 0	Self-defined message used to advertise ability during Auto-Negotiation process

Bit	Name	Type	Default	Description
7.0x0018.15:0	Unformatted Code Field 2	RW	16'b 0	Self-defined message used to advertise ability during Auto-Negotiation process

4.5.6. Multi-GBASE-TBASE-T AN Control 1 Register (MMD 7.0x0020)

Table 44. Multi-GBASE-TBASE-T AN Control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0020.15	MASTER-SLAVE manual config enable	RW	0	1: Enable MASTER-SLAVE manual configuration 0: Disable MASTER-SLAVE manual configuration Default value is 0
7.0x0020.14	MASTER-SLAVE config value	RW	0	1: Configure PHY as MASTER 0: Configure PHY as SLAVE Default value is 0
7.0x0020.13	Port type	RW	1	1: Multiport device 0: single-port device
7.0x0020.12	10GBASE-T ability	RW	1	1: Advertise PHY as 10GBASE-T capable 0: Do not advertise the PHY as 10GBASE-T capable
7.0x0020.11:9	Reserved	RO	3'b 0	Value always 0
7.0x0020.8	5GBASE-T ability	RW	1	1: Advertise PHY as 5GBASE-T capable 0: Do not advertise PHY as 5GBASE-T capable
7.0x0020.7	2.5GBASE-T ability	RW	1	1: Advertise PHY as 2.5GBASE-T capable 0: Do not advertise PHY as 2.5GBASE-T capable
7.0x0020.6	5GBASE-T Fast retrain ability	RW	0	1: Advertise PHY as 5GBASE-T fast retrain capable 0: Do not advertise PHY as 5GBASE-T fast retrain capable
7.0x0020.5	2.5GBASE-T Fast retrain ability	RW	0	1: Advertise PHY as 2.5GBASE-T fast retrain capable 0: Do not advertise PHY as 2.5GBASE-T fast retrain capable
7.0x0020.4:3	Reserved	RO	2'b 0	Value always 0
7.0x0020.2	LD PMA training reset request	RW	0	1: Local device requests that link partner reset PMA training PRBS every frame 0: Local device requests that link partner run PMA training PRBS continuously
7.0x0020.1	10GBASE-T Fast retrain ability	RW	0	1: Advertise PHY as 10GBASE-T fast retrain capable 0: Do not advertise PHY as 10GBASE-T fast retrain capable
7.0x0020.0	LD loop timing ability	RW	1	1: Advertise PHY as capable of loop timing 0: Do not advertise PHY as capable of loop timing

4.5.7. Multi-GBASE-TBASE-T AN Status 1 Register (MMD 7.0x0021)

Table 45. Multi-GBASE-TBASE-T AN Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0021.15	MASTER-SLAVE manual config enable	RO, LH, SC	0	1: MASTER-SLAVE configuration fault detected 0: No MASTER-SLAVE configuration fault detected
7.0x0021.14	MASTER-SLAVE config value	RO	0	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
7.0x0021.13	Local receiver status	RO	0	1: Local receiver OK 0: Local receiver not OK
7.0x0021.12	Remote receiver status	RO	0	1: Remote receiver OK 0: Remote receiver not OK
7.0x0021.11	Link partner 10GBASE-T capability	RO	0	1: Link partner is able to operate as 10GBASE-T 0: Link partner is not able to operate as 10GBASE-T This bit is guaranteed to be valid only when the Page received bit (7.0x0001.6) has been set to 1.
7.0x0021.10	LP loop timing ability	RO	0	1: Link partner is capable of loop timing 0: Link partner is not capable of loop timing
7.0x0021.9	LP PMA training reset request	RO	0	1: Link partner requests that local device reset PMA training PRBS every frame 0: Link partner requests that local device run PMA training PRBS continuously
7.0x0021.8:7	Reserved	RO	2'b 0	Value always 0
7.0x0021.6	Link partner 5GBASE-T capability	RO	0	1: Link partner is able to operate as 5GBASE-T 0: Link partner is not able to operate as 5GBASE-T
7.0x0021.5	Link partner 2.5GBASE-T capability	RO	0	1: Link partner is able to operate as 2.5GBASE-T 0: Link partner is not able to operate as 2.5GBASE-T
7.0x0021.4	5GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 5GBASE-T fast retrain 0: Link partner is not capable of 5GBASE-T fast retrain
7.0x0021.3	2.5GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 2.5GBASE-T fast retrain 0: Link partner is not capable of 2.5GBASE-T fast retrain
7.0x0021.2	Reserved	RO	0	Value always 0
7.0x0021.1	10GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 10GBASE-T fast retrain 0: Link partner is not capable of 10GBASE-T fast retrain
7.0x0021.0	Reserved	RO	0	Value always 0

4.5.8. EEE Advertisement Register (MMD 7.0x003C)

Table 46. EEE Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003C.15:7	Reserved	RO	9'b 0	Value always 0
7.0x003C.6	10GBASE-KR EEE	RO	0	1: Advertise that the 10GBASE-KR has EEE capability 0: Do not advertise that the 10GBASEKR has EEE capability
7.0x003C.5	10GBASE-KX4 EEE	RO	0	1: Advertise that the 10GBASE-KX4 has EEE capability 0: Do not advertise that the 10GBASEKX4 has EEE capability
7.0x003C.4	1000BASE-KX EEE	RO	0	1: Advertise that 1000BASE-KX has EEE capability 0: Do not advertise that 1000BASEKX has EEE capability
7.0x003C.3	10GBASE-T EEE	RO	0	1: Advertise that the 10GBASE-T has EEE capability 0: Do not advertise that the 10GBASE-T has EEE capability
7.0x003C.2	1000BASE-T EEE	RW	1	1: Advertise that 1000BASE-T has EEE capability 0: Do not advertise that 1000BASE-T has EEE capability
7.0x003C.1	100BASE-TX EEE	RW	1	1: Advertise that 100BASE-TX has EEE capability 0: Do not advertise that 100Basetx has EEE capability in
7.0x003C.0	Reserved	RO	0	Value always 0

4.5.9. EEE Link Partner Ability Register (MMD 7.0x003D)

Table 47. EEE Link Partner Ability Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003D.15:7	Reserved	RO	0	Value always 0
7.0x003D.6	10GBASE-KR EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-KR 0: Link partner is not advertising EEE capability for 10GBASE-KR
7.0x003D.5	10GBASE-KX4 EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-KX4 0: Link partner is not advertising EEE capability for 10GBASE-KX4
7.0x003D.4	1000BASE-KX EEE	RO	0	1: Link partner is advertising EEE capability for 1000BASE-KX 0: Link partner is not advertising EEE capability for 1000BASE-KX
7.0x003D.3	10GBASE-T EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-T 0: Link partner is not advertising EEE capability for 10GBASE-T
7.0x003D.2	1000BASE-T EEE	RO	0	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
7.0x003D.1	100BASE-TX EEE	RO	0	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
7.0x003D.0	Reserved	RO	0	Value always 0

4.5.10. EEE Advertisement 2 Register (MMD 7.0x003E)

Table 48. EEE Advertisement 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003E.15:2	Reserved	RO	14'b 0	Value always 0
7.0x003E.1	5GBASE-T EEE	RW	0	1: Advertise that the 5GBASE-T has EEE capability 0: Do not advertise that the 5GBASE-T has EEE capability
7.0x003E.0	2.5GBASE-T EEE	RW	0	1: Advertise that the 2.5GBASE-T has EEE capability 0: Do not advertise that the 2.5GBASE-T has EEE capability

4.5.11. EEE Link Partner Ability 2 Register (MMD 7.0x003F)

Table 49. EEE Link Partner Ability 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003F.15:2	Reserved	RO	14'b 0	Value always 0
7.0x003F.1	5GBASE-T EEE	RO	0	1: Link partner is advertising that the 5GBASE-T has EEE capability 0: Link partner is not advertising that the 5GBASE-T has EEE capability
7.0x003F.0	2.5GBASE-T EEE	RO	0	1: Link partner is advertising that the 2.5GBASE-T has EEE capability 0: Link partner is not advertising that the 2.5GBASE-T has EEE capability

4.5.12. Multi-GBASE-TBASE-T AN Control 2 Register (MMD 7.0x0040)

Table 50. Multi-GBASE-TBASE-T AN Control 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0040.15:4	Reserved	RO	12'b 0	Value always 0
7.0x0040.3	2.5GBASE-T THP Bypass Request	RW	1	1: Local device requests link partner to initially reset THP during fast retrain 0: Local device requests link partner not to initially reset THP during fast retrain
7.0x0040.2	5GBASE-T THP Bypass Request	RW	1	1: Local device requests link partner to initially reset THP during fast retrain 0: Local device requests link partner not to initially reset THP during fast retrain
7.0x0040.1:0	Reserved	RO	2'b 0	Value always 0

4.5.13. Multi-GBASE-TBASE-T AN Status 2 Register (MMD 7.0x0041)

Table 51. Multi-GBASE-TBASE-T AN Status 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0041.15:4	Reserved	RO	12'b 0	Value always 0
7.0x0041.3	2.5GBASE-T Link Partner THP Bypass Request	RO	0	1: Link partner requests local device to initially reset THP during fast retrain 0: Link partner requests local device not to initially reset THP during fast retrain
7.0x0041.2	5GBASE-T Link Partner THP Bypass Request	RO	0	1: Link partner requests local device to initially reset THP during fast retrain 0: Link partner requests local device not to initially reset THP during fast retrain
7.0x0041.1:0	Reserved	RO	2'b 0	Value always 0

4.6. TOP Register

Table 52. TOP Registers Mapping and Definitions

Register Address	Register Name
30.0x103	PKG model
30.0x104	Version ID

4.6.1. Serdes Global Config Register (MMD 30.0xC1)

Table 53. Serdes Global Config Register Bit Definitions

Bit	Name	Type	Default	Description
30.0xC1.15:8	Reserved	RO	0x0	Value always 0
30.0xC1.7	HSO_INV	RW	0x0	HSOP, HSON Inverse
30.0xC1.6	HSI_INV	RW	0x1	HSIP, HSIN inverse
30.0xC1.5:0	Reserved	RO	0x0	Value always 0

4.6.2. PKG model Register (MMD 30.0x103)

Table 54. PKG model Register Bit Definitions

Bit	Name	Type	Default	Description
30.0x103.15:0	PKG_MODEL	RO	0x8261	RTL number : 8261N

4.6.3. Version ID Register (MMD 30.0x104)

Table 55. Version ID Register Bit Definitions

Bit	Name	Type	Default	Description
30.0x104.15:11	MODEL_CHAR_1ST	RO	0xE	First English character of model name 0x0: Industrial-grade 0x1-0x1A: character A - Z 0x1B-0x1E: invalid 0x1F:NULL
30.0x104.15:4	Reserved	RO	0	Value always 0
30.0x104.3:0	Version ID	RO	0x0	RTL number Version ID. Record the RTL Version ID. Counting start from 0. 0,1,2,3 map to version A,B,C,D

4.7. Serdes 10G -R/5G-R Register

4.7.1.PCS Control 1 Register (Page4 Register0)

Table 56. PCS Control 1 Register Bit Definitions

Bit	Name	Description	Type	Default
15	FP_PCS0_RST	Reset: 0b0: Normal operation 0b1: DTE XS reset	RWAC	0x0
14	FP_PCS0_LPB	Loopback: 0b0: Disable loopback mode 0b1: Enable loopback mode	RW	0x0
13	FP_PCS0_SPD_SEL_1	Speed Selection 0b0: Unspecified 0b1: Operation at 10Gb/s and above	RO	0x1
12	FP_PCS0_DUMMY_12	dummy register	RO	0x0
11	FP_PCS0_LO_PWR	Low Power: 0b0: Normal operation 0b1: Low-power mode	RW	0x0
10	FP_PCS0_DUMMY_10	dummy register	RW	0x0
9 : 7	FP_PCS0_DUMMY_9_7	Value always 0	RO	0x0
6	FP_PCS0_SPD_SEL_0	Speed Selection 0b0: Unspecified 0b1: Operation at 10Gb/s and above	RO	0x1
5 : 2	FP_PCS0_SPD_TYPE_SEL	5 4 3 2 1 x x x = Reserved 0 1 1 x = Reserved 0 1 0 1 = 25Gb/s 0 1 0 0 = 100Gb/s 0 0 1 1 = 40Gb/s 0 0 1 0 = 10/1 Gb/s, which is not supported 0 0 0 1 = 10PASS-TS/2BASE-TL, which is not supported 0 0 0 0 = 10Gb/s	RO	0x0
1 : 0	FP_PCS0_DUMMY_1_0	Value always 0	RO	0x0

4.7.2.PCS Status 1 Register (Page4 Register1)

Table 57. PCS Status 1 Register Bit Definitions

Bit	Name	Description	Type	Default
15:12	FP_PCS1_DUMMY_15_12	dummy register	RO	0x0
11	FP_PCS1_TX_LPI_LH	TX latch received LPI 0x0 : TX PCS not latch received LPI 0x1 : TX latch received LPI	RO	0x0
10	FP_PCS1_RX_LPI_LH	RX latch received LPI 0x0 : RX not latch received LPI 0x1 : RX latch received LPI	RO	0x0
9	FP_PCS1_TX_LPI	TX LPI indication 0x0 : TX PCS is currently receiving LPI 0x1 : PCS is not currently receiving LPI	RO	0x0
8	FP_PCS1_RX_LPI	RX LPI indication 0x0 : RX PCS is currently receiving LPI 0x1 : PCS is not currently receiving LPI	RO	0x0
7	FP_PCS1_FAULT_DET	Fault 0b0: No Fault condition detected 0b1: Fault condition detected	RO	0x0
6	FP_PCS1_CLK_STOP_CAP	Clock stop capable 0b0: clock not stoppable 0b1: The MAC may stop the clock during LPI	RO	0x0
5:3	FP_PCS1_DUMMY_5_3	dummy register	RO	0x0
2	FP_PCS1_RX_LINK	DTE XS Receive Link Status: 0b0: DTE XS receive link down 0b1: DTE XS receive link up	RO	0x0
1	FP_PCS1_LO_PWR_ABLTY	Low Power Ability: 0b0: DTE XS does not support low-power mode 0b1: DTE XS supports low-power mode	RO	0x0
0	FP_PCS1_DUMMY_0	dummy register	RW	0x0

4.7.3.PCS Device Identifier Register (Page4 Register2)

Table 58. PCS Device Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS2_DEV_ID	PCS Device Identifier. (See IEEE std. 802.3-45.2.3.3)	RO	0x1c

4.7.4.PCS Device Identifier Register (Page4 Register3)

Table 59. PCS Device Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS2_DEV_ID	PCS Device Identifier. (See IEEE std. 802.3-45.2.3.3)	RO	0xcaf3

4.7.5.PCS Speed Ability Register (Page4 Register4)

Table 60. PCS Speed Ability Register Bit Definitions

Bit	Name	Description	Type	Default
15:5	RESERVED		RW	0x0
4	FP_PCS4_B4	1 = PCS is capable of operating at 25Gb/s 0 = PCS is not capable of operating at 25Gb/s	RO	0x0
3	FP_PCS4_B3	1 = PCS is capable of operating at 100Gb/s 0 = PCS is not capable of operating at 100Gb/s	RO	0x0
2	FP_PCS4_B2	1 = PCS is capable of operating at 40Gb/s 0 = PCS is not capable of operating at 40Gb/s	RO	0x0
1	FP_PCS4_10P_TS_2B_TL_CAPABLE	10PASS-TS/2BASE-TL Capable: (See IEEE std. 802.3-45.2.3.4) 0b0: PCS is not capable of operating as the 10P/2B PCS 0b1: PCS is capable of operating as the 10P/2B PCS	RO	0x0
0	FP_PCS4_10G_CAPABLE	10G Capable: 0b0: DTE is not capable of operating at 10Gb/s 0b1: DTE is capable of operating at 10Gb/s	RO	0x1

4.7.6.PCS Devices In Package Register (Page4 Register5)

Table 61. PCS devices in package Register Bit Definitions

Bit	Name	Description	Type	Default
15:8	FP_PCS5_DUMMY_15_8	dummy register	RO	0x0
7	FP_PCS5_NWAY_PRSNT	Auto-Negotiation Present: 0b0: Auto-Negotiation not present in package 0b1: Auto-Negotiation present in package	RO	0x0
6	FP_PCS5_TC_PRSNT	TC Present: 0b0: TC not present in package 0b1: TC present in package	RO	0x0
5	FP_PCS5_DTE_XS_PRSNT	DTE XS Present: 0b0: DTE XS not present in package 0b1: DTE XS present in package	RO	0x1
4	FP_PCS5_PHY_XS_PRSNT	PHY XS Present: 0b0: PHY XS not present in package 0b1: PHY XS present in package	RO	0x0
3	FP_PCS5_PRSNT	PCS Present: 0b0: PCS not present in package 0b1: PCS present in package	RO	0x1
2	FP_PCS5_WIS_PRSNT	WIS Present: 0b0: WIS not present in package 0b1: WIS present in package	RO	0x0
1	FP_PCS5_PMA_PMD_PRSNT	PMA/PMD Present: 0b0: PMA/PMD not present in package 0b1: PMA/PMD present in package	RO	0x1
0	FP_PCS5_CLAUSE_22_PRSNT	Clause 22 Register Present: 0b0: Clause 22 Register not present in package 0b1: Clause 22 Register present in package	RO	0x0

4.7.7.PCS Devices In Package Register (Page4 Register6)

Table 62. PCS devices in package Register Bit Definitions

Bit	Name	Description	Type	Default
15:3	FP_PCS6_DUMMY_15_3	dummy register	RO	0x0
2	FP_PCS6_VNDR_SPEC_DEV_2_PRSNT	Vendor Specific Device 2 Present: (See IEEE std. Table 45-2) 0b0: Vendor specific device 2 not present in package 0b1: Vendor specific device 2 present in package	RO	0x0
1	FP_PCS6_VNDR_SPEC_DEV_1_PRSNT	Vendor Specific Device 1 Present: 0b0: Vendor specific device 1 not present in package 0b1: Vendor specific device 1 present in package	RO	0x0
0	FP_PCS6_CLAUSE_22_EXT_PRSNT	Clause 22 Extension Present: 0b0: Clause 22 extension not present in package 0b1: Clause 22 extension present in package	RO	0x0

4.7.8.PCS Control 2 Register (Page4 Register7)

Table 63. PCS Control 2 Register Bit Definitions

Bit	Name	Description	Type	Default
15:3	FP_PCS7_DUMMY_15_2	dummy register	RO	0x0
2:0	FP_PCS7_TYPE_SEL	2 1 0 1 1 1 = Select 25GBASE-R PCS type 1 1 0 = Reserved 1 0 1 = Select 100GBASE-R PCS type 1 0 0 = Select 40GBASE-R PCS type 0 1 1 = Select 10GBASE-T PCS type, which is not supported 0 1 0 = Select 10GBASE-W PCS type, which is not supported 0 0 1 = Select 10GBASE-X PCS type, which is not supported 0 0 0 = Select 10GBASE-R PCS type	RO	0x0

4.7.9.PCS Status 2 Register (Page4 Register8)

Table 64. PCS Status 2 Register Bit Definitions

Bit	Name	Description	Type	Default
14	FP_PCS8_DEV_PR_SNT	Device Present: 0x0: No device responding at this address 0x1: No device responding at this address 0x2: Device responding at this address 0x3: No device responding at this address	RO	0x2
12	FP_PCS8_DUMMY_13_12	dummy register	RO	0x0
11	FP_PCS8_TX_FAULT	Transmit Fault: 0b0: No fault condition on transmit path 0b1: Fault condition on transmit path	RO	0x0
10	FP_PCS8_RX_FAULT	Receive Fault: 0b0: No fault condition on receive path 0b1: Fault condition on receive path	RO	0x0
8	RESERVED		RW	0x0
7	FP_PCS8_B7	25GBASE-R Capable 0b0: PCS is not able to support 25GBASE-R PCS type 0b1: PCS is able to support 25GBASE-R PCS type	RO	0x0
6	RESERVED		RW	0x0
5	FP_PCS8_B5	100GBASE-R Capable 0b0: PCS is not able to support 100GBASE-R PCS type 0b1: PCS is able to support 100GBASE-R PCS type	RO	0x0
4	FP_PCS8_B4	40GBASE-R Capable 0b0: PCS is not able to support 40GBASE-R PCS type 0b1: PCS is able to support 40GBASE-R PCS type	RO	0x0
3	FP_PCS8_10GBASE_T_CAPABLE	10GBASE-T Capable. 0b0: PCS is not able to support 10GBASE-T PCS type 0b1: PCS is able to support 10GBASE-T PCS type	RO	0x0
2	FP_PCS8_10GBASE_W_CAPABLE	10GBASE-W Capable: 0b0: PCS is not able to support 10GBASE-W PCS type 0b1: PCS is able to support 10GBASE-W PCS type	RO	0x0
1	FP_PCS8_10GBASE_X_CAPABLE	10GBASE-X Capable: 0b0: PCS is not able to support 10GBASE-X PCS type 0b1: PCS is able to support 10GBASE-X PCS type	RO	0x0
0	FP_PCS8_10GBASE_R_CAPABLE	10GBASE-R Capable: 0b0: PCS is not able to support 10GBASE-R PCS type 0b1: PCS is able to support 10GBASE-R PCS type	RO	0x1
14	FP_PCS8_DEV_PR_SNT	Device Present: 0x0: No device responding at this address 0x1: No device responding at this address 0x2: Device responding at this address 0x3: No device responding at this address	RO	0x2

4.7.10. PCS Package Identifier Register (Page4 Register14)

Table 65. PCS Package Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS14_PKG_ID	DTE XS Package Identifier.	RO	0x0

4.7.11. PCS Package Identifier Register (Page4 Register15)

Table 66. PCS Package Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS15_PKG_ID	DTE XS Package Identifier.	RO	0x0

4.7.12. PCS Package Identifier Register (Page4 Register20)

Table 67. PCS Package Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:7	FP_PCS32_DUMMY_15_7	dummy register	RO	0x0
6	FP_PCS20_10G_KR_EEE	10GBase-KR EEE 1'b0: EEE is not supported for PHY XS 1'b1: EEE is supported for PHY XS	RO	0x0
5:0	FP_PCS20_DUMMY_5_0	dummy register	RO	0x0

4.7.13. PCS Package Identifier Register (Page4 Register22)

Table 68. PCS Package Identifier Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS22_WAKE_ERR_CNT	EEE wake error counter	RO	0x0

4.7.14. 10GBASE-R PCS status 1 register (Page5 Register0)

Table 69. 10GBASE-R PCS status 1 Register Bit Definitions

Bit	Name	Description	Type	Default
15:13	FP_PCS32_DUMMY_15_13	dummy register	RW	0x0
12	FP_PCS32_10GBASE_R_T_RX_LINK	10GBASE-R and 10GBASE-T Receive Link Status: (See IEEE std. 802.3-45.2.3.11) 0b0: 10GBASE-R or 10GBASE-T PCS receive link down 0b1: 10GBASE-R or 10GBASE-T PCS receive link up	RO	0x0
11:4	FP_PCS32_DUMMY_11_4	dummy register	RW	0x0
3	FP_PCS32_PRBS9_TEST_PTR_N_ABLTY	PRBS9 Pattern Testing Ability: 0b0: PCS is not able to support PRBS9 pattern testing 0b1: PCS is able to support PRBS9 pattern testing	RO	0x1
2	FP_PCS32_PRBS31_TEST_PT_RN_ABLTY	PRBS31 Pattern Testing Ability: 0b0: PCS is not able to support PRBS31 pattern testing 0b1: PCS is able to support PRBS31 pattern testing	RO	0x1
1	FP_PCS32_10GBASE_R_T_HI_BER	10GBASE-R and 10GBASE-T PCS High BER: 0b0: 10GBASE-R or 10GBASE-T PCS not reporting a high BER 0b1: 10GBASE-R or 10GBASE-T PCS reporting a high BER	RO	0x0
0	FP_PCS32_10GBASE_R_T_BLK_LOCK	10GBASE-R and 10GBASE-T PCS Block Lock: 0b0: 10GBASE-R or 10GBASE-T PCS not locked to received blocks 0b1: 10GBASE-R or 10GBASE-T PCS locked to received blocks	RO	0x0

4.7.15. 10GBASE-R PCS status 2 register (Page5 Register1)

Table 70. 10GBASE-R PCS status 2 Register Bit Definitions

Bit	Name	Description	Type	Default
15	FP_PCS33_LATCH_BLK_LOCK	Latched Block Lock: (See IEEE std. 802.3-45.2.3.12) 0b0: 10GBASE-R or 10GBASE-T PCS does not have block lock 0b1: 10GBASE-R or 10GBASE-T PCS has block lock	RO	0x0
14	FP_PCS33_LATCH_HI_BER	Latched High BER: 0b0: 10GBASE-R or 10GBASE-T PCS has not reported a high BER 0b1: 10GBASE-R or 10GBASE-T PCS has reported a high BER	RO	0x0
8	FP_PCS33_BER_CNTR	MMD 3.33.13:8 BER BER counter. These bits shall be reset to all zeros MMD 3.33 is read by the management function or upon execution of the PCS reset. If the Errored blocks high order counter, MMD 3.45 is not implemented then these bits shall be held at all ones in the case of overflow	RO	0x0
0	FP_PCS33_ERR_BLK_CNTR	3.33.7:0 Errored blocks Errored blocks counter. These bits shall be reset to all zeros MMD 3.33 is read by the management function or upon execution of the PCS reset. If the BER high order counter, MMD 3.44 is not implemented then these bits shall be held at all ones in the case of overflow.	RO	0x0

4.7.16. 10GBASE-R PCS Test Pattern Seed A Register (Page5 Register2)

Table 71. 10GBASE-R PCS Test Pattern Seed A Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS34_TEST_PTRN_SEE_D_A0	Test Pattern Seed A0: Test pattern seed A bits 0-15	RW	0x0

4.7.17. 10GBASE-R PCS Test Pattern Seed A Register (Page5 Register3)

Table 72. 10GBASE-R PCS Test Pattern Seed A Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS35_TEST_PTRN_SEE_D_A1	Test Pattern Seed A1: (See IEEE std. 802.3-45.2.3.13) Test pattern seed A bits 16-31	RW	0x0

4.7.18. 10GBASE-R PCS Test Pattern Seed A Register (Page5 Register4)

Table 73. 10GBASE-R PCS Test Pattern Seed A Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS36_TEST_PTRN_SEE_D_A2	Test Pattern Seed A2: Test pattern seed A bits 32-47	RW	0x0

4.7.19. 10GBASE-R PCS Test Pattern Seed A Register (Page5 Register5)

Table 74. 10GBASE-R PCS Test Pattern Seed A Register Bit Definitions

Bit	Name	Description	Type	Default
15:10	FP_PCS37_DUMMY_15_10	dummy register	RO	0x0
9:0	FP_PCS37_TEST_PTRN_SEE D_A3	Test Pattern Seed A3: (See IEEE std. 802.3-45.2.3.13) Test pattern seed A bits 48-57	RW	0x0

4.7.20. 10GBASE-R PCS Test Pattern Seed B Register (Page5 Register6)

Table 75. 10GBASE-R PCS Test Pattern Seed B Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS38_TEST_PTRN_SEE D_B0	Test Pattern Seed B0: Test pattern seed B bits 0-15	RW	0x0

4.7.21. 10GBASE-R PCS Test Pattern Seed B Register (Page5 Register7)

Table 76. 10GBASE-R PCS Test Pattern Seed B Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS39_TEST_PTRN_SEE D_B1	Test Pattern Seed B1: (See IEEE std. 802.3-45.2.3.13) Test pattern seed B bits 16-31	RW	0x0

4.7.22. 10GBASE-R PCS Test Pattern Seed B Register (Page5 Register8)

Table 77. 10GBASE-R PCS Test Pattern Seed B Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS40_TEST_PTRN_SEE D_B2	Test Pattern Seed B2: Test pattern seed B bits 32-47	RW	0x0

4.7.23. 10GBASE-R PCS Test Pattern Seed B Register (Page5 Register9)

Table 78. 10GBASE-R PCS Test Pattern Seed B Register Bit Definitions

Bit	Name	Description	Type	Default
15:10	FP_PCS41_DUMMY_15_10	dummy register	RO	0x0
9:0	FP_PCS41_TEST_PTRN_SEE D_B3	Test Pattern Seed B3: (See IEEE std. 802.3-45.2.3.13) Test pattern seed B bits 48-57	RW	0x0

4.7.24. 10GBASE-R PCS test-pattern control Register (Page5 Register10)

Table 79. 10GBASE-R PCS status 2 Register Bit Definitions

Bit	Name	Description	Type	Default
14	FP_PCS42_DUMMY_15_14	dummy register	RW	0x0
13	FP_PCS42_PRBS7_RX_TEST_PTRN_EN	PRBS7 Transmit Test Pattern Enable 0b0: Disable PRBS7 test-pattern mode on the transmit path 0b1: Enable PRBS7 test-pattern mode on the transmit path	RW	0x0
12	FP_PCS42_PRBS7_RX_TEST_PTRN_EN	PRBS7 Receive Test Pattern Enable: 0b0: Disable PRBS7 test-pattern mode on the receive path 0b1: Enable PRBS7 test-pattern mode on the receive path	RW	0x0
11	FP_PCS42_PRBS23_RX_TEST_PTRN_EN	PRBS23 Transmit Test Pattern Enable 0b0: Disable PRBS23 test-pattern mode on the transmit path 0b1: Enable PRBS23 test-pattern mode on the transmit path	RW	0x0
10	FP_PCS42_PRBS23_RX_TEST_PTRN_EN	PRBS23 Receive Test Pattern Enable: 0b0: Disable PRBS23 test-pattern mode on the receive path 0b1: Enable PRBS23 test-pattern mode on the receive path	RW	0x0
9	FP_PCS42_PRBS15_RX_TEST_PTRN_EN	PRBS15 Transmit Test Pattern Enable 0b0: Disable PRBS15 test-pattern mode on the transmit path 0b1: Enable PRBS15 test-pattern mode on the transmit path	RW	0x0
8	FP_PCS42_PRBS15_RX_TEST_PTRN_EN	PRBS15 Receive Test Pattern Enable: 0b0: Disable PRBS15 test-pattern mode on the receive path 0b1: Enable PRBS15 test-pattern mode on the receive path	RW	0x0
7	FP_PCS42_PRBS9_RX_TEST_PTRN_EN	PRBS9 Receive Test Pattern Enable 0b0: Disable PRBS9 test-pattern mode on the transmit path 0b1: Enable PRBS9 test-pattern mode on the transmit path	RW	0x0
6	FP_PCS42_PRBS9_RX_TEST_PTRN_EN	MMD 3.42.6 10GBASE-R PRBS9 transmit test-pattern enable 1 = Enable PRBS9 test-pattern mode on the transmit path 0 = Disable PRBS9 test-pattern mode on the transmit path the mandatory transmit testpattern enable bit (3.42.3) is not one, and the optional PRBS31 transmit test-pattern enable bit (3.42.4) is not one, then when bit 3.42.6 is set to one the PCS shall transmit PRBS9	RW	0x0

Bit	Name	Description	Type	Default
5	FP_PCS42_PRBS31_RX_TEST_PTRN_EN	MMD 3.42.5 10GBASE-R PRBS31 receive test-pattern enable 1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.42.5 to a one shall set the receive path of the PCS into the PRBS31 test-pattern mode	RW	0x0
4	FP_PCS42_PRBS31_TX_TEST_PTRN_EN	MMD 3.42.4 10GBASE-R PRBS31 transmit test-pattern enable 1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode	RW	0x0
3	FP_PCS42_TX_TEST_PTRN_EN	Transmit Test Pattern Enable: 0b0: Disable test-pattern mode on the transmit path 0b1: Enable test-pattern mode on the transmit path	RW	0x0
2	FP_PCS42_RX_TEST_PTRN_EN	Receive Test Pattern Enable: 0b0: Disable test-pattern mode on the receive path 0b1: Enable test-pattern mode on the receive path	RW	0x0
1	FP_PCS42_TEST_PTRN_SEL	Test Pattern Select: 0b0: Pseudo random test pattern 0b1: Square wave test pattern	RW	0x0
0	FP_PCS42_DATA_PTRN_SEL	Data Pattern Select: 0b0: Zeros data pattern 0b1: LF data pattern	RW	0x0

4.7.25. 10GBASE-R PCS Test-Pattern Error Counter Register (Page5 Register11)

Table 80. 10GBASE-R PCS Test-Pattern Error Counter Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS43_TEST_PTRN_ERR_CNT	MMD 3.43.15:0 Test-pattern error counter Error counter. The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.	RO	0x0

4.7.26. 10GBASE-R FEC Ability Register (Page12 Register10)

Table 81. 10GBASE-R FEC Ability Register Bit Definitions

Bit	Name	Description	Type	Default
15:2	FP_PCS170_DUMMY_15_2	MMD 1.170.15:2 Value always 0	RW	0x0
1	FP_PCS170_FEC_ERR_ABILITY	MMD 1.170.1 BASE-R FEC error indication ability A read of 1 in this bit indicates that the sublayer is able to perform report FEC decoding errors to the PCS layer	RO	0x1
0	FP_PCS170_FEC_ABILITY	MMD 1.170.0 BASE-R FEC ability A read of 1 in this bit indicates that the sublayer supports FEC	RO	0x1

4.7.27. 10GBASE-R FEC Control Register (Page12 Register11)

Table 82. 10GBASE-R FEC Control Register Bit Definitions

Bit	Name	Description	Type	Default
15:2	FP_PCS171_DUMMY_15_2	MMD 1.171.15:2 Value always 0	RW	0x0
1	FP_PCS171_FEC_ERR2PCS	MMD 1.171.1 FEC enable error indication A write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer	RW	0x0
0	FP_PCS171_FEC_ENABLE	MMD 1.171.0 FEC enable A write of 1 to this bit enables BASE-R FEC A write of 0 to this bit enables BASE-R FEC	RW	0x0

4.7.28. 10GBASE-R FEC Corrected Blocks Counter Register (Page12 Register12)

Table 83. 10GBASE-R FEC Corrected Blocks Counter Register Bit Definitions

Bit	Name	Description	Type	Default
15:0	FP_PCS172_FEC_CRT_CNT_15_0	MMD 1.172.15:0 FEC corrected blocks lower, RO/NR FEC corrected_blocks_counter<15:0>	RO	0x0

4.7.29. 10GBASE-R FEC Corrected Blocks Counter Register (Page12 Register13)

Table 84. 10GBASE-R FEC Corrected Blocks Counter Register Bit Definitions

Bit	Name	Description	Type	Default
15:0 31_16	FP_PCS173_FEC_CRT_CNT_	MMD 1.173.15:0 FEC corrected blocks upper, RO/NR FEC corrected_blocks_counter<31:16>	RO	0x0

4.7.30. 10GBASE-R FEC Uncorrected Blocks Counter Register (Page12 Register14)

Table 85. 10GBASE-R FEC Uncorrected Blocks Counter Register Bit Definitions

Bit	Name	Description	Type	Default
15:0 T_15_0	FP_PCS174_FEC_UNCRT_CN	MMD 1.174.15:0 FEC uncorrected blocks lower, RO/NR FEC_uncorrected_blocks_counter<15:0> FEC_uncorrected_blocks_upper<15:0>	RO	0x0

4.7.31. 10GBASE-R FEC Uncorrected Blocks Counter Register (Page12 Register15)

Table 86. 10GBASE-R FEC Uncorrected Blocks Counter Register Bit Definitions

Bit	Name	Description	Type	Default
15:0 T_31_16	FP_PCS175_FEC_UNCRT_CN	MMD 1.175.15:0 FEC uncorrected blocks higher, RO/NR FEC_uncorrected_blocks_counter<31:16> FEC_uncorrected_blocks_upper<15:0>	RO	0x0

4.8. Serdes 5G/2.5G/1GBASE-X Register

4.8.1.PCS Register 0: Control (Page4 Register0)

Table 87. PCS Register 0: Control

Bit	Name	Description	Type	Default
15	Reset	1: PHY reset 0: Normal operation This bit is self-clearing.	RW/SC	0x0
14	Loopback (Digital Loopback)	1: Enable loopback This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation	RW	0x0
13	Speed Selection[0]	[0.6, 0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	RW	0x1
12	Auto Negotiation Enable	1: Enable auto-negotiation process 0: Disable auto-negotiation process	RW	0x0
11	Power Down	1: Power down. All functions will be disabled except SMI function 0: Normal operation	RW	0x0
10	Isolate	1: Electrically isolates the PHY The PHY is still able to respond to MDC/MDIO. 0: Normal operation	RW	0x0
9	Restart Auto Negotiation	1: Restart Auto-Negotiation process 0: Normal operation	RW/SC	0x0
8	Duplex Mode	1: Full duplex operation 0: Half duplex operation	RW	0x1
7	Reserved	Reserved	RO	0x0
6	Speed Selection[1]	See Bit 13	RW	0x0
5:0	Reserved	Reserved	RO	0x0

4.8.1.PCS Register 1: Status (Page4 Register1)

Table 88. PCS Register 1: Status

Bit	Name	Description	Type	Default
15 : 6	FIB_CAPBILITY	Fiber Auto-negotiation ability capability	RO	0x180
5	Auto-negotiate Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0x0
4	Remote Fault	1: Remote fault indication from link partner has been detected 0: No remote fault indication detected This bit will remain set until it is cleared by reading register 1 via management interface.	RO/LH	0x0
3	Auto-Negotiation Ability	1: Auto-negotiation capable	RO	0x0
2	Link Status	1: Link has never failed since previous read 0: Link has failed since previous read If link fails, this bit will be set to 0 until bit is read.	RO/LL	0x0
1	Jabber Detect	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	RO/LH	0x0
0	Extended Capability	1: Extended register capable	RO	0x0

4.8.2.PCS Register 2: PHY Identifier 1 (Page4 Register2)

Table 89. PCS Register 2: PHY Identifier 1

Bit	Name	Description	Type	Default
15:0	OUI	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI), Respectively	RO	0x1C

4.8.3.PCS Register 3: PHY Identifier 2 (Page4 Register3)

Table 90. PCS Register 3: PHY Identifier 2

Bit	Name	Description	Type	Default
15:10	OUI	Assigned to the 19th through 24th Bits of the Organizationally Unique Identifier (OUI)	RO	0x32
9:4	Model Number	Manufacturer's Model number	RO	0x2F
3:0	Revision Number	Manufacturer's Revision number	RO	0x3

4.8.4. PCS Register 4: 1000Base-X Auto-Negotiation Advertisement (Page4 Register4)

Table 91. PCS Register 4: 1000Base-X Auto-Negotiation Advertisement

Bit	Name	Description	Type	Default
15	Next Page	1: Additional next pages exchange desired 0: No additional next pages exchange desired	RW	0x0
14	Reserved	Reserved	RO	0x0
13 : 12	Remote Fault	00: No error, link OK (default) 01: Link Failure 10: Offline 11: Auto-Negotiation Error	RW	0x0
11 : 9	Reserved	Reserved	RO	0x6
8 : 7	Pause ability	Bit8 : 1: Enable Asymmetric Pause 0: Disable Asymmetric Pause Bit7 : 1: Advertises that possesses 802.3x flow control capability 0: No flow control capability	RW	0x0
6	Half Duplex	1: Half Duplex capable 0: Not Half Duplex capable	RW	0x0
5	Full Duplex	1: Full Duplex capable 0: Not Full Duplex capable	RW	0x0
4 : 0	Reserved	Reserved	RO	0x1

4.8.5. PCS Register 5: 1000Base-X Auto-Negotiation Link Partner Ability (Page4 Register5)

Table 92. PCS Register 5: 1000Base-X Auto-Negotiation Link Partner Ability

Bit	Name	Description	Type	Default
15	Next Page	1: Additional next pages exchange desired 0: No additional next pages exchange desired	RO	0x0
14	Reserved	Reserved	RO	0x0
13 : 12	Remote Fault	00: No error, link OK (default) 01: Link Failure 10: Offline 11: Auto-Negotiation Error	RO	0x0
11 : 9	Reserved	Reserved	RO	0x0
8 : 7	Pause ability	Bit8 : 1: Enable Asymmetric Pause 0: Disable Asymmetric Pause Bit7 : 1: Advertises that possesses 802.3x flow control capability 0: No flow control capability	RO	0x0
6	Half Duplex	1: Half Duplex capable 0: Not Half Duplex capable	RO	0x0

Bit	Name	Description	Type	Default
5	Full Duplex	1: Full Duplex capable 0: Not Full Duplex capable	RO	0x0
4 : 0	Reserved	Reserved	RO	0x0

4.8.6.PCS Register 6: 1000Base-X Auto-Negotiation Expansion (Page4 Register6)

Table 93. PCS 0~1 Register 6: 1000Base-X Auto-Negotiation Expansion

Bit	Name	Description	Type	Default
15:2	Reserved	Ignore On Read	RO	0x0
1	Page Received	1: A New Page has been received 0: A New Page has not been received	RO	0x0
0	Reserved	Ignore On Read	RO	0x0

4.8.7.PCS Register 7: 1000Base-X Auto-Negotiation Page Transmit Register (Page4 Register7)

Table 94. PCS Register 7: Auto-Negotiation Page Transmit Register

Bit	Name	Description	Type	Default
15	Next Page	1: Another next page desired 0: No other next page to send	RW	0x0
14	Acknowledge	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	RW	0x0
13	Message Page	1: Message page	RW	0x0
12	Acknowledge 2	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	RW	0x0
11	Toggle	Toggle Bit	RW	0x0
10:0	Message/Unformatted Field	Content of Message/Unformatted Page	RW	0x4

4.8.8.PCS Register 8:1000Base-X Auto-Negotiation Link Partner Next Page Register(Page4 Register8)

Table 95. PCS Register 8: Auto-Negotiation Link Partner Next Page Register

Bit	Name	Description	Type	Default
15	Next Page	Received Link Code Word Bit 15	RO	0x0
14	Acknowledge	Received Link Code Word Bit 14	RO	0x0
13	Message Page	Received Link Code Word Bit 13	RO	0x0
12	Acknowledge 2	Received Link Code Word Bit 12	RO	0x0
11	Toggle	Received Link Code Word Bit 11	RO	0x0
10:0	Message/Unformatted Field	Received Link Code Word Bit 10:0	RO	0x0

4.8.9. PCS Register 15: Extended Status(Page4 Register15)

Table 96. PCS Register 15: Extended Status

Bit	Name	Description	Type	Default
15	1000Base-X Full Duplex	1: 1000Base-X full duplex capable 0: Not 1000Base-X full duplex capable	RO	0x1
14	1000Base-X Half Duplex	1: 1000Base-X half duplex capable 0: Not 1000Base-X half duplex capable	RO	0x0
13	1000Base-T Full Duplex	1: 1000Base-T full duplex capable 0: Not 1000Base-T full duplex capable	RO	0x0
12	1000Base-T Half Duplex	1: 1000Base-T half duplex capable 0: Not 1000Base-T half duplex capable	RO	0x0
11:0	Reserved	Reserved	RO	0x0

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 97. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
DVDDIOM, DVDDIOLED, Supply Referenced to DGND.	GND-0.3	+3.63	V
DVDDIO, AVDDH_PHY, AVDDH_PLL, Supply Referenced to DGND, AGND_PHY and AGND_PLL.	GND-0.3	+1.957	V
DVDDL, SVDDL_TR, SVDDL_CK, AVDDL_PHY, AVDDL_PLL, Supply Referenced to DGND, SGND, AGND_PHY and AGND_PLL.	GND-0.3	+1.05	V

5.2. Recommended Operating Range

Table 98. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Storage Temperature	-45		125	°C
Ambient Operating Temperature (Ta)	0	-	70	°C
Operating Junction Temperature (Tj)	-	-	115	°C
AVDDH_PHY, AVDDH_PLL, DVDDIO Supply Voltage Range	1.843	1.9	1.957	V
AVDDL_PHY, AVDDL_PLL Supply, SVDDL_TR, SCDDL_CK Voltage Range	0.97	1.0	1.03	V
DVDDL Supply Voltage Range	0.97	1.0	1.03	V
DVDDIOLED Supply Voltage Range	3.3V	3.135	3.3	3.465
	2.5V	2.375	2.5	2.626
	1.9V	1.843	1.9	1.957
	1.8V	1.710	1.8	1.890
DVDDIOM Supply Voltage Range	3.3V	3.135	3.3	3.465
	2.5V	2.375	2.5	2.626
	1.9V	1.843	1.9	1.957
	1.8V	1.710	1.8	1.890
	1.2V	1.14	1.2	1.26

5.3. Thermal Characteristics

5.3.1. Assembly Description

Table 99. Assembly Description

Package	Type	MRQFN-119L
	Dimension (L×W)	10×10 mm ²
	Thickness	0.675 mm
PCB	PCB Dimension (L×W)	76.2×114.3 mm ²
	PCB Thickness	1.6 mm
	Number of Layer-PCB	Customized(6L)
Heat Sink	Size	25 x 25 x 25 mm ³

5.3.2. Simulation Conditions

Table 100. Simulation Conditions

Input Power	2.92W
Test Board (PCB)	Customized(6L)
Control Condition	Air Flow = 0, 1, 2 m/s

5.3.3. Thermal Performance of MRQFN-119L on PCB without External Heat Sink

Table 101. Thermal Performance of MRQFN-119L on PCB without External Heat Sink for Ta = 70°C

Air Flow Velocity	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
Still air	24.33	0.64	-
1m/s	21.04	0.78	-
2m/s	20.2	0.87	-

Note:

θ_{JA} : Junction to ambient thermal resistance

Ψ_{JT} : Junction to top center thermal characterization parameter

Ψ_{JB} : Junction to bottom surface center of PCB thermal characterization

Table 102. Thermal Performance of MRQFN-119L on PCB without External Heat Sink for Ta = 25°C

Package	°C/W)
θ_{JB}	10.28
θ_{JC}	10.46

Note:

θ_{JB} : Junction to board thermal resistance

θ_{JC} : Junction to case resistance

5.3.4. Thermal Performance of MRQFN-119L on PCB with 25 x 25 x 25 mm³ External Heat Sink

Table 103. Thermal Performance of MRQFN-119L on PCB with 25 x 25 x 25 mm³ External Heat Sink for Ta = 70°C

Air Flow Velocity	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
Still air	18.39	8.03	-
1m/s	13.12	9.12	-
2m/s	12.13	9.30	-

Note:

θ_{JA} : Junction to ambient thermal resistance

Ψ_{JT} : Junction to top center thermal characterization parameter

Ψ_{JB} : Junction to bottom surface center of PCB thermal characterization

5.4. DC Characteristics

Table 104. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
All UTP Ports Link/Active, with 6 LEDs/port					
Power Supply Current for DVDDL_AVDDL_PLL, AVDDL_PHY, SVDDL_TR, SVDDL_CK	I _{DVDDL} I _{AVDDL_PLL} I _{AVDDL_PHY} I _{SVDDL_CMU} I _{SVDDL_CK}	-	-	1.565	A
Power Supply Current for DVDDIO, AVDDH_PLL, AVDDH_PHY	I _{DVDDIO} I _{AVDDH_PLL} I _{AVDDH_PHY}	-	-	0.661	A
Power Supply Current for DVDDIOM(3.3V), DVDDIOLED(3.3V)	I _{DVDDIOM} I _{DVDDIOLED}	-	-	0.011	A
DVDDIOLED/DVDDIOM=3.3V					
CMOS Input High Voltage	V _{ih}	2.0	-	-	V
CMOS Input Low Voltage	V _{il}	-	-	0.75	V
Output High Voltage	V _{oh}	2.4	-	-	V
Output Low Voltage	V _{ol}	-	-	0.4	V
DVDDIOLED/DVDDIOM=2.5V					
CMOS Input High Voltage	V _{ih}	1.7	-	-	V
CMOS Input Low Voltage	V _{il}	-	-	0.7	V
Output High Voltage	V _{oh}	2.0	-	-	V
Output Low Voltage	V _{ol}	-	-	0.4	V
DVDDIO/DVDDIOLED/DVDDIOM=1.9V					
CMOS Input High Voltage	V _{ih}	1.2	-	-	V
CMOS Input Low Voltage	V _{il}	-	-	0.65	V
Output High Voltage	V _{oh}	1.45	-	-	V
Output Low Voltage	V _{ol}	-	-	0.45	V

DVDDIOLED/DVDDIOM=1.8V					
CMOS Input High Voltage	V _{ih}	1.1	-	-	V
CMOS Input Low Voltage	V _{il}	-	-	0.6	V
Output High Voltage	V _{oh}	1.35	-	-	V
Output Low Voltage	V _{ol}	-	-	0.45	V
DVDDIOM=1.2V					
CMOS Input High Voltage	V _{ih}	0.9	-	-	V
CMOS Input Low Voltage	V _{il}	-	-	0.4	V
Output High Voltage	V _{oh}	0.9	-	-	V
Output Low Voltage	V _{ol}	-	-	0.3	V

Note: Typical power consumption measure at T_j 70°C.

5.5. AC Characteristics

5.5.1. MDIO Slave Mode Timing Characteristics

MDIO must connect pull-up resistor on external circuit to assure during TA (Turnaround) and Idle state keep logic high. The range of R_P considering to Loading (PCB Trace & the number of IC) & Timing. The main purpose is if R_P too high so that RC charging timing is long, MDIO might hardly pull-high. Accord to the experience of IEEE 802.3 Clause 22, R_P is recommend 1K~1.5K ohm.

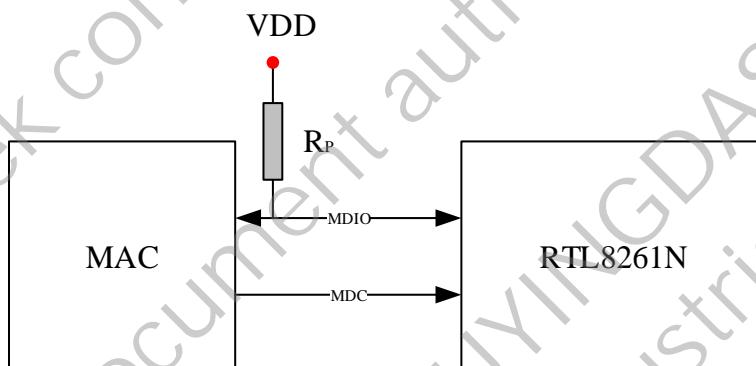


Figure 3. SMI (MDC/MDIO) External R_P circuit

According to IEEE802.3 standard, RTL8261N play as MDC/MDIO slave, no matter MDIO operate "Write/Read", slave always select clock posedge output data; select clock posedge sampling data, read/write timing specification as below..

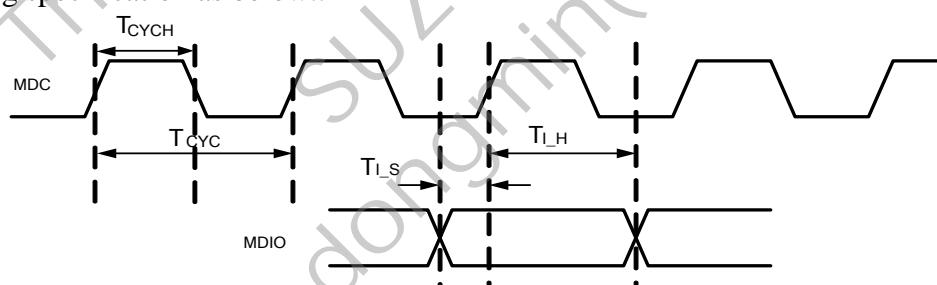
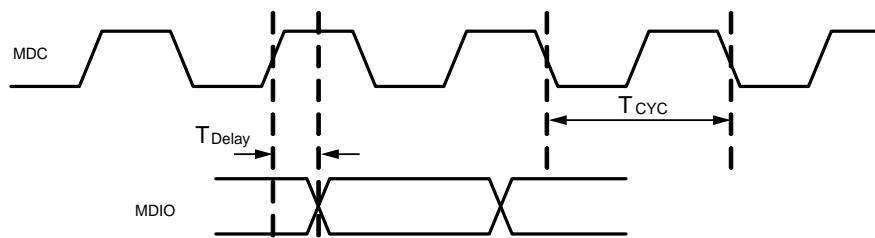


Figure 4. SMI Write Timing

Table 105. SMI Slave Input Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
MDC Clock input Cycle	T _{CYC}	MDC Clock input Cycle	40	-	-	ns
MDC duty cycle	T _{CYCH} / T _{CYC}	MDC duty cycle	30		70	%
MDIO to MDC Rising Input Setup Time	T _{I_S}	MDIO to MDC Rising Input Setup Time	10	-	-	ns
MDIO to MDC Rising Input Hold Time	T _{I_H}	MDIO to MDC Rising Input Hold Time	10	-	-	ns

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Figure 5. SMI Read Timing
Table 106. SMI Slave Output Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
Output delay	T_{Delay}	MDIO to MDC Rising Output Delay	0	-	30	ns

5.5.2. Clock Characteristics

Table 107. System Clock Characteristics

XTAL mode					
Symbol	Description	Min	Typical	Max	Units
FL	Frequency		50		MHz
-	Frequency Tolerance	-50	-	+50	ppm
TH/T	Duty Cycle	45	-	55	%
Rr	Equivalent Series Resistance	-	-	40	ohm
C0	Shunt Capacitance			3	pF
V _{IH}	Input-High Voltage	0.8	-	-	V
V _{IL}	Input-Low Voltage	-	-	0.2	V
Single-ended mode					
Symbol	Description	Min	Typical	Max	Units
FL	Frequency		50		MHz
-	Frequency Tolerance	-50	-	+50	ppm
TH/T	Duty Cycle	45	-	55	%
Tr	Rise Time(10%-90%)	-	-	3	ns
Tf	Fall Time(90%-10%)	-	-	3	ns
-	Input Voltage	GND - 0.1	-	AVDDL_PLL + 0.1	V
V _{IH}	Input-High Voltage	0.8	-	-	V
V _{IL}	Input-Low Voltage	-	-	0.2	V
LVDS mode(differential)					
Symbol	Description	Min	Typical	Max	Units
V _{p-p}	Voltage peak to peak	0.6		1.2	V
FL	Frequency		50		MHz
-	Frequency Tolerance	-50	-	+50	ppm
Tr	Rise Time(10%-90%)	-	-	3	ns
Tf	Fall Time(90%-10%)	-	-	3	ns
TH/T	Duty Cycle	45	-	55	%

Note: All clock parts , need meet as below CLK performance SPEC.

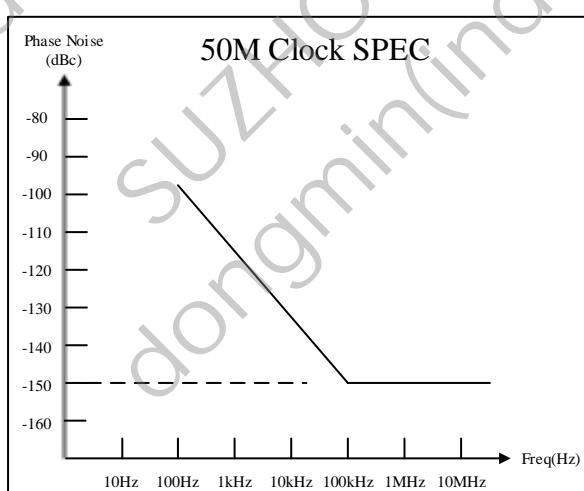


Figure 6. Clock Performance SPEC

5.6. Power and Reset Characteristics

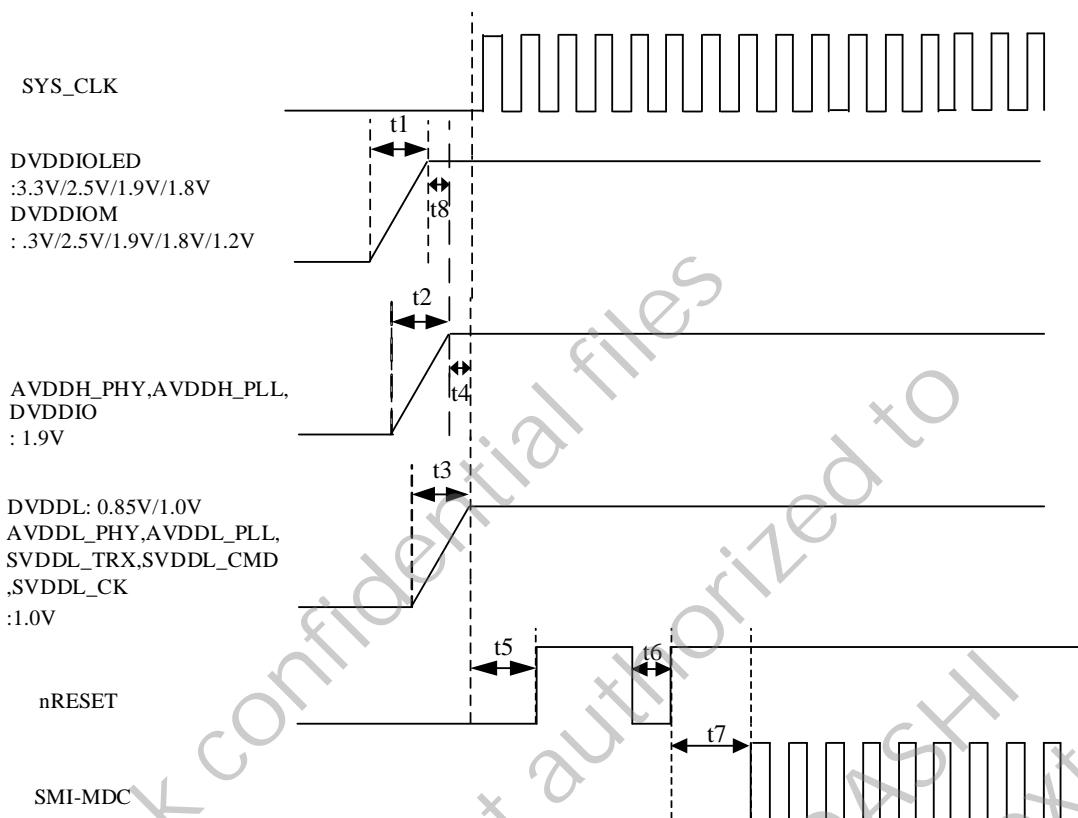


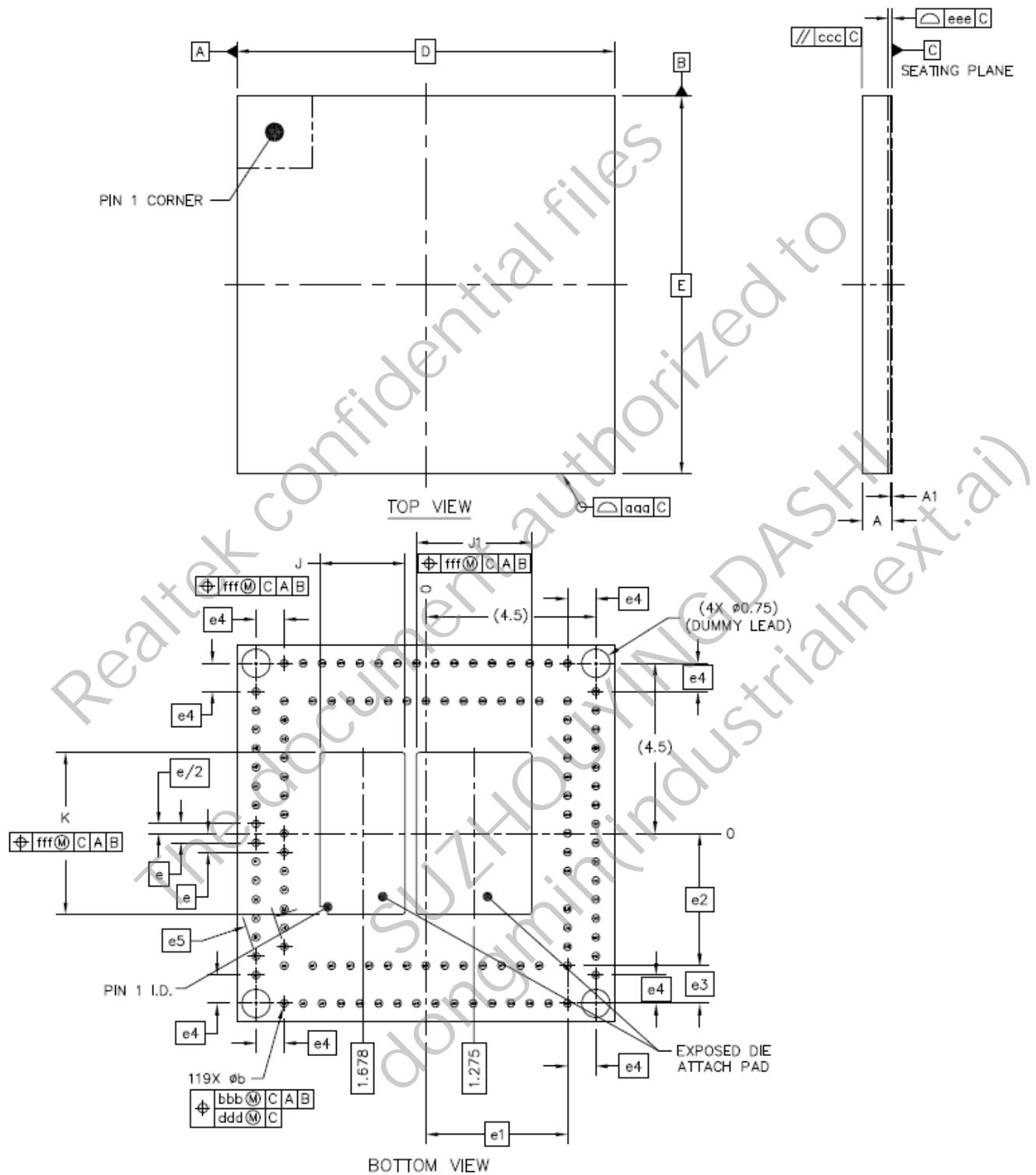
Figure 7. Power and Reset Characteristics

Table 108. Power and Reset Timing Requirements

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
DVDDH	t1	DVDDIOLED, DVDDIOM power rise time. (10% ~90%)	I	0.1		10	ms
AVDDH	t2	AVDDH_PHY, AVDDH_PLL and DVDDIO power rise time. (10% ~90%)	I	0.1		10	ms
DVDDL	t3	DVDDL, AVDDL_PHY, AVDDL_PLL, SVDDL_TR and SVDDL_CK power rise time. (10% ~90%)	I	0.1		10	ms
HV_LV_Sequence	t4	AVDDH between DVDDL Power on Sequence	I	1			us
Reset Delay Time	t5	The duration from all power steady to the reset signal released to high	I	1			ms
Reset Low Time	t6	The duration of reset signal remaining low time before issuing a reset to the RTL8261N	I	40			ns
SMI-ready	t7	SMI-ready use after nRESET release.	I	150			ms
DHV_LV_Sequence	t8	Power on Sequence between AVDDH and DVDDH(LED&IOM)	I	0			ms

6. Mechanical Dimensions

MR Plastic Quad Flat Package 119 Leads 10x10mm² Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.85	-	-	0.003
A ₁	0.02	0.05	0.08	0.00078	0.0019	0.0031
b	0.15	0.2	0.25	0.0059	0.0078	0.0098
D	10 REF			0.393 REF		
E	10 REF			0.393 REF		
e	0.5 BSC			0.0196 BSC		
e ₁	3.75 BSC			0.1476 BSC		
e ₂	3.5 BSC			0.1378 BSC		
e ₃	1.0 BSC			0.0393 BSC		
e ₄	0.75 BSC			0.0295 BSC		
e ₅	0.791 BSC			0.0311 BSC		
J	2.15	2.25	2.35	0.0846	0.0886	0.093
J ₁	2.955	3.055	3.155	0.1163	0.1203	0.1242
K	4.188	4.288	4.388	0.1649	0.1688	0.1728
aaa	0.1			0.0039		
bbb	0.1			0.0039		
ddd	0.05			0.00197		
ccc	0.1			0.0039		
eee	0.1			0.0039		
fff	0.1			0.0039		

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENTL: JEDEC MO-220.

7. Package Identification and Ordering Information

7.1. Package Identification

Part number is indicated by RTL8261N

Green package and Date code are indicated by the ‘G’ and “XXX”.



7.2. Ordering Information

Table 109. Ordering Information

Part Number	Package	Status
RTL8261N-CG	MRQFN-119L (10mm*10mm)	-

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