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RTL8103E-GR
RTL8103EL-GR
RTL8103E-VB-GR
RTL8103EL-VB-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/05/28	First release.
1.1	2008/07/08	Corrected typing error.
1.2	2008/07/29	Updated licensing information.
1.3	2008/08/08	Added Deep Slumber Mode (DSM) power saving to features list on page 3.
1.4	2009/02/18	Corrected typing errors.
1.5	2009/04/10	Added RTL8103E-VB-GR and RTL8103EL-VB-GR part numbers. Revised Deep Slumber Mode (DSM) Feature on page 3. Added section 6.2.6 Deep Slumber Mode (DSM) V1 & V2, page 14.
1.6	2009/06/30	Revised section 6.2.5 Customizable LED Configuration, page 13. Revised section 8.2 RTL8103EL (48-Pin LQFP), page 31. Revised section 8.3 Mechanical Dimensions Notes (RTL8103EL 48-Pin), page 31.
1.7	2009/09/18	Revised section 6.2.5 Customizable LED Configuration, page 13. Revised Table 14 Absolute Maximum Ratings, page 20. Revised Table 15 Recommended Operating Conditions, page 20. Revised Table 18 Oscillator Requirements, page 21. Revised Table 20 DC Characteristics, page 22.
1.8	2010/02/05	Revised V_{NOISE} parameter, Table 24 REFCLK Parameters, page 26.
1.9	2010/07/30	Added RTL8103EL-VB-CG part number.
1.91	2010/09/24	Revised model numbering. Revised Table 8 Power and Ground, page 8.

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1. General Description

The Realtek RTL8103E(L)/RTL8103E(L)-VB Fast Ethernet controller combines an IEEE 802.3 10/100Base-T compliant Media Access Controller (MAC), PCI Express bus controller, and embedded One-Time-Programmable (OTP) memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8103E(L)/RTL8103E(L)-VB offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8103E(L)/RTL8103E(L)-VB features embedded One-Time-Programmable (OTP) memory to replace the external EEPROM (93C46/93C56/93C66).

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™ and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8103E(L) /RTL8103E(L)-VB.

The RTL8103E(L)/RTL8103E(L)-VB is fully compliant with Microsoft® NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8103E(L)/RTL8103E(L)-VB supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. The device

embeds an adaptive equalizer in the PCIE PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 20 inches.

The RTL8103E(L)/RTL8103E(L)-VB is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

Built-in linear regulators provide the RTL8103E(L)/RTL8103E(L)-VB's core power, as well as reducing layout area and external BOM costs. The RTL8103E/RTL8103E(L)-VB supports the Deep Slumber Mode (DSM) power saving V1/V2 feature. See the separate DSM application notes for details (the RTL8103EL does not support the DSM feature).

Note: RTL8103 model differences are listed in section 9 Ordering Information, page 32.

2. Features

- Integrated 10/100 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Customizable LEDs
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully complies with IEEE 802.3, IEEE 802.3u
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- Embedded OTP memory can replace the external EEPROM
- Transmit/Receive on-chip buffer support
- Supports power down/link down power saving
- Built-in Regulator
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports Receive-Side Scaling (RSS)
- Embeds an adaptive equalizer in PCI Express PHY (PCB traces can reach up to 20 inches)
- Supports Deep Slumber Mode (DSM) power saving V1/V2 features (V1 for RTL8103E (QFN64), and V2 for RTL8103E(L)-VB only)
- 64-pin QFN (RTL8103E) & 48-pin LQFP (RTL8103EL) Green package

3. System Applications

- PCI Express Fast Ethernet on Motherboard, Notebook, or Embedded system

4. Pin Assignments

4.1. RTL8103E (64-Pin)

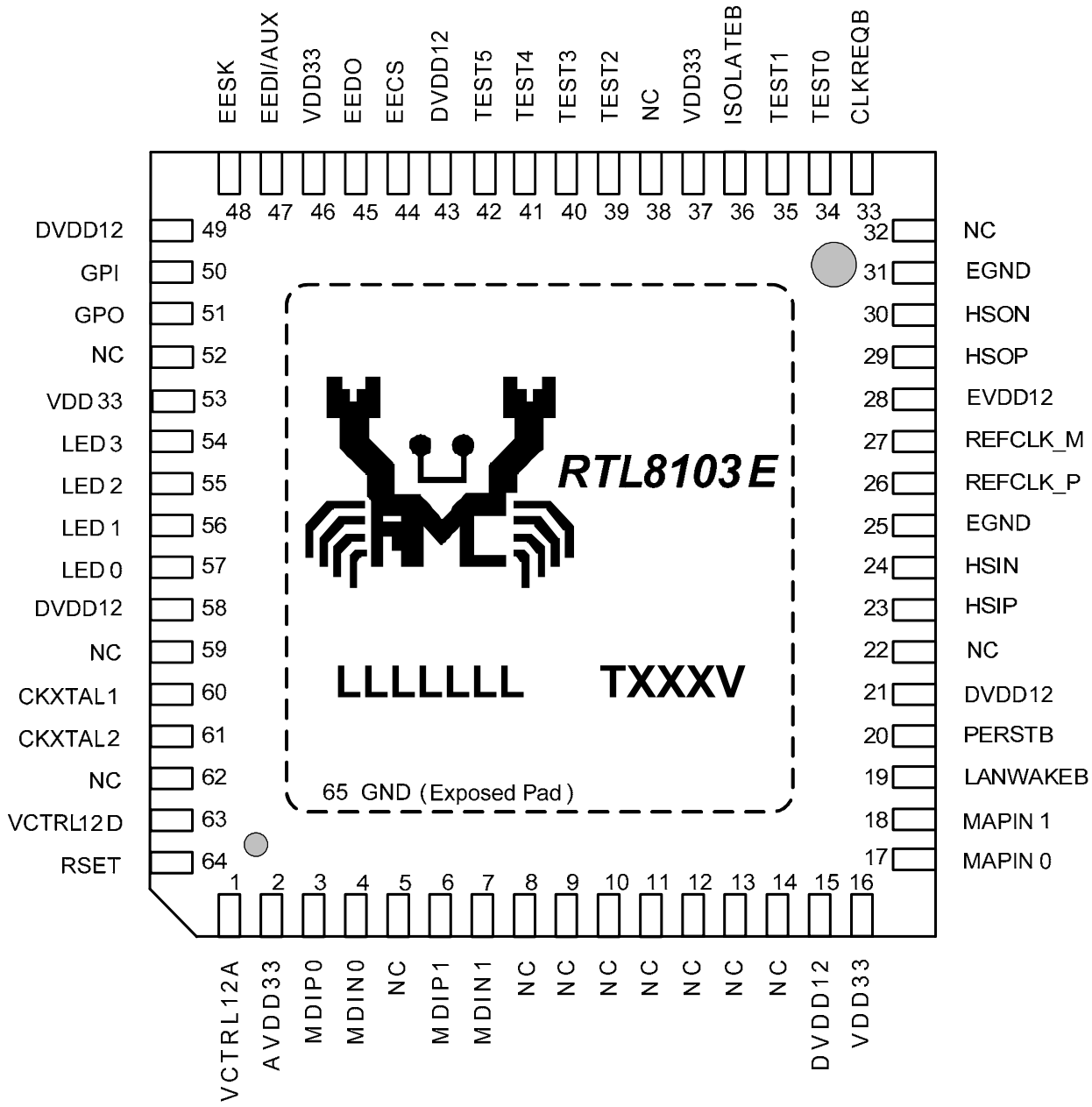


Figure 1. Pin Assignments (RTL8103E 64-Pin)

4.2. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 1. The version is shown in the location marked 'V'.

4.3. RTL8103EL (48-Pin)

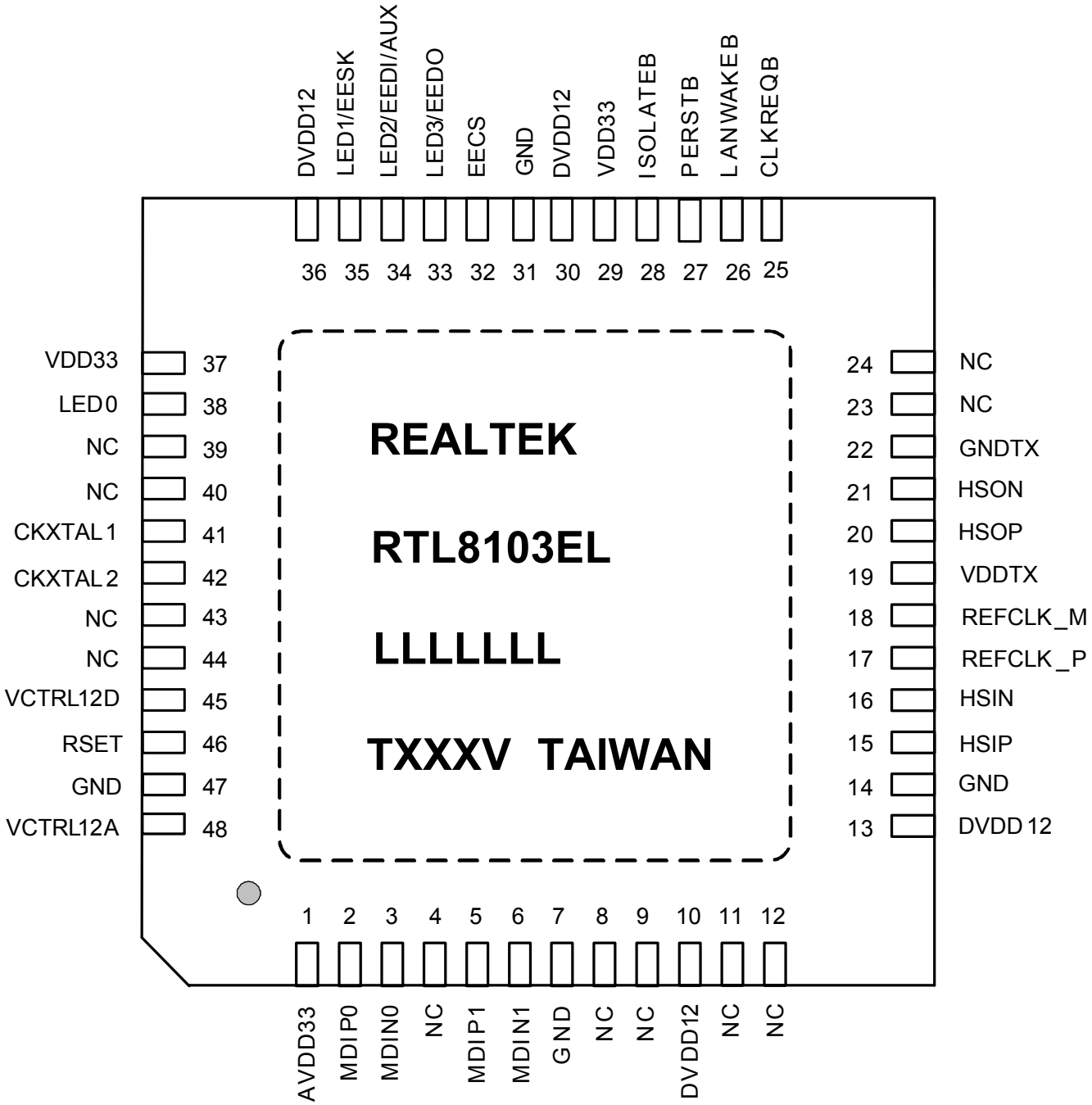


Figure 2. Pin Assignments (RTL8103EL 48-Pin)

4.4. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The version is shown in the location marked 'V'.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State bi-directional input/output pin	P:	Power

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LANWAKEB	O/D	19	26	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	36	28	Isolate Pin: Active low. Used to isolate the RTL8103E(L) from the PCI Express bus. The RTL8103E(L) will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
REFCLK_P	I	26	17	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_M	I	27	18	
HSOP	O	29	20	PCI Express Transmit Differential Pair.
HSON	O	30	21	
HSIP	I	23	15	PCI Express Receive Differential Pair.
HSIN	I	24	16	
PERSTB	I	20	27	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8103E(L) returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	33	25	Reference Clock Request Signal. This signal is used by the RTL8103E(L) to request starting of the PCI Express reference clock.

5.3. EEPROM

Table 3. EEPROM

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
EESK	O	48	35	Serial Data Clock.
EEDI/AUX	OI	47	34	EEDI: Output to serial data input pin of EEPROM. AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8103E(L) assumes that no Aux. Power exists.
EEDO	I	45	33	Input from Serial Data Output Pin of EEPROM.
EECS	O	44	32	EECS: EEPROM chip select.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
MDIP0	IO	3	2	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	4	3	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	6	5	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	7	6	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
CKXTAL1	I	60	41	Input of 25MHz Clock Reference.
CKXTAL2	O	61	42	Output of 25MHz Clock Reference.

5.6. Regulator and Reference

Table 6. Regulator and Reference

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
RSET	I	64	46	Reference. External resistor reference.

5.7. LEDs

Table 7. LEDs

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	RX	LINK10
LED3	NA	NA	NA	NA

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the EEPROM.
If there is no EEPROM, the default value of the (LEDS1, LEDS0) = (0, 0).

5.8. Power and Ground

Table 8. Power and Ground

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
VDD33	P	16, 37, 46, 53	29, 37	Digital 3.3V Power Supply.
AVDD33	P	2	1	Analog 3.3V Power Supply.
DVDD12	P	15, 21, 43, 49, 58	10, 13, 30, 36	Digital 1.2V Power Supply.
VCTRL12D	O	63	45	1.2V Output Supplies Power to DVDD12 Power Pin.
VCTRL12A	O	1	48	1.2V Output.
EVDD12	O	28	-	1.2V Output.
VDDTX	O	-	19	1.2V Output.
GNDTX	P	-	22	Analog Ground.
EGND	P	25, 31	-	Analog Ground.
GND	P	-	7, 14, 31, 47	Ground.
GND	P	65	-	Ground (Exposed Pad).

Note: Refer to the most updated schematic circuit for correct configuration.

5.9. GPIO

Table 9. GPIO Pins

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
GPI	I	50	-	Input GPIO Pin.
GPO	O	51	-	Output GPIO Pin. This pin reflects the link up or link down state. High: Link up Low: Link down

5.10. NC (Not Connected) Pins and Test Pins

Table 10. NC (Not Connected) Pins and Test Pins

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
NC	-	5, 8, 9, 10, 11, 12, 13, 14, 22, 32, 38, 52, 59, 62	4, 8, 9, 11, 12, 23, 24, 39, 40, 43, 44	Not Connected.
MAPIN0	IO	17	-	Realtek Internal Use Only.
MAPIN1	IO	18	-	Realtek Internal Use Only.
TEST0	-	34	-	Realtek Internal Use Only.
TEST1	-	35	-	Realtek Internal Use Only.
TEST2	-	39	-	Realtek Internal Use Only.
TEST3	-	40	-	Realtek Internal Use Only.
TEST4	-	41	-	Realtek Internal Use Only.
TEST5	-	42	-	Realtek Internal Use Only.

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8103E(L) complies with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8103E(L) supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported.

6.1.1. PCI Express Transmitter

The RTL8103E(L)'s PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8103E(L)'s PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8103E(L)'s internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8103E(L) supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, or LINK10/100. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. RX LED

In 10/100Mbps mode, blinking of the RX LED indicates that receive activity is occurring.

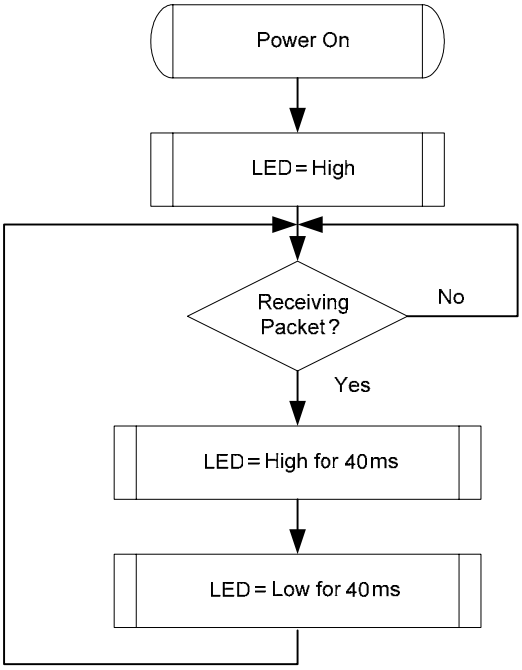


Figure 3. RX LED

6.2.3. TX LED

In 10/100Mbps mode, blinking of the TX LED indicates that transmit activity is occurring.

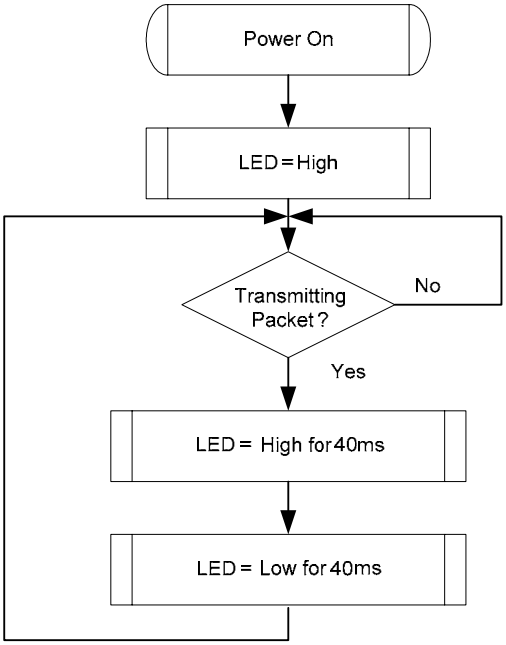


Figure 4. TX LED

6.2.4. TX/RX LED

In 10/100Mbps mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

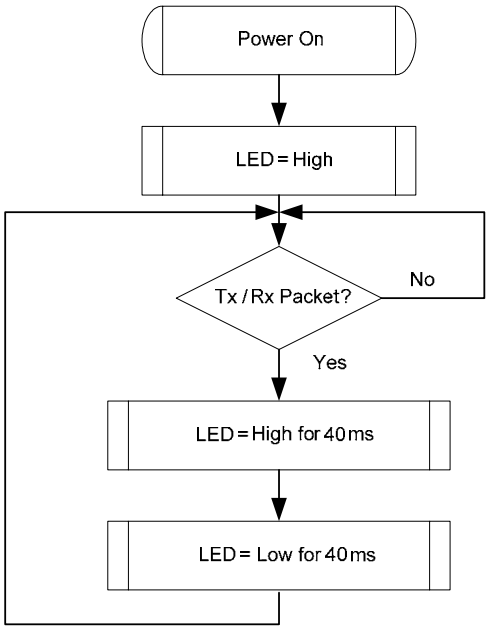


Figure 5. TX/RX LED

6.2.5. Customizable LED Configuration

The RTL8103E(L) supports customizable LED operation modes via IO register offset 18h~19h. Table 11 describes the different LED actions.

Table 11. LED Select (IO Register Offset 18h~19h)

Bit	Symbol	RW	Description
15:12	LEDSEL3	RW	LED Select for PINLED3
11:8	LEDSEL2	RW	LED Select for PINLED2
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

1. Set IO register offset 0x50 bit 7 and bit 6 to 11'b to enable the MAC config register write enable.
2. Set IO register offset 0x55 bit 6 to 1b to enable the customized LED function.
3. Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0xA821h (1010100000100001b), the LED actions are:

- LED 0: On only in 10M mode, with no blinking during TX/RX
- LED 1: On only in 100M mode, with no blinking during TX/RX
- LED 2: Blinks on TX/RX (all modes)
- LED 3: On only in 100M mode. Blinks on 100M mode TX/RX

Table 12. Customized LEDs

	LINK			ACT
Speed	Link 10M	Link100M	Not Defined	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 2	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	LED Blinks when Transmitting or Receiving
LINK>0	LED On when Selected Speed is Linked	LED Blinks when Selected Speed TX/RX

Note1: ACT means blinking TX and RX. LINK indicates Link 10M and Link 100M.
Note2: There are two special modes:
Mode A: LED OFF Mode → Set all bits to 0.
Mode B: Full Duplex Mode → Set LED 0=0, and either LED 1, LED 2, or LED 3 >0.
LED 0 = On in Full Duplex Mode.
LED 1 = Follow Customized LED rule.
LED 2 = Follow Customized LED rule.
LED 3= Follow Customized LED rule.

6.2.6. Deep Slumber Mode (DSM) V1 & V2

The RTL8103E/RTL8103E(L)-VB supports Link Down power saving mode via communication with the BIOS and external circuitry. Note that DSMv2 is a simplified implementation of DSMv1, and is only supported in the RTL8103E(L)-VB. Refer to the separate DSM application note for details (the RTL8103EL does not support the DSM feature).

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8103E(L) operates at 10/100Mbps over standard CAT.5 UTP cable (100Mbps), and CAT.3 UTP cable (10Mbps).

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.4. EEPROM Interface

The RTL8103E(L) can use internal eFUSE memory or an external EEPROM. The 93C46/93C56/93C66 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8103E(L) to read from, and write data to, an external serial EEPROM device.

Note: The RTL8103EL only supports 93C46 EEPROM.

Values in the internal eFUSE memory or external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8103E(L) will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8103E(L) initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The interface consists of EESK, EECS, EEDO, and EEDI.

The correct EEPROM (i.e., 93C46/93C56/93C66) must be used in order to ensure proper LAN function.

Table 13. EEPROM Interface

EEPROM	Description
EECS	93C46/93C56/93C66 Chip Select.
EESK	EEPROM Serial Data Clock.
EEDI/Aux	Input data bus/Input pin to detect whether Aux. Power exists on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8103E(L) assumes that no Aux. Power exists.
EEDO	Output Data Bus.

6.5. Power Management

The RTL8103E(L) is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8103E(L) can monitor the network for a Wakeup Frame, a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or LANWAKEB pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs.

When the RTL8103E(L) is in power down mode (D1 ~ D3):

- The RX state machine is stopped. The RTL8103E(L) monitors the network for wakeup events such as a Magic Packet and Wakeup Frame in order to wake up the system. When in power down mode, the RTL8103E(L) will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8103E(L).
- Transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held.
- After being restored to D0 state, the RTL8103E(L) transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 FF, then PCI PMC = C3 FF)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 FF, then PCI PMC = 03 7E)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C3 FF (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 7F, then PCI PMC = C3 7F)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 7F, then PCI PMC = 03 7E)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 7E.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8103E(L), e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8103E(L) adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8103E(L), e.g., a broadcast, multicast, or unicast address to the current RTL8103E(L) adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8103E(L) is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8103E(L) supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding wake-up method (message, beacon, or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8103E(L) may assert the corresponding wake-up method (message, beacon, or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8103E(L) to stop asserting the corresponding wake-up method (message, beacon, or LANWAKEB) (if enabled).

When the RTL8103E(L) is in power down mode, e.g., D1~D3, the IO and MEM accesses to the RTL8103E(L) are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was D3cold. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.6. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8103E(L)'s PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56/93C66 has completed or not.

Note: The RTL8103EL only supports 93C46 EEPROM.

Write VPD register: (write data to the 93C46/93C56/93C66)
Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8103E(L), the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46/93C56/93C66)
Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8103E(L), the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.3 Specifications for further information.
Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.
Note3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.
Note4: The VPD function of the RTL8103E is designed to be able to access the full range of the 93C46/93C56/93C66 EEPROM, however, the RTL8103EL only supports the 93C46 EEPROM.

6.7. Receive-Side Scaling (RSS)

The RTL8103E(L) is compliant with the Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi-CPU platforms.

6.7.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8103E(L) to store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port.
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address (Note: The RTL8103E(L) does not support the IPv6 extension header hash type in RSS).

Hash Bits

Hash bits are used to index the hash result into the indirection table.

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.7.2. RSS Operation

After the parameters are set, the RTL8103E(L) will start hash calculation on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8103E(L) uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

7. Characteristics

7.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 14. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.3	+0.3	V
DVDD12	Supply Voltage 1.2V	-0.12	+0.12	V
DCinput	Input Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

7.2. Recommended Operating Conditions

Table 15. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD33, AVDD33	3.0	3.3	3.6	V
	DVDD12	1.08	1.2	1.32	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

7.3. Crystal Requirements

Table 16. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a = 0°C~+70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a = 25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.5	mW

7.4. Transformer Characteristics

Table 17. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1
Inductance (min.)	350µH @ 8mA	350µH @ 8mA

7.5. Oscillator Requirements

Table 18. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter [1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

7.6. Thermal Characteristics

Table 19. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

7.7. DC Characteristics

Table 20. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	3.0	3.3	3.6	V
DVDD12	1.2V Supply Voltage	-	1.08	1.2	1.32	V
Voh	Minimum High Level Output Voltage	Ioh = -4mA	0.9*VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	-	0.1*VDD33	V
Vih	Minimum High Level Input Voltage	-	1.8	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc33	Maximum Operating Supply Current from 3.3V	-	-	-	201	mA
Icc12	Maximum Operating Supply Current from 1.2V	-	-	-	127	mA

Note: Refer to the most updated schematic circuit for correct configuration.

7.8. AC Characteristics

7.8.1. Serial EEPROM Interface Timing

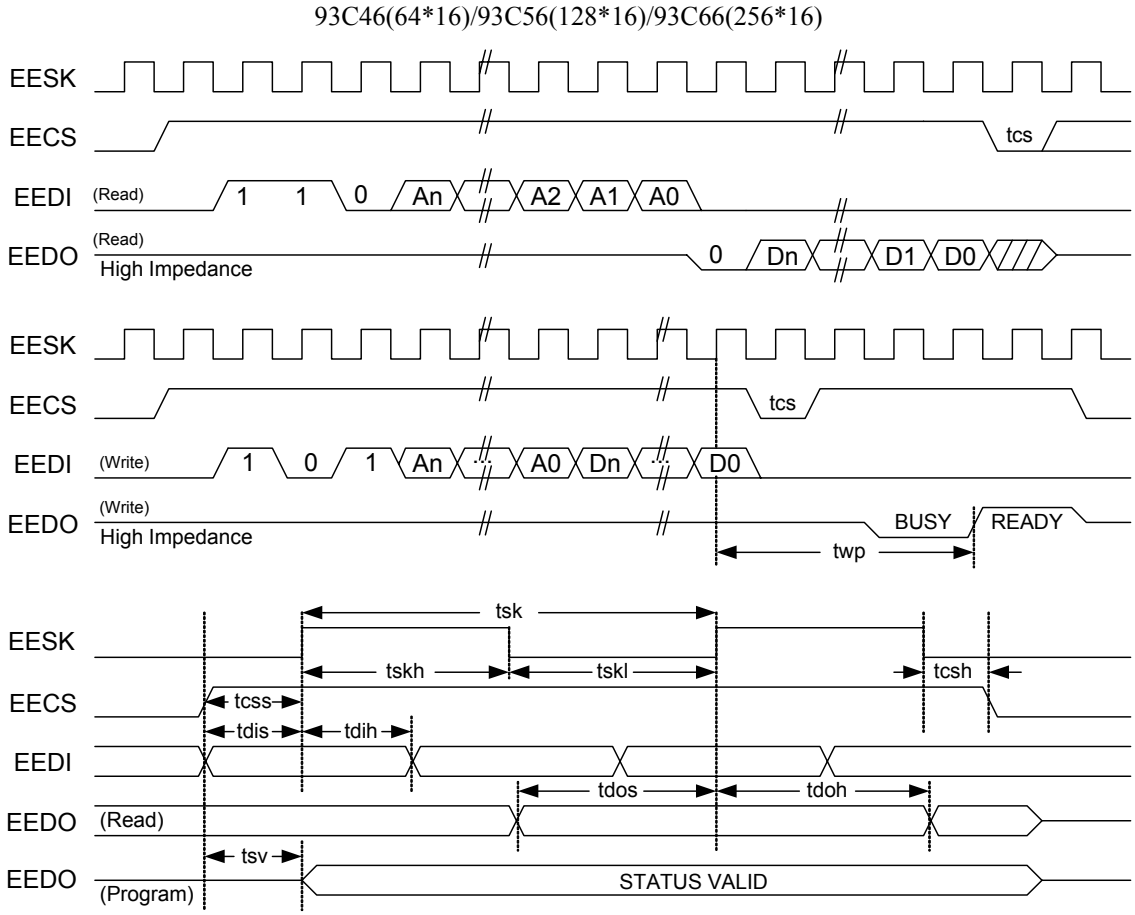


Figure 6. Serial EEPROM Interface Timing

Table 21. EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346/93C56/93C66	1000	-	ns
twp	Write Cycle Time	9346/93C56/93C66	-	10	ms
tsk	SK Clock Cycle Time	9346/93C56/93C66	4	-	µs
tskh	SK High Time	9346/93C56/93C66	1000	-	ns
tskl	SK Low Time	9346/93C56/93C66	1000	-	ns
tcss	CS Setup Time	9346/93C56/93C66	200	-	ns
tcsh	CS Hold Time	9346/93C56/93C66	0	-	ns
tdis	DI Setup Time	9346/93C56/93C66	400	-	ns
tdih	DI Hold Time	9346/93C56/93C66	400	-	ns
tdos	DO Setup Time	9346/93C56/93C66	2000	-	ns
tdoh	DO Hold Time	9346/93C56/93C66	-	2000	ns
tsv	CS to Status Valid	9346/93C56/93C66	-	1000	ns

7.9. PCI Express Bus Parameters

7.9.1. Differential Transmitter Parameters

Table 22. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median And Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-Acp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle after Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications after Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The +/-300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

7.9.2. Differential Receiver Parameters

Table 23. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-Acp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

7.9.3. REFCLK Parameters

Table 24. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Max Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Min Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input Min	100MHz Input Max	Units	Note
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11
V_{NOISE}	Common Mode Noise Allowed	-	+50	mV	-

Note1: Measurement taken from single ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 10, page 28.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 7, page 27.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 7, page 27.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 9, page 27.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 7, page 27.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 7, page 27.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 7, page 27.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 13, page 29. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 12, page 28.

*Note13: ppm refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8, page 27.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

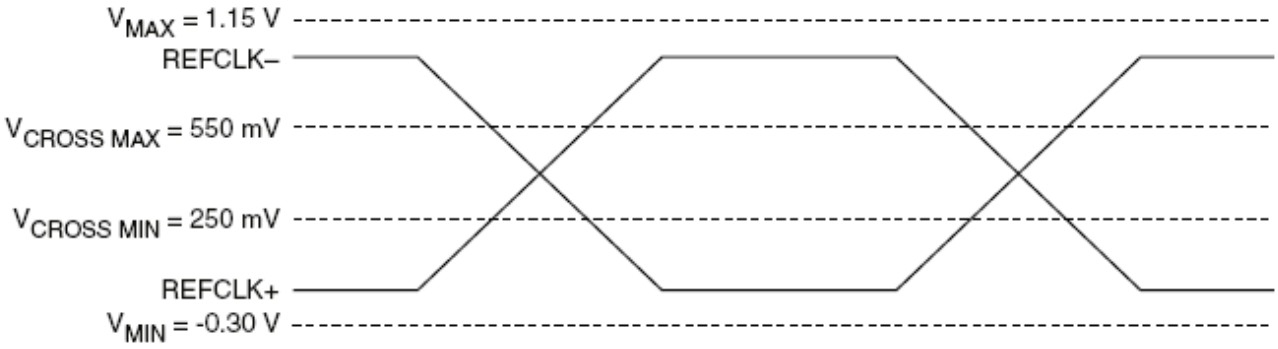


Figure 7. Single-Ended Measurement Points for Absolute Cross Point and Swing

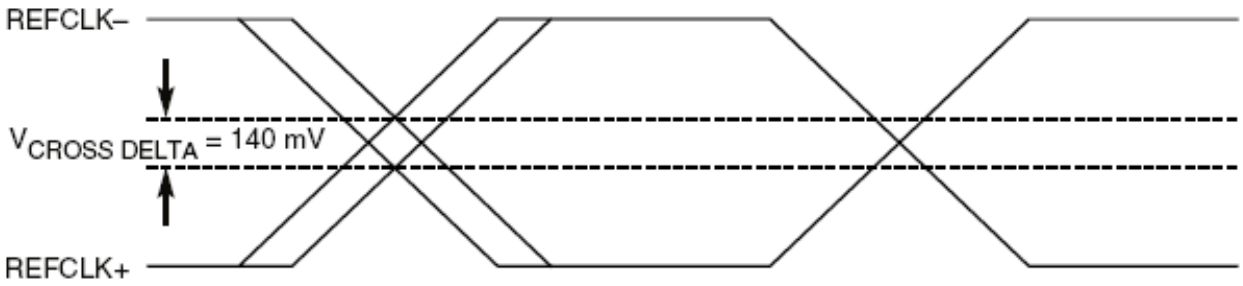


Figure 8. Single-Ended Measurement Points for Delta Cross Point

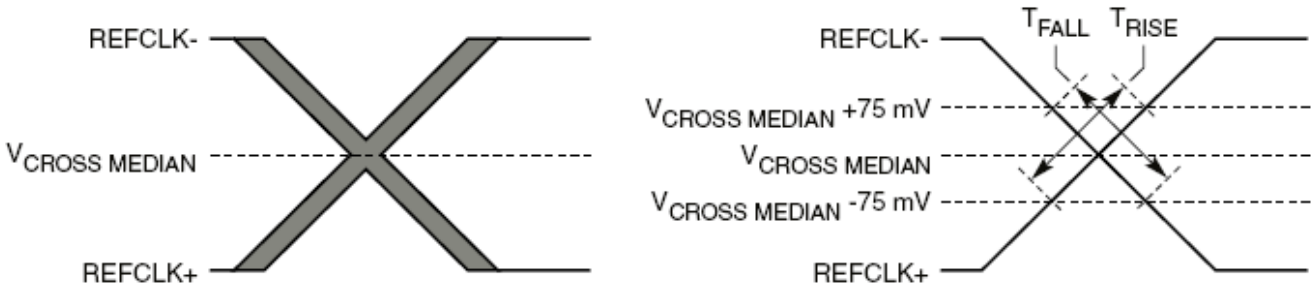


Figure 9. Single-Ended Measurement Points for Rise and Fall Time Matching

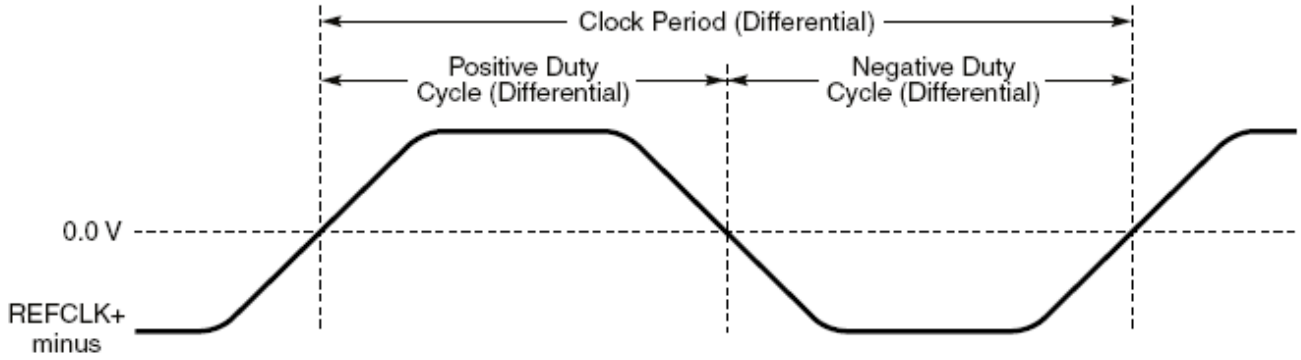


Figure 10. Differential Measurement Points for Duty Cycle and Period

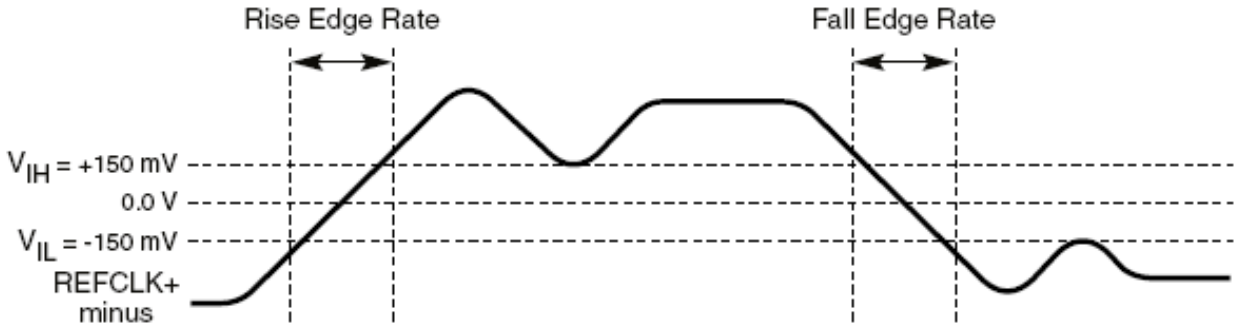


Figure 11. Differential Measurement Points for Rise and Fall Time

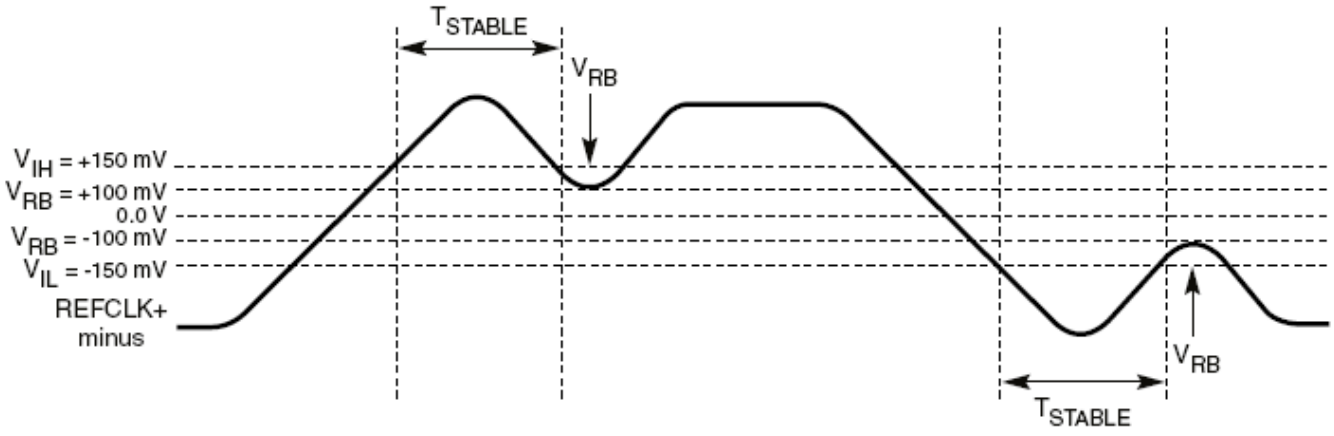


Figure 12. Differential Measurement Points for Ringback

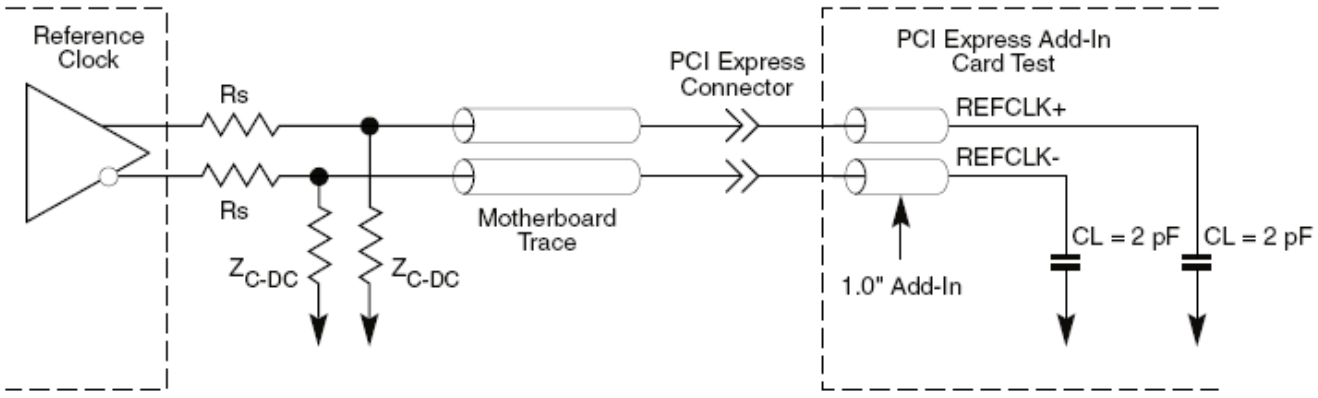


Figure 13. Reference Clock System Measurement Point and Loading

7.9.4. Auxiliary Signal Timing Parameters

Table 25. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
T_{FAIL}	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{WKRF}	LANWAKEB Rise – Fall Time	-	100	ns

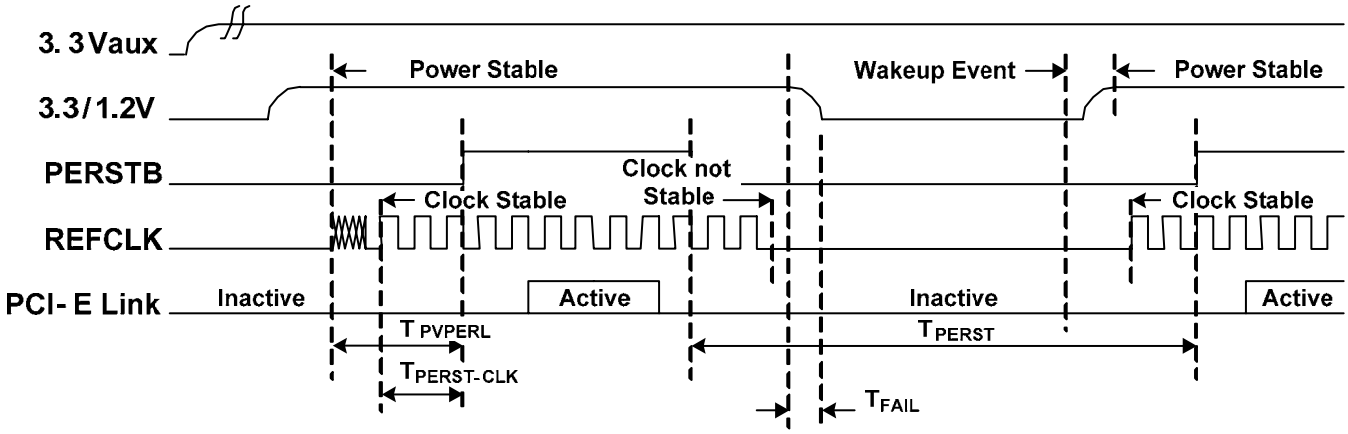
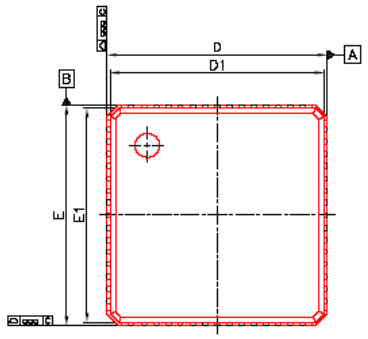
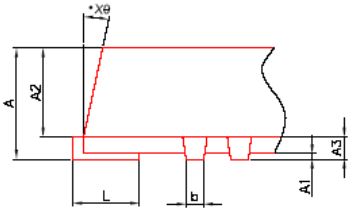


Figure 14. Auxiliary Signal Timing

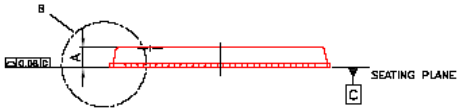
8. Mechanical Dimensions

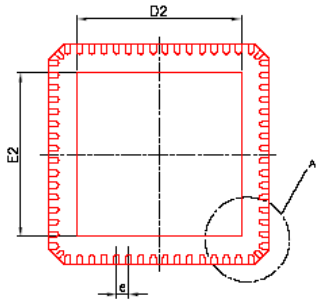
8.1. RTL8103E (64-Pin QFN)

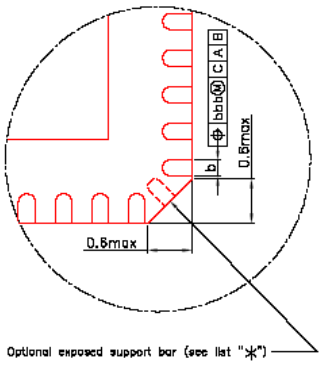




DETAIL : B







DETAIL : A

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3		0.20 REF			0.008 REF	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		9.00 BSC			0.354 BSC	
D1		8.75 BSC			0.344 BSC	
E		9.00 BSC			0.354 BSC	
E1		8.75 BSC			0.344 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table							
L/F	D2 (mm)			E2 (mm)			*
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.79	3.94	NO

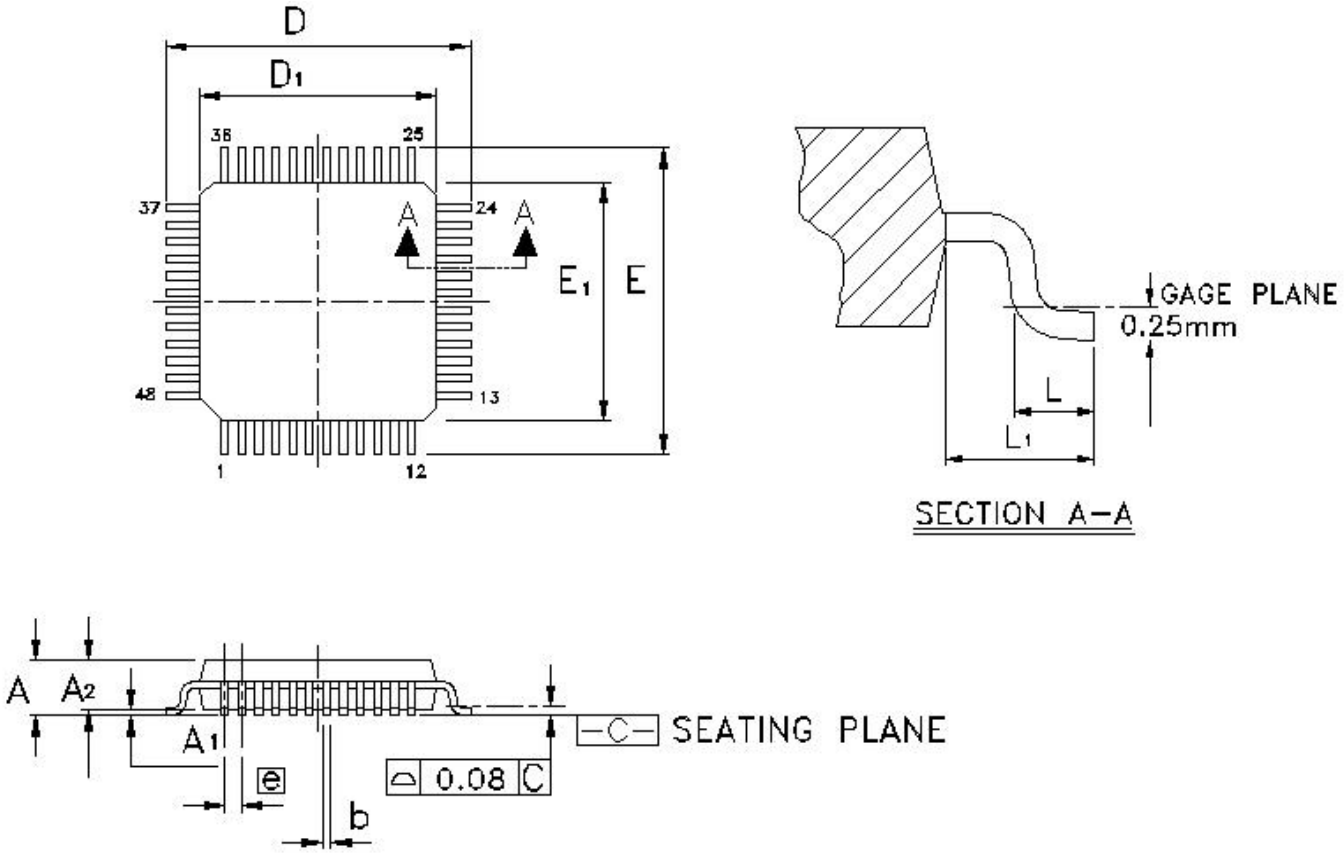
NOTE: The RTL8103E exposed pad size is type 3.

OVER MOLD

TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chen	DWG NO.	CE064-SW1
ENG.	C.Y.Horng	REV NO.	C
QM.	S.T.Liao	PRODUCT CODE	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02
DWG.	R.K.Wang	SHT No.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

COPY CONTROLLED	REV NO	DESCRIPTION	DATE
	C	Add Exposed Pad Size & Support bar table	06/17/02

8.2. RTL8103EL (48-Pin LQFP)



8.3. Mechanical Dimensions Notes (RTL8103EL 48-Pin)

Symbol	Dimension in Inchs			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.063	-	-	1.60
A1	0.002	0.004	0.006	0.00	0.1	0.15
A2	0.053	0.055	0.057	1.30	1.40	1.45
b	0.007	0.009	0.011	0.15	0.22	0.27
D/E	0.354 BSC			9.00 BSC		
D1/E1	0.276 BSC			7.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-026.

9. Ordering Information

Table 26. Ordering Information

Part Number	Package	Status
RTL8103E-GR	64-Pin QFN 'Green' Package with Au Bonding	Mass Production
RTL8103EL-GR	48-Pin LQFP 'Green' Package with Au Bonding	Mass Production
RTL8103E-VB-GR	64-Pin QFN 'Green' Package with Au Bonding; Version B Silicon	Mass Production
RTL8103EL-VB-GR	48-Pin LQFP 'Green' Package with Au Bonding; Version B Silicon	Mass Production

Note: See page 4 and page 5 for package identification information.

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