

[下载](#)[打印](#)

26

/ 27 >

[视图](#)[标记](#)[批注](#)[全文...](#)

格式: PDF | 页数: 27 | 上传日期: 2022-01-08 17:58:59 | 浏览次数: 1000+ | 下载积分: 270 | 加入阅读清单





NOT FOR PUBLIC RELEASE

RTL8238B-VB-GR

**HIGHLY INTEGRATED OCTAL POWER
SOURCING EQUIPMENT CONTROLLER**

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.0
30 June 2021
Track ID: JATR-8275-15



Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com





COPYRIGHT

©2021 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

DISCLAIMER

Realtek provides this document ‘as is’, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

LICENSE

This product is covered by one or more of the following patents: US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

| Revision | Release Date | Summary |
|----------|--------------|----------------|
| 1.0 | 2021/06/30 | First release. |



Table of Contents

| | |
|--|----|
| 1. GENERAL DESCRIPTION | 1 |
| 2. FEATURES | 2 |
| 3. SYSTEM APPLICATIONS | 3 |
| 3.1. MANAGEMENT PSE APPLICATION | 3 |
| 3.2. DUMB PSE APPLICATION | 3 |
| 4. BLOCK DIAGRAM | 4 |
| 5. PIN ASSIGNMENTS | 5 |
| 5.1. PACKAGE IDENTIFICATION | 5 |
| 5.2. PIN ASSIGNMENTS TABLE | 6 |
| 6. PIN DESCRIPTIONS | 8 |
| 6.1. POWER INTERFACE CONNECTION PINS | 8 |
| 6.2. I2C SLAVE PINS | 8 |
| 6.3. I2C MASTER PINS | 8 |
| 6.4. GPIO PINS | 8 |
| 6.5. CONFIGURATION PINS | 9 |
| 6.6. POWER AND GROUND PINS | 9 |
| 6.7. MISCELLANEOUS PINS | 10 |
| 7. FUNCTION DESCRIPTION | 11 |
| 7.1. POWER ON SEQUENCE | 11 |
| 7.2. DETECTION | 12 |
| 7.3. CLASSIFICATION | 13 |
| 7.4. POWER UP | 13 |
| 7.5. DC DISCONNECT | 14 |
| 7.6. PROTECTION | 14 |
| 7.6.1. Port-Voltage Protection | 14 |
| 7.6.2. Over-Load Protection | 14 |
| 7.6.3. Short Protection | 14 |
| 7.6.4. Thermal Protection | 14 |
| 7.7. POWER BANK SELECTION | 14 |
| 7.8. SLAVE I2C INTERFACE | 15 |
| 7.9. MASTER I2C INTERFACE | 16 |
| 7.10. LOW DROPOUT REGULATOR | 16 |
| 8. DC SPECIFICATIONS | 17 |
| 8.1. ABSOLUTE MAXIMUM RATINGS | 17 |
| 8.2. OPERATING CONDITIONS | 17 |
| 8.3. DC PARAMETERS | 17 |
| 9. AC SPECIFICATIONS | 18 |
| 9.1. DETECTION ELECTRICAL CHARACTERISTICS | 18 |
| 9.2. CLASSIFICATION ELECTRICAL CHARACTERISTICS | 18 |
| 9.3. POWER DELIVER ELECTRICAL CHARACTERISTICS | 19 |
| 9.4. THERMAL SENSOR ELECTRICAL CHARACTERISTICS | 19 |
| 9.5. I2C SLAVE INTERFACE TIMING | 20 |
| 9.6. I2C MASTER INTERFACE TIMING | 21 |
| 10. MECHANICAL DIMENSIONS | 22 |
| 11. ORDERING INFORMATION | 23 |





List of Tables

| | | |
|-----------|--|----|
| TABLE 1. | PIN ASSIGNMENTS TABLE | 6 |
| TABLE 2. | POWER INTERFACE CONNECTION PINS | 8 |
| TABLE 3. | I2C SLAVE PINS | 8 |
| TABLE 4. | I2C MASTER PINS | 8 |
| TABLE 5. | GPIO PINS | 8 |
| TABLE 6. | CONFIGURATION PINS | 9 |
| TABLE 7. | POWER AND GROUND PINS | 9 |
| TABLE 8. | MISCELLANEOUS PINS | 10 |
| TABLE 9. | CLASSIFICATIONS AND MULTIPLE EVENT RESPONSES FOR PDs | 13 |
| TABLE 10. | ABSOLUTE MAXIMUM RATINGS | 17 |
| TABLE 11. | OPERATING CONDITIONS | 17 |
| TABLE 12. | DC PARAMETERS | 17 |
| TABLE 13. | DETECTION ELECTRICAL CHARACTERISTICS | 18 |
| TABLE 14. | CLASSIFICATION ELECTRICAL CHARACTERISTICS | 18 |
| TABLE 15. | POWER DELIVER ELECTRICAL CHARACTERISTICS | 19 |
| TABLE 16. | THERMAL SENSOR ELECTRICAL CHARACTERISTICS | 19 |
| TABLE 17. | I2C SLAVE MODE TIMING VALUES | 20 |
| TABLE 18. | I2C MASTER MODE FOR EEPROM AUTO DOWNLOAD TIMING VALUES | 21 |
| TABLE 19. | MECHANICAL DIMENSIONS | 22 |
| TABLE 20. | ORDERING INFORMATION | 23 |

List of Figures

| | | |
|-----------|--|----|
| FIGURE 1. | MULTIPLE CHIPS MANAGEMENT PSE APPLICATION | 3 |
| FIGURE 2. | DUMB PSE APPLICATION | 3 |
| FIGURE 3. | BLOCK DIAGRAM | 4 |
| FIGURE 4. | PIN ASSIGNMENTS | 5 |
| FIGURE 5. | POWER ON SEQUENCE | 11 |
| FIGURE 6. | TYPICAL RTL8238B-VB PORT VOLTAGE WAVEFORM | 12 |
| FIGURE 7. | SLAVE I2C ACCESS SEQUENCE | 15 |
| FIGURE 8. | I2C SLAVE MODE TIMING VALUES | 20 |
| FIGURE 9. | I2C MASTER MODE FOR EEPROM AUTO DOWNLOAD TIMING VALUES | 21 |





1. General Description

The RTL8238B-VB is a highly integrated octal Power Sourcing Equipment (PSE) Controller designed to facilitate the realization of more cost-effective Power over Ethernet (PoE) systems in Midspans and Endpoint PSE applications, allowing network devices to share power and data over the same cable. With a small package and RBOM (Rest of Bill of Materials) saving design, the RTL8238B-VB supports 8 independent 2-pair power ports.

The RTL8238B-VB is compatible with all IEEE 802.3af-2003 and 802.3at-2009 requirements, including resistor detection, PD classification, power-up, DC disconnection, and also supports standard Type-1/Type-2 PD as well as legacy/pre-standard PD (Powered Device).

With eight low-RDS (on) and high-voltage pass-FETs, the RTL8238B-VB device could drive 8 independent 2-pair power ports to supply maximum 36W per port.

The RTL8238B-VB provides PD real-time current, voltage, thermal monitoring, and excellent protection in the chip to protect against overload, short, under-voltage, and over-temperature. Multiple RTL8238B-VB devices can be cascaded for the composition of a PSE system together with an external low cost MCU, which can build a network Link Layer Discovery Protocol (LLDP) providing efficient dynamic power management in real time.

The RTL8238B-VB is available in an 8mm x 8mm QFN56 package and features an embedded 3.3V-1.8V Low Dropout Regulator (LDO) to further lower the BOM cost of the power supply circuit.



2. Features

- Compatible with IEEE 802.3af/IEEE 802.3at
- Supports 8 independent 2-pair power ports (maximum 36W per port)
- Supports detection of standard and part of non-standard PDs
- Supports multi-event classification
- Monitors the DC MPS (Maintain Power Signature)
- Real-time current/voltage/thermal monitoring and protection
 - ◆ Under-voltage protection
 - ◆ Over-voltage protection
 - ◆ Over-current protection
 - ◆ Short protection
 - ◆ Over-temperature protection
- Manual/Semi-Auto/Auto operation mode
- Low power dissipation
- Supports cascading of multiple devices
- Interfaces
 - ◆ Interrupt output pin for system and port events
 - ◆ I2C interface for communication with host
 - ◆ 3 x Configurable Power Bank input
- Operates via external 44V~57V and 3.3V supply
- 8mm*8mm*0.9mm QFN56 Package (0.5 mm pitch) with exposed pad

for 腾达
xieding(tenda.cn)

3. System Applications

3.1. Management PSE Application

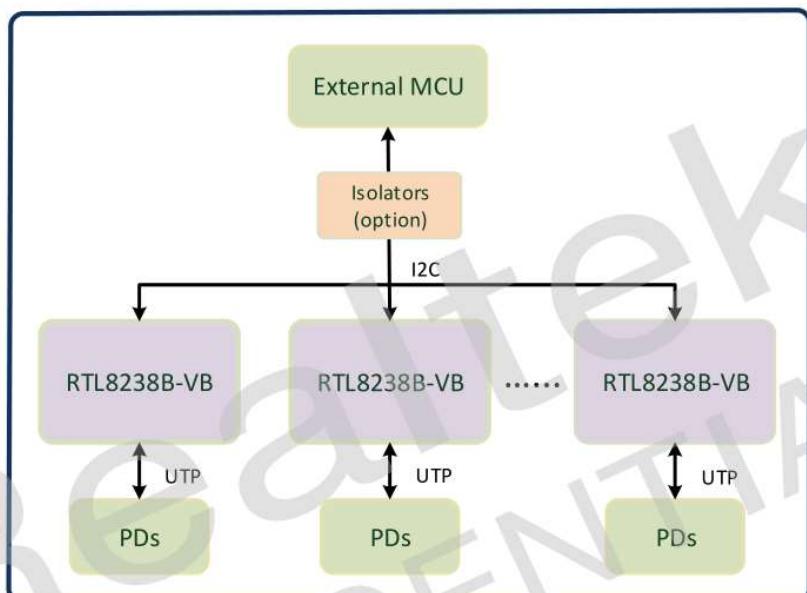


Figure 1. Multiple Chips Management PSE Application

3.2. Dumb PSE Application

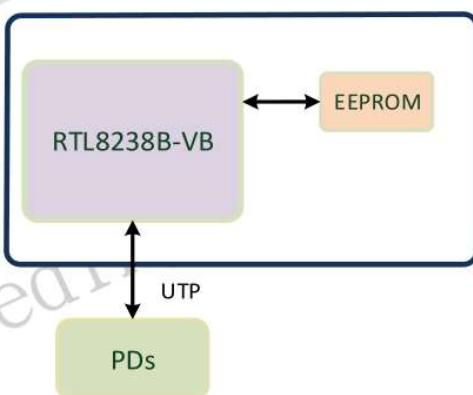


Figure 2. Dumb PSE Application

4. Block Diagram

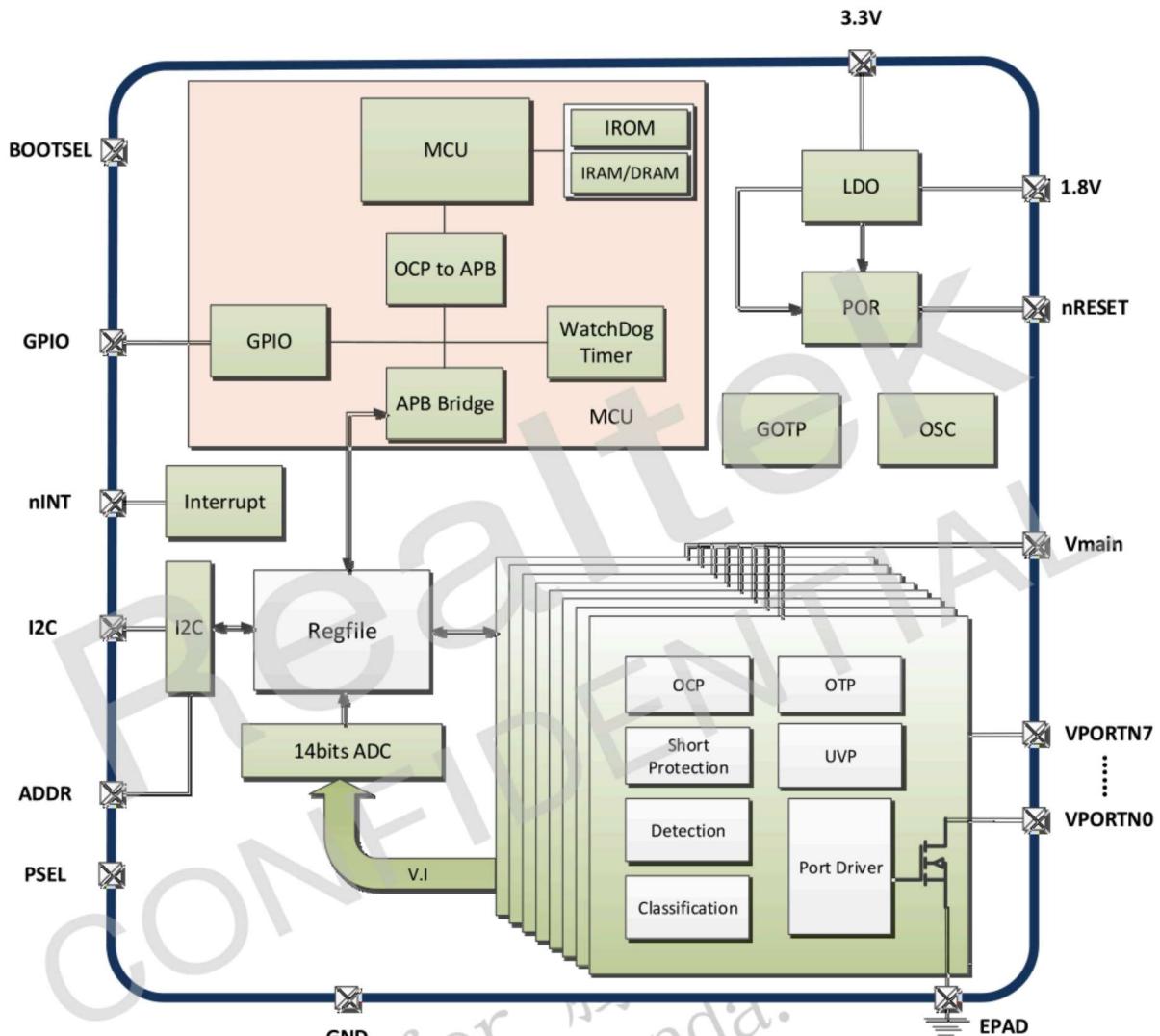


Figure 3. Block Diagram



5. Pin Assignments

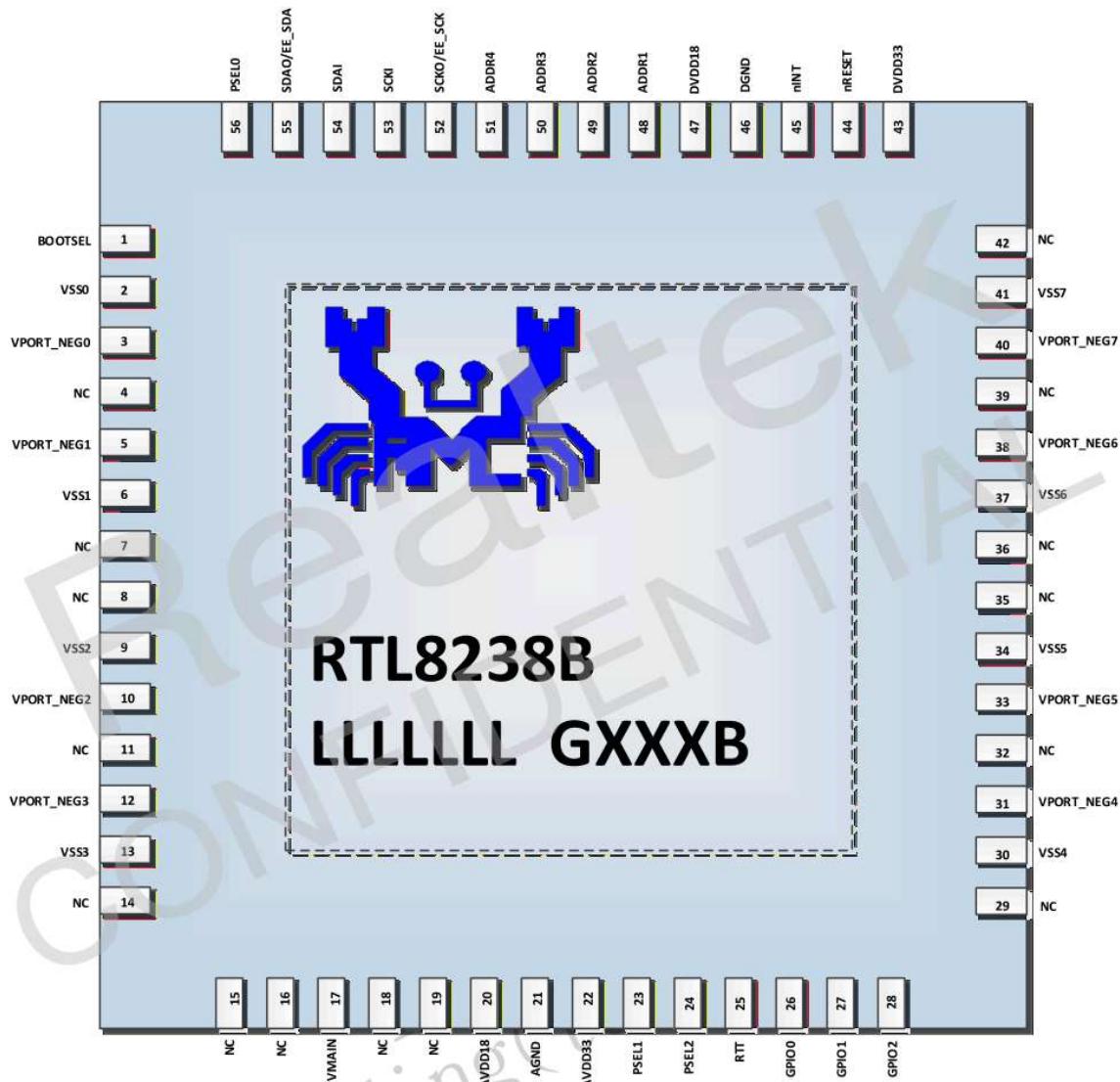


Figure 4. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' and Version B is indicated by the 'B' in GXXXB (Figure 4).



5.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified ‘Upon Reset’ time.

| | | | |
|---------------------|---|-------------------|--|
| P: | Digital Power Pin | G: | Digital Ground Pin |
| AP: | Analog Power Pin | AG: | Analog Ground Pin |
| AI: | Analog Input Pin | AO: | Analog Output Pin |
| AI _{PU} : | Analog Input Pin With Pull-Up Resistor | AI/O: | Analog Bi-Directional Input/Output Pin |
| I _{PU} : | Input Pin With Pull-Up Resistor | O _{PU} : | Output Pin With Pull-Up Resistor |
| I _{PD} : | Input Pin With Pull-Down Resistor | O _{PD} : | Output Pin With Pull-Down Resistor |
| I/O _{PU} : | Bi-Directional Input/Output Pin With Pull-Up Resistor | | |

Note: Pull-Up/ Pull-Down Resistor Typical Value = 75K Ohm

Table 1. Pin Assignments Table

| Name | Pin No. | Type |
|------------|---------|-----------------|
| BOOTSEL | 1 | I _{PD} |
| VSS0 | 2 | AG |
| VPORT_NEG0 | 3 | AI |
| NC | 4 | - |
| VPORT_NEG1 | 5 | AI |
| VSS1 | 6 | AG |
| NC | 7 | - |
| NC | 8 | - |
| VSS2 | 9 | AG |
| VPORT_NEG2 | 10 | AI |
| NC | 11 | - |
| VPORT_NEG3 | 12 | AI |
| VSS3 | 13 | AG |
| NC | 14 | - |
| NC | 15 | - |
| NC | 16 | - |
| VMAIN | 17 | AP |
| NC | 18 | - |
| NC | 19 | - |
| AVDD18 | 20 | AP |
| AGND | 21 | AG |
| AVDD33 | 22 | AP |
| PSEL1 | 23 | I _{PD} |

| Name | Pin No. | Type |
|------------|---------|-------------------|
| PSEL2 | 24 | I _{PD} |
| RTT | 25 | AI/O |
| GPIO0 | 26 | I/O _{PU} |
| GPIO1 | 27 | I/O _{PU} |
| GPIO2 | 28 | I/O _{PU} |
| NC | 29 | - |
| VSS4 | 30 | AG |
| VPORT_NEG4 | 31 | AI |
| NC | 32 | - |
| VPORT_NEG5 | 33 | AI |
| VSS5 | 34 | AG |
| NC | 35 | - |
| NC | 36 | - |
| VSS6 | 37 | AG |
| VPORT_NEG6 | 38 | AI |
| NC | 39 | - |
| VPORT_NEG7 | 40 | AI |
| VSS7 | 41 | AG |
| NC | 42 | - |
| DVDD33 | 43 | P |
| nRESET | 44 | I _{PU} |
| nINT | 45 | O _{PU} |
| DGND | 46 | G |



**RTL8238B-VB
Datasheet**

| Name | Pin No. | Type |
|-------------|---------|-----------------|
| DVDD18 | 47 | P |
| ADDR1 | 48 | I _{PU} |
| ADDR2 | 49 | I _{PU} |
| ADDR3 | 50 | I _{PU} |
| ADDR4 | 51 | I _{PU} |
| SCKO/EE_SCK | 52 | O _{PU} |

| Name | Pin No. | Type |
|-------------|---------|-----------------|
| SCKI | 53 | I _{PU} |
| SDAI | 54 | I _{PU} |
| SDAO/EE_SDA | 55 | O _{PU} |
| PSEL0 | 56 | I _{PD} |
| PGND | EPAD | AG |

for 腾达
xieding(tenda.cn)



6. Pin Descriptions

6.1. Power Interface Connection Pins

Table 2. Power Interface Connection Pins

| Pin Name | Pin No. | Type | Description |
|-------------|---------|------|--|
| VPORTE_NEG0 | 3 | AI | Power Interface connection pins for the current return from PDs. |
| VPORTE_NEG1 | 5 | | |
| VPORTE_NEG2 | 10 | | |
| VPORTE_NEG3 | 12 | | |
| VPORTE_NEG4 | 31 | | |
| VPORTE_NEG5 | 33 | | |
| VPORTE_NEG6 | 38 | | |
| VPORTE_NEG7 | 40 | | |

6.2. I2C Slave Pins

Table 3. I2C Slave Pins

| Pin Name | Pin No. | Type | Description |
|-------------|---------|-----------------|---|
| SCKI | 53 | I _{PU} | Serial Clock Input for Slave I2C interface. |
| SDAI | 54 | I _{PU} | Serial Data Input for Slave I2C interface. |
| SDAO/EE_SDA | 55 | O _{PU} | Serial Data Output for Slave I2C interface. |

6.3. I2C Master Pins

Table 4. I2C Master Pins

| Pin Name | Pin No. | Type | Description |
|-------------|---------|-------------------|--|
| SCKO/EE_SCK | 52 | O _{PU} | Serial Clock Output for Master I2C interface. |
| SDAO/EE_SDA | 55 | I/O _{PU} | Serial Data Input and Output for Master I2C interface. |

6.4. GPIO Pins

Table 5. GPIO Pins

| Pin Name | Pin No. | Type | Description |
|----------|---------|-------------------|-------------------------------|
| GPIO0 | 26 | I/O _{PU} | General Input and Output Pin. |
| GPIO1 | 27 | I/O _{PU} | General Input and Output Pin. |
| GPIO2 | 28 | I/O _{PU} | General Input and Output Pin. |



6.5. Configuration Pins

Table 6. Configuration Pins

| Pin Name | Pin No. | Type | Description |
|----------|---------|-----------------|---|
| PSEL0 | 56 | I _{PD} | Power Bank 0 Selection. |
| PSEL1 | 23 | I _{PD} | Power Bank 1 Selection. |
| PSEL2 | 24 | I _{PD} | Power Bank 2 Selection. |
| ADDR1 | 48 | I _{PU} | Device Address 1 Configuration. |
| ADDR2 | 49 | I _{PU} | Device Address 2 Configuration. |
| ADDR3 | 50 | I _{PU} | Device address 3 configuration. |
| ADDR4 | 51 | I _{PU} | Device address 4 configuration. |
| BOOTSEL | 42 | I _{PD} | Boot selection pin. 1'b0: boot code from External MCU 1'b1: boot code from EEPROM at 400KHz |

6.6. Power and Ground Pins

Table 7. Power and Ground Pins

| Pin Name | Pin No. | Type | Description |
|----------|---------|------|--------------------------------------|
| DVDD18 | 47 | P | Digital 1.8V Power. |
| AVDD18 | 20 | AP | Analog 1.8V Power. |
| DVDD33 | 43 | P | Digital 3.3V Power. |
| AVDD33 | 22 | AP | Analog 3.3V Power. |
| VMAIN | 17 | AP | Analog High Voltage Power (57V~44V). |
| AGND | 21 | AG | Analog Ground. |
| DGND | 46 | G | Digital Ground. |
| VSS0 | 2 | AG | Power Interface Ground. |
| VSS1 | 6 | AG | Power Interface Ground. |
| VSS2 | 9 | AG | Power Interface Ground. |
| VSS3 | 13 | AG | Power Interface Ground. |
| VSS4 | 30 | AG | Power Interface Ground. |
| VSS5 | 34 | AG | Power Interface Ground. |
| VSS6 | 37 | AG | Power Interface Ground. |
| VSS7 | 41 | AG | Power Interface Ground. |
| PGND | EPAD | AG | Power Interface Ground. |





6.7. Miscellaneous Pins

Table 8. Miscellaneous Pins

| Pin Name | Pin No. | Type | Description |
|----------|--|------------------|---|
| nRESET | 44 | I _P U | System Reset Input Pin. Pull the nRESET pin lower to force the chip to reset all circuits. To complete the reset function, this pin must be asserted for at least 7.2ms. It must be pulled high for normal operation. |
| nINT | 45 | O _P U | Interrupt Output Pin. As an open drain pin, it should be pulled high with 4.7Kohm resistor to DVDD33. |
| RTT | 25 | AI/O | Reserved for internal use. It should be left floating. |
| NC | 4, 7, 8, 11, 14~16, 18, 19, 29, 32, 35, 36, 39, 42 | - | No used. It should be left floating. |

7. Function Description

7.1. Power on Sequence

Two power domains are required for normal operation of the RTL8238B-VB (3.3V and 1.8V). For reliable power-on initialization, the following constraints should be included.

- T1 is the time when the 3.3V power starts rising
- T2 is the time when the 3.3V power is higher than V33_thrd (2.6V~2.8V) and the 1.8V power starts rising. The 3.3V power never falls lower than V33_thrd after T2
- T3 is the time when the 3.3V power is ready
- T4 is the time when the 1.8V power is higher than V18_thrd (1.35V~1.45V). The 1.8V power never falls lower than V18_thrd after T4
- T5 is the time when the 1.8V power is ready. The rise time of 1.8V power (time between T2 and T5) is less than 1ms
- T6 is the time when the pin reset signal is de-asserted
- T7 is the time for register access

The requirements are:

- The rising time of 3.3V power (time between T1 and T3) should be more than 0.1ms
- T6 should be later than T3 and T5
- T7 is recommend to be 50ms later than T6

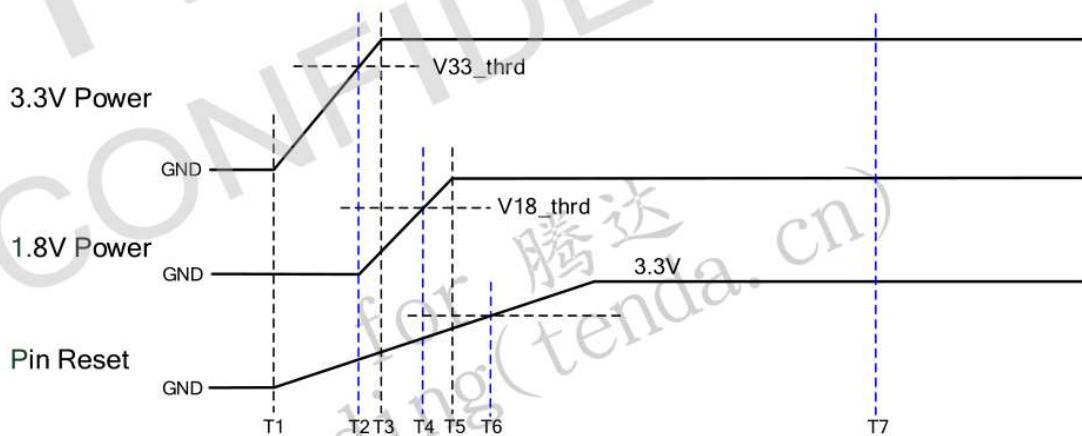


Figure 5. Power on Sequence

7.2. Detection

At detection stage, the RTL8238B-VB can estimate the equivalent circuit of PI (Power Interface) to decide the detection time and voltage. Detection can make two measurements using detected voltages. Each detection voltage lasts for $T_{det}/2$. The RTL8238B-VB calculates the resistance with the formula $\Delta V/\Delta I$.

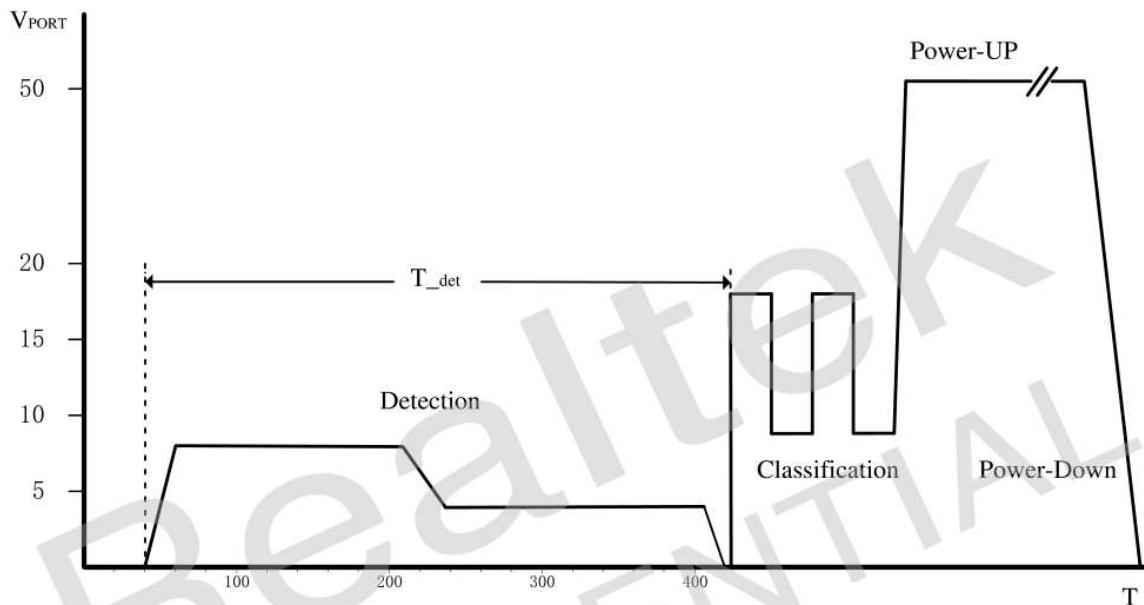


Figure 6. Typical RTL8238B-VB Port Voltage Waveform

The capacitance of PD can be calculated by the formula τ/R (time constant $\tau=RC$). The time constant comes from the climbing voltage.

The RTL8238B-VB detection checks the PI at a constant period. An Open circuit indicates that there is no PD connected to the cable, and there is a short circuit when a small impedance at PI is detected.

According to the standard, a valid signature resistance is in the band of $19k\Omega$ to $26.5k\Omega$ with a parallel capacitance up to $0.67\mu F$. The RTL8238B-VB accepts PDs as a valid signature in the range, rejecting all PDs with a resistance below $15k\Omega$ or above $33k\Omega$ when the legacy PD mode is disabled.

When the legacy PD mode is enabled, the RTL8238B-VB accepts a valid signature range with a legacy PD signature capacitance greater than $2.5\mu F$, and a signature resistance greater than $30k\Omega$. After detecting a non-IEEE Standard PD, the legacy PD mode is disabled and a different detection time will be automatically selected according to the climbing voltage.



7.3. Classification

The classification process is activated after a valid PD is detected. RTL8238B-VB classification is compatible with IEEE802.3af and IEEE802.3at to classify the Standard PD power level. The RTL8238B-VB asserts a voltage (18V) onto the PI and measures the current that the PD draws to judge the PD class signature. The class signatures indicate the PD requested Class as shown in Table 9.

Table 9. Classifications and Multiple Event Responses for PDs

| Current Threshold (mA) | Class Level |
|------------------------|--------------|
| 0 to 5 | 0 |
| 8 to 13 | 1 |
| 16 to 21 | 2 |
| 25 to 31 | 3 |
| 35 to 45 | 4 |
| Above 51 | 0 or invalid |

When the classification result is class 0, 1, 2, or 3, the PD is identified as a Type-1 PD and a 1-event classification is implemented. When the classification result is class 4, the PD is identified as a Type-2 PD and a 2-event classification is implemented. As the IEEE 802.3at standard requires PSE and PD to have mutual identification ability, the RTL8238B-VB provides a mark event voltage and a second class voltage when the first class result is class 4. After that, the PD can identify the RTL8238B-VB as a Type-2 PSE and can provide the required 30W power.

In addition to the above Physical Layer classification, the RTL8238B-VB also supports Data Link Layer (DLL) classification.

The RTL8238B-VB assigns class 0 to all PDs if classification is not implemented. If the class current is greater than the class 4 threshold, the RTL8238B-VB can assign class 0 or an invalid class level to the PD.

The RTL8238B-VB limits the current to the default 75mA threshold at class and mark events.

7.4. Power Up

Upon a successful detection and classification, the RTL8238B-VB supplies the power to the PD. The standard requires that the output current should be limited between 400mA and 450mA in power-up state within an inrush timer. The PD should not draw greater current than the current limit threshold at the inrush timeout. For the RTL8238B-VB, the inrush current to charge the PD load will be limited at typically 425mA within 55ms. If the current limit is still being reached at the inrush timeout, and an inrush error is reported while the power MOS is turned off, the PD would then fail to power up.



7.5. DC Disconnect

The RTL8238B-VB supports a DC disconnect scheme through monitoring the PD load current. When the port current is under the disconnect threshold for more than 360ms, the RTL8238B-VB will turn off the port and restart detection. In the case of a PD implementing MPS (Maintain Power Signature) current pulsing, the Tmpdo counter is reset each time and the current goes continuously higher than the disconnect threshold for 50ms.

7.6. Protection

The RTL8238B-VB supplies an all-round protection scheme through monitoring of port voltage, port current, and port temperature.

7.6.1. Port-Voltage Protection

The RTL8238B-VB will disconnect power from the PD when the port voltage is below the under-voltage protection threshold, which is typically at 32V. Power is also removed when the port voltage is higher than the over-voltage protection threshold, which is typically at 60V.

7.6.2. Over-Load Protection

The over-load current threshold is calculated based on the assigned class. Different class levels of PD have different over-load current thresholds. If an alternative value is desired, it needs to be set after powering up.

When the PD load current is above the threshold for more than the typical 60ms, the RTL8238B-VB will disconnect the power from the PD load.

7.6.3. Short Protection

The RTL8238B-VB monitors the port current in real-time. Once the port current reaches the current limit threshold, the port will activate the short protection mechanism as well as keep the port current at the current limit threshold. If the short protection activation lasts for a period of the set standard time, the RTL8238B-VB will disconnect the power from the PD load.

7.6.4. Thermal Protection

In some conditions, the temperature of any port or the whole chip may be too high to operate normally. The RTL8238B-VB is equipped with one temperature monitor per port, and also one for the whole chip. The port thermal protection system will shut down the power to the PD when it is over 187°C, whereas the thermal protection threshold, typically reached at 130°C, will be re-activated. Similarly, the behavior of whole chip thermal protection, typically reached at over 142°C, is to reset the system, and release the system when the chip temperature is under 128°C.

7.7. Power Bank Selection

The RTL8238B-VB supports eight power banks for system power configuration according to PSEL[2:0] input pins.

7.8. Slave I2C Interface

The RTL8238B-VB supports I2C slave mode for external host devices access. There are three I/O pins (SDAI, SDAO and SCKI) for the serial management interface. SDAI/SDAO is the data input/output signal, and SCKI is the clock input signal. The RTL8238B-VB device address is 7-bit: A0 is used to select access port0~port3 or port4~port7 register, A4~A1 is from the strapping pin ADDR4~ADDR1 configuration, and A6~A5 is 2'b01 by default and can be modified through register setting.

The RTL8238B-VB supports I2C broadcast write mode when ADDR4~ADDR1 are configured to 0x0. The hosts or external microcontroller can configure the same register to all slave devices through a write command. The broadcast write mode can be disabled, and the broadcast address can also be modified through register setting.

The read/write data sequence is shown in Figure 7. The read/write bit is 1'b1/1'b0 respectively.

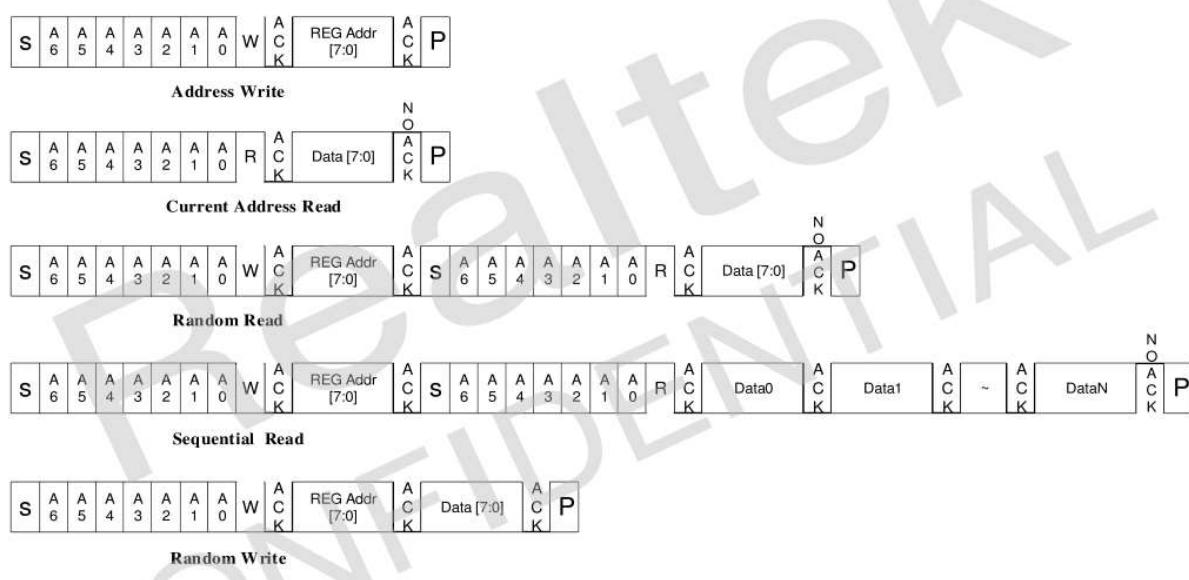


Figure 7. Slave I2C Access Sequence



7.9. Master I2C Interface

Upon reset or power on, the internal MCU can autoload the firmware code from EEPROM by the master I2C interfaces – EE_SDA and EE_SCK. The EE_SDA is the bidirectional data signal, and the EE_SCK is the clock signal output – typically with a frequency of 400KHz.

The RTL8238B-VB only supports at least 256Kb EEPROM. The address is 16-bit (two bytes). The device address should be 0 when auto downloading.

The internal MCU will not drive the master I2C bus to load EEPROM if the strapping pin ‘BOOTSEL’ input is pulled low upon reset, and the EEPROM auto-load sequence will be terminated immediately if the EEPROM does not exist.

7.10. Low Dropout Regulator

To simplify the system design and RBOM, the RTL8238B-VB supplies 3.3V to 1.8V LDO. Each 1.8V power pin requires one 0.1 μ F capacitor.



8. DC Specifications

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 10. Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|---------|-------|-------|
| Storage Temperature | - | +125 | °C |
| VMAIN, Supply Referenced to AGND | GND-0.3 | 72 | V |
| VPORTE_NEG0, VPORTE_NEG1, VPORTE_NEG2, VPORTE_NEG3, VPORTE_NEG4, VPORTE_NEG5, VPORTE_NEG6, VPORTE_NEG7, Supply Referenced to PGND | GND-0.3 | 72 | V |
| DVDD33, AVDD33, Supply Referenced to GND, AGND | GND-0.3 | +3.63 | V |
| DVDD18, AVDD18, Supply Referenced to GND, AGND | GND-0.3 | +1.98 | V |

8.2. Operating Conditions

Table 11. Operating Conditions

| Symbol | Parameter | Min | Typ. | Max | Units |
|--------|---|-------|------|-------|-------|
| Ta | Ambient Operating Temperature. At this operating temperature, the junction temperature of the IC must be under 125°C | -40 | - | 85 | °C |
| Tj | Operating Junction Temperature | -40 | - | 125 | °C |
| VMAIN | Analog High Voltage Power | 44 | - | 57 | V |
| DVDD33 | Digital 3.3V Power | 3.135 | 3.3 | 3.465 | V |
| DVDD18 | Digital 1.8V Power | 1.71 | 1.8 | 1.89 | V |
| AVDD33 | Analog 3.3V Power | 3.135 | 3.3 | 3.465 | V |
| AVDD18 | Analog 1.8V Power | 1.71 | 1.8 | 1.89 | V |

8.3. DC Parameters

Table 12. DC Parameters

| Symbol | Parameter | Conditions | Min | Typ. | Max | Units | Notes |
|-----------------|----------------------------------|-----------------|-----|------|-----|-------|-------|
| V _{IH} | Input-High Voltage | LVTTL | 2.0 | - | - | V | - |
| V _{IL} | Input-Low Voltage | LVTTL | - | - | 0.8 | V | - |
| V _{OH} | Output-High Voltage | - | 2.4 | - | - | V | - |
| V _{OL} | Output-Low Voltage | - | - | - | 0.4 | V | - |
| I _{IL} | Input-Leakage Current | VIN = 3.3V or 0 | -10 | ±1 | 10 | µA | - |
| I _{OZ} | Tri-State Output-Leakage Current | - | -10 | ±1 | 10 | µA | - |
| R _{PU} | Input Pull-Up Resistance | - | - | 75 | - | KΩ | 1 |
| R _{PD} | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 1 |

Note 1: These values are typical values checked in the manufacturing process and are not tested.





9. AC Specifications

9.1. Detection Electrical Characteristics

Table 13. Detection Electrical Characteristics

| Symbol | Parameter | Min | Typ. | Max | Units |
|----------------------|---|-----|------|------|-------|
| R _{good} | Accept Signature Resistance | 19 | - | 26.5 | KΩ |
| R _{bad} | Reject Signature Resistance (Outside This Range) | 15 | - | 33 | KΩ |
| C _{good} | Accept Signature Capacitance | - | - | 670 | nf |
| C _{bad} | Reject Signature Capacitance | 10 | - | - | μF |
| R _{open_pd} | Open Port Signature Resistance | 50 | - | - | KΩ |
| R _{open} | Open Circuit Resistance (No PD Connected) | 500 | - | - | KΩ |
| R _{short} | Short Port Signature Resistance | - | - | 1 | KΩ |
| C _{legacy} | Accept Signature Capacitance for Legacy PD | 2.5 | - | 50 | μF |
| t _{det} | Detection Timing | - | - | 450 | ms |
| t _{dbo} | Alternative B Detection Back-off Time | 2 | - | - | s |
| V _{vaild} | Valid Detection Voltage Range | 2.8 | - | 10 | V |
| ΔV _{test} | Voltage Difference Between Test Points | 1 | - | - | V |
| - | ADC Full Scale on Detection | - | 16 | - | V |
| R _{swoff} | Detection Switch Off Pull-Up Resistor Between V48 and VPORTNx | - | 60 | - | KΩ |
| V _{oc} | Open Circuit Voltage | 12 | - | 30 | V |

9.2. Classification Electrical Characteristics

Table 14. Classification Electrical Characteristics

| Symbol | Parameter | Min | Typ. | Max | Units |
|------------------------|--|------|------|------|-------|
| V _{class} | Classification Voltage | 15.5 | 18 | 20.5 | V |
| V _{mark} | Mark Event Voltage | 7 | 9 | 10 | V |
| I _{class_lim} | Class Event Current Limitation | 51 | 75 | 100 | mA |
| I _{mark_lim} | Mark Event Current Limitation | 51 | 75 | 100 | mA |
| T _{pdc} | 1-Event Physical Layer Classification Time | 10 | 12 | 75 | ms |
| t _{CLE1} | 1 st Class Event Time | 6 | 12 | 30 | ms |
| t _{CLE2} | 2 nd Class Event Time | 6 | 12 | 30 | ms |
| t _{MIE1} | Mark Event Time (Except Last Mark Event) | 6 | 9 | 12 | ms |
| t _{MIE2} | Last Mark Event | 6 | 50 | - | ms |
| I _{class} | Class 0 Criteria | 0 | - | 5 | mA |
| | Class 1 Criteria | 8 | - | 13 | mA |
| | Class 2 Criteria | 16 | - | 21 | mA |
| | Class 3 Criteria | 25 | - | 31 | mA |
| | Class 4 Criteria | 35 | - | 45 | mA |



9.3. Power Deliver Electrical Characteristics

Table 15. Power Deliver Electrical Characteristics

| Symbol | Parameter | Min | Typ. | Max | Units |
|----------------------|---|------|------|------|-------|
| Rdson | Port Switch on Resistance | - | 0.2 | 0.4 | Ω |
| Vport_pse | Output Voltage in the POWER_ON State | | | | |
| Type 1 | 44 | - | 57 | V | |
| Type 2 | 50 | - | 57 | V | |
| - | ADC Full Scale On Power Up/On | - | 64 | - | V |
| - | Voltage Measure Accuracy | -1.5 | - | +1.5 | V |
| I _{Inrush} | Output current in POWER_UP State | 400 | - | 450 | mA |
| t _{Inrush} | Inrush Time | 50 | - | 75 | ms |
| I _{lim} | Short Circuit Current Limit Threshold | | | | |
| Type 1 | 400 | - | 1000 | mA | |
| Type 2 | 750 | - | 1000 | mA | |
| t _{lim} | Short Circuit Time Limit | | | | |
| Type 1 | 50 | - | 75 | ms | |
| Type 2 | 10 | - | 75 | ms | |
| t _{cut} | Overload Time Limit | 50 | - | 75 | ms |
| - | ADC Full Scale On Current Measurement | - | 1000 | - | mA |
| - | Current Measure Accuracy | -22 | - | +22 | mA |
| t _{pon} | Power Turn On Time | - | - | 400 | ms |
| t _{rise} | Switch Turn On Rise Time | 15 | - | - | μs |
| t _{off} | Turn Off Time (Receiving Off Command to Vport_pse < 2.8V) | - | - | 500 | ms |
| V _{off} | Turn Off Voltage | - | - | 2.8 | V |
| I _{hold-2P} | DC MPS Absent Current | 5 | - | 10 | mA |
| t _{MPSDO} | MPS Dropout Time | 300 | - | 400 | ms |
| t _{MPS} | DC MPS Time | - | 50 | 60 | ms |

9.4. Thermal Sensor Electrical Characteristics

Table 16. Thermal Sensor Electrical Characteristics

| Symbol | Parameter | Min | Typ. | Max | Units |
|-----------------------|--|-----|------|-----|-------|
| T _{SHUT} | Port Thermal Shutdown Threshold | - | 187 | - | °C |
| T _{SHUT_REC} | Port Thermal Shutdown Recovery Threshold | - | 130 | - | °C |
| T _{RST} | Global Thermal Shutdown Threshold | - | 142 | - | °C |
| T _{RST_REC} | Global Thermal Shutdown Recovery Threshold | - | 128 | - | °C |

9.5. I2C Slave Interface Timing

Table 17. I2C Slave Mode Timing Values

| Symbol | Parameter | Min | Typ. | Max | Units |
|--------------|--|-----|------|------|-------|
| f_{SCL} | SCL Clock Frequency | - | - | 2.28 | MHz |
| t_{HIGH} | High Period Of The SCL Clock | 176 | - | - | ns |
| $t_{SU.STA}$ | Set-Up Time For START Condition | 88 | - | - | ns |
| $t_{HD.STA}$ | Hold Time For START Condition | 88 | - | - | ns |
| $t_{HD.DAT}$ | Data Input Hold Time | 0 | - | - | ns |
| $t_{SU.DAT}$ | Data Input Set-Up Time | 88 | - | - | ns |
| t_{DH} | Data Output Delay Hold Time (Note1) | 79 | - | 250 | ns |
| $t_{SU.STO}$ | Set-Up Time For STOP Condition | 88 | - | - | ns |
| t_{BUF} | Bus Free Time Between a STOP and START Condition | 351 | - | - | ns |

Note1: t_{DH} is measured under the condition of the external 4.7K pull-up resistor.

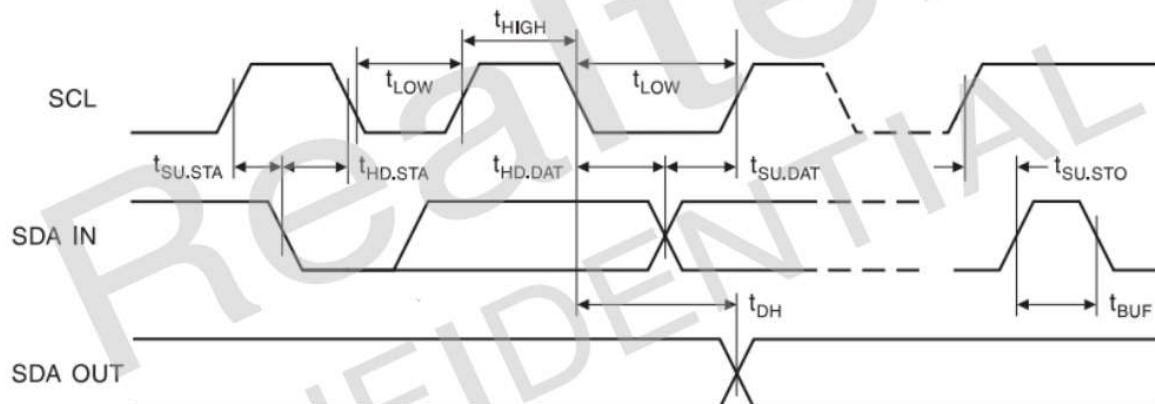


Figure 8. I2C Slave Mode Timing Values

9.6. I2C Master Interface Timing

Table 18. I2C Master Mode for EEPROM Auto Download Timing Values

| Symbol | Parameter | Min | Typ. | Max | Units |
|--------------|-----------------------------|------|------|-----|---------|
| f_{SCL} | SCL Clock Frequency | 380 | - | 420 | KHz |
| t_{LOW} | Clock Pulse Width Low | 1.19 | - | - | μs |
| t_{HIGH} | Clock Pulse Width High | 1.19 | - | - | μs |
| $t_{HD.STA}$ | Start Hold Time | 1.19 | - | - | μs |
| $t_{SU.STA}$ | Start Set-up Time | 1.19 | - | - | μs |
| $t_{SU.STO}$ | Stop Set-up Time | 1.19 | - | - | μs |
| $t_{HD.DAT}$ | PSE Data Output Hold Time | 0.63 | - | - | μs |
| $t_{SU.DAT}$ | PSE Data Output Set-up Time | 0.55 | - | - | μs |
| t_{DH} | PSE Data Input Hold Time | 132 | - | - | ns |
| t_{SU} | PSE Data Input Set-Up Time | 88 | - | - | ns |

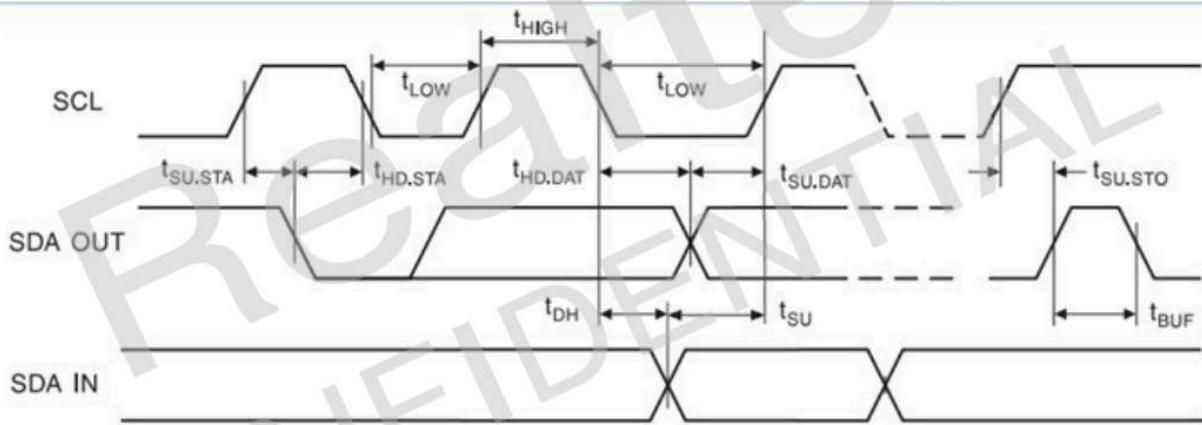


Figure 9. I2C Master Mode for EEPROM Auto Download Timing Values

10. Mechanical Dimensions

Plastic Quad Flat No-Lead Package 56 Leads 8x8mm² Outline.

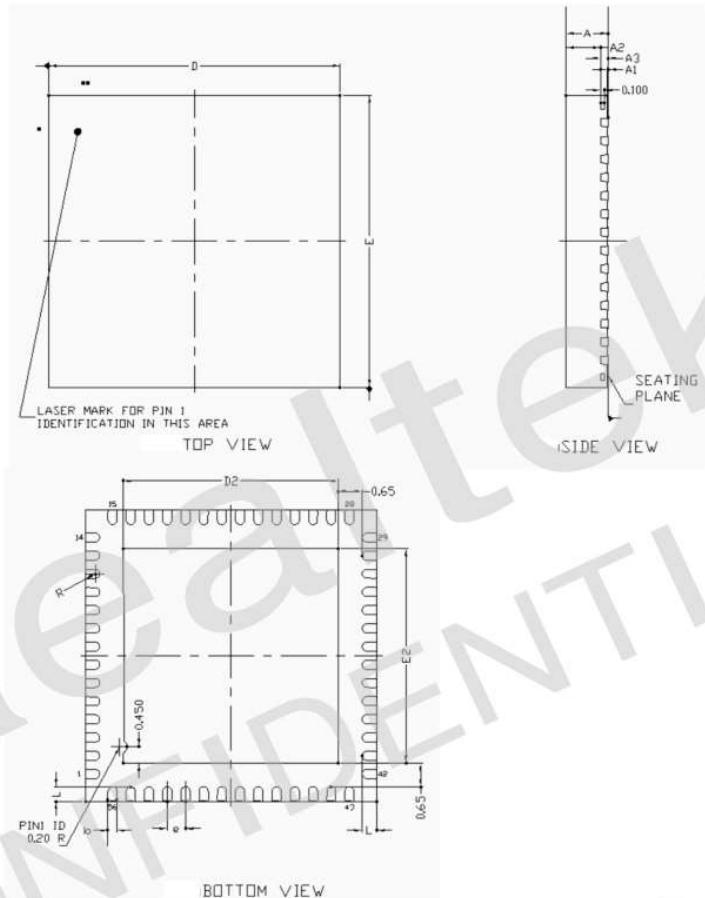


Table 19. Mechanical Dimensions

| Symbol | Dimension in mm | | | Dimension in inch | | |
|--------------------------------|-----------------|------|------|-------------------|-------|-------|
| | Min | Nom. | Max | Min | Nom. | Max |
| A | - | - | 0.90 | - | - | 0.035 |
| A ₁ | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A ₂ | - | 0.65 | 0.70 | - | 0.026 | 0.028 |
| A ₃ | 0.203 REF | | | 0.008 REF | | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D/E | 8.00 BSC | | | 0.315 BSC | | |
| D ₂ /E ₂ | 5.80 | 5.90 | 6.00 | 0.228 | 0.232 | 0.236 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Notes: CONTROLLING DIMENSION: MILLIMETER(mm).

REFERENCE DOCUMENT: JEDEC MO-220.





11. Ordering Information

Table 20. Ordering Information

| Part Number | Package |
|----------------|-----------------------------|
| RTL8238B-VB-GR | QFN56 E-PAD ‘Green’ Package |

Note: See section 5.1, page 5 for package identification information.

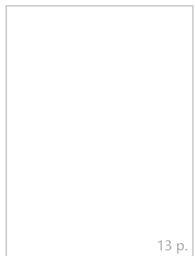
Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: +886-3-5780211 Fax: +886-3-5776047
www.realtek.com

全文阅读已结束，下载本文需要使用

270 积分

 下载此文档

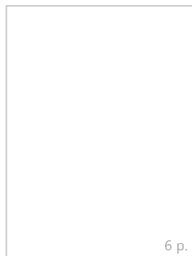
阅读了该文档的用户还阅读了这些文档



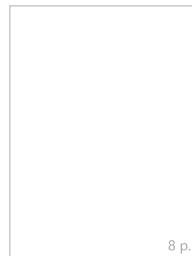
GR5302
Datasheet-V1.0-



GR5301
Datasheet-V1.0-



GR5300
Datasheet-V1.0-



GR6953 Datasheet
Ver1.0-20100324



RTL8211E_G-
VB_VL-



RTL8211B(L)_Li

发表评论

验证码:



换一张

匿名评论

提交

关于我们

关于道客巴巴

网站声明

人才招聘

网站地图

联系我们

APP下载

帮助中心

会员注册

文档下载

如何获取积分

关注我们

新浪微博

