RTL9311BM/R-CG

LAYER 3 MANAGED 24*10/100/1000M + 4*10G PORT SWITCH CONTROLLER

Realtek confidential files
The document authorized to
瑞科 (timelytech.com.cn)
white

DESIGN GUIDE

(CONFIDENTIAL: Development Partners Only)

Rev. 0.3
8 Feb. 2022
Track ID: JATRxxxx-xxxx-xx

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

©2022 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

USING THIS DOCUMENT

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2021-6-7	Draft
0.2	2021-12-30	Update
0.3	2022-2-8	Add ddr3 & Stacked SFP+ layout guide

Realtek confidential files
The document authorized to
white(timelytech.com.cn)

Table of Contents

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

List of Tables

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

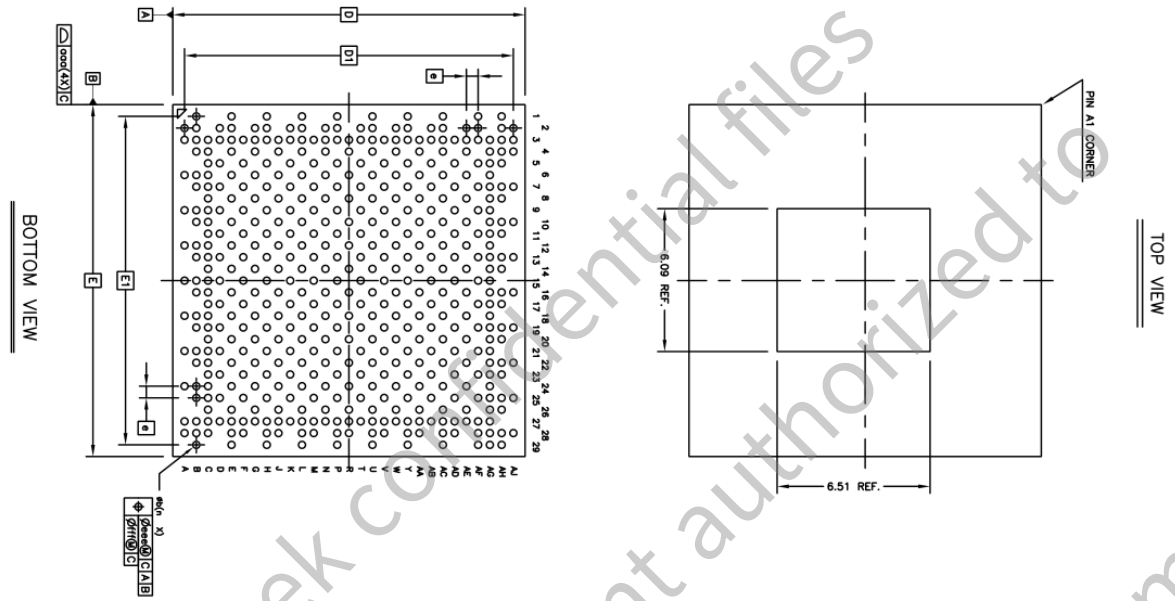
List of Figures

Realtek confidential files
The document authorized to
瑞科
White(timelytech.com.cn)

1. Chip package Description

1.1. Package Information

FC-CSPBGA (15*15)



Package :		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			MFC VFBGA		
Body Size:	X	E	15.000		
	Y	D	15.000		
Ball Pitch :		e		0.500	
Total Thickness :		A	0.748	0.828	0.908
Mold Thickness :		M		0.370	Ref.
Substrate Thickness :		S		0.248	Ref.
Ball Diameter :				0.300	
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa		0.150	
Mold Parallelism :		ccc		0.200	
Coplanarity:		ddd		0.100	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.050	
Ball Count :		n		474	
Edge Ball Center to Center :	X	E1		14.000	
	Y	D1		14.000	

Realtek confidential files
The document authorized to
瑞科
White(timeytech.com.cn)

2. Chip Mode Config Guide

RTL9311BM 共有 29 个 MAC，MAC0~27 为正常 port 并支持 stacking，MAC28 为 CPU port。当配置为 cascade mode 时，MAC24、MAC25 为 cascade channel，其中 MAC24 会升速到 20G。

一般会有如下两种应用：

- 24*10/100/1000Base-T + 4 *10G
- 48*10/100/1000Base-T + 4*10G

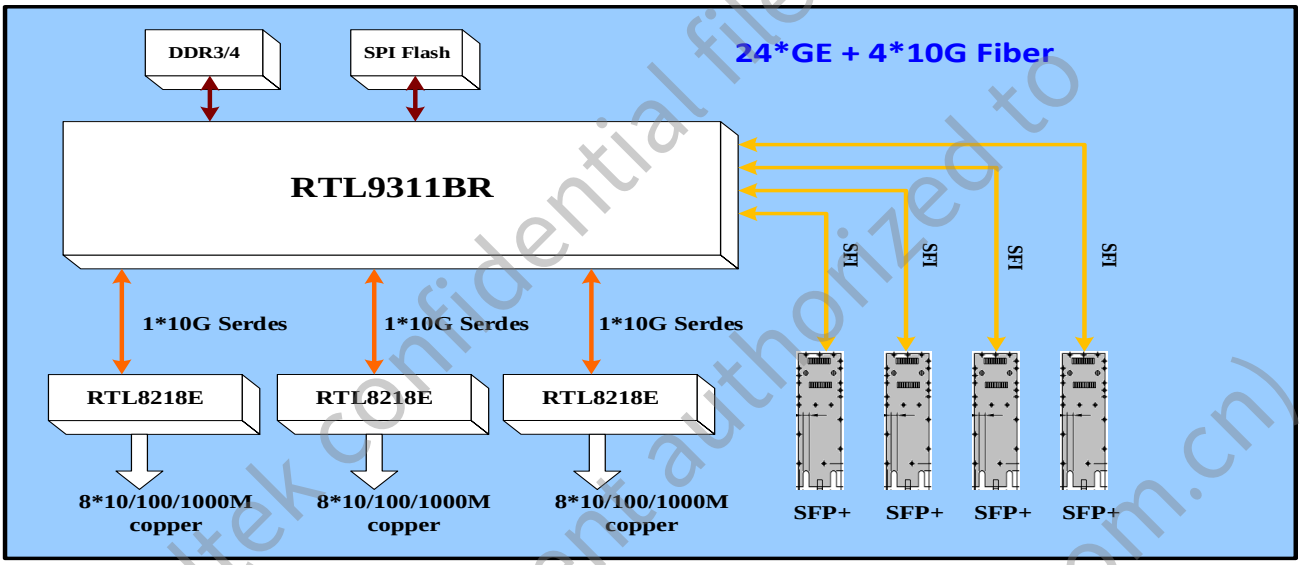


Figure 1. 24 10/100/1000Base-T + 4 10G Fiber

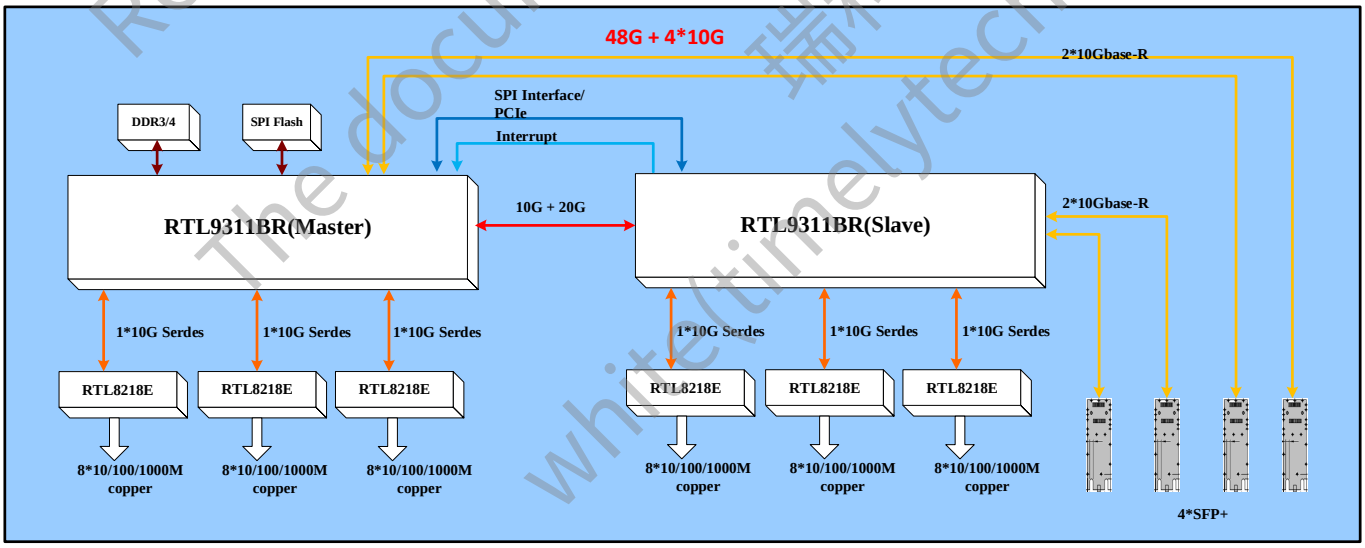


Figure 2. 48 10/100/1000Base-T + 4 10G Fiber

Realtek confidential files
The document authorized to 瑞科
white(timelytech.com.cn)

如 Figure 2 所示 cascade 应用中，master 和 slave RTL9311BM 会有配置差异，加上 24G+4*10G 的模式，会有三种情况，下面会列举这三类配置差异。

2.1. Hardware configure differences

2.1.1. Power Supply

由于 cascade slave RTL9311BM 的 CPU 不工作，所以一些相关的 power 可以不用供电，具体 power pin 如下：

Table 1 Power Supply differences

Power pin	24G+4*10G	24G+20G+3XG(master)	24G+20G+3XG(slave)
MVDDH/MVDD/MVDD_CK	√	√	×
DVDDL_CPU	√	√	×
Other power	√	√	√

2.1.2. External interface

同上，由于 slave RTL9311BM 的 CPU 不工作，所以一些相关的 interface 不支持使用：

Table 2 External interface differences

Interface	24G+4*10G	24G+20G+3XG(master)	24G+20G+3XG(slave)
DDR	√	√	×
SPI Flash	√	√	×
P Nand Flash	√	√	×
UART	√	√	×
USB	√	√	×
PCIE	√	√（RC Mode）	√（EP Mode）
GPIO	√	√	×

2.1.3. Strap pin

Strap pin 会涉及 SYS_CLK_SEL（reg：0xBB00A5C0[0]可查看代值）的区别，cascade mode 下会升频至 375M，另外会由 SOC_PCIE_MODE_SEL[1:0] （reg：0xBB00A5C0[9:8]可查看代值）决定两片 RTL9311BM mode。

Realtek confidential files
The document authorized to white(timelytech.com.cn)
瑞科

SYS_CLK_SEL：

0b0: 24G+4_10G mode

0b1: 24G+1_20G+3_10G mode

SOC_PCIE_MODE_SEL[1:0]：

2b00: internal CPU only (soc on and PCIe power down)

2b01: EP mode (soc power down and PCIe EP)

2b10: RC mode(soc on and PCIe RC)

2b11: RESERVED

Table 3 Strap pin differences

Strap pin	24G+4*10G	24G+20G+3XG(master)	24G+20G+3XG(slave)
SYS_CLK_SEL	0	1	1
SOC_PCIE_MODE_SEL[1]	X	1	0
SOC_PCIE_MODE_SEL[0]	X	0	1

2.1.4. Cascade & Serdes mode differences

Table 4 Cascade & Serdes mode differences

Register	24G+4*10G	24G+20G+3XG(master)	24G+20G+3XG(slave)
MAC_L2_GLOBAL_CTRL2[7]	0x0	0x1	0x1
STK_DBG_CTRL[0]	0x1	0x0	0x0
SDS_MODE_SEL_1[4:0]	Not 0xB	0Xb	0xB
SDS_MODE_SEL_1[9:5]	all value is valid	0x1A	0x1A

2.2. Software configure differences

Table 5 Configure register differences

Register	24G+4*10G	24G+20G+3XG(master)	24G+20G+3XG(slave)
FC_PORT_THR_SET_SEL[17:16]	0x1	0x1	0x1
TRK_CTRL[2]	1	0	0
TRK_CTRL[4]	0	0	0
TRK_LOCAL_TBL_REFRESH[0]	0x1	0x1	0x1
TRK_STK_CTRL[15:0]	0x0	0x3	0x3
TRK_LOCAL_TBL_REFRESH[0]	0x1	0x1	0x1
STK_GBL_CTRL[7:4]	0x0	0x2	0x1

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

STK_GBL_CTRL[3:0]	0x0	0x2	0x2
STK_GBL_CTRL_ENCAP_DUP[7:4]	0x0	0x2	0x1
STK_GBL_CTRL_ENCAP_DUP[3:0]	0x0	0x1	0x1
STK_PORT_ID_CTRL [0]. STK_PORT_ID[5:0]	0x0	0x18	0x18
STK_PORT_ID_CTRL [1]. STK_PORT_ID[11:6]	0x0	0x19	0x19
STK_PORT_ID_CTRL_DUP [0]. STK_PORT_ID[5:0]	0x0	0x18	0x18
STK_PORT_ID_CTRL_DUP [1]. STK_PORT_ID[11:6]	0x0	0x19	0x19
STK_DEV_PORT_MAP_CTRL [1].DEV_PORT_MAP[31:16]	0x0	0x3	0x3
L2_CTRL[11]	0x0	0x1	0x1
TRK_CTRL.STK_HASH_CAL[3:3]	0x0	0x1	0x1
ETE_FC_CTRL[2]	0x0	0x1	0x1
ETE_FC_CTRL[1]	0x0	0x1	0x1
ETE_FC_CTRL[0]	0x0	0x1	0x1
STK_CASCADE_TRK_HASH	0x1	0x21	0x21
STK_CASCADE_TRK_HASH_PORT_SEL	0x0	0x8100100	0x8100100
STK_CASCADE_CTRL. CASCADE_SLAVE_ID[7:4]	0x0	0x1	0x1
STK_CASCADE_CTRL. CASCADE_MASTER_ID[3:0]	0x0	0x2	0x2
MAC_L2_PORT_CTRL [24]	0x800193	0x193	0x193
MAC_L2_PORT_CTRL [25]	0x800193	0x193	0x193
PER_PORT_MAC_RSVD [24]	0x0	0xe	0xe
PER_PORT_MAC_RSVD [25]	0x0	0x8	0x8

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

3. Power domain Description

RTL9311BM 所有的 power pin 见下图，其中 Voltage range 统一为±3%，Current 裕量很大，后续会补上实际测量值。

Table 6 Configure register differences

Power#	NET_NAME	Pin count	Curren/mA	Voltage/A	Description
1	DVDDL_CPU	6	1000	0.9	CPU Digital Low Voltage Power
2	SVDDL	9	1500	0.9	SERDES Low Voltage Power
3	SVDDL_CK0	2	120	0.9	CMU Low Voltage Power
	SVDDL_CK1	1	80	0.9	CMU Low Voltage Power
	SVDDL_CK2	1	40	0.9	CMU Low Voltage Power
	SVDDL_CK3	1	40	0.9	CMU Low Voltage Power
	SVDDL_CK4	1	40	0.9	CMU Low Voltage Power
4	DVDDL	21	6000	0.9	Digital Low Voltage Power
	AVDDL_BG	1	50	0.9	BandGap Low Voltage Power
	AVDDL_XTAL	1	50	0.9	XTAL Low Voltage Power
	AVDDL_PLL	1	50	0.9	PLL Low Voltage Power
	SVDDL_PEX	1	150	0.9	PCIE Low Voltage Power
	SVDDL_SOC	1	150	0.9	SOC serdes（USB &SGMII) Low Voltage Power
5	SVDDH	1	1000	3.3	SERDES High Voltage Power
	DVDDH	2	1000	3.3	Digital High Voltage Power
	DVDDH_XSMI	1	1000	3.3/1.8	XG PHY smi High Voltage Power
	AVDDH_BG	1	1000	3.3	BandGap High Voltage Power
	AVDDH_XTAL	1	1000	3.3	XTAL High Voltage Power
	AVDDH_PLL	1	1000	3.3	PLL High Voltage Power
	MVDDH	1	1000	3.3	DDR PLL High Voltage Power
	SVDDH_SOC	1	1000	3.3	SOC serdes（USB &SGMII&PCIe) High Voltage Power
	VDDH_SOC	1	1000	3.3	SOC Digital High Voltage Power
6	VDD_SPI	1	1000	3.3/1..8	Power for SPI flash controler
	VDD_NAND	1	1000	3.3/1..8	Power for P-nand flash controler
7	MVDD	6	500	1.2	Power for DDR SDRAM IO
	MVDD_CK	1	500	1.2	

Realtek confidential files
The document authorized to 瑞科 white(timelytech.com.cn)

4. LED user guide

4.1. General Description

RTL9311BM provide flexible LED display to show speed, link status and other information of the port status. RTL9311BM supports three LED modes: serial mode, single color scan mode and bi-color scan mode. LED mode is decided by register configured after power on or reset as shown on Table 7.

Table 7 LED mode select register

Register Name	Description
LED_MOD[1:0]	LED MODE selection. 0x0: Disable LED. 0x1: Enable LED, and display LED in serial mode; 0x2: Enable LED, and display LED in single color scan mode; 0x3: Enable LED, and display LED in bicolor scan mode;

4.1.1. LED definition setting

RTL9311BM supports four sets of LED definition setting. Furthermore, RTL9311BM provides two registers for LED_SET selecting, one for copper and the other for fiber.

Note: In bi-color LED mode,LED0 and LED1 cannot light simultaneously, so the definition of LED0 and LED1 should avoid this restriction.

Table 8 LED SET register

Name	Description
SETx_LED3_SEL[15:0]	Select set0 LED3 mode configuration. Default is 500M Link/Act.
SETx_LED2_SEL[15:0]	Select set0 LED2 mode configuration. Default is Full duplex.
SETx_LED1_SEL[15:0]	Select set0 LED1 mode configuration. Default is 1000M Link/Act.
SETx_LED0_SEL[15:0]	Select set0 LED0 mode configuration. Default is 10M/100M Link/Act.
LED_COPR_SET_PSEL[1:0]	Select per port copper LED definition is set0 or set1 or set2 or set3.
LED_FIB_SET_PSEL[1:0]	Select per port fiber LED definition is set0 or set1 or set2 or set3.

Realtek confidential files
The document authorized to 瑞科
white(timelytech.com.cn)

Table 9 LED mode select register

SETx_LEDx_SEL[15:0]		Description	
Bit[0]	10G	Speed selection. Combine with Link/Link Flash/ACT (Bit[11:9])	
Bit[1]	5G		
Bit[2]	two_pair2.5G		
Bit[3]	2.5G		
Bit[4]	two_pair 1G		
Bit[5]	1G		
Bit[6]	500M		
Bit[7]	100M		
Bit[8]	10M		
Bit[9]	Link	LED light when link established	Combine with speed selection (Bit[8:0])
Bit[10]	Link Flash	LED blink when link established	
Bit[11]	ACT	LED blink when packet transmitting or receiving	
Bit[12]	RX	LED blink when packet receiving	There is no relationship with speed selection.
Bit[13]	TX	LED blink when packet transmitting	
Bit[14]	COL	LED blink when collision occurring	
Bit[15]	Duplex	LED light when link at full duplex	

4.1.2. Power on blinking

RTL9311bBR also support power on blinking after every power on or reset. In order to support bi-color LED display, three steps are designed. Table 10 is the list of register that control the LED on/off in step1 and step2, and in step3 all LED are off. LED on/off time in each step can also be set by register.

Table 10 LED POWER SETP register

Register Name	Description
STEP2_PWR_ON_LED_3_0	Select power on blinking LED[3:0] in step 2 power on duration. "0" is LED off, "1" is LED on.
STEP1_PWR_ON_LED_3_0	Select power on blinking LED[3:0] in step 1 power on duration. "0" is LED off, "1" is LED on

Table 11 PWR_ON_BLINK_SEL register

Register Name	Description
PWR_ON_BLINK_SEL[1:0]	Select power on blinking time (T). 0x0: disable 0x1: 400ms 0x2: 800ms 0x3: 1.6s

Realtek confidential files
The document authorized to
瑞科
white@realytech.com.cn)

4.1.3. LED Port Number Selection

RTL9311BM support register COPR_PMASK[27:0], FIB_PMASK[27:0] to decide enable/disable port LED signal stream. Furthermore, Per-Port LED number can be selected by register configured. RTL9311BM also support combo port LED to distinguish from UTP port and Fiber port, when the PHY can work either on UTP mode or fiber mode. and LED_COMBO[27:0] decide whether copper/fiber status display on the same LED, as listed in table 15.

Table 12 LED_COPR_PMASK register

Name	Description
LED_COPR_PMASK [27:0]	Copper LED port mask. Mapping to physical port 27 ~ port 0.

Table 13 LED_FIB_PMASK register

Name	Description
LED_FIB_PMASK [27:0]	Fiber LED port mask. Mapping to physical port 27 ~ port 0.

Table 14 LED_NUM_SEL register

Name	Description
LED_NUM_SEL	Select LED number for each port. 0x0: 1 LEDs for each port. Pn_LED[0]. 0x1: 2 LEDs for each port. Pn_LED[1:0]. 0x2: 3 LEDs for each port. Pn_LED[2:0]. 0x3: 4 LEDs for each port. Pn_LED[3:0]. Note: This register must be select 3-LEDs in Bi-color scan LED mode.

Table 15 LED_COMBO_PMASK register

Name	Description
LED_COMBO_PMASK [27:0]	LED combo port selection. Mapping to physical port 27 ~ port 0. 0b0: Copper status display on copper LED, fiber status display on fiber LED. 0b1: Copper and fiber status display on same LED.

Realtek confidential files
The document authorized to
write(timelytech.com.cn)

4.1.4. Pin Assignments for LED

RTL9311BM provide 2 LED pins to connect with shift register in serial mode or RTL8231 in scan mode. The description of these two pins is listed in table 15.

Table 16 LED pin description

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_MDC	AJ4	O	12	(1) In Serial LED mode: Reference output clock for serial LED interface and Data is latched on the rising of LED_MDC. (2) In single color scan LED mode and bi-color scan LED mode: Reference output clock for MDC/MDIO interface.
LED_MDIO	AJ3	O	12	(1) In Serial LED mode: Serial bit stream of link status information. (2) In single color scan LED mode and bi-color scan LED mode: The data written to LED IC.

4.2. Serial LED mode

4.2.1. Serial LED Mode Setting

The serial LED interface, LED_MDC and LED_MDIO provide clock and data to enable/disable the external shift registers.

What should be take care is that these LED settings should be configured properly before LED mode selected.

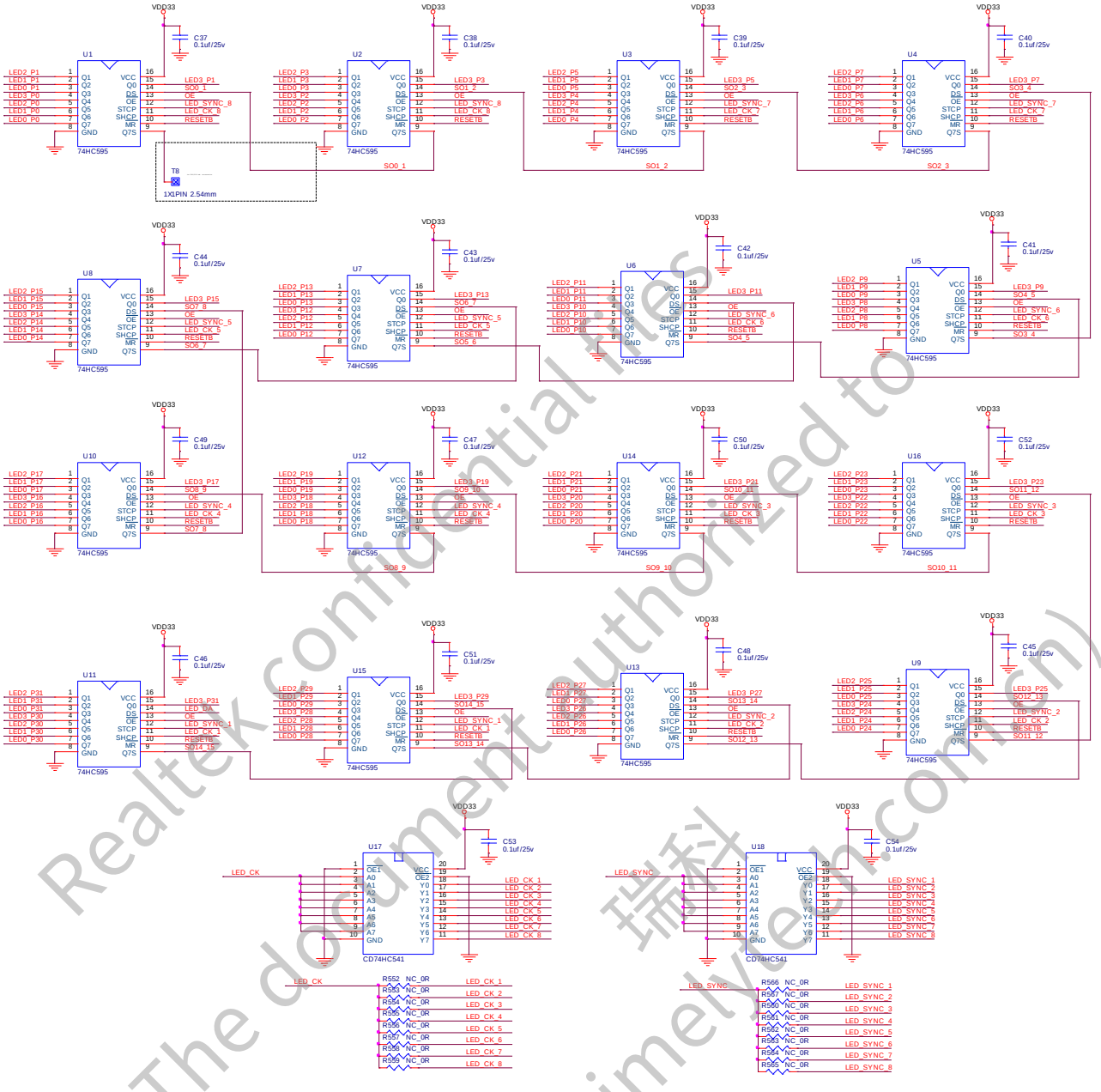
Table 17 Serial LED application

Application mode			LED_NUM_SEL	LED_COPR_PMASK	LED_FIB_PMASK	LED_COMBO_PMASK	Total LED
RTL9311BM	24G+4*10G combo	Per-port 4 LED	0x3	0xffffffff	0xffffffff	0xffffff	128
	24G+4*10G fiber	Per-port 4 LED	0x3	0xffffffff	0xffffffff	0xffffffff	112
		Per-port 3 LED	0x2	0xffffffff	0xffffffff	0xffffffff	84
		Per-port 2 LED	0x1	0xffffffff	0xffffffff	0xffffffff	56

4.2.2. Serial LED with 74HC595

A 74HC595 8−Bit Serial−Input/Serial or Parallel−Output Shift Register with Latched 3−State Outputs captures per-port link status and diagnostic information. The related circuit design for 24G+ 4*10G Combo mode with per-port 4 LED, as shown in figure 3. In non-combo port mode, those fiber LED and related 74HC595(U11 and U15 in figure 3) can be removed.

Realtek confidential files
The document authorized to
write(timely tech.com.cn)
瑞科



Realtek confidential files
The document authorized to
瑞科
white(timelyvcm.com.cn)

Figure 3. RTL9311BM 24G+ 4*10G Combo Serial LED Connection with 74HC595 Diagram

4.2.3. Serial LED with RTL8231

The RTL8231 shift register mode could reserve the serial data, and output parallel data in order. There are 36 shift registers in one RTL8231. The output data sequence is shown below:

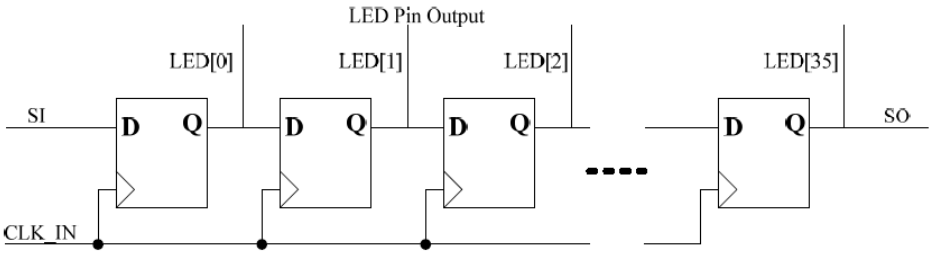


Figure 4. RTL8231 Shift Register Mode Logic Diagram

RTL8231 latches the current serial data which received at the SI pin and shift the preceding data to the next stage at the each rising edge of the serial clock. At the first serial data input, RTL8231 output from pin 15 LED[0]. At the last shift register, the serial data output from LED[35] pin and SO pin at the same time.

Strapping pins configuration of RTL8231 in shift register mode is depicted in table 6.

Table 18 RTL8231 Shift Register Mode Strapping Pins Configuration

Pin Name	Pin Number	Type	Description	Configuration for serial LED mode
LED[0]/Dis_SMI	15	I/O_{PD}	Select RTL8231 in the SMI mode or Shift Register mode. 0: SMI mode.(default) 1: Shift register mode.	Pull high
SO/MOD[1]	16	I/O	MOD[1] defines that application circuit is active high or low. 0: Low active 1: High active Note: internal floating. Must be pulled high or low to select the active high or active low application.	Pull low
LED[15]/MOD[0]	42	I/O_{PU}	MOD[0] defines the initial value is output high or low. 0: Output low after power on or hardware pin reset. 1: Output high after power on or hardware pin reset. (default)	Pull high

The related circuit design is shown in figure 5

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

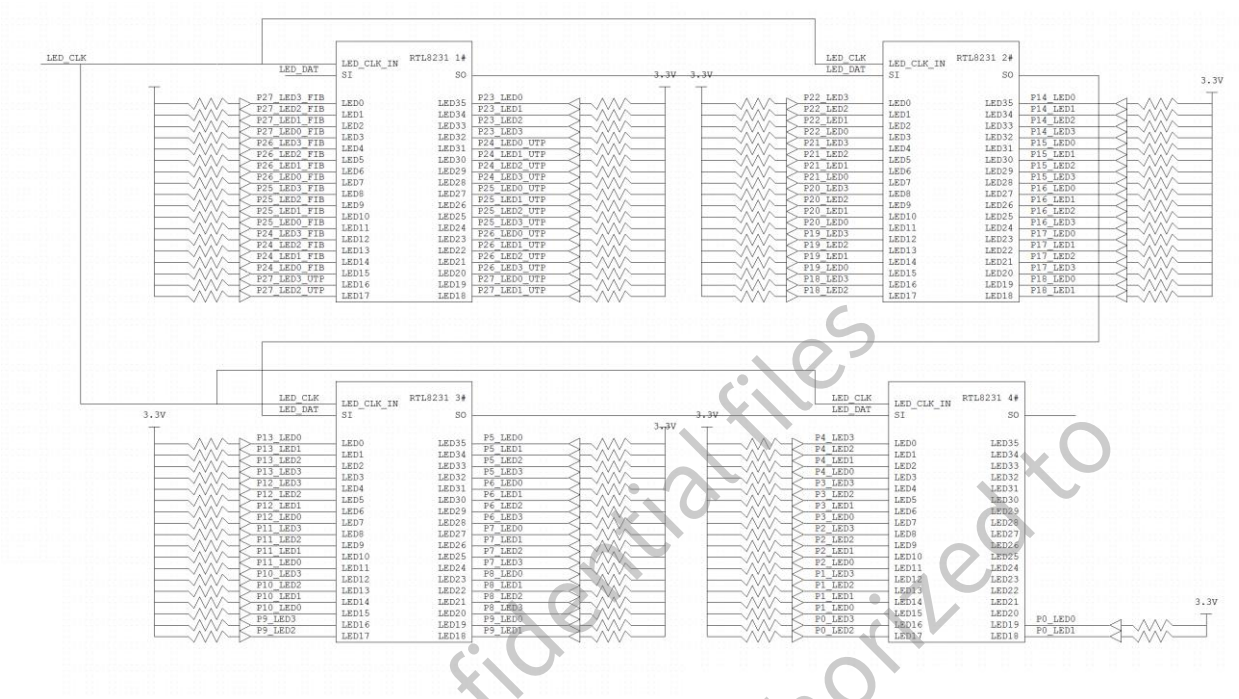


Figure 5. RTL9311BM 24G+ 4*10G Combo Serial LED Connection with RTL8231 Diagram

Figure 5 is an example of RTL8231 shift register mode for 24G+ 4*10G Combo with per-port 4 LED, totally 128 LED are used. In this case, four RTL8231 are needed, connect LED_CLK to both RTL8231 and connect the ahead RTL8231's SO to the next RTL8231's SI so that two RTL8231 can be combined together to form a 144 bits shift register, which is enough for 128 LED application. Same to more RTL8231 applications.

4.3. Scan LED mode

4.3.1. Scan LED Mode Setting

The RTL9311BM support scan LED by connecting with LED IC of the RTL8231, which provides single color and bi-color scan LED. The LED_CLK/ LED_DAT change to MDC/ MDIO interface mode and transmit MDC/ MDIO data to LED IC.

After power on or hardware reset, RTL9311BM initialize the RTL8231, and then write LED status to it to turn on/ off LED.

The strapping pins configuration of RTL8231 in SMI Mode is depicted in table 18.

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

Table 19 RTL8231 SMI Mode Strapping Pins Configuration

Pin Name	Pin Number	Type	Description	Configuration for I2C-like mode
GPIO[35]/Dis_SMI	15	I/O_{PD}	Select RTL8231 in the SMI mode or Shift Register mode. **0: SMI mode.(default)** 1: Shift register mode.	Pull low
SCAN_STAB0/Addr[0]	37	I/ O_{PU}	Addr[4:0] is Device ID. The first LED IC device address should be 0, and others are incrementally addressed;	Pull low
SCAN_STAB1/Addr[1]	38	I/ O_{PU}		Pull low
SCAN_STAB2/Addr[2]	39	I/ O_{PU}		Pull low
SCAN_STAB3/Addr[3]	40	I/ O_{PU}		Pull low
SCAN_STAB4/Addr[4]	41	I/ O_{PU}		Pull low
SCAN_STAB5/MOD[0]	42	I/ O_{PU}	When SMI mode is enable, **1: MDC/MDIO interface(default)** 0: I2C interface	Pull high

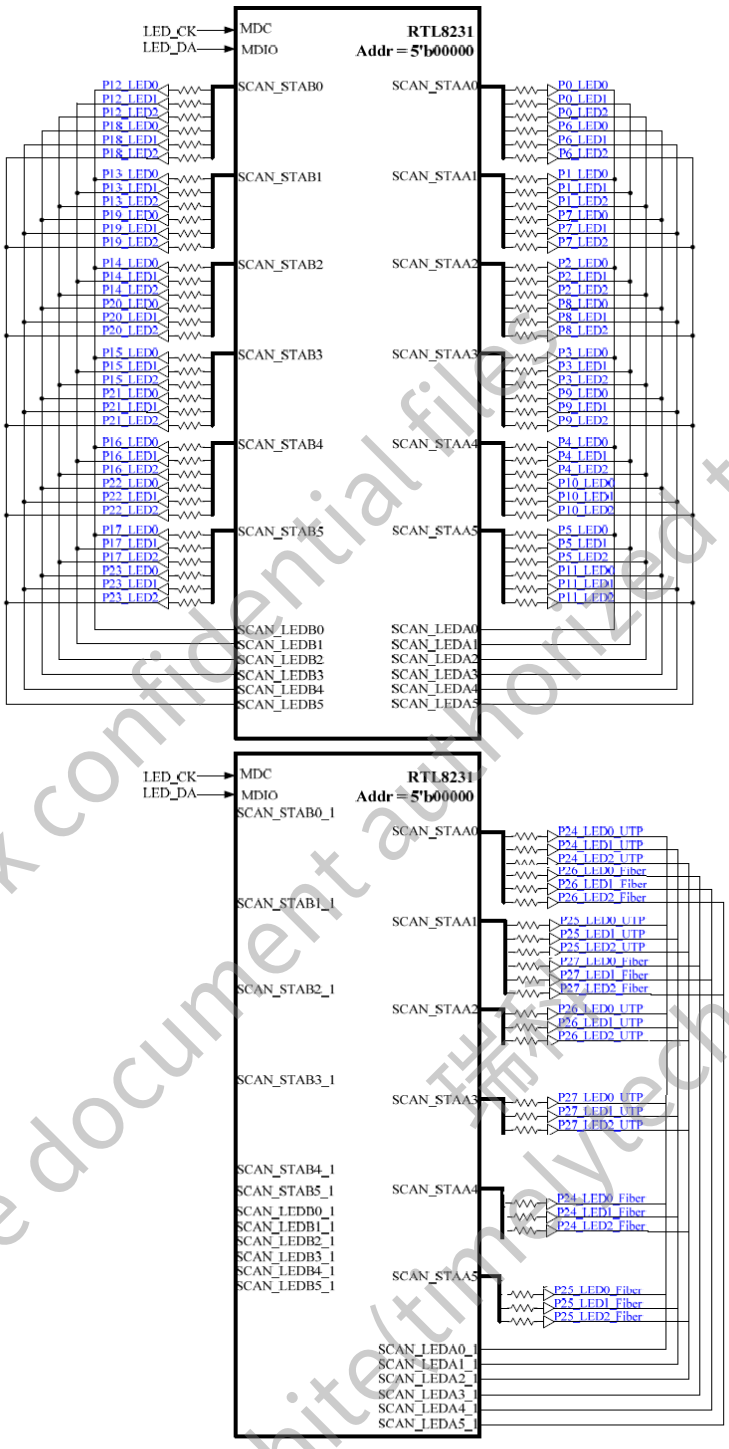
RTL8231 can support at most 72 single color LED in single color mode or 24 bi-color LED plus 24 single color LED in bi-color mode.

In the scan mode, RTL9311BM support at the most 4 single color LED or 1 bi-color plus 1 single color LED for each port.

4.3.2. Single color Scan LED application

Some related circuit design is shown below:

Realtek confidential files
The document authorized to white(timelytech.com.cn)
瑞科



Realtek confidential file
The document authorized to
white(timlytech.com.cn)

Figure 6. RTL9301 24G+ 4*10G Combo and per-port 3 LED circuit in single color scan mode

4.3.3. Bi-color Scan LED Application

In bi-color LED mode, a little difference from single color LED is that LED_NUM_SEL register must be select 3-LEDs.

The related circuit design is shown as below:

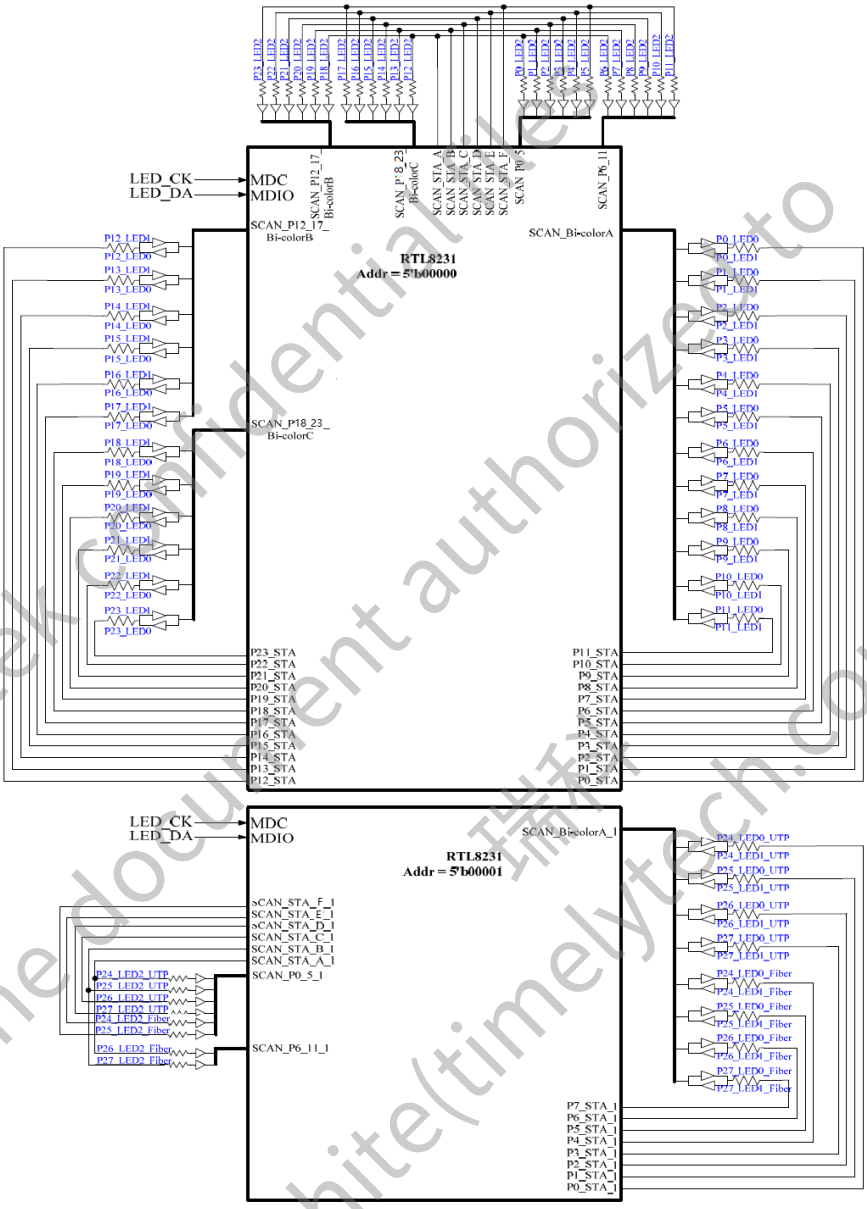


Figure 7. RTL9301 24G+ 4*10G Combo in Bi-color scan mode

Realtek Confidential - The document authorized to white(timelytech.com.cn)

5. SOC related Introduction

5.1. DDR/FLASH User Guide

5.1.1. SPI Nor Flash

The RTL9311BM supports a Maximum 64Mbyte SPI Nor Flash.
Features are shown below:

- Support both 3.3V and 1.8V
- Up to 100MHz
- Two chip select with up to 64MB

Table 20 SPI Nor Flash Recommend Model List

Manu.name	Model name	Note.
MXIC	MX25L25645G	3.3V,32MB
Winbond	W25Q256JVFQ	3.3V,32MB
XTX	XT25F256BSFIGU	3.3V,32MB
GD	GD25LB512MEFFRY	1.8V,64MB

5.1.2. SPI Nand Flash

The RTL9311BM supports a Maximum 512Mbyte SPI Nand Flash.
Features are shown below:

- Support both 3.3V and 1.8V
- Up to 100MHz (3.3V) / 50MHz (1.8V)
- Two chip select with up to 512MB

Table 21 SPI Nand Flash Recommend Model List

Manu.name	Model name	Note.
MXIC	MX35LF2G14AC	3.3V,256MB
	MX35LF4G24AD	3.3V,512MB
Winbond	W25N01GVZEIG	3.3V,128MB
Dosilicon	DS35Q4GM-IB	3.3V,512MB

Realtek confidential files
The document authorized to
瑞科
www.realtimelytech.com.cn)

5.1.3. Parallel Nand Flash

The RTL9311BM supports a Maximum 2Gbyte Parallel Nand Flash.

Features are shown below:

- Support both 3.3V and 1.8V
- Up to 50MHz (3.3V) / 33.3MHz (1.8V). Considering WE_N and OE_N as 1T
- Up to 2GB total for Parallel Nand Flash

Table 22 Parallel Nand Flash Recommend Model List

Manu.name	Model name	Note.
MXIC	MX30LF2G28AD	3.3V,256MB, TSOP48
MXIC	MX60LF8G28AD-TI	3.3V,1GB, TSOP48
Winbond	W29N08GVSIAA	3.3V,1GB, TSOP48
XTX	PN27G02BBGITG	3.3V,256M, BGA24

5.1.4. DDR

The RTL9311BM supports a Maximum 2G-Byte DDR3 SDRAMs, or 4G-Byte DDR4 SDRAMs.

Features are shown below:

- DDR3 / DDR4, 16-bit
- DDR4 Up to 1066MHz (data rate 2133) , DDR3 Up to 933MHz (data rate 1866)
- Support side-band ECC
- DDR4 Support up to 4GB, DDR3 Support up to 2GB
- DDR4 Support dual rank

Table 23 DDR4 Recommend Model List

Manu.name	Model name	Note.
SKhynix	H5ANAG6NCMR	16Gb
	H5AN8G6NDJR	8Gb
Nanya	NT5AD512M16C4	8Gb
	NT5AD256M16D4	4Gb

Table 24 DDR3 Recommend Model List

Manu.name	Model name	Note.
ISSI	IS43TR16K01S2AL	16Gb
Nanya	NT5CB256M16ER	4Gb

Realtek confidential files
Only the document authorized to
瑞科 (www.rumelytech.com.cn)

5.2. PCIe EP&RC User Guide

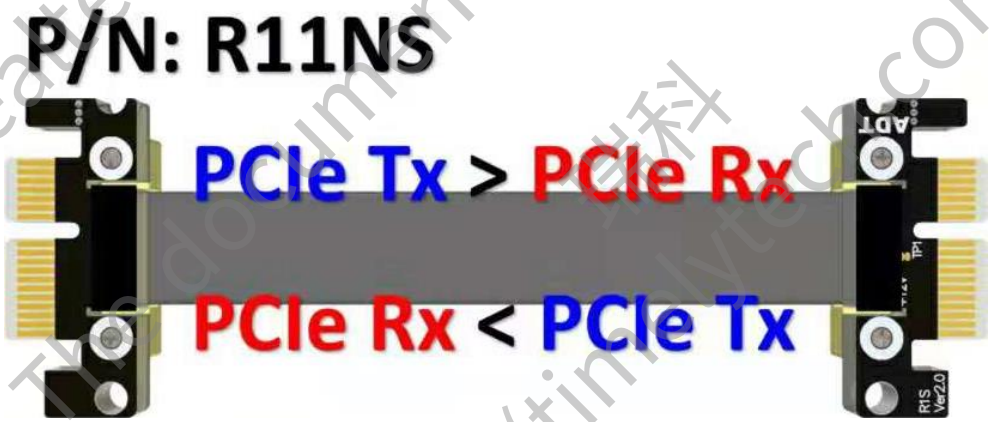
5.2.1. Mode select

可参考 2.1.3 节中，strap pin 的差异，EP mac 和 RC mac 会共用一颗 PHY，通过 strap pin SOC_PCIE_MODE_SEL[1:0]来选择 mode。

5.2.2. Design Note

- RTL9311BM 有专门处理 PCIE 的 PERSTN，有单独出 pin：PCIE_RST(AE2)。在 cascade 运用中，需将此 pin 对接，来实现 RC 对 EP 的 reset 操作。
- 除正常 TX/RX 信号对接外，PCIE_REFCLK_P/M 也许对接，RC 会提供 100M differential clock 给 EP。
- 当一块板子需要同时使用 EP/RC 两种 mode 时，由于 PCIE 接口不同，而 GEN2 速度在 5G，不一定能同时出两套接口，可选择外部 cable 进行接口转换。

  例如，目前 QA board 出的是 PCIe 母座，默认 RC mode，当要使用 EP mode 时，可通过如下 cable 将 PCIe 母座外接转换为金手指（cable 线需选择支持 gen2 的材质）：



5.2.3. GPIO application guide

Refer to RTL9311BM GPIO Application Note_0.1.doc

Realtek confidential files
The document authorized to
white(tinlvtech.com.cn)

6. Layout guide

6.1. General Design and Layout

In order to achieve maximum performance with the RTL9311BM, good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

6.1.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits. The following criteria are recommended; power noise of

  DVDDH/DVDDH_XSMI/AVDDH_BG/AVDDH_PLL/AVDDH_XTAL/SVDDH/SVDDH_SOC/VDDH_SOC/MVDDH should be under 30mV and power noise of SVDDL/SVDDL_CKx(x=0,1,2,3,4) should be under 20mV, power noise of AVDDL_BG/AVDDL_XTAL/AVDDL_PLL/SVDDL_SOC/SVDDL_PEX/DVDDL should be under 30mV
- Verify the critical components, such as clock source and transformer, to meet the application requirements
- Use bulk capacitors (4.7 µF-47 µF) between each power and ground plane
- Use 0.1 µF decoupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep decoupling capacitors as close as possible to the RTL9311BM
- Fill in unused areas of component side and solder side with solid copper and attach them with vias to the ground plane
- The IBREF pin of the RTL9311BM must connect to GND via a 2.49K +/- 1% ohm resistor. This resistor must be placed as close as possible to the RTL9311BM
- The LED_sync pin must use a 4.7K pull low external resistor to GND if used for 74HC595 ST_CP.
- Avoid right angle turns on all traces

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

6.1.2. Clock Circuits

- Place the crystal as close to the RTL9311BM as possible
- Surround clock traces with ground trace to minimize high-frequency emissions
- Use a 1.5K pull up external resistor to 3V3 for MDIO.
- Keep the MDC traces away from other signals
- Keep a clear area under the crystal or OSC component
- Ensure clock traces have an unbroken reference ground plane
- All clock traces should use a source termination scheme to reduce the signal reflection and EMI radiation
- Termination resistors must be as close to the driver side as possible

6.1.3. Power Planes

- Divide the power plane into 3.3V, 0.9V and 1.2V.

  3.3V power plane for DVDDH/DVDDH_XSMI/AVDDH_BG/AVDDH_PLL/AVDDH_XTAL/SVDDH/SVDDH_SOC/VDDH_SOC/MVDDH.

  0.9V power plane for AVDDL_BG/AVDDL_XTAL/AVDDL_PLL/SVDDL_SOC/ SVDDL_PEX/DVDDL/ SVDDL/SVDDL_CKx(x=0,1,2,3,4).

  1.2V power plane for MVDD/MVDD_CK.

  3.3V or 1.8V power plane for VDD_SPI/VDD_NAND
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and ground plane
- Use Pi filter for the power of SVDDL_CK

6.1.4. Ground Planes

- Keep the ground region under the RTL9311BM. Avoid too many breaches to achieve good heat conductive ability and a good signal return path

Realtek confidential files
The document authorized to white(timelytech.com.cn)

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board
- Place a moat (gap) between the system ground and chassis ground

6.1.5. Reset Circuit

At RTL9311BM side, we place a circuit of pull-high R 220K and 0.1uF to ground near the reset input pin to avoid noise trigger reset during system ESD test.

But if reset circuit design used AND-gate logic to implement combinational reset, it needs to take care the C load of AND-gate output if meets the AND-gate datasheet requirement. Normal C load requirement of AND-gate is pF order.

For example, if C load used 0.1uF will cause the AND-gate(74LVC08A) output has glitch signal, and has the risk of system boot-up fail.

6.1.6. Reserved GPIO for SFP+

While planning the RTL9311BM system design with SFP+, the LOS/SDA/SCL/MOD_ABS/TX_DIS pins of SFP+ connector must connect to GPIO pins.

- Connect GPIO to LOS pin:

  If CPU detect the LOS is low, it will execute 10G SerDes rx calibration to optimize 10G SerDes performance.

- Connect GPIO to SDA/SCL pins:

  It provides CPU to judge the fiber transceiver which plug-in is 1G or 10G mode since the SerDes parameters for these two transceivers is different.

- Connect GPIO to MOD_ABS pin:

  It provides the signal of fiber module present for CPU.

- Connect GPIO to TX_DISABLE pin:

  When Tx_Disable is asserted low or grounded the module transmitter is operating normally.

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

6.1.7. PWRMON Electrical Specification

RTL9311BM support OAM dying gasp function, and it monitor the voltage level of PWRMON pin to check if it meets OAM dying gasp conditions.
The electrical specification for PWRMON pins is shown below:

- Trigger condition: voltage is under 1.2V~ 1.25V
- Normal state: voltage must be above 1.55V, and in the range of 1.55V~3.3V

6.2. Serdes Layout Guidelines

As the SFI/XSGMII transmits over 10.3125Gbps/10.3125Gbps differential signal pairs, the PCB layout needs some attentions in order to meet layout guidelines. The following lists some important guidelines for layout of the SFI/XSGMII.

When using 2x2 or 2x1 SFP+ cage, please Refer to Chapter 6.2.3.

6.2.1. General Guidelines

- All SFI/XSGMII must be laid on the top side of a 4/6-layer or PCB, and cannot pass through a via
- Recommend ground shielding for Serdes TX & RX differential pairs. Clearance between signal and ground least 30mils in a 4-layer PCB
- As possible to space to all other signals be at least 30-mil in order to avoid harmful coupling issues in a 4-layer PCB (see Figure 8)

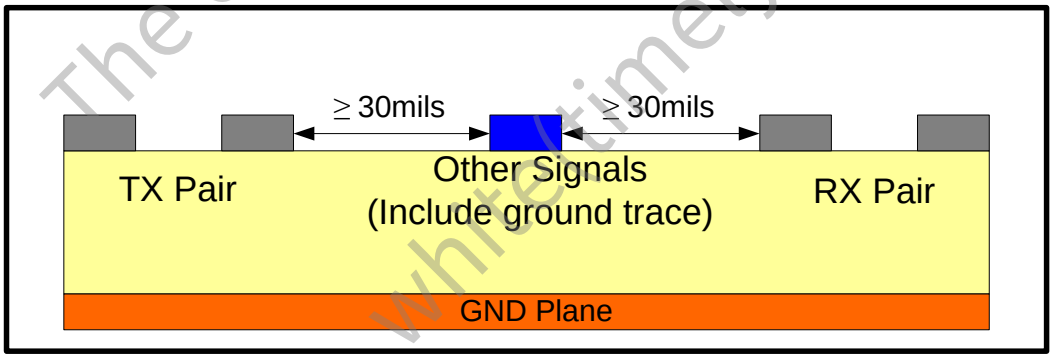


Figure 8. Trace Spacing Recommendation for a 4-Layer PCB

Realtek confidential files
The document authorized to
瑞科 (whf@timelytech.com.cn)

- Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible.

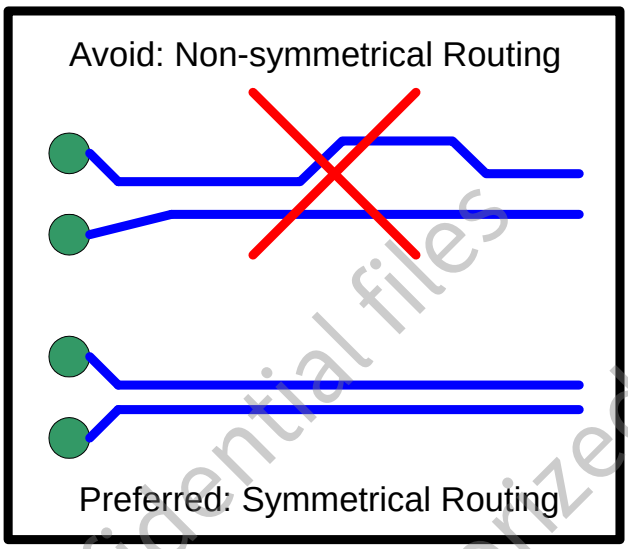


Figure 9. Symmetrical Routing

- Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiber glass bundle weaves and resin-rich areas of the dielectric

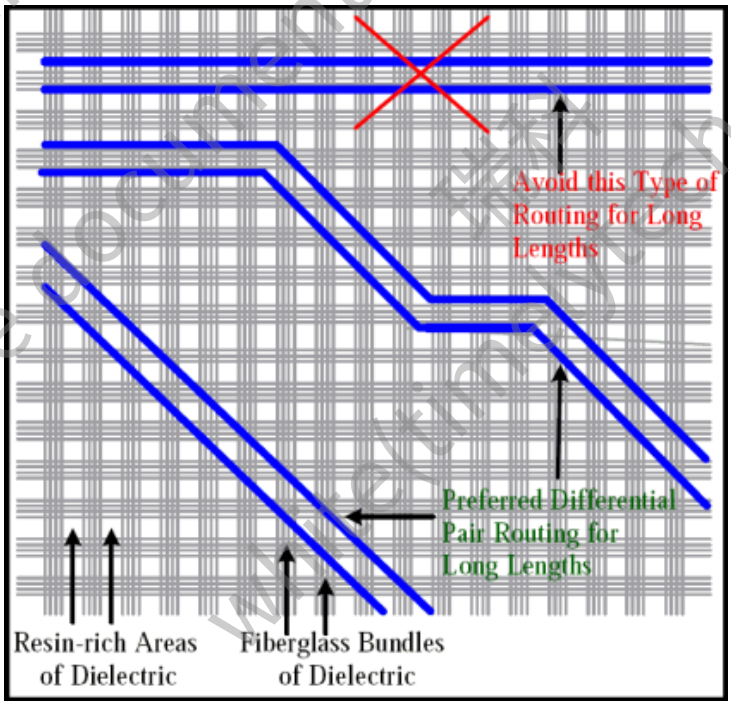


Figure 10. Long Trace Layout for Serdes

Realtek confidential files
The document is authorized to (...@realtek.com.cn)

- Differential pairs should have a continuous reference plane, and avoid via
- For XSGMII interface, size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL
- **For SFI** interface **to take account of** SFF-**8431 testing**, AC coupling capacitors are not needed
- Place AC coupling capacitors near output pins of differential pairs
- Locate capacitors for coupled traces at the same location along the differential traces

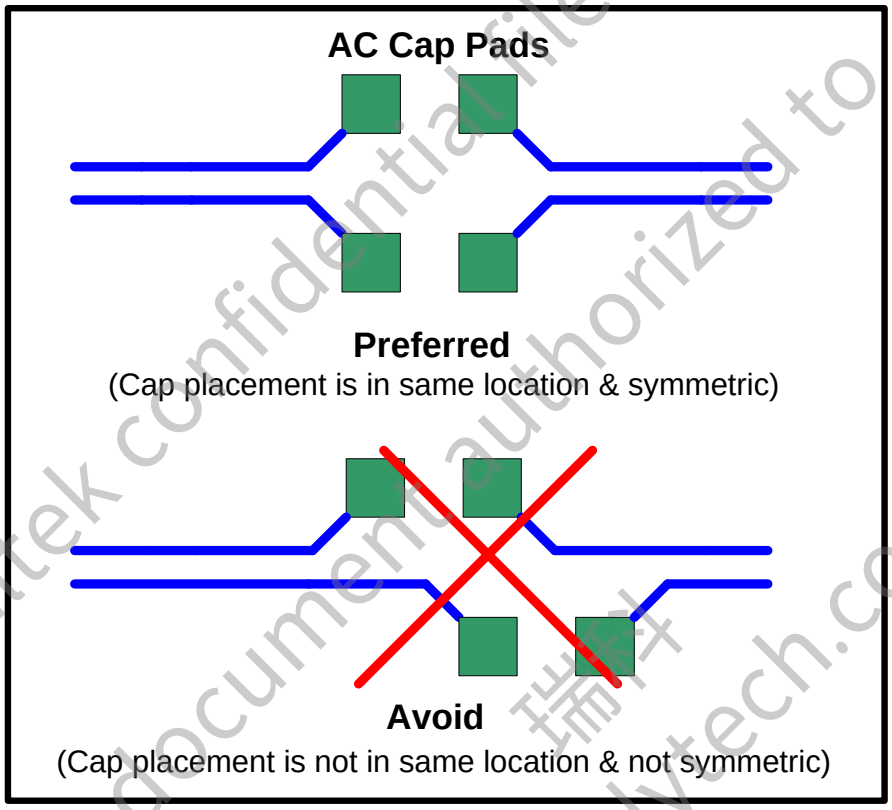


Figure 11. Symmetrical Routing Into AC Capacitors

Realtek confidential files
The document authorized to
white(timelytech.com.cn)
瑞科

6.2.2. SFI/XSGMII Layout Guidelines

- Differential pair impedance for SFI/XSGMII is 100Ω ± 10%
- SFI trace length is required to follow bellow rules for SFF-8431 testing:
  - SFI host interconnect budget SDD21 at 5.5GHz is between -6.5dB and -2.25dB (SDD21 is defined from chip pads to SFP+ connector). The minimum channel transfer SDD21 (maximum loss) is given by:

$$SDD21(dB) = -0.73 \quad \text{f from 0.01 GHz to 0.25 GHz}$$

$$SDD21(dB) = (-0.108 - 0.845 \times \sqrt{f} - 0.802 \times f) \quad \text{f from 0.25 GHz to 7 GHz}$$

$$SDD21(dB) = 20 - 4 \times f \quad \text{f from 7 GHz to 8 GHz}$$

$$SDD21(dB) \geq -16 \quad \text{f from 8 GHz to 11.1 GHz}$$

where *f* is the frequency in GHz.

- The reflection coefficients, SDD11and SDD22, of the SFI channel are recommend to meet following equations:

The reflection coefficients, SDD11 and SDD22, of the SFI channel are recommended to meet the following equations:

$$SDDxx(dB) \leq -14.5 \quad \text{f from 0.01 to 5 GHz}$$

$$SDDxx(dB) \leq -23.25 + 8.75 \times \left(\frac{f}{5}\right) \quad \text{f from 5 to 11.1 GHz}$$

where *f* is the frequency in GHz and SDDxx is either SDD11 or SDD22.

- SFI PCB trace length maximum is -inch in a 4-layer of normal FR4 PCB and recommend SFI PCB trace length is 3.5-inch for SFF-8431 testing

- XSGMII trace length is required to follow the bellow rule:
  - Trace length must between 1.5 inches and 15 inches in a 4-layer of normal FR4 PCB
- Connected to DAC, System link budget SDD21 at 5.15625G is greater than -20dB.
  - The recommended minimum channel transfer SDD21 of DAC is greater than -11dB.
  - The recommended maximum channel transfer SDDxx of DAC is less than -14dB.

  Application example: PCB TX: - 3dB + RX: -3dB + Connecter: -1dB + CABLE: -11dB + thermal/environmental margin: -2dB, Total: -20dB.
- Differential pairs P and N trace in substrate and PCB total mismatch cannot over 5mils for SFI interface (Connected to Fiber Module/DAC) or 30mils for XSGMII interface (Connected to other chip directly). If total length matched within 5 mils or 30mils, avoid serpentine routing. If total length matched over 5 mils or 30mils, serpentine routing is acceptable. The length matching compensation should be made as close as possible to the point where the length variation occurs, for example, near chip pins. Minimize the length of the serpentine sections as much as possible. SFI/ XSGMII trace

Realtek confidential files
The document authorized to
White(timelytech.com.cn)

length in substrate:

Table 25 SFI/ XSGMII trace length in substrate

Ball No.	Pin Name	Substrate Total Trace Skew Pos vs Neg (mil)
AH22	HSOP_S0	4.6
AJ22	HSON_S0	
AG23	HSIP_S0	0.07
AFG24	HSIN_S0	
AH25	HSOP_S1	4.63
AJ25	HSON_S1	
AG26	HSIP_S1	0.2
AG27	HSIN_S1	
AH28	HSOP_S2	4.63
AJ28	HSON_S2	
AG29	HSIP_S2	0.2
AF29	HSIN_S2	
AA27	HSOP_S3	-0.44
AB27	HSON_S3	
Y28	HSIP_S3	0.19
Y29	HSIN_S3	
V27	HSOP_S4	-0.41
W26	HSON_S4	
U28	HSIP_S4	0.02
U29	HSIN_S4	
R27	HSOP_S5	0.61
T27	HSON_S5	
P28	HSIP_S5	-0.4
P29	HSIN_S5	
M27	HSOP_S6	0.62
N27	HSON_S6	
L28	HSIP_S6	0.31
L29	HSIN_S6	
AA27	HSOP_S7	0.19
AB27	HSON_S7	
AD27	HSIP_S7	0.2
AE27	HSIN_S7	

Realtek confidential files
The document authorized to
瑞科
write(timelytech.com.cn)

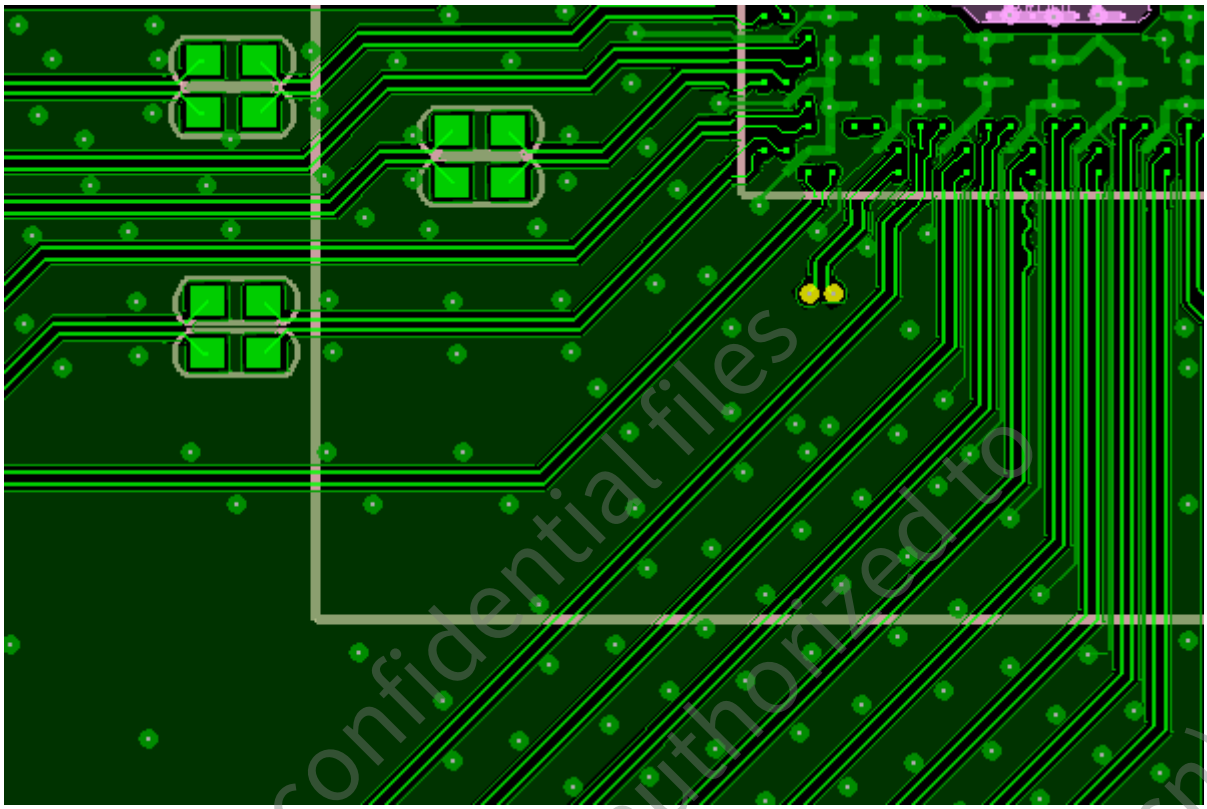


Figure 12. Length Matching and Compensation Example

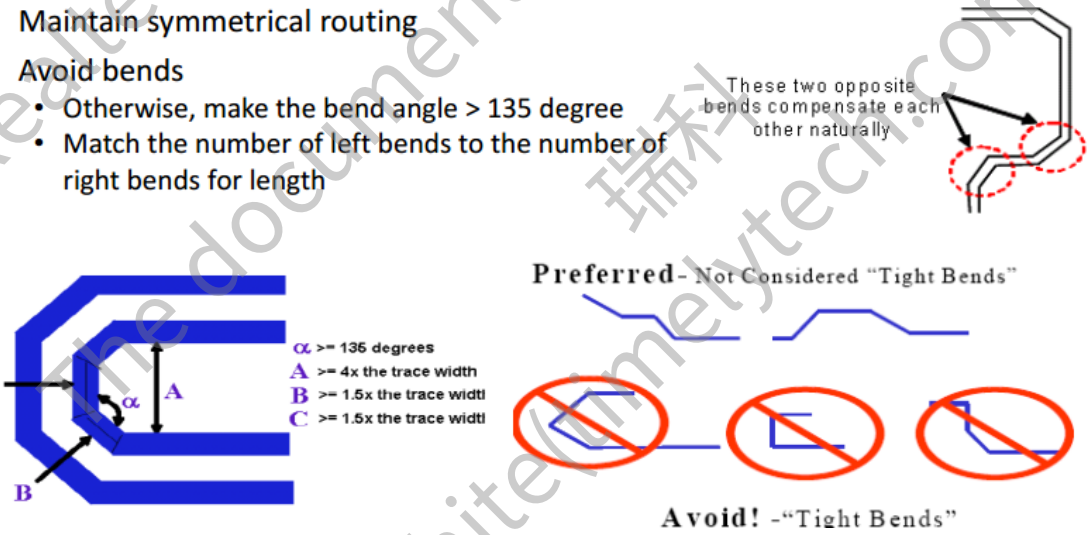


Figure 13. Bend Rule Example

- Recommend arc turn and oblique line for SFI/XSGMII trace
- Minimize impedance mismatch between transmission lines & mounting pads for SFI/XSGMII PCB layout:

Realtek confidential files
The document authorized to
white@realtek.com.cn)
瑞科

1. Use smallest mounting pad size if possible.
2. Partially void the reference layer (~60%) to reduce the capacitance. (see Figure 14)

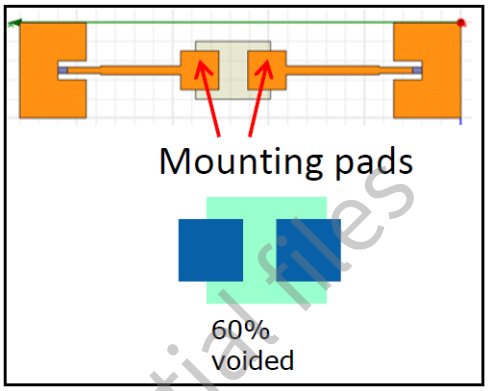


Figure 14. SFI Layout Rules for AC Coupling Capacitors

- The biggest discontinuity of impedance occurs at the connector; use ground voiding under the connector footprint to mitigate the effect. The void for tx & rx differential pair pins of SFP+ connector is shown in Figure 15

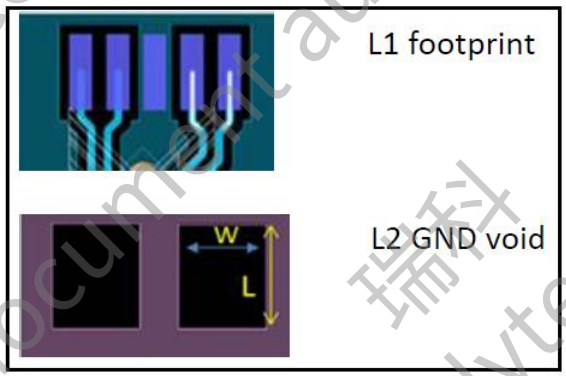


Figure 15. SFP+ Connector Footprint Voiding

6.2.3. Stacked SFP+ Connectors Layout Guidelines

RTL9311BR Demo board layout on FR4 4-layers PCB

- Trace routes from BGA-> Layer1 -> Vias -> Layer4 -> Connector

Realtek confidential files
The document authorized to write(timelytech.com.cn)
瑞科

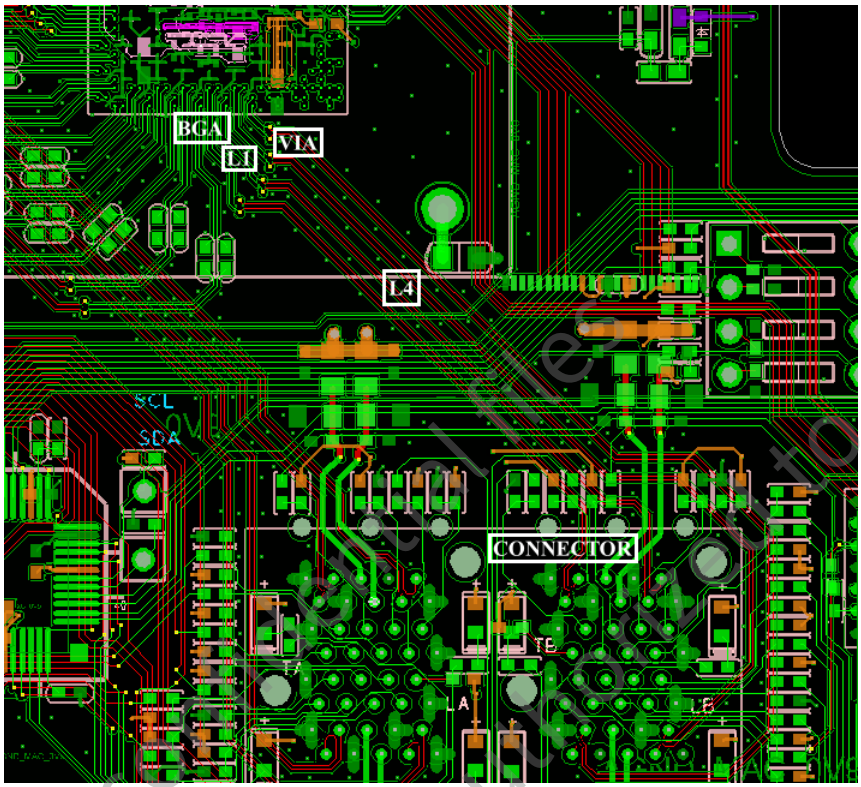


Figure 16. Stacked SFP+ Connector Layout on FR4 4-layer PCB

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

1. Route Differential pairs on bottom layer

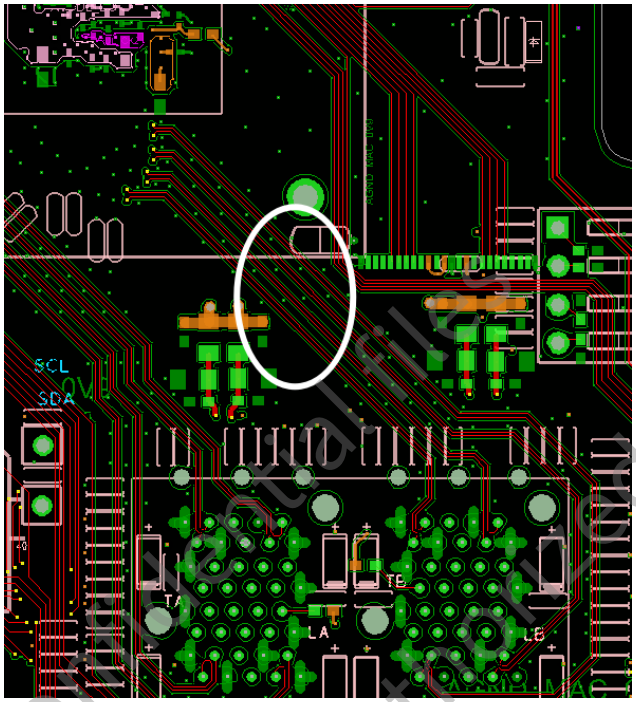


Figure 17. Differential pairs traces on L4

2. Diff. pairs on connector side, ring pad & L1

- Remove connector pin ring pad on inner layers.
- L1 (Top layer) pad void 40mils (1mm)

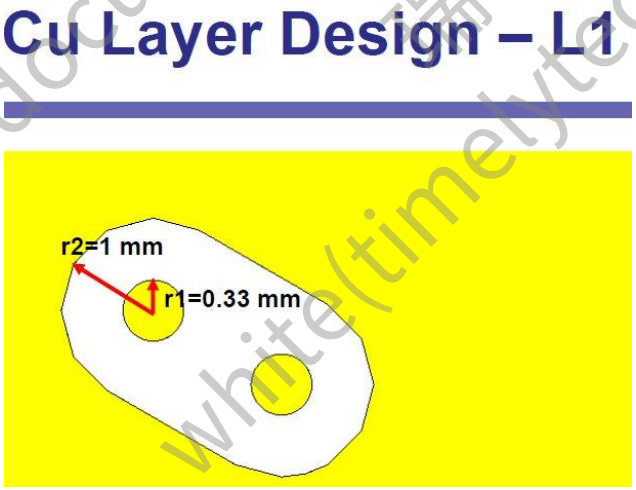


Figure 18. Diff. pairs on connector side, ring pad & L1

Realtek confidential files
The document authorized to white(timelytech.com.cn)

3. Diff. pairs on connector side, L2

- L2 pad void 40mils (1mm)

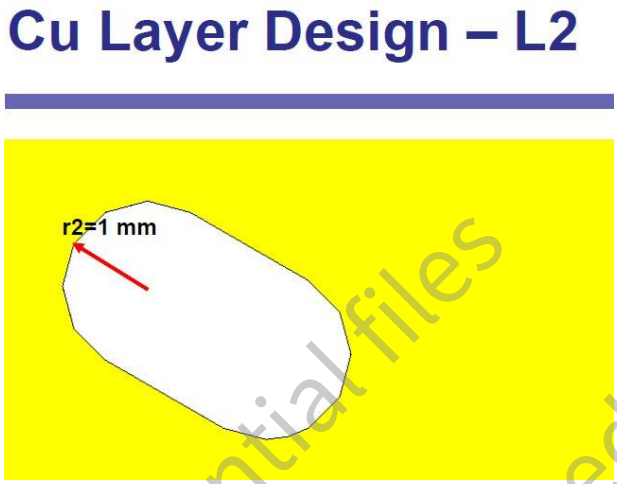


Figure 19. Diff. pairs on connector side, L2

4. Diff. pairs on connector side, L3

- L3 pad void 20mils (0.5mm)

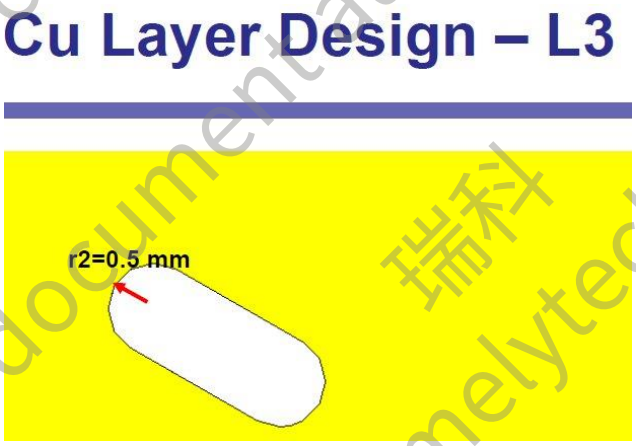


Figure 20. Diff. pairs on connector side, L3

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

5. Diff. pairs on connector side, L4

- L4 (bottom) pad void 44mils (1.1mm)

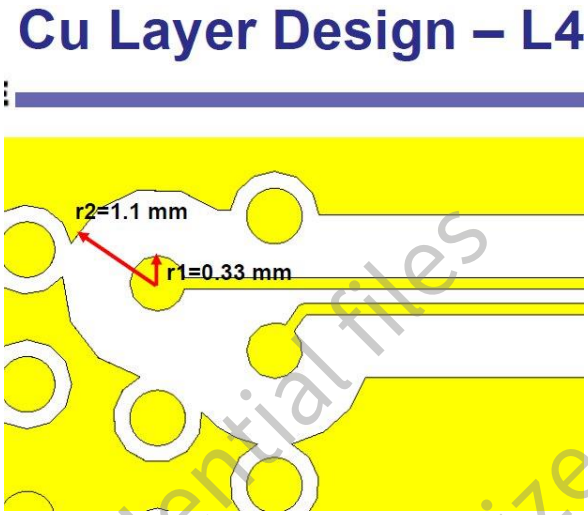


Figure 21. Diff. pairs on connector side, L4

6. Diff. pairs layer changing from top to bottom

- Via pitch 32mils (0.8mm)

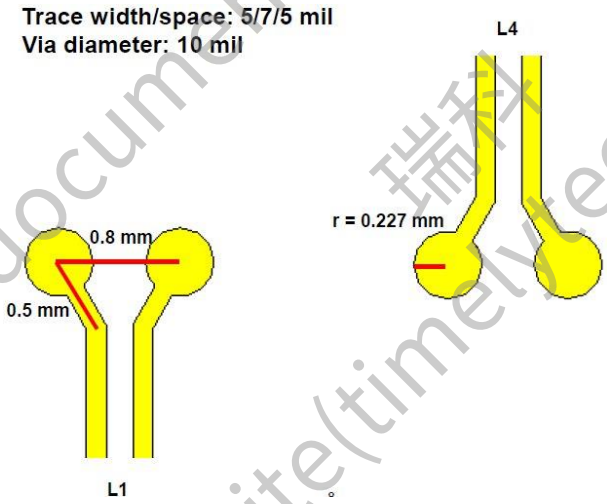


Figure 22. Diff. pairs layer changing from top to bottom

Realtek confidential files
The document authorized to
white(timelytech.com.cn)

7. Diff. pairs layer changing void

- Void 20mils (0.5mm) on inner layers

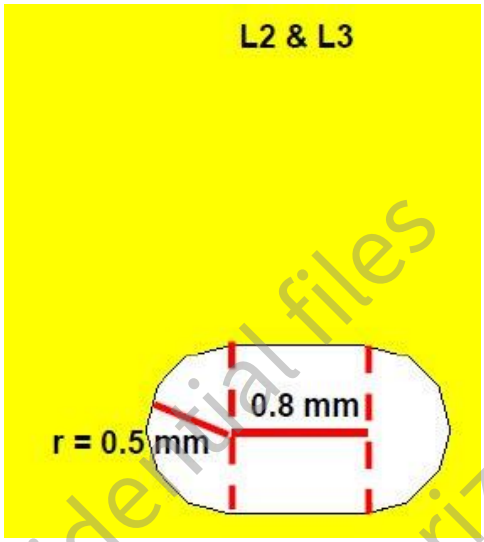


Figure 23. Diff. pairs layer changing void

8. Diff. pairs layer changing: GND stitching via

- Add symmetrical GND stitching vias as possible.

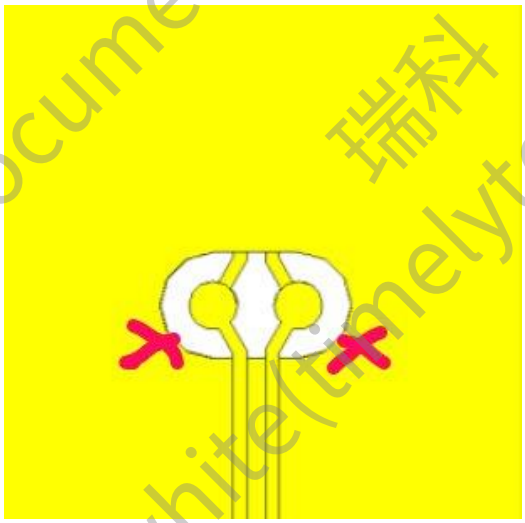


Figure 24. Diff. pairs on connector side, ring pad & L1

Realtek confidential files
The document authorized to
瑞科
White(timelytech.com.cn)

6.3. PCIe Layout Guidelines

Realtek PCI Express 2.0 PCB Differential Traces Design and Layout Guide.doc

6.4. USB Guidelines

- Differential pair impedance for USB is 90Ω ± 10%

Realtek USB 2.0 PCB Differential Traces Design and Layout Guide.doc

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

6.5. DDR4 PCB Layout Guidelines

- DDR4 will run up to 1066MHz. The following PCB layout guidelines should be followed
- DDR4 signal traces should be kept as short as possible
- The suggested longest trace length for DQ0-DQ15 / DM0 / DM1 / DQS0/N / DQS1/N is not over 1000-mil, allowing no more than a 300-mil delta between the lengths of DQ0-DQ15 / DM0 / DM1 and DQS0/N / DQS1/N
- The suggested longest trace length for A0-A16 / BA0-BA1 / BG0-BG1 / CLK/N / CLK1/N / CKE[0-3] / CSN[0-3] / PAR / TEN / ACTN / ODT0-ODT1 / ALERTN / RSTN is not over 5000-mil, allowing no more than a 1000-mil delta between the lengths of Address/Command and CLK/N
- Match the length of both sets of the differential pairs (CLK/N / CLK1/N / DQS0/N / DQS1/N), allowing no more than a 50-mil delta between the lengths of the P/N signals
- A0-A16 / BA0-BA1 / BG0-BG1 / CLK/N / CLK1/N / CKE[0-3] / CSN[0-3] / PAR / TEN / ACTN / ODT0-ODT1 / ALERTN / RSTN should use a source termination resistor
- Termination resistors must be as close to the driver side as possible
- Recommend differential-pair impedance is 100Ω±10%, single-ended impedance is 55Ω±10% in 4-layer PCB

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

- DDR4 (Single rank + ECC) layout reference for a 4-layer PCB:

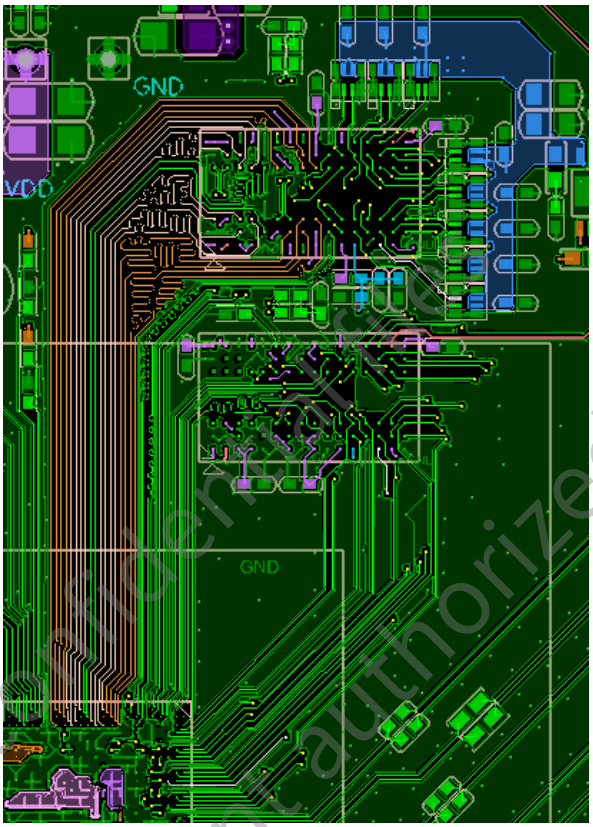


Figure 25. DDR4 Layout Reference for 4-Layer PCB

- The CK_P/N pins must be dealt as following figure to adjust the amplitude of CK_P/N and filter noise.

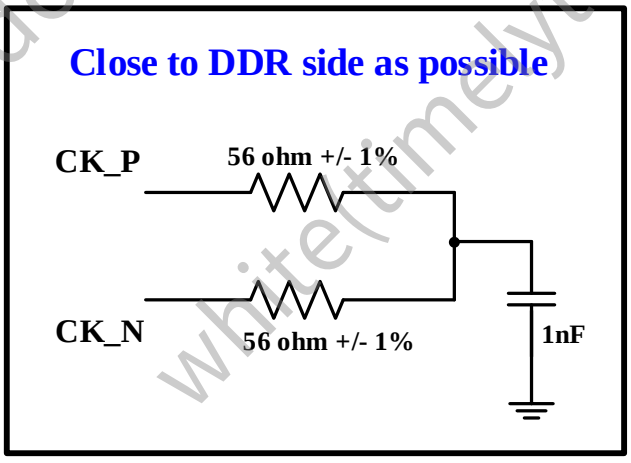


Figure 26. The Scheme for CK_P/N Pins

Realtek confidential
The document authorized to
瑞科
white(timelytech.com.cn)

6.6. DDR3 PCB Layout Guidelines

- DDR3 will run up to 933MHz. The following PCB layout guidelines should be followed
- DDR3 signal traces should be kept as short as possible
- The suggested longest trace length for DQ0-DQ15 / DM0 / DM1 / DQS0/N / DQS1/N is not over 1800-mil, allowing no more than a 700-mil delta between the lengths of DQ0-DQ15 / DM0 / DM1 and DQS0/N / DQS1/N
- The suggested longest trace length for A0-A15 / BA0-BA2 / CLK/N / CLK1/N / CKE[0-3] / CSN[0-3] / RAS# / CAS# / WE# / ODT0-ODT1 / RSTN is not over 3000-mil, allowing no more than a 1300-mil delta between the lengths of Address/Command and CLK/N
- Match the length of both sets of the differential pairs (CLK/N / CLK1/N / DQS0/N / DQS1/N), allowing no more than a 100-mil delta between the lengths of the P/N signals
- No more than a 1200-mil delta between the lengths of DQS0/N / DQS1/N and CLK/N / CLK1/N is suggested
- A0-A16 / BA0-BA1 / BG0-BG1 / CLK/N / CLK1/N / CKE[0-3] / CSN[0-3] / RAS# / CAS# / WE# / ODT0-ODT1 should use a source termination resistor
- Termination resistors must be as close to the driver side as possible
- Recommend differential-pair impedance is 100Ω±10%, single-ended impedance is 55Ω±10% in 4-layer PCB

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

- DDR3 (Single rank + ECC) layout reference for a 4-layer PCB:

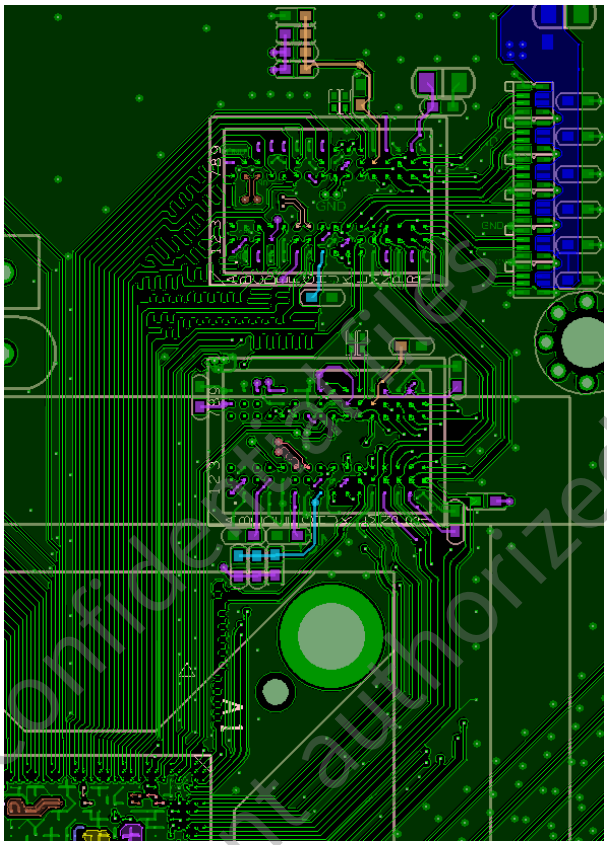


Figure 27. DDR3 Layout Reference for 4-Layer PCB

- The CK_P/N pins must be dealt as following figure to adjust the amplitude of CK_P/N and filter noise.

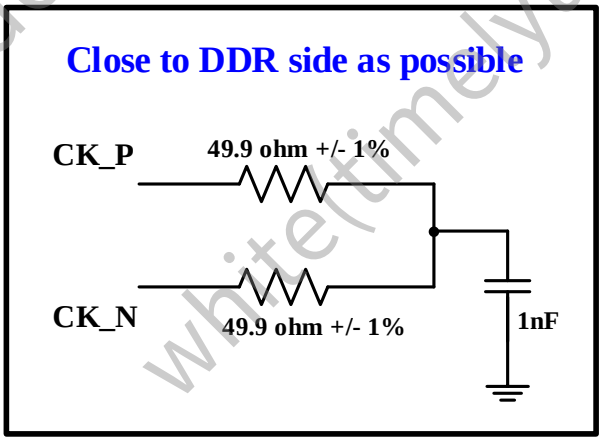


Figure 28. The Scheme for CK_P/N Pins

Realtek confidential files
The document authorized to
瑞科
white(timelytech.com.cn)

6.7. ESD/EMI Design Guide

- Merge Fiber_Cage_GND with System_GND together(See Figure 29) will improve its ESD performance.

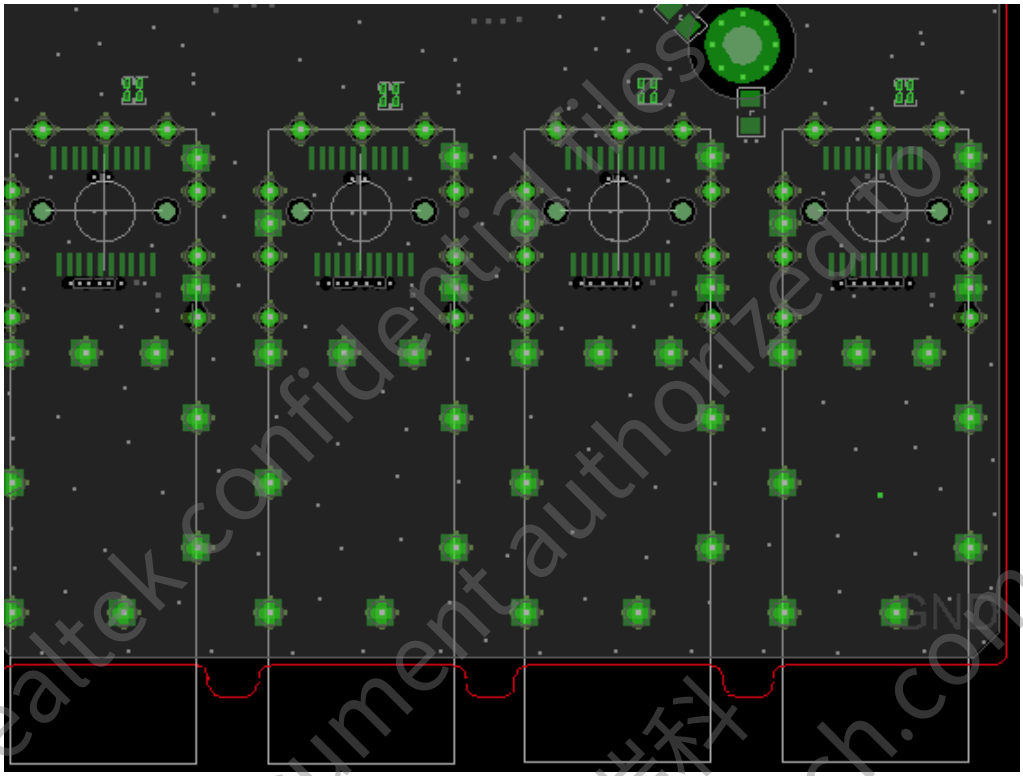


Figure 29. GND plane on Layer 2 in 4-layer PCB for Fiber

Realtek confidential files
The document authorized to white(timelytech.com.cn)

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com