

REALTEK

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RTL9000BF/BN/BR/BS/BSS

INTEGRATED PRECISION AUTOMOTIVE PHY WITH 100BASE-T1 TRANSCEIVER

DATASHEET

Rev. 1.0

21 December 2021

Track ID: JATR-8275-15



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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2021/12/21	First release.

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1. General Description

The RTL9000BF/BN/BR/BS/BSS is a highly integrated automotive transceiver that is compatible with IEEE 802.3bw 100BASE-T1 standards, including auto-negotiation and OAM features. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over single Unshielded Twisted Pair (UTP) cable for Automotive Electronics.

Data transfer between Medium Access Control (MAC) and the RTL9000BF/BN/BR/BS/BSS PHY is via the Media Independent Interface (MII), Reduced Media Independent Interface (RMII), Reduced Gigabit Media Independent Interface (RGMII) or Serial Gigabit Media Independent Interface (SGMII). The RTL9000BF/BN/BR support 3.3V/2.5V/1.8V I/O signaling of MII/RMII/RGMII. The RTL9000BF/BS/BSS supports the signaling of SGMII. The INTB/DISB/PHYRSTB pins of the RTL9000BF/BN/BR/BS/BSS that are connected with the microcontroller are 5V-friendly.

The RTL9000BF/BR/BS supports the behavior of the OPEN Alliance TC10 Sleep/Wake function for automotive Ethernet. The Sleep function implements the PHY into the Sleep mode, which has lower power consumption. The Wake function can allow the PHY to be efficiently woken up to the normal operating mode from Sleep mode.

The RTL9000BF/BN/BR/BS/BSS provides full hardware support for high-precision clock synchronization based on the Precision Time Protocol (PTP) of the IEEE 1588 and 802.1AS standards. The integrated PTP functionality accurately timestamps each PTP packet on the Tx/Rx path, and the upper layer software can take this timing information to determine the timing offset to the 1588 master clock. The device also provides General Purpose Input/Output (GPIO) as the PTP application interface. Besides, the integrated extended PTP parser support PTP message with VLAN tag and domain number in PTP header.

The RTL9000BF/BN/BR/BS/BSS uses state-of-the-art Digital Signal Processor (DSP) technology and an Analog Front End (AFE) to enable robust and high-speed data transmission and reception. It offers high Electro-Static Discharge (ESD) protection as well as excellent Electromagnetic Compatibility (EMC) performance. The Under-voltage and Temperature monitoring built into the RTL9000BF/BN/BR/BS/BSS will continuously monitor the operating condition of the chip, take corresponding action, and show status or error information to the upper layer.

2. Features

● 100BASE-T1 Transceiver

- ◆ Compatible with 100BASE-T1 IEEE 802.3bw standards over single-pair copper cable
- ◆ Data transfer up to 100Mbps
- ◆ Rapid link-up time (< 100ms)
- ◆ Full-duplex supported
- ◆ Auto-negotiation.

● Interfaces

- ◆ Supports MII/RMII/RGMII with optional internal delay on Tx and Rx path
(RTL9000BF/BN/BR Only)
- ◆ Supports SGMII.**(RTL9000BF/BS/BSS Only)**
- ◆ High-speed MDC/MDIO interface
- ◆ Supports I/O power as 1.8V/2.5V/3.3V
- ◆ Interrupt notifications
- ◆ PTP GPIO

● Power Supply

- ◆ Embedded LDO that switches voltages and provides 0.9V power for digital/analog core power

● Clocking

- ◆ Supports 25MHz crystal /external clock

● Power Saving

- ◆ Open Alliance Standard Sleep mechanism
(RTL9000BF/BR/BS Only)
- ◆ Ultra-low power consumption during Sleep mode (typical: 9 μ A)
(RTL9000BF/BR/BS Only)
- ◆ Supports Remote/Local Wake-up

● Precision Time Protocol (PTP)

- ◆ Support for Precision Time Protocol, including IEEE1588v1, v2, and 802.1AS
- ◆ PTP Packet parser supports Layer 2 Ethernet, IPv4/UDP, IPv6/UDP packets
- ◆ One-Step operation supported
- ◆ Support ingress timestamp insertion
- ◆ Adjustable PTP clock for synchronization
- ◆ 15ns timestamp resolution
- ◆ Deterministic and low transmission latency for PTP mechanism
- ◆ Programmable Time Application Interfaces through the PTP GPIO
- ◆ Selectable PTP clock input from the external reference clock source
- ◆ Extended PTP parser
- ◆ Supports PTP message with VLAN tag
- ◆ Supports Domain number in PTP header

● Performance

- ◆ Conforms to AEC-Q100 Grade 1 (-40~125°C)
- ◆ Low Electro-Magnetic Emission (EMC)
- ◆ HBM ESD protection level: ±6KV for all pins
- ◆ Open Alliance EMC Test Contact discharge: E-Gun - MDIP, MDIN±6KV for MDI pins: ±6KV
- ◆ MDI pins are tolerant of transient conditions according to ISO 7637 class C
- ◆ Supports at least 15m for single-pair cable
- ◆ Echo Cancellation mechanism

- **Diagnostics**

- ◆ Realtek Cable Test Diagnostics (RTCT) detects open/short status and distance of the cable (resolution: ±1m) and status indication
- ◆ Under-voltage detection
- ◆ Over-temperature detection
- ◆ IEEE 1149.1 JTAG testing and Built-In Self-Test (BIST) mode supported
- ◆ Open Alliance TC1 Signal Quality Index (SQI)

- **Process and Packages**

- ◆ 28nm LP process
- ◆ RTL9000BF: 48-pin QFN package(7*7)
- ◆ RTL9000BN: 36-pin QFN package(6*6)
- ◆ RTL9000BR: 32-pin QFN package(5*5)
- ◆ RTL9000BS: 32-pin QFN package(5*5)
- ◆ RTL9000BSS: 24-pin QFN package(4*4)

3. Device Comparison Table

Table 1. Device Comparison Table

Product	RTL9000BF	RTL9000BN	RTL9000BR	RTL9000BS	RTL9000BSS
Package Size	7x7	6x6	5x5	5x5	4x4
Package Type	QFN 48	QFN 36	QFN 32	QFN 32	QFN 24
MII/RMII	Yes	Yes	Yes	No	No
RGMII	Yes	Yes	Yes	No	No
SGMII	Yes	No	No	Yes	Yes
Wake Up Compliant	Yes	Yes	Yes	Yes	Yes
TC10 Deep Sleep Mode	Yes	No	Yes	Yes	No

4. Application Diagrams

4.1. General Application Diagram

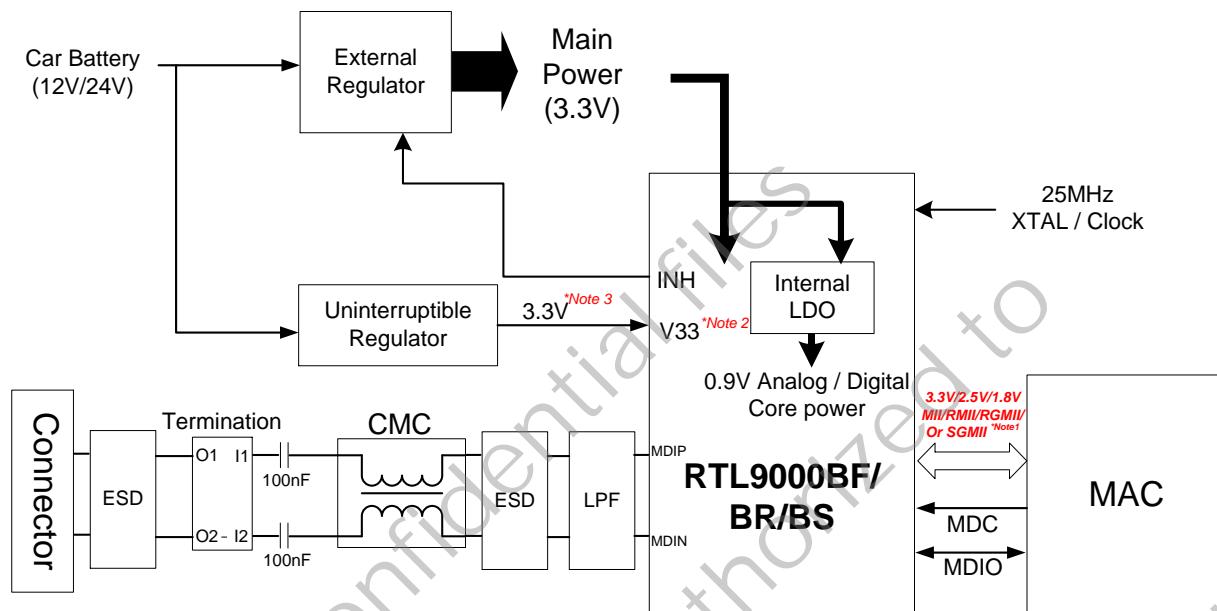


Figure 1. RTL9000BF/BR/BS General Application Diagram

Note 1: Availability of the MII interface with MAC depends on the product.

Note2: For more information on these applications, refer to “Sleep mode” in section 8.4.1 Operating Modes, page 23. The RTL9000BN/BSS does not support “Deep Sleep Mode”.

Note3: The independent 3.3V should always be supplied for fulfilling TC10 requirements. If the application does not support TC10, V33 can be supplied by Main Power(3.3V).

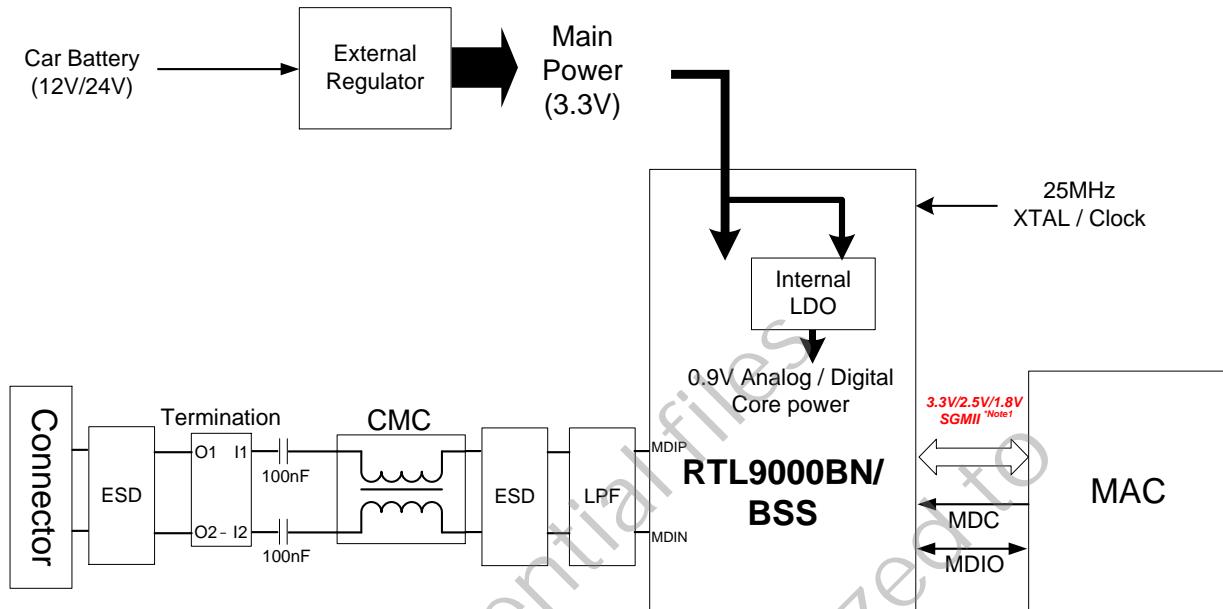


Figure 2. RTL9000BN/BSS General Application Diagram

4.2. PTP Application Diagram

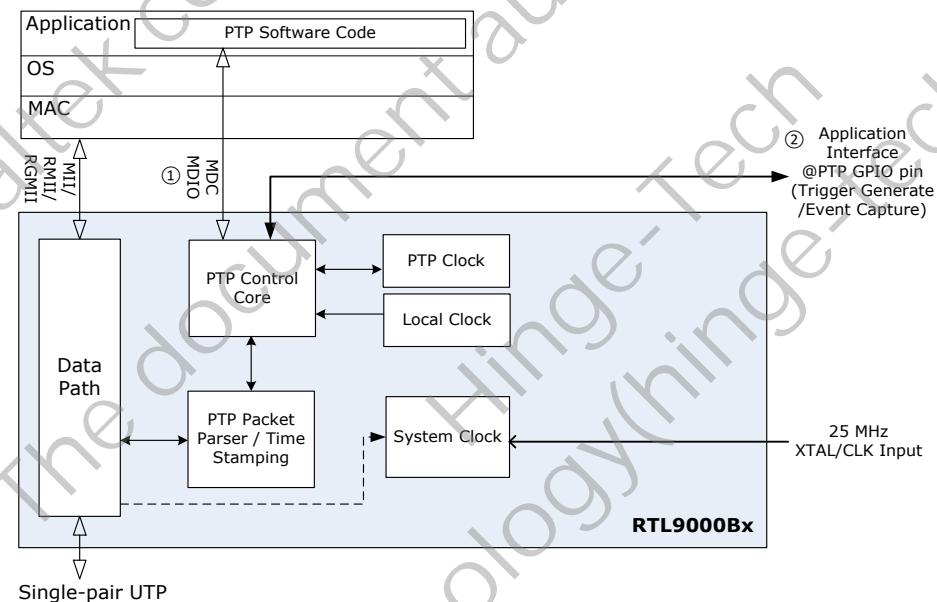


Figure 3. PTP Application Diagram

Note 1: By setting the PTP registers through the MDIO interface, the local PTP clock can be adjusted and synchronized according to the timing offset calculated by the upper layer software

Note 2: A PTP GPIO provides Time Application Interfaces (TAI) to upper layer or external utilization. The TAI include Trigger Generate (supports periodic trigger with nanosec-level jitter) and Event Capture functions.

5. Block Diagram

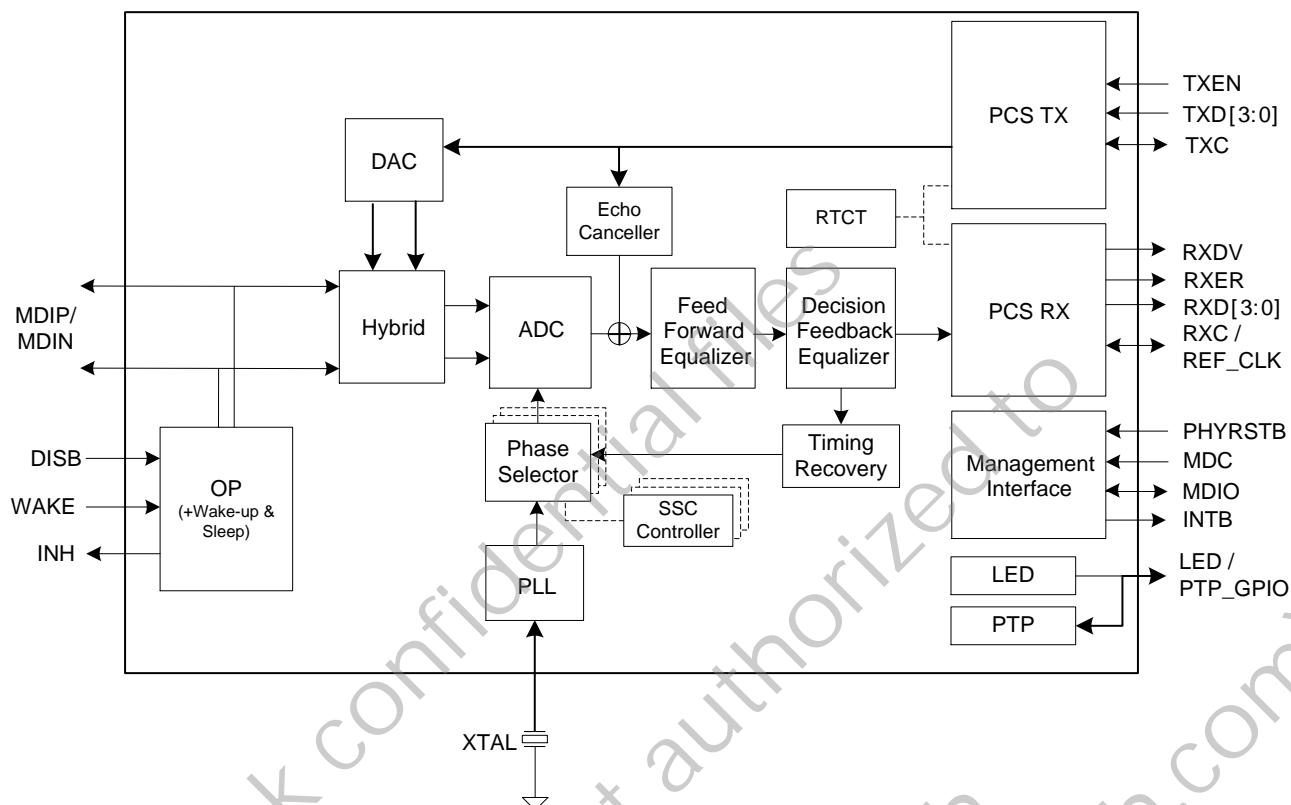


Figure 4. Block Diagram

6. Pin Assignments

6.1. RTL9000BF (QFN-48)

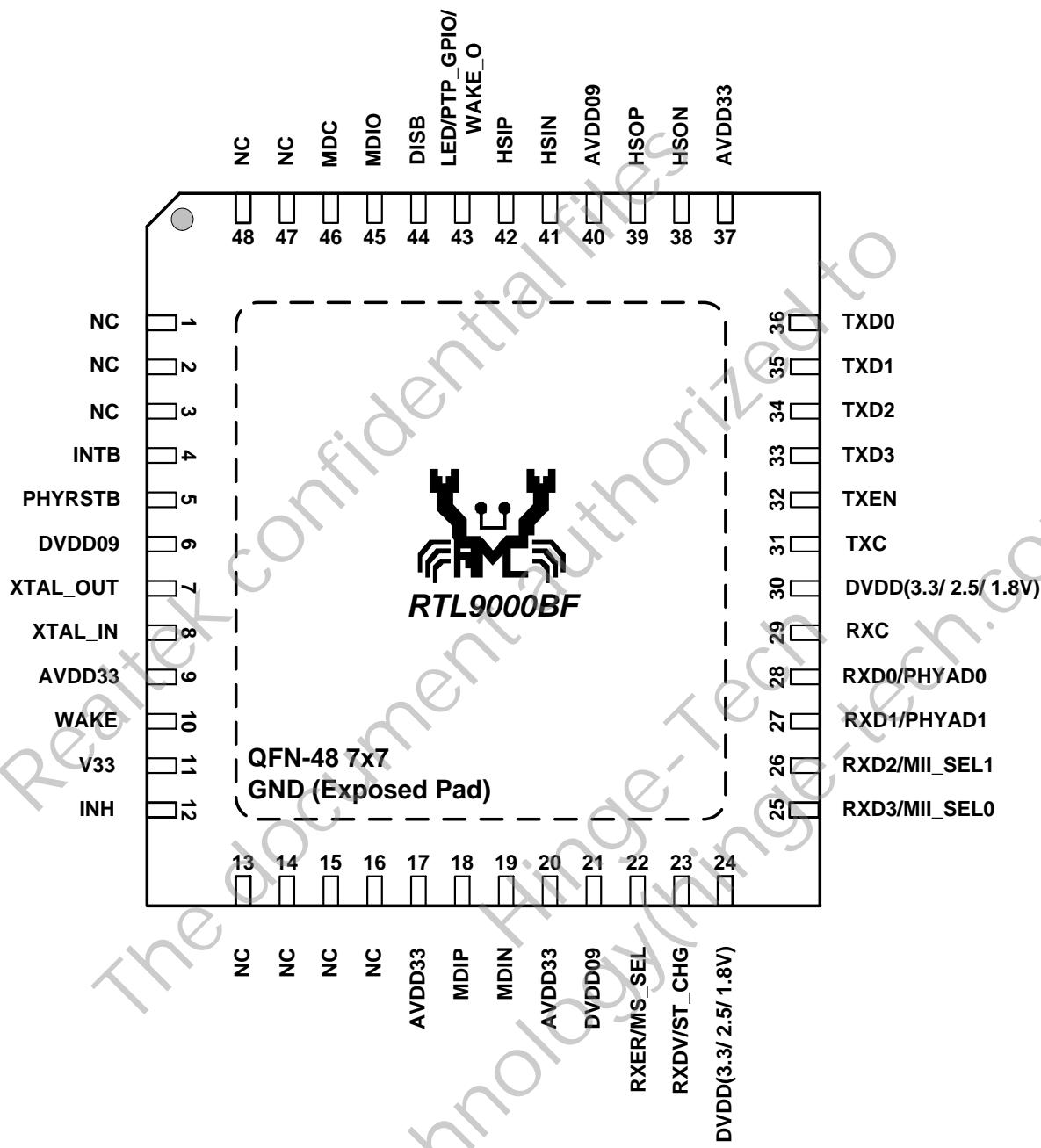


Figure 5. RTL9000BF Pin Assignments (QFN-48)

6.2. RTL9000BN (QFN-36)

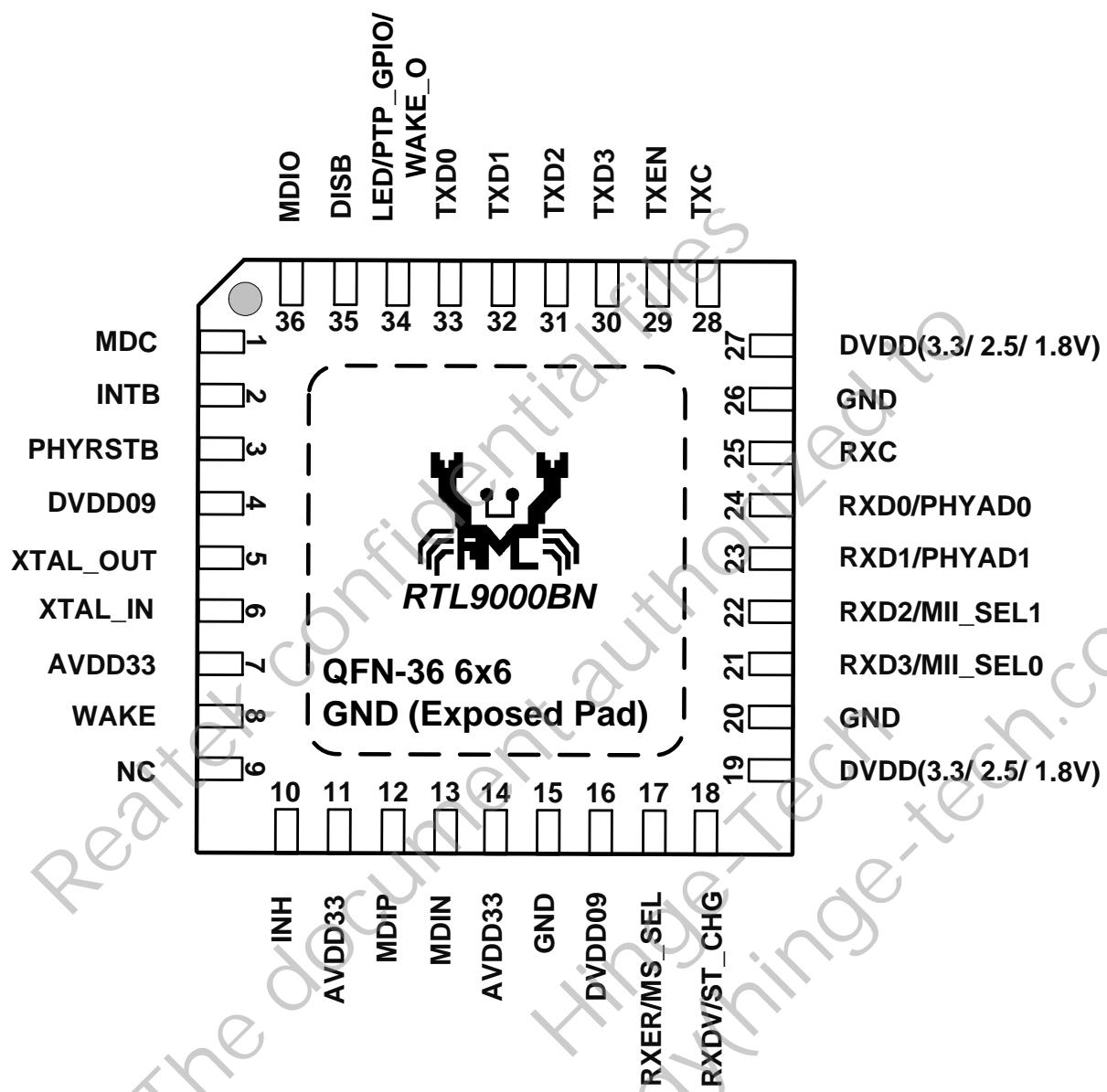


Figure 6. RTL9000BN Pin Assignments (QFN-36)

6.3. RTL9000BR (QFN-32)

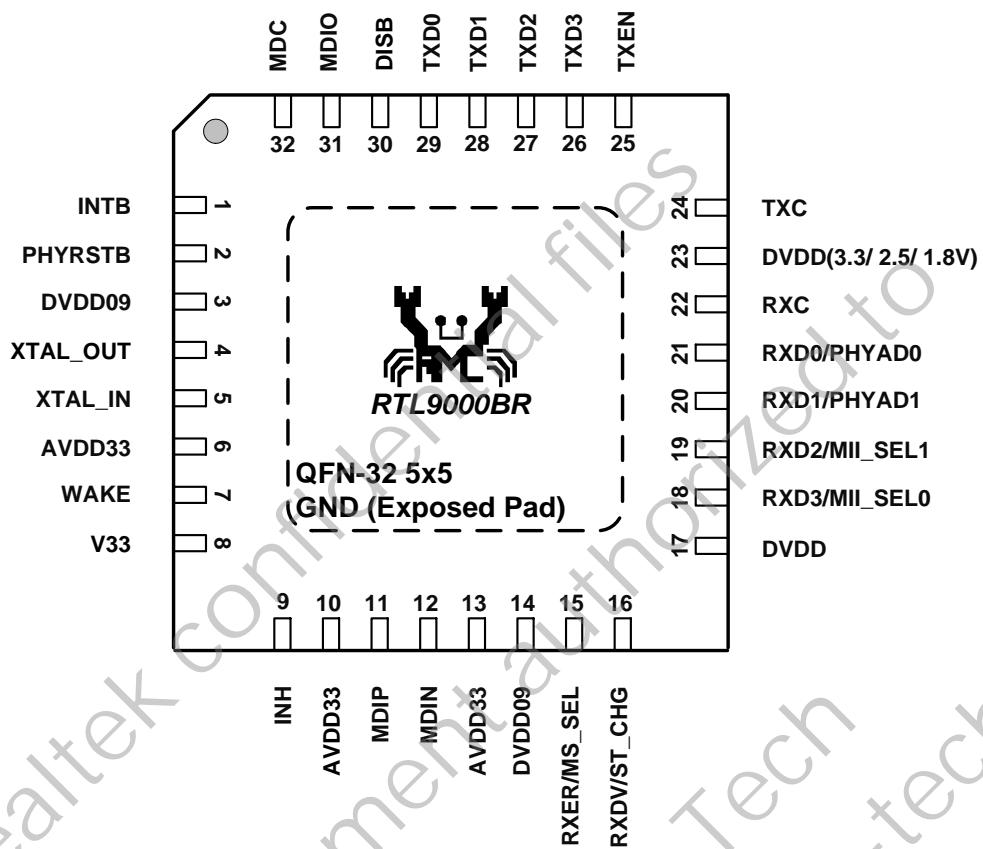


Figure 7. RTL9000BR Pin Assignments (QFN-32)

6.4. RTL9000BS (QFN-32)

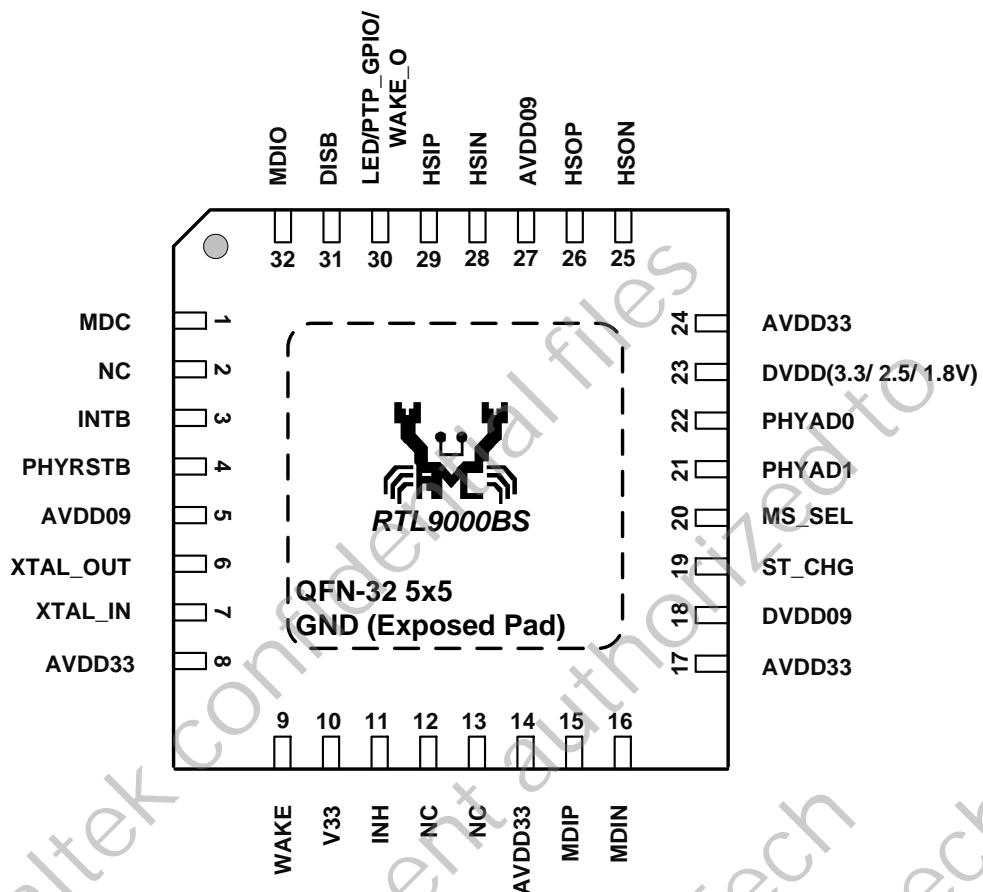


Figure 8. RTL9000BS Pin Assignments (QFN-32)

6.5. RTL9000BSS (QFN-24)

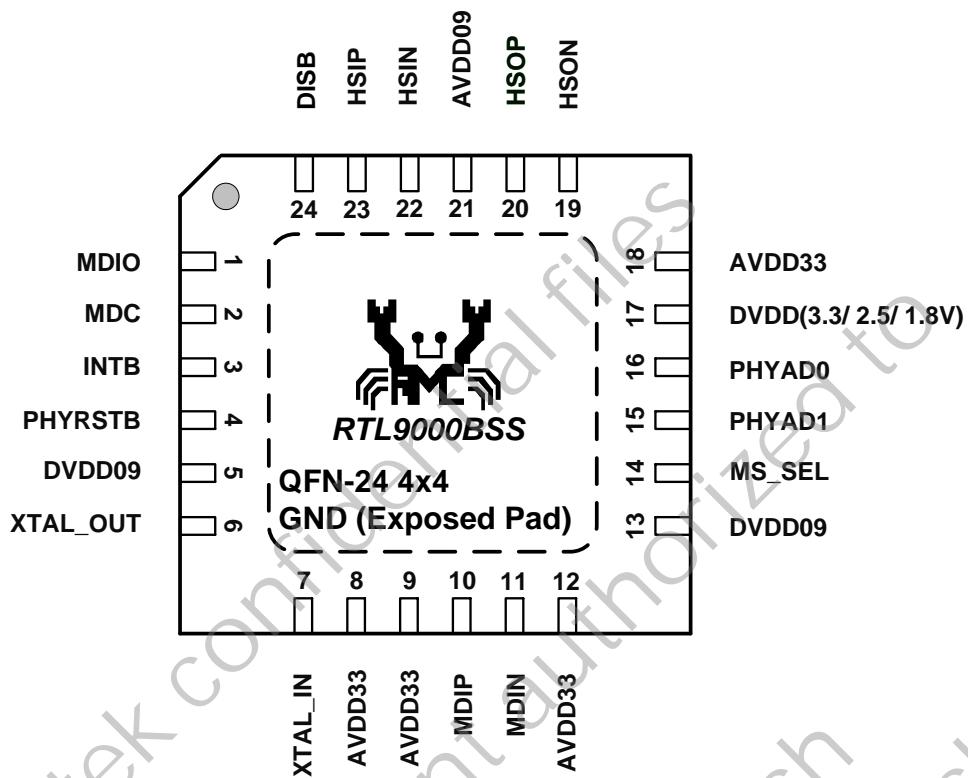


Figure 9. RTL9000BSS Pin Assignments (QFN-24)

7. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignments section on page 7 for a graphical representation.

I:	Input	LI:	Latched Input During Power up or Reset
O:	Output	IO:	Bi-Directional Input and Output
P:	Power	PD:	Internal Pull Down During Power-on Reset
PU:	Internal Pull Up During Power-on Reset	OD:	Open Drain
G:	Ground		

7.1. Transceiver Interface

Table 2. Transceiver Interface

Pin No.	Product	Pin Name	Type	Description
18	RTL9000BF	MDIP	IO	Transceiver + / -.
12	RTL9000BN			
11	RTL9000BR			
15	RTL9000BS			
10	RTL9000BSS			
19	RTL9000BF			
13	RTL9000BN			
12	RTL9000BR			
16	RTL9000BS			
11	RTL900BSS			

7.2. Clock

Table 3. Clock

Pin No.	Product	Pin Name	Type	Description
8	RTL9000BF	XTAL_IN	I	25MHz Crystal Input / External Clock Input. If a 25MHz oscillator is used, connect this pin to the oscillator's output (see section 11.10, page 154 for clock source specifications). Note that in RMII input mode, if connect the XTAL_IN to AVDD33, the REF_CLK will be the system clock source. (RTL9000BF/BN/BR only)
6	RTL9000BN			
5	RTL9000BR			
7	RTL9000BS			
7	RTL9000BSS			
7	RTL9000BF	XTAL_OUT	O	25MHz Crystal Output When using the external clock/oscillator, keep this pin floating.
5	RTL9000BN			
4	RTL9000BR			
6	RTL9000BS			
6	RTL9000BSS			

7.3. MII

Table 4. MII

Pin No.	Product	Pin Name	Type	Description
31	RTL9000BF	TXC	O	Transmit Clock. The transmit reference clock will be 25MHz. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN signals.
28	RTL9000BN			
24	RTL9000BR			
36	RTL9000BF	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
33	RTL9000BN			
29	RTL9000BR			
35	RTL9000BF	TXD1	I	
32	RTL9000BN			
28	RTL9000BR			
34	RTL9000BF	TXD2	I	
31	RTL9000BN			
27	RTL9000BR			
33	RTL9000BF	TXD3	I	
30	RTL9000BN			
26	RTL9000BR			
32	RTL9000BF	TXEN	I	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD[3:0].
29	RTL9000BN			
25	RTL9000BR			
29	RTL9000BF	RXC	O	Receive Clock.
25	RTL9000BN			
22	RTL9000BR			
28	RTL9000BF	RXD0	O/LI/PU	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
24	RTL9000BN			
21	RTL9000BR			
27	RTL9000BF	RXD1	O/LI/PD	
23	RTL9000BN			
20	RTL9000BR			
26	RTL9000BF	RXD2	O/LI/PD	
22	RTL9000BN			
19	RTL9000BR			
25	RTL9000BF	RXD3	O/LI/PD	
21	RTL9000BN			
18	RTL9000BR			
23	RTL9000BF	RXDV	O/LI/PU	Receive Data Valid. This pin is asserted high when received data is present on RXD[3:0]. This signal is valid on the rising edge of RXC.
18	RTL9000BN			
16	RTL9000BR			
22	RTL9000BF	RXER	O/LI/PD	Receive Error. RXER is a required output from the PHY, but is an optional input to the MAC.
17	RTL9000BN			
15	RTL9000BR			

7.4. RMII

Table 5. RMII

Pin No.	Product	Pin Name	Type	Description
31	RTL9000BF	TXC	Not used	This pin is not used in RMII mode; keep floating.
28	RTL9000BN			
24	RTL9000BR			
36	RTL9000BF	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[1:0].
33	RTL9000BN			
29	RTL9000BR			
35	RTL9000BF	TXD1	I	
32	RTL9000BN			
28	RTL9000BR			
34	RTL9000BF	TXD2	Not used	This pin is not used in RMII mode; keep floating.
31	RTL9000BN			
27	RTL9000BR			
33	RTL9000BF	TXD3	Not used	This pin is not used in RMII mode; keep floating.
30	RTL9000BN			
26	RTL9000BR			
32	RTL9000BF	TXEN	I	Transmit Enable.
29	RTL9000BN			
25	RTL9000BR			
29	RTL9000BF	REF_CLK	IO	Synchronous 50MHz Reference Clock for Transmit, Receive, and Control Interfaces. When operating at RMII Output mode, this pin will output the 50MHz Reference clock. When operating at RMII Input mode, the Reference Clock 50MHz \pm 50ppm generated by an external oscillator should be inputted to this pin. Note that in RMII input mode, if connect the XTAL_IN to AVDD33, the REF_CLK will be the system clock source. Otherwise, XTAL_IN (crystal) is applied instead of REF_CLK.
25	RTL9000BN			
22	RTL9000BR			
28	RTL9000BF	RXD0	O/LI/PU	Receive Data. Data is transmitted from PHY to MAC via RXD[1:0].
24	RTL9000BN			
21	RTL9000BR			
27	RTL9000BF	RXD1	O/LI/PD	
23	RTL9000BN			
20	RTL9000BR			
26	RTL9000BF	RXD2	Not used	This pin is not used in RMII mode; keep floating.
22	RTL9000BN			
19	RTL9000BR			
25	RTL9000BF	RXD3	Not used	This pin is not used in RMII mode; keep floating.
21	RTL9000BN			
18	RTL9000BR			

Pin No.	Product	Pin Name	Type	Description
22	RTL9000BF	RXER	O/LI/PD	Receive Error. RXER is a required output from the PHY, but is an optional input to the MAC.
17	RTL9000BN			
15	RTL9000BR			
23	RTL9000BF	RXDV	O/LI/PU	Receive Data Valid This pin is asserted high when received data is present on RXD[1:0]. This signal is asserted asynchronously to REF_CLK.
18	RTL9000BN			
16	RTL9000BR			

7.5. RGMII

Table 6. RGMII

Pin No.	Product	Pin Name	Type	Description
31	RTL9000BF	TXC	I	Transmit Clock. The transmit reference clock should be supplied by 25MHz. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXCTL signals.
28	RTL9000BN			
24	RTL9000BR			
36	RTL9000BF	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
33	RTL9000BN			
29	RTL9000BR			
35	RTL9000BF	TXD1	I	
32	RTL9000BN			
28	RTL9000BR			
34	RTL9000BF	TXD2	I	
31	RTL9000BN			
27	RTL9000BR			
33	RTL9000BF	TXD3	I	
30	RTL9000BN			
26	RTL9000BR			
32	RTL9000BF	TXEN	I	Transmit Control Signal from the MAC (i.e. TXCTL).
29	RTL9000BN			
25	RTL9000BR			
29	RTL9000BF	RXC	O	Receive Clock. This pin provides a continuous clock as a timing reference for RXD[3:0] and RXCTL signals.
25	RTL9000BN			
22	RTL9000BR			

Pin No.	Product	Pin Name	Type	Description
28	RTL9000BF	RXD0	O/LI/PU	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
24	RTL9000BN			
21	RTL9000BR			
27	RTL9000BF			
23	RTL9000BN			
20	RTL9000BR			
26	RTL9000BF			
22	RTL9000BN			
19	RTL9000BR			
25	RTL9000BF			
21	RTL9000BN	RXD3	O/LI/PD	
18	RTL9000BR			
22	RTL9000BF			
17	RTL9000BN	RXER	Not used/PD	This pin is not used in RGMII mode; keep floating.
15	RTL9000BR			
23	RTL9000BF			
18	RTL9000BN	RXDV	O/LI/PU	Receive Control Signal to the MAC (i.e. RXCTL).
16	RTL9000BR			

7.6. SGMII

Table 7 SGMII

Pin No.	Product	Pin Name	Type	Description
42	RTL9000BF	HSIP	I	SGMII Input Data. Positive
29	RTL9000BS			
23	RTL9000BSS			
41	RTL9000BF	HSIN	I	SGMII Input Data. Negative.
28	RTL9000BS			
22	RTL9000BSS			
39	RTL9000BF	HSOP	O	SGMII Output Data. Positive.
26	RTL9000BS			
20	RTL9000BSS			
38	RTL9000BF	HSON	O	SGMII Output Data. Negative.
25	RTL9000BS			
19	RTL9000BSS			

7.7. LED/PTP Application Interface

Table 8. LED/PTP Application Interface

Pin No.	Product	Pin Name	Type	Description
43	RTL9000BF	LED / PTP_GPIO/ WAKE_O	OD (LED/WAKE_O)/ IO (PTP_GPIO)/	1. Debug LED (default) 2. PTP GPIO 3. PTP clock input from the external reference clock source. Keep this pin floating if the function is not used. Note: The function priority of pin 34 is as above when all of the functions are enabled. This pin will function as PTP GPIO by setting Address 0xD42A, bit[0] = 0 (see 9.2.52, page 112); when setting Address 0xE410, bit[4] = 1 (see section 9.3.4, page 117, the PTP clock input function will take over.) 4. Wake-out forward function, see section 8.6.3, page 33.
34	RTL9000BN			
30	RTL9000BS			

7.8. Management Interface

Table 9. Management Interface

Pin No.	Product	Pin Name	Type	Description
46	RTL9000BF	MDC	I	Management Data Clock. (MDC) Refer to section 11.11.1 MDC/MDIO Timing.
1	RTL9000BN			
32	RTL9000BR			
1	RTL9000BS			
2	RTL9000BSS			
45	RTL9000BF	MDIO	IO/PU	Input/ Output of Management Data. (MDIO) Pull up to DVDD. For Register access, refer to 8.10.8 Register Access and 11.11.1 MDC/MDIO Timing.
36	RTL9000BN			
31	RTL9000BR			
32	RTL9000BS			
1	RTL9000BSS			
4	RTL9000BF	INTB	O/OD	Interrupt. Set low if status changed; active low. Keep this pin floating if the function is not used. <i>Note: The behavior of this pin is level-triggered.</i> This pin is 5V-friendly (up to 5.25 V).
2	RTL9000BN			
1	RTL9000BR			
3	RTL9000BS			
3	RTL9000BSS			
5	RTL9000BF	PHYRSTB	I/PU	Hardware Reset. Active low. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers except OP registers will be cleared after this hardware reset. This pin is 5V-friendly (up to 5.25 V).
3	RTL9000BN			
2	RTL9000BR			
4	RTL9000BS			
4	RTL9000BSS			
44	RTL9000BF	DISB	I/PD	Disable packet transmission and MDIO will be read-only. Active low. Note that this pin is active low and internal pull down, there must to place a pull up resistor or the transmission will be disabled. This pin is 5V-friendly (up to 5.25 V).
35	RTL9000BN			
30	RTL9000BR			
31	RTL9000BS			
24	RTL9000BSS			
12	RTL9000BF	INH	O	Output floating when PHY is in the Sleep mode. or application of the INH pin, refer to section 8.4.1, Sleep mode. Keep this pin floating if the function is not used.
10	RTL9000BN			
9	RTL9000BR			
11	RTL9000BS			
10	RTL9000BF	WAKE	I	Local Wake-up Input. The edge detection can refer to section 8.6. The default setting is raising edge detection hence it is active high. The level of detection can be selected by OPCR1, section 9.4.1.
8	RTL9000BN			
7	RTL9000BR			
9	RTL9000BS			

7.9. Power and Ground

Table 10. Power and Ground

Pin No.	Product	Pin Name	Type	Description
11	RTL9000BF	V33	P	Connect to independent 3.3V.
8	RTL9000BR			
10	RTL9000BS			
9, 17, 20, 37	RTL9000BF	AVDD33	P	Analog 3.3V Power. Connect to main power 3.3V.
7, 11, 14	RTL9000BN			
6, 10, 13	RTL9000BR			
8, 14, 17, 24	RTL9000BS			
8, 9, 12, 18	RTL9000BSS			
40	RTL9000BF			
5, 27	RTL9000BS	AVDD09	P	Analog 0.9V Power. See reference schematic of the RTL9000BF/BS/BSS.
21	RTL9000BSS			
6, 21	RTL9000BF			
4, 16	RTL9000BN			
3, 14	RTL9000BR			
18	RTL9000BS	DVDD09	P	Digital 0.9V Power and Internal LDO Output. The digital 0.9V power is supplied by the internal LDO output directly inside the RTL9000BF/BN/BR/BS/BSS.
5, 13	RTL9000BSS			
24, 30	RTL9000BF			
19, 27	RTL9000BN			
17, 23	RTL9000BR			
23	RTL9000BS	DVDD	P	Note that it is not recommended to use the internal LDO for DVDD power supplying when using bridge mode in speed of 1000Mbps.
17	RTL9000BSS			
49	RTL9000BF			
37	RTL9000BN			
33	RTL9000BR			
33	RTL9000BS	GND	G	Ground by Exposed Pad (E-Pad).
25	RTL9000BSS			

7.10. Hardware Strapping Configuration

Table 11. Hardware Strapping Configuration

Pin No.	Product	Configuration	Type	Description													
22	RTL9000BF	MS_SEL	O/LI/PD	Master / Slave Mode Configuration. HIGH: Master LOW: Slave													
17	RTL9000BN																
15	RTL9000BR																
20	RTL9000BS																
14	RTL9000BSS																
25	RTL9000BF	MII_SEL0 MII_SEL1	O/LI/PD O/LI/PD	MII Mode Configuration.													
26				<table border="1"> <thead> <tr> <th>MII_SEL1 (RXD2)</th> <th>MII_SEL0 (RXD3)</th> <th>MII Mode</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>MII</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>RMII Output mode</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>RGMII</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>RMII Input mode</td> </tr> </tbody> </table>	MII_SEL1 (RXD2)	MII_SEL0 (RXD3)	MII Mode	LOW	LOW	MII	LOW	HIGH	RMII Output mode	HIGH	LOW	RGMII	HIGH
MII_SEL1 (RXD2)	MII_SEL0 (RXD3)	MII Mode															
LOW	LOW	MII															
LOW	HIGH	RMII Output mode															
HIGH	LOW	RGMII															
HIGH	HIGH	RMII Input mode															
21	RTL9000BN																
22																	
18	RTL9000BR																
19				For the pin assignment of RMII Output/Input mode, refer to section 7.4.													
28 (RXD0)	RTL9000BF	PHYAD0 PHYAD1	O/LI/PU O/LI/PD	PHY Address [1:0] Configuration.													
27 (RXD1)				<table border="1"> <thead> <tr> <th>PHYAD1 (RXD1)</th> <th>PHYAD0 (RXD0)</th> <th>PHY Address</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>0</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>1</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>2</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>3</td> </tr> </tbody> </table>	PHYAD1 (RXD1)	PHYAD0 (RXD0)	PHY Address	LOW	LOW	0	LOW	HIGH	1	HIGH	LOW	2	HIGH
PHYAD1 (RXD1)	PHYAD0 (RXD0)	PHY Address															
LOW	LOW	0															
LOW	HIGH	1															
HIGH	LOW	2															
HIGH	HIGH	3															
24 (RXD0)	RTL9000BN																
23 (RXD1)																	
21 (RXD0)	RTL9000BR	<p>Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xA43, Reg 0x18, bit[13]=0 (see 0, page 99).</p> <p>Note 2: If the user wants to use PHYAD is 0 in a multiple PHY case, the broadcast should be disabled on all PHYs before PHYAD 0 can be used.</p> <p>Note 3: The RTL9000BR/BS/BSS with PHYAD[1:0]=00 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xA43, Reg 0x18, bit[6]=1 (see 0, page 99).</p>															
22	RTL9000BS	ST_CHG	O/LI/PU														
21																	
16	RTL9000BSS																
15																	
23	RTL9000BF	ST_CHG	O/LI/PU	Operating Modes (OP) State Change Condition Configuration For ST_CHG applications, refer to section 8.4 Standby mode. HIGH: Auto mode, the PHY goes to Normal Mode automatically, when it powers on/wakes up it asserts PHYRSTB to low. LOW: Manual mode, the PHY goes to Normal Mode manually, when it powers on/wakes up it asserts PHYRSTB to low (The OP goes to sleep/normal command; refer to section 8.4.2).													
18	RTL9000BN																
16	RTL9000BR																
19	RTL9000BS																

8. Function Description

8.1. Transmitter

The RTL9000BF/BN/BR/BS/BSS's PCS layer receives data bytes from the MAC through the MII/RMII interface (RTL9000BF/BN/BR) or SGMII interface (RTL9000BS/BSS) and performs generation of continuous code-groups through 2D-PAM3 coding technology. These code groups are transmitted onto the 1-twisted pair at 66.67M Baud/s through a D/A converter, and then the analog signal passes through a filter to minimize EMI effects.

8.2. Receiver

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, echo cancellation, timing recovery, and 2D-PAM3 decoding. The 8-bit-wide data is recovered and is sent to the MII/RMII interface at a clock speed of 25/50MHz. The Rx MAC retrieves the packet data from the receive MII/RMII interface and sends it to the Rx Buffer Manager.

8.3. Loopback Modes

The RTL9000BF/BN/BR/BS/BSS provides three loopback modes: PCS, MDI, and Remote loopback. PCS and Local PMA (MDI) loopback are specified in the IEEE 100BASE-T1 specification.

8.3.1. PCS Loopback Mode

The PCS shall enter PCS loopback mode when the PCS loopback bit [14] in section 9.2.1 is set to 1 (see Figure 10). In this mode, once the data from the MII transmit passes the PCS transmit, the data is sent back to the PCS receive directly, i.e., the PCS receive gets the data from PCS transmit directly. This action allows the MAC to compare packets sent through the MII Transmit function to packets received from the MII Receive function to validate the functionality of 100BASE-T1 PCS functions. Note that in PCS Loopback mode, the link status indicates active.

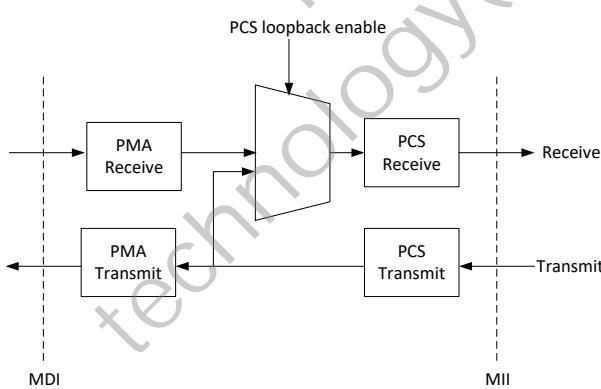


Figure 10. PCS Loopback Data Flow

8.3.2. MDI Loopback

The PHY shall enter MDI loopback mode when the MDI loopback bit [10] in section 0 is set to 1. (see Figure 11). In this mode, the PMA Receive function utilizes the echo signals from the unterminated MDI and decodes these signals to pass the data back to the MII Receive interface. Note that the cable link on the MDI pins must be removed in this test. The MAC may compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 100BASE-T1 PCS and PMA functions. Note that in MDI Loopback the link status indicates active.

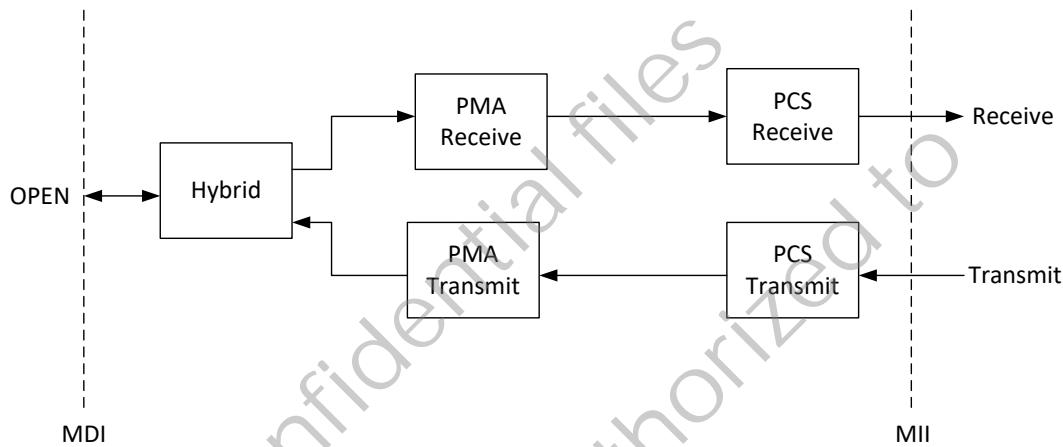


Figure 11. MDI Loopback Data Flow

8.3.3. Remote Loopback

The PHY shall enter Remote Loopback mode when the bit [5:4] in section 9.2.32 is set to 1. In Remote Loopback mode, packets received from the Link Partner through the MDI will go through the PMA Receive and PCS Receive to the MII, and also be sent back through PCS Transmit and MDI to the Link partner as shown in Figure 12. The MAC is allowed to compare the amount of the packets sent to the MDI with the packets received from MDI to validate the physical channel. Note that the link must be active when Remote Loopback is performed.

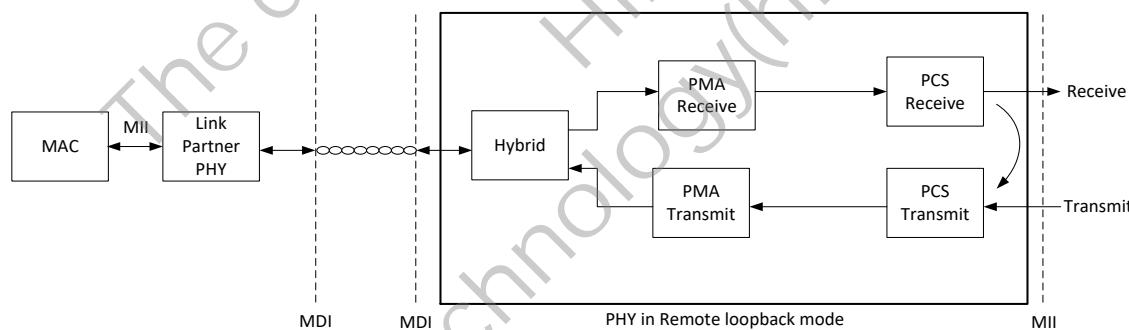


Figure 12. Remote Loopback Data Flow

8.4. Operating Modes (OP)

8.4.1. Operating Modes

Figure 13 shows the transitions of the RTL9000BF/BN/BR/BS/BSS Operating Modes (OP). There are various modes in the PHY, including Power-off, Sleep, Safety, Normal, and Standby modes. Each operating mode has different power consumption (refer to section 11.4, page 147). Availability of establishing the link depends upon whether the MDIO command is accessible or not. The register can indicate Normal, Safety and Standby mode as shown in section 9.2.54, page 113.

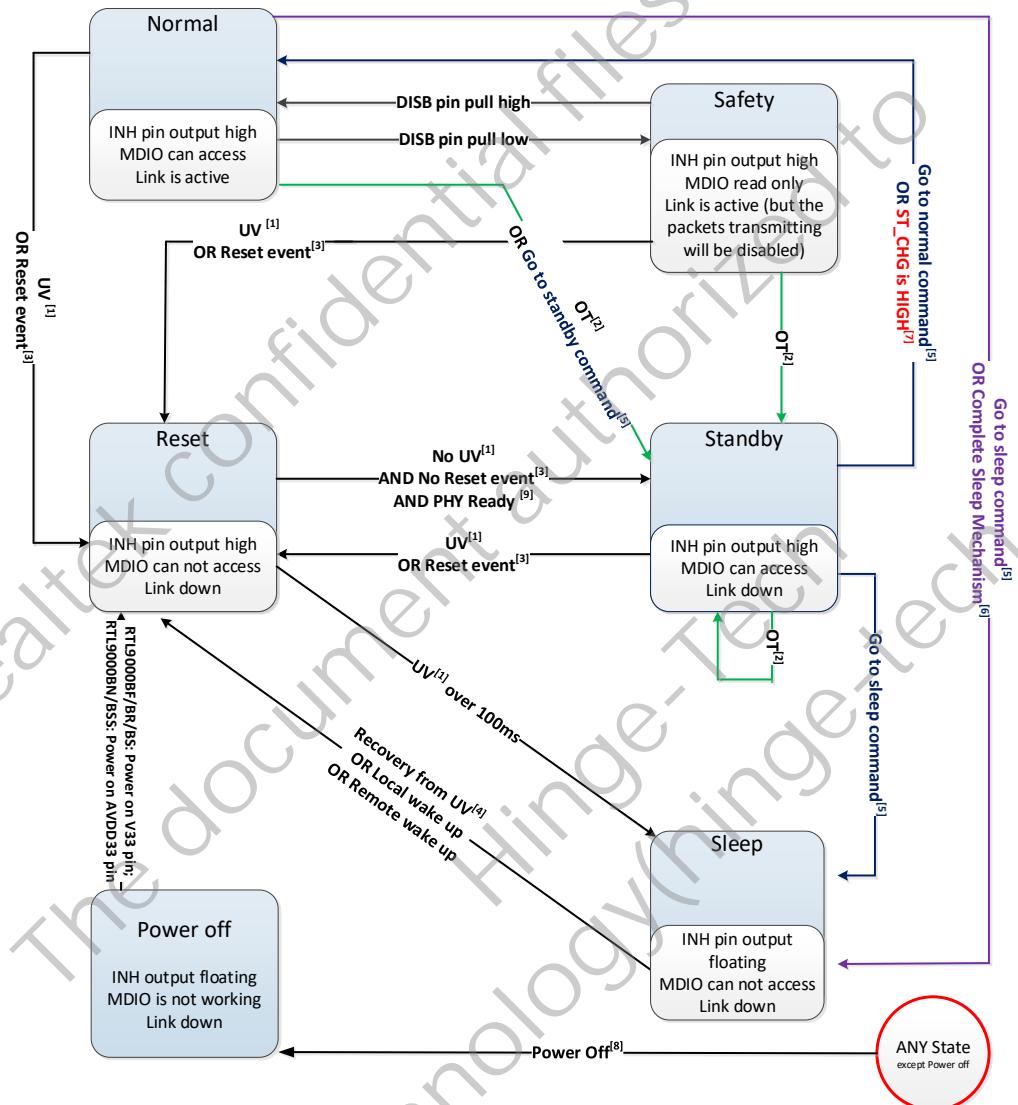


Figure 13. Operating Mode Transitions

UV means Undervoltage

[1] For RTL9000BF/BR/BS, UV on one of the power supply AVDD33, DVDD, AVDD09, DVDD09.

For RTL9000BN/BSS, UV on one of the power supply DVDD, AVDD09, DVDD09.

[2] OT means Over-Temperature.

[3] A Reset event means ‘the PHYRSTB pin was asserted low’ or ‘the MDIO reset command occurred (set Address 0xDD00, bit[5] = 1)’.

Note that when the MDIO reset command completes the Reset event, it will be self-cleared.

[4] Recovery from UV means re-power up the undervoltage power supply pin.

[5] For details of the ‘Go to Normal/Standby/Sleep’ command, refer to section 9.4.2 and 9.4.13.

[6] For details of the complete Sleep Mechanism, refer to section 8.5

[7] The value of ST_CHG is decided only during the hardware configuration procedure on power on/wake up/assert PHYRSTB to low by the external resistor. For details of the setting, refer to section 8.9.

[8] For the RTL9000BF/BR/BS, UV is measured at the V33 pin. For the RTL9000BN/BSS, UV is measured at the AVDD33 pin.

[9] PHY Ready means that the register at page 0xA42, reg 0x10, bit [2:0] = 0x30.

Power-Off Mode

The RTL9000BF/BR/BS remains in Power-off mode when the voltage on the V33 pin is below the Undervoltage (UV) threshold. For the RTL9000BN/BSS, it will go to Power-off mode when a UV event occurs on AVDD33 pins. When in Power off mode, all functions of the PHY are disabled. When the PHY is powered on, it goes to the Reset mode first.

Sleep Mode

The RTL9000BF/BN/BR/BS can be turned to Sleep mode for lower power consumption via the ‘Go to sleep command’ (section 9.4.2, page 127) or ‘Complete sleep flow’ (section 8.4, page 23). A UV event can also cause the PHY to enter Sleep mode. When the PHY is in Sleep mode, the data transmit and receive functions are disabled, which means that the MDI twisted-pair lines cannot transmit any signals. Any transmit requests from the MII interface will be ignored. The MDIO read/write command cannot access the PHY in Sleep mode.

Depending on the power supplied domain, there are two types of Sleep mode:

One is Deep Sleep mode, which turns off the supply power of AVDD33, but keeps the supply power of the V33 pin and optimizes the system for ultra-low power consumption.

The other is Lite Sleep mode, which supplies AVDD 33 and V33 power permanently; i.e. no power domain will be turned off. The RTL9000BF/BR/BS supports both Deep Sleep mode and Lite Sleep mode, while the RTL9000BN/BSS only supports Lite Sleep mode.

There are two implementations for Deep Sleep mode (see Figure 1, page 4). In one mode the INH pin turns off the 3.3V external regulator of AVDD33 and only the V33 pin is powered by independent external 3.3V; the other mode supplies the V33 pin and main power separately, and the supplied AVDD33 power is turned off when the PHY is in Deep Sleep mode. The INH pin will output floating in Sleep mode.

When the device is in Sleep mode, it can be woken up by local wake up (WAKE pin asserted, see section 8.6.1, page 29) or remote wake up (received a Wake Up Pattern (WUP) from its link partner), see section 8.6.2, page 32). Note that when the supply power of AVDD33 is recovered, the PHY will also be woken up from Deep Sleep mode. When the PHY wakes, the INH pin will output high and the PHY will switch to Normal mode (set ST_CHG to HIGH) or Standby mode (set ST_CHG to LOW).

Reset Mode

The RTL9000BF/BN/BR/BS/BSS will go to Reset mode when the PHYRSTB pin is asserted low or it receives the MDIO reset command (set Address 0xDD00, bit [5] = 1, refer to section 9.4.2, page 127). The PHY will be reset, and all registers will be set to default values except for the OP registers in section 8.5, page 27. When the MDIO Reset command completes the Reset event, it will be self-cleared. The link cannot be established and the MDIO command cannot be accessed when the PHY is in Reset mode.

Standby Mode

If the RTL9000BF/BN/BR/BS/BSS is set to manual mode (set ST_CHG to LOW), when it powers on/wakes up, it will stay in Standby mode. When the PHY is in Standby mode, the link cannot be established but the PHY can be accessed by the MDIO command. Users can also set the ‘Go to Normal /Sleep mode’ command to let the PHY transit to other states. In addition, the OT event will allow the PHY to exit from Normal or Safety mode to Standby mode.

Normal Mode

To establish a valid link with the link partner, the RTL9000BF/BN/BR/BS/BSS must be operated in Normal mode. If the PHY is set to auto mode (set ST_CHG to LOW), it will change to Normal mode automatically and activate the link after power-on/wake up.

Safety Mode

When the DISB pin is pulled low, the RTL9000BF/BN/BR/BS/BSS will change from Normal to Safety mode. In Safety mode, the link remains active, packet transmission is disabled but the received function is still active. The main MDIO write function is also disabled if bit 1 of section 9.2.38 is not enabled before entering Safety mode, but MDIO can be read.

For Normal Register Access (section 8.10.8.1, page 74), Register 31 can still be written to switch to the page of the read desired register in Safety mode. For the Special Register Access (section 8.10.8.2, page 74), if the user wants to write the register address of the read desired register into Register 27 whilst in Safety mode, the register at Address 0xD030 bit [4] should be set to 1 before entering Safety mode.

Table 12 presents an overview of the status of RTL9000BF/BN/BR/BS/BSS functional blocks in each operating mode.

Table 12. Overview of the Operating Modes

	Power-Off	Sleep	Reset	Standby	Normal	Safety
MDI Impedance	Open/High impedance	100ohm	100ohm	100ohm	100ohm	100ohm
Link Status	Passive	Passive	Passive	Passive	Active	Active
WUP Detection	Off	On	On	On	Off	Off
OT Detection	Off	Off	Off	On	On	On
INH Pin Output	Floating	Floating	High	High	High	High
MDIO Command	Not accessible	Not accessible	Not accessible	▲ Read/Write in general condition ▲ Read only when DISB pin pulled low	Read/Write	Read only ^[1]
PHY is Reset or not	Yes	Yes	Yes	No	No	No

Note 1: MDIO write function can be enabled by setting bit 1 of section 9.2.38 before entering Safety mode.

8.4.2. Operating Mode Transition

The following events, listed in order of priority, trigger mode transitions:

1. **RTL9000BF/BR:** Undervoltage on V33 pin
RTL9000BN/BS/BSS: Undervoltage on AVDD33 pin
2. Undervoltage (UV) on other power pins
3. Reset event
4. OT event
5. Local wake up; Remote wake up
6. Go to sleep/normal/Standby command (Refer to section 9.4.2, page 127)
7. Hardware strapping pin

As an example, if ST_CHG is set to HIGH, but the ‘go to Standby’ command lets the PHY go to Standby mode, then the PHY will not go back to Normal mode automatically, as the ‘go to Standby’ mode command has priority over the strap pin (set the ST_CHG to HIGH).

OP Go to Sleep/Normal/Standy command (Refer to section 9.4.3, page 128)

The register table shown in section 9.4.2, page 127 shows all the Go to Sleep/Normal/Standy commands. Be aware that the OP Go to Normal command must be combined with op_cmd_2 in section 9.4.13, page 134. The OP Go to Sleep/Normal/Standy command will be cleared in the following conditions:

1. The PHY goes to Sleep mode
2. UV event occurred in Normal/Safety mode
3. Reset event occurred in Normal/Safety mode
4. OT event occurred in Normal/Safety mode
5. Wake up event occurred in any state (Option to set OCPR3 at section 9.4.4, page 128)

OP Event Flags

The RTL9000BF/BN/BR/BS/BSS supports UV/UV recovery/Wake up/Sleep/OT Power-on flags. For details refer to section 9.4.4, page 128, and section 9.4.10, page 132. In order to ensure the next wake up event can be detected, note that the lwake_flag and rwake_flag (in section 9.4.10, page 132) will be cleared if the following events occur.

1. PHY goes to Reset or Standby from Normal mode
2. PHY goes to Reset or Standby from Safety mode
3. PHY goes to Sleep mode from any state

8.5. Sleep Mechanism

The RTL9000BF/BR/BS supports the behavior of OPEN Alliance TC10 Sleep/Wake-up function for automotive Ethernet. The Sleep function puts the PHY into Sleep mode, which has lower power consumption, refer to section 11.4, page 147. For sleep mode refer to section 8.4.1, page 23.

To enable the Sleep function, the register at Page 0xA5A Reg 20 bit [0] must be set to 1 and a software reset asserted (Reg 0x0 bit [15] set to 1) to allow the Sleep capability to take effect. When the MAC gives a sleep request (refer to section 9.2.13, page 98) to the PHY (the Sleep Initiator), the PHY will start to perform sleep handshaking with its link partner (the Sleep Responder). Note that the sleep handshaking flow is available only when both PHYs (Sleep Initiator and Sleep Responder) are in Normal mode and their link is active. The sleep flow is successful if both PHYs finish the sleep handshaking (transmitted and received sleep signal on the MDI) properly (both of them will enter Sleep mode).

The sleep mechanism is able to reject sleep flow, and handle a sleep fail case. At the beginning of the sleep flow, the Sleep Initiator transmits the sleep signal to the Sleep Responder. The Sleep Responder will indicate its upper layer (namely MAC) through pulling the INTB pin low. If the MAC does not want the Sleep Responder to go to Sleep mode because of the unfinished transmission, the MAC should keep setting stop_sleep to 1 (see section 9.2.13, page 98) until the PHY stays in Normal mode. Both the Sleep Initiator and the Sleep Responder will stay in Normal mode, and the link between them will remain active. If the link between the Sleep Initiator and the Sleep Responder is accidentally interrupted while the handshaking of the sleep flow is in progress, the sleep flow will fail and both Sleep Initiator and Sleep Responder will stay in Normal mode.

Figure 14 shows the flow chart for both the Sleep Initiator and Sleep Responder. For details of the transition and status of Sleep mode, refer to section 8.4.1, page 23.

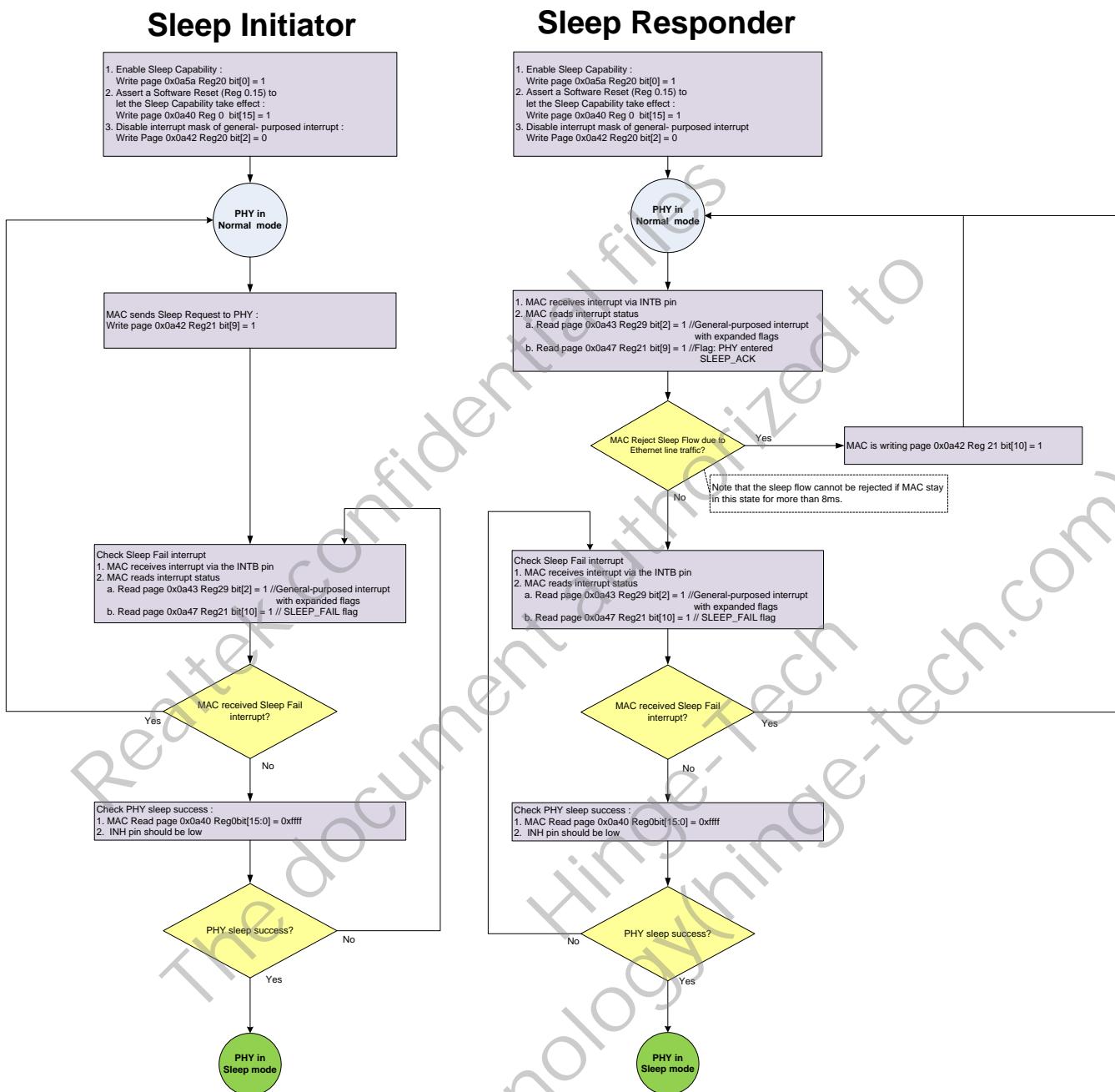


Figure 14. Sleep Mechanism Flow Chart

8.6. Wake-Up

8.6.1. Local Wake-Up

When the RTL9000BF/BN/BR/BS are in Sleep mode, they can be woken by detecting a local wake pulse on the WAKE pin. There are two kinds of detection for a local wake up event (Lwake event), one is rising edge detection; the other is falling edge detection. The rising/falling edge detection can be configured by setting a specified register (Address 0xDC0C, bit [5] = 0 for rising edge detection; set to 1 for falling edge detection; see section 9.4.1, page 127). The default is set to rising edge detection.

As shown in Figure 15, in the RTL9000BF/BN/BR/BS, there is a detected level voltage for both rising and falling edge. If rising edge detection is chosen, the RTL9000BF/BN/BR/BS detects a Lwake event when the voltage on the WAKE pin is higher than detected high-level voltage V_{IH_WAKE} (rising edge on the WAKE pin) for longer than detected time T_{det_WAKE} . If falling edge detection is chosen, the RTL9000BF/BN/BR/BS detects a Lwake event when the voltage on the WAKE pin is lower than detected low-level voltage V_{IL_WAKE} (falling edge on the WAKE pin) for longer than detected time T_{det_WAKE} .

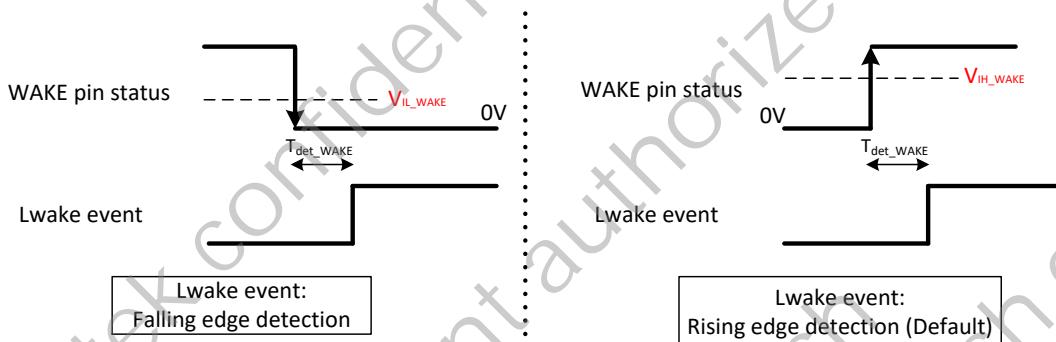


Figure 15. RTL9000BF/BN/BR/BS Local Wake Up (Lwake) Event Detection

As shown in Figure 16, in the application of Deep Sleep mode of the RTL9000BF/BR/BS, after detecting a local wake pulse on the WAKE pin, the INH signal rises and then turns-on the external regulator. Thus, the whole chip is powered on by the 3.3V voltage output from the external regulator.

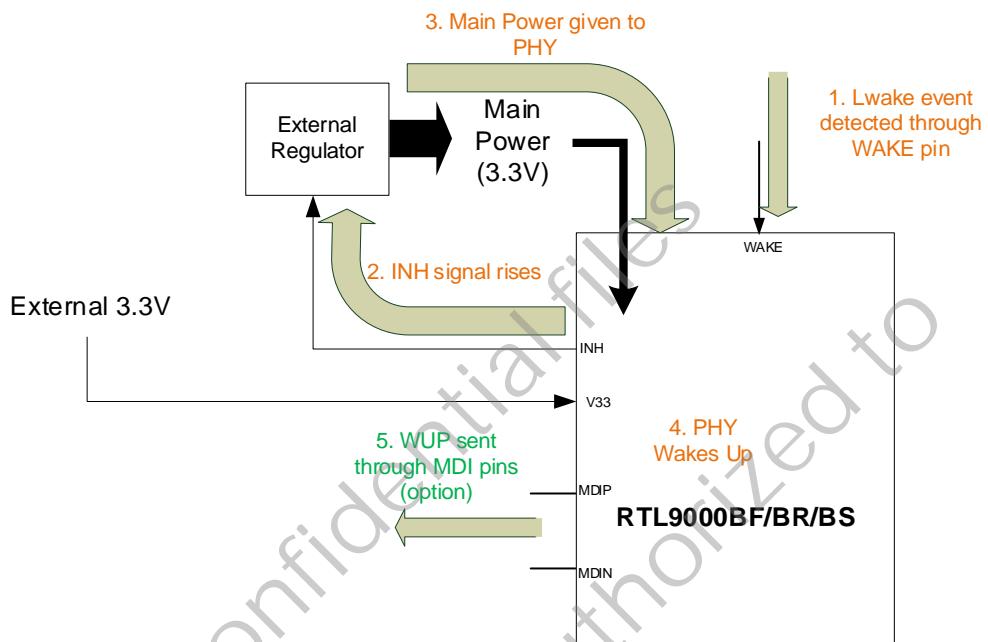


Figure 16. RTL9000BF/BR/BS Wake Flow for Local Wake Up With the INH Pin

As shown in Figure 17 and Figure 18, in the application of Lite Sleep mode in both the RTL9000BF/BR/BS, after detecting a local wake up pulse, the functions that were disabled in Sleep mode will recover.

After a local wake up, the RTL9000BF/BR/BS will remotely wake up its link partner automatically by sending the WUP on the MDI pins. If the application does not want the PHY to remotely wake up its link partner automatically, users can set the register at Address 0xDC0E, bit [0] to 0 (refer to section 9.4.2, page 127) disable the ability to forward the remote wake up to its link partner.

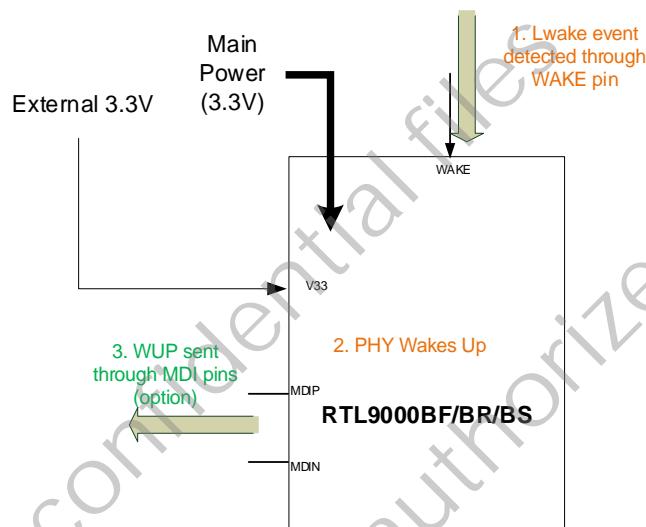


Figure 17. RTL9000BF/BR/BS Wake Flow for Local Wake Up Without the INH Pin

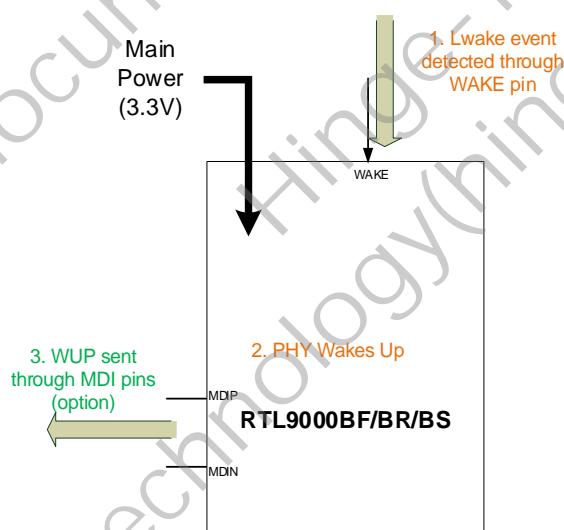


Figure 18. RTL9000BF/BR/BS Wake Flow for Local Wake Up

8.6.2. Remote Wake-Up

The RTL9000BF/BN/BR/BS detects a ‘Remote wake-up’ (Rwake) event when it detects the WUP on the MDI pins. Using a similar sequence as the local wake up as shown in Figure 19, Figure 20, and Figure 21, the RTL9000BF/BN/BR/BS are woken up by a remote wake up via a WUP detected through the MDI interface instead of the WAKE pin. The detection of the Rwake event can be disabled by writing the register at address 0x0DC0C bit [0] to 1, refer to section 9.4.1, page 127.

In the application of the Deep Sleep mode of the RTL9000BF/BN/BR/BS , after detecting the WUP on the MDI pins, the INH pin rises and then turns on the external regulator. Thus, the whole chip is powered on by the 3.3V voltage output from the external regulator. In the application of Lite Sleep mode for both RTL9000BF/BN/BR/BS, after detecting WUP on the MDI pins, the functions that were disabled in Sleep mode will recover.

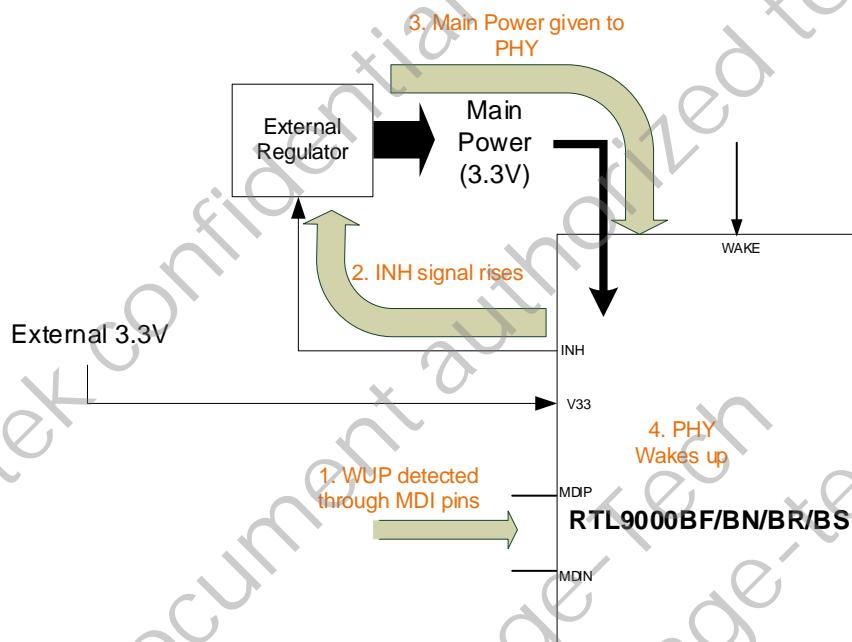


Figure 19. RTL9000BF/BN/BR/BS Wake Flow for Remote Wake-Up With the INH Pin

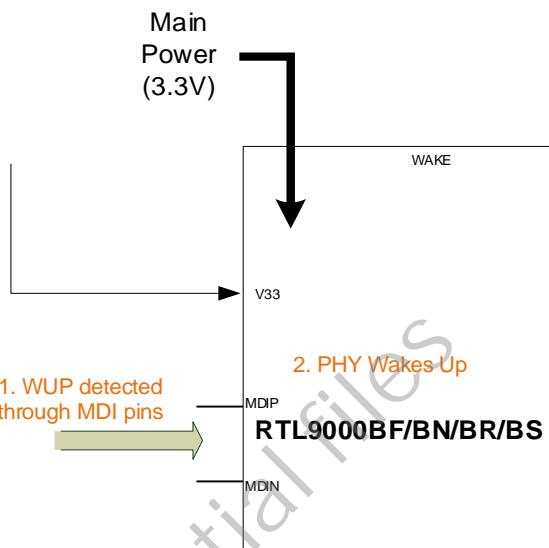


Figure 20. RTL9000BF/BN/BR/BS Wake Flow for Remote Wake Up

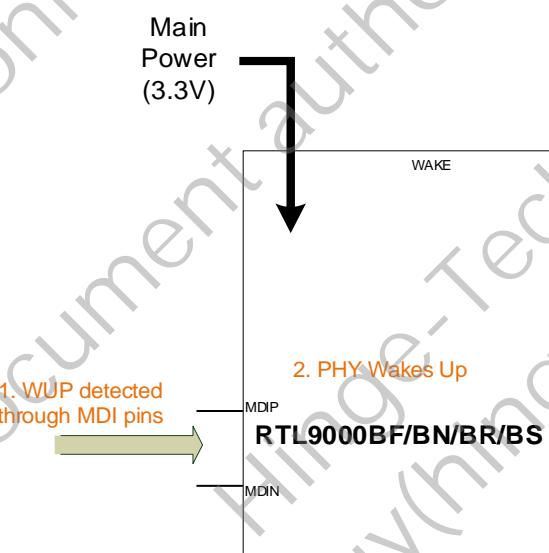


Figure 21. RTL9000BF/BN/BR/BS Wake Flow for Remote Wake Up

8.6.3. Wake-Out Forward

The RTL9000BF/BN/BR/BS supports the Wake-out forward function. When the PHY detects a Remote wake-up event (WUP or WUR), it will forward a pulse via the WAKE_O pin. The pulse width can be set to 40~50 μ s or 490~510ms by setting WAKE_O register (bit 1 of section 9.2.53). Note that the WAKE pin will be deactivated when the WAKE_O pin is outputting the wake-out pulse.

For a WUP forward wake-out pulse case, after the PHY wakes up from Deep sleep or Lite sleep mode, it will forward the wake-out pulse automatically when the Wake-out forward function (bit 0 of section 9.2.53) is enabled.

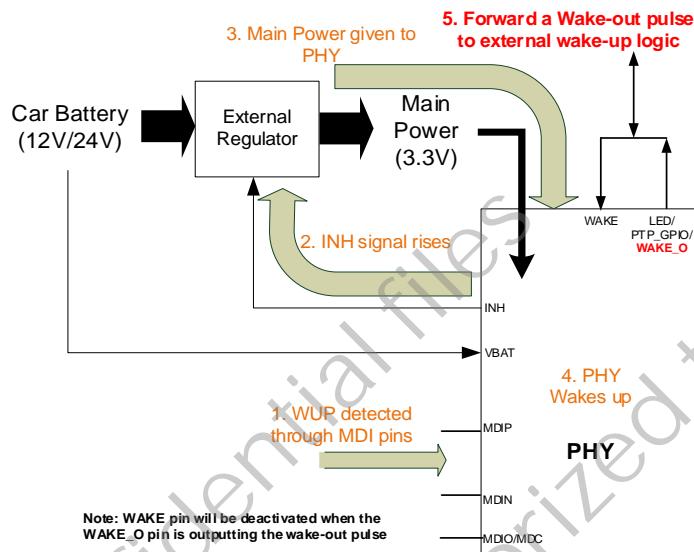


Figure 22. Wake-out forward Flow for receive WUP in Deep sleep mode

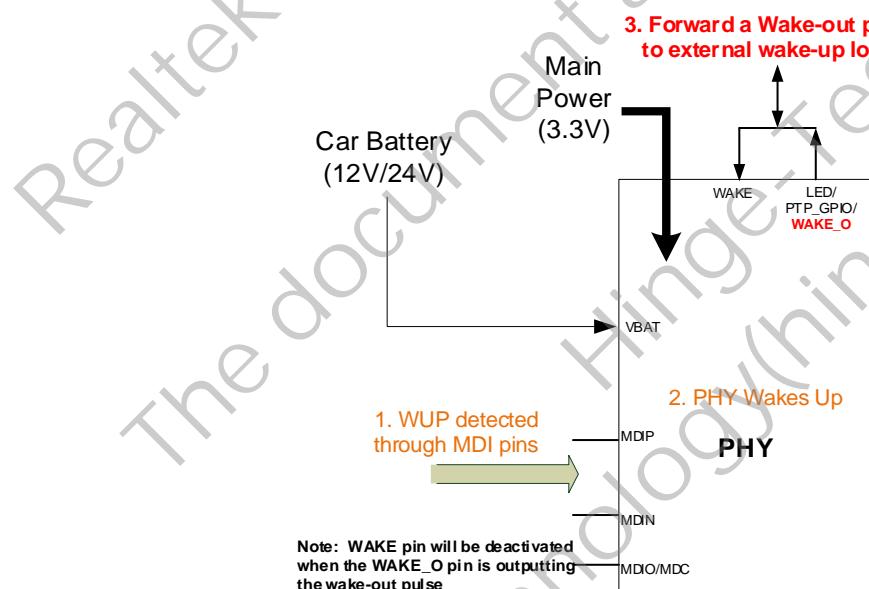


Figure 23. Wake-out forward Flow for receive WUP in Lite sleep mode

In a WUR forward wake-out pulse case. The PHY will forward the wake-out pulse when it receive a WUR command, if the Wake-out forward function (bit 0 of section 9.2.53), and sleep cap (bit 0 of section 9.2.24) are all enabled.

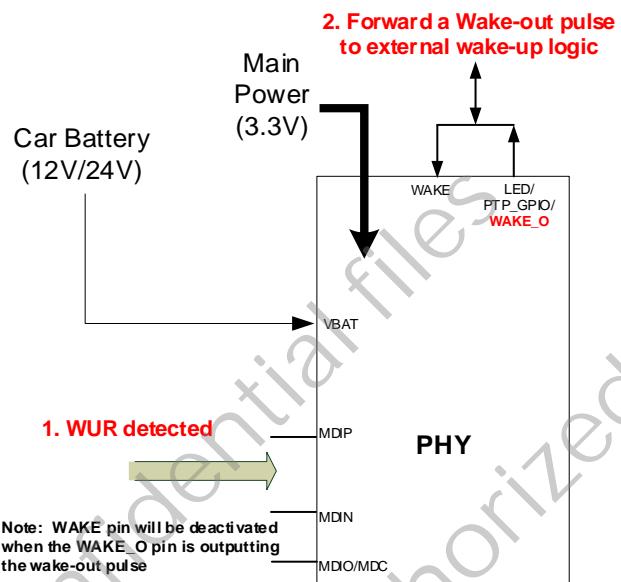


Figure 24. Wake-out forward Flow for receive WUR in Link-up mode

8.6.4. Wake Up Flow

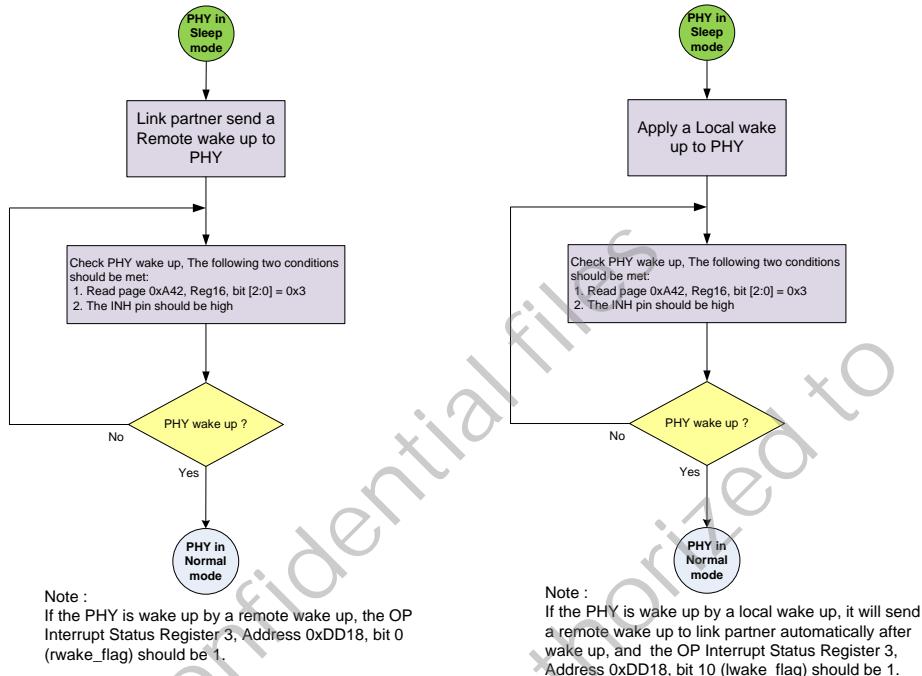


Figure 25. Local/Remote Wake-Up Flow

8.7. Precision Time Protocol (PTP)

Precision Time Protocol (PTP) is a series of IEEE specifications, including IEEE 1588 ver. 1, IEEE 1588 ver. 2, and IEEE 802.1AS*, that synchronize the time of the day or a standard time across a network system. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is timestamping specified PTP frames with high precision as close to the transmission media as possible. Timestamping in the PHY provides increased accuracy compared to timestamping in the MAC or higher layers.

The PTP block in the RTL9000BF/BN/BR/BS/BSS consists of three main functions (see Figure 26, page 37):

- PTP clock and Local clock
- Packet parser
- Application interface

By combining the above functions, the RTL9000BF/BN/BR/BS/BSS provides complete and accurate support for applications in a time-synchronous system.

*Note: For detailed specifications, refer to the IEEE standards - IEEE 1588 and IEEE 802.1AS.

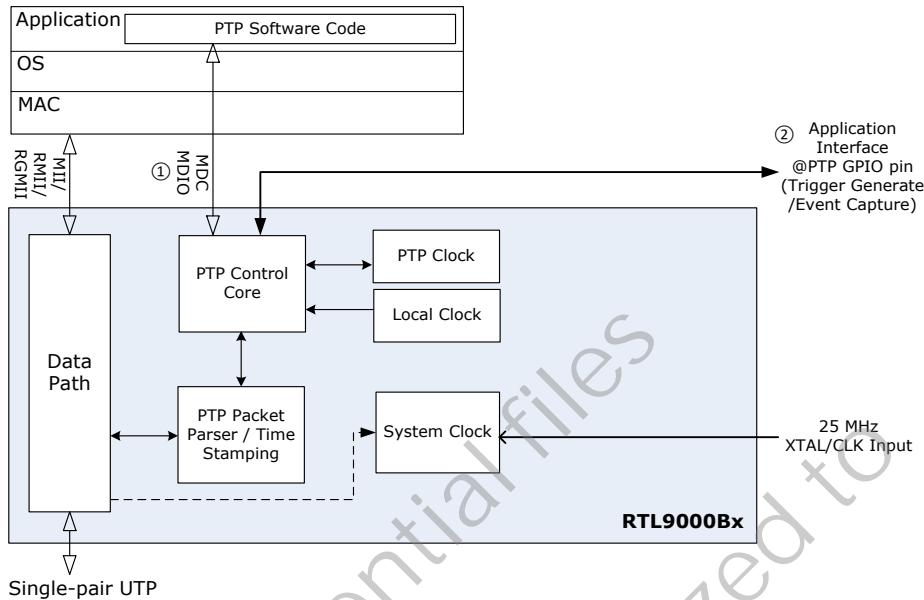


Figure 26. PTP Application Diagram

Note 1: By setting the PTP registers through the MDIO interface, the local PTP clock can be adjusted and synchronized according to the timing offset calculated by the upper layer software.

Note 2: A PTP GPIO provides Application Interfaces to upper layer or external utilization, including Trigger Generate (supports periodic trigger with nanosec-level jitter) and Event Capture functions, refer to section 8.7.3.

8.7.1. Synchronized PTP Clock

The RTL9000BF/BN/BR/BS/BSS supports 1 PTP instance, which consists of 1 PTP clock and 1 Local clock. Each clock consists of following time fields: seconds (48 bits), nanoseconds (30 bits), and fractional nanoseconds (in units of 2^{-32} ns). The Local clock is a free run clock used for reference, and its time is read only; the PTP clock is the adjustable clock for time synchronization. The PTP clock is PTP master/slave clock corresponding to the PTP role.

The RTL9000BF/BN/BR/BS/BSS provides several ways to access and update this internal PTP clock. The methods are listed below:

- Direct Read/Write
- Step Adjustment
- Rate Adjustment

A **Direct Write** of the time value is done by setting a new value to all time fields. This function may be used when initializing a PTP synchronization that needs an immediate setting to the time value due to the local PTP time being far apart from the Master clock time. Also for the PTP Master, it can be used to assign the standard time directly.

A **Step Adjustment** is an alternative method for making a quick compensation to the PTP clock time. Note that the adjustment can be incremented and decremented.

When the local time is close enough to the PTP Master, **Rate Adjustment** is a better way to fine-tune the time and compensate frequency drift. The Rate Adjustment allows correction by the order of 2^{-32} ns per clock cycle; that is, it can correct the offset over time accurately.

Refer to section 9.3.1, and 9.3.4 to 9.3.9 for register detail.

8.7.2. Packet Parser

8.7.2.1 Timestamping

The PTP packet parser in the RTL9000BF/BN/BR/BS/BSS continually monitors transmit/receive packet data in order to record the timestamp for the PTP Event Messages. The parser will recognize PTP messages transported in Layer 2 Ethernet, IPv4/UDP, or IPv6/UDP packet formats automatically. Upon detection of a PTP Event Message the RTL9000BF/BN/BR/BS/BSS will record the specific transmit/receive timestamp and provide it to the external PTP software through PTP_TRX_TS registers. The parser keeps timestamp in a pair of Local clock time and PTP clock time, simultaneously. If interrupt is enabled, a PTP interrupt will be generated when the transmit/receive timestamp is ready.

The network node operating PTP will exchange timestamp information by specific PTP Event Messages negotiation between itself and its link peer (link partner). After gathering necessary timestamp information, the external software of PTP Slave can compute the time offset and the rate ratio of PTP clock to the PTP master, and adjust the PTP clock to synchronize.

Refer to section 9.3.1 for PTP message capability, section 9.3.2 and 9.3.3 for interrupt, and 9.3.17 to 9.3.30 for timestamp.

8.7.2.2 One-Step Operation

The RTL9000BF/BN/BR/BS/BSS supports **One-Step** operation, which could help to reduce the work of the upper layer. The egress timestamp of a Sync message is on-the-fly inserted to the Sync itself by the PTP packet parser; while for the conventional **Two-Step** operation, the upper layer shall issue another Follow-Up message followed by a Sync message, which contains the egress timestamp of the Sync (t_1).

Furthermore, for the *Peer delay mechanism*, **One-Step** operation would calculate and insert the result of “ $<\text{Pdelay_Resp Egress Timestamp } (\text{pt}_3) > - <\text{Pdelay_Req Ingress Timestamp } (\text{pt}_2) >$ ” into Pdelay_Resp message directly; while for the **Two-Step** operation, the upper layer shall issue another Pdelay_Resp_Follow_Up message, which contains the egress timestamp of the Pdelay_Resp (pt_3), and let the initiator side calculate the above result ($\text{pt}_3 - \text{pt}_2$) by itself.

The differences between One-Step and Two-Step operation are illustrated in section 8.7.4.2, page 41 by Figure 27 and Figure 28.

The inserted timestamp can be configured to select from either the Local clock or the PTP clock.

Refer to section 9.3.1 and 9.3.33 for register detail.

8.7.2.3 Hardware-assisted Timestamp Insertion of Two-Step Operation

As well as the conventional **Two-Step** operation, *Hardware-assisted Timestamp Insertion* features are also implemented. With these features enabled, the PTP packet parser of the RTL9000BF/BN/BR/BS/BSS will insert some timestamps directly to the upcoming PTP event messages, which means upper layer software does not need to access these timestamp registers:

- For the *Delay request-response mechanism*:
 - Insert the egress timestamp of Sync (t_1) into the following Follow_Up message.
 - Insert the ingress timestamp of Delay_Req (t_4) into the following Delay_Resp message.
- For the *Peer delay mechanism*:
 - Insert the ingress timestamp of Pdelay_Req (pt_2) into the following Pdelay_Resp message.
 - Insert the egress timestamp of Pdelay_Resp (pt_3) into the following Pdelay_Resp_Follow_Up message.

Refer to section 9.3.1 for register detail.

8.7.2.4 Ingress Timestamp Insertion

The RTL9000BF/BN/BR/BS/BSS supports ingress timestamp insertion in the received PTP event message. The inserted timestamp format is 2 bits second and 30 bits nanoseconds, extracted from the least significant 2 bits of seconds, and entire 30 bits of the nanosecond field. If the sync period is less than 1 second, the external software is suggested to calculate the time offset by using the inserted timestamp without accessing the registers. If the complete timestamp is required, the timestamp is still available in registers.

The inserted timestamp can be configured to select from either the Local clock or the PTP clock.

Refer to section 9.3.1 and 9.3.33 for register detail.

8.7.2.5 VLAN Support and Configurable EtherType for PTP

The RTL9000BF/BN/BR/BS/BSS supports extended parser configuration:

- Parser supports PTP message with VLAN tag, as required by the OPEN Alliance. A PTP message with VLAN tag can be recognized by the parser.
- Parser supports customizable EtherType for PTP. In a close environment application, the customized EtherType could be used. A PTP message with customized EtherType can be recognized by the parser.

Refer to section 9.3.1 for the VLAN support; 9.3.32 and 9.3.31 for customized EtherType.

8.7.3. Application Interface

When the end-point's PTP clock is synchronized to the PTP Master clock, its time information and local clock can be provided to peripheral time applications that need to work simultaneously with the central clock. The RTL9000BF/BN/BS features these PTP Application Interfaces in the following, via the PTP_GPIO pin:

Event Capture Interface

- Monitors the PTP_GPIO pin, and records the timestamp of incoming pulses, edges, or time alignment signals, similar to a stopwatch.

Trigger Generate Interface

- Arms the PTP_GPIO pin to generate a pulse, edge, or periodic clock signal at a specific time, similar to an alarm clock. The periodic clock has configurable period and duty cycles.

External Reference Clock Interface

- PTP local clock can also be referred to the external clock source with frequency 10M/25M/125MHz via the PTP_GPIO pin.

Note 1: The PTP_GPIO pin works as one application interface at a time.

Note 2: The application interface can refer to the PTP clock or the Local clock.

The PTP application interface configurations can be set by the related registers (section 9.3.10 to 9.3.16, pages 120~122).

8.7.4. PTP Function Configuration Flow

8.7.4.1 STEP 1: Enable & Disable PTP Function

[STEP 1-1] PTP capability configuration registers are defined in section 9.3.1, page 116, including protocol support types and the PTP enable register. It usually sets the capability at the initial stage of the PTP program.

[STEP 1-2] After setting the PTP capability (PTP_CTL register), a software reset must be issued (Reg 0, bit [15] = 1) to start the PTP function.

8.7.4.2 STEP 2: PTP Synchronization Mechanisms

There are two PTP synchronization mechanisms: *Delay request-response mechanism* and *Peer delay mechanism*. Both have **Two-Step** and **One-Step** operation as illustrated below:

Note 1: In the following figures, the time tags e.g. ‘ t_1 ’, represent the ingress or egress timestamp of the corresponding PTP Event Message (shown in the middle of the arrows); while ingress/egress depends on the direction of each arrow. E.g. ‘ t_1 ’ on the upper left side in Figure 27, page 41 means the egress timestamp of the Sync message issued by the PTP Master.

Note 2: The time tags inside parentheses, e.g. ‘ (t_1) ’, mean the timestamp information that is carried by the specified PTP Event Message. E.g. ‘Follow_Up (t_1)’ on the upper left side in Figure 27, page 41 represents the Follow_Up packet containing the Sync egress timestamp information.

- Two-Step PTP Synchronization:

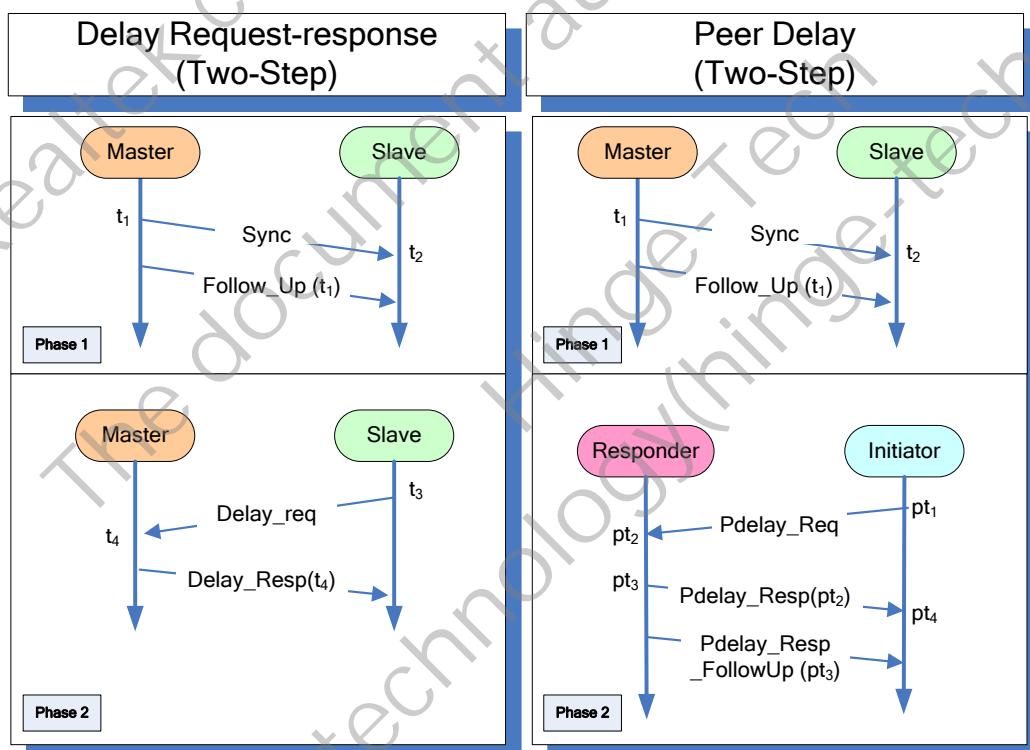


Figure 27. Two-Step PTP Synchronization Mechanisms

- One-Step PTP synchronization mechanisms:

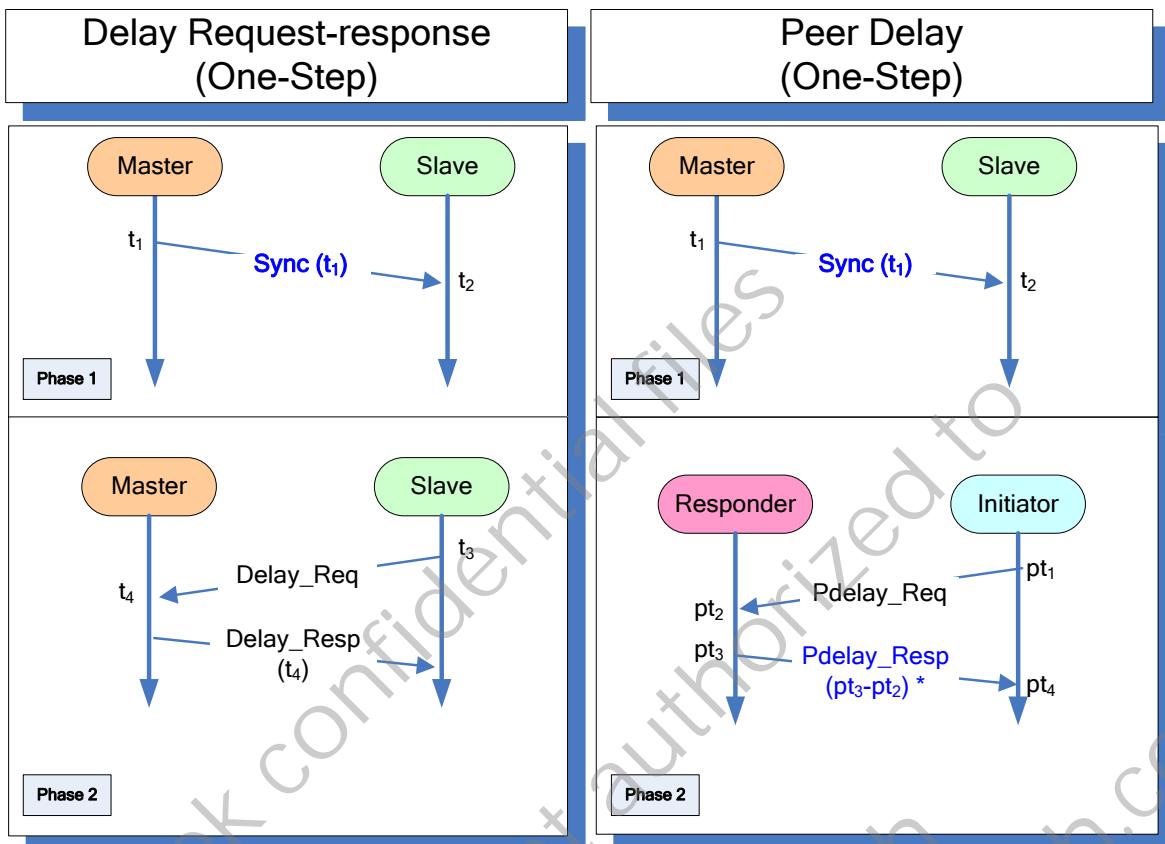


Figure 28. One-Step PTP Synchronization Mechanisms

Read Transmit (Egress) / Receive (Ingress) Timestamps ($t_1 \sim t_4$; $pt_1 \sim pt_4$)

The timestamp is recorded by the RTL9000BF/BN/BR/BS/BSS after receiving or transmitting a PTP Event Message packet.

Before reading the timestamp value, the READY flags should be checked first. If the READY flag is set, it means the timestamp is prepared and recorded completely, defined at bit [15:8] in section 9.3.18, page 123.

Furthermore, there are interrupts related to the READY flags. The interrupts can be enabled by the PTP_INER register (section 9.3.2, page 117) and the interrupt status is shown by PTP_INSR register (section 9.3.3, page 117).

After confirming the READY flag is asserted for the specified timestamp, we must select the protocol message type and the message direction (Transmit/Receive) for the corresponding timestamp. Then set the Transmit/Receive Timestamp Read Enable bit. These registers are defined in bit[4:0] of PTP_TRX_TS_STA register, section 9.3.18, page 123. After a timestamp read is done, the read enable bit will self-clear and the corresponding READY flag will be cleared, too.

The detailed timestamp information is shown in PTP TX/RX Timestamp registers (see section 9.3.17 to 9.3.25, page 122~125).

The PTP version is shown by ‘trxts_ptpver’ and ‘trxts_transpec’ fields in Table 106, page 123.

- For IEEE 1588 ver.1: trxts_ptpver = 1
- For IEEE 1588 ver.2: trxts_ptpver = 2; trxts_transpec = 0
- For IEEE 802.1AS: trxts_ptpver = 2; trxts_transpec = 1

The PTP packet type will be indicated by ‘trxts_msgtype’ in Table 106.

Table 13. Summary of PTP Packet Types

Value of ‘trxts_msgtype’ (in HEX)	IEEE 1588 v1 Packet Type	IEEE 1588 v2 & 802.1AS Packet Type
0	Sync	Sync
1	Delay_Req	Delay_Req
2	Follow_Up	Pdelay_Req
3	Delay_Resp	Pdelay_Resp
4-7	Management	Reserved
8	-	Follow_Up
9	-	Delay_Resp
A	-	Pdelay_Resp_Follow_Up
B	-	Announce
C	-	Signaling
D	-	Management
E-F	-	Reserved

The PTP clock timestamp is in PTP_TRX_TS register (sections 9.3.21 ~ 9.3.25), the local clock timestamp is in LOCAL_TRX_TS register (sections 9.3.26 ~ 9.3.30)

8.7.4.3 STEP 3: Offset and Delay Calculation

Calculation of Offset_from_Master

The time offset between a Slave and a Master clock is defined as follows:

$$\text{Offset_from_Master} = t_2 - t_1 - \text{Mean_Path_Delay}$$

Calculation of Mean_Path_Delay

- For the *Delay request-response mechanism*:

Calculate the timestamp by using both Phase 1 & Phase 2 stage

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

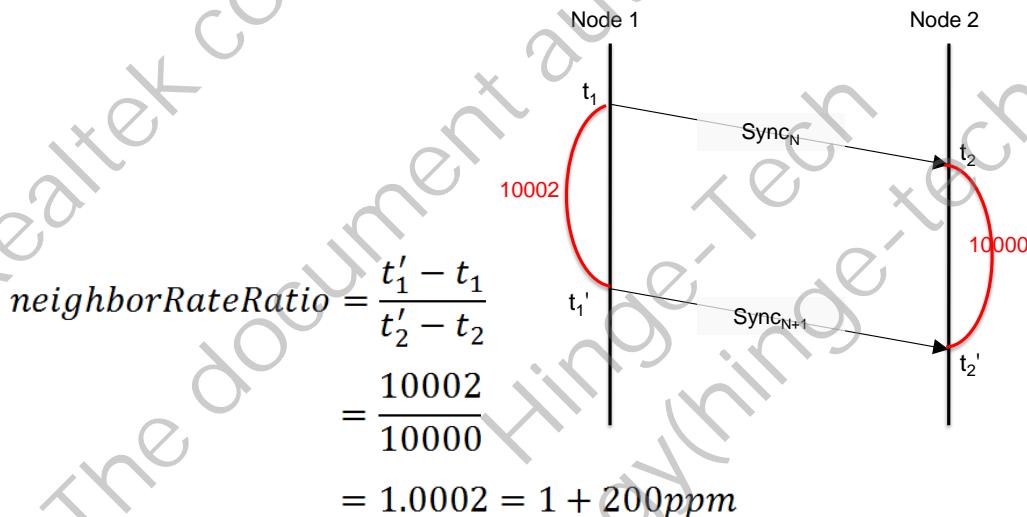
- For the *Peer delay mechanism*:

Calculate the timestamp at Phase 2 stage

$$\text{MeanPathDelay} = \frac{(pt_4 - pt_1) - (pt_3 - pt_2)}{2}$$

*Note: For the RTL9000BF/BN/BR/BS/BSS, PDelayResp one-step correctionField update will not exactly match <PDelayResp Egress Timestamp (pt3) > - <PDelayReq Ingress Timestamp (pt2) >. As a more accurate timer with resolution 2^{-3} ns is used to calculate the value, the difference would be smaller than 1ns compared to the result of <PDelayResp Egress Timestamp (pt3) > - <PDelayReq Ingress Timestamp (pt2) >.

Calculation of Rate_Drift



$$\begin{aligned} \text{neighborRateRatio} &= \frac{t'_1 - t_1}{t'_2 - t_2} \\ &= \frac{10002}{10000} \\ &= 1.0002 = 1 + 200\text{ppm} \end{aligned}$$

Figure 29. Calculation of neighborRateRatio

If the time is adjusted between the two timestamps, the interval calculation should compensate the adjustment. For another example, assume t2 is 100, and the sync process added a 1000 offset to PTPclock. Then assume t2' is 1205; assume t1: 1100, t1' = 1200; then rateRatio is $(1200 - 1100)/(1205 - 100 - 1000) = 100/105$ (with compensation) instead of $100/1105$ (without compensation).

8.7.4.4 STEP 4: Set PTP Local Clock Time

Set PTP Local Clock Time

There are three modes for PTP clock adjustment of PTP Local Time:

- (1) Direct Read/Write clock
- (2) Increment/Decrement Step Adjustment
- (3) Rate Adjustment

The register is defined at section 9.3.4 PTP_CLK_CFG (PTP Clock Config Register, Address 0xE410), page 117 – bit [3:1].

In addition, the desired adjustment value should be entered in PTP Time Config registers (section 9.3.5 to 9.3.9, pages 118 to 119).

After setting the PTP Clock adjustment value, set the PTP clock adjustment Activate bit. The register bit is defined at bit [0] of PTP_CLK_CFG register (i.e. set Address 0xE410, bit [0] = 1).

Note 1: We suggest that the time latency from the ‘Egress Timestamp point’ to the MDI, and from the MDI to the ‘Ingress Timestamp point’ should all be taken into account in order to attain more accurate PTP clock tuning.

Note 2: The Direct Write would be another suitable method for an initialization where a setup with a whole new time value is needed.

Note 3: Example of rate adjustment:

*Assume rateRatio shows that the slave should speed up by 1 ppm to synchronize frequency with the master. We can convert this to a register value by ppm / unit = 1ppm / 2⁻³² ns = 4294.967 ~= 4295. Then we can write this rate-to-rate adjustment. The meaning is that the slave needs to speed up 4295 * 2⁻³²ns each tick (8ns).*

Read PTP Local Clock Time

To read out local time of the PTP clock, set bit [3:1] = 3'b010, and then issue the Activate bit (bit[0]) in PTP_CLK_CFG register. After these settings, the PTP local time would be shown in PTP Time Config registers (sections 9.3.5 to 9.3.9, pages 118 to 119).

8.7.4.5 STEP 5: PTP Application Interface Configuration

The RTL9000BF/BN/BS supports different PTP Application Interfaces. There are four modes for the related configurations:

- (1) Function Disabled
- (2) Trigger Generate
- (3) Event Capture
- (4) Read Trigger Start Time/Event captured timestamp (according to current PTP_GPIO settings)

The configuration can be set by bit [2:1] of 9.3.10 PTP_TAI_CFG (PTP Application I/F Config Register, Address 0xE420), page 120. Detailed description as follows:

Set PTP Application Interfaces

- If the PTP Application interface configuration mode is ‘Trigger Generate’

The Trigger start time is specified in PTP Application I/F Timestamp registers (section 9.3.13 to 9.3.16, page 121 to 122).

The Trigger Generate mode can be by Address 0xe420, bit[9:8] (PTP_TAI_CFG register, section 9.3.10, page 120) for edge, pulse, or periodic type selection.

The duty cycle, unit, and period of a trigger signal also can be specified in the PTP_TRIG_CFG register (section 9.3.11, page 121). The period would be represented as ‘pulse_amt * pulse_amt_unit’. Please note when ‘pulse_amt’ is set < 8, the RTL9000BF/BN/BS only supports ‘50%’ duty cycle configuration for periodic trigger function due to the limitation of clock frequency.

After the PTP Application I/F Activate bit is set (Address 0xE420, bit [0] = 1), the GPIO trigger function will start working.

[Example]: If a periodic pulse per sec (PPS) signal is desired to be generated, with period = 1 sec, duty cycle = 50%, after 10 seconds from now. Registers should be set as below:

(1) Read current PTP Clock time by setting Address 0xE410 (PTP_CLK_CFG register)

- bit [3:1] = 3'b010 (Direct Read mode)
- bit [0] = 1'b1 (activate the Direct Read)

Then access the current PTP local time from Address 0xE412~0xE41A (PTP Time Config registers); e.g., assume, current time is X.

(2) Set the trigger start time to be ‘current time plus 10 seconds’ (i.e. X+10 sec) into corresponding PTP App. I/F Timestamp registers (section 9.3.13 to 9.3.16, pages 121 to 122).

(3) Set Address 0xE420 (PTP_TAI_CFG register)

- bit [9:8] = 2'b11 (trigger type is periodic pulse)
- bit [4:3] = 2'b00 (GPIO #0)
- bit[2:1] = 2'b01 (select to trigger generate function)

(4) Set the parameters of this periodic pulse by Address 0xE422 (PTP_TRIG_CFG register)

- bit [13:12] = 2'b10 (50% duty cycle)
- bit[11:10] = 2'b10 (pulse_amt_unit = 1.25 ms)
- bit[9:0] = 0x8 (pulse_amt = 8; i.e. period = 8 * 1.25ms = 1 sec)

(5) Set PTP Application I/F Activate bit: Address 0xE420 (PTP_TAI_CFG register)

- bit [0] = 1 (activate the trigger)

Finally the PPS signal will be output at PTP_GPIO pin at time (X + 10 sec).

*Note: Due to the time needed for hardware to process the trigger setting, some fixed latency would be induced from the specified 'trigger start time' to the trigger actually starting. The value is 6 * PTP_CLK period, that is, 90 ns. Users should take this offset into account when setting the 'trigger start time'.*

● If the PTP Application interface configuration mode is Event Capture

We can set the Event Generate mode at Address 0xE420, bit [6] = 1 for edge type selection.

After the PTP Application I/F Activate bit is set (Address 0xE420, bit [0] = 1), the Event Capture function will start.

The event capture time is specified in PTP Application I/F Timestamp registers (section 9.3.13 to 9.3.16, pages 121 to 122).

**Note 1: Users should always disable the current function of the PTP_GPIO pin before setting a new Application Interface function.*

**Note 2: If a PHY reset is asserted during the PTP_GPIO armed (e.g. periodic pulses are toggling), after the reset, PTP Application I/F Activate bit (Address 0xE420, bit [0]) should be set again in order to restart the same PTP_GPIO configuration.*

Read PTP Application Interface Timestamp

The PTP Application I/F Timestamp registers are defined in section 9.3.13 to 9.3.16, page 121 to 122. The value can be read or write, depending on the PTP Application interface configuration.

8.7.4.6 PTP Reference Clock Input

The RTL9000BF/BN/BS provides the option that the local PTP clock can be sourced from an external reference clock, e.g. a GPS-based clock, with frequencies of 10M, 25M, and 125MHz supported.

To enable the reference clock input mode, follow the steps below:

- (1) Disable the Application Interface functions at PTP_GPIO of the RTL9000BF/BN/BS
- (2) Connect the external reference clock to the PTP_GPIO pin
- (3) Select the frequency of the input reference clock by bit[6:5] of PTP_CLK_CFG register (see 9.3.4, page 117), and enable the clock input function by asserting bit[4] =1
- (4) Issue a software reset (Reg 0, bit [15] = 1) to allow the setting take effect.

Note: The maximum jitter of the external clock should be within 400 ps.

8.7.4.7 STEP 6: Disable PTP Function

[STEP 6-1] As with STEP 1, the PTP function can be disabled by the PTP_CTL registers in section 9.3.1, page 116, by setting all of the enable bits to 0.

[STEP 6-2] After disabling the PTP function, a software reset shall also be issued (Reg 0, bit [15] = 1) to take effect.

8.7.5. PTP Sample Flow

In this section, we provide two examples for implementing the PTP synchronization coding by the upper layer, and the negotiation between the PTP Master and Slave:

IEEE 802.1AS Peer Delay Two-Step mode; and

IEEE 1588 ver.2 Peer Delay One-Step mode

8.7.5.1 IEEE 802.1AS Peer Delay Two-Step Mode

The following figure shows an overview of the PTP handshaking protocol: IEEE 802.1AS Peer Delay Two-Step operation:

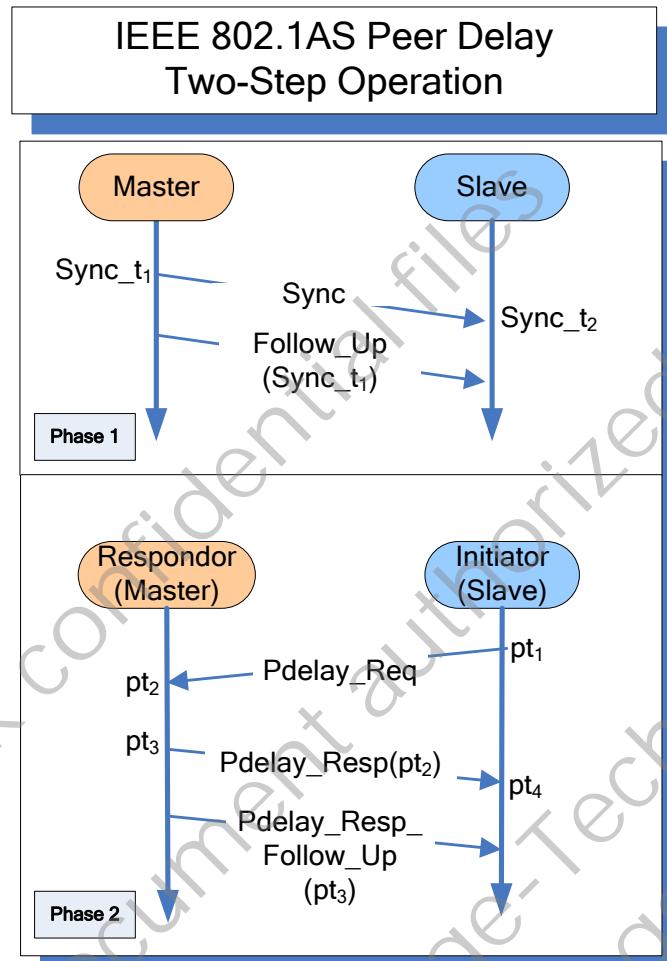


Figure 30. IEEE 802.1AS Peer Delay Two-Step Operation

In Figure 31 we illustrate the sample flow chart by the main function and each detailed sub-functions of the PTP Master and Slave, separately, based on IEEE 802.1AS Peer Delay Two-Step protocol. The Master transmits PTP Event Messages per second, that is, Sync interval = 1 second. Corresponding Steps and Phases mentioned by previous sections are also listed accordingly:

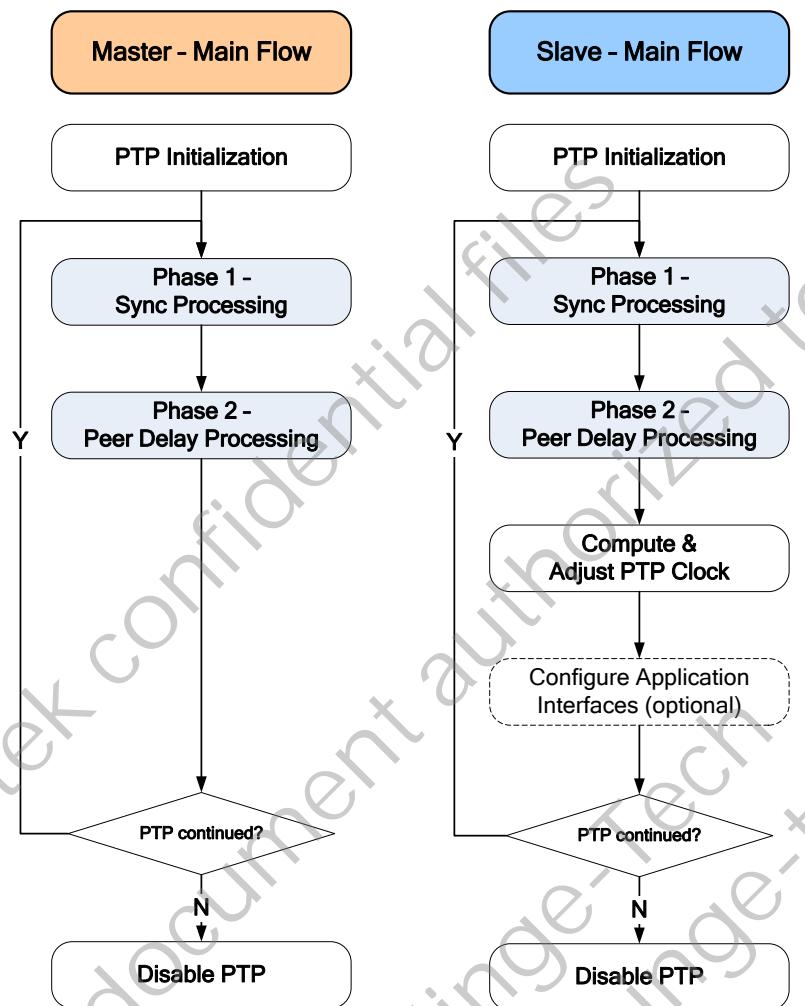


Figure 31. Master & Slave Main Flow Chart of IEEE 802.1AS Peer Delay Two-Step

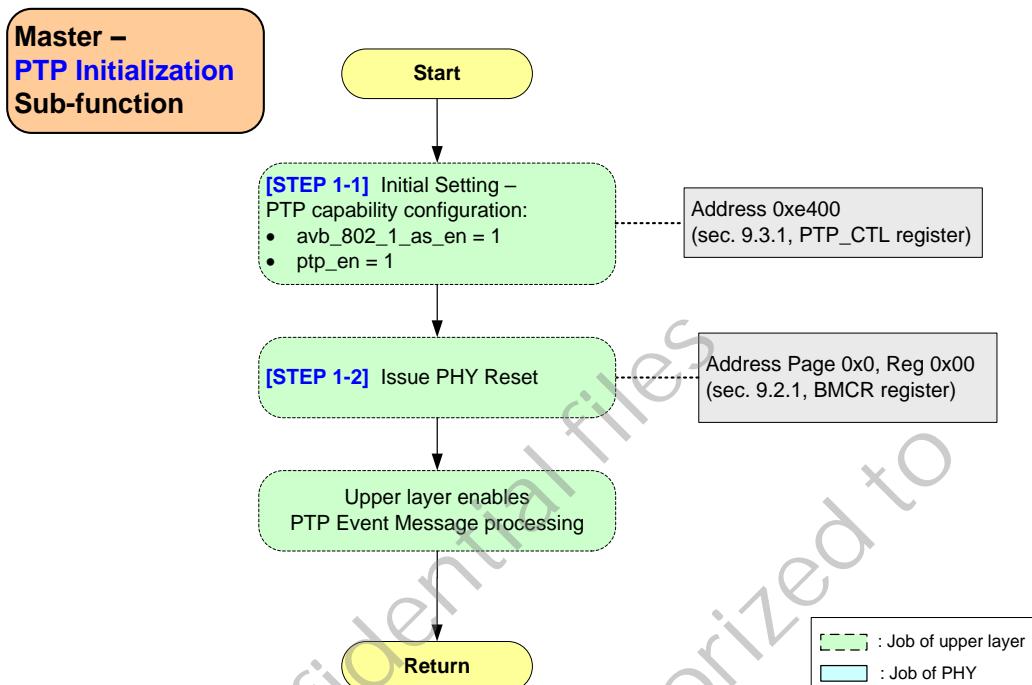


Figure 32. Master PTP Initialization Sub-Function of IEEE 802.1AS Peer Delay Two-Step

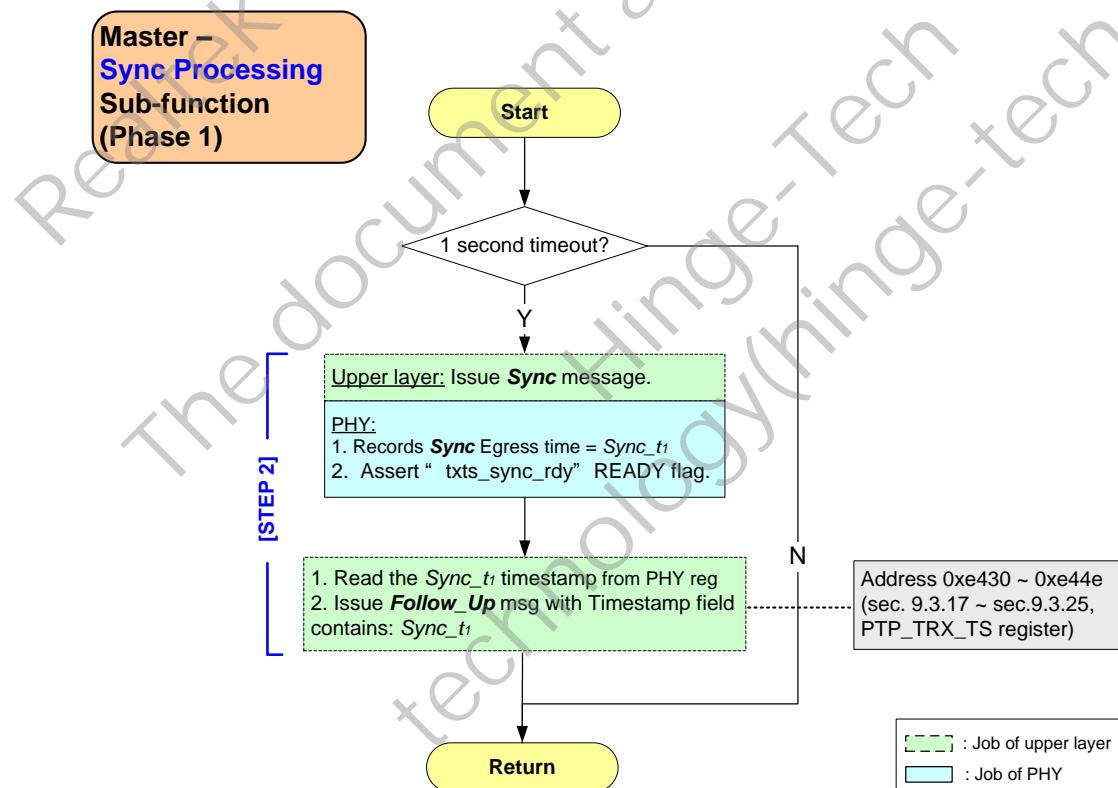


Figure 33. Master Sync Processing Sub-Function of IEEE 802.1AS Peer Delay Two-Step

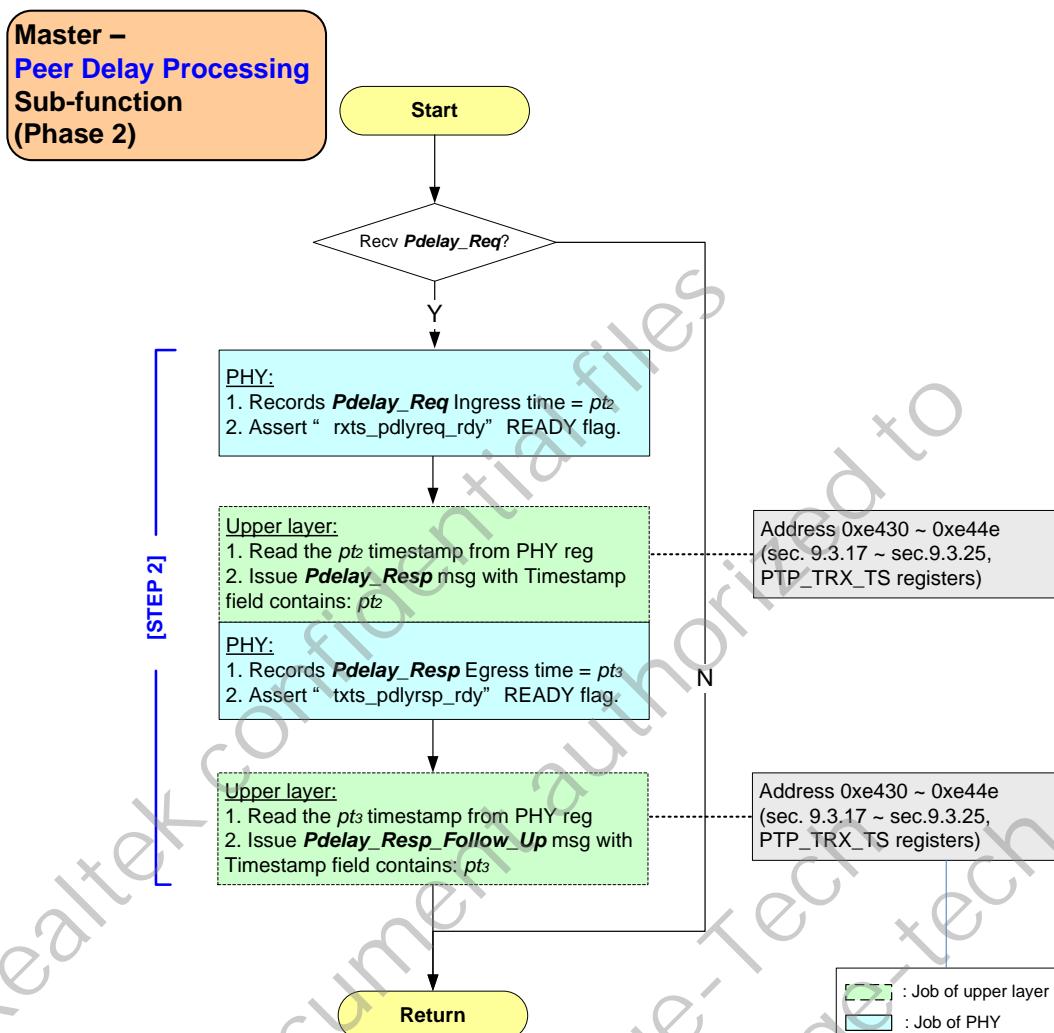


Figure 34. Master Peer Delay Processing Sub-Function of IEEE 802.1AS Peer Delay Two-Step

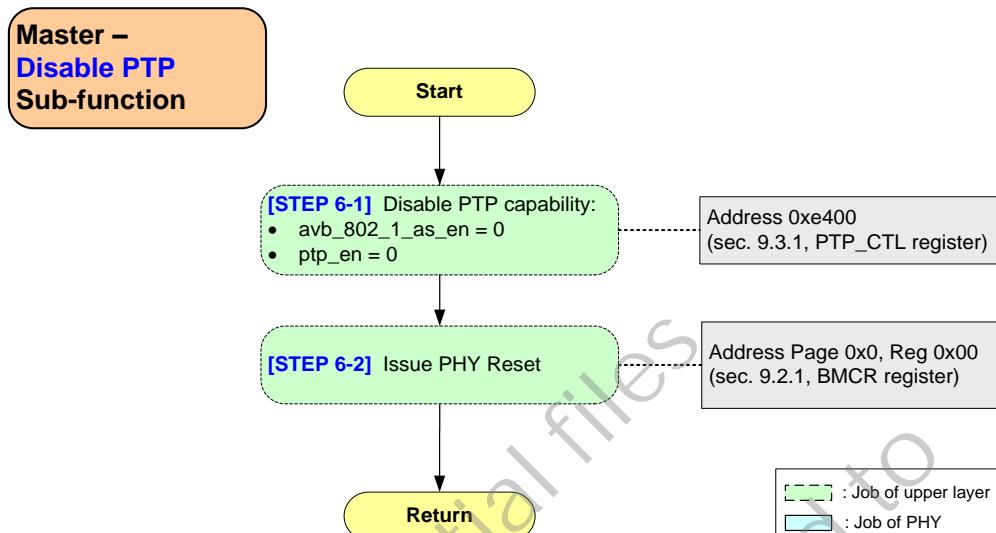


Figure 35. Master Disable PTP Sub-Function of IEEE 802.1AS Peer Delay Two-Step

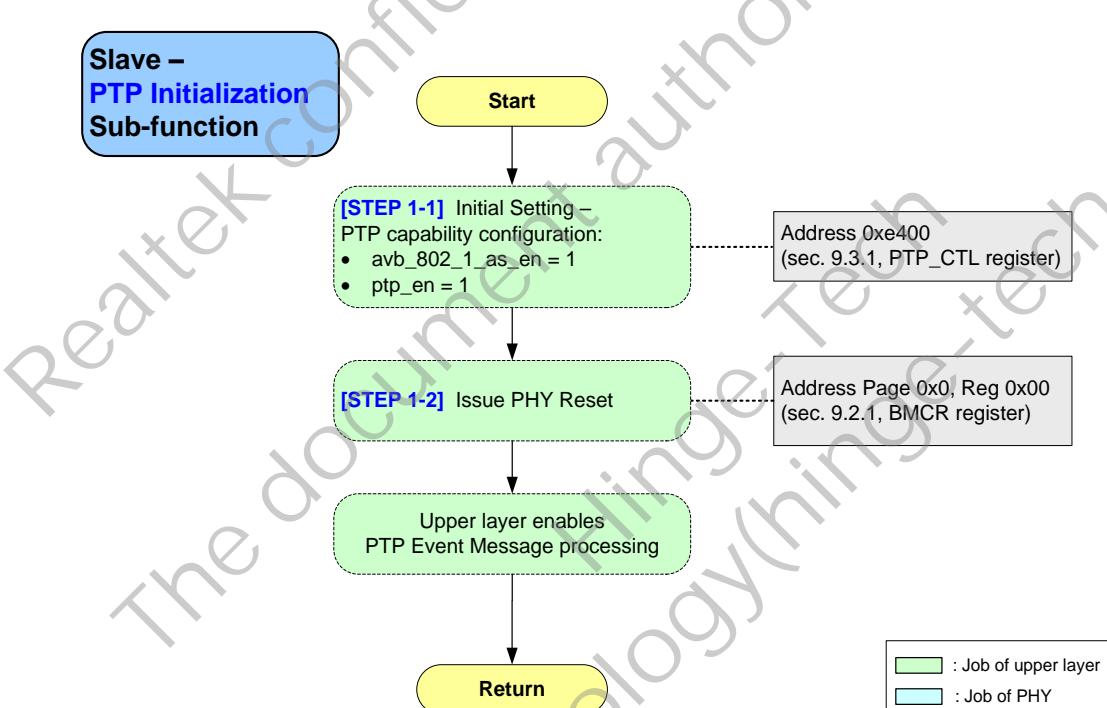


Figure 36. Slave PTP Initialization Sub-Function of IEEE 802.1AS Peer Delay Two-Step

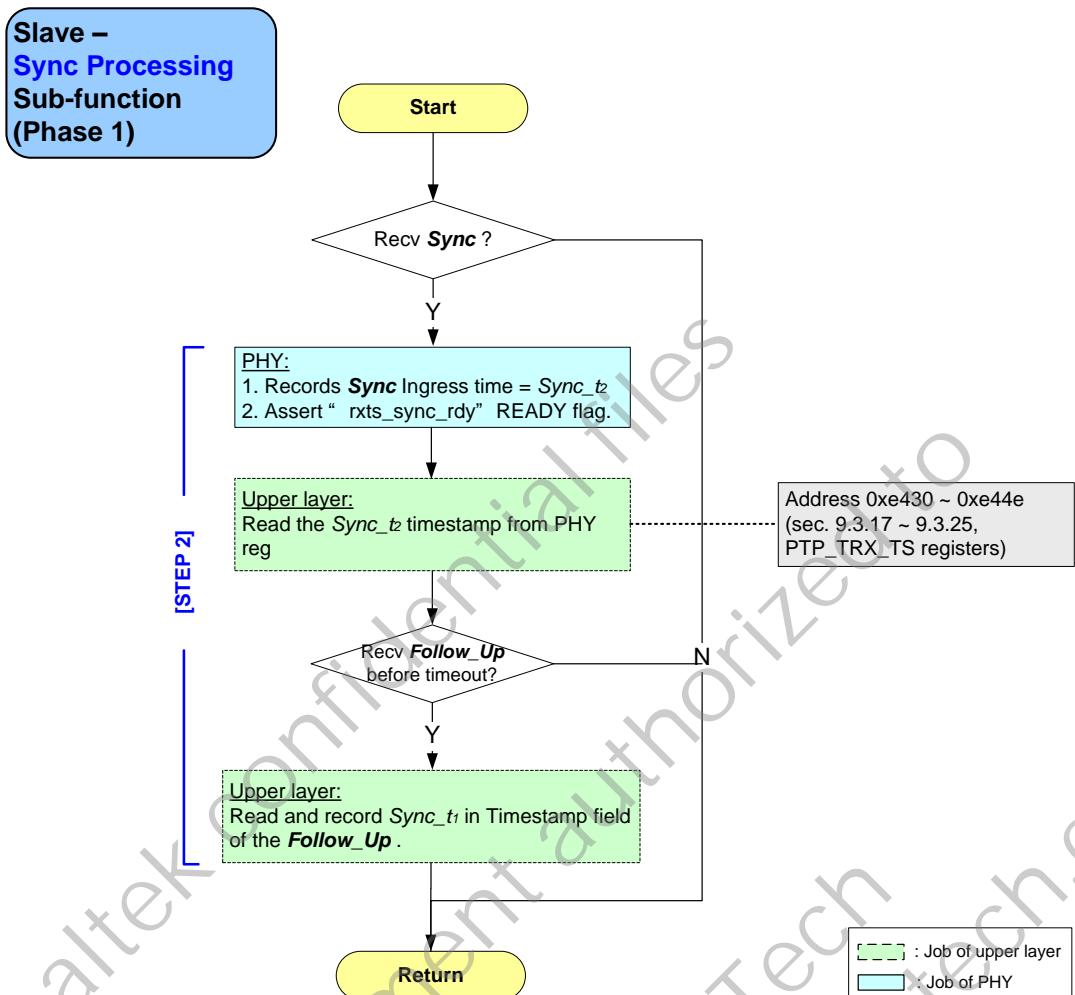


Figure 37. Slave Sync Processing Sub-Function of IEEE 802.1AS Peer Delay Two-Step

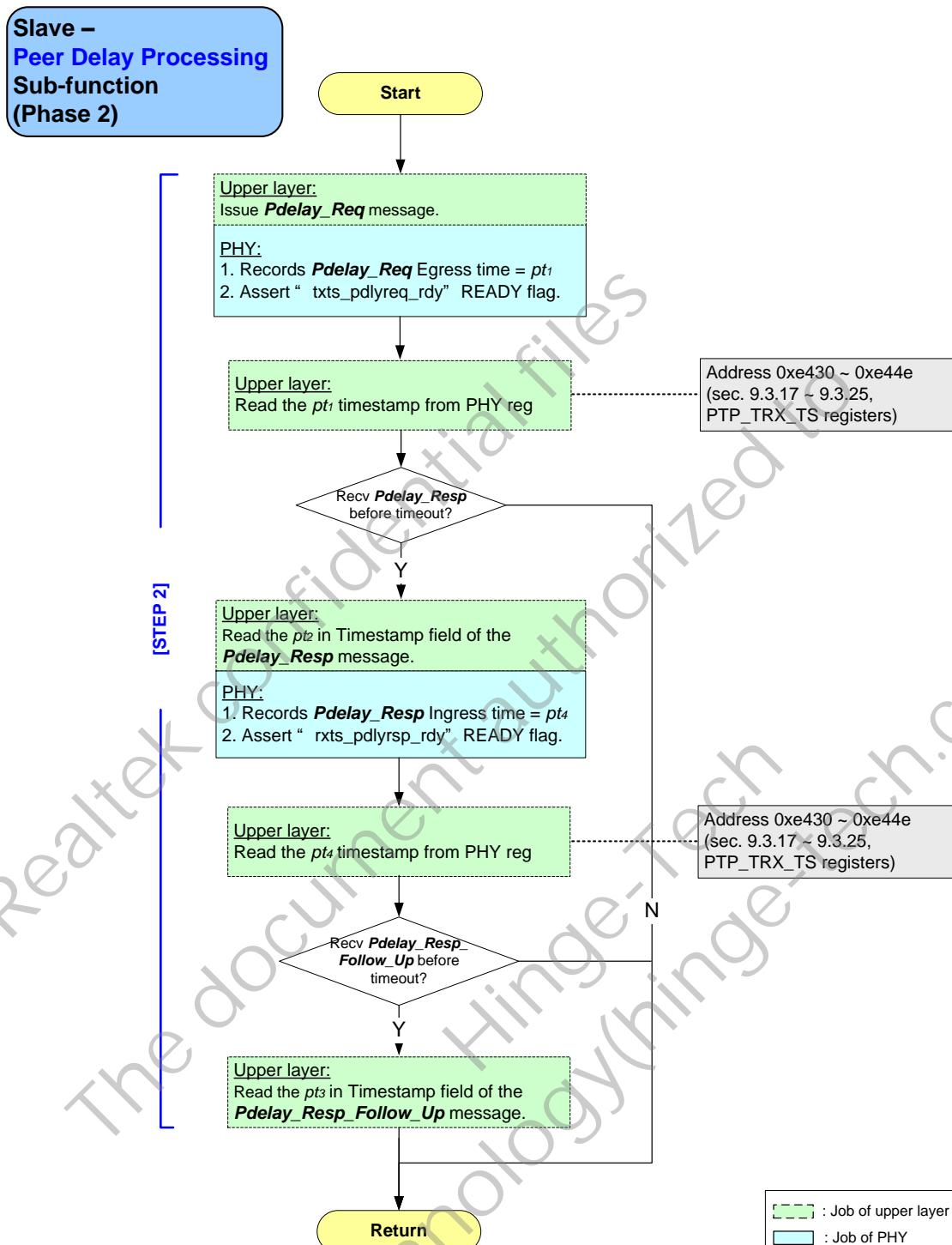


Figure 38. Slave Peer Delay Processing Sub-Function of IEEE 802.1AS Peer Delay Two-Step

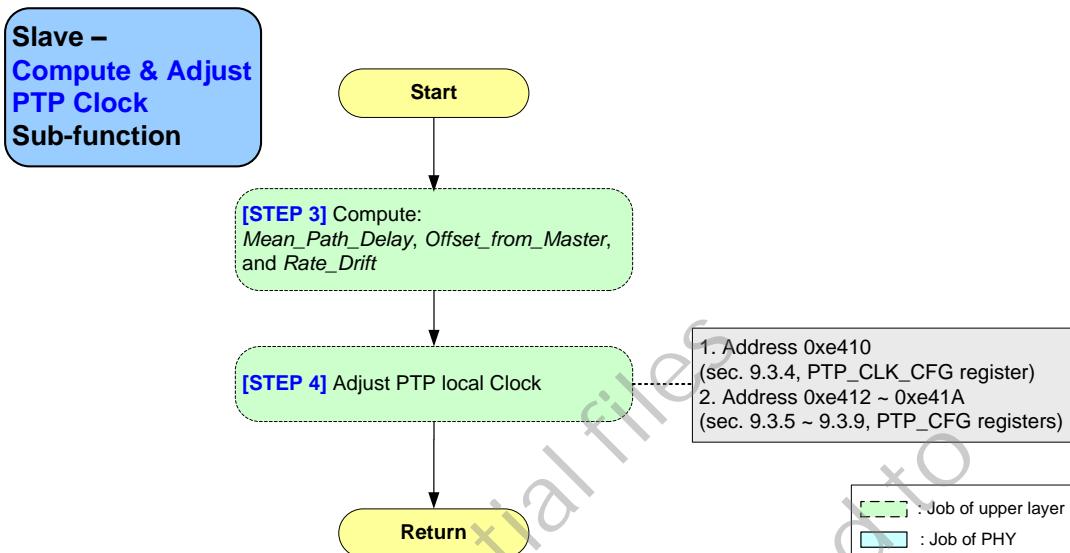


Figure 39. Slave Compute & Adjust PTP Clock Sub-Function of IEEE 802.1AS Peer Delay Two-Step

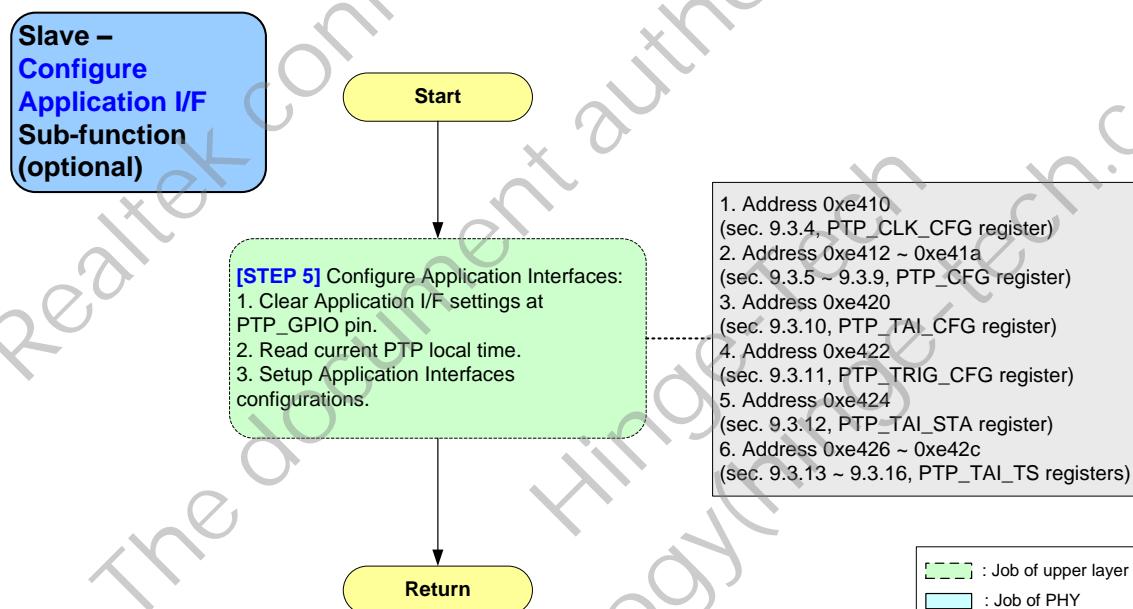


Figure 40. Slave Configure Application I/F Sub-Function of IEEE 802.1AS Peer Delay Two-Step

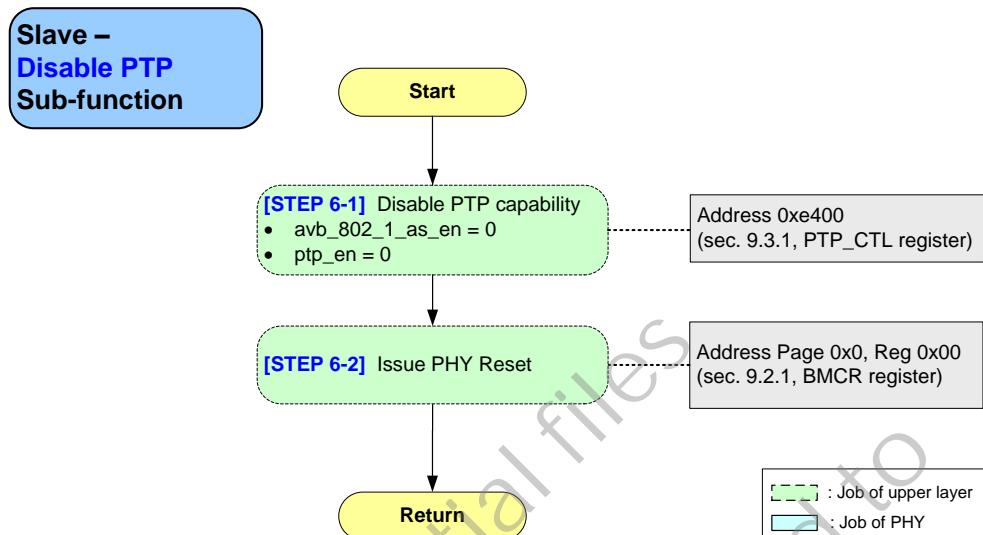


Figure 41. Slave Disable PTP Sub-Function of IEEE 802.1AS Peer Delay Two-Step

8.7.5.2 IEEE 1588 ver.2 Peer Delay One-Step Mode

The following figure shows an overview of the PTP handshaking protocol: IEEE 1588 ver.2 Peer Delay One-Step operation:

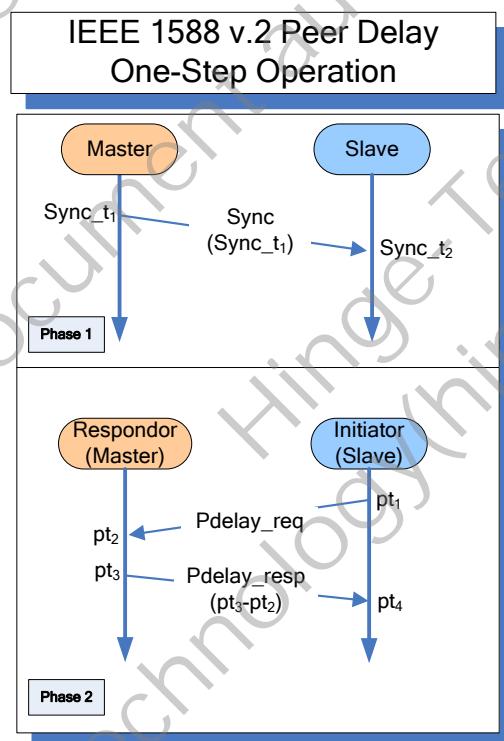


Figure 42. IEEE 1588 Peer Delay One-Step Operation

We also illustrate the sample flow chart by the main function and each detailed sub-function of the PTP Master and Slave, separately, based on IEEE 1588 Peer Delay One-Step protocol. The Master transmits PTP Event Messages per second, that is, Sync interval = 1 second. Corresponding Steps and Phases mentioned by previous sections are also listed accordingly.

The main function flow would look the same as IEEE 802.1AS Peer Delay Two-Step operation in Figure 43. In the following, the sub-functions are directly presented:

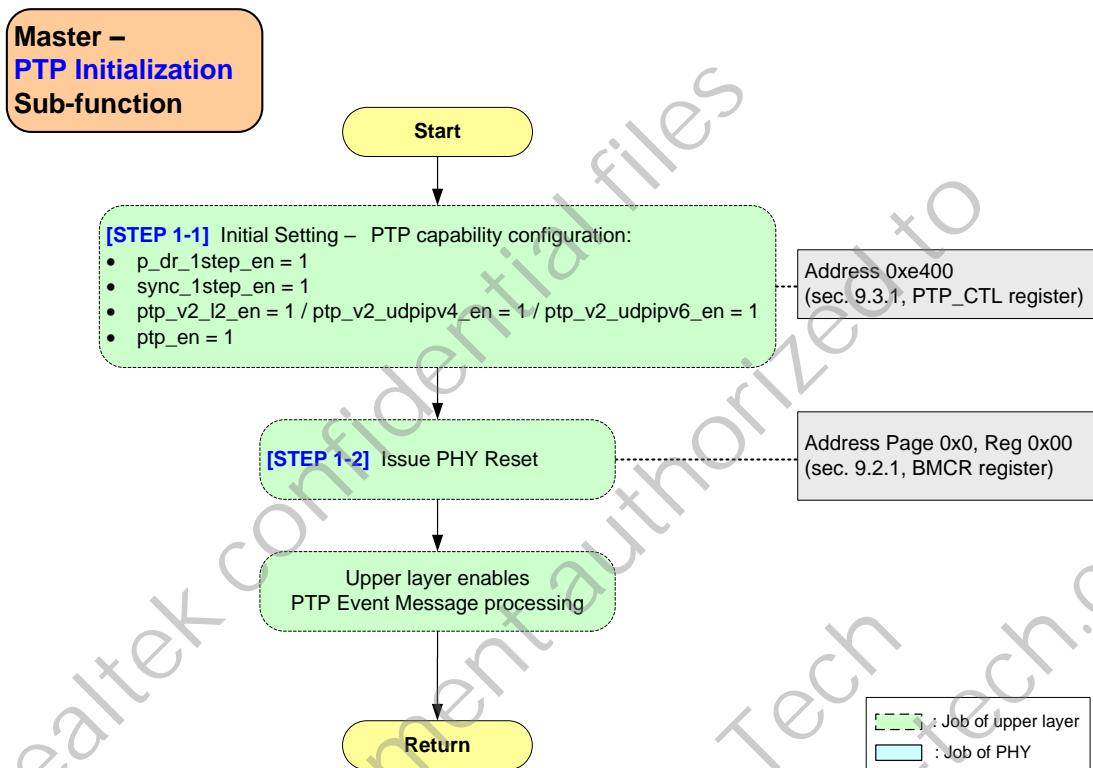


Figure 43. Master PTP Initialization Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

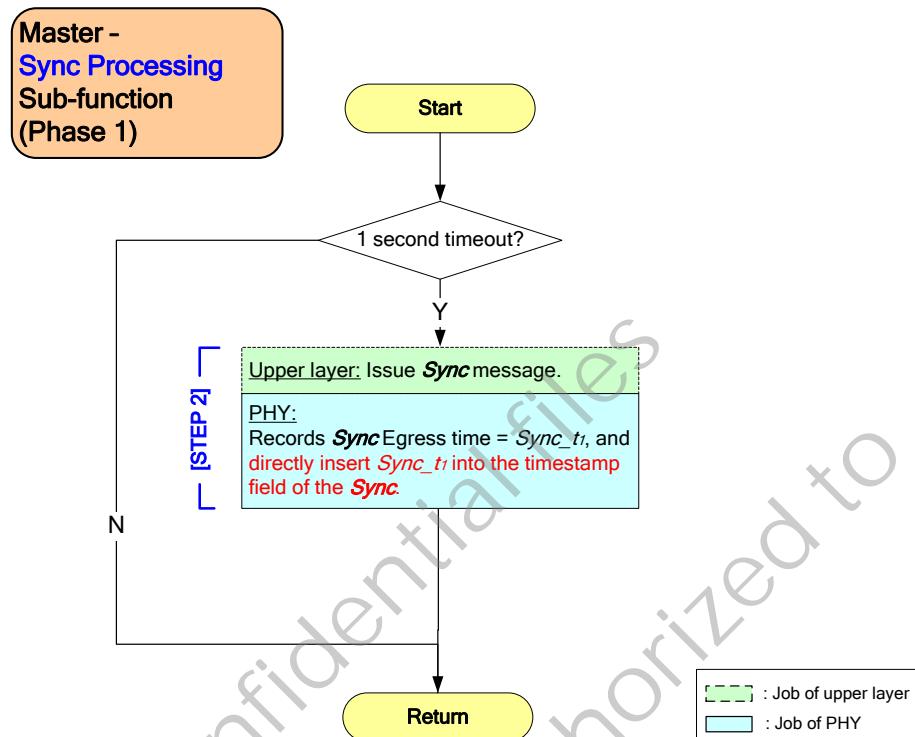


Figure 44. Master Sync Processing Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

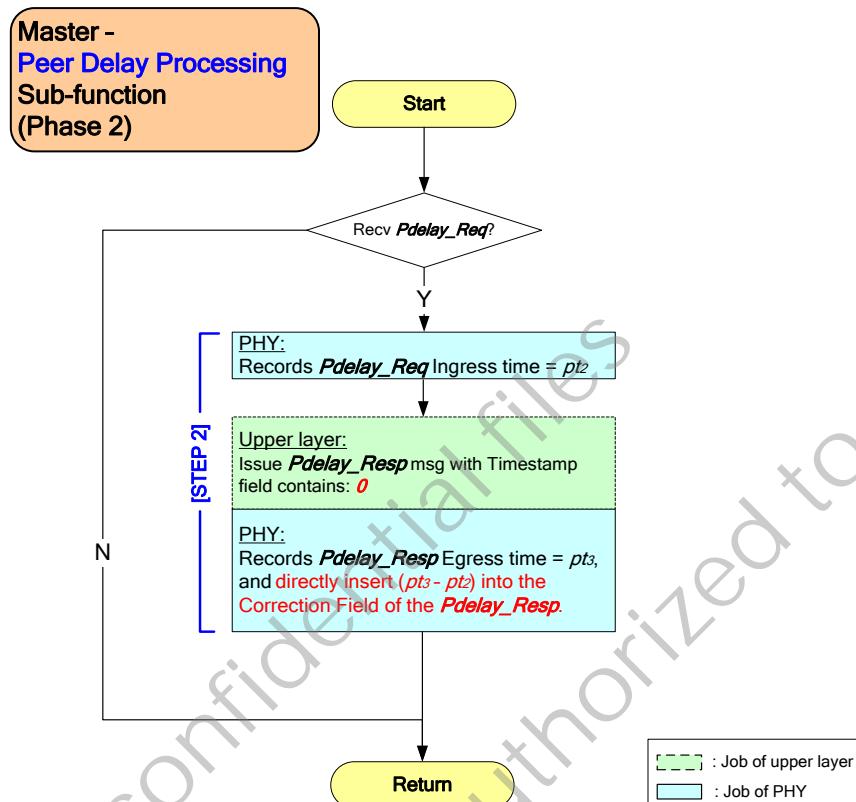


Figure 45. Master Peer Delay Processing Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

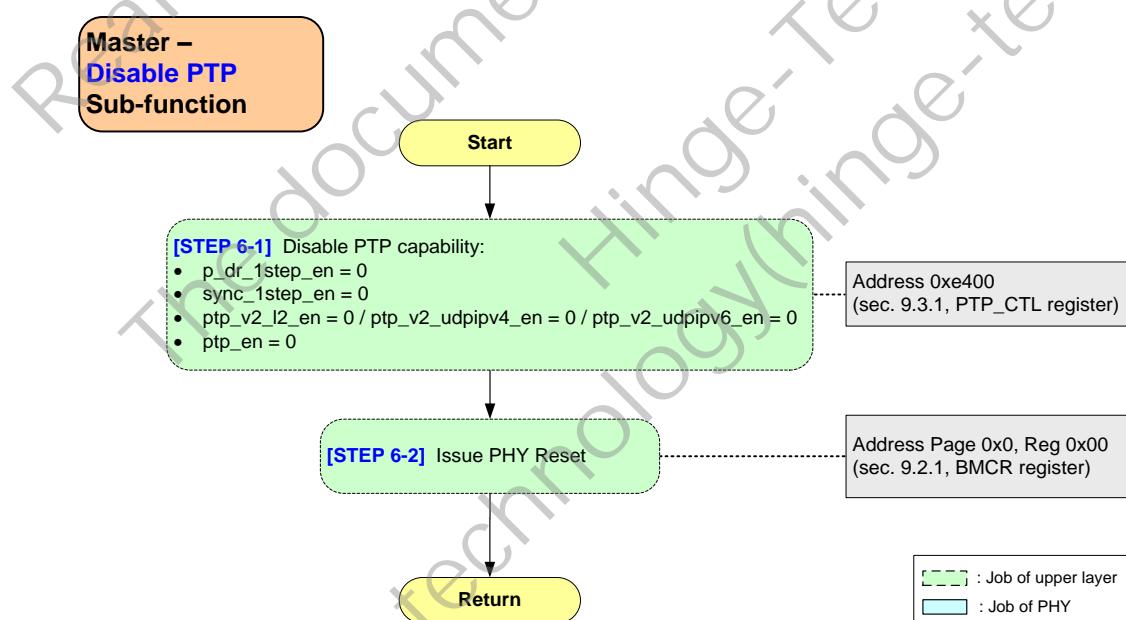


Figure 46. Master Disable PTP Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

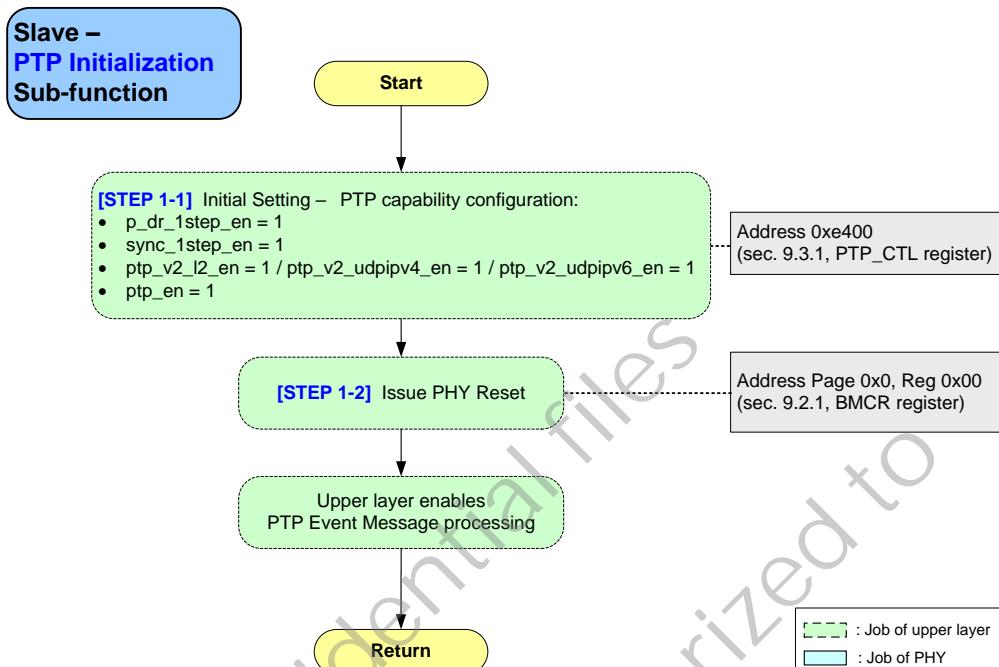


Figure 47. Slave PTP Initialization Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

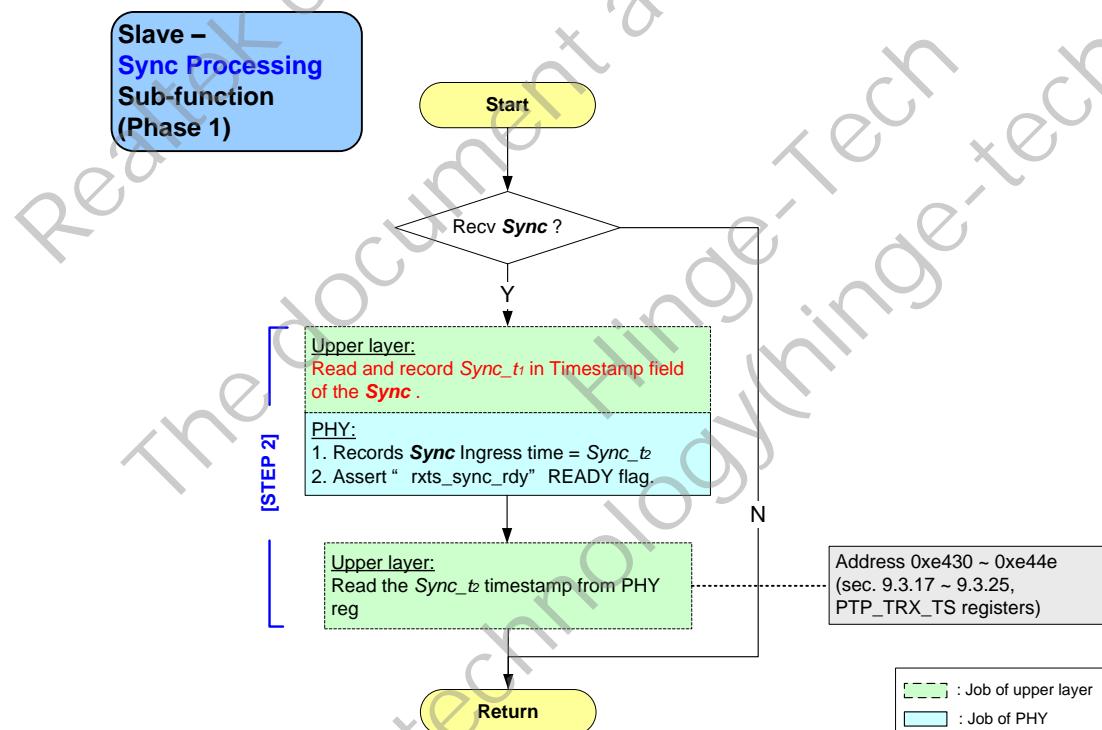


Figure 48. Slave Sync Processing Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

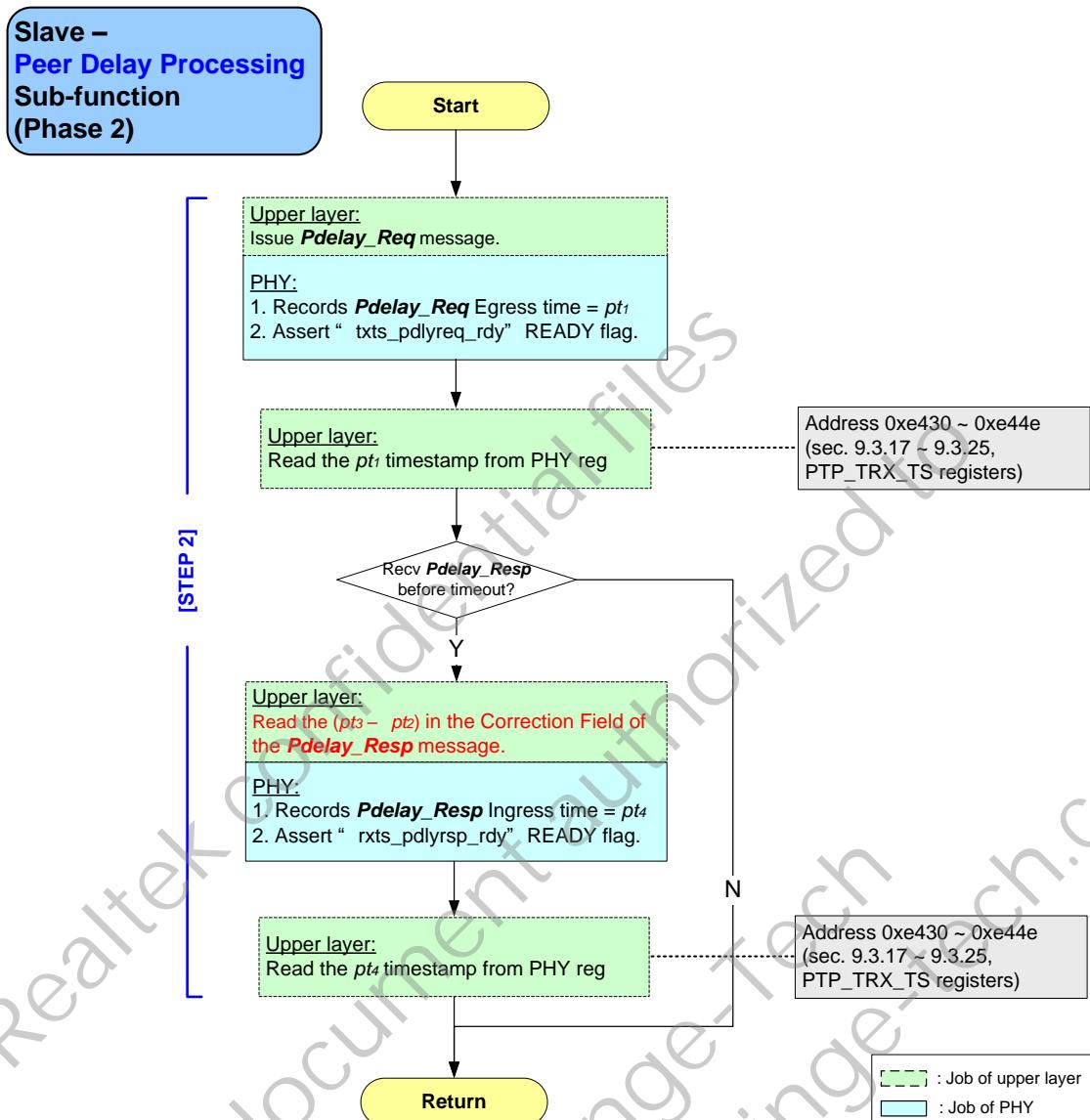


Figure 49. Slave Peer Delay Processing Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

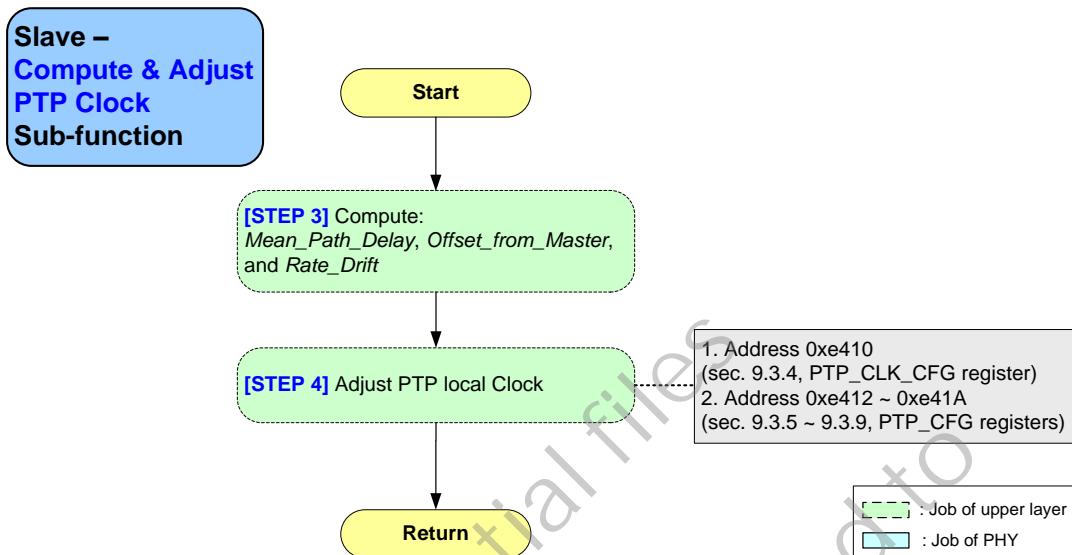


Figure 50. Slave Compute & Adjust PTP Clock Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

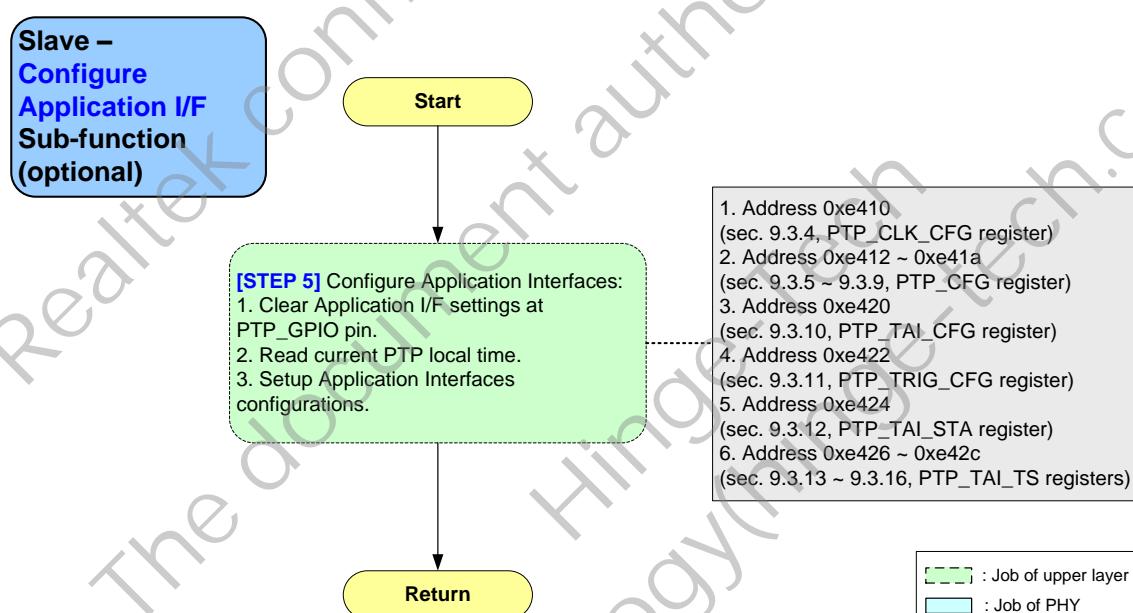


Figure 51. Slave Configure Application I/F Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

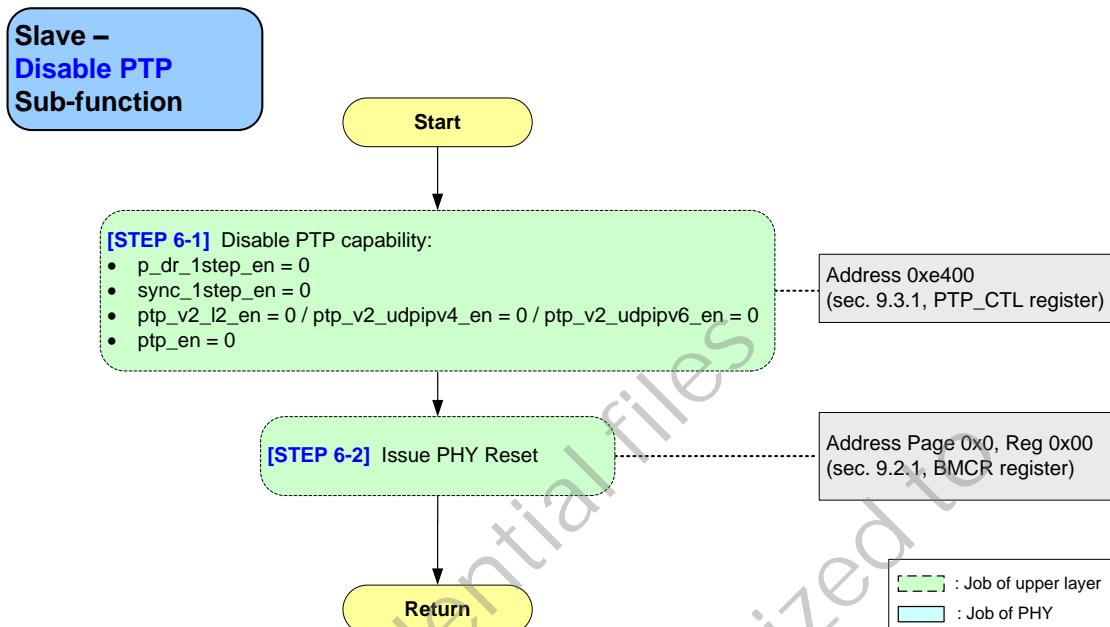


Figure 52. Slave Disable PTP Sub-Function of IEEE 1588 ver.2 Peer Delay One-Step

8.8. Interrupt

The RTL9000BF/BN/BR/BS/BSS provides an interrupt function with an active low interrupt output pin (INTB) to inform the MAC about changes or errors in the PHY status. The interrupt function of the RTL9000BF/BN/BR/BS/BSS uses a level-triggered mechanism. To use the interrupt function of the RTL9000BF/BN/BR/BS/BSS properly, three types of interrupt control should be taken into account:

1. Interrupt Enable Register

The interrupts can be individually enabled or disabled by setting or clearing bits in the following interrupt enable registers:

- General Interrupt enable register – GINER (General Interrupt Enable Register, Page 0xA42, Reg 0x12), page 97
- OP Interrupt enable registers –
- OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C), OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14), and OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C)

With a dedicated interrupt enabled, the corresponding interrupt status register bit will be recorded ‘1’ if an event occurred.

2. Interrupt Mask

The interrupt mask function provides more flexible usage. With the ‘mask’ of the specified interrupt enabled, when the corresponding event occurs it will be recorded in the interrupt status register of the RTL9000BF/BN/BR/BS/BSS, however the MAC will not be informed through the INTB pin until the mask is disabled.

General Interrupt mask register – GINMR (General Interrupt Mask Register, Page 0xA42, Reg 0x14)

- GINMR (General Interrupt Mask Register, Page 0xA42, Reg 0x14), page 98.
- OP Interrupt mask registers – OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E)OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E), OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16)OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16), and OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E).OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E).

3. Interrupt Status Register

Every General Interrupt condition is represented by the general interrupt status register; while the Operating Mode related statuses like UV recovery, Sleep/Wake up events, Reset event, OTP event ... etc., are represented by the OP interrupt status register. The interrupt status registers are ‘read-only’ and ‘read-cleared’ type:

- General Interrupt status register – GINSR (General Interrupt Status Register, Reg 0x1D), page 100.
- OP Interrupt status registers – OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08), OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10) and OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18).

The index of the particular interrupt is the same among interrupt enable, mask, and status registers. If an enabled interrupt event occurred, the INTB pin will be driven low accordingly (with mask disabled). This interrupt will be self-cleared (INTB pin de-asserted) by reading the corresponding interrupt status registers through the MDC/MDIO interface. Figure 53 summarizes the behavior stated above.

If more than one interrupt occurs simultaneously, the INTB pin will remain low until all of the interrupt status registers are read by the upper layer.

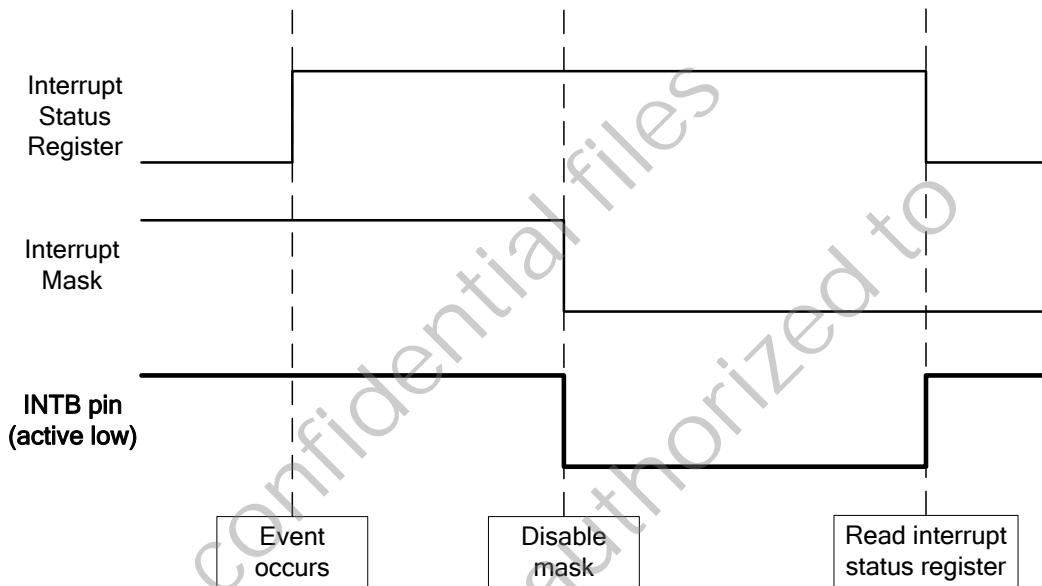


Figure 53. Interrupt and Mask Behavior

Some sub-flags of the General Interrupt are presented in order to provide detailed event information; e.g., PHY fatal errors, PTP events, and general purpose events summarized by one of the General Interrupts.

For example, when the upper layer is informed by the INTB pin and wishes to access the General Interrupt status register for these types of events, it is required to check the related sub-flag registers accordingly. The relation of the General Interrupts and its sub-flags are listed in Table 14.

Table 14. General Interrupts and Sub-Flags

Index	General Interrupts	Sub-flags of General Interrupts
	Enable Register: GINER (General Interrupt Enable Register, Page 0xA42, Reg 0x12), page 97 Status Register: GINSR (General Interrupt Status Register, Reg 0x1D), page 100 Mask Register: GINMR (General Interrupt Mask Register, Page 0xA42, Reg 0x14), page 98	
15:12	Reserved	-
11	PHY fatal errors occurred: Indicates PHY internal SRAM or clock fail.	-
10	Jabber detected <i>Note that the Jabber packet will be detected if the transmission time of the packet is longer than 1.08ms, namely around 13.5kbytes packet size.</i>	-
9	Reserved	-
8	PTP events occur	Sub-flags Enable Register: PTP_INER (PTP Interrupt Enable Register, Address 0xE402), page 117 Sub-flags Register: PTP_INSR (PTP Interrupt Status Register, Address 0xE404), page 117
7:5	Reserved	-
4	Link status change	-
3	Reserved	-
2	General purpose events occur	Sub-flags Register: GPSFR (General Purpose Sub-Flag Register, Page 0xA47, Reg 0x15), page 101
1	Reserved	-
0	PHY status change	-

8.9. Hardware Configuration

The PHY address, Master/Slave setting, MII interface, and state change setting can be set by the CONFIG pins. The corresponding configuration will be strapped and set as the default value whenever the following three events occur: power-on, wake up, the PHYRSTB pin is asserted to low. The respective value mapping of CONFIG with the configurable vector is listed in Table 15.

To set the CONFIG pins, an external pull-high or pull-low via resistor is required. If there is no external pull-high or pull-down resistor on the CONFIG pins, the setting depends on the internal pull-high or pull-down resistor; for the internal register settings refer to section 7. If the user wants to use the external pull up/down I/O signal to do the hardware-strapping configuration, for the timing for the external I/O, refer to Figure 67, page 142.

Table 15. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
RXD0	PHYAD[0]
RXD1	PHYAD[1]
RXER	MS_SEL
RXD2	MII_SEL[1]
RXD3	MII_SEL[0]
RXDV	ST_CHG

Table 16. Configuration Register Definitions

Configuration	Description																	
PHYAD[1:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL9000BF/BN/BR/BS supports PHY addresses from 01 to 11. PHY Address [1:0] Configuration. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>PHYAD1 (RXD1)</th> <th>PHYAD0 (RXD0)</th> <th>PHY Address</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>0</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>1</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>2</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>3</td> </tr> </tbody> </table> <p><i>Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xA43, Reg 0x18, bit[13]=0 (see section 0, page 99).</i></p> <p><i>Note 2: If the user wants to use PHYAD is 0 in a multiple PHY case, the broadcast should be disabled for all PHYs.</i></p> <p><i>Note 3: The RTL9000BF/BN/BR/BS with PHYAD[1:0]=00 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xA43, Reg 0x18, bit[6]=1 (see section 0, page 99).</i></p>			PHYAD1 (RXD1)	PHYAD0 (RXD0)	PHY Address	LOW	LOW	0	LOW	HIGH	1	HIGH	LOW	2	HIGH	HIGH	3
PHYAD1 (RXD1)	PHYAD0 (RXD0)	PHY Address																
LOW	LOW	0																
LOW	HIGH	1																
HIGH	LOW	2																
HIGH	HIGH	3																
MS_SEL	PHY Master / Slave Mode Configuration. HIGH: Master (via pull up resistor to DVDD power) LOW: Slave (via pull down resistor to GND) The role setting can be change by the register at section 9.2.5.																	

Configuration	Description		
MII_SEL[1:0]	MII/RMII/RGMII Mode Configuration.		
	MII_SEL1 (RXD2)	MII_SEL0 (RXD3)	MII Mode
	LOW	LOW	MII
	LOW	HIGH	RMII Output mode
	HIGH	LOW	RGMII
	HIGH	HIGH	RMII Input mode
For the pin assignments of RMII Output/Input mode, refer to section 7.4.			
ST_CHG	Operating Modes (OP) State Change Condition Configuration The application for the ST_CHG can refer to section 8.4, Standby mode. HIGH: Auto mode, the PHY goes to Normal Mode automatically, when power-on/wake up/assert PHYRSTB to low (via a pull up resistor to DVDD power), LOW: Manual mode, the PHY goes to Normal Mode manually, when power-on/wake up/assert PHYRSTB to low (Wait for OP go to sleep/normal command, refer to section 8.4.2, page 26.) (via a pull down resistor to GND).		

8.10. MAC/PHY Interface

The RTL9000BF/BN/BR supports automotive standards and is suitable for most off-the-shelf MACs with an MII/RMII/RGMII interface. Note that default driving strength of the MII/RMII/RGMII interface is set for the trace 15cm plus 5pf loading.

8.10.1. MII

If MII (Media Independent Interface) mode is selected, TXC and RXC sources are 25MHz. TXC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions.

8.10.2. RMII

The purpose of the RMII (Reduced Media Independent Interface) interface is to provide a low cost alternative to the MII. Architecturally, the RMII provides for an additional reconciliation layer on either side of the MII but can be implemented in the absence of an MII. The RMII sources from the reference clock REF_CLK, which can be provided either by the PHY or the MAC. TXD[1:0] and RXD[1:0] signals are used for data transitions.

8.10.3. RGMII

The RGMII interface in 100BASE-T1, TXC, and RXC sources are 25MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on the rising and falling edge of the clock.

8.10.4. MII/RMII/RGMII Driving Strengths

RTL9000BF/BN/BR supports ‘Typical’ and ‘Weak’ driving strengths for MII/RMII/RGMII, which can be adjusted by parameter setting with reference to the errata list. The default driving strength is ‘Typical’.

Note that when setting IO power (I/O Power Select Register, section 9.2.22), the driving strength will be set to ‘Typical’ setting automatically.

8.10.5. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a standard interface that is used to carry frame data and link status information between a PHY and an Ethernet MAC. The SGMII uses a differential pair for data and clock signals to provide signal integrity while minimizing system noise. The data signals operate at 1.25G/baud and the clocks operate as a 625MHz Double Data Rate (DDR) interface. The 1.25GHz SERDES I/Os are current logic (CML). If the user wants to connect the SERDES CML to LVDS, Figure 54 shows an example of a SERDES CML to LVDS connection. Note that if the LVDS receiver includes both the 100 ohm termination and internal biasing, there is no need for external termination and biasing. The detailed termination circuit, biasing, and voltage of VBB depends on the design of the LVDS Receiver.

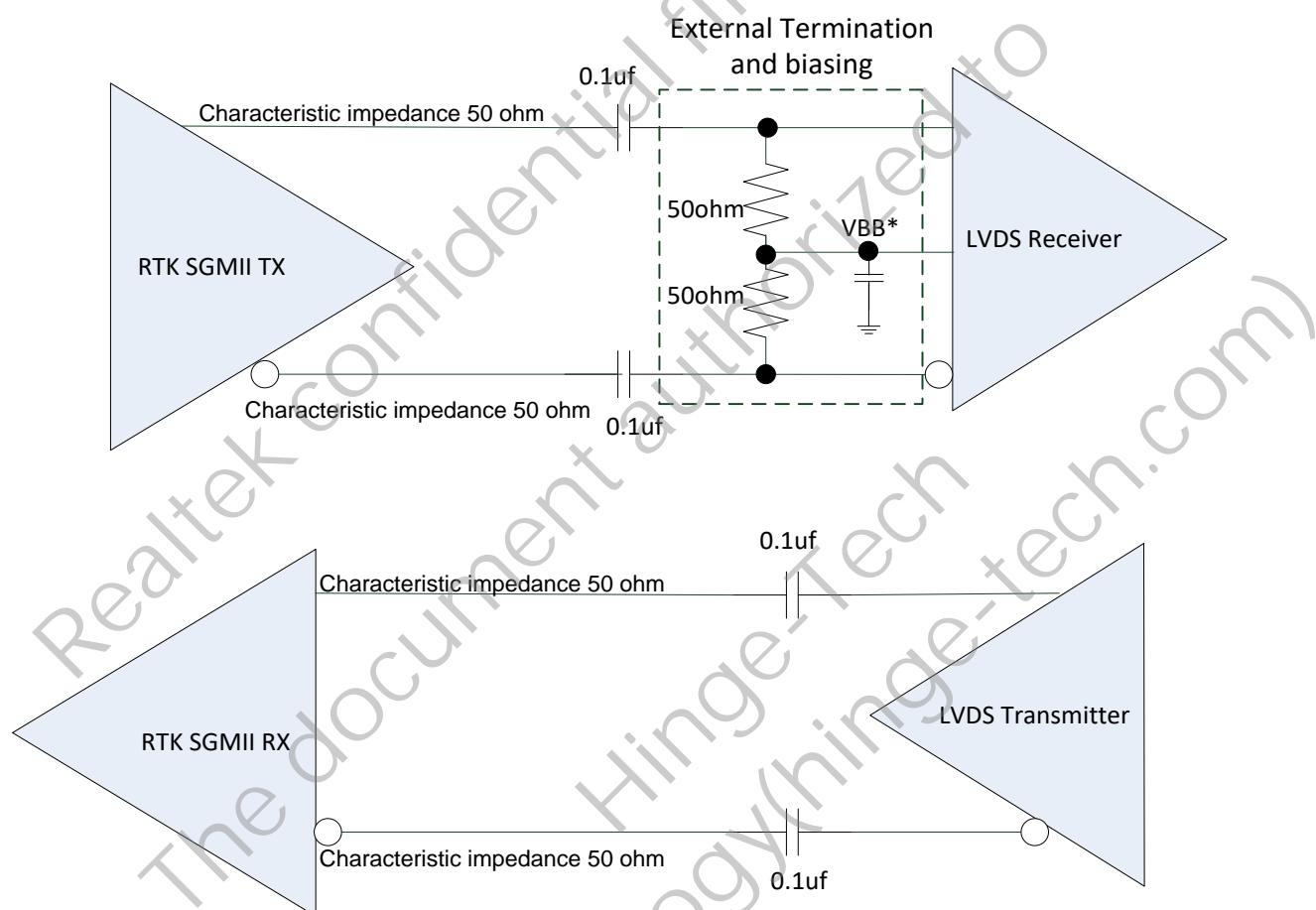


Figure 54. SERDES CML to LVDS Connection Diagram

The RTL9000BF supports both xMII (MII/RMII/RGMII) and SGMII, please refer to section 9.2.55 and the following setting for switching between xMII (MII/RMII/RGMII) and SGMII.

- Switch to SGMII from xMII (MII/RMII/RGMII):

Step 1: Write page 0xA47, reg 23, bit[3:0] = 0x1.
 Step 2: Write page 0xD41, reg 18, bit 15 = 1.
 Step 3: Write page 0xD41, reg 18, bit 7 = 1.
 Step 4: Write page 0xD41, reg 19, bit 15 = 1.
 Step 5: Write page 0xD41, reg 19, bit 7 = 1.
 Step 6: Write page 0xD41, reg 20, bit 15 = 1.
 Step 7: Write page 0xD41, reg 21, bit 15 = 1.
 Step 8: Write page 0xD41, reg 21, bit 7 = 1.

- Switching to xMII (MII/RMII/RGMII) from SGMII:

Step 1: Write page 0xA47, reg 23, bit[3:0] = 0x0.
 Step 2: Write page 0xD41, reg 18, bit 15 = 0.
 Step 3: Write page 0xD41, reg 18, bit 7 = 0.
 Step 4: Write page 0xD41, reg 19, bit 15 = 0.
 Step 5: Write page 0xD41, reg 19, bit 7 = 0.
 Step 6: Write page 0xD41, reg 20, bit 15 = 0.
 Step 7: Write page 0xD41, reg 21, bit 15 = 0.
 Step 8: Write page 0xD41, reg 21, bit 7 = 0.

Note:

1. Step 2~7 to control xMII pad on/off for power saving
2. When switching to xMII, the MII/RMII/RGMII setting depends on the hardware strapping configuration

8.10.6. RGMII to SGMII bridge mode

RTL9000BF supports the following bridge mode, please refer to section 9.2.55 for configuration.

RGMII to SGMII (PHY side@100Mbps):

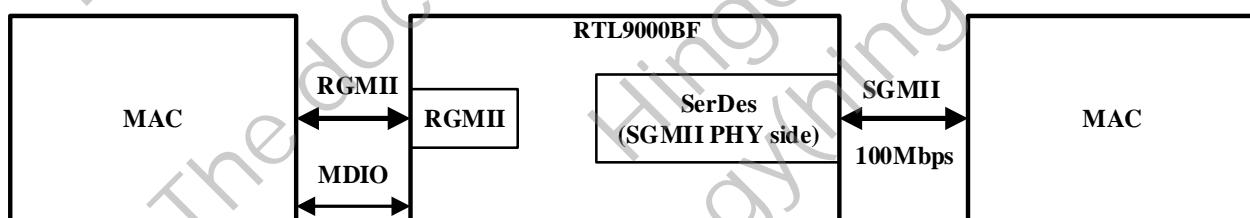


Figure 55. RGMII to SGMII Bridge Mode: PHY side, 100Mbps.

RGMII to SGMII (PHY side@1000Mbps):

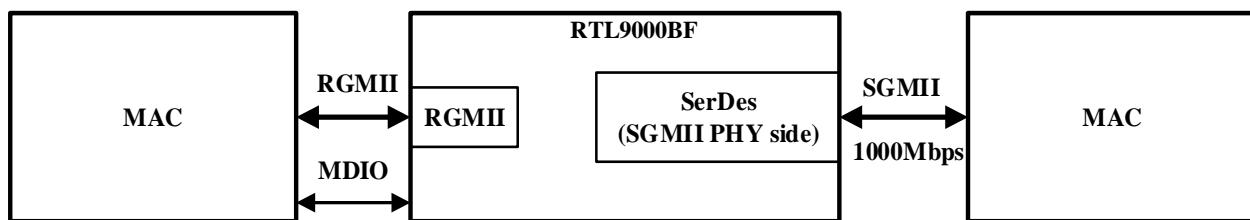


Figure 56. RGMII to SGMII Bridge Mode: PHY side, 1000Mbps

RGMII to SGMII (MAC side):

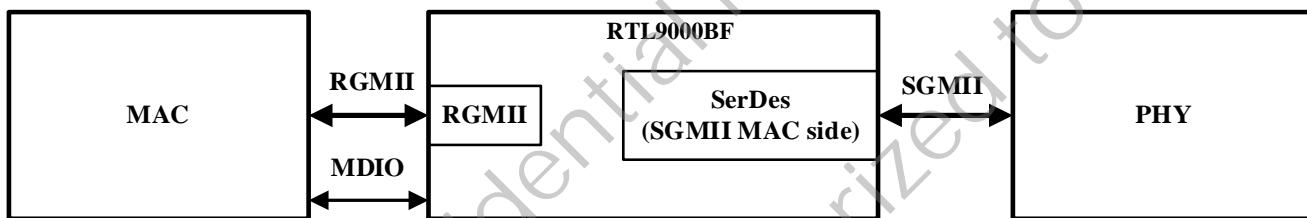


Figure 57. RGMII to SGMII Bridge Mode: MAC side

8.10.7. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a pull-up resistor to maintain the MDIO high during idle and turnaround.

The RTL9000BF/BN/BR/BS/BSS can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the management registers, see section 9, page 92.

Table 17. Management Frame Format

-	Management Frame Fields								
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE	
Read	1...1	01	10	AAAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z	
Write	1...1	01	01	AAAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z	

Table 18. Management Frame Description

Name	Description
Preamble	32 Contiguous Logical 1's sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

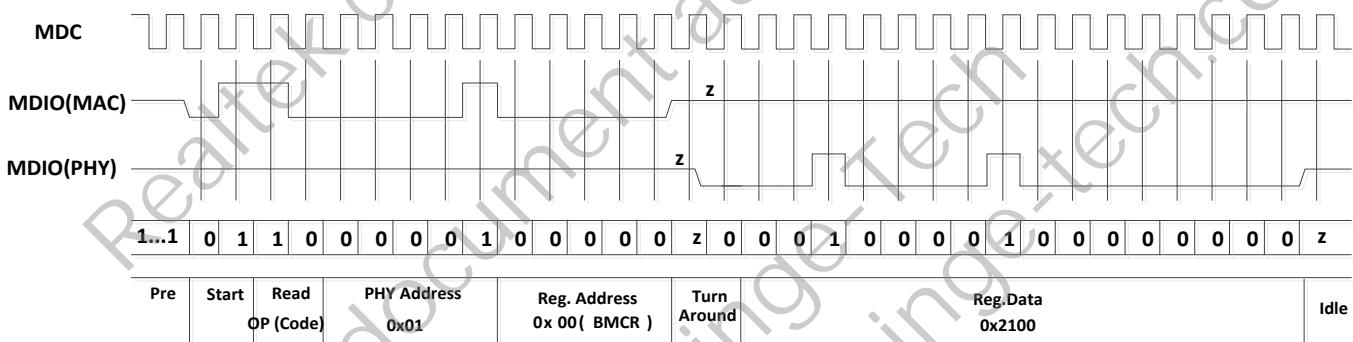


Figure 58. MDC/MDIO Read Timing

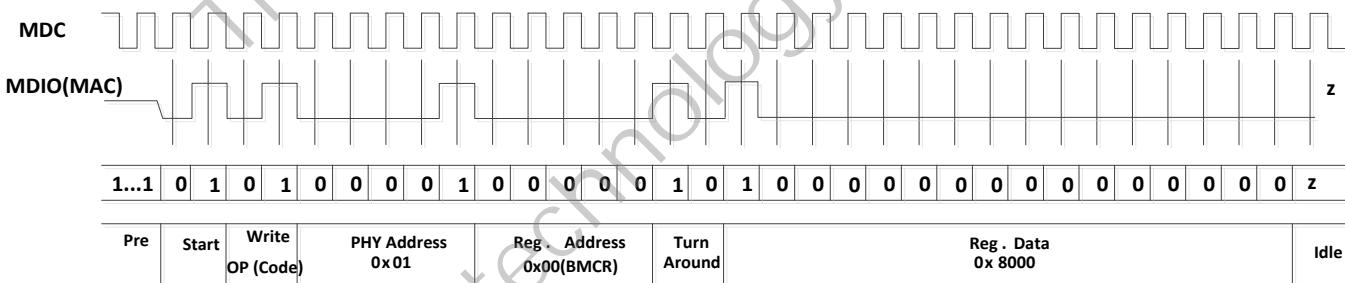


Figure 59. MDC/MDIO Write Timing

8.10.8. Register Access

The RTL9000BF/BN/BR/BS/BSS provides two methods of accessing the registers. One is Normal Register Access, which is for most IEEE standard registers; the other is Special Register Access, which is especially for the OP register and others. Table 19 should be followed while accessing the registers by the corresponding accessing method.

Table 19. Method of Accessing Registers

Register Table	Method of Accessing Registers
General Register Table Section 9.2.1. - 9.2.28	8.10.8.1 Normal Register Access
General Register Table Section 9.2.29 - 9.2.54	8.10.8.2 Special Register Access
9.3 PTP Register Tables	

8.10.8.1 Normal Register Access

In Normal Register Access, the Page should be set to the target register's page first, and then read/write the target register with its register address (Reg 0xAB). The MDIO commands and an example are shown below. Note that the registers in Table 20 can be accessed no matter what the Page is; i.e., these registers can be accessed no matter what value Register 31 is.

Table 20. Registers can be Accessed on any Page

The registers can be accessed on any Page
General Register Table Section 9.2.1. - 9.2.8
General Register Table Section 9.2.20

Take the register at Page 0xWXYZ (in Hex), Reg 0xAB as an example.

1. Write Register 31 Data = 0xWXYZ (switch to Page 0xWXYZ)
2. Read/Write Register 0xAB (target register's Reg 0xAB) Data directly

**Note that if the registers are on the same pages, no need to re-write the Page 0xWXYZ.*

8.10.8.2 Special Register Access

In Special Register Access, by reading/writing register 27 and register 28 to read/write the target register with its address (Address 0xWXYZ). Page switching is not required. The MDIO commands and an example are shown below.

Take the register with Address 0xWXYZ as an example.

1. Write Register 27 Data = 0xWXYZ (Register with Address 0xWXYZ)
2. Read/Write the target Register Data through Register 28

**Note: Writing the 'register address' should always be done (Step 1) each time when accessing registers, even for access to the same register.*

8.10.9. Internal Packet Counter

The RTL9000BF/BN/BS/BS/BSS support an internal packet counter and internal error packet counter that can choose the monitor path of the packet counter in sections 9.2.32, 9.2.34, and 9.2.35. When the monitor path is selected as the PHY'RX path, namely the normal path, the internal packet counter can record the number of received packets.

If the monitor path is selected as the MAX's TX path, the internal packet counter can record the number of packets from MAC to PHY. Note that the bit [1] at the register at address 0xC800 should be set to 1 to enable the internal packet counter. The internal error packet counter increases when an invalid packet is received by the PHY (refer to section 9.2.36). Note that as defined in the IEEE standard, the bit error rate should be less than 10^{-10} . If more than 7 errors are observed in 3×10^{10} bits (about 2,470,000 1,518-byte packets), it can be concluded that the error rate is greater than 10^{-10} with less than a 5% chance of error. I.e., if less than 7 errors are observed in 3×10^{10} bits, the error number is reasonable.

8.11. Polarity Correction

The RTL9000BF/BN/BR/BS/BSS automatically corrects polarity errors on the receive pairs. Received polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock. Bit [8] at section 9.2.27 will show if the polarity is swapped or not. The polarity correction can be disabled by writing the bit [3] and bit [1] as 1 at section 9.2.23.

8.12. Spread Spectrum Clock (SSC)

The clock could be a very likely source of EMI noise. Spread Spectrum Clock (SSC) spreads the signal across a wider bandwidth, reducing the peak radiated energy at any one frequency, and lowering unwanted EMI noise. For the RTL9000BF/BN/BR, Spread Spectrum Clock (SSC) is supported in three clock domains: system clock, RXC of MII/RGMII, and REF_CLK (output mode) of RMII. Note that the SSC function is enabled in the RTL9000BF/BN/BR by default.

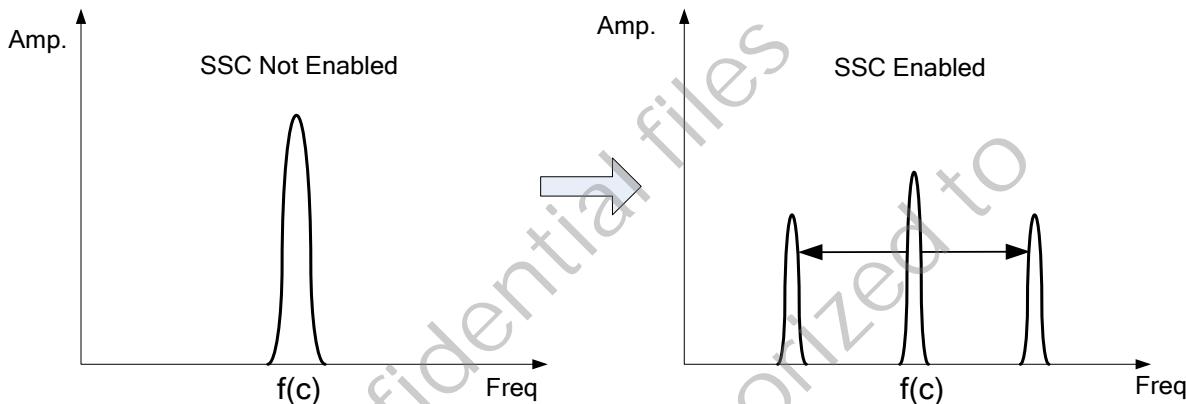


Figure 60. Spread Spectrum Clock

If Jumbo packets should be supported with SSC enabled in RMII/RGMII mode, the strength should be adjusted by setting Address 0xD096, bit [14:13] to 1 and Address 0xD0B6, bit [14:13] to 1, refer to section SPCR1 (SSC Phase Control Register 1, Address 0xD096), page 108, and SPCR2 (SSC Strength Control Register 2, Address 0xD0B6), page 109.

8.13. Realtek Cable Test Diagnostics (RTCT)

8.13.1. RTCT Introduction

The RTL9000BF/BN/BR/BS/BSS has an integrated DSP engine to detect the cable status, which is described as ‘Realtek Cable Test Diagnostics (RTCT)’. The RTL9000BF/BN/BR/BS/BSS supports RTCT no matter what the Master/Slave role setting is. When the PHY enters the RTCT process, it transmits the cable detecting sequence rather than the normal signal; hence the link cannot be established during this mode and PHY will go back to normal mode by itself after the process is finished. There are three cable status’s that can be detected and shown in registers; namely the Normal, Open, and Short. If the cable is not diagnosed as Normal status, the position of the abnormal point can be indicated through the register. The following diagram shows how RTCT works in the RTL9000BF/BN/BR/BS/BSS.

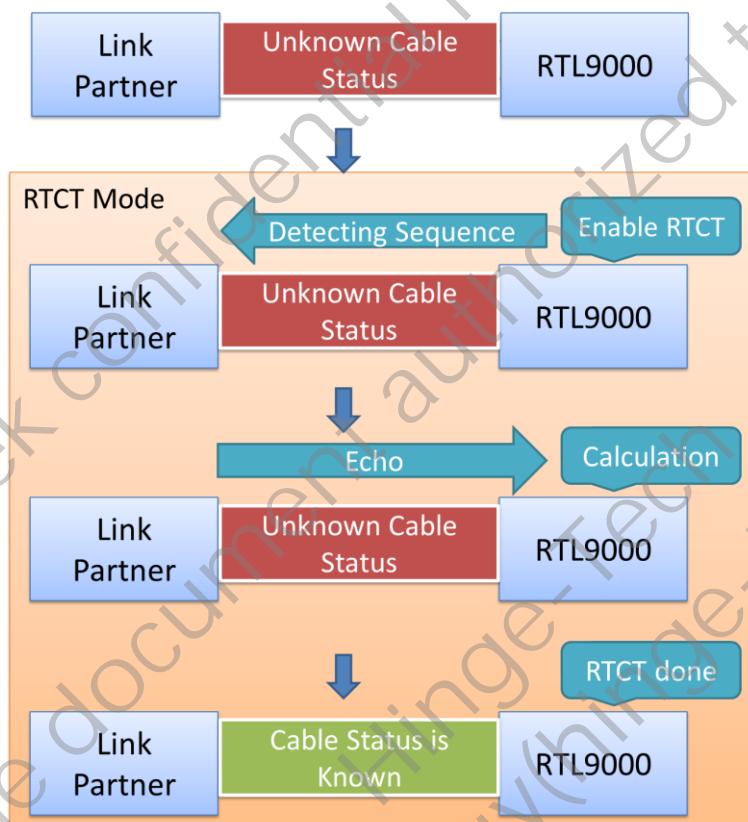


Figure 61. RTCT Introduction

8.13.2. Use Cases

The following figure shows the normal use cases of RTCT. Note that the RTL9000BF/BN/BR/BS/BSS supports the RTCT function whether the link partner is silent or not.

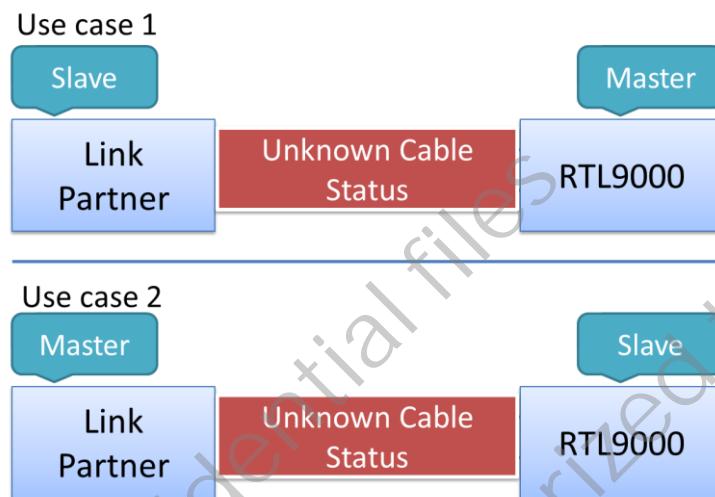


Figure 62. RTCT Use Cases

8.13.3. RTCT Configuration

Follow the steps below to start the RTL9000BF/BN/BR/BS/BSS RTCT. For related registers, refer to section 9.2.10 RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11), page 97, section 9.2.29 RTCTS (RTCT Status Register, Address 0x8022), page 104, and section 9.2.30 RTCTL (RTCT Length Register, Address 0x8023), page 104.

Figure 63 shows the setup flow of RTCT Configuration. Detailed descriptions are shown in the following sub sections, along with the corresponding steps.

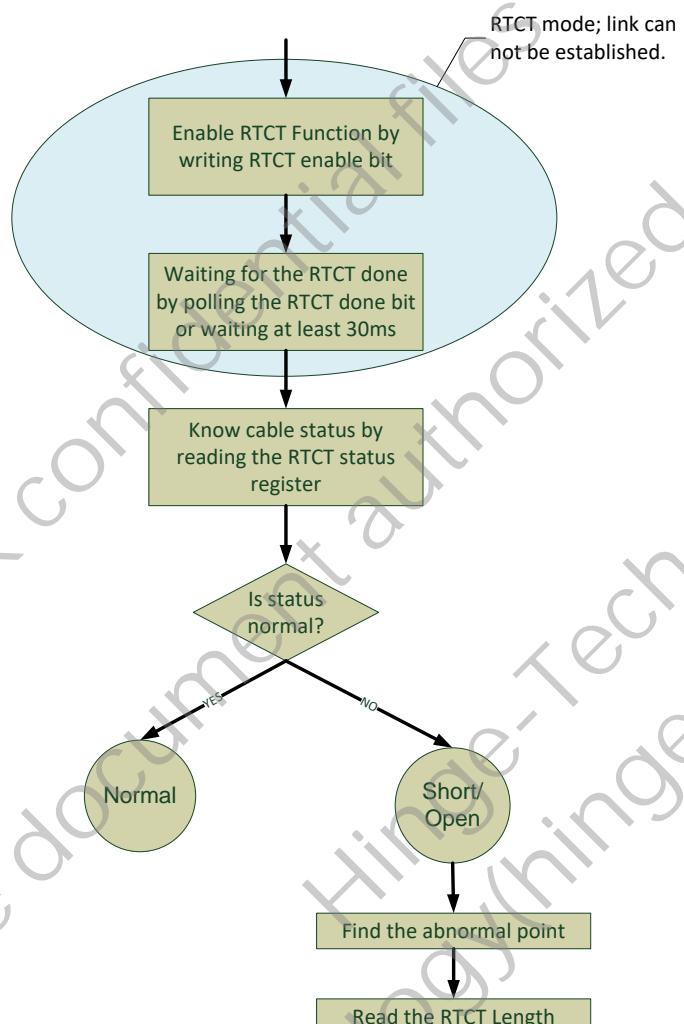


Figure 63. RTCT Steps Flow

8.13.3.1 Enable the RTCT Function

Enable the RTCT Function by setting the register at 9.2.10 RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11), page 97, bit [0] rtct_enable to 1. The PHY will enter RTCT mode at this time. Note that once RTCT is enabled, a normal link cannot be established in this mode.

8.13.3.2 RTCT Done Within 5 ms

RTCT will poll the 9.2.10 RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11), page 97 bit [15] rtct_done until it is 1. When the value ‘1’ is returned, it means the RTCT test is finished. If the value ‘0’ is returned, the test is still running. Note that the test will be done in 5ms.

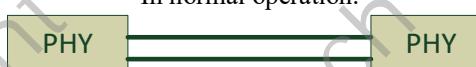
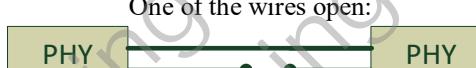
8.13.3.3 Establish Link after RTCT Done

Write Address 0xC002 bit [15] as 0 after RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11) bit [15] rtct_done is 1 to make sure RTCT is finished and the RTL9000BF/BN/BR/BS/BSS is ready to establish a link.

8.13.3.4 Result Shown by the Register

Read the register at 9.2.29 RTCTSR (RTCT Status Register, Address 0x8022), page 104 for the test results. The status can be mapped using the table below to indicate whether cable status is normal operation, cable open, or cable short. If the result is not normal operation, the next step can indicate the abnormal point.

Table 21. RTCT Cable Status Indication

Cable Status	Register Value (in Hex)	Description
Normal	0x60XX	<p>Cable is indicated to be normal in the following situation.</p> <p>In normal operation:</p> 
Open	0x48XX	<p>Cable is indicated to be open in the following situations.</p> <p>Both of the wires open:</p>  <p>One of the wires open:</p> 
Short	0x50XX	<p>Cable is indicated to be short in the following situations.</p> <p>Wires shorted:</p>  <p>Both of the wires short to GND or Supply:</p> 

*Note: Cable status can also be indicated by the LED pin. See section 8.15, page 83

8.13.3.5 Locating the Abnormal Point

Read the register at 9.2.29 RTCTSR (RTCT Status Register, Address 0x8022), page 104 to determine the defect point of the cable.

Read the register at section 9.2.30 RTCTLR (RTCT Length Register, Address 0x8023), page 104. The value can be read by transforming the hexadecimal value into a decimal value then dividing by 80. The result indicates the distance from the chip side to the defect point of the cable in meters with resolution +/- 1m.

8.14. Signal Quality Indexes (SQI)

8.14.1. SQI Introduction

The Signal Quality Index is an index for understanding the communication quality of the system. It is divided into two parts, one is the Dynamic Channel Quality (DCQ) and the other is the Link Quality (LQ). Note that Mean Square Errors (MSE), Signal Quality Index (SQI) and peak Mean Square Errors (pMSE) are included in DCQ.

Link Training Time (LTT), Local Receiver Time (LRT), Remote Receiver Time (RRT) and link failures and losses are included in link quality. The information of the signal quality index can be obtained by reading the corresponding register address when the link is selected. Therefore, the SQI latch register is available to read the status of link ok, remote ok, local ok, scramble ok, pcs state, equalizer errors, maximum error, Signal To Noise Ratio (SNR), and ADC peak values simultaneously without any timing delay.

The RTL9000BF/BN/BR/BS/BSS provides two signal quality indexes (SQI) to indicate real-time MDI signal quality information. These indexes are listed as follows:

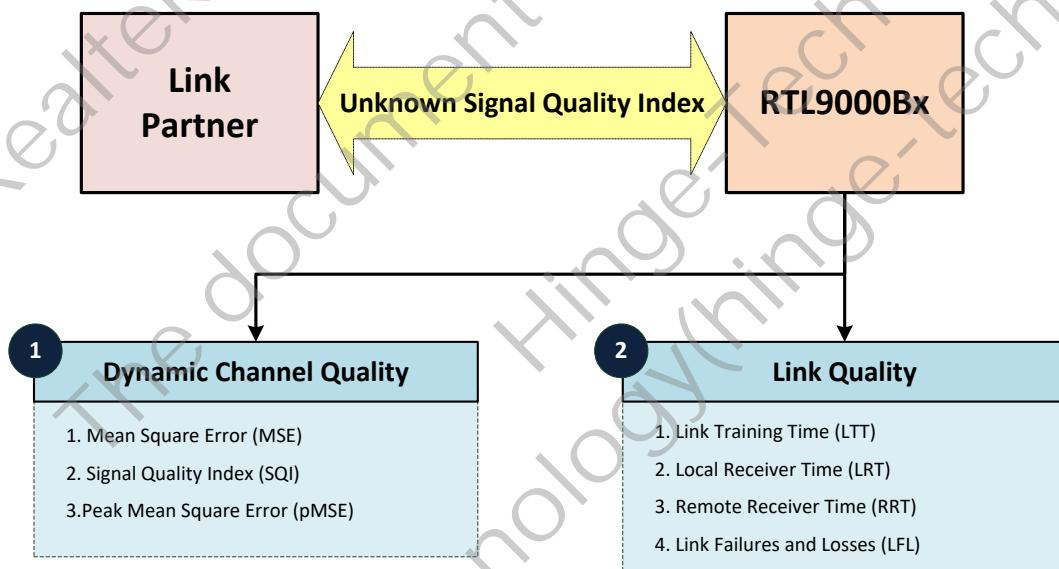


Figure 64. SQI Introduction

8.14.2. SQI Use Case

The following figure shows the usual use case of SQI.

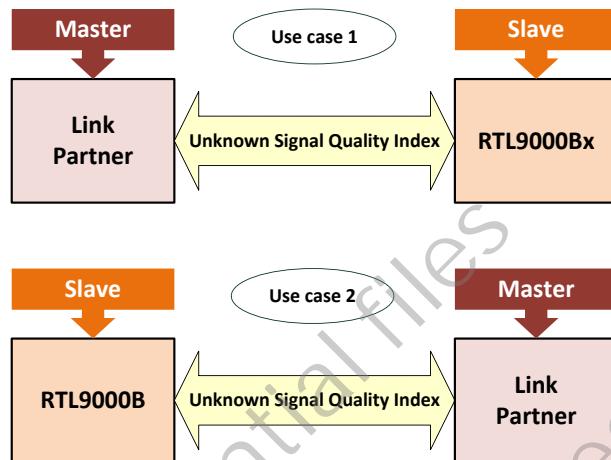


Figure 65. SQI Use Cases

8.14.3. Index

8.14.3.1 Dynamic Channel Quality

Dynamic channel quality includes MSE values, SQI values and peak MSE values.

8.14.3.2 Mean Square Error (MSE)

Mean Square Error (MSE) of the slicer measures the average of the squares of the errors. The higher the signal-to-noise ratio (SNR), the lower the MSE. MSE is stored from range 0 to 511 in section 9.2.44. MSE worst case can also be obtained since the last read. MSE WC value also ranges from 0 to 511 (see section 0). Both MSE and MSE_WC are defined as valid only under link status.

8.14.3.3 Peak MSE Value

Peak MSE value records the maximum value of MSE during transient time, which is typically under micro second range. Therefore, the transient disturbances can be observed by Peak MSE values. Peak MSE value stored ranges from 0 to 63 (see section 0). Peak MSE worst case value stored ranges from 0 to 63 (see section 0).

8.14.3.4 Signal Quality Index (SQI)

The Signal Quality Index is determined by Signal to Noise Ratio (SNR) and the range is from 0 to 7 levels. A higher SNR indicates that the performance of the communication system is better. When the SQI value is less than zero, it implies that the bit error rate may be higher than 1e-10. The following table is the mapping of SQI index and SNR value. The SQI will be zero when the link is not established. For the SQI value and the worst SQI value registers, see section 9.2.47.

8.14.4. Link Quality(LQ) – Start-Up Time and Link Losses

8.14.4.1 Link Training Time (LTT)

LTT is the time required to establish a link. The timer for the time measurement starts when entering SLAVE_SILENT. The timer stops when entering loc_phy_ready and rem_phy_ready. Refer to IEEE802.3bw figure 96-18, which shows the exact start and stop timing on the PHY control state diagram. The LTT value is the link training time of the last link training, refer to 0. It stores the value from a range of 0 ms to 250 ms. Timing over 250 ms will be defined as measurement not possible.

8.14.4.2 Local Receiver Time (LRT)

LRT is the time required until the local receiver is locked. The timer for the time measurement starts when entering SLAVE_SILENT. The timer stops when entering loc_phy_ready. For the LRT value, refer to section 0. It stores the value from a range of 0 ms to 250 ms. Timing over 250 ms will be defined as measurement not possible.

8.14.4.3 Remote Receiver Time (RRT)

RRT is the time required until the remote receiver is sending data and is locked. The timer for the time measurement starts when entering SLAVE_SILENT. The timer stops when entering rem_phy_ready. For the RRT value, refer to section 0. It stores the value from a range of 0 ms to 250 ms. Timing over 250 ms will be defined as measurement not possible.

8.14.4.4 Link Failures and Losses (LFL)

LFL stores the number of failures that occurred since the last power cycle. For the value of link failures that did not cause a link loss, and the value of link losses, refer to section 0.

8.15. LED

The RTL9000BF/BN/BS provides an LED pin as an indication for debugging use. Its functions are listed in Table 22.

Table 22. LED

	Link Status	Cable Diagnostics (RTCT) Results
LED Behavior	On: Link up Off: Link down Blinking: Traffic transmitting	On: Cable Open Off: Cable Normal Off for 1 sec followed by On for 3s: Cable Short
Register Settings	Address 0xD040, bit[0] = 1 (led_link) Address 0xD040, bit[1] = 1 (led_act) Address 0xD040, bit[13] = 0 (led_rtct)	Address 0xD040, bit[13] = 1 (led_rtct)

Note: The LED behavior above will be presented in the 'RTCT Result' interval in Figure 66.

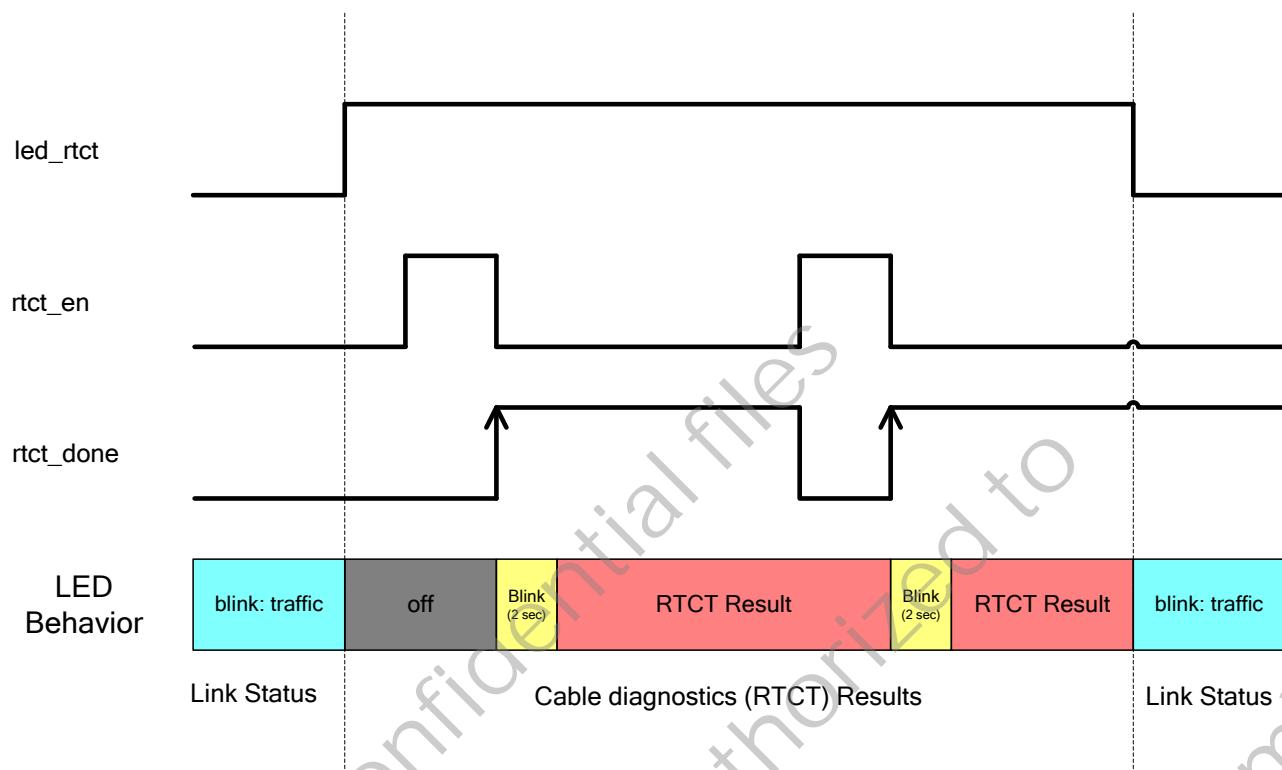


Figure 66. LED Behavior

Note 1: For the definitions of 'rtct_en' and 'rtct_done', refer to section 8.13, page 77, and section 9.2.10 RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11), page 97.

Note 2: For detailed LED setting, refer to section 9.2.41, page 108.

8.16. UNH IOL Test

The test modes of IEEE 802.3bw^[1] are supported by the RTL9000BF/BN/BR/BS/BSS. The test modes can be selected independently and the test signal will present at MDI pins (MDIP and MDIN) in the Normal mode while the link is disabled. Enable the UNH IOL Test Modes by setting the Page 0, Reg 9, bit [15:13], see Table 30, page 95. For transmitter test result details, refer to section 11.5, page 149.

The PTP_GPIO pin can be used as a clock output TX_TCLK in test modes that need a reference clock via the following steps.

1. Write Address 0xd41E, bit [15:13]=0
2. Write Address 0xd42A, bit [0]=0
3. Write Address 0xd42C, bit [0]=1 // outputs the clock to the PTP_GPIO pin

8.16.1. Test Mode 1

Test mode 1 is a measurement of Transmit droop. When test mode 1 is enabled, the PHY shall transmit greater than 500ns '+1' symbols followed by greater than 500 ns '-1' symbols. This sequence is repeated continually.

8.16.2. Test Mode 2

Test mode 2 is a measurement of Transmit jitter in MASTER mode. When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+1, -1} repeatedly. The transmitter shall time the transmitted symbols from a $66.666 \text{ MHz} \pm 100 \text{ ppm}$ clock in the MASTER timing mode.

8.16.3. Test Mode 4

Test mode 4 is a measurement of Transmit distortion. When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the scrambler generator polynomial, bit generation, and level mappings as equation 96-1 in [1]. The transmitter shall time the transmitted symbols from a $66.666 \text{ MHz} \pm 100 \text{ ppm}$ clock in the MASTER timing mode.

8.16.4. Test Mode 5

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask. When test mode 5 is enabled, the PHY shall transmit a pseudo-random sequence of PAM3 symbols.

8.16.5. SLAVE Jitter

When the PHY is configured as SLAVE in normal mode, the jitter on the received signal reflects jitter on the TX_TCLK, which can be outputted to the PTP_GPIO pin. The SSC should be turned off while measuring SLAVE Jitter. When Receiving a valid signal from a compliant PHY operating as the MASTER with test port connected to the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an un-jittered reference shall be less than 0.01 unit interval after the receiver is properly receiving the data.

Write Address 0xD012, bit [2:0] =0 // Turns off SSC (refer to section 9.2.37).

After finishing the test, the RTL9000BF/BN/BR/BS/BSS should be reset via PHYRSTB.

[1] IEEE Standard for Ethernet Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1), 26 October, 2015.

8.16.6. Testing Condition and Set Up

Pre-Conditions and Requirements

1. DUT

- (a) A test fixture is needed if there is no SMA or MMCX connector on the DUT board. The test fixture must be verified to meet the requirements of a test fixture in the OPEN Alliance standard for 100BASE-T1 (usually provided by the oscilloscope vendor). The length between the DUT and test fixture should be as short as possible.
- (b) Registers can be configured as MASTER or SLAVE, and to various Test Modes.

2. Link Partner

3. SMA Cables

4. Oscilloscope

- (a) Bandwidth $f_s > 2\text{GHz}$
- (b) Compliance test software installed
- (c) Should be correlated to the UNH-IOL's measurement results

5. Network Analyzer

- (a) Measuring MDI return loss and mode conversion loss
- (b) The noise flow after the calibration of the Network analyzer, include the test fixture, must not exceed the limit line defined in the OPEN Alliance TC8 test suite

6. (Optional) Balun

- This depends on different test methods of the oscilloscope, please consult with the provider

7. (Optional) Function Generators

- This depends on the different test methods of the oscilloscope, used for Test Mode 4 synchronization between the DUT and the oscilloscope, and also for the disturbing signal

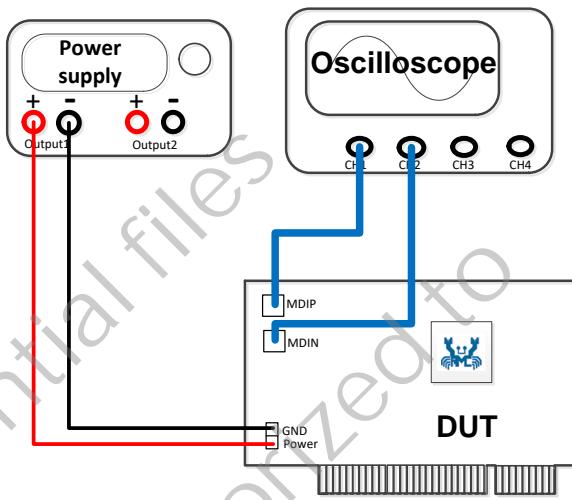
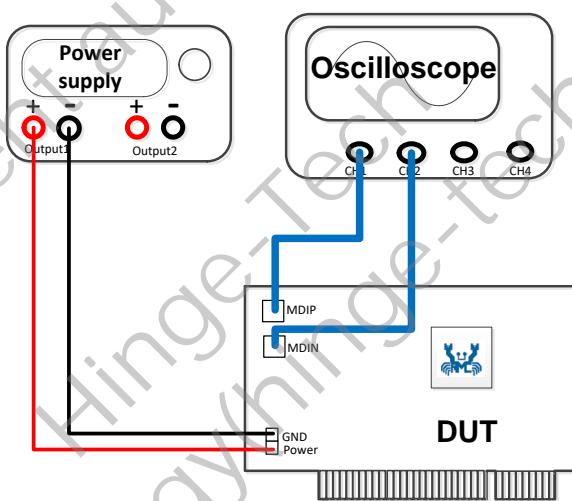
8. (Optional) Spectrum analyzer

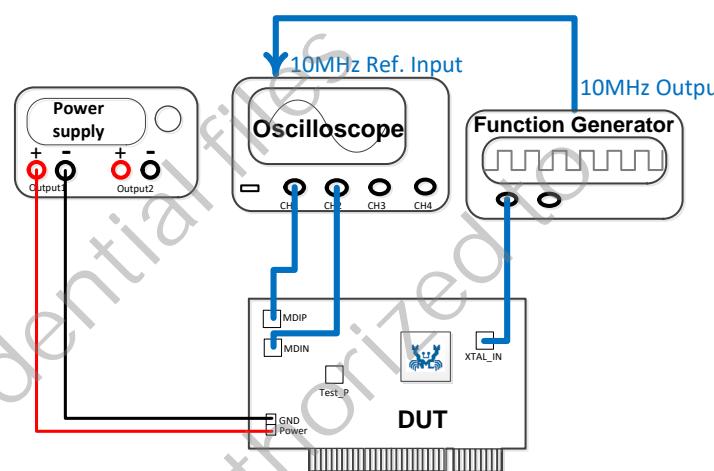
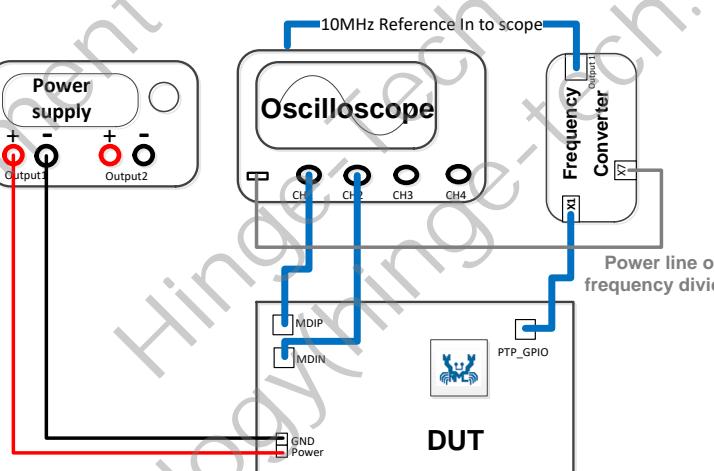
- (a) Bandwidth $> 2\text{GHz}$
- (b) Alternative way to measure the Test Mode 5 PSD

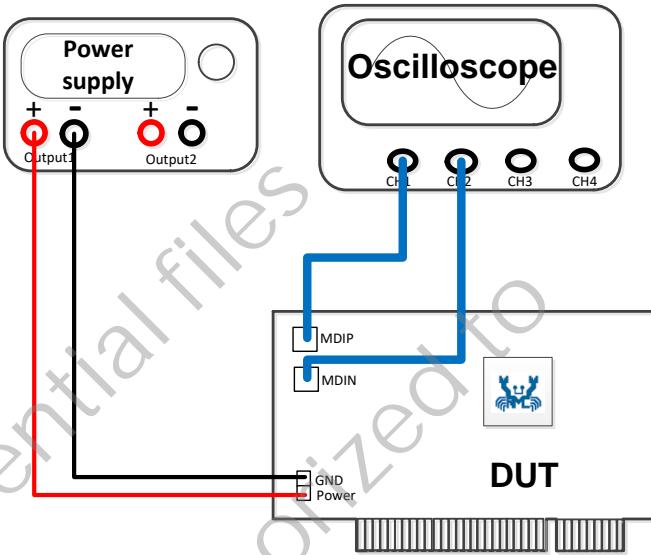
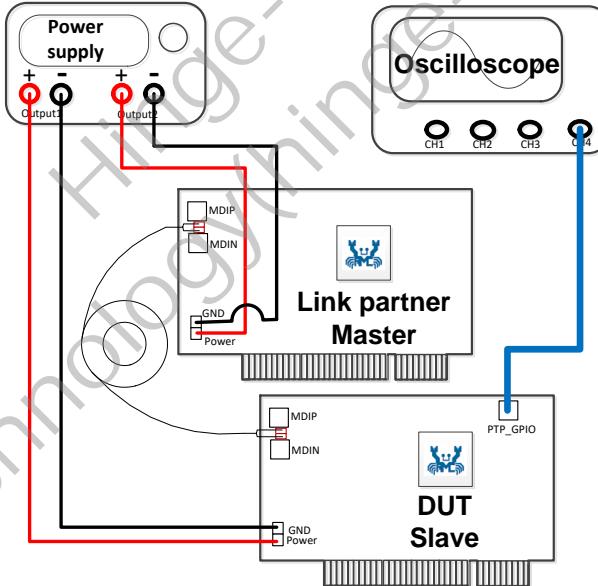
9. Reference

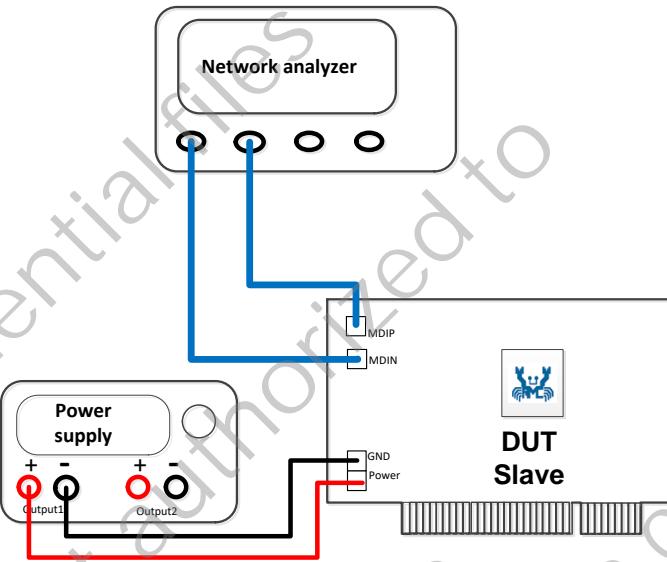
- (a) IEEE Std. 802.3bw, section 96.5
- (b) Open Alliance 100BASE-T1 PMA Test Suite v1.2

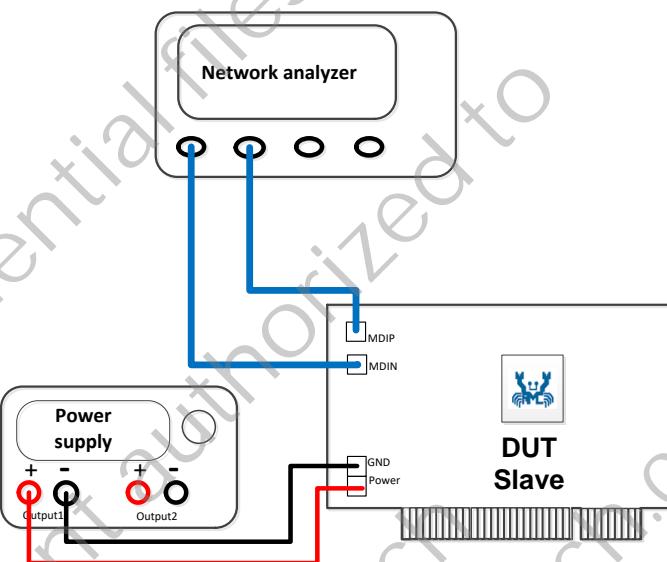
Table 23. UNI-IOL Testing Condition and Set Up

Test Mode #	Description	Setup
1	Transmit droop test mode	<p>1. Connect the MDIP pin & MDIN to the oscilloscope via SMA cables. 2. Configure DUT as Test mode 1; run the Compliance test software on the oscilloscope.</p> 
2	Transmit jitter test in MASTER mode	<p>1. Connect the MDIP pin & MDIN to the oscilloscope via SMA cables. 2. Configure DUT as Test mode 2; run the Compliance test software on the oscilloscope.</p> 

Test Mode #	Description	Setup
4	Transmit distortion	<p>1. Connect the MDIP pin & MDIN to the oscilloscope via SMA cables.</p> <p>2. DUT, oscilloscope, and the disturbing signal should be synchronized by the same clock. The test suite does not define the method of synchronization. The following provides two common methods for synchronization.</p> <p>2a. Use an external function generator as a clock source of the DUT then connect the reference 10MHz input/output between the function generator and oscilloscope for synchronized.</p>  <p>2b. Output the TX_TXCLK on the PTP_GPIO pin and connect to a frequency divider (usually provided by the oscilloscope vendor). The frequency divider could provide a reference 10MHz to the oscilloscope.</p>  <p>3. Configure DUT as Test mode 4. Run the Compliance test software on the oscilloscope.</p>

Test Mode #	Description	Setup
5	PSD mask	<p>1. Connect the MDIP pin & MDIN to the oscilloscope via SMA cables. 2. Configure the DUT as Test mode 5. Run the Compliance test software on the oscilloscope.</p> 
NA	Slave transmit timing Jitter	<p>1. Configure the DUT as Slave and link up with the link partner. 2. Output the TX_TCLK on the PTP_GPIO pin and turn off the SSC function via the following settings. 2a. Write Address 0xD41E, bit [15:13]=0 2b. Write Address 0xD42A, bit [0]=0 2c. Write Address 0xD42C, bit [0]=1 2d. Write Address 0xD012, bit [2:0] =0 3. Connect the PTP_GPIO pin to the oscilloscope via an SMA cable 4. Run the Jitter measurement software on the oscilloscope.</p> 

Test Mode #	Description	Setup
NA	MDI Return Loss	<p>1. Configure the DUT as Slave. 2. Calibrate the Network analyzer and set the test parameter (usually provided by the test equipment vendor). 3. Connect the MDI pins to the Network analyzer via an SMA cable or through the test fixture. 4. Measure the reflections at the MDI referenced to a 100Ω characteristic impedance</p> 

Test Mode #	Description	Setup
NA	MDI Mode Conversion Loss	<p>1. Configure the DUT as Slave. 2. Calibrate the Network analyzer and set the test parameter (usually provided by the test equipment vendor.) The noise flow after the calibration of the Network analyzer, including the test fixture, must not exceed the limit line defined in the OPEN Alliance TC8 test suite, and the lower the better. 3. Connect the MDI pins to the Network analyzer via an SMA cable or through the test fixture. 4. Measure the reflections at the MDI referenced to a 100Ω characteristic impedance.</p> 

8.17. Auto-Negotiation

The RTL9000BF/BN/BR/BS/BSS supports Auto-Negotiation as defined in Clause 98 of the IEEE 802.3 specification. Through the mechanism of the Auto-Negotiation function, two devices negotiate the speed and role settings. Auto-Negotiation is disabled by default, and can be enabled by setting the relative bit shown in section 9.2.1, page 93, section 9.5.1, page 135, or section 9.5.3, page 136.

When the Auto-Negotiation function is enabled, registers from sections 9.5.1 to 9.5.16 show information related to Auto-Negotiation. Note that the two devices can only establish the link through Auto-Negotiation when both of them support it. That is to say, one PHY that enables the Auto-Negotiation function cannot link-up with another PHY that has no Auto-Negotiation function.

For both speed and role settings after Auto-Negotiation is complete, refer to section 9.2.16, page 100. Note that all Auto-Negotiation control registers will be reset to the default value after a software reset (see section 9.2.1, page 93, bit 15 to 1).

9. Register Descriptions

The registers of the RTL9000BF/BN/BR/BS/BSS are classified into three categories:

- General registers – Section 9.2, page 93
- PTP registers – Section 9.3, page 116
- OP registers – Section 9.4, page 125

Note: Each register has its own access method (refer to Table 19 Method of Accessing Registers, page 74).

The register access types are listed in Table 24:

Table 24. Register Access Types

Type	Description
LH	Latch high. If the status is high, this field is set to ‘1’ and remains set.
RC	Read-cleared. The register field is cleared after a read.
RO	Read only.
RW	Read and Write
SC	Self-cleared. Writing a ‘1’ to this register field causes the function to be activated immediately, and then the field will be automatically cleared to ‘0’.

Note that some of the reserved registers with RW type are internally used; WRITE is not allowed.

9.1. IEEE Standard Register Mapping and Definitions

Table 25. IEEE Standard Register Mapping and Definitions

Offset	Access	Name	Description
0	RW	BMCR	Basic Mode Control Register
1	RO	BMSR	Basic Mode Status Register
2	RO	PHYID1	PHY Identifier Register 1
3	RO	PHYID2	PHY Identifier Register 2
4~8	RO	RSVD	Reserved
9	RW	PHYCR	PHY Control Register
10	RO	PHYSR	PHY Status Register
13	RW	MACR	MMD Access Control Register
14	RW	MAADR	MMD Access Address Data Register
11,12,15	RO	RSVD	Reserved

9.2. General Register Tables

9.2.1. BMCR (Basic Mode Control Register, Reg 0x00)

Table 26. BMCR (Basic Mode Control Register, Reg 0x00)

Bit	Name	Type	Default	Description															
0.15	Reset	RW, SC	0	<p>Reset. 1: PHY reset 0: Normal operation</p> <p>Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit15 to 1). This action may change the internal the PHY state and the state of the physical link associated with the PHY.</p> <p>When software Reset is done by setting Reset (0.15) to 1, poll until Reset (0.15) to 0, or wait for at least 20ms to make sure the reset procedure is finished. The other PHY registers are accessible after the reset procedure.</p>															
0.14	PCS Loopback	RW	0	<p>PCS Loopback Mode. 1: Enable PCS loopback mode 0: Disable PCS loopback mode</p> <p>The loopback function enables MII/RMII/RGMII transmit data to be routed to the MII/RMII/RGMII receive data path. Refer to section 8.3.1, page 21.</p>															
0.13	Speed[0]	RO	0x01	<p>Speed Select Bit 0. In forced mode, bits 6 and 13 determine device speed selection.</p> <table border="1"> <thead> <tr> <th>Speed 1</th> <th>Speed 0</th> <th>Speed Enabled</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>100Mbps</td> </tr> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table>	Speed 1	Speed 0	Speed Enabled	1	1	Reserved	1	0	Reserved	0	1	100Mbps	0	0	Reserved
Speed 1	Speed 0	Speed Enabled																	
1	1	Reserved																	
1	0	Reserved																	
0	1	100Mbps																	
0	0	Reserved																	
0.12	Auto-Negotiation Enable	RW	0	<p>1: Enable Auto-Negotiation process 0: Disable Auto-Negotiation process</p>															
0.11	PWD	RW	0	<p>Power Down. 1: Power down (only Management Interface and logic are active; link is down) 0: Normal operation</p>															
0.10	Isolate	RW	0	<p>Isolate. 1: MII/RMII/RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL9000BF/BN/BR ignores TXD[3:0], and TXEN inputs, and presents a high impedance on TXC, RXC, RXDV, RXER, RXD[3:0]. 0: Normal operation</p>															
0.9	RSVD	RO	0	Reserved.															
0.8	Duplex	RO	0x01	<p>Duplex Mode. 1: Full Duplex operation</p>															
0.7	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.															
0.6	Speed[1]	RO	0	<p>Speed Select Bit 1. Refer to bit 0.13.</p>															

Bit	Name	Type	Default	Description
0.5	RSVD	RO	0	Reserved.
0.4:0	RSVD	RO	0	Reserved.

Note: When the RTL9000BF/BN/BR/BS/BSS is switched from power down to normal operation, a software reset is performed, even if bits Reset (Reg 0 bit[15]=1) is not set by the user.

9.2.2. BMSR (Basic Mode Status Register, Reg 0x01)

Table 27. BMSR (Basic Mode Status Register, Reg 0x01)

Bit	Name	Type	Default	Description
1.15:8	RSVD	RO	0	Reserved
1.6	Preamble Suppression	RO	0	1: PHY will accept mdc/mdio frames with preamble suppressed 0: PHY will not accept mdc/mdio frames with preamble suppressed
1.5:3	RSVD	RO	0x01	Reserved.
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, read this register twice. When the link status is 1, it also indicates local receiver status = 1 and scrambler_ok = 1. For the real time link status, refer to Table 41, page 100
1.1	Jabber Detect	RC, LH	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	0x01	1: Extended register capabilities, always 1

9.2.3. PHYID1 (PHY Identifier Register 1, Reg 0x02)

Table 28. PHYID1 (PHY Identifier Register 1, Reg 0x02)

Bit	Name	Type	Default	Description
2.15:0	OUI_MSB	RO	0x1C	Organizationally Unique Identifier Bit 3:18. Always 000000000011100.

Note: Realtek OUI is 0x00E04C

9.2.4. PHYID2 (PHY Identifier Register 2, Reg 0x03)

Table 29. PHYID2 (PHY Identifier Register 2, Reg 0x03)

Bit	Name	Type	Default	Description
3.15:10	OUI_LSB	RO	0x32	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	0x30	Manufacture's Model Number
3.3:0	Revision Number	RO	0000	Revision Number

9.2.5. PHYCR (PHY Control Register, Reg 0x09)

Table 30. PHYCR (PHY Control Register, Reg 0x09)

Bit	Name	Type	Default	Description
9.15:13	Test Mode	RW	0	Test Mode Select. 000: Normal mode 001: Test Mode 1 – Transmit droop Test 010: Test Mode 2 – Transmit Jitter Test (MASTER mode) 100: Test Mode 4 – Transmit Distortion Test 101: Test Mode 5 – Normal operation at full power (for PSD mask) 011, 110, 111: Reserved The test signal presents at MDI pins (MDIP and MDIN)
9.12	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
9.10:0	RSVD	RO	0	Reserved.

Note: A Software Reset (Reg 0 bit[15]=1) should be asserted in order to allow the change of bit 9.11 take effect.

9.2.6. PHYSR1 (PHY Status Register 1, Reg 0x0A)

Table 31. PHYSR1 (PHY Status Register 1, Reg 0x0A)

Bit	Name	Type	Default	Description
10.15	RSVD	RO	0	Reserved.
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK
10.11:8	RSVD	RO	0	Reserved.
10.7:0	Idle Error Count	RO, RC	0	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xFF.

9.2.7. MACR (MMD Access Control Register, Reg 0x0D)

Table 32. MACR (MMD Access Control Register, Reg 0x0D)

Bit	Name	Type	Default	Description
13.15:14	Function	RW	0	00: Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	0	Reserved.
13.4:0	DEVAD	RW	0	Device Address.

Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.

9.2.8. MAADR (MMD Access Address Data Register, Reg 0x0E)

Table 33. MAADR (MMD Access Address Data Register, Reg 0x0E)

Bit	Name	Type	Default	Description
14.15:0	Address Data	RW	0	13.15:14 = 00 → MMD DEVAD's address register 13.15:14 = 01, 10, or 11 → MMD DEVAD's data register as indicated by the contents of its address register

Note: This register is used in conjunction with the MACR (Register 13; Table 32) to provide access to the MMD address space.

9.2.9. PHYSFR (PHY Status Sub-flag Register, Page 0xA42, Reg 0x10)

Table 34. PHYSFR (PHY Status Sub-flag Register, Page 0xA42, Reg 0x10)

Bit	Name	Type	Default	Description
16.15:3	RSVD	RO	0x0C	Reserved.
16.2:0	PHY Status sub-flag	RO	0	PHY Status Indicator: 3'b000: Reserved 3'b001: PHY Initialization 3'b010: Reserved 3'b011: PHY Ready 3'b100: IEEE Std. Reset (Reg 0 bit[15]) 3'b101: PHY Power Down (Reg 0 bit[11])

9.2.10. RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11)

Table 35. RTCTCR (RTCT Control Register, Page 0xA42, Reg 0x11)

Bit	Name	Type	Default	Description
17.15	RTCT Done	RW	0	1: Indicates RTCT finished WRITE is not allowed.
17.14:1	RSVD	RO	0	Reserved
17.0	RTCT Enable	RW	0	1: Enable RTCT function

9.2.11. GINER (General Interrupt Enable Register, Page 0xA42, Reg 0x12)

Table 36. GINER (General Interrupt Enable Register, Page 0xA42, Reg 0x12)

Bit	Name	Type	Default	Description
18.15:12	RSVD	RW	0x0F	Reserved. Used internally; WRITE is not allowed.
18.11	PHY Fatal Error Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event. Page 0xA43, Reg29 Bit[11] always reflects the jabber interrupt behavior.
18.10	Jabber Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event. Page 0xA43, Reg29 Bit[10] always reflects the jabber interrupt behavior.
18.9	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
18.8	PTP Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PTP interrupt event. Page 0xA43, Reg29 Bit[8] always reflects the PTP interrupt behavior.
18.7:5	RSVD	RW	0x07	Reserved. Used internally; WRITE is not allowed.
18.4	Link Status Change Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the link status change interrupt event. Page 0xA43, Reg29 Bit[4] always reflects the link change interrupt behavior.
18.3	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
18.2	General Purpose Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the general purpose interrupt event. Page 0xA43, Reg29 Bit[2] always reflects the general purpose interrupt behavior.
18.1	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.

Bit	Name	Type	Default	Description
18.0	PHY Status Change Interrupt	RW	0x01	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PHY status change interrupt event. Page 0xA43, Reg29 Bit[0] always reflects the PHY status change interrupt behavior.

9.2.12. GINMR (General Interrupt Mask Register, Page 0xA42, Reg 0x14)

Table 37. GINMR (General Interrupt Mask Register, Page 0xA42, Reg 0x14)

Bit	Name	Type	Default	Description
20.15:12	RSVD	RW	0x0F	Reserved. Used internally; WRITE is not allowed.
20.11	MASK: PHY Fatal Error Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable
20.10	MASK: Jabber Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable
20.9	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
20.8	MASK: PTP Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable
20.7:5	RSVD	RW	0x07	Reserved. Used internally; WRITE is not allowed.
20.4	MASK: Link Status Change Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable
20.3	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
20.2	MASK: General Purpose Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable
20.1	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
20.0	MASK: PHY Status Change Interrupt	RW	0x01	1: Mask Enable 0: Mask Disable

9.2.13. SLPCR (Sleep Control Register, Page 0xA42, Reg 0x15)

Table 38. SLPCR (Sleep Control Register, Page 0xA42, Reg 0x15)

Bit	Name	Type	Default	Description
21.15:11	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
21.10	Stop_sleep	RW	0	1: Reject sleep flow
21.9	Sleep_Request	RW	0	1: Send Sleep Request to PHY and start sleep flow
21.8:0	RSVD	RW	0x36	Reserved. Used internally; WRITE is not allowed.

9.2.14. LKTCR (Link Timer Control Register, Page 0xA42, Reg 0x16)

Table 39. LKTCR (Link Timer Control Register, Page 0xA42, Reg 0x16)

Bit	Name	Type	Default	Description
22.15:3	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
22.2	Link_timer_stop_point	RW	0	1: The Link-timer will be stopped when both the link status of the DUT and the link partner are up 0: The Link-timer will be stopped when only the link status of the DUT is up
22.1:0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.

9.2.15. PHYCR (PHY Specific Control Register, Reg 0x18)

Table 40. PHYCR (PHY Specific Control Register, Reg 0x18)

Bit	Name	Type	Default	Description
24.15:14	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
24.13	PHYAD_0 Enable	RW	0x01	1: A broadcast from MAC (A command with the PHY address = 0) is valid. MDC/MDIO will respond to this command.
24.12:11	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
24.10	MDI Loopback	RW	0	1: Enable MDI Loopback mode 0: Disable MDI Loopback mode Refer to section 8.3.2, note that the MDI cable link must be removed in this mode.
24.9:8	RSVD	RO	0	Reserved.
24.7	TX CRS Enable	RW	0x01	1: Assert CRS on transmit 0: Never assert CRS on transmit
24.6	PHYAD Non-zero Detect	RW	0	1: The RTL9000BF/BN/BR/BS/BSS with PHYAD[2:0] = 000 will latch the first non-zero PHY address as its own PHY address
24.5	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
24.4	Preamble Check Enable	RW	0x01	1: Check preamble when receiving an MDC/MDIO command
24.3	Jabber Detection Enable	RW	0x01	1: Enable Jabber Detection
24.2:0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.

9.2.16. PHYSR2 (PHY Status Register 2, Reg 0x1A)

Table 41. PHYSR2 (PHY Status Register 2, Reg 0x1A)

Bit	Name	Type	Default	Description
26.15:12	RSVD	RO	0x02	Reserved.
26.11	Master mode	RO	0	Role setting after Auto-Negotiation. 1: Master Mode 0: Slave Mode
26.10:3	RSVD	RO	0x03	Reserved
26.2	Real-time Link Status	RO	0	Real-time Link Status. 1: Link 0: Not Link When the link status is 1, it also indicates local receiver status = 1 and scrambler_ok = 1.
26.1:0	RSVD	RO	0	Reserved

9.2.17. PHYSRAD (PHY SRAM Address Register, Reg 0x1B)

Table 42. PHYSRAD (PHY SRAM Address Register, Reg 0x1B)

Bit	Name	Type	Default	Description
27.15:0	PHY SRAM addr	RW	0	PHY internal SRAM address

9.2.18. PHYSRD (PHY SRAM Data Register, Reg 0x1C)

Table 43. PHYSRD (PHY SRAM Data Register, Reg 0x1C)

Bit	Name	Type	Default	Description
28.15:0	PHY SRAM data	RW	0	PHY internal SRAM data

9.2.19. GINSR (General Interrupt Status Register, Reg 0x1D)

Table 44. GINSR (General Interrupt Status Register, Reg 0x1D)

Bit	Name	Type	Default	Description
29.15:12	RSVD	RO	0	Reserved.
29.11	PHY Fatal Error	RO, RC	0	1: PHY Fatal Error occurred 0: No PHY Fatal Error occurred
29.10	Jabber	RO, RC	0	1: Jabber detected 0: No jabber detected <i>Note that the Jabber packet will be detected if the transmission time of the packet is longer than 1.08ms, namely around 13.5kbytes packet size.</i>
29.9	RSVD	RO	0	Reserved.
29.8	PTP Interrupt	RO, RC	0	1: PTP event occurred 0: No PTP event occurred
29.7:5	RSVD	RO	0	Reserved.
29.4	Link Status Change	RO, RC	0	1: Link status changed 0: Link status not changed
29.3	RSVD	RO	0	Reserved.

Bit	Name	Type	Default	Description
29.2	General Purpose Interrupt	RO, RC	0	1: General purpose event occurred 0: No general purpose event occurred Refer to the GPSFR (General Purpose Sub-Flag Register, Page 0xA47, Reg 0x15), page 101.
29.1	RSVD	RO	0	Reserved.
29.0	PHY Status Change	RO, RC	0x01	1: PHY status changed 0: PHY status not changed

9.2.20. PAGSR (Page Select Register, Reg 0x1F)

Table 45. PAGSR (Page Select Register, Reg 0x1F)

Bit	Name	Type	Default	Description
31.15:12	RSVD	RW	0	Reserved.
31.11:0	PageSel	RW	0xA42	Page Select (in Hex). 0xA42: Page 0xA42 (default page)

9.2.21. GPSFR (General Purpose Sub-Flag Register, Page 0xA47, Reg 0x15)

Table 46. GPSFR (General Purpose Sub-flag Register, Page 0xA47, Reg 0x15)

Bit	Name	Type	Default	Description
21.15:13	RSVD	RO	0	Reserved.
21.12	intr_LPS_WUR_encode	RO, RC	0	Sub-flag: LPS and WUR encoded at the same time
21.11	RSVD	RO	0	Reserved
21.10	intr_sleep_fail	RO, RC	0	Sub-flag: PHY has once entered SLEEP_FAIL state
21.9	intr_sleep_ack	RO, RC	0	Sub-flag: PHY has once entered SLEEP_ACK state
21.8:0	RSVD	RO	0	Reserved.

9.2.22. ISR (I/O Power Select Register, Page 0xA4C, Reg 0x12)

Table 47. ISR (I/O Power Select Register, Page 0xA4C, Reg 0x12)

Bit	Name	Type	Default	Description
18.15:14	RSVD	RO	0	Reserved.
18.13:11	IO_Power	RW	0	001: DVDD power supplied by the internal LDO, voltage is 1.8V. 010: DVDD power supplied by the internal LDO, voltage is 2.5V. 100: DVDD power supplied by external power, voltage is 1.8V. 101: DVDD power supplied by external power, voltage is 2.5V. 110: DVDD power supplied by external power, voltage is 3.3V.
18.10:0	RSVD	RO	0xFF	Reserved.

Note: Setting IO_Power register will also set the MII/RMII/RGMII driving strengths to Typical driving of the selected voltage (refer to section 8.10.4).

9.2.23. PCR (Polarity Control Register, Page 0xA58, Reg 0x15)

Table 48. PCR (Polarity Control Register, Page 0xA58, Reg 0x15)

Bit	Name	Type	Default	Description
21.15:10	RSVD	RO	0x3C	Reserved.
21.9:8	RSVD	RW	0x02	Reserved. Used internally; WRITE is not allowed.
21.7:5	RSVD	RO	0	Reserved.
21.4	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
21.3	Polarity_rx	RW	0	1: Disable the Polarity Correction Note that the bit [1] should be set to 1 at the same time.
21.2	RSVD	RO	0	Reserved.
21.1	Polarity_tx	RW	0	1: Disable the Polarity Correction Note that the bit [3] should be set to 1 at the same time
21.0	RSVD	RO	0	Reserved.

9.2.24. SLPCAP (Sleep Capability Register, Page 0xA5A, Reg 0x14)

Table 49. SLPCAP (Sleep Capability Register, Page 0xA5A, Reg 0x14)

Bit	Name	Type	Default	Description
20.15:1	RSVD	RO	0	Reserved.
20.0	Sleep Cap	RW	0	1: Enable Sleep capability

Note: A Software Reset (Reg 0 bit[15]=1) should be asserted in order To allow the change of bit 20.0 take effect.

9.2.25. PCS State (PCS State Register, Page 0xA60, Reg 0x10)

Table 50. PCS State (PCS State Register, Page 0xA60, Reg 0x10)

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0x33	Reserved.
16.7:0	PCS State	RO	Manual mode: 0 Auto mode: 0x41(Slave), 0x42(Master)	0x40: Disable Transmitter State 0x41: Slave Silent State 0x42: Training State 0x43: SEND IDLE State 0x44: SEND IDLE OR DATA State Refer to IEEE 802.3bw PHY Control State Diagram

9.2.26. SLR (Scrambler Lock Register, Page 0xA60, Reg 0x11)

Table 51. PLCR (Scrambler Lock Register, Page 0xA60, Reg 0x11)

Bit	Name	Type	Default	Description
17.15:5	RSVD	RO	-	Reserved.
17.4	Scrambler_ok	RO	0	1: Scrambler locked 0: Scrambler unlocked
17.3:0	RSVD	RO	-	Reserved

9.2.27. PCR (Polarity Correction Register, Page 0xA60, Reg 0x14)

Table 52. PLCR (Polarity Correction Register, Page 0xA60, Reg 0x14)

Bit	Name	Type	Default	Description
20.15:7	RSVD	RO	0	Reserved
20.8	Polarity Swap	RO	0	1: Polarity Swap
20.7:0	RSVD	RO	0	Reserved

9.2.28. LKTR (Link Timer Register, Page 0xA61, Reg 0x10)

Table 53. LKTR (Link Timer Register, Page 0xA61, Reg 0x10)

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0	Reserved
16.7:0	Link_timer	RO	-	To derive the link-up time, follow the steps in order: a. Set the stop point by writing Page 0xA42, Reg 22, bit [2] to 1 (refer to Section 9.2.12, page 98) b. Write, Reg 0, bit [15:0] to 0x8000 (SW Reset) c. Read the value of Page 0xA61, Reg 16, bit [7:0]. d. Calculation: Multiply the value of Page 0xA61, Reg 16, bit [7:0] (in decimal) to 983 (Resolution). The result is in μ C order.

9.2.29. RTCTSR (RTCT Status Register, Address 0x8022)

Table 54. RTCTSR (RTCT Status Register, Address 0x8022)

Bit	Name	Type	Default	Description
15:8	RTCT Status	RW	0	RTCT Cable Status Indication, refer to section 8.13, page 77 0x60: Normal 0x48: Open 0x50: Short WRITE is not allowed.
7:0	RSVD	RW	Varies	Do not care value. Used internally; WRITE is not allowed.

9.2.30. RTCTLR (RTCT Length Register, Address 0x8023)

Table 55. RTCTSR (RTCT Status Register, Address 0x8023)

Bit	Name	Type	Default	Description
15:0	RSVD	RW	Varies	RTCT abnormal point. WRITE is not allowed.

9.2.31. XDR (XTAL Driving Register, Address 0xBC52)

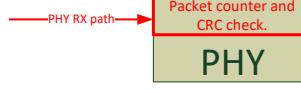
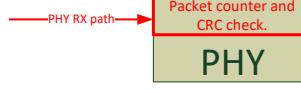
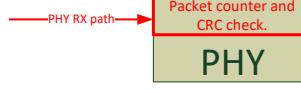
Table 56. XDR (XTAL Driving Register, Address 0xBC52)

Bit	Name	Type	Default	Description
15:12	RSVD	RW	0	Reserved Used internally; WRITE is not allowed.
11:10	Xtal_driving	RW	0	00: Maximum driving strength 11: Minimum driving strength The higher value the lower driving strength.
9:0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.

9.2.32. IPGR1 (Internal Packet Counter Register 1, Address 0xC800)

Table 57. IPCR1 (Internal Packet Counter Register 1, Address 0xC800)

Bit	Name	Type	Default	Description
15:8	RSVD	RW	0x5C	Reserved Used internally; WRITE is not allowed.
7:6	RSVD	RW	0	Reserved Used internally; WRITE is not allowed.
5:4	Remote Loopback	RW	0	2b'01: Enable Remote Loopback mode; refer to section 8.3.3.

Bit	Name	Type	Default	Description										
3:2	cnt_monitor_path_sel	RW	0	The selection of monitor path for the counter and CRC check of the internal packet counter.										
				<table border="1"> <thead> <tr> <th>Setting</th> <th>Monitor path</th> </tr> </thead> <tbody> <tr> <td>2b'00</td> <td>Monitor PHY's RX path; normal path. </td> </tr> <tr> <td>2b'01</td> <td>Monitor MAC's TX path. </td> </tr> <tr> <td>2b'10</td> <td>Reserved. Used internally; WRITE is not allowed.</td></tr> <tr> <td>2b'11</td> <td>Reserved. Used internally; WRITE is not allowed.</td></tr> </tbody> </table>	Setting	Monitor path	2b'00	Monitor PHY's RX path; normal path. 	2b'01	Monitor MAC's TX path. 	2b'10	Reserved. Used internally; WRITE is not allowed.	2b'11	Reserved. Used internally; WRITE is not allowed.
Setting	Monitor path													
2b'00	Monitor PHY's RX path; normal path. 													
2b'01	Monitor MAC's TX path. 													
2b'10	Reserved. Used internally; WRITE is not allowed.													
2b'11	Reserved. Used internally; WRITE is not allowed.													
1	En_int_cnt	RW	0	1: Enable the PHY's packet counter.										
0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.										

9.2.33. IPCR2 (Internal Packet Counter Register 2, Address 0xC802)

Table 58. IPGR2 (Internal Packet Counter Register 2, Address 0xC802)

Bit	Name	Type	Default	Description
15:7	RSVD	RO	0	Reserved.
6	int_cnterr_clr	RW, SC	0	1: Clear the error packet counter.
5	int_cnt_clr	RW, SC	0	1: Clear the packet counter.
4:2	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
1	Rx_pktgen_reset	RW, SC	0	1: Reset packet counter.
0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.

9.2.34. IPCR3 (Internal Packet Counter Register 3, Address 0xC810)

Table 59. IPCR3 (Internal Packet Counter Register 3, Address 0xC810)

Bit	Name	Type	Default	Description
15:0	int_cnt_lsb	RO	0	LSB [15:0] of received packet counter; wrap to zero when overflow. Can be cleared by int_cnt_clr on the section 9.2.33.

9.2.35. IPCR4 (Internal Packet Counter Register 4, Address 0xC812)

Table 60. IPCR4 (Internal Packet Counter Register 4, Address 0xC812)

Bit	Name	Type	Default	Description
15:0	int_cnt_msb	RO	0x00	MSB [31:16] of received packet counter; wrap to zero when overflow. Can be cleared by int_cnt_clr; see section 9.2.33.

9.2.36. IEPCR (Internal Error Packet Counter Register, Address 0xC814)

Table 61. IEPCR (Internal Error Packet Counter Register, Address 0xC814)

Bit	Name	Type	Default	Description
15:0	int_err_cnt	RO	0	Received error packet counter; Saturated when it reaches 16h'FFFF. Can be cleared by int_cnterr_clr; see section 9.2.33.

9.2.37. SSCCR (SSC Control Register, Address 0xD012)

Table 62. SSCCR (SSC Control Register, Address 0xD012)

Bit	Name	Type	Default	Description
15:3	RSVD	RW	0x02	Reserved. Used internally; WRITE is not allowed.
2	RMII REF_CLK SSC Enable	RW	0x01	1: Enable RMII REF_CLK spread spectrum clocking.
1	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
0	System Clock SSC Enable	RW	0x01	1: Enable system clock spread spectrum clocking.

9.2.38. SAER (Special Access Enable Register, Address 0xD030)

Table 63. SAER (Special Access Enable Register, Address 0xD030)

Bit	Name	Type	Default	Description
15:10	RSVD	RO	0	Reserved.
9:8	RSVD	RW	0x02	Reserved. Used internally; WRITE is not allowed.
7:5	RSVD	RO	0	Reserved.
4	En_reg_27_dis	RW	0x01	1: Enable the write function of the Register 27 during the Safety Mode
3:2	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
1	En_mdio_write	RW	0	1: Enable the MDIO write function during the Safety Mode.
0	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.

9.2.39. RXDVCR (RXDV Control Register, Address 0xD050)

Table 64. RXDVCR (RXDV Control Register, Address 0xD050)

Bit	Name	Type	Default	Description
15	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
14	RMII Mode	RW	Varies	0: PHY is operating in MII mode 1: PHY is operating in RMII mode Decided by hardware configuration, WRITE is not allowed.
13	RMII_clk_dir	RW	Varies	Clock direction of RMII mode 0: RMII Output mode 1: RMII Input mode Decided by hardware configuration, WRITE is not allowed.
12:9	RMII_TX_timing*	RW	0x07	Adjust the RMII_TX_Timing, can be set to 0-9; around 2ns per level
8:5	RMII_RX_timing*	RW	0x03	Adjust the RMII_RX_Timing, can be set to 0-9; around 2ns per level
4:3	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
2	RMII_CRS_SEL*	RW	0x01	1: The RXDV signal is sent with CRS signal 0: The RXDV signal is sent without CRS signal
1:0	RSVD	RW	0x03	Reserved. Used internally; WRITE is not allowed.

Note: *Issue a Software Reset (Reg 0 bit[15]=1) after any adjustment above.

9.2.40. RGTR (RGMII Timing Control Register, Address 0xD082)

Table 65. RGTR (RGMII Timing Control Register, Address 0xD082)

Bit	Name	Type	Default	Description
15	RSVD	RO	0	Reserved.
14	RGMII Mode	RW	Varies	1: PHY is operating in RGMII mode Decided by hardware configuration, WRITE is not allowed.
13:11	RSVD	RW	0	Reserved. Used internally; WRITE is not allowed.
10	TXC_inv*	RW	0	1: Inverse the TXC waveform <i>Note that if this bit is set to 1, the bit[9:8] RGMII TXC timing should be set to 2'b 10</i>
9:8	RGMII_TXC_timing*	RW	00	Add the delay for TXC latching TXD; 4ns per level. For timing requirements, refer to section 11.11.5.
7:4	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
3:0	RGMII_RXC_timing*	RW	0	Add the delay for RXC latching RXD, can be set from 0-9; 4ns per level. For timing requirements, refer to section 11.11.5.

Note: *Issue a Software Reset (Reg 0 bit[15]=1) after any adjustment above.

9.2.41. LEDCR (LED Control Register, Address 0xD040)

Table 66. LEDCR (LED Control Register, Address 0xD040)

Bit	Name	Type	Default	Description
15	led_enable	RW	0x01	1: LED enable
14	led_polar	RW	0x01	LED polarity bit. 1: Active high 0: Active low
13	led_rtct	RW	0	Switch LED modes between link status & cable diagnostics (RTCT) results. 0: Link status 1: RTCT results
12:11	RSVD	RO	0	Reserved.
10:8	RSVD	RW	0x06	Reserved. Used internally; WRITE is not allowed.
7:6	RSVD	RO	0	Reserved.
5:4	led_blink_duty	RW	0x02	LED blink duty cycle. 2'b00: 12.5% 2'b01: 25% 2'b10: 50% 2'b11: 75%
3:2	led_blink_freq	RW	0x01	LED blink frequency control. 2'b00: 20ms 2'b01: 40ms 2'b10: 60ms 2'b11: Reserved
1	led_act	RW	0x01	1: LED blinks when in traffic
0	led_link	RW	0x01	1: LED turns ON when link-up

9.2.42. SPCR1 (SSC Phase Control Register 1, Address 0xD096)

Table 67. SPCR1 (SSC Strength Control Register 1, Address 0xD096)

Bit	Name	Type	Default	Description
15	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
14:13	Phase_strength1	RW	0x02	2'b00: LOW 2'b01: Medium 2'b10: HIGH To support the Jumbo frame in RGMII and MII mode, refer to section 8.12. Note that Phase_strength 2 should be adjusted at the same time, refer to section 9.2.43.
12:0	RSVD	RW	0x1F05	Reserved. Used internally; WRITE is not allowed.

9.2.43. SPCR2 (SSC Strength Control Register 2, Address 0xD0B6)

Table 68. SPCR2 (SSC Strength Control Register 2, Address 0xD0B6)

Bit	Name	Type	Default	Description
15	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
14:13	Phase_strength2	RW	0x02	2'b00: LOW 2'b01: Medium 2'b10: HIGH To support the Jumbo frame in RGMII and MII mode, refer to section 8.12. Note that Phase_strength1 should be adjusted at the same time; refer to section 9.2.42.
12:0	RSVD	RW	0x1F05	Reserved. Used internally; WRITE is not allowed.

9.2.44. MSE (Mean Square Error Register, Address 0xD100)

Table 69. MSE (Mean Square Error Register, Address 0xD100)

Bit	Name	Type	Default	Description
16.15:10	RSVD	RO	0	Reserved
16.9	MSE_valid	RO	0x01	1: The MSE value [8:0] is invalid 0: The MSE value [8:0] is valid
16.8:0	MSE	RO	0x01FF	MSE value 0x0000 MSE = 0 ... 0x01FE MSE = 510 0x01FF MSE = 511

9.2.45. WMSE (Worst MSE Value Register, Address 0xD102)

Table 70. WMSE (Worst MSE Value Register, Address 0xD102)

Bit	Name	Type	Default	Description
17.15:10	RSVD	RO	0	Reserved
17.9	MSE_WC_valid	RO	0x01	1: The MSE_WC value [8:0] is invalid 0: The MSE_WC value [8:0] is valid
17.8:0	MSE_WC	RO	0x01FF	Worst MSE value since the last read 0x0000 MSE_WC = 0 ... 0x01FE MSE_WC = 510 0x01FF MSE_WC = 511

9.2.46. PMSE (Peak MSE Value Register, Address 0xD104)

Table 71. PMSE (Peak MSE Value Register, Address 0xD104)

Bit	Name	Type	Default	Description
18.15	RSVD	RO	0	RSVD
18.14	pMSE_WC_valid	RO	0x01	1: The pMSE_WC value [13:8] is invalid 0: The pMSE_WC value [13:8] is valid
18.13:8	pMSE_WC	RO	0	Worst case peak MSE value since last read 0x00 peakMSE = 0 0x01 peakMSE = 1 0x3E peakMSE = 62 0x3F peakMSE = 63 0x40 value invalid
18.6	pMSE_valid	RO	0x01	1: The pMSE value [5:0] is invalid 0: The pMSE value [5:0] is valid
18.5:0	pMSE	RO	0	Current 0x00 peakMSE = 0 0x01 peakMSE = 1 0x3E peakMSE = 62 0x3F peakMSE = 63 0x40 value invalid

9.2.47. SQI (Signal Quality Index Register, Address 0xD106)

Table 72. SQI (Signal Quality Index Register, Address 0xD106)

Bit	Name	Type	Default	Description
19.15:8	RSVD	RO	0	Reserved
19.7:5	Worst case SQI value	RO	0	Worst case SQI value
19.4	RSVD	RO	0	Reserved
19.3:1	Current SQI Value	RO	0	000: SQI=0 (worst value) 001: SQI=1 010: SQI=2 011: SQI=3 100: SQI=4 101: SQI=5 110: SQI=6 111: SQI=7 (best value)
19.0	RSVD	RO	0	Reserved

9.2.48. LTT (Link Training Time Register, Address 0xD110)

Table 73. LTT (Link Training Time Register, Address 0xD110)

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0	Reserved
16.7:0	LTT	RO	0xFF	Link training time 0x00: 0ms 0x01: 1ms ... : ... 0x64: 100ms ... : ... 0xFA: 250ms 0xFB: more than 250ms ... : timer is not available 0xFF : measurement not possible

9.2.49. LRT (Local Receiver Time Register, Address 0xD112)

Table 74. LRT (Local Receiver Time Register, Address 0xD112)

Bit	Name	Type	Default	Description
17.15:8	RSVD	RO	0	Reserved
17.7:0	Loc_rcvr_t	RO	0xFF	Time until local_receiver status =OK 0x00: 0ms 0x01: 1ms ... : ... 0x64: 100ms ... : ... 0xFA: 250ms 0xFB: more than 250ms ... : timer is not available 0xFF : measurement not possible

9.2.50. RRT (Remote Receiver Time Register, Address 0xD114)

Table 75. RRT (Remote Receiver Time Register, Address 0xD114)

Bit	Name	Type	Default	Description
18.15:8	RSVD	RO	0	Reserved
18.7:0	rem_rcvr_t	RO	0xFF	Time until remote_receiver status =OK 0x00: 0ms 0x01: 1ms ... : ... 0x64: 100ms ... : ... 0xFA: 250ms 0xFB: more than 250ms ... : timer is not available 0xFF : measurement not possible

9.2.51. LFL (Link Failures and Losses Counter Register, Address 0xD120)

Table 76. LFL (Link Failures and Losses Counter Register, Address 0xD120)

Bit	Name	Type	Default	Description
16.15:10	Link_loss	RO	0	Number of Link Losses occurred since last power cycle
16.9:0	Link_fail	RO	0	Number of Link Failures causing NOT a link loss (SSD failure, ESD failure, etc.) since last power cycle

9.2.52. LED_PTP (LED/PTP_GPIO Select Register, Address 0xD42A)

Table 77. LED_PTP (LED/PTP_GPIO Select Register, Address 0xD42A)

Bit	Name	Type	Default	Description
15:1	RSVD	RW	0x7FFF	Reserved. Used internally; WRITE is not allowed.
0	rg_led_thru_ptp_pin	RW	0x01	1: Pin 34 acts as LED pin 0: Pin 34 acts as PTP_GPIO pin

9.2.53. WAKE_O (WAKE Out Select Register, Address 0xD446)

Table 78. WAKE_O (WAKE Out Select Register, Address 0xD446)

Bit	Name	Type	Default	Description
15:2	RSVD	RO	0x04	Reserved.
1	Wake_out_pulse_length	RW	0	1: Wake-out pulse will be 490~510ms positive pulse. 0: Wake-out pulse will be 40~50us positive pulse.
0	Wake_out_enable	RW	0	1: Wake-out function enable, LED/PTP_GPIO/WAKE_O pin will be configure as WAKE_O pin and it will forward wake-out pulse when it receive WUP or WUR. 0: Wake-out function disable.

Note: Do not change Wake_out_pulse_length after Wake_out_enable = 1.

9.2.54. OP Mode (OP Mode Register, Address 0xDF10)

Table 79. OP Mode (OP Mode Register, Address 0xDF10)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0	Reserved.
7:0	Op_Mode	RW	Varies	Indicates the operating mode as follows: 0x20: Standby Mode 0x30: Normal Mode 0x31: Safety Mode

9.2.55. RG_Config (RG App Configure Register, Page 0xA47, Reg 0x17)

Table 80. RG_Config (RG APP Configure Register, Page 0xA47, Reg 0x17)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	0	Reserved.
3:0	rg_application_cfg	RW	0	0: xMII (MII/RMII/RGMII) => 100Base-T1. 1: SGMII (PHY side) => 100Base-T1. 2: RGMII to SGMII (PHY side@100Mbps) 3: RGMII to SGMII (PHY side@1000Mbps) 4: RGMII to SGMII (MAC side)

9.2.56. SGMIICR1 (SGMII Control Register 1, Address 0xCC04)

Table 81. SGMIICR1 (SGMII Control Register 1, Address 0xCC04)

Bit	Name	Type	Default	Description
15:10	RSVD	RW	0x1C	Reserved. Used internally; WRITE is not allowed.
9:8	SGMII_mode	RW	0	00: Enable SGMII Auto-Negotiation 01: Enable SGMII Force mode
7:0	RSVD	RW	0x80	Reserved. Used internally; WRITE is not allowed.

9.2.57. SGMIICR2 (SGMII Control Register 2, Address 0xCE00)

Table 82. SGMIICR2 (SGMII Control Register 2, Address 0xCE00)

Bit	Name	Type	Default	Description
15:1	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
0	SGMII_rst	RW	0x01	To reset the SGMII, please write this bit to 0 first then write back to 1.

9.2.58. SGMIISR1 (SGMII Status Register 1, Address 0xCE0C)

Table 83. SGMIISR1 (SGMII Status Register 1, Address 0xCE0C)

Bit	Name	Type	Default	Description
15:5	RSVD	RO	0x04	Reserved.
4	MDI_link_status	RO	0	MDI link status. 1: Link up 0: Link down
3:2	RSVD	RO	0x01	Reserved.
1:0	SGMII_speed	RO	0x01	SGMII link speed. 01: 100M 10: 1000M

9.2.59. SGMIISR2 (SGMII Status Register 2, Address 0xCF04)

Table 84. SGMIISR2 (SGMII Status Register 2, Address 0xCF04)

Bit	Name	Type	Default	Description
15:13	RSVD	RO	Varies.	Reserved.
12	SGMII_link_status	RO	0	SGMII link status. 1: SGMII link up 0: SGMII not link up Note that SGMII will re-link up after 5-10ms when MDI link up.
1:0	RSVD	RO	0	Reserved.

9.2.60. SGMIICR3 (SGMII Control Register 3, Page 0xCD1, Reg 0x16)

Table 85. SGMIICR3 (SGMII Control Register 3, Page 0xCD1, Reg 0x16)

Bit	Name	Type	Default	Description										
15:7	RSVD	RW	0	Reserved.										
6:1	TX_AMP	RW	0x24	TX amplitude adjustment for SGMII. <table border="1" data-bbox="794 1347 1429 1594"> <tr> <td>TX_AMP</td> <td>Nominal value of Vpp.</td> </tr> <tr> <td>0x24</td> <td>700mv</td> </tr> <tr> <td>0x2D</td> <td>580mv</td> </tr> <tr> <td>0x36</td> <td>450mv</td> </tr> <tr> <td>Other value</td> <td>Not recommended; May result in out of SGMII mask specification.</td> </tr> </table> Note: Please check the minimum acceptable receiving voltage of link partner, if want to decrease the TX amplitude.	TX_AMP	Nominal value of Vpp.	0x24	700mv	0x2D	580mv	0x36	450mv	Other value	Not recommended; May result in out of SGMII mask specification.
TX_AMP	Nominal value of Vpp.													
0x24	700mv													
0x2D	580mv													
0x36	450mv													
Other value	Not recommended; May result in out of SGMII mask specification.													
0	RSVD	RW	0	Reserved.										

9.2.61. COMR (Communication Register, Page 0xD12, Reg 0x11)

Table 86. COMR (Communication Register, Page 0xD12, Reg0x11)

Bit	Name	Type	Default	Description
15:1	RSVD	RO	0	Reserved.
0	comm_ready_status	RO	0	Communication ready status.

9.2.62. TRACR (Training Control Register, Page 0xA5A, Reg 0x15)

Table 87. TRACR (Training Control Register, Page 0xA5A, Reg0x15)

Bit	Name	Type	Default	Description
15:1	RSVD	RO	0	Reserved.
0	en_maxwait_timeout_transition_path	RW	0	<p>Enable the additional transition path at the PHY control state diagram when the maxwait_timer expires.</p> <p>1: Enable 0: Disable</p> <p><i>Note: When enabled, the PHY control state diagram will return to SLAVE_SLAVE state upon timer expiration.</i></p>

9.3. PTP Register Tables

9.3.1. PTP_CTL (PTP Control Register, Address 0xE400)

Table 88. PTP_CTL (PTP Control Register, Address 0xE400)

Bit	Name	Type	Default	Description
15	Rx_TS_insertion_en	RW	0	Enable Rx timestamp insertion for Sync/delay_req/pdelay_req/pdelay_resp: 0: Disable 1: Enable <i>Note. If PTP message is carried in UDP, the UDP checksum is neither checked nor recalculated, it is changed to 0 to skip checksum.</i>
14	RSVD	RW	0x01	Reserved. Used internally; WRITE is not allowed.
13	PTP_VLAN_EN	RW	0x01	Enable parsing PTP message with VLAN tag. 0: Disable support PTP message with VLAN tag 1: Enable support PTP message with VLAN tag
12	UDP_CHKSUM Update	RW	0	Enable auto-correction of UDP Checksum if One-Step Timestamp Insertion is enabled. Only effective for IPv6/UDP packets. 0: Set 0x0000 to the UDP Checksum field 1: Re-compute the UDP Checksum
11	P_DRFU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp_Follow_Up messages.
10	P_DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp messages.
9	DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Delay_Resp messages.
8	FU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Follow_Up messages.
7	P_DR_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t3-t2) to Pdelay_Response messages.
6	SYNC_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t1) to Sync messages.
5	802.1AS Support	RW	0	1: 802.1AS standard support
4	PTPv2_Layer2 Support	RW	0	1: PTPv2 Layer 2 packet support
3	PTPv2_UDPIPv4 Support	RW	0	1: PTPv2 UDP/IPv4 packet support
2	PTPv2_UDPIPv6 Support	RW	0	1: PTPv2 UDP/IPv6 packet support
1	PTPv1 Support	RW	0	1: PTPv1 packet support
0	PTP_Enable	RW	0	PTP function enable. <i>Note: Issue a Software Reset (Reg 0 bit[15]=1) after setting this bit in order to enable/disable PTP function.</i>

9.3.2. PTP_INER (PTP Interrupt Enable Register, Address 0xE402)

Table 89. PTP_INER (PTP Interrupt Enable Register, Address 0xE402)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	0	Reserved.
3	Tx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Transmit Timestamp ready interrupt.
2	Rx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Receive Timestamp ready interrupt.
1	TrigGen Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Trigger Generate complete interrupt.
0	EventCap Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Event Capture timestamp ready interrupt.

9.3.3. PTP_INSR (PTP Interrupt Status Register, Address 0xE404)

Table 90. PTP_INSR (PTP Interrupt Status Register, Address 0xE404)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	0	Reserved
3	Tx Timestamp Interrupt	RO, RC	0	1: Transmit Timestamp ready interrupt detected
2	Rx Timestamp Interrupt	RO, RC	0	1: Receive Timestamp ready interrupt detected
1	TrigGen Interrupt	RO, RC	0	1: Trigger Generate complete interrupt detected
0	EventCap Interrupt	RO, RC	0	1: Event Capture timestamp ready interrupt detected

9.3.4. PTP_CLK_CFG (PTP Clock Config Register, Address 0xE410)

Table 91. PTP_CLK_CFG (PTP Clock Config Register, Address 0xE410)

Bit	Name	Type	Default	Description
15:9	RSVD	RO	0	Reserved.
8:7	ptp_target_timer_sel	RW	0	Select Target PTP timer: 0: Local clock (Read only timer) 1: PTP timer 0 2: Reserved 3: Reserved
6:5	ptp_clkin_freq_sel	RW	0	PTP CLKIN Frequency Select. 00: 125MHz 01: 25MHz 10: 10MHz 11: Reserved <i>Note: Issue a Software Reset (Reg 0 bit[15]=1) in order to allow the setting to take effect.</i>
4	ptp_clkin_en	RW	0	1: Enable PTP CLKIN function at PTP_GPIO pin <i>Note: Issue a Software Reset (Reg 0 bit[15]=1) in order to allow the setting to take effect.</i>

Bit	Name	Type	Default	Description
3:1	ptp_clkadj_mod	RW	0	PTP Clock Adjustment Mode Select. 000: No function 001: Reserved - Issue Direct Read/Write to PTP_Local_Time through PTP_Time_Config registers 010: Direct Read 011: Direct Write - Issue Step Adjustment to PTP_Local_Time through PTP_Time_Config registers 100: Increment Step 101: Decrement Step - Issue Rate Adjustment Read/Write to PTP_Rate_Adj_Amt through PTP_Time_Config_ns registers [24:0]. A 2's complement representation should be used if a negative rate adjustment is needed. 110: Rate Read 111: Rate Write
0	ptp_clkadj_mod_set	RW, SC	0	PTP Clock Adjustment Mode Set. 1: Activate the selected clock adjustment mode as related parameters are properly inserted.

9.3.5. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Address 0xE412)

Table 92. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Address 0xE412)

Bit	Name	Type	Default	Description
15:0	PTP_Time_Config_ns[15:0]	RW	0	Time configuration nano-sec field [15:0] / Rate adjustment multiplier field [15:0] A 2's complement representation should be used if a negative rate adjustment is needed.

9.3.6. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Address 0xE414)

Table 93. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Address 0xE414)

Bit	Name	Type	Default	Description
15:14	RSVD	RO	0	Reserved.
13:0	PTP_Time_Config_ns[29:16]	RW	0	<p>Time configuration nano-sec field_ns [29:16] when PTP Clock Adjustment Mode Select is not rate read/write.</p> <p>Rate adjustment multiplier field [24:16] when PTP Clock Adjustment Mode Select is rate read/write: A 2's complement representation should be used if a negative rate adjustment is needed.</p> <p>[29:25]: No effect when written; reflects Sign Extension result when read.</p>

9.3.7. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Address 0xE416)

Table 94. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Address 0xE416)

Bit	Name	Type	Default	Description
15:0	PTP_Time_Config_s[15:0]	RW	0	Time configuration sec field [15:0].

9.3.8. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Address 0xE418)

Table 95. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Address 0xE418)

Bit	Name	Type	Default	Description
15:0	PTP_Time_Config_s[31:16]	RW	0	Time configuration sec field [31:16].

9.3.9. PTP_CFG_S_HI (PTP Time Config Sec High Register, Address 0xE41A)

Table 96. PTP_S_HI (PTP Time Config Sec High Register, Address 0xE41A)

Bit	Name	Type	Default	Description
15:0	PTP_Time_Config_s[47:32]	RW	0	Time configuration sec field [47:32].

9.3.10. PTP_TAI_CFG (PTP Application I/F Config Register, Address 0xE420)

Table 97. PTP_TAI_CFG (PTP Application I/F Config Register, Address 0xE420)

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0	Reserved.
11:10	reference_timer_sel	RW	0	Select reference PTP timer for GPIO(Tai) function: 00: Local clock 01: PTP clock - instance 0 10: Reserved 11: Reserved
9:8	trig_mod_sel	RW	0	Trigger Generate mode select. Trigger(s) start at time specified in TAI_TS_RW registers. Valid if tai_func_sel = 01. 00: Single rising edge 01: Single falling edge (The high/low level of the GPIO will be adjusted by HW automatically.) 10: Single pulse. The pulse width can be set by pulse_amt fields 11: Periodic pulses. The pulse period and duty cycle can be set by pulse_amt (Address 0xE422, bit[9:0]) and pulse_dc (Address 0xE422, bit[13:12]) fields, see section 9.3.11.
7	trig_iflate	RW	0	Trigger-if-Late Control. Valid if tai_func_sel (Bit 2:1) = 01. 1: Allow an immediate Trigger when setting a time value that is earlier than the current time.
6	evnt_rf_det	RW	0	Event Capture rising/falling edge detects selection. Valid if tai_func_sel (Bit 2:1) = 10. 0: Detection of a rising edge 1: Detection of a falling edge SW should take care of the high/low level of GPIO with this setting.
5	evnt_overwr_en	RW	0x01	Event Capture timestamp overwrite enables. Valid if tai_func_sel (Bit 2:1) = 10. 0: Keep the old value, 1: Cause the event timestamp to be overwritten if a new event is detected at the specific GPIO if the upper layer has not yet read the old event timestamp.
4:3	tai_gpio_num	RW	0	The GPIO number that is going to be armed.
2:1	tai_func_sel	RW	0	PTP Application Interface function select of selected GPIO. 00: Disable function 01: Trigger Generate 10: Event Capture 11: Trigger start time/Event timestamp read (according to current GPIO settings)
0	tai_cfg_set	RW, SC	0	PTP Application Interface configuration set. Setting this bit will issue a TAI Configuration ‘Set’ to the selected GPIO via tai_gpio_num

9.3.11. PTP_TRIGGER_CFG (PTP Trigger Config Register, Address 0xE422)

Table 98. PTP_TRIGGER_CFG (PTP Trigger Config Register, Address 0xE422)

Bit	Name	Type	Default	Description
15:14	RSVD	RO	0	Reserved.
13:12	pulse_dc	RW	0	Duty Cycle of a Trigger Pulse. Valid if tai_func_sel (Address 0xE420, bit[2:1]) = 01. Takes effect only on GPIO 0/1. 00: 0% 01: 25% 10: 50% 11: 75%. <i>Note: The options of 0%, 25%, and 75% are available only when pulse_amt >= 8.</i>
11:10	pulse_amt_unit	RW	0	The unit of pulse_amt field. 00: 10 nano-second (10 ns) 01: 1.25 micro-second (1.25 µs) 10: 1.25 milli-second (1.25 ms) 11: 1.25 second (1.25 sec)
9:0	pulse_amt	RW	0	Period of periodic pulses/Width of a single pulse. <i>Note: pulse_amt should be greater than 0.</i>

9.3.12. PTP_TAI_STA (PTP Application I/F Status Register, Address 0xE424)

Table 99. PTP_TAI_STA (PTP Application I/F Status Register, Address 0xE424)

Bit	Name	Type	Default	Description
15	tai_gpio_func	RO	0	Indicate PTP_GPIO's TAI function 0: Trigger Generate 1: Event Capture
14	tai_gpio_en	RO	0	TAI function is enabled at PTP_GPIO.
13	tai_gpio_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at PTP_GPIO.
12	tai_gpio_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept.
11:0	RSVD	RO	0	Reserved.

9.3.13. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Address 0xE426)

Table 100. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Address 0xE426)

Bit	Name	Type	Default	Description
15:0	TAI_TS_ns[15:0]	RW	0	PTP Application Interface timestamp Read/Write interface nanosec field [15:0].

9.3.14. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Address 0xE428)

Table 101. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Address 0xE428)

Bit	Name	Type	Default	Description
15:14	RSVD	RO	0	Reserved.
13:0	TAI_TS_ns[29:16]	RW	0	PTP Application Interface timestamp Read/Write interface nanosec field [29:16].

9.3.15. PTP_TAI_TS_S_LO (PTP TAI Timestamp Sec Low Register, Address 0xE42A)

Table 102. PTP_S_LO (PTP Time Config Sec Low Register, Address 0xE42A)

Bit	Name	Type	Default	Description
15:0	TAI_TS_s[15:0]	RW	0	PTP Application Interface timestamp Read/Write interface sec field [15:0].

9.3.16. PTP_TAI_TS_S_HI (PTP TAI Timestamp Sec High Register, Address 0xE42C)

Table 103. PTP_S_MI (PTP Time Config Sec Mid Register, Address 0xE42C)

Bit	Name	Type	Default	Description
15:0	TAI_TS_s[31:16]	RW	0	PTP Application Interface timestamp Read/Write interface sec field [31:16].

9.3.17. PTP_TRX_TS_CTL (PTP TxRx Timestamp Control Register, Address 0xE430)

Table 104. PTP_TRX_TS_CTL (PTP TxRx Timestamp Control Register, Address 0xE430)

Bit	Name	Type	Default	Description
15:7	RSVD	RO	0	Reserved.
6	compen_ssc_en	RW	0x01	Compensate SSC affected time: 0: Disable compensation 1: Enable compensation
5	trxts_instance_sel	RW	0	PTP instance selection: 0: Instance 0 1: Reserved
4	trxts_overwr_en	RW	0x01	Transmit/Receive timestamp overwrite enable. When a new PTP packet comes that needs to be timestamped, HW will: 0: Keep the old timestamp value 1: Overwrite the old timestamp value if the older one has not been read by the upper layer

Bit	Name	Type	Default	Description
3:2	trxts_msatype_sel	RW	0	Message Type of Transmit/Receive timestamp select. 00: Sync 01: Delay_Request 10: PDelay_Request 11: PDelay_Response
1	trxts_sel	RW	0	Transmit/Receive timestamp read select. 0: Tx 1: Rx
0	trxts_rd	RW, SC	0	Transmit/Receive timestamp read enable. Issue a ‘Read’ for Transmit/Receive timestamp.

9.3.18. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Address 0xE432)

Table 105. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Address 0xE432)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0	Reserved.
7	txts_sync_rdy_0	RO	0	Sync message Transmit timestamp ready of instance 0
6	txts_dlyreq_rdy_0	RO	0	Delay_Request Transmit timestamp ready of instance 0
5	txts_pdlyreq_rdy_0	RO	0	PDelay_Request Transmit timestamp ready of instance 0
4	txts_pdlyrsp_rdy_0	RO	0	PDelay_Response Transmit timestamp ready of instance 0
3	rxts_sync_rdy_0	RO	0	Sync message Receive timestamp ready of instance 0 timestamp
2	rxts_dlyreq_rdy_0	RO	0	Delay_Request Receive timestamp ready of instance 0
1	rxts_pdlyreq_rdy_0	RO	0	PDelay_Request Receive timestamp ready of instance 0
0	rxts_pdlyrsp_rdy_0	RO	0	PDelay_Response Receive timestamp ready of instance 0

9.3.19. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Address 0xE440)

Table 106. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Address 0xE440)

Bit	Name	Type	Default	Description
15:12	trxts_transspec	RO	0	Transmit/Receive timestamp Transport Specific field
11:8	trxts_msatype	RO	0	Transmit/Receive timestamp Message Type field
7:4	RSVD	RO	0	Reserved
3:0	trxts_ptpver	RO	0	Transmit/Receive timestamp PTP Version field

9.3.20. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Address 0xE444)

Table 107. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Address 0xE444)

Bit	Name	Type	Default	Description
15:0	trxts_seqid	RO	0	Transmit/Receive timestamp Sequence ID field

9.3.21. PTP_TRX_TS_NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Address 0xE446)

Table 108. PTP_TRX_TS_NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Address 0xE446)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_ns[15:0]	RO	0	Transmit/Receive timestamp nanosecond field [15:0]

9.3.22. PTP_TRX_TS_NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Address 0xE448)

Table 109. PTP_TRX_TS_NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Address 0xE448)

Bit	Name	Type	Default	Description
15:14	RSVD	RO	0	Reserved
13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosecond field [29:16]

9.3.23. PTP_TRX_TS_S_LO (PTP TxRx Timestamp Sec Low Register, Address 0xE44A)

Table 110. PTP_TRX_TS_S_LO (PTP TxRx Timestamp Sec Low Register, Address 0xE44A)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[15:0]	RW	0	Transmit/Receive timestamp second field [15:0]

9.3.24. PTP_TRX_TS_S_MI (PTP TxRx Timestamp Sec Mid Register, Address 0xE44C)

Table 111. PTP_TRX_TS_S_MID (PTP TxRx Timestamp Sec Mid Register, Address 0xE44C)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[31:16]	RW	0	Transmit/Receive timestamp second field [31:16]

9.3.25. PTP_TRX_TS_S_HI (PTP TxRx Timestamp Sec High Register, Address 0xE44E)

Table 112. PTP_TRX_TS_S_HI (PTP TxRx Timestamp Sec High Register, Address 0xE44E)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[47:32]	RW	0	Transmit/Receive timestamp sec field [47:32]

9.3.26. LOCAL_TRX_TS_NS_LO (Local TxRx Timestamp Nano-Sec Low Register, Address 0xE450)

Table 113. LOCAL_TRX_TS_NS_LO (Local TxRx Timestamp Nano-Sec Low Register, Address 0xE450)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_ns[15:0]	RO	0	Transmit/Receive timestamp nanosecond field [15:0]

9.3.27. LOCAL_TRX_TS_NS_HI (Local TxRx Timestamp Nano-Sec High Register, Address 0xE452)

Table 114. LOCAL_TRX_TS_NS_HI (Local TxRx Timestamp Nano-Sec High Register, Address 0xE452)

Bit	Name	Type	Default	Description
15:14	RSVD	RO	0	Reserved
13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosecond field [29:16]

9.3.28. LOCAL_TRX_TS_S_LO (Local TxRx Timestamp Sec Low Register, Address 0xE454)

Table 115. LOCAL_TRX_TS_S_LO (Local TxRx Timestamp Sec Low Register, Address 0xE454)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[15:0]	RW	0	Transmit/Receive timestamp second field [15:0]

9.3.29. LOCAL_TRX_TS_S_MI (Local TxRx Timestamp Sec Mid Register, Address 0xE456)

Table 116. LOCAL_TRX_TS_S_MI (Local TxRx Timestamp Sec Mid Register, Address 0xE456)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[31:16]	RW	0	Transmit/Receive timestamp second field [31:16]

9.3.30. LOCAL_TRX_TS_S_HI (Local TxRx Timestamp Sec High Register, Address 0xE458)

Table 117. LOCAL_TRX_TS_S_HI (Local TxRx Timestamp Sec High Register, Address 0xE458)

Bit	Name	Type	Default	Description
15:0	TXRX_TS_s[47:32]	RW	0	Transmit/Receive timestamp second field [47:32]

9.3.31. PTP_ETHERTYPE_CONFIG (PTP EtherType Parser Config Register, Address 0xE460)

Table 118. PTP_ETHERTYPE_CONFIG (PTP EtherType Parser Config Register, Address 0xE460)

Bit	Name	Type	Default	Description
15:2	RSVD	RO	0	Reserved
1	PTP_eth_std_en	RW	0x01	Recognize standard EtherType (0x88F7) option: 0: not recognized 1: recognized
0	PTP_eth_customize_en	RW	0	Recognize customized EtherType option: 0: not recognized 1: recognized

9.3.32. PTP_CUSTOMIZED_ETHERTYPE (PTP Customized EtherType Register, Address 0xE462)

Table 119. PTP_CUSTOMIZED_ETHERTYPE (PTP Customized EtherType Register, Address 0xE462)

Bit	Name	Type	Default	Description
15:0	PTP_customize_EtherType	RW	0	The customized EtherType value.

9.3.33. PTP_INSTANCE_0_DOMAIN_NUMBER (PTP Instance 0 Domain Number Register, Address 0xE466)

Table 120. PTP_INSTANCE_0_DOMAIN_NUMBER (PTP Instance 0 Domain Number Register, Address 0xE466)

Bit	Name	Type	Default	Description
15:9	RSVD	RO	0	Reserved
8	Timestamp_sel	RW	0x01	Select the timestamp source when offloading/insertion: 0: Use the timestamp of Local clock for 1-step operation and hardware-assisted timestamp insertion 1: Use the timestamp of PTP clock for 1-step operation and hardware-assisted timestamp insertion
7:0	Domain number	RW	0	The configured domain number for PTP instance 0.

9.4. OP Register Tables

For registers listed in this section, a special method should be used to access them. Refer to section 8.10.8.2 Special Register Access, page 74 for details.

9.4.1. OPCR1 (OP Control Register 1, Address 0xDC0C)

Table 121. OPCR1 (OP Control Register 1, Address 0xDC0C)

Bit	Name	Type	Default	Description
15:6	RSVD	RW	0	Reserved. WRITE is not allowed.
5	lwake_edge_sel	RW	0	Edge selection for local wake-up detection. 1: Falling edge detection 0: Rising edge detection
4:1	RSVD	RW	0	Reserved. WRITE is not allowed.
0	Dis_rwake	RW	0	1: Disable the remote wake up; namely the PHY cannot detect the Rwake event

9.4.2. RWCR1 (Remote Wake-Up Control Register, Address 0xDC0E)

Table 122. RWCR (Remote Wake-Up Control Register, Address 0xDC0E)

Bit	Name	Type	Default	Description
15:1	RSVD	RW	0x20	Reserved. WRITE is not allowed.
0	lwake_rwake_en	RW	0x01	1: The RTL9000BF/BN/BR/BS will remotely wake up its link partner automatically by sending the WUP on the MDI pins after the local wake up 0: The RTL9000BF/BN/BR/BS will not remotely wake up its link partner automatically by sending the WUP on the MDI pins after the local wake up

9.4.3. OPCR2 (OP Control Register 2, Address 0xDD00)

Table 123. OPCR2 (OP Control Register 2, Address 0xDD00)

Bit	Name	Type	Default	Description
15:6	RSVD	RW	Hardware Dependent	Reserved. The default values depend on hardware configuration. Used internally; WRITE is not allowed.
5	reg_HW_reset	RW, SC	0	1: Enable a Hardware reset by this register. The PHY will be reset, which means all registers will be set to default value except for the OP registers When the reset is completed, it will be self-cleared
4:0	op_cmd	RW	0	10010: Go to Standby mode 10011: Go to Normal mode* 10100: Go to Sleep mode Others: Reserved <i>*Note: To allow the PHY to go to Normal mode, op_cmd_2 should also be adopted, refer to 9.4.14.</i> The OP Go to Sleep/Normal/Standy command will be cleared in the following conditions: 1. PHY goes to the Sleep mode 2. UV event occurred in Normal/Safety mode 3. Reset event occurred in Normal/Safety mode 4. OT event occurred in Normal/Safety mode 5. Wake up event occurred in state (Option to set OPCR3 at section 9.4.4)

9.4.4. OPCR3 (OP Control Register 3, Address 0xDD02)

Table 124. OPCR3 (OP Control Register 3, Address 0xDD02)

Bit	Name	Type	Default	Description
15:7	RSVD	RW	0x1E	Reserved, Used internally; WRITE is not allowed.
6	wake_event_clr_op_cmd_valid_en	RW	0x01	1: Wake event is able to clear OP go to Sleep/Normal/Standy command Valid bit
5:0	RSVD	RW	0x21	Reserved. Used internally; WRITE is not allowed.

9.4.5. OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08)

Table 125. OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0	Reserved.
7	sleep_by_opcmd_flag	RO, RC	0	1: Transition to Sleep mode by OP go to Sleep command.
6	RSVD	RO	0	Reserved
5	sleep_by_uv_avdd33_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on AVDD33.
4	sleep_by_uv_dvdd_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD.
3	sleep_by_uv_avdd09_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on AVDD09.
2	sleep_by_uv_dvdd09_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD09.
1	sleep_by_uv_mii1_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD.
0	RSVD	RO	0	Reserved.

9.4.6. OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C)

Table 126. OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0	Reserved.
7	sleep_by_hostcmd_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by OP go to Sleep command 0: Disable the interrupt of the transition to Sleep mode by OP go to Sleep command
6	RSVD	RO	0x01	Reserved.
5	sleep_by_uv_avdd33_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on AVDD33 0: Disable the interrupt of the transition to Sleep mode by undervoltage on AVDD33
4	sleep_by_uv_dvdd_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD. 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD
3	sleep_by_uv_avdd09_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on AVDD09 0: Disable the interrupt of the transition to Sleep mode by undervoltage on AVDD09
2	sleep_by_uv_dvdd09_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD09 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD09
1	sleep_by_uv_miil_intr_en	RW	0x01	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD
0	RSVD	RO	0	Reserved.

9.4.7. OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E)

Table 127. OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0	Reserved.
7	sleep_by_cmd_intr_msk	RW	0x01	1: Transition to Sleep mode by OP go to Sleep command interrupt MASK enable
6	Reserved	RW	0x01	Reserved. Used internally; WRITE is not allowed.
5	sleep_by_uv_avdd33_intr_msk	RW	0x01	1: Transition to Sleep mode by undervoltage on AVDD33 interrupt MASK enable
4	sleep_by_uv_dvdd_intr_msk	RW	0x01	1: Transition to Sleep mode by undervoltage on DVDD interrupt MASK enable
3	sleep_by_uv_avdd09_intr_msk	RW	0x01	1: Transition to Sleep mode by undervoltage on AVDD09 interrupt MASK enable
2	sleep_by_uv_dvdd09_intr_msk	RW	0x01	1: Transition to Sleep mode by undervoltage on DVDD09 interrupt MASK enable
1	sleep_by_uv_mii1_intr_msk	RW	0x01	1: Transition to Sleep mode by undervoltage on DVDD_MII interrupt MASK enable
0	RSVD	RO	0	Reserved.

9.4.8. OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10)

Table 128. OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10)

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0	Reserved.
11	ot_flag	RO, RC	0	1: Over-temperature event occurred
10:5	RSVD	RO	0	Reserved.
4	evnt_mii1_flag	RO, RC	0x01	1: Indicates recovery of undervoltage on DVDD has occurred
3	rec_dvdd09_flag	RO, RC	0x01	1: Indicates recovery of undervoltage on DVDD09 has occurred
2	rec_avdd09_flag	RO, RC	0x01	1: Indicates recovery of undervoltage on AVDD09 has occurred
1	rec_dvdd_flag	RO, RC	0x01	1: Indicates recovery of undervoltage on DVDD has occurred
0	rec_avdd33_flag	RO, RC	0x01	1: Indicates recovery of undervoltage on AVDD33 has occurred

9.4.9. OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14)

Table 129. OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14)

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0	Reserved.
11	ot_intr_en	RW	0x01	1: Enable the OT to trigger an interrupt 0: Disable the OT to trigger an interrupt
10:5	RSVD	RO	0x20	Reserved.
4	evnt_mii1_intr_en	RW	0x01	1: Enable the UV recovery on DVDD to trigger an interrupt 0: Disable the UV recovery on DVDD to trigger an interrupt
3	rec_dvdd09_intr_en	RW	0x01	1: Enable the UV recovery on DVDD09 to trigger an interrupt 0: Disable the UV recovery on DVDD09 to trigger an interrupt
2	rec_avdd09_intr_en	RW	0x01	1: Enable the UV recovery on AVDD09 to trigger an interrupt 0: Disable the UV recovery on AVDD09 to trigger an interrupt
1	rec_dvdd_intr_en	RW	0x01	1: Enable the UV recovery on DVDD to trigger an interrupt 0: Disable the UV recovery on DVDD to trigger an interrupt
0	rec_avdd33_intr_en	RW	0x01	1: Enable the UV recovery on AVDD33 to trigger an interrupt 0: Disable the UV recovery on AVDD33 to trigger an interrupt

9.4.10. OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16)

Table 130. OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16)

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0	Reserved.
11	ot_intr_msk	RW	0x01	1: OT interrupt MASK enable
10:5	RSVD	RO	0x20	Reserved.
4	evnt_mii1_intr_msk	RW	0x01	1: UV recovery on DVDD interrupt MASK enable
3	rec_dvdd09_intr_msk	RW	0x01	1: UV recovery on DVDD09 interrupt MASK enable
2	rec_avdd09_intr_msk	RW	0x01	1: UV recovery on AVDD09 interrupt MASK enable
1	rec_dvdd_intr_msk	RW	0x01	1: UV recovery on DVDD interrupt MASK enable
0	rec_avdd33_intr_msk	RW	0x01	1: UV recovery on AVDD33 interrupt MASK enable

9.4.11. OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18)

Table 131. OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18)

Bit	Name	Type	Default	Description
15	rec_rg_rst_flag	RO, RC	0	1: Reset is active by the MDIO command
14	rec_pin_rst_flag	RO, RC	0	1: Reset is active by the PHYRSTB pin
13	RSVD	RO	0	Reserved.
12	RSVD	RO	0x01	Reserved.
11	pwon_flag	RO, RC	0x01	1: PHY is powered on by V33 (RTL9000BR/BS) PHY is powered on by AVDD33 (RTL9000BSS)
10	lwake_flag	RO, RC	0	1: PHY is woken up by local wake up This flag will be cleared if the following events occur. 1. PHY goes to the Reset or Standby from Normal mode. 2. PHY goes to the Reset or Standby from Safety mode. 3. PHY goes to the Sleep mode from any state.
9:6	RSVD	RO	0	Reserved.
5	wur_flag	RO, RC	0	1: PHY received WUR
4:1	RSVD	RO	0	Reserved.
0	rwake_flag	RO, RC	0	1: PHY is woken up by remote wake up This flag will be cleared if the following events occur. 1. PHY goes to the Reset or Standby from Normal mode. 2. PHY goes to the Reset or Standby from Safety mode. 3. PHY goes to the Sleep mode from any state

9.4.12. OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C)

Table 132. OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C)

Bit	Name	Type	Default	Description
15	rec_rg_rst_intr_en	RW	0x01	1: Enable reset by the register to trigger interrupt
14	rec_pin_rst_intr_en	RW	0x01	1: Enable reset by the pin to trigger interrupt
13:12	RSVD	RO	0	Reserved
11	pwon_intr_en	RW	0x01	1: Enable power-on event to trigger interrupt
10	lwake_intr_en	RW	0x01	1: Enable local wake up to trigger interrupt
9:6	RSVD	RO	0	Reserved.
5	wur_intr_en	RW	0x01	1: Enable wakeup request to trigger interrupt
4:1	RSVD	RO	0	Reserved.
0	rwake_intr_en	RW	0x01	1: Enable remote wake up to trigger interrupt

9.4.13. OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E)

Table 133. OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E)

Bit	Name	Type	Default	Description
15	rec_rg_rst_intr_msk	RW	0x01	1: Reset by register interrupt MASK enable
14	rec_pin_rst_intr_msk	RW	0x01	1: Reset by the PHYRSTB pin interrupt MASK enable
13:12	RSVD	RO	0	Reserved
11	pwon_intr_msk	RW	0x01	1: Power-on interrupt MASK enable
10	lwake_intr_msk	RW	0x01	1: Local wake up interrupt MASK enable
9:6	RSVD	RO	0	Reserved.
5	wur_intr_msk	RW	0x01	1: WUR interrupt MASK enable
4:1	RSVD	RO	0	Reserved.
0	rwake_intr_msk	RW	0x01	1: Remote wake up interrupt MASK enable

9.4.14. OPCR4 (OP Control Register 4, Address 0xDD20)

Table 134. OPCR4 (OP Control Register 4, Address 0xDD20)

Bit	Name	Type	Default	Description
15:5	RSVD	RO	0	Reserved.
4	wupr_tx	RW, SC	0	1: Enable WUP / WUR Request Once the WUR transmission is enabled, the transmission is about 3ms; when the transmission finishes, this bit is cleared to 0.
3:0	op_cmd_2	RW	0	1011: Go to Normal mode * Others: Reserved <i>*Note: To allow the PHY to go to Normal mode, op_cmd should be also adopted, refer to 9.4.3.</i> The OP Go to Sleep/Normal/Standy command will be cleared in the following conditions: 1. PHY goes to the Sleep mode 2. UV event occurred in Normal/Safety mode 3. Reset event occurred in Normal/Safety mode 4. OT event occurred in Normal/Safety mode 5. Wake up event occurred in any state. (Option to set OPCR3 at section 9.4.4)

9.4.15. OPCR5 (OP Control Register 5, Address 0xDC16)

Table 135. OPCR5 (OP Control Register 5, Address 0xDC16)

Bit	Name	Type	Default	Description
15:5	RSVD	RW	0x0459	Reserved. Used internally; WRITE is not allowed.
4	Lwake_detect_time	RW	0	Local wake detection time 0: 20 μs 1: At least 10ms After setting this bit, please set cfg_update bit in section 9.4.16
3:0	RSVD	RW	0x08	Reserved. Used internally; WRITE is not allowed.

9.4.16. OPCR6 (OP Control Register 6, Address 0xDC18)

Table 136. OPCR6 (OP Control Register 6, Address 0xDC18)

Bit	Name	Type	Default	Description
15:4	RSVD	RW	0x0E00	Reserved. Used internally; WRITE is not allowed.
3	Cfg_update	RW	0	To update the register operation: write this bit to 1 first then write to 0. The register in section 0 needs the above operation of this bit to take effect.
2:0	RSVD	RW	0x04	Reserved. Used internally; WRITE is not allowed.

9.5. MMD Register Tables

9.5.1. AN Control Register (Device 7, Register 0x0)

Table 137. AN Control Register (Device 7, Register 0x0)

Bit	Name	Type	Default	Description
7.0.15	AN Reset	RW, SC	0	1: AN Reset, 0: AN normal operation
7.0.14:13	RSVD	RO	0	Reserved.
7.0.12	AN enable	RW	0	1: Enable AN process If this bit is set to 1, type selection bits 1.2100.3:0 & MASTER-SLAVE bits 1.2100.14 shall have no effect on the link configuration. If this bit is cleared to 0, then bits 1.2100.3:0 & 1.2100.14 determine the link configuration regardless of the prior state of the link configuration and the AN process.
7.0.11:10	RSVD	RO	0	Reserved.
7.0.9	Restart AN	RW, SC	0	1: Restart AN process 0: AN in process, disabled, or not supported
7.0.8:0	RSVD	RO	0	Reserved.

9.5.2. AN Status Register (Device 7, Register 0x1)

Table 138. AN Status Register (Device 7, Register 0x1)

Bit	Name	Type	Default	Description
7.1.15:7	RSVD	RO	0	Reserved.
7.1.6	Page received	RO, LH	0	1: A page has been received 0: A page has not received
7.1.5	AN complete	RO	0	1: AN process completed 0: AN process not completed
7.1.4	Remote Fault	RO, LH	0	1: Remote fault condition detected 0: No remote fault condition detected
7.1.3	AN ability	RO	0x01	1: PHY is able to perform AN 0: PHY is not able to perform AN
7.1.2	Link status	RO, LL	0	1: Link is up 0: Link is down
7.1.1	RSVD	RO	0	Reserved.
7.1.0	LP AN ability	RO	0	1: LP is able to perform AN 0: LP is not able to perform AN

9.5.3. BASE-T1 AN Control Register (Device 7, Register 0x0200)

Table 139. BASE-T1 AN Control Register (Device 7, Register 0x0200)

Bit	Name	Type	Default	Description
7.512.15	AN Reset	RW, SC	0	1: AN Reset, 0: AN normal operation
7.512.14:13	RSVD	RO	0	Reserved.
7.512.12	AN enable	RW	0	1: Enable AN process If this bit is set to 1, type selection bits 1.2100.3:0 & MASTER-SLAVE bits 1.2100.14 shall have no effect on the link configuration. If this bit is cleared to 0, then bits 1.2100.3:0 & 1.2100.14 determine the link configuration regardless of the prior state of the link configuration and the AN process.
7.512.11:10	RSVD	RO	0	Reserved.
7.512.9	Restart AN	RW, SC	0	1: Restart AN process 0: AN in process, disabled, or not support
7.512.8:0	RSVD	RO	0	Reserved.

9.5.4. BASE-T1 AN Status Register (Device 7, Register 0x0201)

Table 140. BASE-T1 AN Status Register (Device 7, Register 0x0201)

Bit	Name	Type	Default	Description
7.513.15:7	RSVD	RO	0	Reserved.
7.513.6	Page received	RO, LH	0	1: A page has been received 0: A page has not received
7.513.5	AN complete	RO	0	1: AN process completed 0: AN process not completed

Bit	Name	Type	Default	Description
7.513.4	Remote Fault	RO, LH	0	1: Remote fault condition detected 0: No remote fault condition detected
7.513.3	AN ability	RO	0x01	1: PHY is able to perform AN 0: PHY is not able to perform AN
7.513.2	Link status	RO, LL	0	1: Link is up 0: Link is down
7.513.1:0	RSVD	RO	0	Reserved.

9.5.5. BASE-T1 AN Advertisement Register 1 (Device 7, Register 0x0202)

Table 141. BASE-T1 AN Advertisement Register 1 (Device 7, Register 0x0202)

Bit	Name	Type	Default	Description
7.514.15	Next Page	RW	0	0: Device does not have any Next Page to send 1: Device wishes to engage in Next Page exchange
7.514.14	RSVD	RO	0	Reserved
7.514.13	Remote Fault	RW	0	0: Do not set the remote fault bit 1: Set the remote fault bit
7.514.12	Force MASTER-SLAVE	RW	0	0: Device is in preferred mode 1: Device is in the force mode
7.514.11:10	Pause Ability	RW	0	Pause capability advertisement. Refer to IEEE802.3bp, 98.2.1.2.
7.514.9:5	EchoedNonce field	RO	0	Pause capability advertisement. Refer to IEEE802.3bp, 98.2.1.2. Controlled by the Auto-negotiation state machine.
7.514.4:0	Selector field	RW	0x01	00001: 802.3

9.5.6. BASE-T1 AN Advertisement Register 2 (Device 7, Register 0x0203)

Table 142. BASE-T1 AN advertisement Register 2 (Device 7, Register 0x0203)

Bit	Name	Type	Default	Description
7.515.15:6	D31_D22	RW	0	Reserved. Used internally; WRITE is not allowed.
7.515.5	D21	RW	0	Reserved. Used internally; WRITE is not allowed.
7.515.4	D20	RW	Varies	Reserved. Used internally; WRITE is not allowed.
7.515.3:0	D19_D16	RO	0	Reserved.

9.5.7. BASE-T1 AN Advertisement Register 3 (Device 7, Register 0x0204)

Table 143. BASE-T1 AN Advertisement Register 3 (Device 7, Register 0x0204)

Bit	Name	Type	Default	Description
7.516.15:0	D47_D32	RW	0	D47: D32, refer to IEEE802.3bp, 98.2.1.2.

9.5.8. BASE-T1 AN LP Base Page Ability Register 1 (Device 7, Register 0x0205)

Table 144. BASE-T1 AN LP Base Page Ability Register 1 (Device 7, Register 0x0205)

Bit	Name	Type	Default	Description
7.517.15:0	D15_D0	RO	0	D15: D0, refer to IEEE802.3bp, 98.2.1.2.

9.5.9. BASE-T1 AN LP Base Page Ability Register 2 (Device 7, Register 0x0206)

Table 145. BASE-T1 AN LP Base Page Ability Register 2 (Device 7, Register 0x0206)

Bit	Name	Type	Default	Description
7.518.15:0	D31_D16	RO	0	D31: D16, refer to IEEE802.3bp, 98.2.1.2.

9.5.10. BASE-T1 AN LP Base Page Ability Register 3 (Device 7, Register 0x0207)

Table 146. BASE-T1 AN LP Base Page Ability Register 3 (Device 7, Register 0x0207)

Bit	Name	Type	Default	Description
7.519.15:0	D47_D32	RO	0	D47: D32, refer to IEEE802.3bp, 98.2.1.2.

9.5.11. BASE-T1 AN Next Page Transmit Register 1 (Device 7, Register 0x0208)

Table 147. BASE-T1 AN Next Page Transmit Register 1 (Device 7, Register 0x0208)

Bit	Name	Type	Default	Description
7.520.15	Next Page	RW	0	0: Next page transmission ends 1: Have more pages to transmit
7.520.14	RSVD	RO	0	Reserved.
7.520.13	Message page	RW	0	0: Unformatted page 1: Message page
7.520.12	Acknowledge 2	RW	0	0: Cannot comply with message 1: Will comply with message
7.520.11	Toggle	RO	0	0: Previous value of the transmitted link codeword is 1 1: Previous value of the transmitted link codeword is 0
7.520.10:0	Message/Unformatted code field	RW	0	Message/Unformatted code field, refer to IEEE 802.3bp, 98.2.4.3.1.

9.5.12. BASE-T1 AN Next Page Transmit Register 2 (Device 7, Register 0x0209)

Table 148. BASE-T1 AN Next Page Transmit Register 2 (Device 7, Register 0x0209)

Bit	Name	Type	Default	Description
7.521.15:0	Unformatted code field 1	RW	0	Unformatted code field 1, refer to IEEE 802.3bp, 98.2.4.3.1.

9.5.13. BASE-T1 AN Next Page Transmit Register 3 (Device 7, Register 0x020A)

Table 149. BASE-T1 AN Next Page Transmit Register 3 (Device 7, Register 0x020A)

Bit	Name	Type	Default	Description
7.522.15:0	Unformatted code field 2	RW	0	Unformatted code field 2, refer to IEEE 802.3bp, 98.2.4.3.1.

9.5.14. BASE-T1 AN LP Next Page Transmit Register 1 (Device 7, Register 0x020B)

Table 150. BASE-T1 AN LP Next Page Transmit Register 1 (Device 7, Register 0x020B)

Bit	Name	Type	Default	Description
7.523.15	Next Page	RO	0	0: Next page transmission ends 1: More pages to transmit
7.523.14	RSVD	RO	0	Reserved.
7.523.13	Message page	RO	0	0: Unformatted page 1: Message page
7.523.12	Acknowledge 2	RO	0	0: Cannot comply with message 1: Will comply with message
7.523.11	Toggle	RO	0	0: Previous value of the transmitted link codeword is 1 1: Previous value of the transmitted link codeword is 0
7.523.10:0	Message/Unformatted code field	RO	0	Message/Unformatted code field, refer to IEEE 802.3bp, 98.2.4.3.1.

9.5.15. BASE-T1 AN LP Next Page Transmit Register 2 (Device 7, Register 0x020C)

Table 151. BASE-T1 AN LP Next Page Transmit Register 2 (Device 7, Register 0x020C)

Bit	Name	Type	Default	Description
7.524.15:0	Unformatted code field 1	RO	0	Unformatted code field 1, refer to IEEE 802.3bp, 98.2.4.3.1.

9.5.16. BASE-T1 AN LP Next Page Transmit Register 3 (Device 7, Register 0x020D)

Table 152. BASE-T1 AN LP Next Page Transmit Register 3 (Device 7, Register 0x020D)

Bit	Name	Type	Default	Description
7.525.15:0	Unformatted code field 2	RO	0	Unformatted code field 2, refer to IEEE 802.3bp, 98.2.4.3.1.

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10. Power Sequence and Regulators

The RTL9000BF/BN/BR/BS/BSS incorporates linear Low-Dropout Regulators (LDO) that features high power supply ripple rejection and low output noise. Power inductors are not needed for the RTL9000BF/BN/BR/BS/BSS; only an output capacitor is required between the 0.9V outputs and the analog ground for phase compensation, which reduces cost and PCB real estate. Note that the output of the LDO cannot be provided as a power source to other devices.

Use an X5R/X7R low-ESR ceramic capacitor, with capacitance of at least $0.1\mu F$, to enhance the stability of output voltage. The bypass capacitors should be placed as close as possible to power pins (AVDD09 and DVDD09) for adequate filtering.

The RTL9000BF/BN/BR supports 3.3V/2.5V/1.8V I/O voltage of the MII/RMII/RGMII interface. When using 3.3V as the power source, it must be provided by an external power source for RTL9000BF/BN/BR/BS/BSS. For 1.8V/2.5V I/O voltage, the RTL9000BF/BN/BR supports voltage from internal or external LDO while RTL9000BS/BSS only supports voltage from an external LDO. Table 47. ISR (I/O Power Select Register, Page 0xA4C, Reg 0x12) shows the parameter setting for I/O Power selection when using different power sources.

10.1. Power Sequence

Figure 67 show the power-on sequence of different power domains and the corresponding Operating Modes (refer to section 8.4). As shown, the PHY goes to reset mode first and waits for 0.9V ready and core logic ready, and then goes to Normal or Standby mode depending on the hardware configuration of the ST_CHG pin.

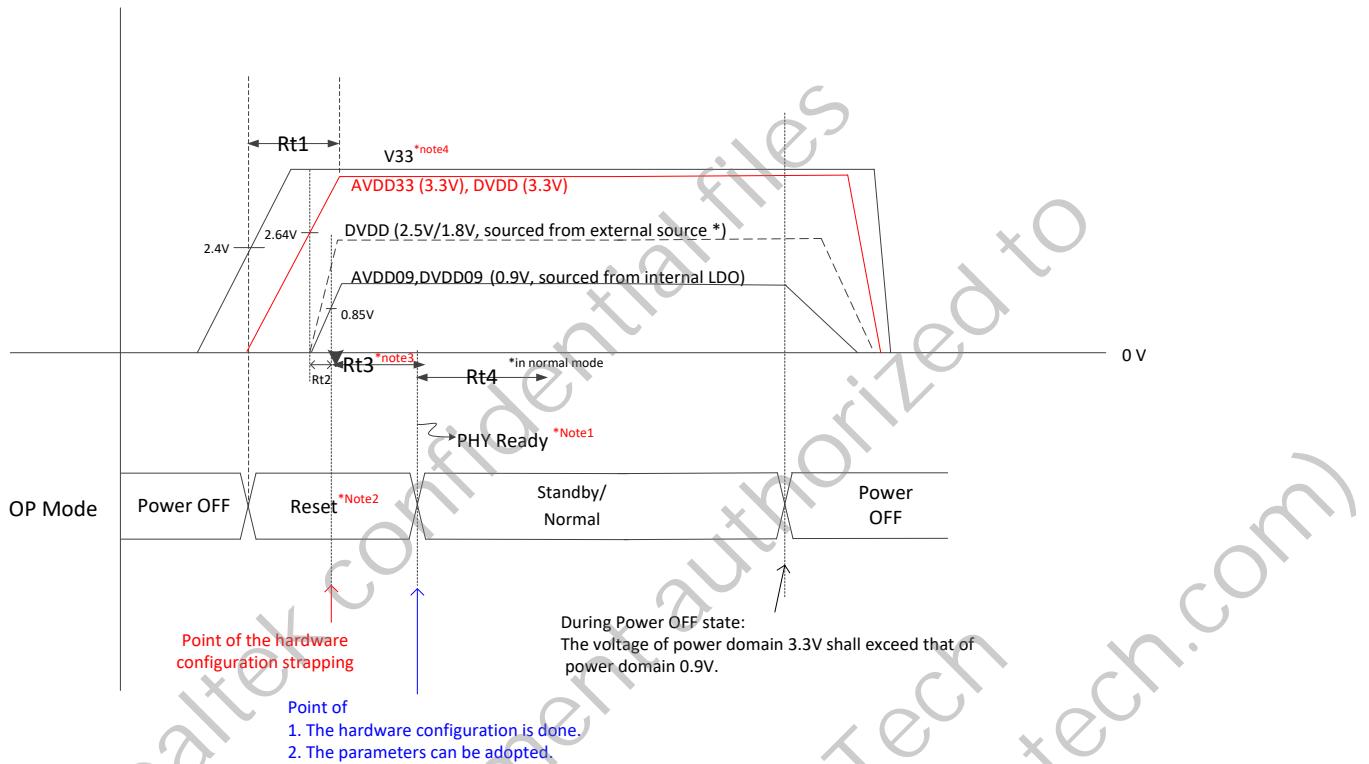


Figure 67. RTL9000BF/BN/BR/BS/BSS Power Sequence

Note 1: The PHY should be confirmed to be in PHY Ready State after the first power-on and after each hardware reset (refer to section 10.2) by polling the value of PHY Status Sub-flag Register, Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3 to make sure PHY is ready. If not use the way of the polling the register, wait for at least 4ms and then checking the value of PHY Status Sub-flag Register, Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3.

Note 2: On first time power-on, PHY will have some initialization in the Reset mode.

Note 3: The hardware configuration will be done before the end of Rt3; if the user wants to use the external I/O to do the hardware strapping configuration, the desired pull up/down I/O signal should be ready at the beginning of Rt3 and be kept during the whole duration of Rt3.

Note 4: Please note the RTL9000BSS/BN has no V33 pin.

Note 5: The order for Powering-On is $V33 \geq AVDD33/VDD33 \geq DVDD \geq AVDD09/DVDD09$. The order for Powering-Off is $AVDD09/DVDD09 > DVDD \geq AVDD33/VDD33 \geq V33$.

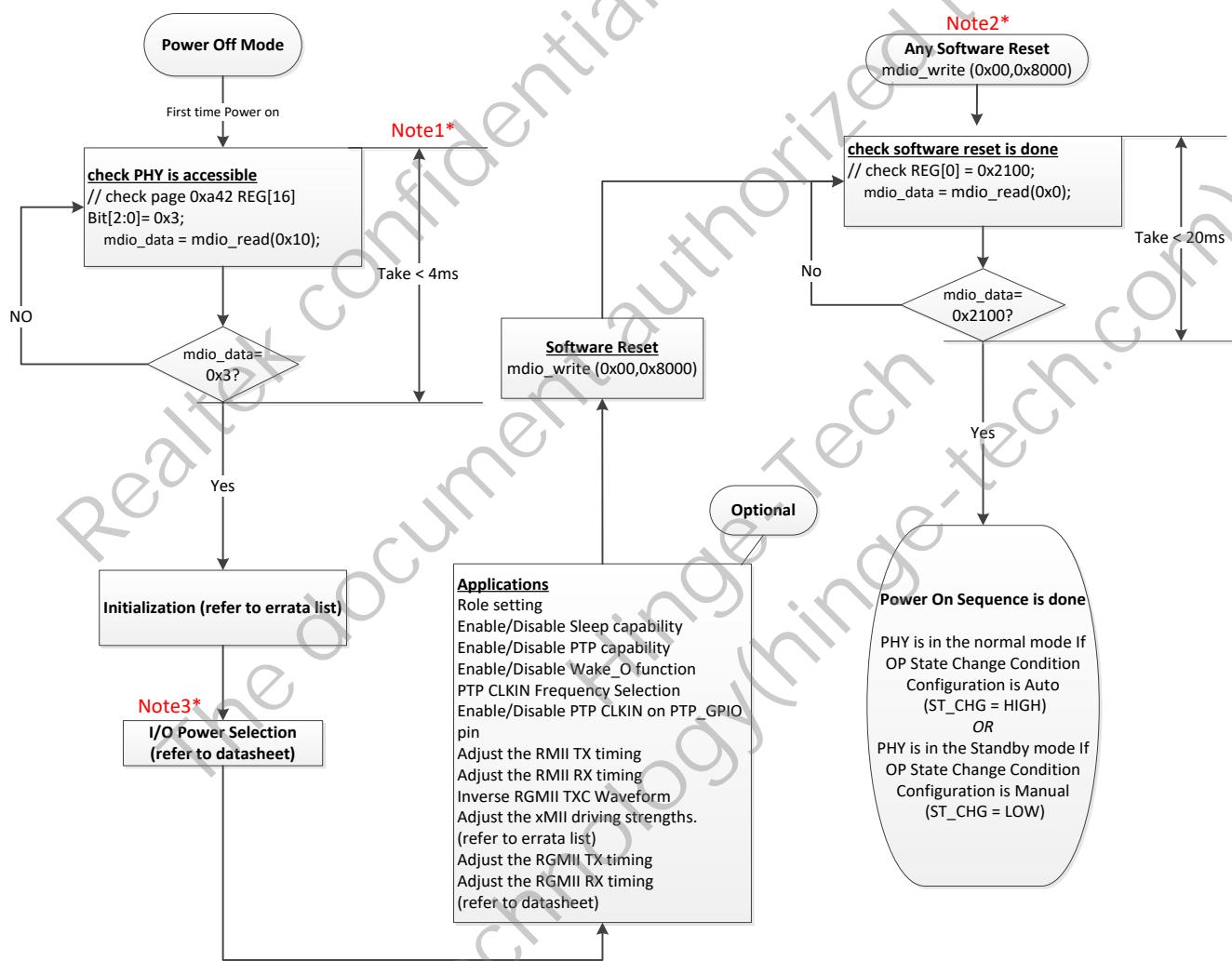
Note 6: Please make sure of the order for Powering-Off, as if the 3.3V falls lower than 0.9V, it will cause the IC to enter unknown status and this may risk cause damage to the IC.

Note 7: The user needs to maintain the relative relationship between 3.3V and 0.9V which means the 3.3V cannot fall lower than 0.9V when doing the power-off sequence.

Table 153. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.15	-	100	ms
Rt2	3.3V ready to 0.9V ready time	-	100	-	μs
Rt3	Core Logic Ready Time	-	-	4	ms
Rt4	Link-up time	-	-	100	ms

*Note: The external power for I/O must be given before Rt2.

Power-On Patch and Control Flow for RTL9000BF/BN/BR/BS/BSS

Figure 68. Power-On Patch and Control Flow

Note 1: The PHY should be confirmed to be in PHY Ready State after the first power-on and after every hardware reset (refer to section 10.2) by polling the value of PHY Status Sub-flag Register; Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3 to make

sure the PHY is ready. If not, use the polling the register method, wait for at least 4ms and then check that the value of PHY Status Sub-flag Register, Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3.

Note 2: For software reset details refer to section 10.2. When a software reset is done, poll the value of Reg 0x00 until it is equal to 0x2100, or wait for at least 20ms before accessing the other registers of the PHY.

Note 3: The external power must be ready before I/O power selection if DVDD I/O power is supplied by it.

Figure 68 shows the power-on control and control flow for the RTL9000BF/BN/BR/BS/BSS. Note the timing for adopting I/O power selection (Section 9.2.22) and adopting the patch code (if necessary).

Regarding the power off sequence, if DVDD is 2.5V or 1.8V, the power off sequence should be power off DVDD first, then AVDD33, and then V33.

10.2. Reset

The RTL9000BF/BN/BR/BS/BSS implements two methods to reset the chip:

Hardware Reset

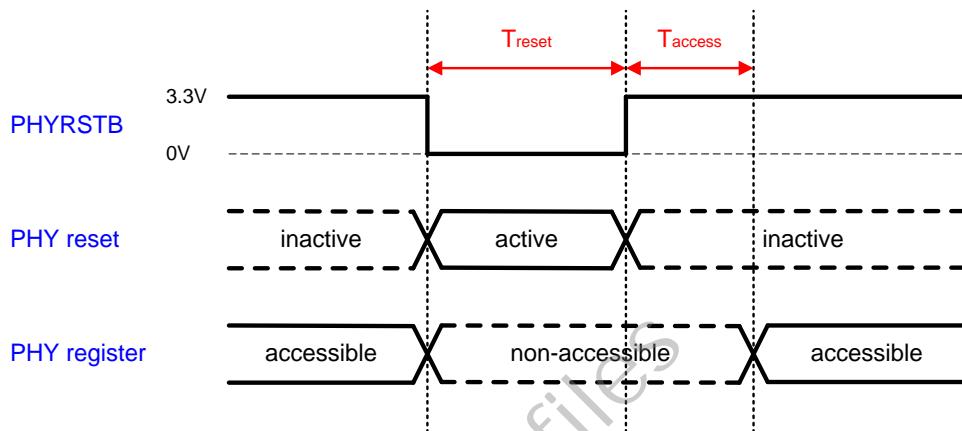
The RTL9000BF/BN/BR/BS/BSS has a PHYRSTB pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (as shown in Figure 69) to return to a pre-defined reset state. After the de-assertion of PHYRSTB, wait for at least 4ms (for internal circuits setting time; see Figure 69).

Users can also set the bit [5] at address 0xDD00 (section 9.4.3) to 1. The Hardware reset triggered by this register is equal to asserting the PHYRSTB pin low for 10ms. I.e., setting reg_HW_RST to 1 requires a waiting period of at least 4ms for internal circuits setting.

The PHY should be confirmed to be in PHY Ready state after the first power-on and after every hardware reset. Polling the value of PHY Status Sub-flag Register, Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3 to make sure PHY is accessible. If not use the polling the register method. Check that the value of PHY Status Sub-flag Register, Page 0xA42, Reg 0x10, bit [2:0], is equal to 0x3 after the 4ms for internal circuits setting.

All registers except for OP registers (section 9.4) will return to default values after a hardware reset. I.e., all of the parameters, for example, the parameter setting in users' desired initial parameter setting and etc., should be adopted again after a Hardware Reset. A Hardware Reset is regarded as a power-on event and the Hardware Configuration will be re-done again.

When asserting the PHYRSTB to low, the PHY enters ‘Reset mode’ (refer to section 8.4). In cases where the upper layer may have incorrect configuration of the PHY, and the user wants all of the registers except for OP registers of the PHY back to the default values before re-configuration, a Hardware reset is recommended.


Figure 69. PHY Reset Timing
Table 154. PHY Reset Signal Timing Parameter

Symbol	Parameter	Min	Max	Units
T _{reset}	PHY reset active time	10	-	ms
T _{access}	Timing from PHYRSTB de-asserted to access PHY registers	-	4	ms

Software Reset

Use the BMCR reset command at Reg 0x00, bit[15] = 1, see 9.2.1, to reset the chip. When a software reset is done, poll the value of Reg 0x00 until it is equal to 0x2100, or wait for at least 20ms before accessing the other registers of the PHY.

A Software Reset is applied to allow some register settings to take effect, for example, Master/Slave setting (Register 0x9, bit[11]), sleep capability (page 0xA5A, Register 0x14, bit [0]), PTP function enable (Address 0xE400, bit[0]), Enable PTP CLKIN function at PTP_GPIO pin (address0xE410, bit[4]) and PTP CLKIN Frequency Select (address0xE410, bit[5]) and etc.. A Software Reset can also be used to start a relink flow.

Table 155. Functions Requiring Issue of a Software Reset

Register	Description
Reg 0x9, bit [11]	Role setting
Page 0xA5A, Reg 0x14 bit [0]	Enable/Disable Sleep capability
Address 0xE400, bit [0]	Enable/Disable PTP capability
Address 0xE410, bit [6:5]	PTP CLKIN Frequency Selection
Address 0xE410, bit [4]	Enable/Disable PTP CLKIN on PTP_GPIO pin
Address 0xD050, bit [12:9]	Adjust the RMII TX timing
Address 0xD050, bit [8:5]	Adjust the RMII RX timing
Address 0xD082, bit [10]	Inverse RGMII TXC Waveform
Address 0xD082, bit [9:8]	Adjust the RGMII TX timing
Address 0xD082, bit [3:0]	Adjust the RGMII RX timing

11. Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 156. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V33	Supply Voltage 3.3V	-0.3	3.63	V
AVDD33, DVDD	Supply Voltage 3.3V	-0.3	3.63	V
AVDD09, DVDD09	Supply Voltage 0.9V	-0.3	0.99	V
MDIP, MDIN	Voltage on pins MDIP, MDIN	-0.3	3.63	V
INH	Voltage on pin INH	-0.3	V33+0.3V	V
WAKE	Voltage on pin WAKE	-0.3	V33+0.3V	V
XTAL_IN, XTAL_OUT	Voltage on pins XTAL_IN, XTAL_OUT	-0.3	3.63	V
RXD[3:0], RXDV, RXER, INTB	Voltage on digital output pins (configured as 3.3V I/O)	-0.3	3.63	V
	Voltage on digital output pins (configured as 2.5V I/O)	-0.3	2.8	V
	Voltage on digital output pins (configured as 1.8V I/O)	-0.3	2.3	V
Other Pins	Voltage on other pins	-0.3	5.25	V
T _{STG}	Storage temperature	-55	150	°C

Note 1: Refer to the most updated schematic circuit for correct configuration.

11.2. Recommended Operating Conditions

Table 157. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage 3.3V	V33	3.14	3.3	3.46	V
Supply Voltage 3.3V	AVDD33	3.14	3.3	3.46	V
Supply Voltage 0.9V	AVDD09, DVDD09	0.855	0.9	0.945	V
Supply Voltage I/O Power (configured as 3.3V I/O)	DVDD	3.14	3.3	3.46	V
Supply Voltage I/O Power (configured as 2.5V I/O)	DVDD	2.38	2.5	2.63	V
Supply Voltage I/O Power (configured as 1.8V I/O)	DVDD	1.71	1.8	1.89	V
Ambient Operating Temperature, T _{AMB}	-	-40	-	125	°C

Note: Note that the power rising slope should be monotonic. As for the maximum voltage ripple, the ripple and noise on 3.3V domain should be within 66mVpp (+/-1% 3.3V), within 30mVpp (+/-1.67% 0.9V) on 0.9V domain, and the DVDD should be within +/-2% DVDD. Plus the DC inaccuracy, the summation of the power variation cannot exceed +/-5%.

11.3. Thermal Characteristics

Table 158. Thermal Characteristics – JEDEC PCB 4L (QFN48)

Symbol	Parameter	Min	Typ.	Max	Unit
$R_{th(j-a)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	32.83	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to case)	-	13.90	-	$^\circ\text{C}/\text{W}$
$R_{th(j-a)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	28.28	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to case)	-	13.90	-	$^\circ\text{C}/\text{W}$

Table 159. Thermal Characteristics – JEDEC PCB 4L (QFN32)

Symbol	Parameter	Min	Typ.	Max	Unit
$R_{th(j-a)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	39.39	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to case)	-	20.44	-	$^\circ\text{C}/\text{W}$
$R_{th(j-a)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	34.92	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to case)	-	20.44	-	$^\circ\text{C}/\text{W}$

Table 160. Thermal Characteristics – JEDEC PCB 4L (QFN24)

Symbol	Parameter	Min	Typ.	Max	Unit
$R_{th(j-a)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	50.59	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 25^\circ\text{C}$)	Thermal Resistance (junction to case)	-	25.87	-	$^\circ\text{C}/\text{W}$
$R_{th(j-a)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to ambient)	-	45.85	-	$^\circ\text{C}/\text{W}$
$R_{th(j-c)}$ ($T_a = 125^\circ\text{C}$)	Thermal Resistance (junction to case)	-	25.87	-	$^\circ\text{C}/\text{W}$

11.4. Power Dissipation

The following data was measured under temperatures from 25°C to 125°C . V33 voltage is from 3.3V to 3.47V, AVDD33 voltage is from 3.3V to 3.47V, AVDD09 voltage is from 0.9V to 0.945V, DVDD09 voltage is from 0.9V to 0.945V, and DVDD voltage is from 3.3V to 3.47V.

Table 161. RTL9000BF(xMII)/BR/BN Power Dissipation

Power Pin	Minimum	Typical	Maximum	Unit
Normal Mode (Traffic)				
V33	-	0.6	2.5	mA
AVDD33	-	18	21	mA
DVDD	-	7	10	mA
DVDD09	-	10	24	mA
Standby Mode				
V33	-	0.5	2.5	mA
AVDD33	-	4	6	mA
DVDD	-	3.5	4.5	mA
DVDD09	-	7	21	mA

Power Pin	Minimum	Typical	Maximum	Unit
Reset Mode				
V33	-	0.5	2.5	mA
AVDD33	-	2	3	mA
DVDD	-	0.5	1	mA
DVDD09	-	1.3	17	mA
Deep Sleep Mode				
V33	-	8	15	µA
AVDD33	-	0	-	mA
DVDD	-	0	-	mA
DVDD09	-	0	-	mA

Table 162. RTL9000BF(SGMII)/BS/BSS Power Dissipation

Power Pin	Minimum	Typical	Maximum	Unit
Normal Mode (Traffic)				
V33	-	0.6	2.5	mA
AVDD33	-	21	23	mA
DVDD	-	1.4	2	mA
AVDD09	-	15	18	mA
DVDD09	-	15	28	mA
Standby Mode				
V33	-	0.5	2.5	mA
AVDD33	-	7	9	mA
DVDD	-	1.4	2	mA
AVDD09	-	15	18	mA
DVDD09	-	12	25	mA
Reset Mode				
V33	-	0.5	2.5	mA
AVDD33	-	2	3	mA
DVDD	-	0.5	1	mA
AVDD09	-	0	0	mA
DVDD09	-	1.3	17	mA
Lite Sleep Mode				
V33	-	8	15	µA
AVDD33	-	0	-	mA
DVDD	-	0	-	mA
AVDD09	-	0	-	mA
DVDD09	-	0	-	mA

11.5. DC Characteristics

Table 163. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Pin V33						
V _{uvd_V33}	Under voltage detection voltage on V33 pin	-	-	2.4	-	V
V _{uvr_V33}	Under voltage recovery voltage on V33 pin	-	-	2.4	-	V
Pin AVDD33						
V _{uvd_AVDD33}	Undervoltage detection voltage on AVDD33 pin	-	-	3.03	-	V
V _{uvr_AVDD33}	Undervoltage recovery voltage on AVDD33 pin	-	-	3.06	-	V
V _{uvhys_AVDD33}	Undervoltage hysteresis voltage on AVDD33 pin	-	-	30	-	mV
T _{uvd_AVDD33}	Undervoltage detection time	-	-	12	-	μs
T _{uvr_AVDD33}	Undervoltage recovery time	-	-	12	-	μs
T _{tout_AVDD33}	Undervoltage timeout to Sleep	-	-	100	-	ms
Pin DVDD (if DVDD is applied by 3.3V)						
V _{uvd_DVDD}	Under voltage detection voltage on DVDD pin	-	-	3.03	-	V
V _{uvr_DVDD}	Under voltage recovery voltage on DVDD pin	-	-	3.06	-	V
V _{uvhys_DVDD}	Under voltage hysteresis voltage on DVDD pin	-	-	30	-	mV
T _{uvd_DVDD}	Under voltage detection time	-	-	8	-	μs
T _{uvr_DVDD}	Under voltage recovery time	-	-	8	-	μs
T _{tout_DVDD}	Under voltage timeout to Sleep	-	-	100	-	ms
Pin DVDD (if DVDD is applied by 2.5V)						
V _{uvd_DVDD}	Under voltage detection voltage on DVDD pin	-	-	2.30	-	V
V _{uvr_DVDD}	Under voltage recovery voltage on DVDD pin	-	-	2.32	-	V
V _{uvhys_DVDD}	Under voltage hysteresis voltage on DVDD pin	-	-	20	-	mV
T _{uvd_DVDD}	Under voltage detection time	-	-	8	-	μs
T _{uvr_DVDD}	Under voltage recovery time	-	-	8	-	μs
T _{tout_DVDD}	Under voltage timeout to Sleep	-	-	100	-	ms
Pin DVDD (if DVDD is applied by 1.8V)						
V _{uvd_DVDD}	Under voltage detection voltage on DVDD pin	-	-	1.65	-	V
V _{uvr_DVDD}	Under voltage recovery voltage on DVDD pin	-	-	1.67	-	V
V _{uvhys_DVDD}	Under voltage hysteresis voltage on DVDD pin	-	-	20	-	mV
T _{uvd_DVDD}	Under voltage detection time	-	-	8	-	μs

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T _{uvr_DVDD}	Under voltage recovery time	-	-	8	-	μs
T _{tout_DVDD}	Under voltage timeout to Sleep	-	-	100	-	ms
Pin AVDD09, Pin DVDD09						
V _{uvd_AVDD09}	Under voltage detection voltage on AVDD09 pin and DVDD09 pin	-	-	0.82	-	V
V _{uvr_AVDD09}	Under voltage recovery voltage on AVDD09 pin and DVDD09 pin	-	-	0.85	-	V
V _{uvphys_AVDD09}	Under voltage hysteresis voltage on AVDD09 pin and DVDD09 pin	-	-	30	-	mV
T _{uvd_AVDD09}	Under voltage detection time on AVDD09 pin and DVDD09 pin	-	-	8	-	μs
T _{uvr_AVDD09}	Under voltage recovery time on AVDD09 pin and DVDD09 pin	-	-	8	-	μs
T _{tout_AVDD09}	Under voltage timeout to Sleep on AVDD09 pin and DVDD09 pin	-	-	100	-	ms
Pin INH						
V _{OH_INH}	HIGH-level output voltage	I _{OH} = -400uA V33 = 3.3V	V33 -0.3	-	V33	V
V _{OL_INH}	LOW-level output voltage	I _{OH} = -5mA V33 = 3.3V	V33 -2	-	V33	V
I _{leakage}	Leakage current	Power off	-	-	4	μA
Pin WAKE						
V _{IH_WAKE}	HIGH-level input voltage	Sleep mode	1.20	-	2.55	V
V _{IL_WAKE}	LOW-level input voltage	Sleep mode	0.55	-	1.07	V
T _{det_WAKE}	Local WAKE event detection time	Sleep mode	10	-	40	μs
T _{det_rWAKE}	Remote WAKE event detection time	Through MDIP and MDIN	-	-	2	ms
Pin XTAL_IN						
V _{IH_XTAL_IN}	HIGH-level input voltage	-	1.4	-	-	V
V _{IL_XTAL_IN}	LOW-level input voltage	-	-	-	0.4	V
C _i	Input capacitance	Pin XTAL_IN, XTAL_OUT	-	2.5	-	pF
g _{m(DC)}	DC transconductance	Xtal_driving ^{Note3} is 00	10	-	-	mA/V
Pins PHYRSTB, DISB						
V _{DET}	Detection time	-	-	24	-	μs
R _{pu}	pull-up resistance(1.8V)	-	112	179	286	kohm
	pull-up resistance(2.5V)	-	74	113	182	kohm
	pull-up resistance(3.3V)	-	57	84	134	kohm
R _{pd}	pull-down resistance(1.8V)	-	52	82	154	kohm
	pull-down resistance(2.5V)	-	105	193	381	kohm
	pull-down resistance(3.3V)	-	67	113	221	kohm
Pins RXD0-3, RXDV, RXER						
R _{pu}	pull-up resistance(1.8V)	-	112	179	286	kohm
	pull-up resistance(2.5V)	-	74	113	182	kohm

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R _{pd}	pull-up resistance(3.3V)	-	57	84	134	kohm
	pull-down resistance(1.8V)	-	52	82	154	kohm
	pull-down resistance(2.5V)	-	105	193	381	kohm
	pull-down resistance(3.3V)	-	67	113	221	kohm
Pin MDIO						
R _{pu}	pull-up resistance(1.8V)	-	112	179	286	kohm
	pull-up resistance(2.5V)	-	74	113	182	kohm
	pull-up resistance(3.3V)	-	57	84	134	kohm
Pins MDIP and MDIN						
Z _{O_MDI}	Output impedance	Normal mode	40	50	60	Ω
Transmitter Test Results						
V _{pos_droop}	Positive droop; droop voltage to peak voltage ratio	IEEE 802.3bw Test mode 1; Transmit droop test mode	-	-	45	%
V _{neg_droop}	Negative droop; droop voltage to peak voltage ratio	IEEE 802.3bw Test mode 1; Transmit droop test mode	-45	-	-	%
T _{m_jit}	RMS jitter time; Master mode	IEEE 802.3bw Test mode 2; Transmit jitter test in MASTER mode	-	-	50	ps
T _{s_jit}	RMS jitter time; Slave mode	RMS jitter time; Slave mode with Link	-	-	150	ps
T _f	Transmit Clock Frequency	IEEE 802.3bw Test mode 2; Transmit jitter test in MASTER mode	66.66-100ppm	66.66	66.66+100ppm	MHz
V _{dis}	Peak distortion voltage	IEEE 802.3bw Test mode 4; Transmit distortion test	-	-	15	mV
PSDM	Power Spectral Density Mask	IEEE 802.3bw Test mode 5; Normal operation at full power (for the PSD mask)	-	-	-	dBm
		f = 1 MHz	-30.9	-	-23.3	
		f = 20 MHz	-35.8	-	-24.8	
		f = 40 MHz	-49.2	-	-28.5	
		f = 57 to 200 MHz	-	-	-36.5	

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{pdo}	Transmitter Peak Differential Output	IEEE 802.3bw Test mode 5	-	-	2.2	V

Note 1: Pins not mentioned above remain at 3.3V.

Note 2: Positive currents flow into the chip.

Note 3: Refer to section 9.2.31 for Xtal_driving.

11.6. Digital IO Characteristics

Table 164. Digital IO Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Input Current	I _{in}	-	0	-	100	μA
Leakage Current	I _L	Power off; V _{IO} = 3.3V	-	0	2.5	μA
HIGH-level input voltage	V _{IH}	Power Supply for Digital IO=3.3V	2.0	-	DVDD33+0.3	V
LOW-level input voltage	V _{IL}	Power Supply for Digital IO=3.3V	-0.3	-	0.8	V
HIGH-level output voltage	V _{OH}	Power Supply for Digital IO=3.3V; I _{OH} = 8mA	2.4	-	-	V
LOW-level output voltage	V _{OL}	Power Supply for Digital IO=3.3V; I _{OL} = 8mA	-	-	0.4	V
HIGH-level input voltage	V _{IH}	Power Supply for Digital IO=2.5V	1.7	-	DVDD25+0.3	V
LOW-level input voltage	V _{IL}	Power Supply for Digital IO=2.5V	-0.3	-	0.7	V
HIGH-level output voltage	V _{OH}	Power Supply for Digital IO=2.5V; I _{OH} = 4mA	2.0	-	-	V
LOW-level output voltage	V _{OL}	Power Supply for Digital IO=2.5V; I _{OL} = 4mA	-	-	0.4	V
HIGH-level input voltage	V _{IH}	Power Supply for Digital IO=1.8V	1.2	-	DVDD18+0.3	V
LOW-level input voltage	V _{IL}	Power Supply for Digital IO=1.8V	-0.3	-	0.5	V
HIGH-level output voltage	V _{OH}	Power Supply for Digital IO=1.8V; I _{OH} = 2mA	0.9*VDD18	-	-	V
LOW-level output voltage	V _{OL}	Power Supply for Digital IO=1.8V; I _{OL} = 2mA	-	-	0.1*DVDD18	V

Note: Digital IO pins include MDC, MDIO, INTB, PHYRSTB, DISB, LED/PTP_GPIO, TXC, TXEN, TXD[3:0], RXC, RXDV, RXER, RXD[3:0]

11.7. Over Temperature Protection

Table 165. Over Temperature Protection

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T _{otp_det}	Over temperature protection detection junction temperature	-	141	145	149	°C
T _{otp_rec}	Over temperature protection recovery junction temperature	-	131	135	139	°C
T _{otp_hys}	Over temperature protection hysteresis temperature	-	-	10	-	°C

11.8. ESD

The ESD tolerances of the RTL9000BF/BN/BR/BS/BSS are listed in Table 166.

Table 166. RTL9000BF/BN/BR/BS/BSS ESD Criteria

Feature Description		Value	Comment
HBM – All pins		±6kV	-
CDM – All pins		±750V	-
Open Alliance-Un-powered/Powered ESD	Contact discharge: E-Gun - MDIP, MDIN	±6kV	The test method references the Open Alliance EMC test. (IEEE 100BASE-T1 EMC Test Specification for Transceivers ver.1.0)
Latch Up	Power: 1.5*VDD; I: 100mA		-

11.9. Crystal Requirements

Table 167. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F _{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F _{ref} Tolerance ^{[2][3]}	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T _a = -40°C~125°C.	-100	-	+100	ppm
F _{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	100 ^[4]	Ω
Jitter	RMS Jitter ^[1]	-	3	-	ps
V _{ih} _CKXTAL	Crystal Output High Level	1.4	-	-	V
V _{il} _CKXTAL	Crystal Output Low Level	-	-	0.4	V

Note 1: Phase noise 25kHz to 25MHz RMS < 3ps.

Note 2: The clock accuracy specification of F_{ref} Tolerance +/- 100ppm including total variance due to crystal/oscillator frequency tolerance, temperature, aging, and circuit variations.

Note 3: If application has the limits of ±50ppm tolerance for RGMII timing, use crystal with ±50ppm tolerance instead.

Note 4: The maximum value of ESR depends on the 'shunt capacitance' specified by the crystal manufacturer and the two 'load capacitors'. As a result, the feasible max shunt capacitance is 5 pF.

11.10. Oscillator/External Clock Requirements

Table 168. Oscillator/External Clock Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance ^{[2][3]}	Ta=-40°C~125°C	-100	-	100	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter ^[1]	-	-	3	30 ^[4]	ps
Vih	-	1.4	-	-	V
Vil	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	-40	-	125	°C

Note 1: Phase noise 25kHz to 25MHz RMS <3ps.

Note 2: The clock accuracy specification of F_{ref} Tolerance +/- 100ppm including total variance due to crystal/oscillator frequency tolerance, temperature, aging, and circuit variations.

Note 3: If application has the limits of +/- 50ppm tolerance for RGMII timing, use crystal with +/- 50ppm tolerance instead.

Note 4: The external input clock with RMS jitter 30ps is the worst case. Any degradation factors on the RMS jitter of external clock source should be taken into consideration, including the supply voltage, temperature, aging, process ... etc.

11.11. AC Characteristics

11.11.1. MDC/MDIO Timing

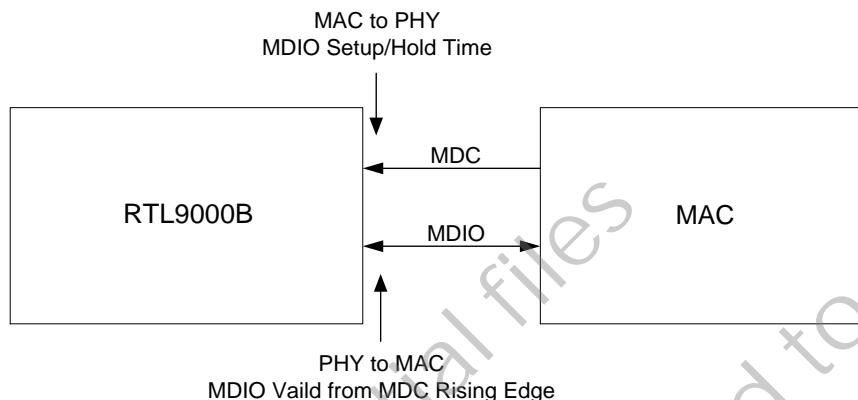


Figure 70. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

MDC/MDIO Timing – Management Port

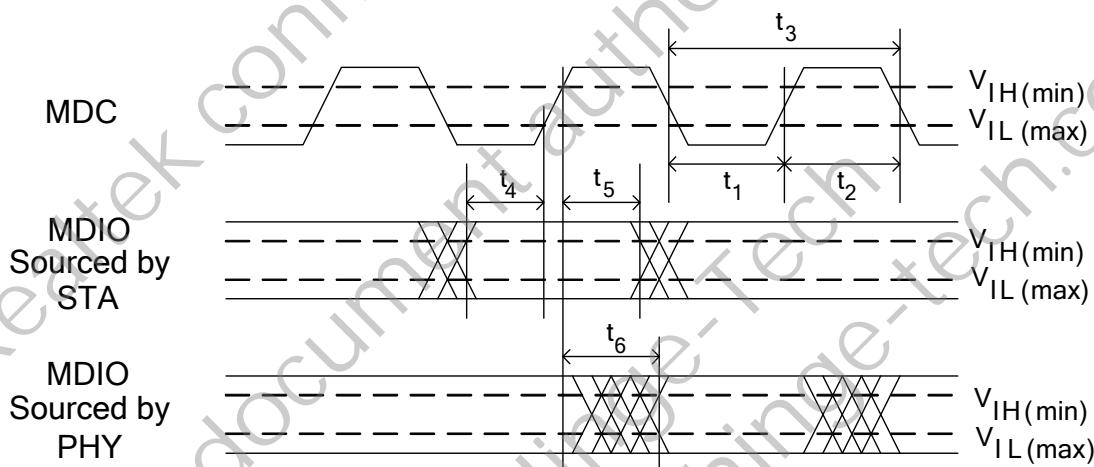


Figure 71. MDC/MDIO Management Timing Parameters

Table 169. MDC/MDIO Management Timing Parameters

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC Low Pulse Width	160	-	ns
t_2	MDC High Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

11.11.2. MII Transmission Cycle Timing

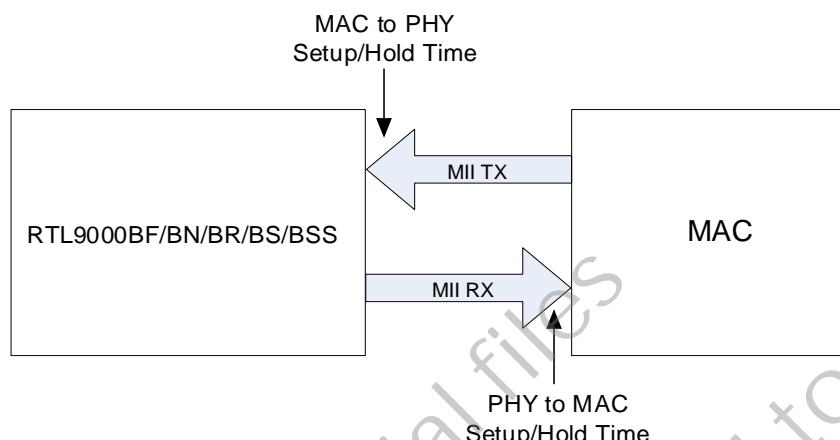


Figure 72. MII Interface Setup/Hold Time Definitions

Figure 73 shows an example of a packet transfer from MAC to PHY on the MII interface.

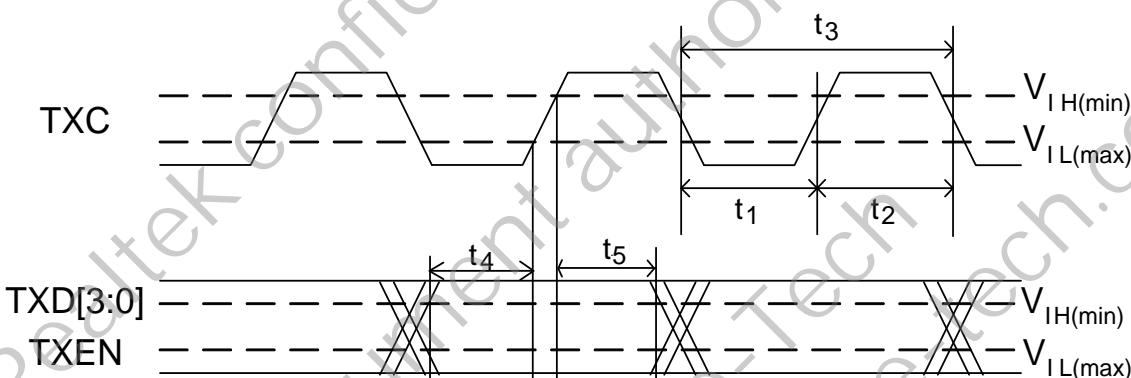


Figure 73. MII Transmission Cycle Timing

Table 170. MII Transmission Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
t_1, t_2	TXCLK Duty Cycle	40	50	60	%
t_3	TXCLK Period	-	40	-	ns
t_4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	15	-	-	ns
t_5	TXEN, TXD[0:3] Hold after TXCLK Rising Edge	0	-	-	ns

11.11.3. MII Reception Cycle Timing

Figure 74 shows an example of a packet transfer from PHY to MAC on the MII interface.

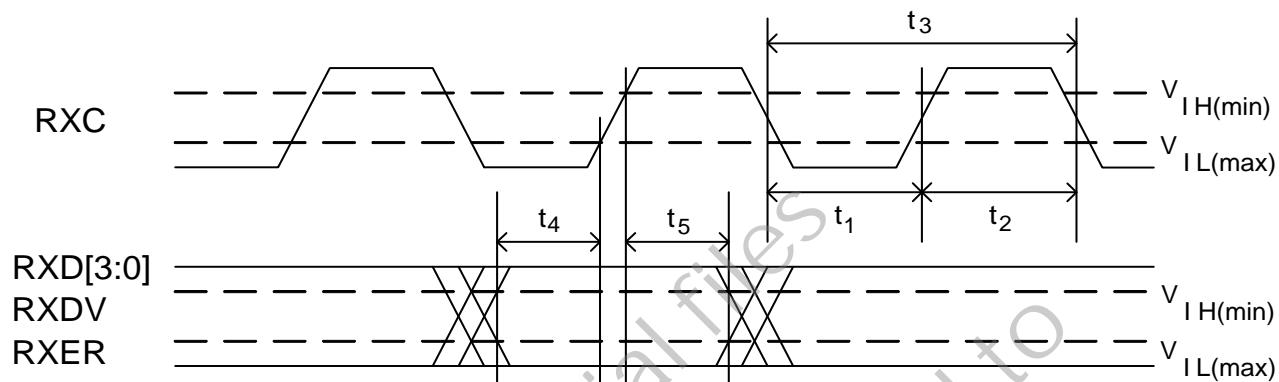


Figure 74. MII Reception Cycle Timing

Table 171. MII Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
t_1, t_2	RXC Duty Cycle	40	50	60	%
t_3	RXC Period	-	40	-	ns
t_4	RXER, RXDV, RXD[3:0] Setup to RXC Rising Edge	15	-	-	ns
t_5	RXER, RXDV, RXD[3:0] Hold After RXC Rising Edge	15	-	-	ns

11.11.4. RMII Transmission and Reception Cycle Timing

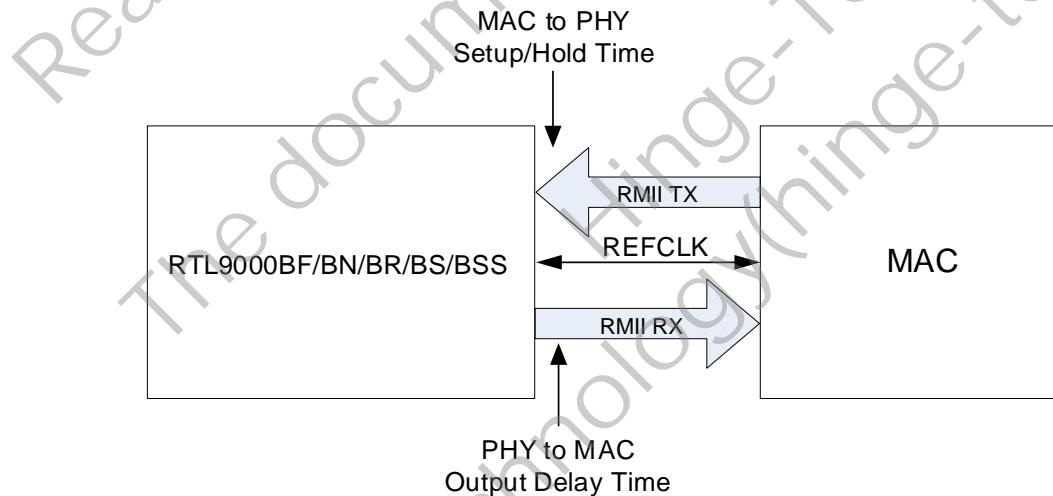


Figure 75. RMII Interfaces Setup, Hold Time, and Output Delay Time Definitions

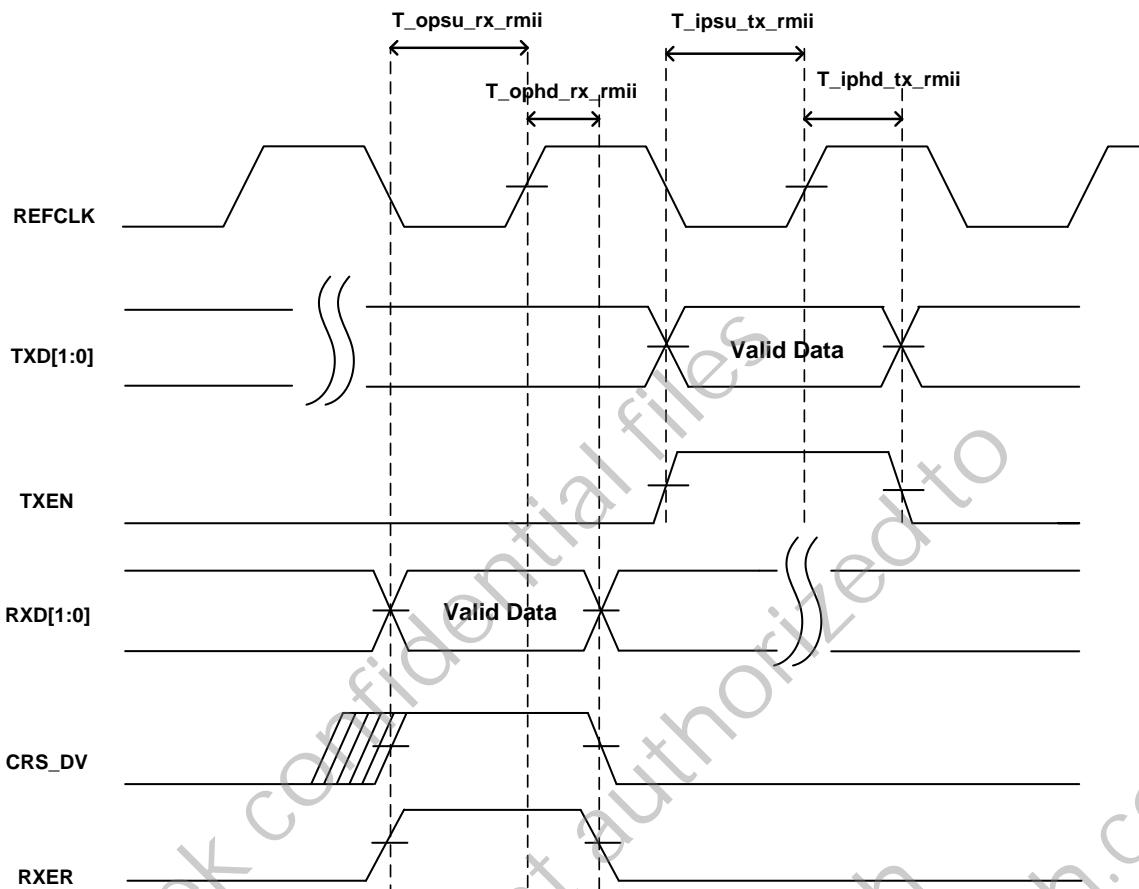


Figure 76. RMII Transmission and Reception Cycle Timing

Table 172. RMII Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii ^{Note1}	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii ^{Note1}	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_opsu_rx_rmii ^{Note2}	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	4	-	-	ns
T_iphd_rx_rmii ^{Note2}	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns
Tr ^{Note3}	Rising time	1	-	5	ns
Tf ^{Note3}	Falling time	1	-	5	ns

Note 1: RMII TX timing can be adjusted by setting RMII_TX_timing in section 9.2.39..

Note 2: RMII RX timing can be adjusted by setting RMII_RX_timing in section 9.2.39.

Note 3: Please note the the Vih = 2.0V, Vil = 0.8V for 3.3V; Vih = 1.7V, Vil = 0.7V for 2.5V; as for the 1.8V the rising/falling time range is 35%~65%.

11.11.5. RGMII Timing Modes

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals, and therefore skew between the clock and data is critical to proper operation.

The OPEN RGMII interface definition supports two delay modes. One is Delay on Destination (DoD), in which clock, data, and control signals are transferred edge aligned. The delay of the clock signal must be accomplished by the receiver device.

The other is Delay on Source (DoS), in which the transmitter device already provides a delayed clock signal. Thus, in the TX path as shown in Figure 77, the MAC is the Source signal and the PHY is the Destination signal; the waveform and the defined timing parameters should be followed depending on which delay mode is used. For example, when the internal delay to RXC for RXD latching is enabled in the PHY, the waveform arriving at the PHY side should follow the timing defined by DoD at the signal destination. Figure 79 and Table 173 show the waveform in DoD mode. DoS mode and the timing parameters when arrives the PHY side should be followed. Note that the position of defined waveform and timing parameters is the blue dot in Figure 77. To add the delay to RXC/TXC for data latching refer to section 9.2.40.

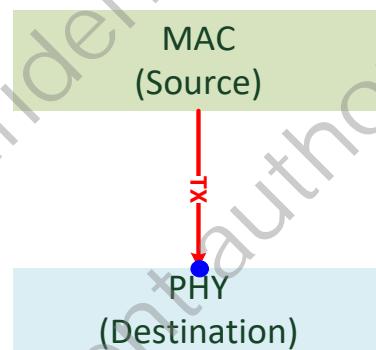


Figure 77. TX Path

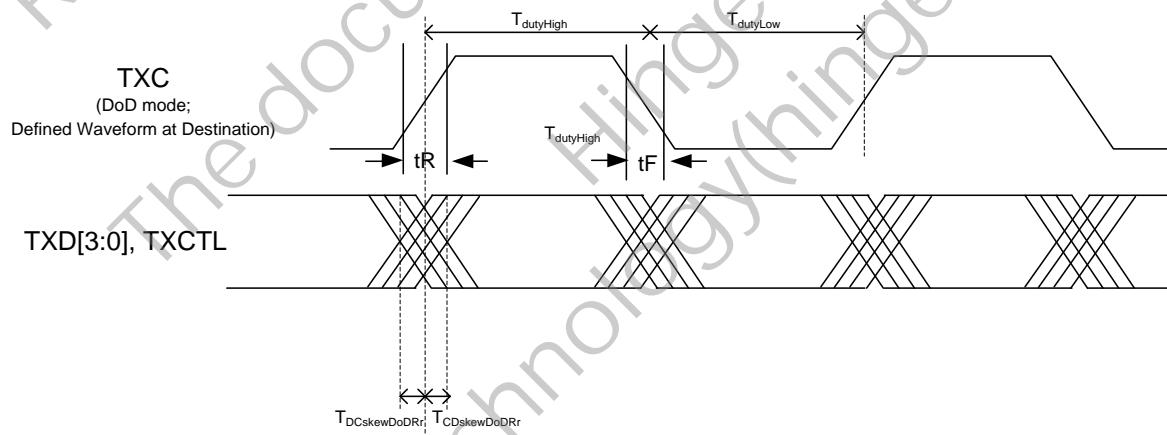


Figure 78. Signal Timing Parameters at Signal Destination in DoD Mode

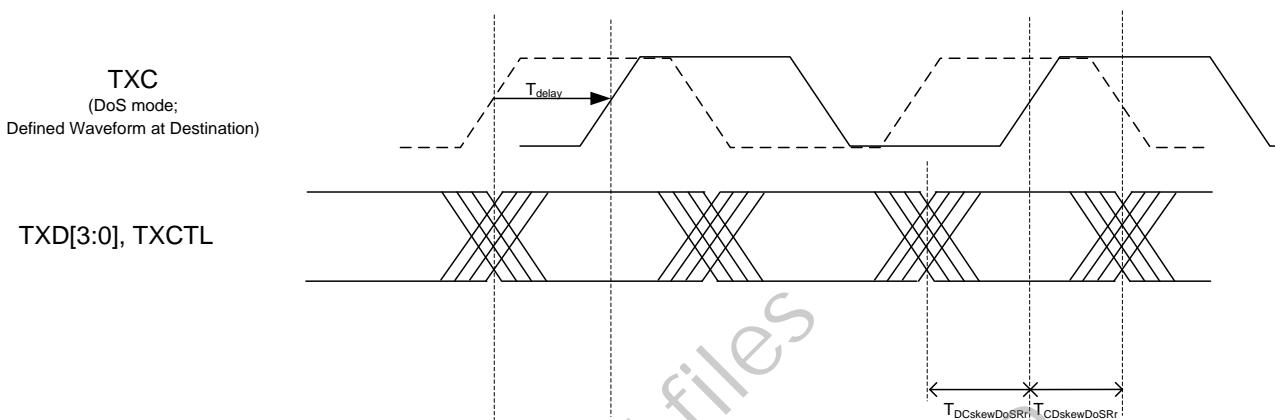


Figure 79. Signal Timing Parameters at Signal Destination in DoS Mode

Table 173. RGMII Timing Parameters in TX path

Symbol	Description	Min	Typical	Max	Units
Tcyc * ¹	Clock Cycle Duration (100Mbps)	36	40	44	ns
Duty_T	Duty Cycle	40	50	60	%
tR	TXC/RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	TXC/RXC Fall Time (20%~80%)	-	-	0.75	ns
DoD Mode at Signal Destination Rising Edge					
TDCskewDoDRr	Data to Clock skew in Delay on Destination mode at signal destination rising edge	-	-	0.65	ns
TCDskewDoDRr	Clock to Data skew in Delay on Destination mode at signal destination rising edge	-	-	0.65	ns
DoS Mode at Signal Destination Rising Edge					
TDCskewDoSRr	Data to Clock skew in Delay on Source mode at signal destination rising edge	-	-	4* ²	ns
TCDskewDoSRr	Clock to Data skew in Delay on Source mode at signal destination rising edge	15	-	-	ns

Note 1: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Note 2: The RTL9000BF/BN/BR/BS/BSS have an internal delay by default and cannot be deactivated. The T_{delay} in the TX path arriving at the PHY side should be less than or equal to 4ns. If the T_{delay} is longer than 4ns (maximum is 11ns), we suggest that the TXC_INV should be set to 1 and the RGMII_TXC_Timing be set to 2b'11. Refer to section 9.2.40.

In the RX path shown in Figure 80, the MAC is the Destination signal and the PHY is the Source signal; the waveform and the defined timing parameters should be followed depending on which delay mode is used. For example, when the user adds the delay on the signal Destination and the internal delay to RXC for RXD latching is disabled in PHY, the waveform transmitted by the PHY side is defined by the timing in DoD at the signal source.

Figure 81, Figure 82, and Table 174 show the waveform in the DoD mode and DoS mode, as well as the timing parameters transmitted by the PHY. Note that the position of the defined waveform and timing parameters is the blue dot in Figure 80.

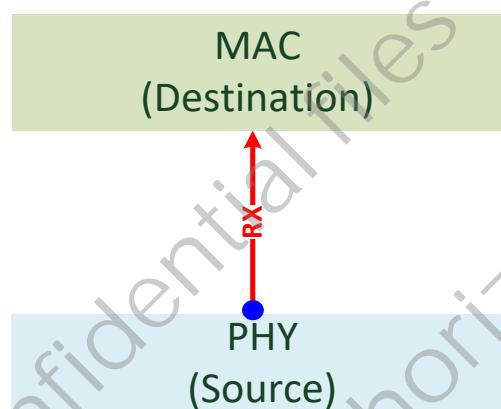


Figure 80. RX Path

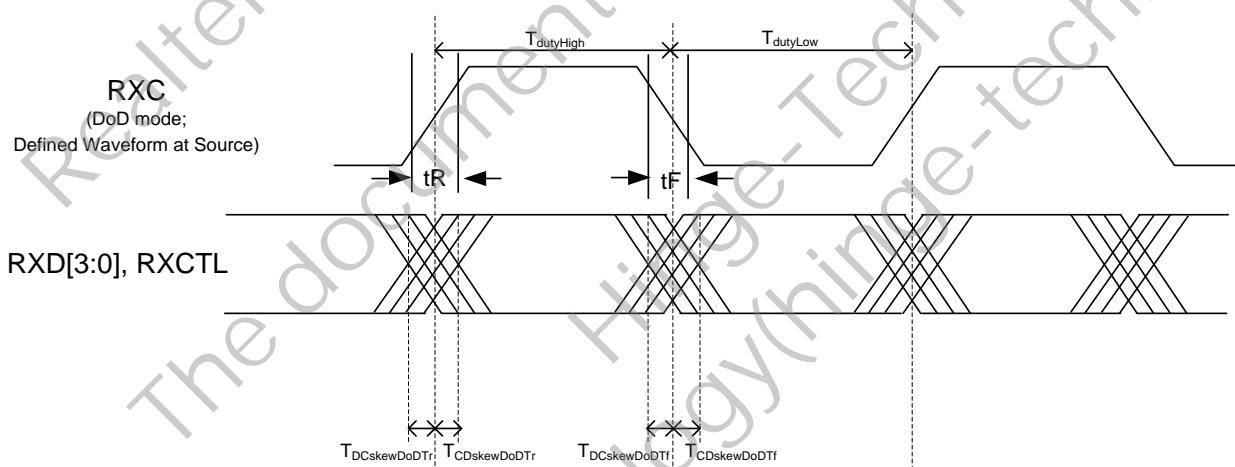


Figure 81. Signal Timing Parameters at Signal Source in DoD Mode

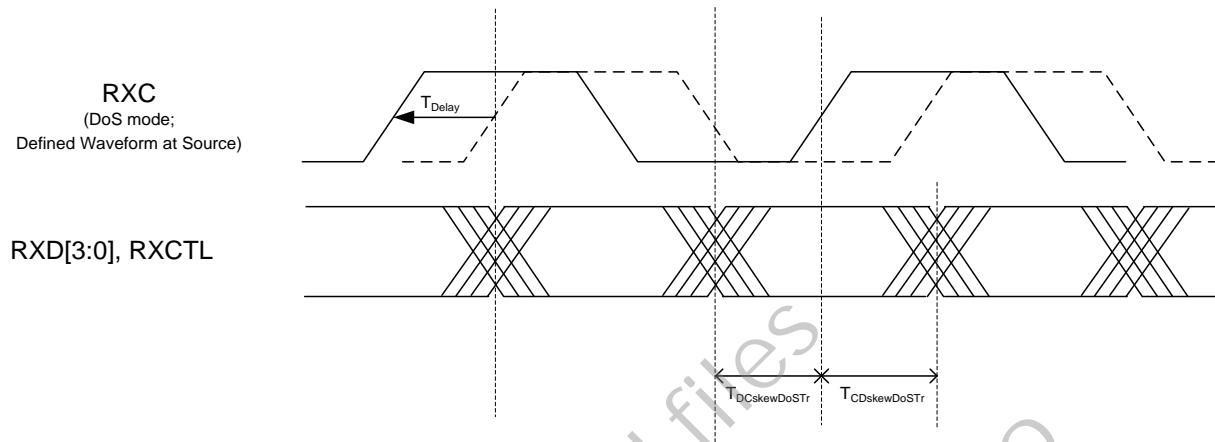


Figure 82. Signal Timing Parameters at Signal Source in DoS Mode

Table 174. RGMII Timing Parameters in RX path

Symbol	Description	Min	Typical	Max	Units
Tcyc *1	Clock Cycle Duration (100Mbps)	36	40	44	ns
Duty_T	Duty Cycle	40	50	60	%
tR	TXC/RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	TXC/RXC Fall Time (20%~80%)	-	-	0.75	ns
DoD Mode at Signal Source rising edge					
TDCskewDoDTr	Data to Clock skew in Delay on Destination mode at signal Source rising edge	-	-	2	ns
TCDskewDoDTr	Clock to Data skew in Delay on Destination mode at signal Source rising edge	-	-	2	ns
DoS Mode at Signal Source rising edge					
TDCskewDoSTr	Data to Clock skew in Delay on Source mode at signal Source rising edge *2	-	20 - TDelay	-	ns
TCDskewDoSTr	Clock to Data skew in Delay on Source mode at signal Source rising edge *2	-	TDelay *3	-	ns

Note 1: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Note 2: The internal delay is deactivated with default hence the RXC and RXD is aligned. Refer to section 9.2.40 for enabling and adding the delay.

Note 3: Refer to section 9.2.40 for enabling and adding the delay. The delay level increases to 4ns for RXC latching RXD, refer to TDelay in Figure 82.

11.11.6. SGMII Timing

Table 175. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Notes
UI	Unit Interval	-	800	-	ps	$800\text{ps} \pm 100\text{ppm}$
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	150	-	-	mV	-
T_Y2	Eye Mask	-	-	400	mV	-
V _{TX-DIFFp-p}	Output Differential Voltage	300	-	800	mV	-
T _{TX-JITTER} *a	Output Jitter	-	-	0.3	UI	CDR BW depend on data rate 750K(Data Rate/1667), 1 st -order
T _{TX-RISE}	Output Rise Time	0.15	-	-	UI	20% ~ 80%
T _{TX-FALL}	Output Fall Time	0.15	-	-	UI	20% ~ 80%
R _{TX}	Differential Resistance	80	100	120	ohm	-
C _{TX}	AC Coupling Capacitor	80	100	120	nF	-
L _{TX}	Transmit Length in PCB	-	-	10	inch	-

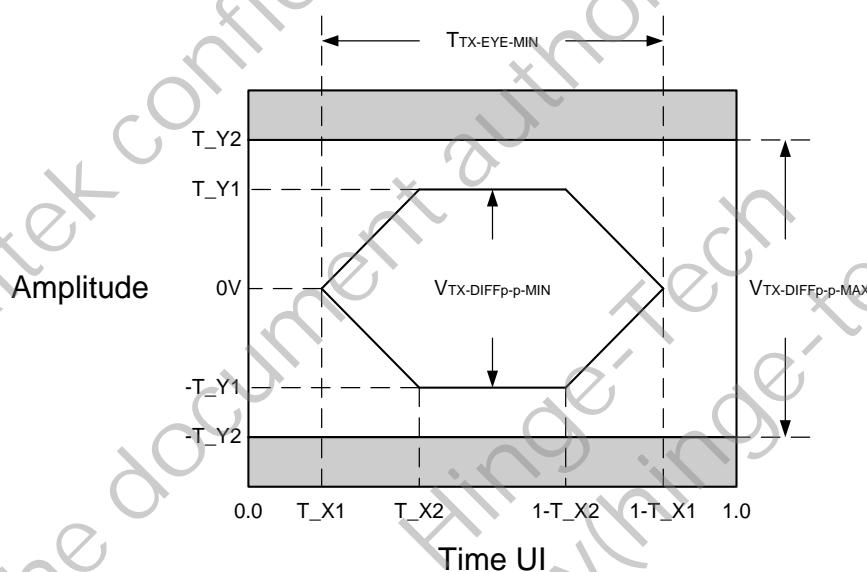
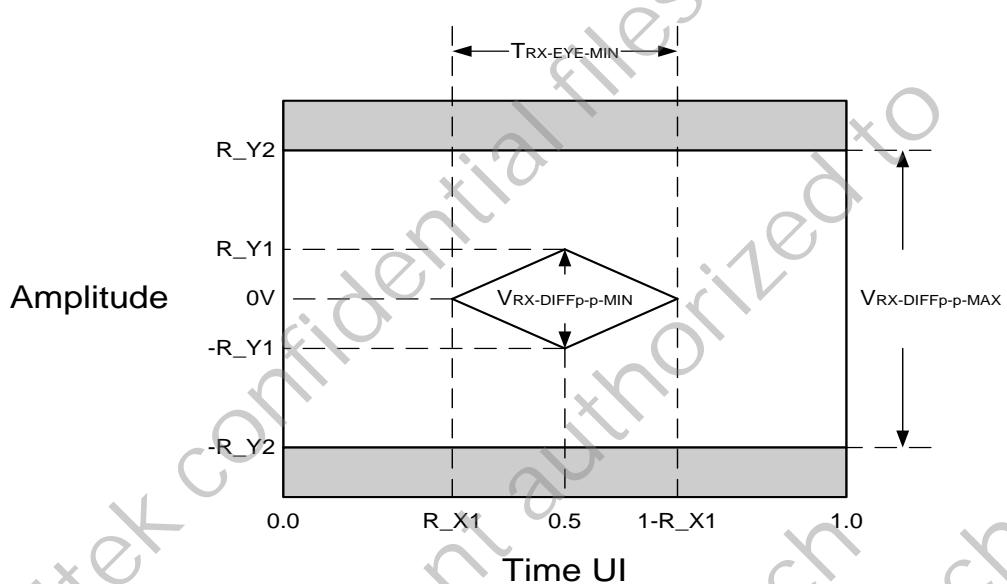


Figure 83. SGMII Differential Transmitter Characteristics Eye Mask

Table 176. SGMII Differential Receiver Characteristics

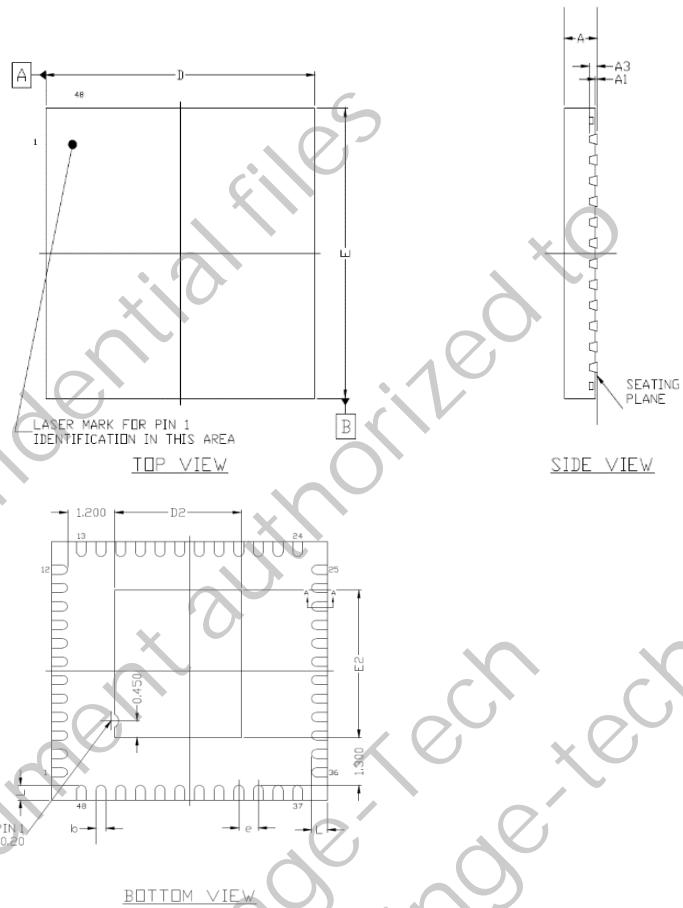
Symbol	Parameter	Min	Typ.	Max	Units	Notes
UI	Unit Interval	-	800	-	ps	$800\text{ps} \pm 100\text{ppm}$
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
V_RX-DIFFp-p	Input Differential Voltage	200	-	1200	mV	-
R_RX	Differential Resistance	80	100	120	ohm	-


Figure 84. SGMII Differential Receiver Characteristics Eye Mask

12. Mechanical Dimensions

12.1. RTL9000BF Mechanical Dimensions Notes

12.1.1. Full-Cut

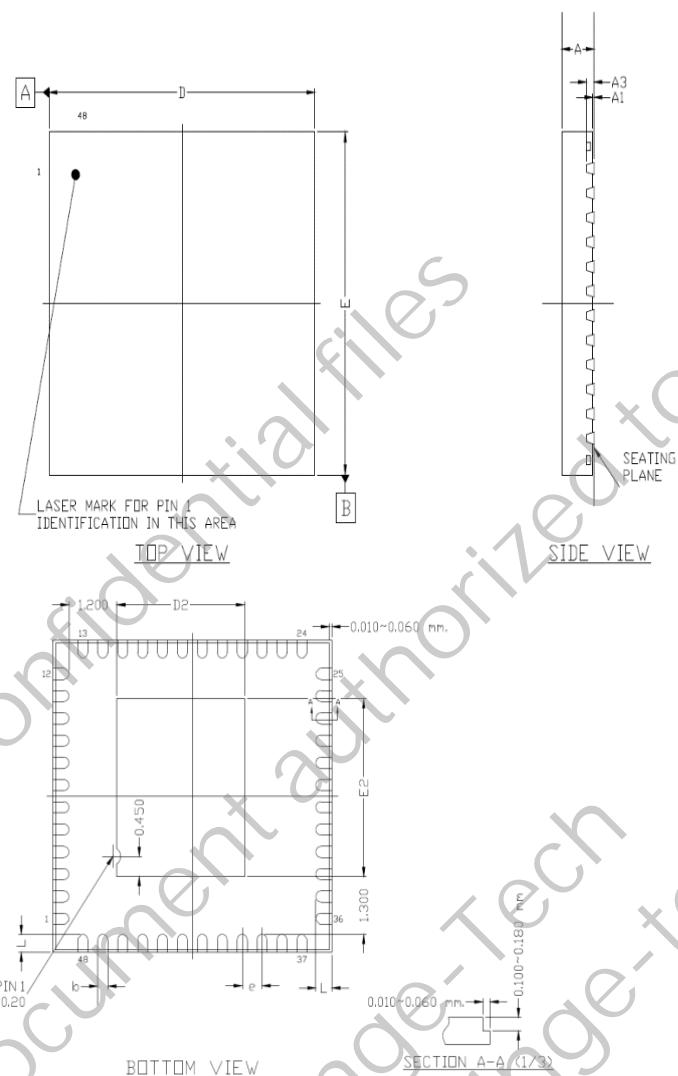


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	7.00 BSC			0.276 BSC		
D2	3.11	3.21	3.31	0.122	0.126	0.130
E2	3.89	3.99	4.09	0.153	0.157	0.161
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

12.1.2. Step-Cut



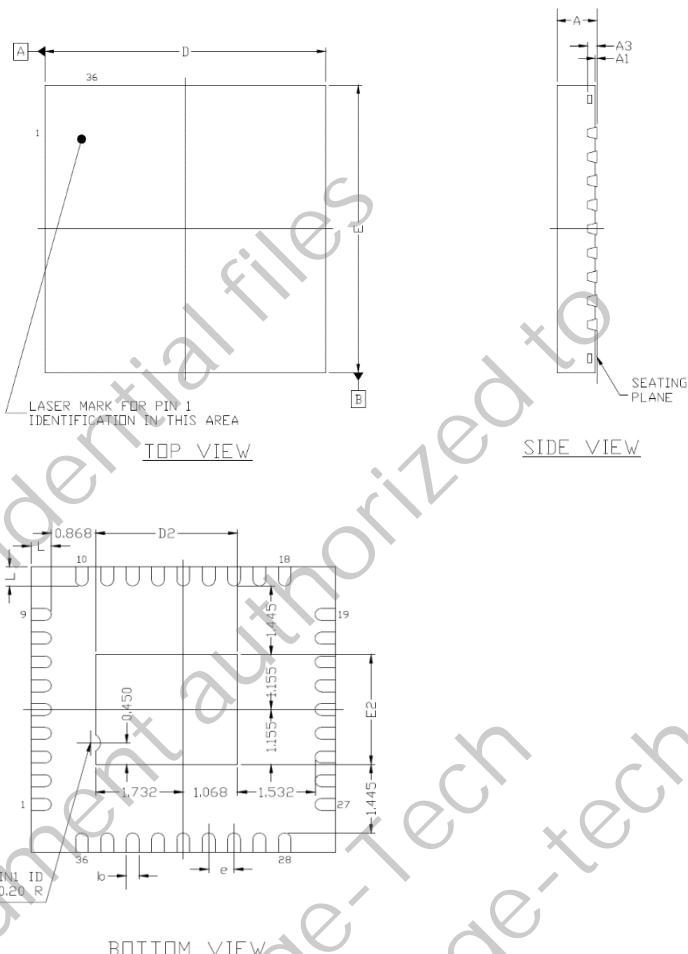
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	7.00 BSC			0.276 BSC		
D2	3.11	3.21	3.31	0.122	0.126	0.130
E2	3.89	3.99	4.09	0.153	0.157	0.161
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

12.1. RTL9000BN Mechanical Dimensions Notes

12.1.1. Full-Cut

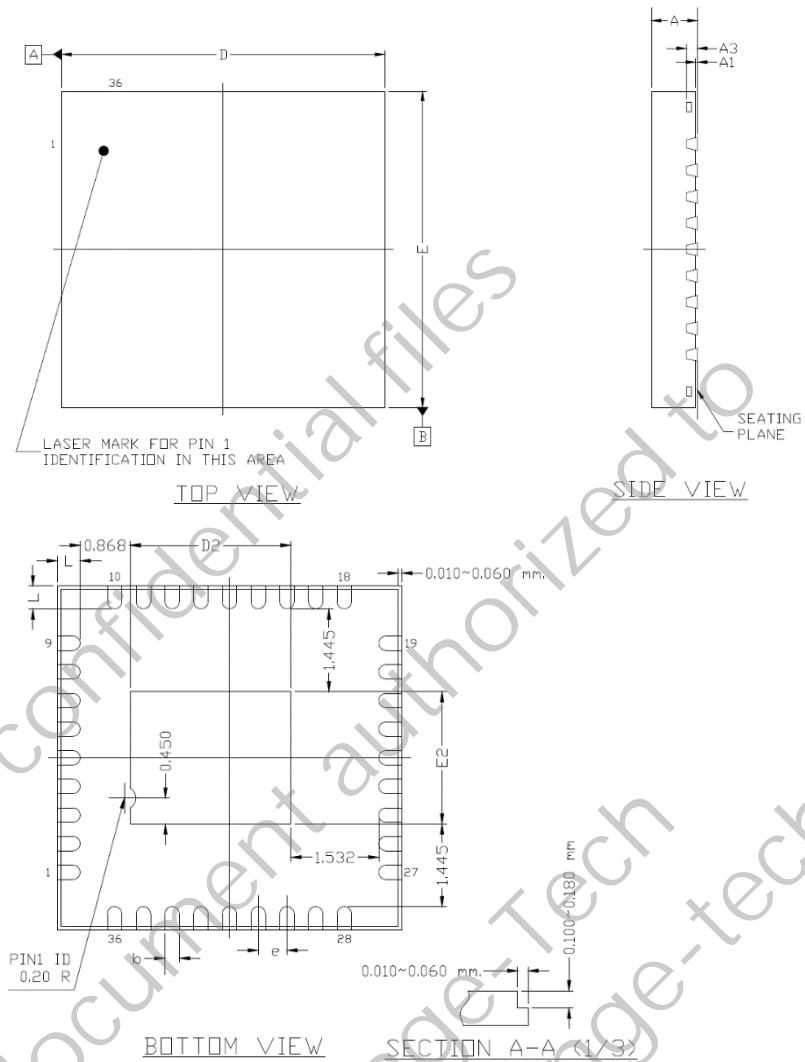


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.00 BSC			0.236 BSC		
D2	2.70	2.80	2.90	0.106	0.110	0.114
E2	2.21	2.31	2.41	0.087	0.091	0.095
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

12.1.2. Step-Cut



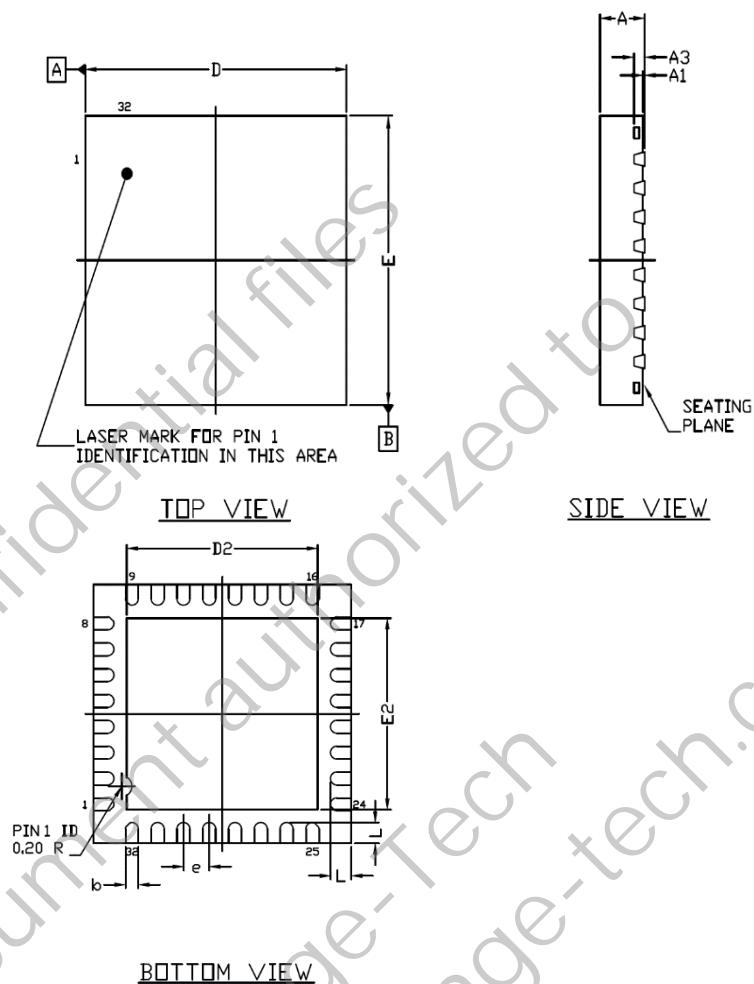
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.00 BSC			0.236 BSC		
D2	2.70	2.80	2.90	0.106	0.110	0.114
E2	2.21	2.31	2.41	0.087	0.091	0.095
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

- CONTROLLING DIMENSION: MILLIMETER(mm).
- REFERENCE DOCUMENT: JEDEC MO-220.

12.2. RTL9000BR Mechanical Dimensions Notes

12.2.1. Full-Cut

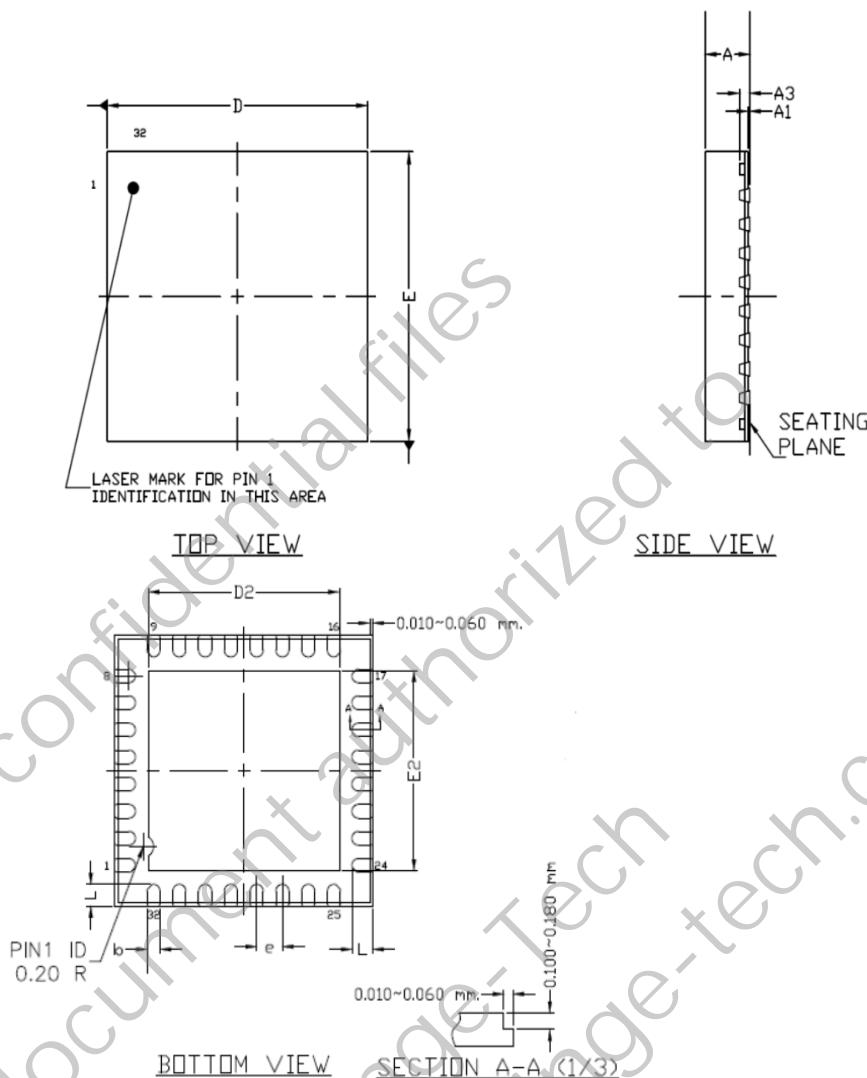


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2	3.60	3.70	3.80	0.142	0.146	0.150
E2	3.60	3.70	3.80	0.142	0.146	0.150
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

- CONTROLLING DIMENSION: MILLIMETER(mm).
- REFERENCE DOCUMENT: JEDEC MO-220.

12.2.2. Step-Cut



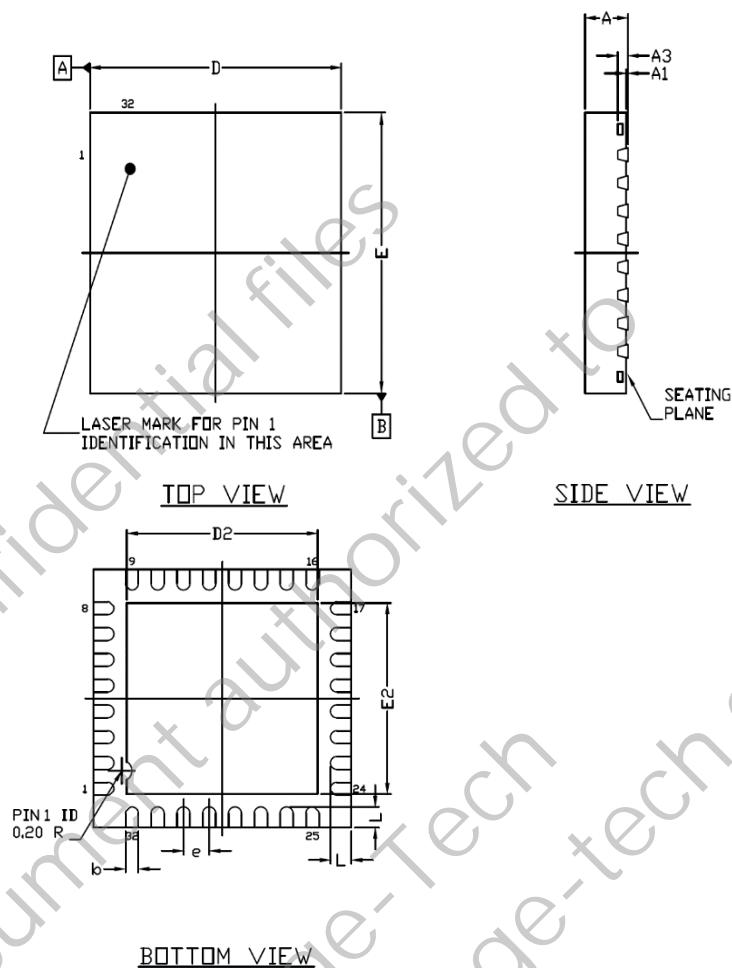
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2	3.60	3.70	3.80	0.142	0.146	0.150
E2	3.60	3.70	3.80	0.142	0.146	0.150
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

- CONTROLLING DIMENSION: MILLIMETER(mm).
- REFERENCE DOCUMENT: JEDEC MO-220.

12.3. RTL9000BS Mechanical Dimensions Notes

12.3.1. Full-Cut

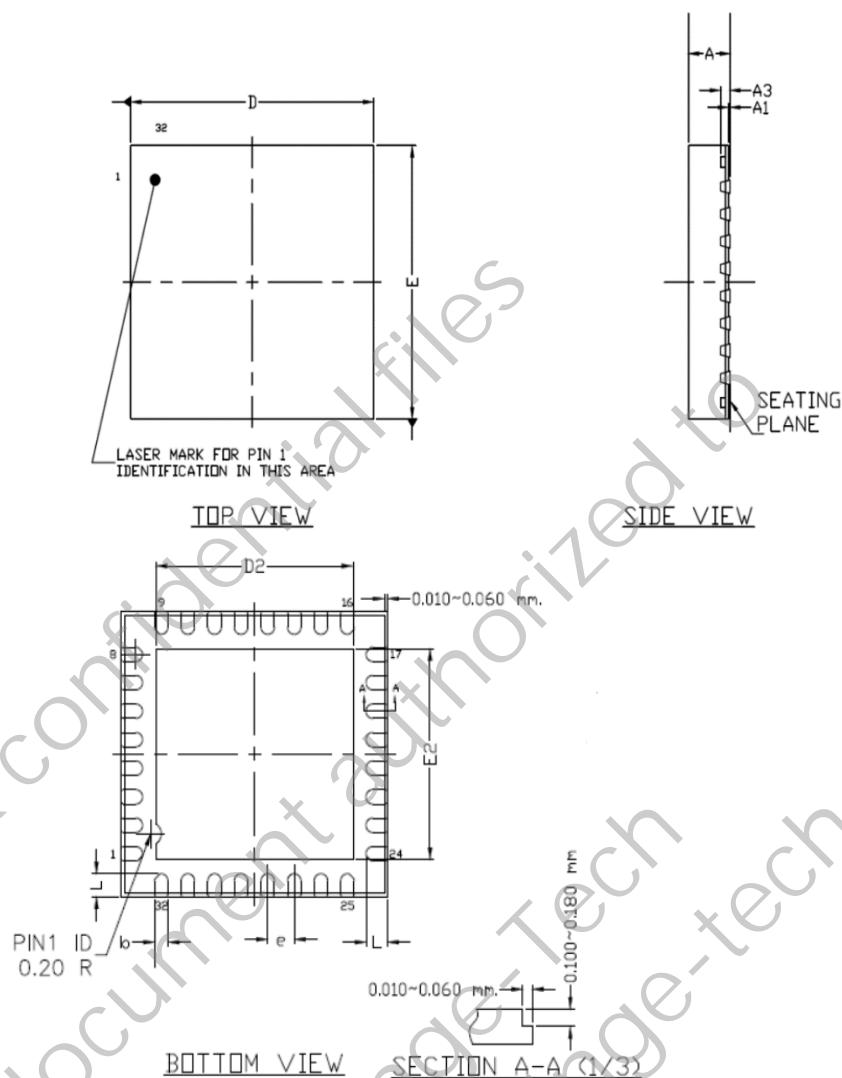


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2	3.60	3.70	3.80	0.142	0.146	0.150
E2	3.60	3.70	3.80	0.142	0.146	0.150
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

12.3.2. Step-Cut



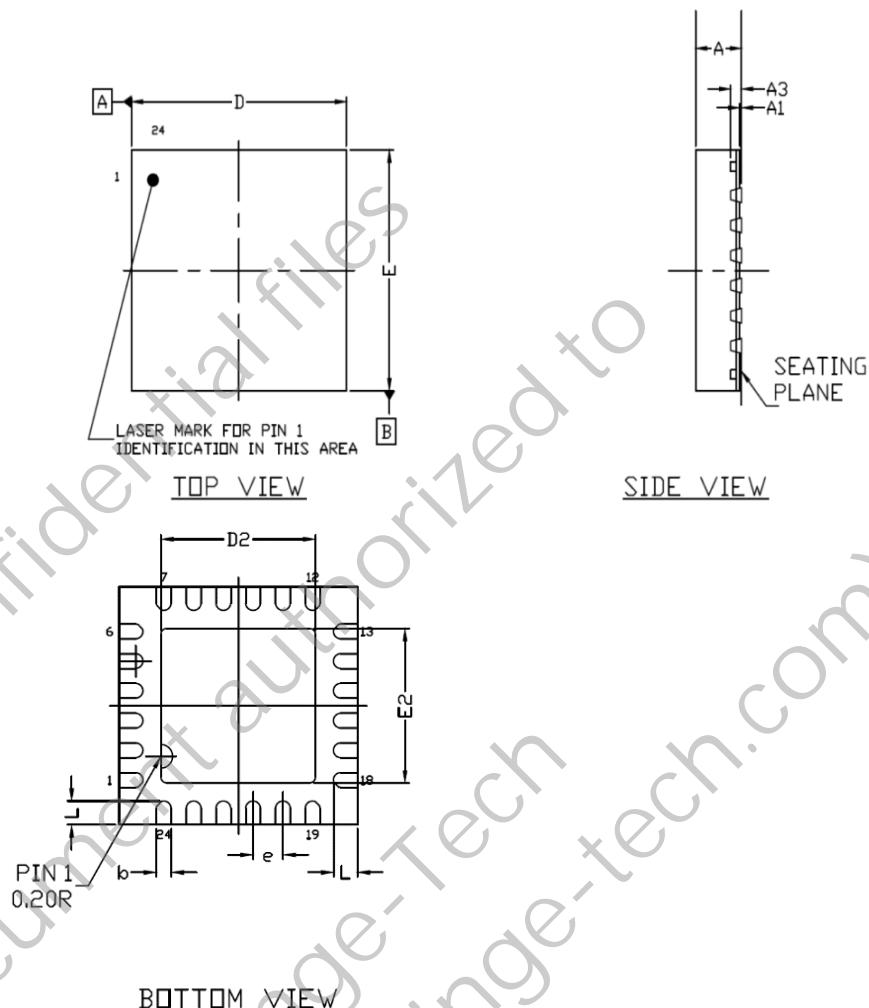
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2	3.60	3.70	3.80	0.142	0.146	0.150
E2	3.60	3.70	3.80	0.142	0.146	0.150
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

- CONTROLLING DIMENSION: MILLIMETER(mm).
- REFERENCE DOCUMENT: JEDEC MO-220.

12.4. RTL9000BSS Mechanical Dimensions Notes

12.4.1. Full-Cut

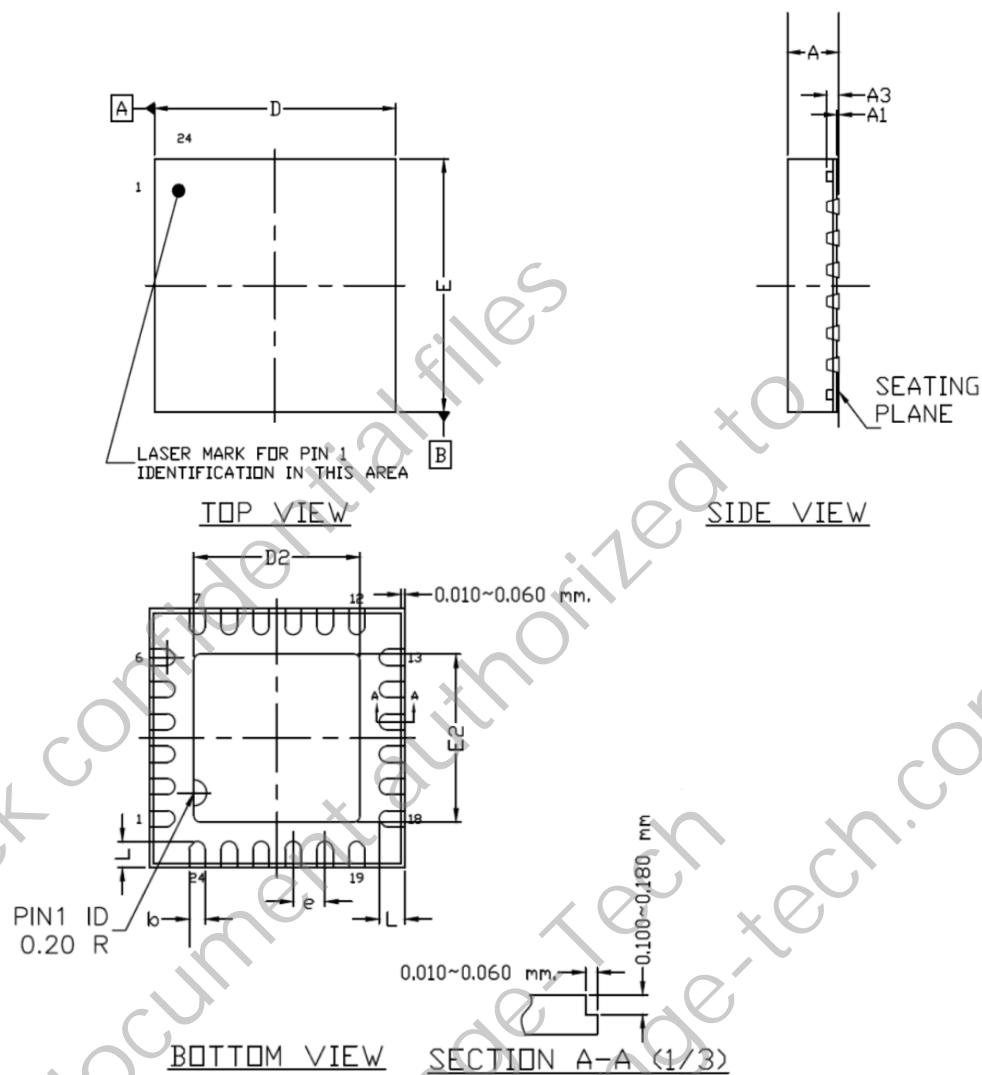


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.00 BSC			0.157 BSC		
D2	2.50	2.60	2.70	0.098	0.102	0.106
E2	2.50	2.60	2.70	0.098	0.102	0.106
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

1. CONTROLLING DIMENSION: MILLIMETER(mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

12.4.2. Step-Cut



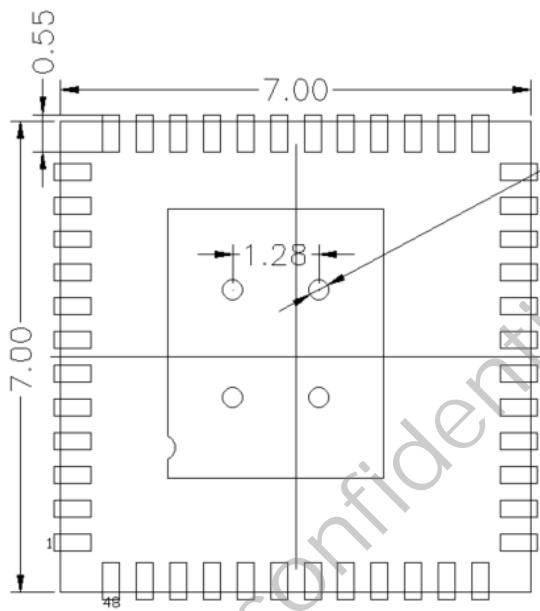
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.00 BSC			0.157 BSC		
D2	2.50	2.60	2.70	0.098	0.102	0.106
E2	2.50	2.60	2.70	0.098	0.102	0.106
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes:

- CONTROLLING DIMENSION: MILLIMETER(mm).
- REFERENCE DOCUMENT: JEDEC MO-220.

12.5. RTL9000BF Board Layout

PCB Outline



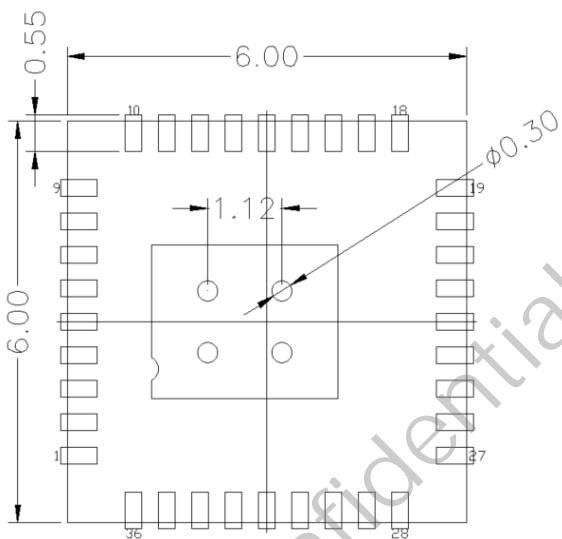
DOFU QFN 7X7 48L
PCB DESIGN
Pitch: 0.5mm
Lead width: 0.25mm
Lead length: 0.55mm
Thermal pad: 3.21 x 3.99mm
Thermal via: pitch 1.28mm
dia. 0.3mm x 4

Notes:

1. NON SOLDER MASK DEFINED IS PREFERRED
2. CONTROLLING DIMENSION: MILLIMETER(mm).
3. REFERENCE DOCUMENT: IPC-7351

12.6. RTL9000BN Board Layout

PCB Outline



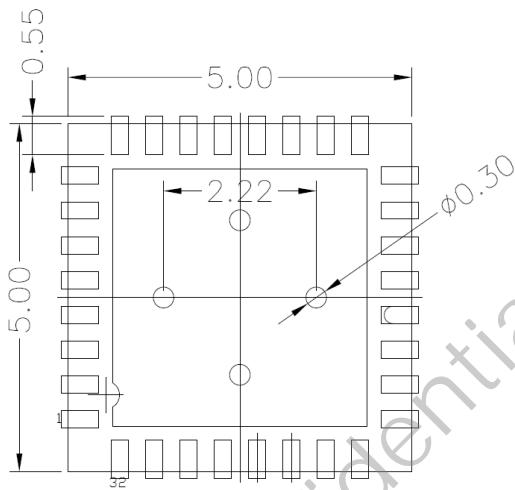
DOFU QFN 6X6 36L
 PCB DESIGN
 Pitch: 0.5mm
 Lead width: 0.25mm
 Lead length: 0.55mm
 Thermal pad: 2.80 x 2.31mm
 Thermal via: pitch 1.12mm
 dia. 0.3mm x 4

Notes:

1. *NON SOLDER MASK DEFINED IS PREFERRED*
2. *CONTROLLING DIMENSION: MILLIMETER(mm).*
3. *REFERENCE DOCUMENT: IPC-7351*

12.7. RTL9000BR Board Layout

PCB Outline



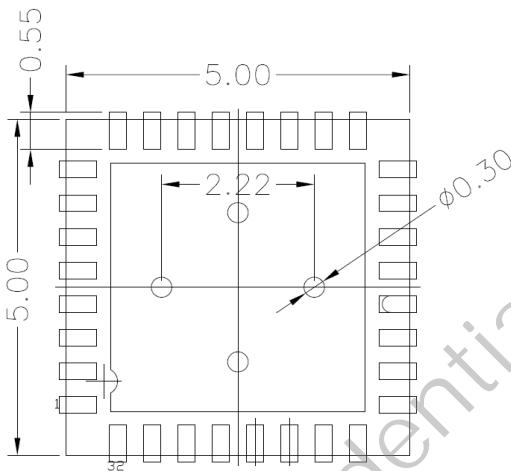
DOFU QFN 5X5 32L
PCB DESIGN
Pitch: 0.5mm
Lead width: 0.25mm
Lead length: 0.55mm
Thermal pad: 3.7 x 3.7mm
Thermal via: pitch 2.22mm
dia. 0.3mm x 4

Notes:

1. *NON SOLDER MASK DEFINED IS PREFERRED*
2. *CONTROLLING DIMENSION: MILLIMETER(mm).*
3. *REFERENCE DOCUMENT: IPC-7351*

12.8. RTL9000BS Board Layout

PCB Outline



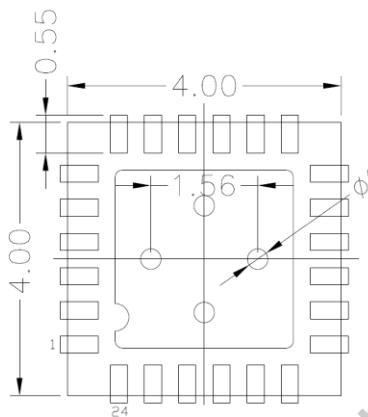
DOFU QFN 5X5 32L
 PCB DESIGN
 Pitch: 0.5mm
 Lead width: 0.25mm
 Lead length: 0.55mm
 Thermal pad: 3.7 x 3.7mm
 Thermal via: pitch 2.22mm
 dia. 0.3mm x 4

Notes:

1. *NON SOLDER MASK DEFINED IS PREFERRED*
2. *CONTROLLING DIMENSION: MILLIMETER(mm).*
3. *REFERENCE DOCUMENT: IPC-7351*

12.9. RTL9000BSS Board Layout

PCB Outline



DOFU QFN 4X4 24L

PCB DESIGN

Pitch: 0.5mm

Lead width: 0.25mm

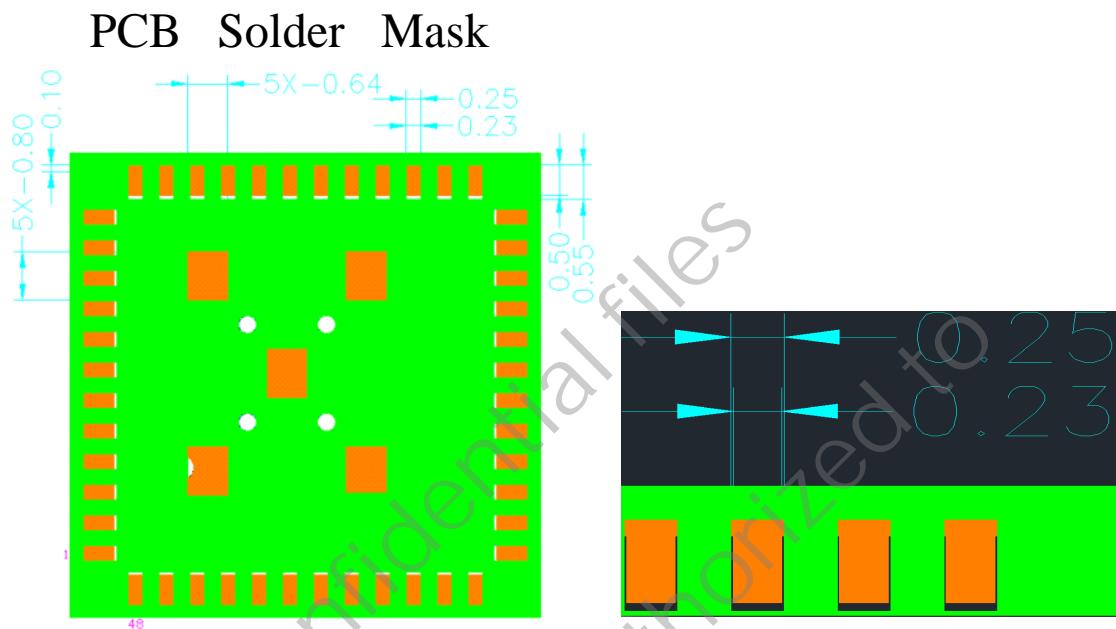
Lead length: 0.55mm

Thermal pad: 2.6 x 2.6mm

Thermal via: pitch 1.56mm
dia. 0.3mm x 4**Notes:**

1. *NON SOLDER MASK DEFINED IS PREFERRED*
2. *CONTROLLING DIMENSION: MILLIMETER(mm).*
3. *REFERENCE DOCUMENT: IPC-7351*

12.10. RTL9000BF Solder Mask Design

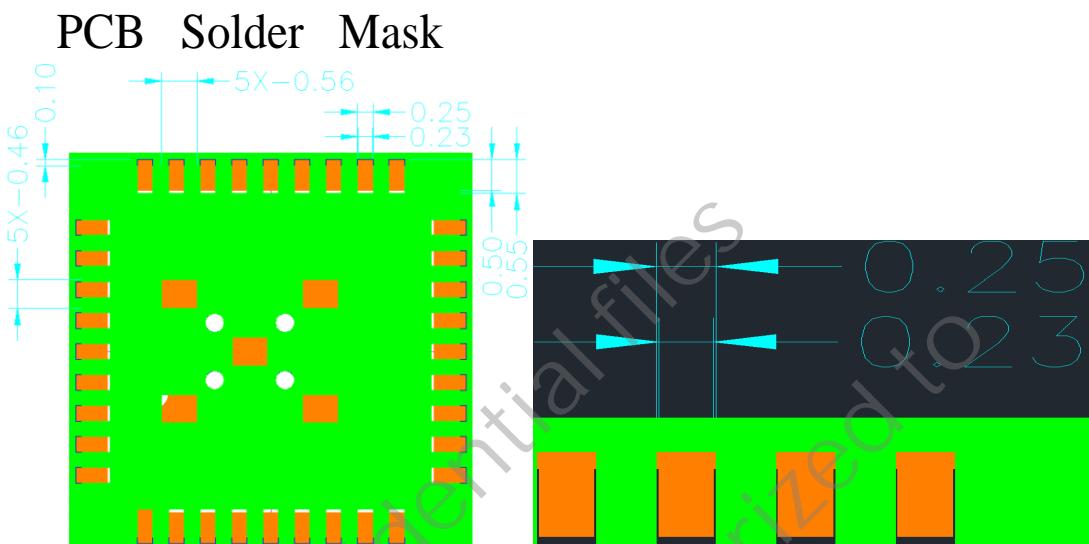


DOFU QFN 7X7 48L
PCB Solder Mask DESIGN
 Pitch: 0.5mm
 Thermal pad: 3.21 x 3.99mm
 Thermal via: pitch 1.2mm
 dia. 0.3mm x 4

Notes:

1. *NON SOLDER MASK DEFINED IS PREFERRED*
2. *CONTROLLING DIMENSION: MILLIMETER(mm).*
3. *REFERENCE DOCUMENT: IPC-7351*

12.11. RTL9000BN Solder Mask Design

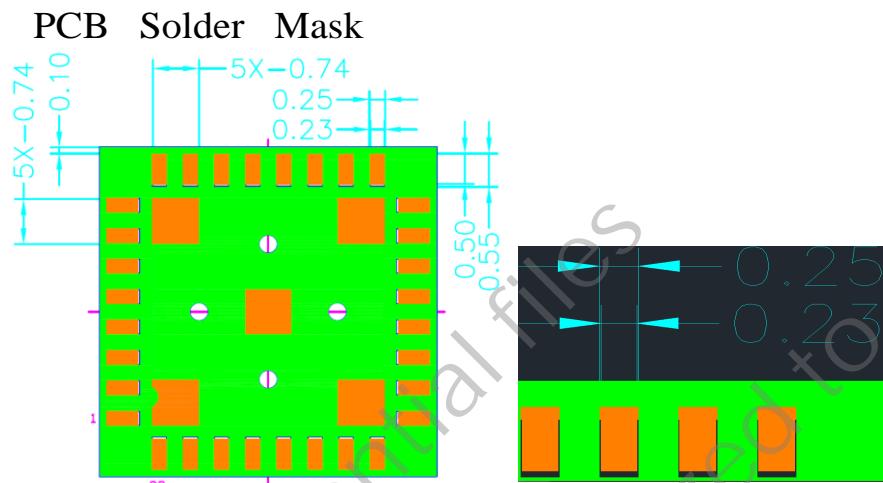


DOFU QFN 6X6 36L
 PCB Solder Mask DESIGN
 Pitch: 0.5mm
 Thermal pad: 2.80 x 2.31mm
 Thermal via: pitch 1.12mm
 dia. 0.3mm x 4

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER(mm)*
2. *BASED ON 0.1 mm THICK STENCIL*
3. *REFERENCE DOCUMENT: IPC-7351 & IPC-7525*

12.12. RTL9000BR Solder Mask Design

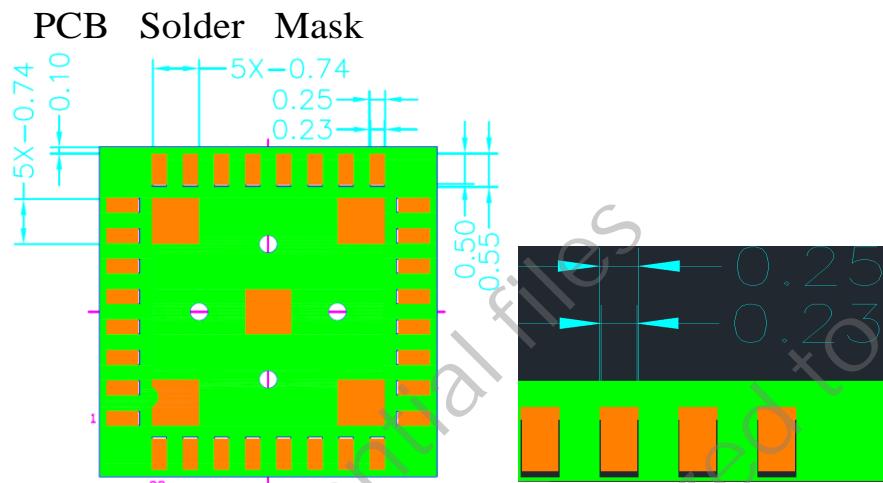


DOFU QFN 5X5 32L
PCB Solder Mask DESIGN
 Pitch: 0.5mm
 Thermal pad: 3.7 x 3.7mm
 Thermal via: pitch 2.22mm
 dia. 0.3mm x 4

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER(mm)*
2. *BASED ON 0.1 mm THICK STENCIL*
3. *REFERENCE DOCUMENT: IPC-7351 & IPC-7525*

12.13. RTL9000BS Solder Mask Design

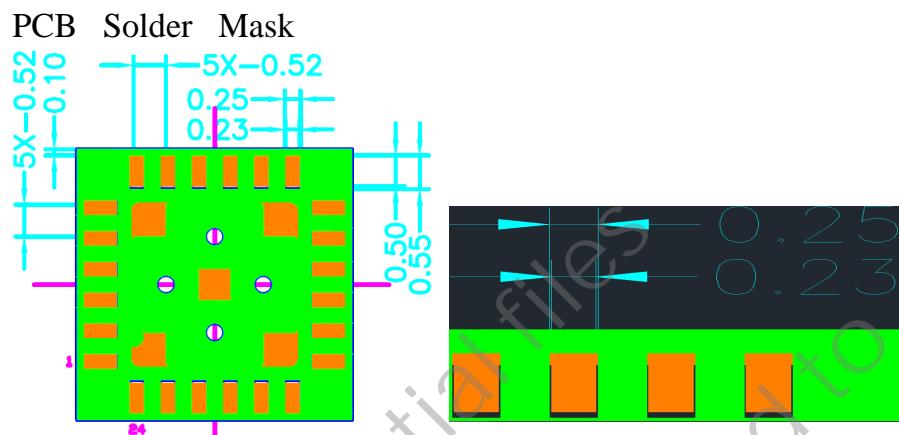


DOFU QFN 5X5 32L
PCB Solder Mask DESIGN
 Pitch: 0.5mm
 Thermal pad: 3.7 x 3.7mm
 Thermal via: pitch 2.22mm
 dia. 0.3mm x 4

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER(mm)*
2. *BASED ON 0.1 mm THICK STENCIL*
3. *REFERENCE DOCUMENT: IPC-7351 & IPC-7525*

12.14. RTL9000BSS Solder Mask Design



DOFU QFN 4X4 24L
 PCB Solder Mask DESIGN
 Pitch: 0.5mm
 Thermal pad: 2.6 x 2.6mm
 Thermal via: pitch 1.56mm
 dia. 0.3mm x 4

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER(mm)*
2. *BASED ON 0.1 mm THICK STENCIL*
3. *REFERENCE DOCUMENT: IPC-7351 & IPC-7525*

13. Ordering Information

Table 177. Ordering Information

Part Number	Package type	Status	Weight (g)
RTL9000BF-VB-CG	48pin QFN with 'Green' Copper wire Package, 7mm x 7mm, shipment in tray	ES	0.134
RTL9000BF-VBA-CG	48pin QFN with 'Green' Copper wire Package, 7mm x 7mm, shipment in tray, Full cut	ES	0.134
RTL9000BN-VB-CG	36pin QFN with 'Green' Copper wire Package, 6mm x 6mm, shipment in tray	In development	0.075
RTL9000BN-VBA-CG	36pin QFN with 'Green' Copper wire Package, 6mm x 6mm, shipment in tray, Full cut	In development	0.075
RTL9000BR-VB-CG	32pin QFN with 'Green' Copper wire Package, 5mm x 5mm, shipment in tray	MP	0.068
RTL9000BR-VB-CGT	32pin QFN with 'Green' Copper wire Package, 5mm x 5mm, shipment in tape&reel	MP	0.068
RTL9000BR-VBA-CG	32pin QFN with 'Green' Copper wire Package, 5mm x 5mm, shipment in tray, Full cut	MP	0.068
RTL9000BS-VB1-CG	32pin QFN with 'Green' Copper wire Package, 5mm x 5mm, shipment in tray	ES	0.068
RTL9000BS-VBA-CG	32pin QFN with 'Green' Copper wire Package, 5mm x 5mm, shipment in tray, Full cut	ES	0.068
RTL9000BSS-VB-CG	24pin QFN with 'Green' Copper wire Package, 4mm x 4mm, shipment in tray	ES, Limited Design-in	0.041
RTL9000BSS-VBA-CG	24pin QFN with 'Green' Copper wire Package, 4mm x 4mm, shipment in tray, Full cut	In development	0.041
MSL (Moisture Sensitivity Level)		Level 3	-

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