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RTL8105E-VB-GR
RTL8105E-VC-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/10/15	First release.
1.1	2009/11/27	Corrected typing errors. Revised Table 15 Absolute Maximum Ratings, page 21.
1.2	2009/12/11	Removed TWSI data.
1.3	2009/12/17	Revised product number.
1.4	2010/04/02	Added Version C data (built-in linear regulator; LDO).
1.5	2010/05/10	Revised the IEEE 802.3az version to Draft 2.4. Revised Table 5 Switching Regulator and Reference, page 6. Added Table 6 LDO Regulator Pins (RTL8105E-VC Only), page 6. Revised Table 9 Power and Ground, page 7. Added section 8 LDO Regulator (RTL8105E-VC Only), page 20.
1.6	2010/09/17	Revised the IEEE 802.3az version to Draft 3.2. Revised LDO Regulator from 1.15V to 1.14V. Revised section 6.2.6 Customizable LED Configuration, page 12. Revised Table 21 DC Characteristics, page 23.
1.7	2011/05/06	Revised section 9.1 Absolute Maximum Ratings, page 21. Added section 9.3 Electrostatic Discharge Performance, page 21. Revised section 9.9.4 Auxiliary Signal Timing Parameters, page 30.

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8105E-VB-GR/RTL8105E-VC-GR Fast Ethernet controller combines a 10/100M IEEE 802.3 compliant Media Access Controller (MAC) with a 10/100M Ethernet transceiver, PCI Express bus controller, and embedded memory. A state-of-the-art switching regulator (RTL8105E-VB & RTL8105-VC) and a linear regulator (LDO; RTL8105E-VC only) are incorporated for reduced BOM cost and enhanced power efficiency.

With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8105E offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, and timing recovery are implemented to provide robust transmission and reception capability at high speeds.

The RTL8105E supports the PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 10/100M Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8105E features embedded One-Time-Programmable (OTP) memory that can replace the external EEPROM (93C46).

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8105E.

The RTL8105E is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8105E supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The RTL8105E supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake up and further reduce power consumption. The RTL8105E can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8105E supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The device also features PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8105E is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

- Integrated 10/100M transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Supports Wake-on-LAN and remote wake-up
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)
- Supports power down/link down power saving
- Transmit/Receive on-chip buffer support
- Embedded OTP memory can replace the external EEPROM
- Serial EEPROM
- Built-in switching regulator
- Built-in linear regulator (LDO; RTL8105E-VC only)
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports quad core Receive-Side Scaling (RSS)
- Supports Protocol Offload (ARP & NS)
- Supports Customized LEDs
- Supports 1-Lane 2.5Gbps PCI Express Bus
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function
- 48-pin QFN ‘Green’ package

3. System Applications

- PCI Express Fast Ethernet on Motherboard, Notebook, or Embedded system

4. Pin Assignments

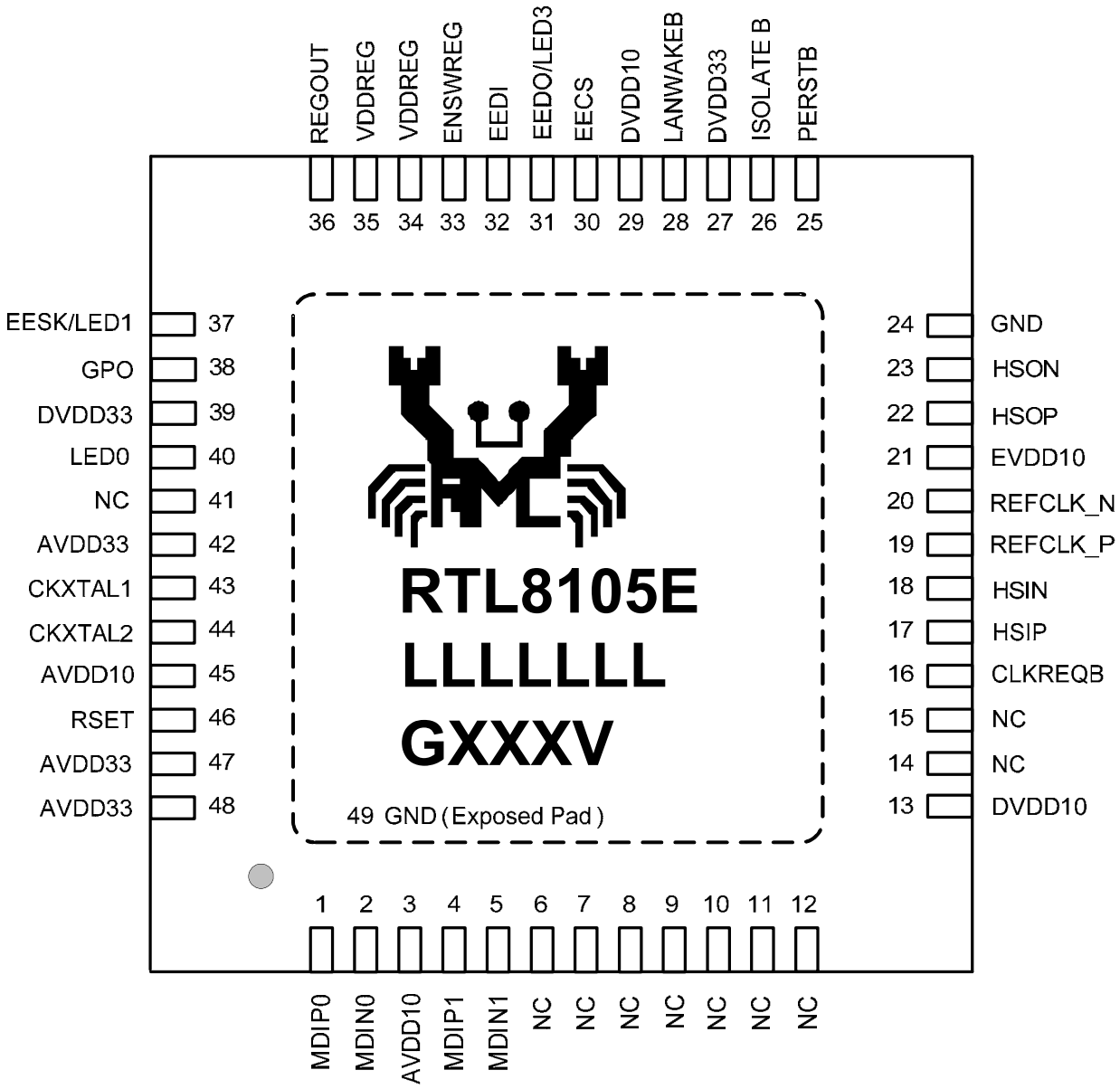


Figure 1. Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 1). The version is shown in the location marked 'V'.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input

O: Output

O/D: Open Drain

P: Power

5.1. Power Management/Isolation Pins

Table 1. Power Management/Isolation Pins

Symbol	Type	Pin No	Description
LANWAKEB	O/D	28	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	26	Isolate Pin: Active low. Used to isolate the RTL8105E from the PCI Express bus. The RTL8105E will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface Pins

Table 2. PCI Express Interface Pins

Symbol	Type	Pin No	Description
REFCLK_P	I	19	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	20	
HSOP	O	22	PCI Express Transmit Differential Pair.
HSON	O	23	
HSIP	I	17	PCI Express Receive Differential Pair.
HSIN	I	18	
PERSTB	I	25	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8105E returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	16	Reference Clock Request Signal. This signal is used by the RTL8105E to request starting of the PCI Express reference clock.

5.3. Transceiver Interface Pins

Table 3. Transceiver Interface Pins

Symbol	Type	Pin No	Description
MDIP0	IO	1	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	2	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	4	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.

5.4. Clock Pins

Table 4. Clock Pins

Symbol	Type	Pin No	Description
CKXTAL1	I	43	Input of 25MHz Clock Reference.
CKXTAL2	IO	44	Output of 25MHz Clock Reference. Input of External Clock Source.

5.5. Switching Regulator and Reference Pins

Table 5. Switching Regulator and Reference Pins

Symbol	Type	Pin No	Description
REGOUT	O	36	Switching Regulator 1.05V Output.
ENSWREG	I	33	3.3V: Enable switching regulator or external 1.05V input mode 0V: Enable LDO regulator
VDDREG	P	34, 35	Digital 3.3V Power Supply for Switching Regulator.
RSET	I	46	Reference. External resistor reference.

Note: See section 7, page 19 for switching regulator.

5.6. LDO Regulator Pins (RTL8105E-VC Only)

Table 6. LDO Regulator Pins (RTL8105E-VC Only)

Symbol	Type	Pin No	Description
AVDD10	P	45	Linear Regulator (LDO) 1.14V Output.
ENSWREG	I	33	3.3V: Enable switching regulator or external 1.05V input mode 0V: Enable LDO regulator

Note1: AVDD10 1.05V output when used with Linear Regulator (LDO) is 1.14V.
Note2: See section 8, page 20 for LDO regulator.

5.7. EEPROM Pins

Table 7. EEPROM Pins

Symbol	Type	Pin No	Description
EESK	O	37	Serial Data Clock.
EEDI	O	32	Output to serial data input pin of EEPROM.
EEDO	I	31	Input from Serial Data Output Pin of EEPROM.
EECS	O	30	EEPROM chip select.

5.8. LED Pins

Table 8. LED Pins

Symbol	Type	Pin No	Description
LED0	O	40	
LED1	O	37	
LED3	O	31	

LEDS1-0	00	01	10	11
LED0	ACT_{ALL}	$Link_{ALL}$/ ACT_{ALL}	Link10/ ACT_{ALL}	LINK10/ ACT_{10}
LED1	LINK100	LINK100	LINK100	LINK100/ ACT_{100}
LED3	Reserved	Reserved	Reserved	Reserved

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the EEPROM.
If there is no EEPROM, the default value of the (LEDS1, LEDS0)=(1, 1).

When implementing dual-color LEDs and EEPROM at the same time:

Pin31 & Pin37 are shared pins. Follow the RTL8105E reference design (version 1.00 or later) to select these 2 pins for a dual color LED circuit. Otherwise, the RTL8105E EEPROM may not function.

5.9. Power and Ground Pins

Table 9. Power and Ground Pins

Symbol	Type	Pin No	Description
DVDD33	P	27, 39	Digital 3.3V Power Supply.
AVDD33	P	42, 47, 48	Analog 3.3V Power Supply. *Note: Pin42 of the RTL8105E-VC is not connected.*
DVDD10	P	13, 29	Digital 1.05V Power Supply.
AVDD10	P	3, 45	Analog 1.05V Power Supply (1.14V when used with Linear Regulator (LDO)). *Note: Pin3 of the RTL8105E-VC is not connected.*
EVDD10	P	21	Analog 1.05V Power Supply.
GND	P	24	Ground.
GND	P	49	Ground (Exposed Pad).

Note: Refer to the latest schematic circuit for correct configuration.

5.10. GPO Pin

Table 10. GPO Pin

Symbol	Type	Pin No	Description
GPO	O	38	General Purpose Output Pin. This pin reflects the link up or link down state. High: Link up Low: Link down

5.11. NC (Not Connected) Pins

Table 11. NC (Not Connected) Pins

Symbol	Type	Pin No	Description
NC	-	6, 7, 8, 9, 10, 11, 12, 14, 15, 41	Not Connected.

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8105E complies with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8105E supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported.

6.1.1. PCI Express Transmitter

The RTL8105E's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8105E's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8105E's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8105E supports three LED signals in four configurable operation modes. The following sections describe the various LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK10/ACT, or LINK100/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. RX LED

In 10/100M mode, blinking of the RX LED indicates that receive activity is occurring.

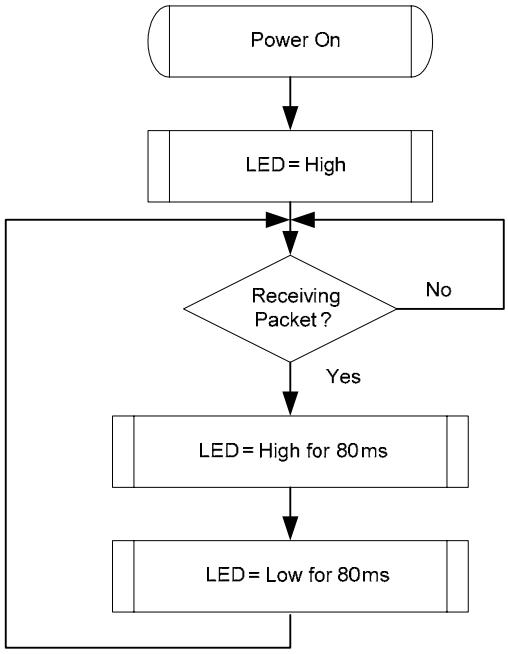


Figure 2. RX LED

6.2.3. TX LED

In 10/100M mode, blinking of the TX LED indicates that transmit activity is occurring.

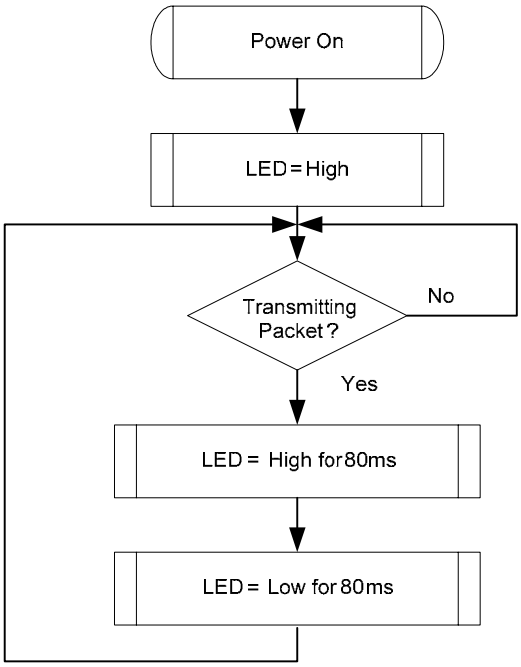


Figure 3. TX LED

6.2.4. TX/RX LED

In 10/100M mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

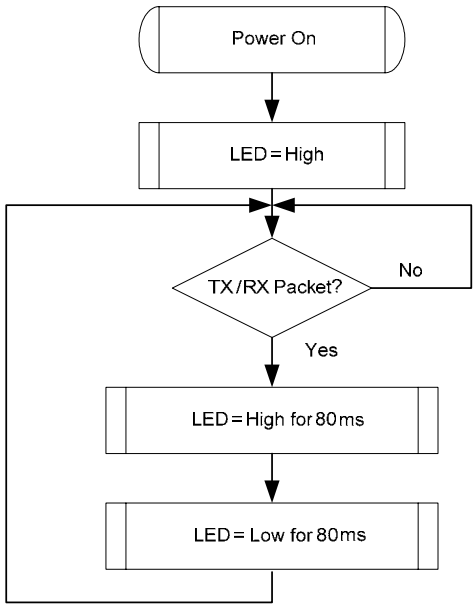


Figure 4. TX/RX LED

6.2.5. LINK/ACT LED

In 10/100M mode, blinking of the LINK/ACT LED indicates that the RTL8105E is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

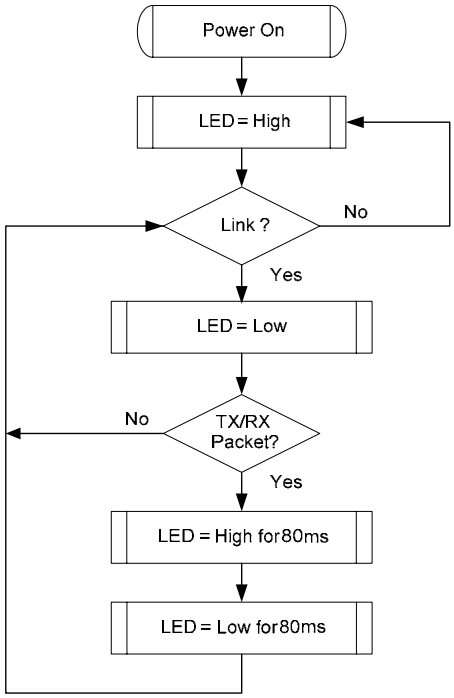


Figure 5. LINK/ACT LED

6.2.6. Customizable LED Configuration

The RTL8105E supports customizable LED operation modes via IO register offset 18h~19h. Table 12 describes the different LED actions.

Table 12. RTL8105E LED Select (IO Register Offset 18h~19h)

Bit	Symbol	RW	Description
15:12	LEDSEL3	RW	LED Select for PINLED3
11:8	Reserved	-	Reserved
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

1. Set IO register offset 0x55 bit 6 to 1b to enable the customized LED function

2. Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x80A1h (1000000010100001b), the LED actions are:

- LED 0: On only in 10M mode, with no blinking during TX/RX
- LED 1: On only in 100M mode, with TX/RX blinking
- LED 3: Blinking only during TX/RX at all speed

Table 13. Customized LEDs

	LINK		ACT
Speed	Link 10M	Link 100M	-
LED 0	Bit 0	Bit 1	Bit 3
LED 1	Bit 4	Bit 5	Bit 7
Not Defined	Bit 8	Bit 9	Bit 11
LED 3	Bit 12	Bit 13	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK + ACT

Note1: ACT means blinking TX and RX. LINK indicates Link 10M and Link 100M.
Note2: There are four special modes:
Mode A: LED OFF Mode → Set all bits to 0
Mode B: Full Duplex Mode → Set LED 0=0, and either LED 1 or LED 3 >0
LED 0=Full Duplex
LED 1=Follow Customized LED rule
LED 3=Follow Customized LED rule
Mode C: Separated TX/RX LED Mode → Set LED 0=0, LED 1=0, LED 3=1
LED 0=TX
LED 1=RX
LED 3=LINK
Mode D: Separated Speed ACT Mode → Set LED 0=0, LED 1=1, LED 3=1
LED 0=10ACT
LED 1=100ACT
LED 3=OFF

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8105E operates at 10/100M over standard CAT.5 UTP cable (100Mbps), or CAT.3 UTP cable (10Mbps).

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.4. EEPROM Interface

The RTL8105E requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM. The EEPROM interface permits the RTL8105E to read from, and write data to, an external serial EEPROM device.

Values in the internal eFUSE memory or external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8105E will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8105E initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The EEPROM interface consists of EESK, EECS, EEDO, and EEDI.

The correct EEPROM (i.e., 93C46) must be used in order to ensure proper LAN function.

Table 14. EEPROM Interface

EEPROM	Description
EECS	93C46 Chip Select.
EESK	EEPROM Serial Data Clock.
EEDI	Output to Serial Data Input Pin of EEPROM.
EEDO	Output Data Bus.

6.5. Power Management

The RTL8105E complies with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8105E can monitor the network for a Wakeup Frame or a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or the LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8105E is in power down mode (D1~D3):

- The RX state machine is stopped. The RTL8105E monitors the network for wakeup events such as a Magic Packet and Wakeup Frame in order to wake up the system. When in power down mode, the RTL8105E will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8105E.
- Transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held.
- After being restored to D0 state, the RTL8105E transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The $D3_{cold}$_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 FF, then PCI PMC = C3 FF)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 FF, then PCI PMC = 03 7E)

In the above case, if wakeup support is desired when main power is off, we suggest that the EEPROM PMC be set to C3 FF (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 7F, then PCI PMC = C3 7F)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 7F, then PCI PMC = 03 7E)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 7E.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8105E, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8105E.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8105E, e.g., a broadcast, multicast, or unicast address to the current RTL8105E.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8105E is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8105E supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^{5}+1$.

The corresponding wake-up method (message or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8105E may assert the corresponding wake-up method (message or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15~11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8105E to stop asserting the corresponding wake-up method (message or LANWAKEB) (if enabled).

When the RTL8105E is in power down mode, e.g., D1~D3, the IO, and MEM accesses to the RTL8105E are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.6. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8105E's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46 has completed or not.

Write VPD register: (write data to the 93C46):
Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8105E, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46):
Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8105E, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.3 Specifications for further information.

Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.

Note4: The VPD function of the RTL8105E is designed to be able to access the full range of the 93C46 EEPROM.

6.7. Receive-Side Scaling (RSS)

The RTL8105E complies with the Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi-CPU platforms.

6.7.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8105E that it should store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port.
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address *(Note: The RTL8105E does not support the IPv6 extension header hash type in RSS).*

Hash Bits

Hash bits are used to index the hash result into the indirection table.

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.7.2. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It is an entity that maintains network presence for a sleeping higher power host. It prevents spurious wake up and further reduces power consumption. It maintains connectivity while hosts are asleep, including responding to requests from other nodes on the network, ignoring packets, generating packets while in the sleep state, and intelligently waking up host systems.

6.7.3. RSS Operation

After the parameters are set, the RTL8105E will start hash calculations on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8105E uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

6.8. Energy Efficient Ethernet (EEE)

The RTL8105E supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps and 100Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

7. Switching Regulator

The RTL8105E incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.05V output pin (REGOUT) must be connected only to DVDD10, AVDD10, and EVDD10 (do not provide this power source to other devices).

Note: Refer to the separate RTL8105E Layout Guide for details.

8. LDO Regulator (RTL8105E-VC Only)

The RTL8105E-VC incorporates a linear Low-Dropout (LDO) regulator that features high power supply ripple rejection and low output noise. The RTL8105E-VC embedded LDO regulator does not require power inductors on the PCB; only a 1.14V output capacitor between its 1.14V output and analog ground for phase compensation, which saves cost and PCB real estate. Use a X5R low-ESR ceramic capacitor, with a capacitance of at least 1µF, to enhance output voltage stability.

Note: AVDD10 1.05V output when used with Linear Regulator (LDO) is 1.14V.

The output capacitors (and bypass capacitors) should be placed as close as possible to the power pins (AVDD10, DVDD10, EVDD10) for adequate filtering. The switching regulator output/input pins (REGOUT/VDDREG) are floating when operating in LDO mode.

Note that with regard to voltage conversion efficiency, LDO is inferior to a switching regulator. This balance between cost, size, and efficiency should be taken into consideration when choosing the regulator type.

Note: The embedded LDO is designed for RTL8105E-VC internal use only. Do not provide this power source to other devices.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 15. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
DVDD33, AVDD33	Supply Voltage 3.3V	-0.3	3.63	V
DVDD10, AVDD10, EVDD10	Supply Voltage 1.05V*	-0.05	1.32	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	-0.3	3.63	V
1.05V DCinput 1.05V DCoutput	Input Voltage Output Voltage	-0.05	1.32	V
N/A	Storage Temperature	-55	+125	°C

Note: '' instates AVDD10 1.05V output when used with Linear Regulator (LDO) is 1.14V.*

9.2. Recommended Operating Conditions

Table 16. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	3.14	3.30	3.46	V
	DVDD10, AVDD10, EVDD10	1.00	1.05	1.10	V
		1.09	1.14*	1.19	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note1: '' instates AVDD10 1.05V output when used with Linear Regulator (LDO) is 1.14V.*

9.3. Electrostatic Discharge Performance

Table 17. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: |4KV|
MM ESD	All Pins: |200V|
CDM ESD	All Pins: |1000V|
Cable ESD*	All MDI Pins: |6KV|
	All Pairs: |12KV|
Latch Up	I/O Pins: |300mA| Power Pins: 1.5×VDD

Note: 'All MDI pins' means the ESD current is introduced to each MDI pin separately. 'All pairs' means the ESD current is introduced to the aggregated MDI pairs.

9.4. Crystal Requirements

Table 18. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.	-	25	-	MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
Jitter	Broadband Peak-to-Peak Jitter[2]	-	-	200	ps
DL	Drive Level.	-	-	0.3	mW

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

9.5. Oscillator Requirements

Table 19. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[2]	-	-	-	200	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

9.6. Thermal Characteristics

Table 20. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

9.7. DC Characteristics

Table 21. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
DVDD33, AVDD33	3.3V Supply Voltage	-	3.14	3.30	3.46	V
DVDD10, AVDD10*, EVDD10	1.05V Supply Voltage	-	1.00	1.05	1.10	V
	1.14V Supply Voltage	-	1.09	1.14	1.19	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage	-	2.0	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc33	Average Operating Supply Current from 3.3V	At 100Mbps with heavy network traffic	-	30	-	mA
Icc10	Average Operating Supply Current from 1.05V	At 100Mbps with heavy network traffic	-	120	-	mA

Note1: '' instates AVDD10 1.05V output when used with Linear Regulator (LDO) is 1.14V.*
Note2: Refer to the latest schematic circuit for correct configuration.
Note3: All Supply Voltage power noise <±5% of Supply Voltage.

9.8. AC Characteristics

9.8.1. Serial EEPROM Interface Timing

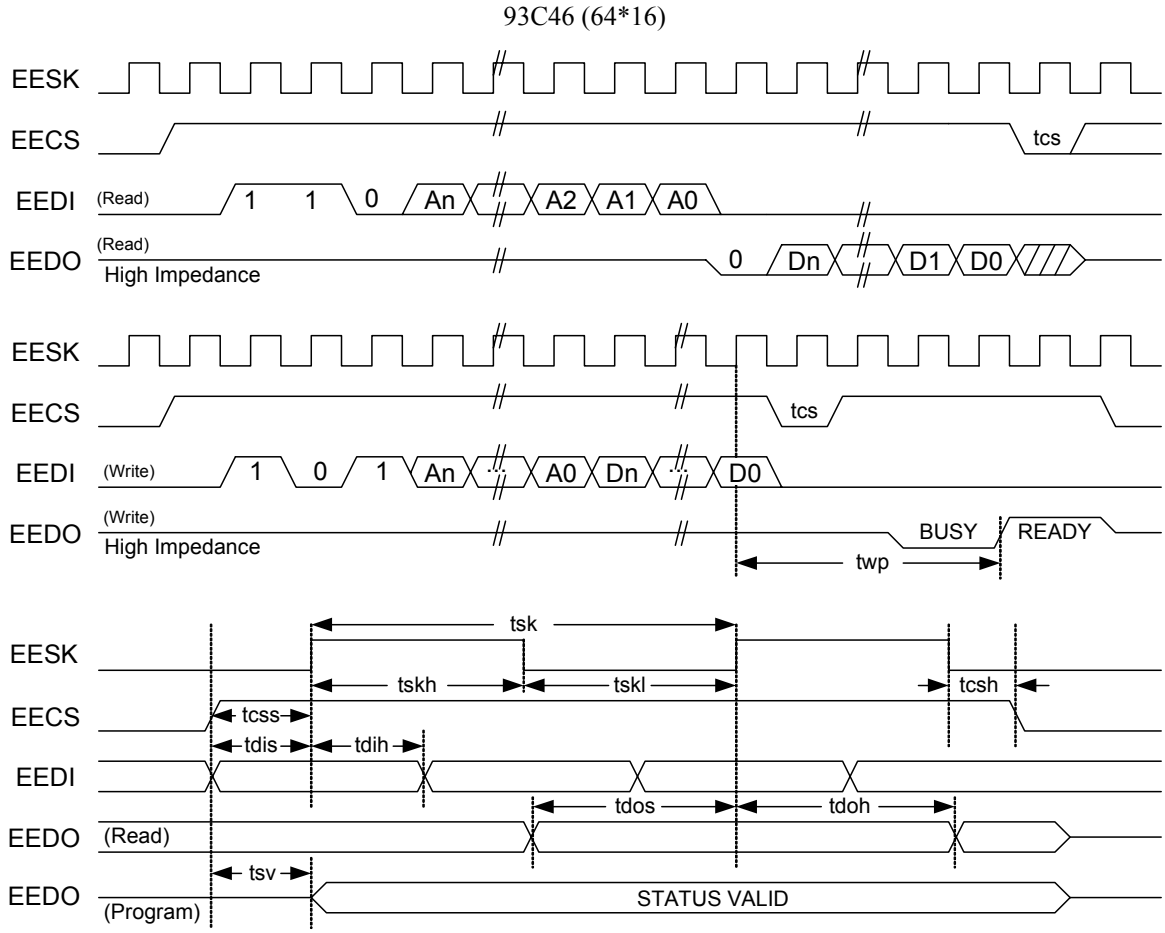


Figure 6. Serial EEPROM Interface Timing

Table 22. EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346	1000	-	ns
twp	Write Cycle Time	9346	-	10	ms
tsk	SK Clock Cycle Time	9346	4	-	µs
tskh	SK High Time	9346	1000	-	ns
tskl	SK Low Time	9346	1000	-	ns
tcss	CS Setup Time	9346	200	-	ns
tcsh	CS Hold Time	9346	0	-	ns
tdis	DI Setup Time	9346	400	-	ns
tdih	DI Hold Time	9346	400	-	ns
tdos	DO Setup Time	9346	2000	-	ns
tdoh	DO Hold Time	9346	-	2000	ns
tsv	CS to Status Valid	9346	-	1000	ns

9.9. PCI Express Bus Parameters

9.9.1. Differential Transmitter Parameters

Table 23. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.05	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

9.9.2. Differential Receiver Parameters

Table 24. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.05	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between The Jitter Median and Maximum Deviation from The Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

9.9.3. REFCLK Parameters

Table 25. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 10, page 29.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 7, page 28.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 7, page 28.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 9, page 28.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 7, page 28.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 7, page 28.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 7, page 28.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 13, page 30. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range. See Figure 12, page 29.

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8, page 28.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

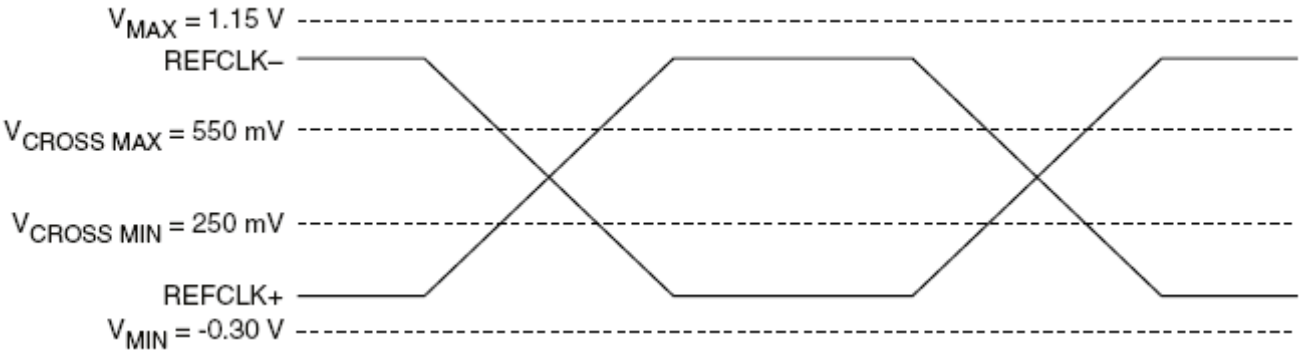


Figure 7. Single-Ended Measurement Points for Absolute Cross Point and Swing

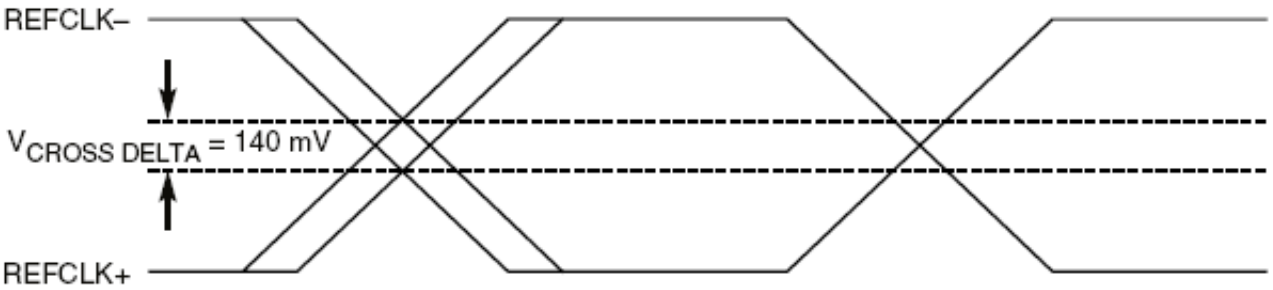


Figure 8. Single-Ended Measurement Points for Delta Cross Point

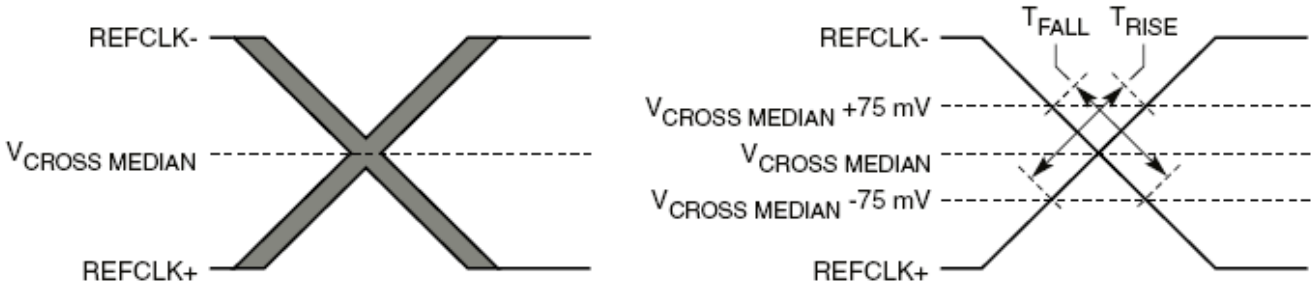


Figure 9. Single-Ended Measurement Points for Rise and Fall Time Matching

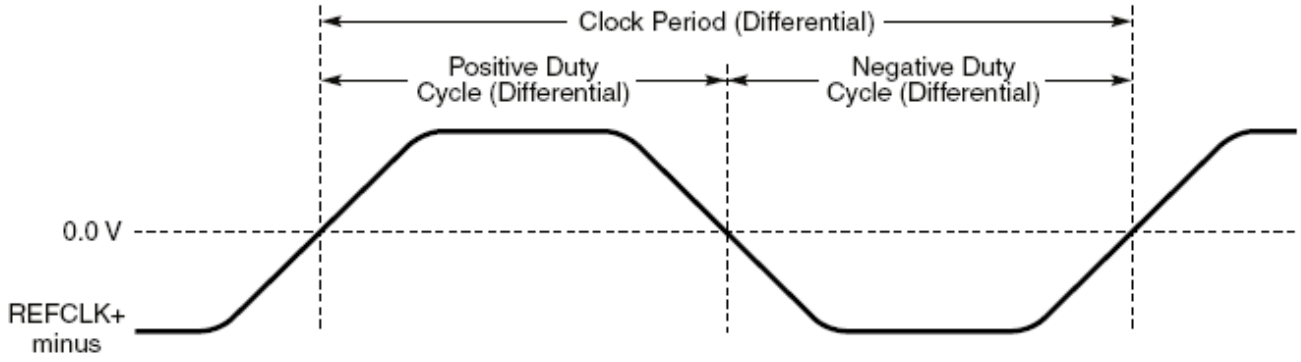


Figure 10. Differential Measurement Points for Duty Cycle and Period

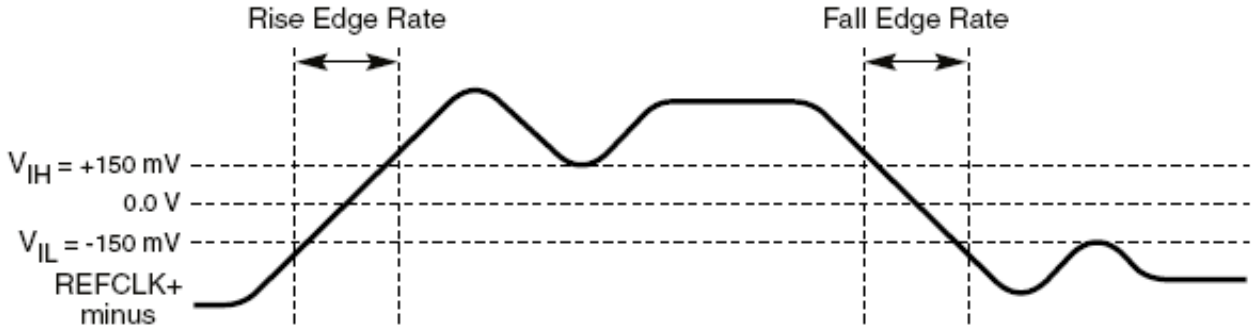


Figure 11. Differential Measurement Points for Rise and Fall Time

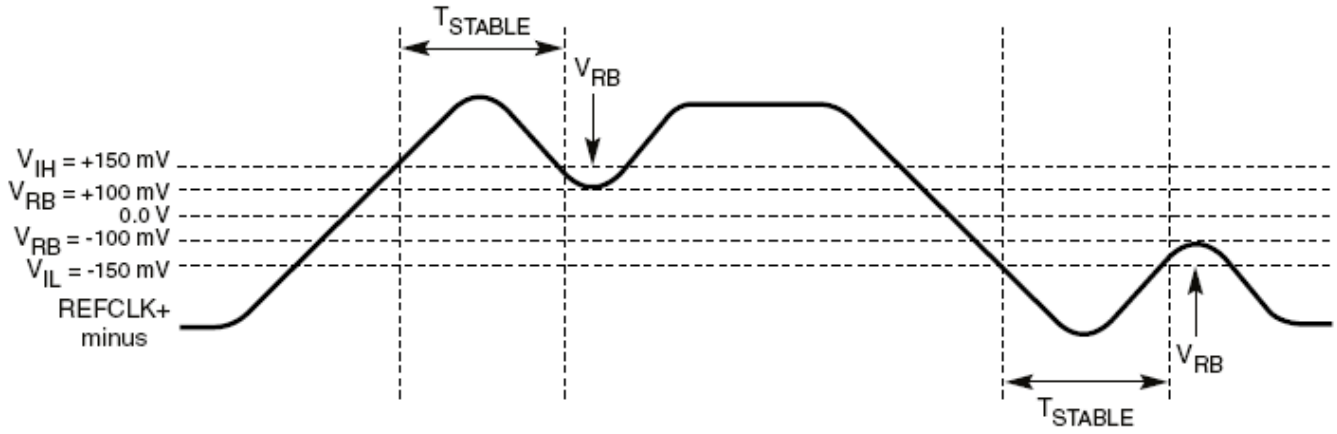


Figure 12. Differential Measurement Points for Ringback

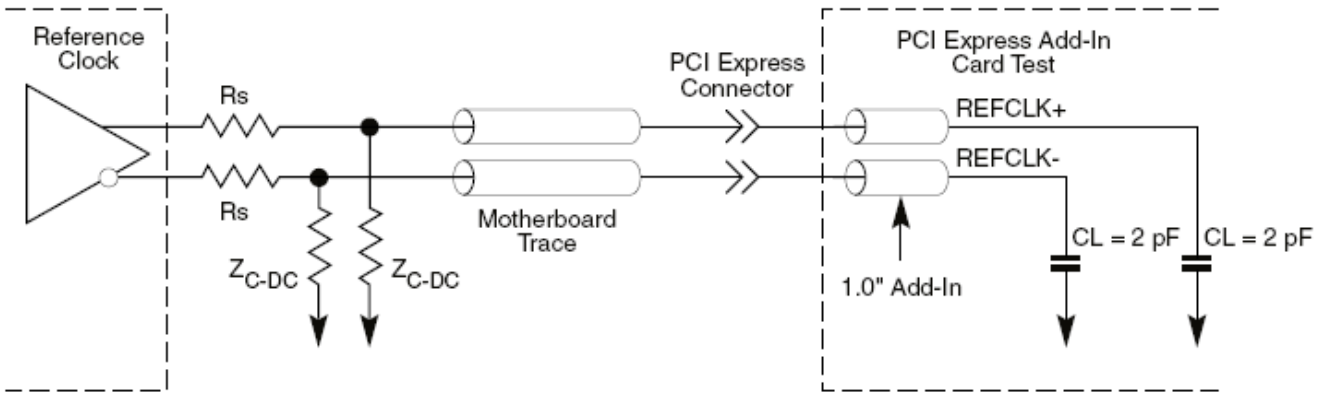


Figure 13. Reference Clock System Measurement Point and Loading

9.9.4. Auxiliary Signal Timing Parameters

Table 26. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
T_{FAIL}*	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{WKRF}	LANWAKEB Rise – Fall Time	-	100	ns
T_{PWRON}	3.3V Power On Time	1	-	ms

Note: T_{FAIL} means 500 ns from the power rail exceeds specifications (exceeds the specified tolerance by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.

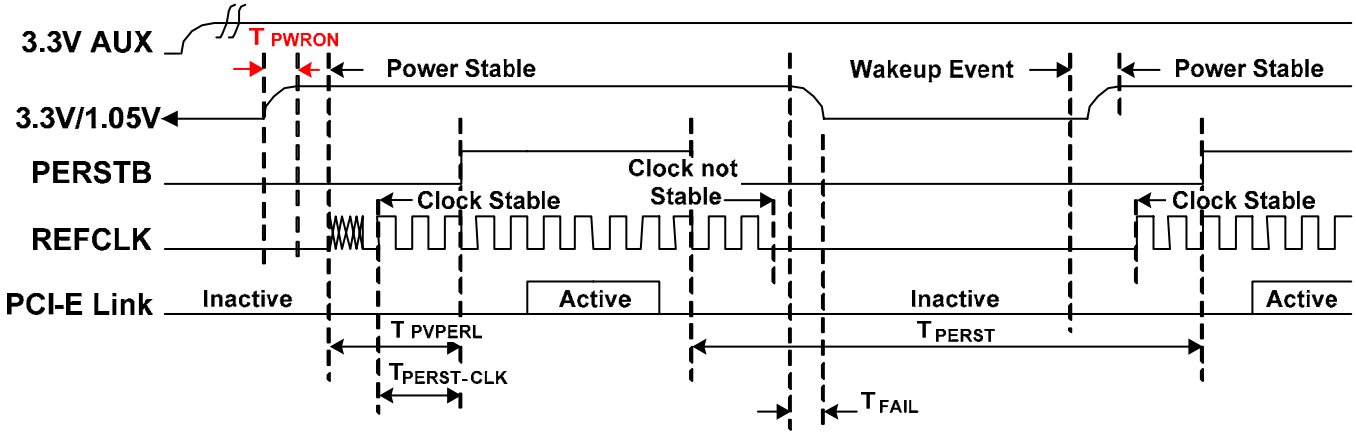
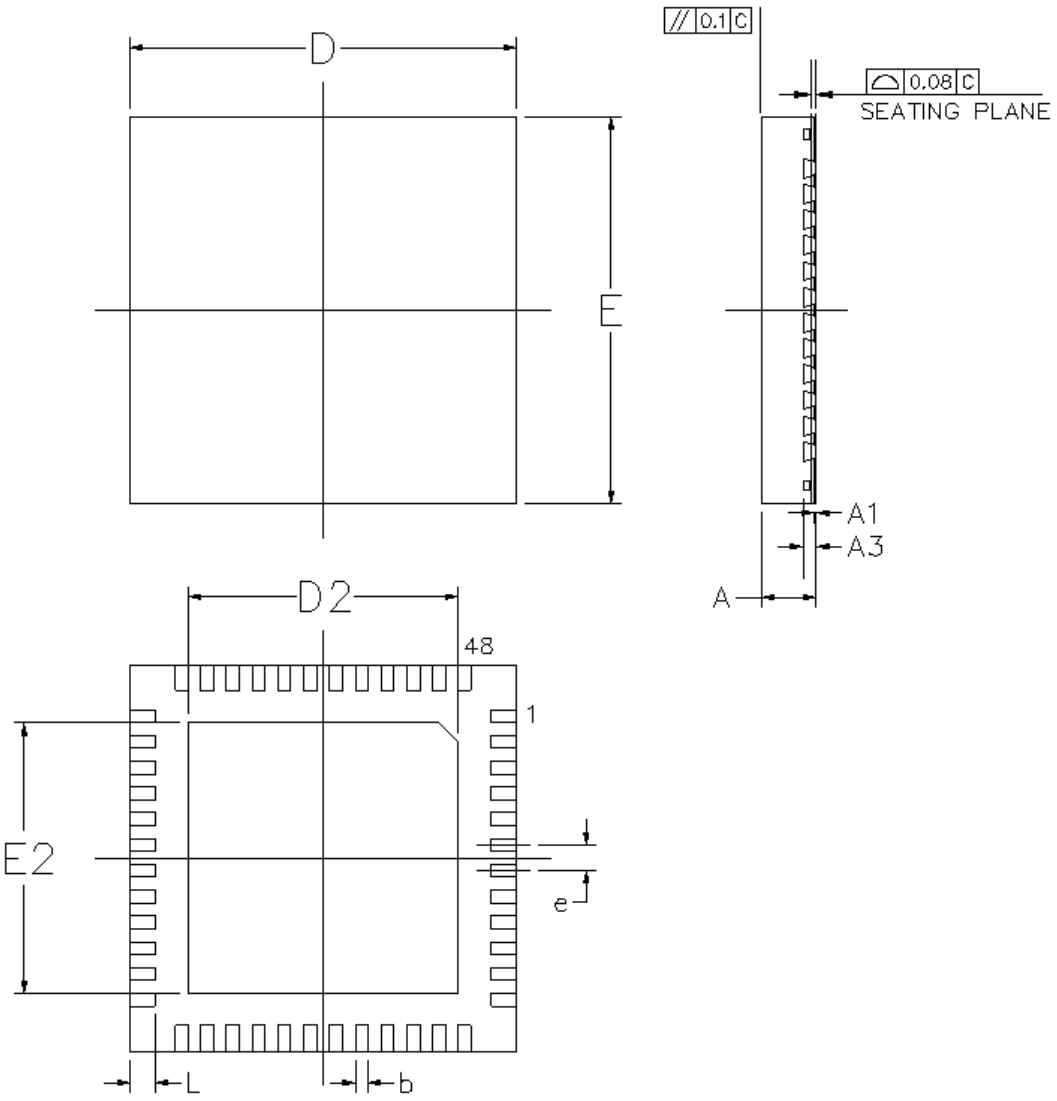


Figure 14. Auxiliary Signal Timing

10. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 27. Ordering Information

Part Number	Package	Status
RTL8105E-VB-GR	48-Pin QFN 'Green' Package (with EEPROM interface and switching regulator)	Mass Production
RTL8105E-VC-GR	48-Pin QFN 'Green' Package (with EEPROM interface, switching regulator, and LDO)	Mass Production

Note: See page 4 for package identification information.

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