RTL930x Power Sequence Note

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when use RTL930x Single Chip .Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2017/1/23	First release.

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1. RTL930x Power Sequence Description

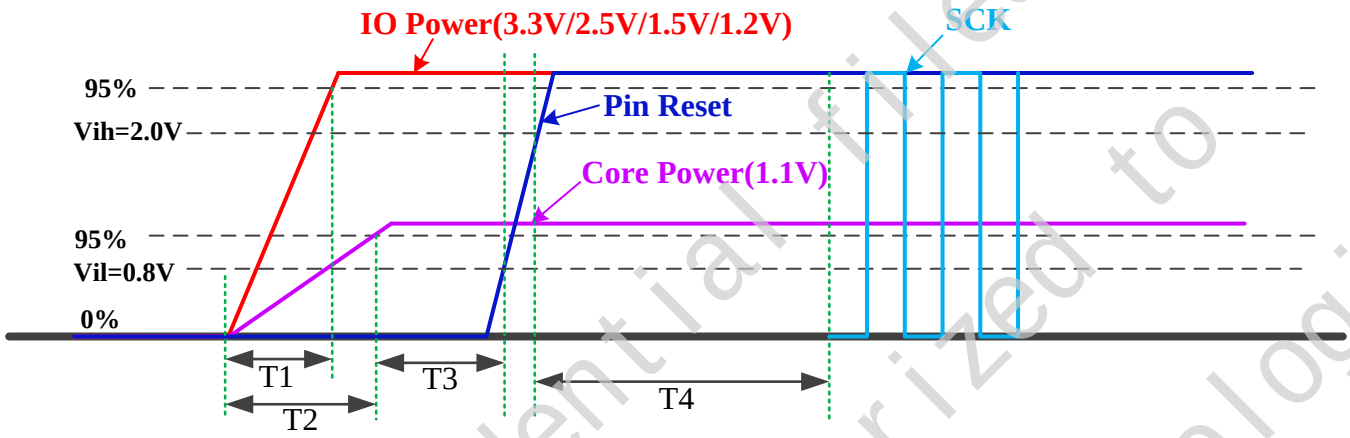

Figure 1. RTL930x power sequence

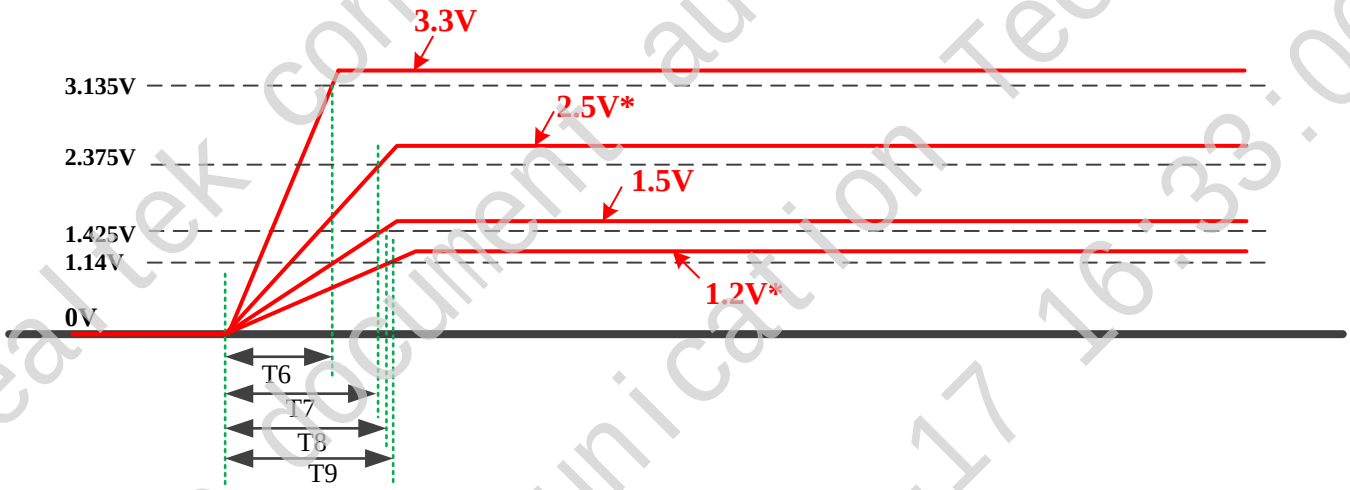

Figure 2. IO Powers sequence

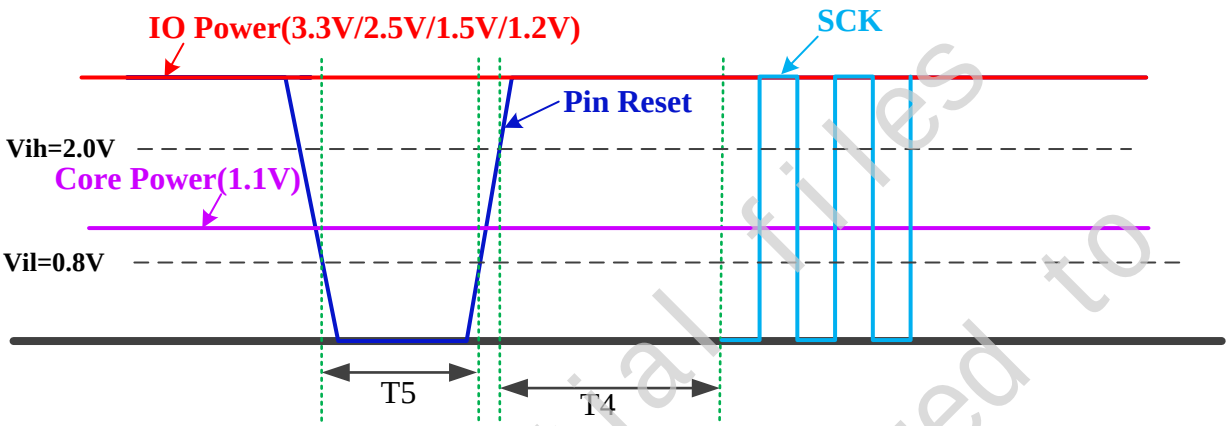

Figure 3. Pin reset sequence triggered by manual or watchdog

Table 1. Power and Reset Characteristics

Parameter	SYM	Min	Typical	Max	Units
IO powers rising settling time (0% to 95%).	T1	0.5	-	100	ms
3.3V IO powers rising settling time (0% to 95%).	T6	0.5	-	100	ms
2.5V IO powers rising settling time (0% to 95%). Optional for 2.5V GPIO application.	T7	0.5	-	100	ms
1.5V IO powers rising settling time (0% to 95%).	T8	0.5	-	100	ms
1.2V IO powers rising settling time (0% to 95%). Optional for Clause 45 MDIO interface application.	T9	0.5	-	100	ms
1.1V Core Power rising settling time (0% to 95%).	T2	0.5	-	100	ms
Pin reset staying active time after both the IO and core powers are stable.	T3	10	-	-	ms
The time from pin reset de-active state to that external device start to initialize RTL930x switch core through I2C/SPI slave interface.	T4	100	-	-	ms
Pin reset staying active time when triggered by manual or watchdog.	T5	10	-	-	ms

Note:

1) 'IO power' includes DVDDH, DVDDIO_Gx (x=0,1,2,3), DVDD_MDXx (x=0,1,2,3), AVDDH_USB, AVDDH_PLLx (x=0,1,2), AVDDH_CEN, AVDDH_XTAL, SVDDH and MDVDDH. There's no requirement for these different IO powers (3.3V/2.5V/1.5V/1.2V) to be stable at the same time. For a successful power-up sequence, RealTek recommends that |Tm-Tn| < 20ms（m =6, 7, 8, 9, n = 6, 7, 8, 9, m ≠ n）.
2) 'Core power' includes SVDDL，AVDDL_USB， AVDDL_DLL，AVDDL_CK， AVDDL_PLLx (x=0,1,2)，AVDDL_CEN and DVDDL. These 1.1V powers should be stable at the same time.
3) There's no requirement for the IO powers and core powers to be stable at the same time. For a successful power-up sequence, RealTek recommend that |T1-T2| < 20ms.

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