

REALTEK

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RTL9075AAD, RTL9072AAD

RTL9068AAD, RTL9068ABD

RTL9054AN

SINGLE-CHIP AUTOMOTIVE ETHERNET SWITCH CONTROLLER WITH 100BASE- T1/1000BASE-T1 TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

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- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2020/12/24	First release.
1.1	2021/01/29	Revised section 9.4 Power Dissipation, page 183. Removed redundant data. Corrected minor typing errors.
1.2	2021/04/27	Revised Figure 15 RTL9054AN Pin Assignments, Page 14 Revised Table 6 SGMII Pins, Page 17. Revised Table 26 Power Controller Pins, Page 59. Revised Table 27 Configuration Strapping Pins, Page 60 (Pin GPIOF [3:0]). Revised Table 30 Other Pins, Page 66. Revised Figure 29 MDC/MDIO Read Operation Timing, page 79. Revised Figure 30 MDC/MDIO Write Operation Timing, page 79. Revised Table 53 MIB per Port Counter List, Page 132. Revised Table 54 MIB System Counter List, Page 138. Revised Table 73 SGMII Differential Receiver Characteristics, Page 192 (R_Y2). Revised Table 75 HSGMII Differential Receiver Characteristics, Page 194(R_Y2). Added Note 3 To Sections 11.1.1, 11.1.2, 11.2.1 And 11.2.2. Corrected Minor Typing Errors.
1.3	2021/06/18	Revised section 2 Features, page 2. Revised section 4 System Applications, page 6. Revised Figure 15 RTL9054AN Pin Assignments, page 14. Added the RTL9068ABD-VA1, which does not support PCI-E. Revised Table 28 Power and GND Pins, page 62. Revised section 8.1 Power Sequence, page 87. Revised section 8.22 Under Voltage & Over Temperature, page 143 (added V33). Revised section 8.23.1 Operating Modes, page 144 (added V33). Revised section 8.23.2 Operating Mode Transition, page 147 (added RTL9054: Under voltage on V33 pin). Revised section 8.34.1 Layer 2/3/4 Malicious Packet Filter, page 178. Revised Table 62 Absolute Maximum Ratings, page 179. Revised Table 63 Recommended Operating Range, page 180 (added V33). Revised Table 64 DC Characteristics, page 181. Revised section 9.9 PCI Express Bus Parameters, page 201. Revised section 12 Ordering Information, page 212. Corrected Minor Typing Errors.

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1. General Description

The RTL9054AN/RTL9068AAD/RTL9068ABD/RTL9075AAD/RTL9072AAD (hereafter referred to as the RTL9054/RTL9068/RTL907x) is an automotive Ethernet switch controller with eight integrated 100BASE-T1 PHY transceivers, and two 1000BASE-T1/100BASE-T1 combo PHY transceivers. The RTL9054/RTL9068/RTL907X supports RGMII/(R)MII/SGMII/HSGMII/USXGMII/PCI-E3.0 interfaces to provide access via an external CPU or to cascade switches.

The RTL9054/RTL9068/RTL907x can smoothly forward Ethernet traffic between the Fast Ethernet (FE), RGMII/RMII, 100BASE-T1, 1000BASE-T1, PCI-E, HSGMII, and USXGMII ports at wire speed. All MAC functions, VLAN, QoS, etc., are equally applied to all ports. The RTL9054/RTL9068/RTL907x is ideal for applications such as Advanced Driver Assistance Systems (ADAS), infotainment systems and gateway.

The RTL9054/RTL9068/RTL907x is AEC Q100 grade 2 qualified. It features an embedded ARM Based CPU Real-M500 CPU to execute programs in the internal ROM or external SPI flash. With an embedded Real-M500 and internal memory controller, the RTL9054/RTL9068/RTL907x supports IGMP snooping and Rapid Spanning Tree Protocol (RSTP) functions without any additional external CPU loading and MLD snooping hardware.

The RTL9054/RTL9068/RTL907x provides a 4K-entry table with a 8-way hash algorithm and 256-entry CAM for layer-2 MAC address learning and searching, and a 128-entry IGMP Group table with a 8-way hash table for IP multicast forwarding.

With eight physical queues in each port, the RTL9054/RTL9068/RTL907x provides four types of packet scheduling, including SP (Strict Priority), WRR (Weighted Round Robin), WFQ (Weighted Fair Queuing) and IEEE 802.1-Qav specified Credit-Based Shaper (CBS) for Ethernet AV. Per-port ingress/egress bandwidth control and per-port/per-queue egress bandwidth control are supported. The RTL9054/RTL9068/RTL907x supports Time-Sensitive Networking (TSN) such as IEEE 802.1 AS-REV, IEEE 802.1Qbv, and IEEE 802.1Qci.

The RTL9054/RTL9068/RTL907x supports a 512-entry Access Control List (ACL) that parses various protocol packet types and performs configurable actions, e.g. Permit/Drop, redirect, and traffic policing.

The RTL9054/RTL9068/RTL907x provides an Embedded Security Module (ESM) for secure boot and authentication.

The RTL9054/RTL9068/RTL907x supports OPEN Alliance TC10 sleep and wake-up and is compliant with TC11 switch requirements.

2. Features

- Interfaces
 - ◆ Integrates eight 100BASE-T1 PHYs
 - ◆ Integrates two 1000BASE-T1/100BASE-T1 combo PHYs
 - ◆ 100BASE-TX for diagnostics
 - ◆ Two USXGMII interfaces for uplink and stacking/cascading switch
 - ◆ Two PCI-E 3.0 interfaces
 - ◆ Two HSGMII
 - ◆ Four SGMII
 - ◆ Three RGMII/(R)MII
 - ◆ I2C slave, SPI slave, MDC/MDIO slave and Ethernet interface for external CPU access
 - ◆ SPI flash interface
 - ◆ MDC/MDIO master mode for external PHY access
 - ◆ GPIO and parallel LED
- OPEN Alliance TC10 sleep and wake-up compliant
- OPEN Alliance TC11 Switch requirements compliant
- Link aggregation (IEEE 802.1ax) for 2 groups of link aggregators with up to 2/3 port per-group
- Layer2 Address Lookup
 - ◆ High performance wire-speed layer-2 forwarding
 - ◆ IVL, SVL, IVL/SVL
 - ◆ 4K 8-way lookup engine and 256-entry CAM
 - ◆ Static entry
- Source MAC blocking/Destination MAC blocking
- Aging time from 0.01s to 1757497s
- Embedded Regulator
 - ◆ Three individual 2.5V and 1.8V LDOs for three RGMII/(R)MII interfaces
 - ◆ Switching regulator (core power) for power saving
- VLAN
 - ◆ Port based and Tag-based VLAN
 - ◆ 4096 VLAN entries
 - ◆ Supports 802.1ad or Q-in-Q
 - ◆ VLAN translation for ingress
 - ◆ Ingress and Egress VLAN retagging
- Loop Detection and Prevention
 - ◆ Supports 802.1d/1s/1w
 - ◆ 15 spanning tree instances
 - ◆ Supports RSTP without extra loading on the external CPU
- IGMP/MLD Snooping
 - ◆ Supports IGMP v1/v2/v3 (include/exclude mode) snooping without extra loading on the external CPU
 - ◆ 128-entry IGMP Group Table, 8-way hash
 - ◆ Supports MLD v1 snooping hardware

- Cyber Security
 - ◆ Secure boot
 - ◆ Hardware cipher engine: AES256, RSA2048/3072
 - ◆ Hardware hash engine: SHA-1, MD5, SHA-1 and SHA-256
 - ◆ OTP: Key storing
 - ◆ True random number generator
- Performance
 - ◆ Very low Electro-Magnetic Emission (EMC)
 - ◆ HBM ESD protection level
 - $\pm 6\text{kV}$ for MDI and global pins (Global pins: VBAT, WAKE)
 - $\pm 2\text{kV}$ for other pins
 - ◆ IEC 61000-4-2 ESD protection level:
 - ◆ Meet AEC-Q100 Grade 2 (-40 ~ 105°C)
 - ◆ MDI pins are tolerant of transient conditions according to ISO 7637 Class C
 - ◆ Supports 15m for single-pair cable
 - ◆ Baseline Wander Correction feature
 - ◆ Echo Cancellation mechanism
- Automotive Compliant
 - ◆ Under-voltage detection
 - ◆ Over-temperature detection
 - ◆ Ready to transmit and receive packets within 100ms after power stable
- Cable Diagnostics (RTCT)
 - ◆ Detects open/short status, and length of the cable (resolution: ± 1 meter)
 - ◆ Indicates status via the LED pin
- IEEE 802.1X
 - ◆ Port-based IEEE 802.1X
- Port Mirror
 - ◆ TX and RX mirror
 - ◆ Good packet, bad packet, unicast packet, multicast and broadcast packet mirror filter, drop packet mirror filter
 - ◆ Original packet mirror and modified packet mirror
 - ◆ ACL based flow mirror
- Storm Suppression
 - ◆ Supports broadcast, multicast unknown unicast, unknown multicast storm filter
- Access Control List (ACL)
 - ◆ Supports 512-entry ACL
 - ◆ Supports MAC, LLC, ARP, TCP, UDP, ICMP, IGMP
 - ◆ Supports per-flow traffic policing
 - ◆ Supports VID range/IPv4 range/layer4 port range/source port mask/packet length range checking
- IP Routing
 - ◆ Supports 64-entry L3 interface
 - ◆ Supports 256-entry Network Route
 - ◆ 4K IPv6 Unicast L3 host table (shared with IPv4)
 - ◆ 12K IPv4 Unicast L3 host table (shared with IPv6)
 - ◆ 2K IPv6 Multicast L3 host table (shared with IPv4)
 - ◆ 4K IPv4 Multicast L3 host table (shared with IPv6)

- QoS
 - ◆ Supports 8 priority queues
 - ◆ Supports min-max scheduling
 - ◆ Supports Strict Priority/WRR/WFQ scheduling algorithm
 - ◆ Supports Credit-Based Shaper (CBS)
 - ◆ Supports input bandwidth control from 8Kbps to 1Gbps by step 8kbps
- Time-Sensitive Networking (TSN)
 - ◆ IEEE Std 802.1AS-Rev
 - ◆ IEEE Std 802.1Qbv
 - ◆ IEEE Std 802.1Qci
- Packet Modifier
 - ◆ Add, modify, or remove outer-tag and/or inner-tag
 - ◆ Modify IP TOS field
 - ◆ L2 Checksum recalculation
- Port Isolation
 - ◆ Provides traffic isolation between different physical ports
- MIB
 - ◆ MIB-II and interface MIB (RFC 1213 & 2863)
 - ◆ Ethernet-like MIB (RFC 3635)
 - ◆ RMON (RFC 1757)
 - ◆ Bridge MIB (RFC 4188)
- Stacking
 - ◆ Supports 4 RTL9068/RTL907x switches stackable for single management
 - ◆ Stacking boot
- PCIE Function
- VLAN / Layer-3, Layer-4 checksum / TCP segmentation offload
- Supports SR-IOV, provides up to 7 virtual functions
- ARM Base CPU Real-M500
 - ◆ CPU clock runs at 333Mhz for different protocols and applications
 - ◆ Implements the IEEE 802.1AS-Rev protocol stack, IEEE 802.1X, IGMP/MLD Snooping, SNMP, LACP, Security, RSTP and Safety function
- Functional Safety
 - QM level at the time of writing, target level: ISO 26262 ASIL-B
 - ◆ Under-voltage detection
 - ◆ Over-temperature detection
 - ◆ SRAM ECC
 - ◆ DISB pin to disable the switch transmission
- Process and Package
 - ◆ 28nm process
 - ◆ RTL9075AAD/RTL9072AAD/RTL9068 AAD LFBGA 20.2x20.2
 - ◆ RTL9068ABD/RTL9068ABD LFBGA 17.0x17.0
 - ◆ RTL9054AN LFBGA 20.2x20.2
- Attack Prevention
 - ◆ Supports layer 2, layer 3 and layer 4 malicious packet filter

3. Block Diagram

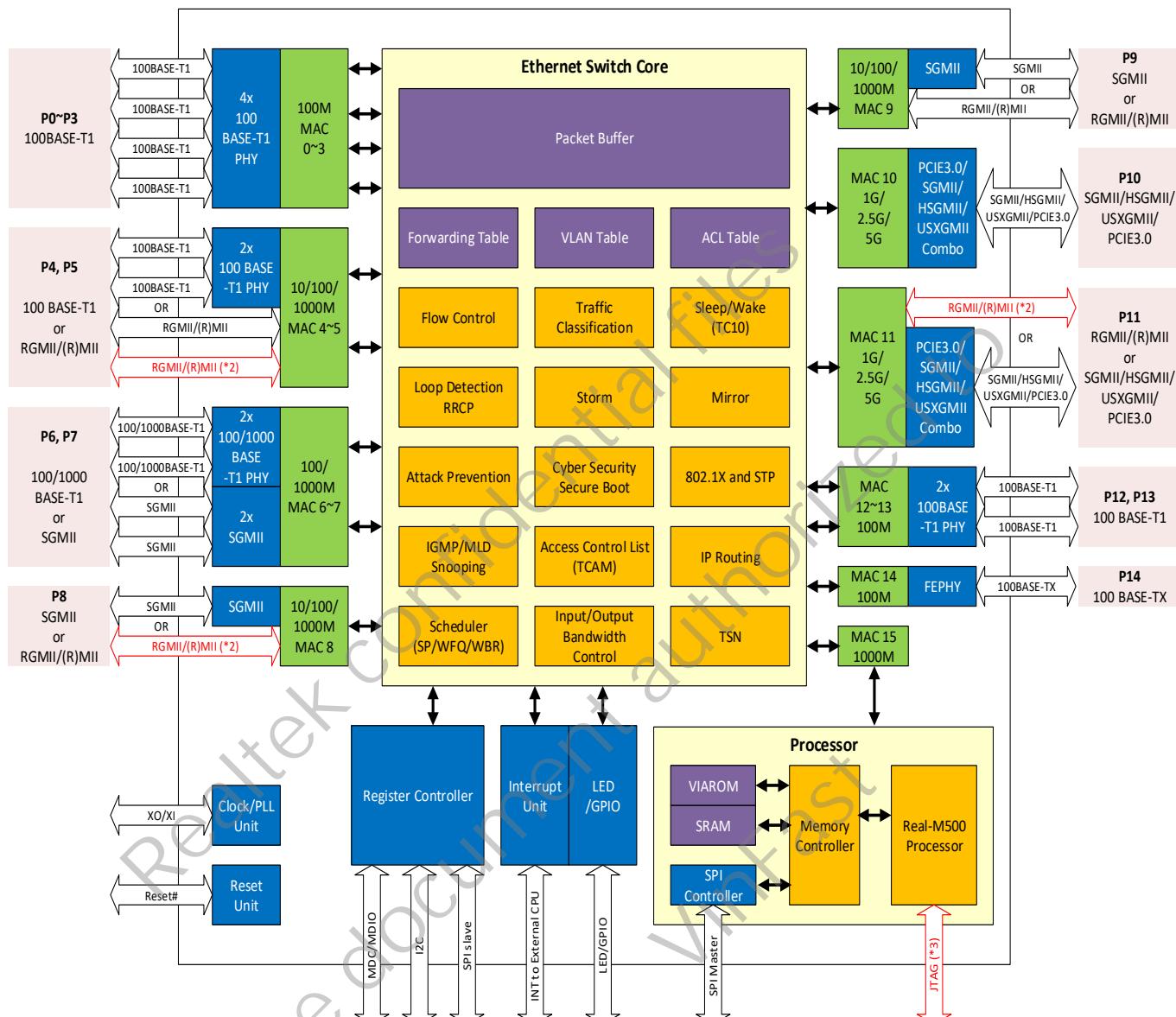


Figure 1. Block Diagram

Notes:

Note 1: Figure 1 shows the block diagram of RTL9075AAD, the other package port number refers to section 4.1.

Note 2: RGMII/(R)MII of port5, port8 and port11 are shared. Ex. If port11 is configured as RGMII/(R)MII interface, port5 can only be configured as 100BASE-T1 and port8 can only be configured as not an occupied interface. More details are shown in section 4.1.

Note 3: JTAG access is only for Realtek internal use, and not open to external users.

4. System Applications

4.1. Overview

The RTL9075AAD/RTL9072AAD (Figure 2 and Figure 3) offers 15/12 ports to connect the camera, sensor, diagnostics and SoCs. For greater flexibility configure ports 4 ~ 14 to the suite interface for a different endpoint.

When the vehicle is returned back to the dealer services center, the engineer gets OBD data through the diagnostic port (100BASE-TX port).

Port10/11 are designed for connecting with SoCs such as a head-end unit. The RTL9075AAD/RTL9072AAD offers PCI-E 3.0, USXGMII/HSGMII/SGMII, RGMII/(R)MII interfaces for the data path and offers a selection of the interfaces (SPI, I2C, MDC/MDIO) that are used for register access. The USXGMII can be used for cascade switch.

The RTL9068AAD/RTL9068ABD (Figure 4 and Figure 5) offers 8 ports to connect camera, sensor, diagnostic and SoCs. The RTL9054AN (Figure 6) offers 14 ports without a high speed interface. Table 1 shows the RTL9054/RTL9068/RTL907x family and port interface.

Table 1. RTL9054/RTL9068/RTL907x Family List

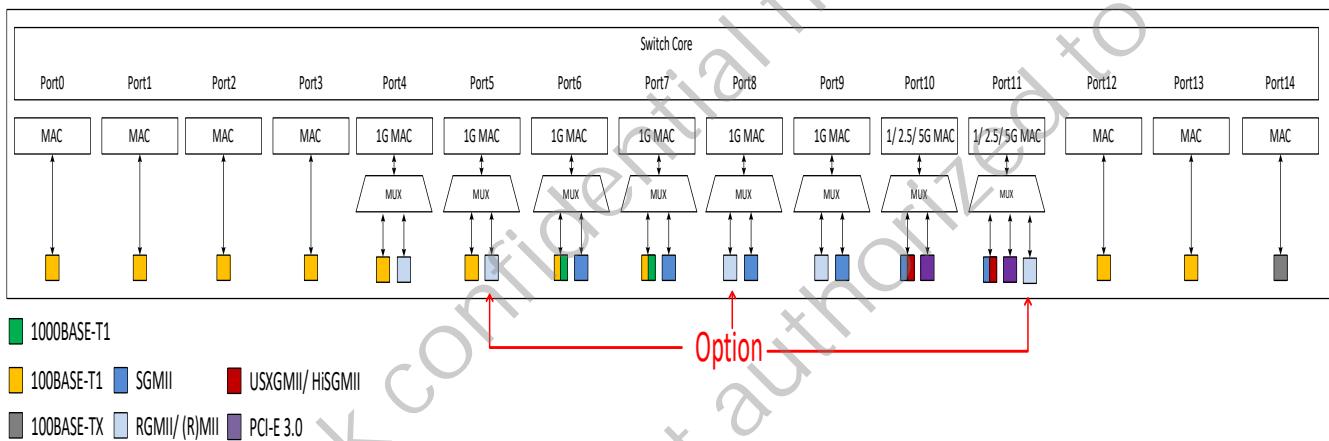
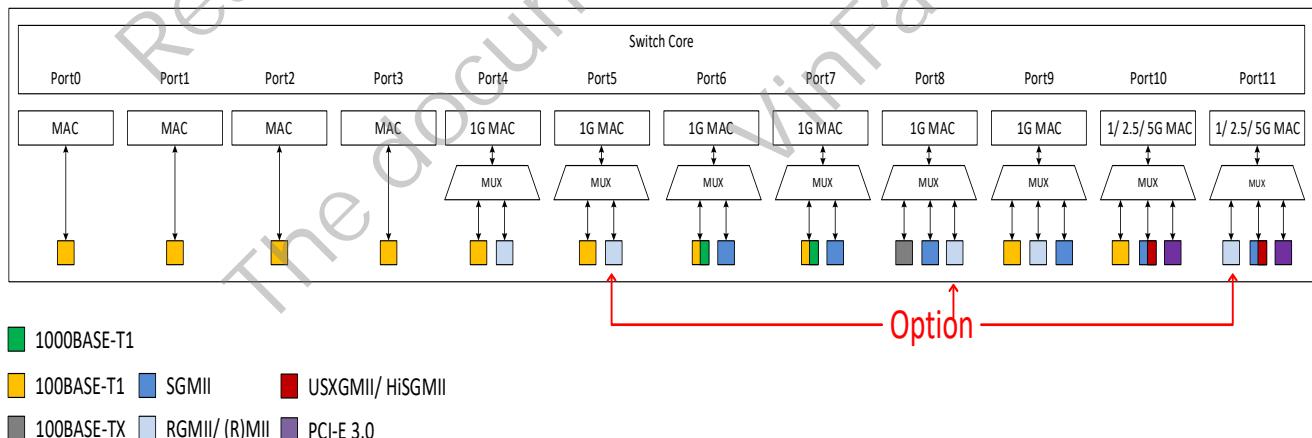
Product Name	Package	Description
RTL9075AAD	LFBGA 20.2x20.2x1.70	<p>Port 0 ~ 3: 100BASE-T1 PHY</p> <p>Port 4 ~ 5: 100BASE-T1 PHY or RGMII/MII/RMII</p> <p>Port 6 ~ 7: 100BASE-T1, 1000BASE-T1, or SGMII</p> <p>Port 8: SGMII or RGMII/MII/RMII</p> <p>Port 9: SGMII or RGMII/MII/RMII</p> <p>Port 10: SGMII, HSGMII, USXGMII, or PCI-E 3.0</p> <p>Port 11: RGMII/MII/RMII, SGMII, HSGMII, USXGMII or PCI-E 3.0</p> <p>Port 12: 100BASE-T1</p> <p>Port 13: 100BASE-T1</p> <p>Port 14: 100BASE-TX (Fast Ethernet)</p> <p><i>Note: Choose only one of P5, P8 or P11 as RGMII/MII/RMII port.</i></p>
RTL9072AAD	LFBGA 20.2x20.2x1.70	<p>Port 0 ~ 3: 100BASE-T1 PHY</p> <p>Port 4 ~ 5: 100BASE-T1 PHY or RGMII/MII/RMII</p> <p>Port 6 ~ 7: 100BASE-T1, 1000BASE-T1, or SGMII</p> <p>Port 8: 100BASE-TX (Fast Ethernet), SGMII, or RGMII/MII/RMII</p> <p>Port 9: 100BASE-T1, SGMII, or RGMII/MII/RMII</p> <p>Port 10: 100BASE-T1, SGMII, HSGMII, USXGMII, or PCI-E 3.0</p> <p>Port 11: RGMII/MII/RMII, SGMII, HSGMII, USXGMII, or PCI-E 3.0</p> <p><i>Note: Choose only one of P5, P8 or P11 as RGMII/MII/RMII's port.</i></p>

Product Name	Package	Description
RTL9068AAD	LFBGA 20.2x20.2x1.70	<p>Port 0 ~ 1: 100BASE-T1 PHY or RGMII/MII/RMII Port 2 ~ 3: 100BASE-T1, 1000BASE-T1, or SGMII Port 4: 100BASE-TX (Fast Ethernet), SGMII, or RGMII/MII/RMII Port 5: 100BASE-T1, SGMII, or RGMII/MII/RMII Port 6: 100BASE-T1, SGMII, HSGMII, USXGMII, or PCI-E 3.0 Port 7: RGMII/MII/RMII, SGMII, HSGMII, USXGMII, or PCI-E 3.0</p> <p><i>Note: Choose only one of P1, P4 or P7 as RGMII/MII/RMII's port.</i></p>
RTL9068ABD	LFBGA 17x17x1.70	<p>1. RTL9068ABD-VA-CG Port 0 ~ 1: 100BASE-T1 PHY or RGMII/MII/RMII Port 2 ~ 3: 100BASE-T1 or 1000BASE-T1 Port 4: 100BASE-TX (Fast Ethernet), SGMII, or RGMII/MII/RMII Port 5: 100BASE-T1, SGMII, or RGMII/MII/RMII Port 6: 100BASE-T1, SGMII, HISGMII, USXGMII, or PCI-E 3.0 Port 7: RGMII/MII/RMII, SGMII, HISGMII, USXGMII, or PCI-E 3.0</p> <p>2. RTL9068ABD-VA1-CG Port 0 ~ 1: 100BASE-T1 PHY or RGMII/MII/RMII Port 2 ~ 3: 100BASE-T1 or 1000BASE-T1 Port 4: 100BASE-TX (Fast Ethernet), SGMII, or RGMII/MII/RMII Port 5: 100BASE-T1, SGMII, or RGMII/MII/RMII Port 6: 100BASE-T1, SGMII, HISGMII, or USXGMII Port 7: RGMII/MII/RMII, SGMII, HISGMII, or USXGMII</p> <p><i>Note: Choose only one of P1, P4 or P7 as RGMII/MII/RMII's port.</i></p>
RTL9054AN	LFBGA 20.2x20.2x1.70	<p>Port 0 ~ 7: 100BASE-T1 Port 8: SGMII Port 9: SGMII or RGMII/MII/RMII Port 10: N/A Port 11: RGMII/MII/RMII Port 12~13: 100BASE-T1 Port 14: 100BASE-TX (Fast Ethernet)</p> <p><i>Note: The pins of P11 RGMII/MII/RMII port is named as P5_XXX since P5/P8/P11 shares the same pin. The pins of P6, P7 100BASE-T1 port are named as P6_GIGA_XXX and P7_GIGA_XXX.</i></p>

Table 2. RTL9054/RTL9068/RTL907x SERDES Data Rate and Bandwidth

SERDES	Interface Data Rate	Bandwidth
SGMII	1.25Gbps	1Gbps
HSGMII	3.125Gbps	2.5Gbps
USXGMII	5.15625Gbps	5Gbps
PCI-E 3.0	8.0Gbps	5Gbps

Several options are available for RTL9075AAD/RTL9072AAD. The RGMII/MII/RMII of port5 can be configured to either port8 or port11 (i.e. choose only one of either P5, P8 or P11 as RGMII/MII/RMII's port) for the RTL9075AAD/RTL9072AAD. The “option” can be thought of as a MUX and the physical output of xMII MUX is P5_RGMII pins.


Figure 2. RTL9075AAD

Figure 3. RTL9072AAD

The same idea can be applied to the RTL9068AAD/RTL9068ABD. The RGMII/MII/RMII of port1 can be configured to either port4 or port7 (i.e. choose only one of P1 or P4 or P7 as RGMII/MII/RMII port). The “option” can be thought of as a MUX and the physical output of xMII MUX is P1_RGMII pins.

The RTL9068ABD has two sub part numbers. The RTL9068ABD-VA-CG supports PCI-E. The RTL9068ABD-VA1-CG does not support PCI-E.

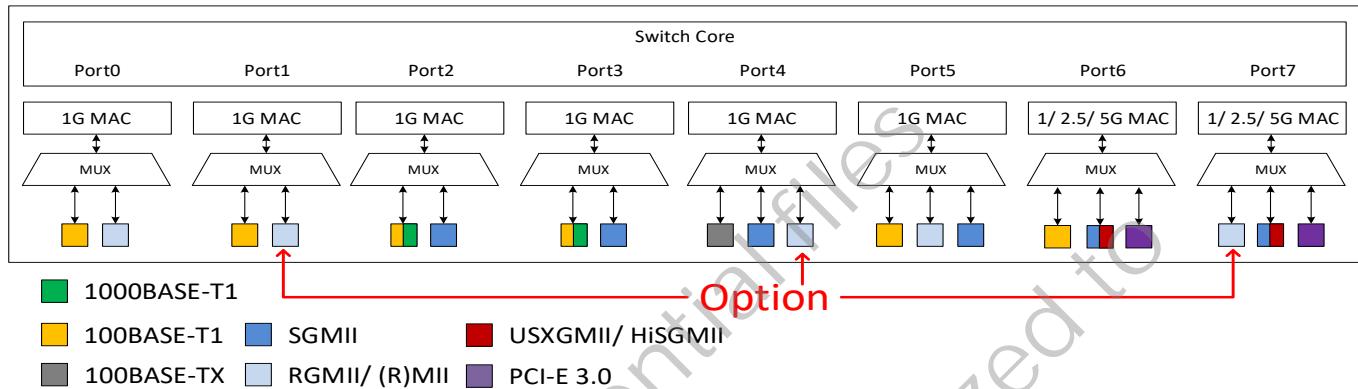
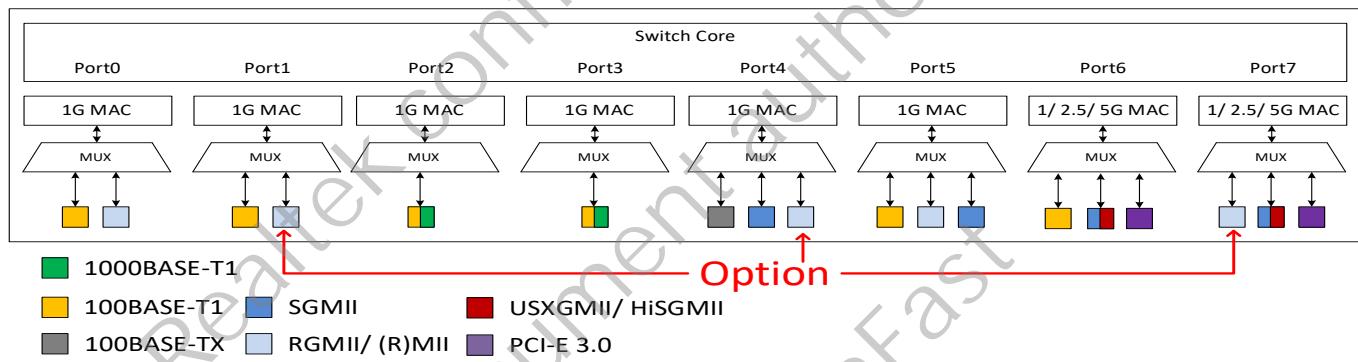


Figure 4. RTL9068AAD



Note. RTL9068ABD-VA1-CG does not support PCI-E

Figure 5. RTL9068ABD

The RTL9054AN is a low speed interface only version of the RTL9054/RTL9068/RTL907x family. It provides 10 100BASE-T1, 1 RGMII/MII/RMII, 1 shared port of SGMII or RGMII/MII/RMII and 1 FEPHY.

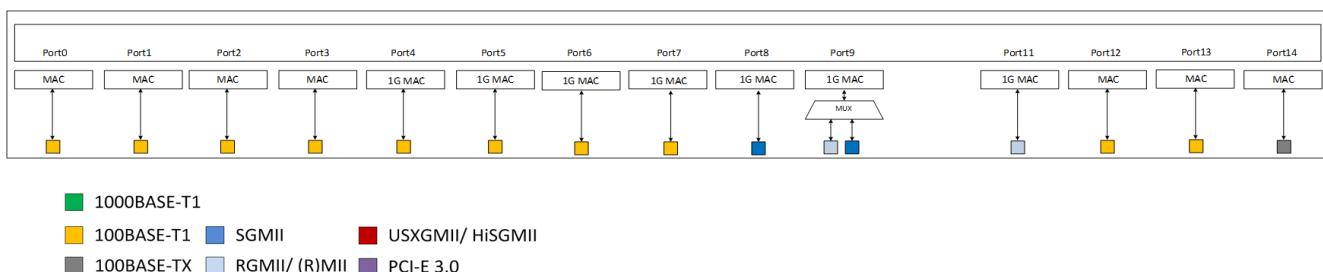


Figure 6. RTL9054AN

5. Pin Assignments

5.1. Pin Assignments (RTL9075AAD)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	GND	P2_MDN	P2_MDP	P3_MDN	P3_MDP	P4_MDN	P4_MDP	P5_MDN	P6_MDN	P12_MDN	P12_MDP	GND	FE_MDNB	FE_MDPB	GND	RSET	GND	P6_GIGA_MDN	P6_GIGA_MDP	P7_GIGA_MDN	P7_GIGA_MDP	GND	XO	GND	
B	P1_MDP	AVD033	AVD033	AVD033	AVD033_0G	AVD033_0G	AVD033_0G	AVD033	AVD009	AVD009	P13_MDN	P13_MDP	GND	FE_MDPA	GND	AVD009_GIGA	AVD033_P6	AVD033_P7	AVD033_P7	AVD033_XTAL	GND	XI	GND		
C	P1_MDN																							P2_LED	P3_LED
D	P6_MDP	VSENSE	P2GATE	NGATE	GND	GND	GND	GND	GND	GND	GND	GND	GND	AVD009_FE	AVD033_FE	RTT_CKNG	AVD033_CEN	ATP	ATN	AVD033_MCK	P1_LED	P2_LED	P4_LED	P5_LED	
E	GND	P6_MDN	V009	AVD033_JVD	AVD033_JHV	GND	GND	GND	GND	GND	GND	GND	GND	AVD009_FE	AVD033_FE	GND	AVD009_MCK	AVD009_MCK	P1_LED	P2_LED	P4_LED	P5_LED	P7_LED	C	
F	P4_TXD3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AVD009_FE	AVD033_FE	GND	AVD009_MCK	AVD009_MCK	P1_LED	P2_LED	P4_LED	P5_LED	P7_LED	D	
G	P4_TXD4	GND	INR	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_LED	P2_LED	P4_LED	P5_LED	F
H	P4_RXD	GND	VBAT	DV009	GND	GND	GND	GND	GND	P1_LED	P2_LED	P4_LED	P5_LED	G											
J	P4_TXD0	P4_VDDIO	WAKE	DV009	GND	GND	GND	GND	GND	DV009	DV003	P1_RXD1	P2_RXD2	J											
K	P4_TXE1	P4_VDDIO	GND	P4_LDOIN	GND	GND	GND	GND	GND	DV009	DV003	P1_RXD3	P2_RXD4	K											
L	P4_RX	P4_TESTD	P4_LDOOUT	P4_LDOIN	GND	GND	GND	GND	GND	DV009	GND	P1_RXD5	P2_RXD6	L											
M	P4_RXE	P4_VDDIO	P4_LDOOUT	P4_LDOIN	GND	GND	GND	GND	GND	DV009	GND	P1_RXD7	P2_RXD8	M											
N	P4_RXER	P4_VDDIO	GP01_VDDIO	DV009	GND	GND	GND	GND	GND	P1_RXD9	P2_RXD10	P4_RXD11	P5_RXD12	N											
P	P4_RXD1	GP02_0	GP02_5	DV009	GND	GND	GND	GND	GND	P1_RXD13	P2_RXD14	P4_RXD15	P5_RXD16	P7_RXD17											
R	P4_RXD2	GP02_1	GP02_6	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_RXD18	P2_RXD19	P4_RXD20	P5_RXD21	R	
T	P4_RXD3	GP02_2	GP02_7	NC	GND	GND	GND	GND	GND	P1_RXD22	P2_RXD23	P4_RXD24	P5_RXD25	T											
U	P4_RXD4	GP02_3	MAC_VDDIO	NC	GND	GND	GND	GND	GND	P1_RXD26	P2_RXD27	P4_RXD28	P5_RXD29	U											
V	P4_RXD5	GP02_4	MAC_VDDIO	NC	GND	GND	GND	GND	GND	P1_RXD30	P2_RXD31	P4_RXD32	P5_RXD33	V											
W	GP02_0	GP02_8	P1_LAWAKEB	P1_CLKREGB	GP02_1	GP02_9	GP02_10	GP02_11	GP02_12	GP02_13	GP02_14	GP02_15	GP02_16	GP02_17	GP02_18	GP02_19	GP02_20	GP02_21	GP02_22	GP02_23	GP02_24	GP02_25	GP02_26	GP02_27	W
Y	GP02_1	GP02_9	P1_ISOLATEB	P1_ISOLATEB	GP02_10	GP02_11	GP02_12	GP02_13	GP02_14	GP02_15	GP02_16	GP02_17	GP02_18	GP02_19	GP02_20	GP02_21	GP02_22	GP02_23	GP02_24	GP02_25	GP02_26	GP02_27	GP02_28	GP02_29	Y
AA	GP02_2	GP02_10	P1_LAWAKEB	P1_CLKREGB	GP02_11	GP02_12	GP02_13	GP02_14	GP02_15	GP02_16	GP02_17	GP02_18	GP02_19	GP02_20	GP02_21	GP02_22	GP02_23	GP02_24	GP02_25	GP02_26	GP02_27	GP02_28	GP02_29	AA	
AB	GP02_3	GP02_11	P1_ISOLATEB	P1_ISOLATEB	GP02_12	GP02_13	GP02_14	GP02_15	GP02_16	GP02_17	GP02_18	GP02_19	GP02_20	GP02_21	GP02_22	GP02_23	GP02_24	GP02_25	GP02_26	GP02_27	GP02_28	GP02_29	AB		
AC	TAPSL1	TAPSL1																						AC	
AD	RESETB	DSB	GND	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	P10_HSDP	P10_HSDP	P10_HSDP	P10_HSDP	AD	
AE	GND	GND	GND	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	GND_SERIES	P10_REFCLK_P	GND_SERIES	P10_REFCLK_N	P10_HSDP	P10_HSDP	P10_HSDP	P10_HSDP	AE	

Figure 7. RTL9075AAD Pin Assignments

5.2. Package Identification (RTL9075AAD)

Green package is indicated by the ‘G’ in GXXXV (Figure 8).



Figure 8. RTL9075AAD Package Identification Mark

5.3. Pin Assignments (RTL9072AAD)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	GND	P2_MON	P2_MDP	P3_MON	P3_MDP	P4_MON	P4_MDP	P5_MON	P5_MDP	P6_MON	P6_MDP	GND	FE_MONB	FE_MDPB	GND	RSET	GND	P6_OGA_MON	P6_OGA_MDP	P7_OGA_MON	P7_OGA_MDP	GND	X0	GND		
B	P1_MDP	AV0033	AV0033	AV0033	AV0033	AV0033_DG	AV0033_DG	AV0009	AV0009	AV0009	AV0009	GND	FE_MONA	FE_MDPA	GND	AV0009_GNA	AV0033_PB	AV0033_PB	AV0033_PT	AV0033_PT	AV0033_XTAL	GND	X1			
C	P1_MON	GND				VSENSE	PGATE	NGATE	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	RTT_CDG	AV0033_CEN	ATP	ATN	AV0033_MCK	P1_LED	P0_LED	P2_LED		
D	GND	P0_MDP																					P4_LED	P5_LED		
E	GND	P0_MON	V009	AV0033_HVD	AV0033_AVV	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_CDG	GND	GND	AV0009_MCK	P5_LDOIN	P5_LDOIN	P6_LDOIN	E	
F	P4_TXD1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_LED	F	
G	P4_RXD2	GND	INH	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOOUT	P5_LDOOUT	P6_LDOOUT	P9_LED	G	
H	P4_TXD1	GND	VBAT	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOOUT	P5_LDOOUT	P6_LDOOUT	P9_VDDO	H	
J	P4_RXD0	P4_VDDIO	WAKE	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	J	
K	P4_RXIN	P4_VDDIO	P4_LDOIN	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	K	
L	P4_TIC	P4_TESTD	P4_LDOOUT	P4_LDOIN	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	L	
M	P4_RXC	P4_VDDIO	P4_LDOOUT	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	M	
N	P4_RXER	P4_VDDIO	GPIO4_VDDIO	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	N	
P	P4_RXDV	GPIOC_0	GPIOC_5	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	P	
R	P4_RXD3	GPIOC_1	GPIOC_6	DV0009	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	R	
T	P4_RXD2	GPIOC_2	GPIOE_0	DV0009	NC	GND	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	T	
U	P4_RXD1	GPIOC_3	DV0009	MAC_VDDIO	NC	NC	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	U	
V	P4_RXD0	GPIOC_4	DV0009	MAC_VDDIO	NC	NC	GND	GND	GND	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	V	
W	GPIOA_9	GPIOB_0	P10_LANWAKEB	P10_CLKREGB	GPIO1_VDDIO	GPIO1_VDDIO	GPIOF_1	GND	DV0009	GND	GND	GND	GND	AV0009_FE	AV0033_FE	GND	AV0009_MCK	AV0033_MCK	GND	GND	P5_LDOIN	P5_LDOIN	P6_LDOIN	P9_RXD2	W	
Y	GPIOA_1	GPIOB_1	P10_ISOLATEB	P10_PCR_RESETB																	SPI_VDDIO	SPI_VDDIO	SPI_VDDIO	SPI_VDDIO	Y	
AA	GPIOA_2	GPIOB_2	P11_LANWAKEB	P11_CLKREGB	GPIOE_1	GPIOE_4	GPIOF_0	GPIOF_2	GPIOF_3	GPIOF_4	AV0009_TX	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	SPI_SCK	SPI_SDI1	SPI_SDI2	P5_VDDIO	P5_TXEN	AA	
AB	GPIOA_3	GPIOB_3	P11_ISOLATEB	P11_PCR_RESETB	GPIOE_2	GPIOE_3	AV0033_CMU	AV0009_CMU	AV0009_CMU	AV0009_CMU	AV0009_TX	AV0009_TX	AV0009_SGMII	AV0009_SGMII	AV0033_SGMII	AV0033_SGMII	AV0033_SGMII	AV0033_SGMII	AV0033_SGMII	AV0033_SGMII	SPI_SDO1	SPI_SDO2	SPI_SDO3	SPI_SDO4	AB	
AC	TAPSL1	TAPSL0																							AC	
AD	RESETB	DINB	GND	GND_SERDES	P10_REFCLK_P	GND_SERDES	P10_REFCLK_N	GND_SERDES	P10_REFCLK_P	GND_SERDES	P11_REFCLK_P	GND_SERDES	P11_REFCLK_N	AV0009_TX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AV0009_RX	AD
AE	GND	GND	GND_SERDES	P10_REFCLK_N	P10_ISDOP	P10_HSON	P10_HSN	P10_HSP	P11_HSON	P11_HSN	P11_HSP	P11_HSON	P11_HSN	P11_HSP	P11_HSON	P11_HSN	P11_HSP	P11_HSON	P11_HSN	P11_HSP	P11_HSON	P11_HSN	P11_HSP	P11_HSON	AE	

Figure 9. RTL9072AAD Pin Assignments

5.4. Package Identification (RTL9072AAD)

Green package is indicated by the ‘G’ in GXXXX (Figure 10).



Figure 10. RTL9072AAD Package Identification Mark

5.5. Pin Assignments (RTL9068AAD)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	GND	NC	NC	NC	NC	P0_MDN	P0_MDP	P1_MDN	P1_MDP	P5_MDN	P5_MDP	GND	FE_MDN	FE_MDP	GND	RSET	GND	P2_GIGA_MDN	P2_GIGA_MDP	P3_GIGA_MDN	P3_GIGA_MDP	GND	XO	GND	
B	NC	AV0D33	AV0D33	AV0D33	AV0D33_0G	AV0D33_0G	AV0D33_0G	AV0D09	AV0D09	AV0D09	AV0D09	GND	AV0D09_FE	AV0D33_FE	GND	RTT_CKDG	AV0D33_CEN	ATP	ATN	AV0D33_MCK	NC	TDO	P0_LED	P1_LED	
C	NC	GND																						NC	NC
D	GND	NC	VSENSE	PGATE	NGATE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV0D09_GIGA	AV0D33_P2	AV0D33_P2	AV0D33_P3	AV0D33_XTAL	GND	XI
E	GND	NC	VO09	AV0D33_HVD	AV0D33_AHV	GND	GND	GND	GND	GND	GND	GND	GND	AV0D09_FE	AV0D33_FE	GND	AV0D33_CKDG	GND	GND	AV0D09_MCK	AV0D09_MCK	P5_LDOIN	P1_LDOIN	P2_LED	P3_LED
F	P0_RXD0	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P5_LDOIN	P1_LDOIN	P2_LED	P3_LED	F
G	P0_RXD2	GND	INH	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P5_LDOOUT	P1_LDOOUT	FE_LDO1	FE_LDO2	G
H	P0_RXD1	GND	VBAT	DV009	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P5_LDOOUT	P1_LDOOUT	P5_VDD0	P5_RXD0	H
J	P0_RXD0	P0_VDDIO	WAKE	DV009	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DV009	DV0033	P5_RDO1	P5_RXD2	J		
K	P0_RXEN	P0_VDDIO	GND	P0_LDOIN	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DV009	DV0033	P5_RDO2	P5_RXD0	K		
L	P0_TXIC	P0_TESTD	P0_LDOOUT	P0_LDOIN	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DV009	GND	P5_RXER	P5_RXC	L		
M	P0_RXC	P0_VDDIO	P0_LDOOUT	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DV009	GND	P5_VDD0	P5_VDD0	M		
N	P0_RXER	P0_VDDIO	GPIOE_VDDIO	DV009	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P5_TXE	P5_TXEN	N		
P	P0_RXD0	GPIOC_0	GPIOC_5	DV009	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P5_RXD2	P5_RXD3	P		
R	P0_RXD2	GPIOC_1	GPIOC_6	GPIOC_1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_VDD0	P1_VDD0	T		
T	P0_RXD2	GPIOC_2	GPIOC_0	GPIOE_0	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_RXD0	P1_RXD1	U		
U	P0_RXD1	GPIOC_3	DV009	DV009	MAC_VDDIO	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_RXD2	P1_RXD3	V		
V	P0_RXD0	GPIOC_4	DV009	DV009	MAC_VDDIO	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_RXD0	P1_RXD3	W		
W	GPIOA_0	GPIOB_0	P0_LANWAKEB	P0_CLKRQD	GPIO1_VDDIO	GPIO1_VDDIO	GPIO1_1	DV009	DV009	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	P1_RXER	P1_VDD0	W		
Y	GPIOA_1	GPIOB_1	P0_ISOLATEB	P0_PCE_RESETB															SPI_VDDIO	SPI_VDDIO	P1_RXC	P1_VDD0	Y		
AA	GPIOA_2	GPIOB_2	P7_LANWAKEB	P7_CLKRQD	GPIOE_1	GPIOE_4	GPIOE_0	GPIOF_2	GPIOF_3	GPIOF_4	AV0D09_TX	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	GND_SGMII	SPI_SCK	SPI_SIO1	SPI_SIO2	P1_VDD0	P1_TXC	AA		
AB	GPIOA_3	GPIOB_3	P7_ISOLATEB	P7_PCE_RESETB	GPIOE_2	GPIOE_3	AV0D33_CMU	AV0D09_CMU	AV0D09_CMU	AV0D09_TX	AV0D09_SGMII	AV0D09_SGMII	AV0D33_SGMII	AV0D33_SGMII	AV0D33_SGMII	AV0D33_SGMII	SPI_SIO0	SPI_SIO3	SPI_CS8			AB			
AC	TAPSL1	TAPSL0																			P1_RXD0	P1_RXD1	AC		
AD	RESETB	DISB	GND	GND_SERDES	P0_REFCLK_P	GND_SERDES	GND_SERDES	AV0D33_CMU	GND_SERDES	P0_REFCLK_N	GND_SERDES	AV0D09_TX	AV0D09_RX	AV0D09_RX	P4_HSP	P4_HSOP	P5_HSP	P2_HSP	P3_HSP	P1_HSOP	P1_HSOP	P1_HSOP	AD		
AE	GND	GND	GND	GND_SERDES	P0_REFCLK_P	GND_SERDES	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	P0_HSOP	GND	AE	

Figure 11. RTL9068AAD Pin Assignments

5.6. Package Identification (RTL9068AAD)

Green package is indicated by the ‘G’ in GXXXV (Figure 12).



Figure 12. RTL9068AAD Package Identification Mark

5.7. Pin Assignments (RTL9068ABD)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	GND	P0_M DIN	P0_M DIP	P5_M DIN	P5_M DIP	FE_M DINB	FE_M DIPB	AVDD09_FE	GND	RSET	GND	XO	XI	GND	P2_GIGA_M DIN	P2_GIGA_M DIP	P3_GIGA_M DIN	P3_GIGA_M DIP	GND	
B	P0_VDDIO	GND	P1_M DIN	P1_M DIP	P6_M DIN	P6_M DIP	FE_M DIN A	FE_M DIPA	GND	GND	AVDD33_XTAL	AVDD33_XTAL	AVDD33_CEN	ATP	ATN	AVDD33_MCK	AVDD33_MCK	GND	GND	
C	P0_TX03	P0_TX02																		
D	P0_TX01	P0_TX00	AVDD33	AVDD33	AVDD33_DIG	AVDD33_FE	AVDD09_FE	GND	GND	RTT_CKDG	GND	GND	GND	AVDD09_MCK	AVDD09_GIGA		P5_VDDIO	P5_RX00	D	
E	P0_TXEN	P0_TXC	AVDD09	AVDD09	AVDD33_DIG	AVDD33_FE	GND	GND	GND	AVDD33_CKDG	GND	GND	GND	AVDD09_MCK	AVDD09_GIGA		P5_RX01	P5_RX01	E	
F	P0_VDDIO	P0_VDDIO	VSENSE	NGATE										AVDD33_P2	AVDD33_P3		P5_RX03	P5_RX00	F	
G	P0_RXC	P0_TESTD	VO09	AVDD33_AHV		VBAT	DVDD09	GND	GND	GND	GND	GND	GND	AVDD33_P2	AVDD33_P3		P5_RXER	P5_RXC	G	
H	P0_RXER	P0_RXDV	GND	PGATE	P0_LDOOUT	P0_LDOOUT	DVDD09	GND	GND	P5_LDOIN	P1_LDOIN	P0_LED	TDO			P5_VDDIO	P5_VDDIO	H		
J	P0_RX03	P0_RX02	INH	AVDD33_HVD	P0_LDOIN	GPIOF_3	DVDD09	GND	GND	P5_LDOIN	P1_LDOIN	P2_LED	P1_LED			P5_RXC	P5_RXEN	J		
K	P0_RX01	P0_RX00	WAKE	GND_HGD	P0_LDOIN	GPIOF_2	DVDD09	GND	GND	P5_LDOOUT	P1_LDOOUT	P3_LED	SPI_S02			P5_RX00	P5_RX01	K		
L	GPIOA_0	GPIOB_0	GPIOC_0	GPIOC_1	GPIO0_VDDIO	GPIO1_VDDIO	DVDD09	GND	GND	P5_LDOOUT	P1_LDOOUT	P5_LED	SPI_CS			P5_RX02	P5_RX03	L		
M	GPIOA_1	GPIOB_1	GPIOC_2	GPIOC_3	GPIOE_0	GPIOE_1	GPIO1_VDDIO	DVDD09	DVDD09	DVDD09	DVDD09	P6_LED	SPI_S01			P1_RX00	P1_RX01	M		
N	GPIOA_2	GPIOB_2	GPIOC_4	GPIOC_5	GPIOE_2	GPIOE_4	GPIO1_VDDIO	DVDD09	DVDD09	DVDD09	DVDD09	FE_LED0	SPI_S03			P1_RX02	P1_RX03	N		
P	GPIOA_3	TAPSL0	GPIOD_0	GPIOD_1								FE_LED1	SPI_SCK			P1_RX00	P1_RXER	P		
R	DISB	TAPSL1	P7_LANWAKEB	P7_CLKREQB	MAC_VDDIO	GPIOE_0	GPIOE_1	GPIO1_2	GND	GND	GND	GND	GND	SPI_VDDIO	SPI_S00	P1_RXC	P1_VDDIO	R		
T	RESETB	P6_LANWAKEB	P7_ISOLATEB	P7_PCIE_RESETB	MAC_VDDIO	GND_SERDES	GND_SERDES	AVDD33_CMU	AVDD33_CMU	GND_SERDES	GND_SERDES	AVDD09_SGMII	AVDD09_SGMII	AVDD33_SGMII	AVDD33_SGMII		P1_VDDIO	P1_RXC	T	
U	P6_CLKREQB	P6_ISOLATEB														P1_TESTD	P1_RXEN	U		
V	P6_PCIE_RESETB	P6_REFCLK_P	P6_REFCLK_N	AVDD09_RX	AVDD09_RX	P7_REFCLK_P	P7_REFCLK_N	AVDD09_CMU	AVDD09_CMU	AVDD09_TX	AVDD09_TX	P4_HSIP	P4_HSIN	P5_HSIP	P5_HSIN	AVDD33_SGMII	P1_RX03	P1_RX01	V	
W	GND	GND_SERDES	P6_HSOP	P6_HS0N	P6_HSIN	P6_HSIP	GND_SERDES	P7_HSOP	P7_HS0N	P7_HSIP	P7_HSIP	GND_SGMII	P4_HSOP	P4_HS0N	P5_HSOP	P5_HS0N	GND_SGMII	P1_RX02	GND	W

Figure 13. RTL9068ABD Pin Assignments

5.8. Package Identification (RTL9068ABD)

Green package is indicated by the ‘G’ in GXXXV (Figure 14).



Figure 14. RTL9068ABD Package Identification Mark

5.9. Pin Assignments (RTL9054AN)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	GND	P2_MDN	P2_MDP	P3_MDN	P3_MDP	P4_MDN	P4_MDP	P5_MDN	P5_MDP	P12_MDN	P12_MDP	GND	PE_MONI	PE_MDPB	GND	RSET	GND	P6_GIGA_MDN	P7_GIGA_MDP	GND	GND	XO	GND		
B	P1_MDP	AVID033	AVID033	AVID033	AVID033	AVID033	AVID033	AVID033	AVID033	AVID033	AVID033	GND	PE_MONA	PE_MDPA	GND	AVID033_GIGA	AVID033_P6	AVID033_P7	AVID033_XTAL	GND	XI				
C	P1_MDN	GND																							
D	P6_MDP	NC	NC	NC	GND	GND	GND	GND	GND	AVID033_FE	AVID033_FE	GND	RITI_CLKRD	AVID033_CEN	ATP	ATN	AVID033_MCK	P1_LED	P6_LED	P4_LED	P5_LED	P2_LED	P3_LED	P1	
E	P6_MDN	NC	NC	NC	GND	GND	GND	GND	GND	AVID033_FE	AVID033_FE	GND	AVID033_CLKRD	AVID033_CEN	GND	AVID033_MCK	P5_L20IN	P5_L20IN	P4_LED	P5_LED	P2_LED	P3_LED	P12_LED	P13_LED	
F	TSTTB	GND																							
G	TSTTB	GND																							
H	TSTTB	GND																							
J	TSTTB	VDD	DVDD09																						
K	TSTTB	P4_VDDIO	WAKE	DVDD09																					
L	TSTTB	P4_VDDIO	GND	P4_L20IN																					
M	TSTTB	TSTTB	P4_L20OUT	P4_L20IN																					
N	TSTTB	P4_VDDIO	P4_VDDIO	VDD09	DVDD09																				
P	TSTTB	GPIOC_0	GPIOC_5	DVDD09																					
R	TSTTB	GPIOC_1	GPIOC_1	GPIOC_0	DVDD09																				
T	TSTTB	GPIOC_2	GPIOC_2	GPIOE_0	GPIOC_1																				
U	TSTTB	GPIOC_3	DVDD09	DVDD09	MAC_VDDIO	NC																			
V	TSTTB	GPIOC_4	DVDD09	DVDD09	MAC_VDDIO	NC																			
W	GPIOA_0	GPIOB_0	NC	NC	GPIO1_VDDIO	GPIO1_VDDIO	GPIO1_VDDIO	GPIO1_VDDIO	NC	DVDD09	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	
Y	GPIOA_1	GPIOB_1	NC	NC																					
AA	GPIOA_2	GPIOB_2	NC	NC	GPIOE_1	GPIOE_4	GPIOF_0	GPIOF_2	GPIOF_3	GPIOF_4	AVD033_TX	GND_SOMI	GND_SOMI	GND_SOMI	GND_SOMI	GND_SOMI	GND_SOMI	GND_SOMI	SPI_VDDIO	SPI_VDDIO	P5_RXD0	P5_RXD0	P5_RXD0	P5_RXD0	
AB	GPIOA_3	GPIOB_3	NC	NC	GPIOE_2	GPIOE_3	AVID033_CMU	AVID033_CMU	AVID033_CMU	AVID033_CMU	AVID033_TX	AVID033_TX	AVID033_TX	AVID033_TX	AVID033_TX	AVID033_TX	AVID033_TX	AVID033_TX	SPI_SCK	SPI_SCK	SPI_SIO1	SPI_SIO2	P5_Video	P5_Video	
AC	TAPSL1	TAPSL0																							
AD	RESETB	DSB	GND	GND_SERDES	NC	GND_SERDES	GND_SERDES	AVID033_CMU	GND_SERDES	NC	GND_SERDES	AVID033_TX	AVID033_RX	AVID033_RX	P6_HSP	P6_HSOP	P9_HSP	P9_HSOP	NC	NC	NC	NC	GND_SOMI	P5_TxD0	
AE			GND	GND	GND_SERDES	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	GND	

Figure 15. RTL9054AN Pin Assignments

Note. In the RTL9054AN, the pins for Port 11 RGMII/MII/RMII are named as P5_XXX. The pins for Port 6 and Port 7 100BASE-T1 are named as P6_GIGA_XXX and P7_GIGA_XXX respectively.

5.10. Package Identification (RTL9054AN)

Green package is indicated by the 'G' in GXXXV (Figure 16).



Figure 16. RTL9054AN Package Identification Mark

6. Pin Descriptions

Codes used in the following tables are listed below.

I: Input Pin	AI: Analog Input Pin
O: Output Pin	AO: Analog Output Pin
I/O: Bi-Directional Input/Output Pin	G: Ground Pin
P: Power Pin	O/D: Open Drain

6.1. 100BASE-T1 PHY Media Connection Pins

Note: For the RTL9054AN, port 6 and port 7 100BASE-T1 pins refer to P6_GIGA_XXX and P7_GIGA_XXX pins.

Table 3. 100BASE-T1 PHY Media Connection Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P13_MDIN	B11	B11	-	-	-	AI/O	Differential Transmit and Receive Data Pair. Supports 100BASE-T1.
P13_MDIP	B12	B12	-	-	-		
P12_MDIN	A10	A10	-	-	-		
P12_MDIP	A11	A11	-	-	-		
P10_MDIN	-	-	B11	-	-		
P10_MDIP	-	-	B12	-	-		
P9_MDIN	-	-	A10	-	-		
P9_MDIP	-	-	A11	-	-		
P6_MDIN	-	-	-	B11	B5		
P6_MDIP	-	-	-	B12	B6		
P5_MDIN	A8	A8	A8	A10	A4		
P5_MDIP	A9	A9	A9	A11	A5		
P4_MDIN	A6	A6	A6	-	-		
P4_MDIP	A7	A7	A7	-	-		
P3_MDIN	A4	A4	A4	-	-		
P3_MDIP	A5	A5	A5	-	-		
P2_MDIN	A2	A2	A2	-	-		
P2_MDIP	A3	A3	A3	-	-		
P1_MDIN	C1	C1	C1	A8	B3		
P1_MDIP	B1	B1	B1	A9	B4		
P0_MDIN	E2	E2	E2	A6	A2		
P0_MDIP	D2	D2	D2	A7	A3		

6.2. 1000BASE-T1 PHY Media Connection Pins

Note: For the RTL9054AN, P6_GIGA_XXX and P7_GIGA_XXX pins are used for port 6 and port 7 100BASE-T1.

Table 4. 1000BASE-T1 PHY Media Connection Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P6_GIGA_MDIN	A18	A18	A18	-	-	AI/O	Differential Transmit and Receive Data Pair. Supports 1000BASE-T1.
P6_GIGA_MDIP	A19	A19	A19	-	-		
P2_GIGA_MDIN	-	-	-	A18	A15	AI/O	Differential Transmit and Receive Data Pair. Supports 1000BASE-T1.
P2_GIGA_MDIP	-	-	-	A19	A16		
P7_GIGA_MDIN	A20	A20	A20	-	-	AI/O	Differential Transmit and Receive Data Pair. Supports 1000BASE-T1.
P7_GIGA_MDIP	A21	A21	A21	-	-		
P3_GIGA_MDIN	-	-	-	A20	A17	AI/O	Differential Transmit and Receive Data Pair. Supports 1000BASE-T1.
P3_GIGA_MDIP	-	-	-	A21	A18		

6.3. FE PHY Media Connection Pins

Table 5. FE PHY Media Connection Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
FE_MDINA	B14	B14	B14	B14	B7	AO	Differential Transmit Data Output. Supports 100BASE-TX, 10BASE-T. RTL9075AAD is port 14. RTL9072AAD is port 8. RTL9068AAD and RTL9068ABD are port 4.
FE_MDIPA	B15	B15	B15	B15	B8		
FE_MDINB	A13	A13	A13	A13	A6	AI	Differential Receive Data Input. Supports 100BASE-TX, 10BASE-T. Port information refers to FE_MDINA/FE_MDIPA.
FE_MDIPB	A14	A14	A14	A14	A7		

6.4. SGMII Pins

Table 6. SGMII Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P2_HSON P2_HSOP	- -	- -	- -	AE19 AD19	- -	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P2_HSIN P2_HSIP	- -	- -	- -	AE20 AD20	- -	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P3_HSON P3_HSOP	- -	- -	- -	AE22 AD22	- -	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P3_HSIN P3_HSIP	- -	- -	- -	AE21 AD21	- -	AI	SGMII Differential Input: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P4_HSON P4_HSOP	- -	- -	- -	AE16 AD16	W14 W13	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P4_HSIN P4_HSIP	- -	- -	- -	AE15 AD15	V13 V12	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P5_HSON P5_HSOP	- -	- -	- -	AE17 AD17	W16 W15	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P5_HSIN P5_HSIP	- -	- -	- -	AE18 AD18	V15 V14	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P6_HSON P6_HSOP	- -	AE19 AD19	AE19 AD19	AE7 AE6	W4 W3	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P6_HSIN P6_HSIP	- -	AE20 AD20	AE20 AD20	AE8 AE9	W5 W6	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P7_HSON P7_HSOP	- -	AE22 AD22	AE22 AD22	AE12 AE11	W9 W8	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P7_HSIN P7_HSIP	- -	AE21 AD21	AE21 AD21	AE13 AE14	W10 W11	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P8_HSON P8_HSOP	AE16 AD16	AE16 AD16	AE16 AD16	- -	- -	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P8_HSIN P8_HSIP	AE15 AD15	AE15 AD15	AE15 AD15	- -	- -	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P9_HSON P9_HSOP	AE17 AD17	AE17 AD17	AE17 AD17	- -	- -	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P9_HSIN P9_HSIP	AE18 AD18	AE18 AD18	AE18 AD18	-	-	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P10_HSON P10_HSOP	- -	AE7 AE6	AE7 AE6	- -	- -	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P10_HSIN P10_HSIP	- -	AE8 AE9	AE8 AE9	-	-	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P11_HSON P11_HSOP	- -	AE12 AE11	AE12 AE11	-	-	AO	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
P11_HSIN P11_HSIP	- -	AE13 AE14	AE13 AE14	-	-	AI	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an external device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.

6.5. USXGMII Pins

Table 7. USXGMII Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P6_HSON	-	-	-	AE7	W4	AO	USXGMII Differential Output.
P6_HSOP	-	-	-	AE6	W3	AO	USXGMII Differential Output.
P6_HSIN	-	-	-	AE8	W5	AI	USXGMII Differential Input.
P6_HSIP	-	-	-	AE9	W6	AI	USXGMII Differential Input.
P7_HSON	-	-	-	AE12	W9	AO	USXGMII Differential Output.
P7_HSOP	-	-	-	AE11	W8	AO	USXGMII Differential Output.
P7_HSIN	-	-	-	AE13	W10	AI	USXGMII Differential Input.
P7_HSIP	-	-	-	AE14	W11	AI	USXGMII Differential Input.
P10_HSON	-	AE7	AE7	-	-	AO	USXGMII Differential Output.
P10_HSOP	-	AE6	AE6	-	-	AO	USXGMII Differential Output.
P10_HSIN	-	AE8	AE8	-	-	AI	USXGMII Differential Input.
P10_HSIP	-	AE9	AE9	-	-	AI	USXGMII Differential Input.
P11_HSON	-	AE12	AE12	-	-	AO	USXGMII Differential Output.
P11_HSOP	-	AE11	AE11	-	-	AO	USXGMII Differential Output.
P11_HSIN	-	AE13	AE13	-	-	AI	USXGMII Differential Input.
P11_HSIP	-	AE14	AE14	-	-	AI	USXGMII Differential Input.

6.6. HSGMII Pins

Table 8. HSGMII Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P6_HSON	-	-	-	AE7	W4	AO	HSGMII Differential Output.
P6_HSOP	-	-	-	AE6	W3	AO	HSGMII Differential Output.
P6_HSIN	-	-	-	AE8	W5	AI	HSGMII Differential Input.
P6_HSIP	-	-	-	AE9	W6	AI	HSGMII Differential Input.
P7_HSON	-	-	-	AE12	W9	AO	HSGMII Differential Output.
P7_HSOP	-	-	-	AE11	W8	AO	HSGMII Differential Output.
P7_HSIN	-	-	-	AE13	W10	AI	HSGMII Differential Input.
P7_HSIP	-	-	-	AE14	W11	AI	HSGMII Differential Input.
P10_HSON	-	AE7	AE7	-	-	AO	HSGMII Differential Output.
P10_HSOP	-	AE6	AE6	-	-	AO	HSGMII Differential Output.
P10_HSIN	-	AE8	AE8	-	-	AI	HSGMII Differential Input.
P10_HSIP	-	AE9	AE9	-	-	AI	HSGMII Differential Input.
P11_HSON	-	AE12	AE12	-	-	AO	HSGMII Differential Output.
P11_HSOP	-	AE11	AE11	-	-	AO	HSGMII Differential Output.
P11_HSIN	-	AE13	AE13	-	-	AI	HSGMII Differential Input.
P11_HSIP	-	AE14	AE14	-	-	AI	HSGMII Differential Input.

6.7. PCI-Express Pins

Table 9. PCI-Express Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P6_HSON	-	-	-	AE7	W4	AO	PCI Express Differential Output.
P6_HSOP	-	-	-	AE6	W3	AO	PCI Express Differential Output.
P6_HSIN	-	-	-	AE8	W5	AI	PCI Express Differential Input.
P6_HSIP	-	-	-	AE9	W6	AI	PCI Express Differential Input.
P6_REFCL_K_N	-	-	-	AE5	V3	AI	PCI Express Differential Reference Clock Source (100Mhz ±300ppm).
P6_REFCL_K_P	-	-	-	AD5	V2	AI	PCI Express Differential Reference Clock Source (100Mhz ±300ppm).
P6_PCIE_RESETB	-	-	-	Y5	V1	I	PCI Express Reset Signal (Active Low). When the PCIE_RESETB is asserted at power-on state, the PCIE interface returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of PCIE_RESETB.
P6_CLKREQB	-	-	-	W5	U1	O/D	Reference Clock Request Signal (Open drain; Active Low output mode with a weak external pull up resistor). This signal is used by the PCI Express interface to request starting of the PCI Express reference clock.
P6_LANW_AKEB	-	-	-	W4	T2	O/D	PCI Express Power Management Event (Open drain; Active low output mode with a weak external pull up resistor). Used to re-activate the PCI Express slot's main power rails and reference clocks.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P6_ISOLATEB	-	-	-	Y4	U2	I	Isolate Pin (Active Low). Used to isolate the PCI Express interface of RTL9068/RTL907x from the PCI Express bus. The RTL9068/RTL907x will not drive its PCI Express output (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted. The isolate pin will follow the system state S0 to high, and S3/S4 to low.
P7_HSON P7_HSOP	-	-	-	AE12 AE11	W9 W8	AO	PCI Express Differential Output.
P7_HSIN P7_HSIP	-	-	-	AE13 AE14	W10 W11	AI	PCI Express Differential Input.
P7_REFCL K_N P7_REFCLK_P	-	-	-	AE10 AD10	V7 V6	AI	PCI Express Differential Reference Clock Source (100Mhz ±300ppm).
P7_PCIE_RESETB	-	-	-	AB5	T5	I	PCI Express Reset Signal (Active Low). When the PCIE_RESETB is asserted at power-on state, the PCIE interface returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of PCIE_RESETB.
P7_CLKREQB	-	-	-	AA5	R5	O/D	Reference Clock Request Signal (Open drain; Active Low output mode with a weak external pull up resistor). This signal is used by the PCI Express interface to request starting of the PCI Express reference clock.
P7_LANW_AKEB	-	-	-	AA4	R4	O/D	PCI Express Power Management Event (Open drain; Active low output mode with a weak external pull up resistor). Used to re-activate the PCI Express slot's main power rails and reference clocks.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P7_ISOLATEB	-	-	-	AB4	T4	I	Isolate Pin (Active Low). Used to isolate the PCI Express interface of the RTL9068/RTL907x from the PCI Express bus. The RTL9068/RTL907x will not drive its PCI Express output (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted. The isolate pin will follow the system state S0 to high, and S3/S4 to low.
P10_HSON P10_HSOP	- -	AE7 AE6	AE7 AE6	- -	- -	AO	PCI Express Differential Output.
P10_HSIN P10_HSIP	- -	AE8 AE9	AE8 AE9	- -	- -	AI	PCI Express Differential Input.
P10_REFCLK_N P10_REFCLK_P	- -	AE5 AD5	AE5 AD5	- -	- -	AI	PCI Express Differential Reference Clock Source (100Mhz ±300ppm).
P10_PCIE_RESETB	-	Y5	Y5	-	-	I	PCI Express Reset Signal (Active Low). When the PCIE_RESETB is asserted at power-on state, the PCIE interface returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of PCIE_RESETB.
P10_CLKREQB	-	W5	W5	-	-	O/D	Reference Clock Request Signal (Open drain; Active Low output mode with a weak external pull up resistor). This signal is used by the PCI Express interface to request starting of the PCI Express reference clock.
P10_LANWAKEB	-	W4	W4	-	-	O/D	PCI Express Power Management Event (Open drain; Active low output mode with a weak external pull up resistor). Used to re-activate the PCI Express slot's main power rails and reference clocks.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P10_ISOLATEB	-	Y4	Y4	-	-	I	Isolate Pin (Active Low). Used to isolate the PCI Express interface of RTL9068/RTL907x from the PCI Express bus. The RTL9068/RTL907x will not drive its PCI Express output (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted. The isolate pin will follow the system state S0 to high, and S3/S4 to low.
P11_HSON P11_HSOP	- -	AE12 AE11	AE12 AE11	- -	- -	AO	PCI Express Differential Output.
P11_HSIN P11_HSIP	- -	AE13 AE14	AE13 AE14	- -	- -	AI	PCI Express Differential Input.
P11_REFCLK_LK_N P11_REFCLK_P	- -	AE10 AD10	AE10 AD10	- -	- -	AI	PCI Express Differential Reference Clock Source (100Mhz ±300ppm).
P11_PCIE_RESETB	-	AB5	AB5	-	-	I	PCI Express Reset Signal (Active Low). When the PCIE_RESETB is asserted at power-on state, the PCIE interface returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of PCIE_RESETB.
P11_CLKREQB	-	AA5	AA5	-	-	O/D	Reference Clock Request Signal (Open drain; Active Low output mode with a weak external pull up resistor). This signal is used by the PCI Express interface to request starting of the PCI Express reference clock.
P11_LANWAKEB	-	AA4	AA4	-	-	O/D	PCI Express Power Management Event (Open drain; Active low output mode with a weak external pull up resistor). Used to re-activate the PCI Express slot's main power rails and reference clocks.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P11_ISOLATEB	-	AB4	AB4	-	-	I	Isolate Pin (Active Low). Used to isolate the PCI Express interface of RTL9068/RTL907x from the PCI Express bus. The RTL9054/RTL9068/RTL907x will not drive its PCI Express output (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted. The isolate pin will follow the system state S0 to high, and S3/S4 to low.

6.8. RGMII Interface Pins

Note. For the RTL9054AN Port 11 RGMII pins, refer to P5_XXX pins.

Table 10. RGMII Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_RXDV	-	-	-	P1	H2	I	RGMII Receive Control. The P0_RXDV indicates RXDV at rising edge of P0_RXC and the logical derivative of RXER and RXDV at the falling edge of P0_RXC.
P0_RXD0	-	-	-	V1	K2	I	RGMII Receive Data Bus. In RGMII 1000Mbps, P0_RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P0_RXC and bit[7:4] presented on the falling edge of P0_RXC. In RGMII 10/100Mbps, the received data nibble is presented on P0_RXD[3:0] on the rising edge of P0_RXC and duplicated on the falling edge of P0_RXC.
P0_RXD1	-	-	-	U1	K1		
P0_RXD2	-	-	-	T1	J2		
P0_RXD3	-	-	-	R1	J1		

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_RXC	-	-	-	M1	G1	I	RGMII Receive Clock. All RGMII received inputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P0_TXC	-	-	-	L1	E2	O	RGMII Transmit Clock. All RGMII transmitted outputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P0_TXD0 P0_TXD1 P0_TXD2 P0_TXD3	- - - -	- - - -	- - - -	J1 H1 G1 F1	D2 D1 C2 C1	O	RGMII Transmit Data Bus. In RGMII 1000Mbps, P0_TXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P0_TXC and bit[7:4] presented on the falling edge of P0_TXC. In RGMII 10/100Mbps, the transmitted data nibble is presented on P0_TXD[3:0] on the rising edge of P0_TXC and duplicated on the falling edge of P0_TXC.
P0_TXEN	-	-	-	K1	E1	O	RGMII Transmit Control. The P0_TXEN indicates TXEN at rising edge of P0_TXC, and the logical derivative of TXER and TXEN at the falling edge of P0_TXC.
P1_RXDV	-	-	-	W24	P18	I	RGMII Receive Control. The P1_RXDV indicates RXDV at rising edge of P1_RXC and the logical derivative of RXER and RXDV at the falling edge of P1_RXC.
P1_RXD0 P1_RXD1	- -	- -	- -	U24 U25	M18 M19	I	RGMII Receive Data Bus.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_RXD2 P1_RXD3	- -	- -	- -	V24 V25	N18 N19		In RGMII 1000Mbps, P1_RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P1_RXC and bit[7:4] presented on the falling edge of P1_RXC. In RGMII 10/100Mbps, the received data nibble is presented on P1_RXD[3:0] on the rising edge of P1_RXC and duplicated on the falling edge of P1_RXC.
P1_RXC	-	-	-	Y24	R18	I	RGMII Receive Clock. All RGMII received inputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P1_TXC	-	-	-	AA25	T19	O	RGMII Transmit Clock. All RGMII transmitted outputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P1_TXD0 P1_TXD1 P1_TXD2 P1_TXD3	- - - -	- - - -	- - - -	AC24 AC25 AD24 AD25	V19 V18 W18 V17	O	RGMII Transmit Data Bus. In RGMII 1000Mbps, P1_TXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P1_TXC and bit[7:4] presented on the falling edge of P1_TXC. In RGMII 10/100Mbps, the transmitted data nibble is presented on P1_TXD[3:0] on the rising edge of P1_TXC and duplicated on the falling edge of P1_TXC.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_TXEN	-	-	-	AB25	U19	O	RGMII Transmit Control. The P1_TXEN indicates TXEN at rising edge of P1_TXC, and the logical derivative of TXER and TXEN at the falling edge of P1_TXC.
P4_RXDV	-	P1	P1	-	-	I	RGMII Receive Control. The P4_RXDV indicates RXDV at rising edge of P4_RXC and the logical derivative of RXER and RXDV at the falling edge of P4_RXC.
P4_RXD0 P4_RXD1 P4_RXD2 P4_RXD3	- - - -	V1 U1 T1 R1	V1 U1 T1 R1	- - - -	- - - -	I	RGMII Receive Data Bus. In RGMII 1000Mbps, P4_RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P4_RXC and bit[7:4] presented on the falling edge of P4_RXC. In RGMII 10/100Mbps, the received data nibble is presented on P4_RXD[3:0] on the rising edge of P4_RXC and duplicated on the falling edge of P4_RXC.
P4_RXC	-	M1	M1	-	-	I	RGMII Receive Clock. All RGMII received inputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P4_TXC	-	L1	L1	-	-	O	RGMII Transmit Clock. All RGMII transmitted outputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P4_TXD0 P4_TXD1	- -	J1 H1	J1 H1	- -	- -	O	RGMII Transmit Data Bus.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P4_TXD2 P4_TXD3	- -	G1 F1	G1 F1	- -	- -		In RGMII 1000Mbps, P4_TXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P4_TXC and bit[7:4] presented on the falling edge of P4_TXC. In RGMII 10/100Mbps, the transmitted data nibble is presented on P4_TXD[3:0] on the rising edge of P4_TXC and duplicated on the falling edge of P4_TXC.
P4_TXEN	-	K1	K1	-	-	O	RGMII Transmit Control. The P4_TXEN indicates TXEN at rising edge of P4_TXC, and the logical derivative of TXER and TXEN at the falling edge of P4_TXC.
P5_RXDV	-	W24	W24	K25	F19	I	RGMII Receive Control. The P5_RXDV indicates RXDV at rising edge of P5_RXC and the logical derivative of RXER and RXDV at the falling edge of P5_RXC.
P5_RXD0 P5_RXD1 P5_RXD2 P5_RXD3	W24	U24 U25 V24 V25	U24 U25 V24 V25	H25 J24 J25 K24	D19 E18 E19 F18	I	RGMII Receive Data Bus. In RGMII 1000Mbps, P5_RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P5_RXC and bit[7:4] presented on the falling edge of P5_RXC. In RGMII 10/100Mbps, the received data nibble is presented on P5_RXD[3:0] on the rising edge of P5_RXC and duplicated on the falling edge of P5_RXC.
P5_RXC	U24 U25 V24 V25	Y24	Y24	L25	G19	I	RGMII Receive Clock. All RGMII received inputs must be synchronized to this clock. The frequency (with ±50ppm tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_TXC	Y24	AA25	AA25	N24	J18	O	RGMII Transmit Clock. All RGMII transmitted outputs must be synchronized to this clock. The frequency (with $\pm 50\text{ppm}$ tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P5_TXD0 P5_TXD1 P5_TXD2 P5_TXD3	AA25	AC24 AC25 AD24 AD25	AC24 AC25 AD24 AD25	P24 P25 R24 R25	K18 K19 L18 L19	O	RGMII Transmit Data Bus. In RGMII 1000Mbps, P5_TXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P5_TXC and bit[7:4] presented on the falling edge of P5_TXC. In RGMII 10/100Mbps, the transmitted data nibble is presented on P5_TXD[3:0] on the rising edge of P5_TXC and duplicated on the falling edge of P5_TXC.
P5_TXEN	AC24 AC25 AD24 AD25	AB25	AB25	N25	J19	O	RGMII Transmit Control. The P5_TXEN indicates TXEN at rising edge of P5_TXC, and the logical derivative of TXER and TXEN at the falling edge of P5_TXC.
P9_RXDV	K25	K25	K25	-	-	I	RGMII Receive Control. The P9_RXDV indicates RXDV at rising edge of P9_RXC and the logical derivative of RXER and RXDV at the falling edge of P9_RXC.
P9_RXD0 P9_RXD1 P9_RXD2 P9_RXD3	H25 J24 J25 K24	H25	H25 J24 J25 K24	- - - -	- - - -	I	RGMII Receive Data Bus. In RGMII 1000Mbps, P9_RXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P9_RXC and bit[7:4] presented on the falling edge of P9_RXC. In RGMII 10/100Mbps, the received data nibble is presented on P9_RXD[3:0] on the rising edge of

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
							P9_RXC and duplicated on the falling edge of P9_RXC.
P9_RXC	L25	L25	L25	-	-	I	RGMII Receive Clock. All RGMII received inputs must be synchronized to this clock. The frequency (with $\pm 50\text{ppm}$ tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P9_TXC	N24	N24	N24	-	-	O	RGMII Transmit Clock. All RGMII transmitted outputs must be synchronized to this clock. The frequency (with $\pm 50\text{ppm}$ tolerance) depends on the link speed. 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
P9_TXD0 P9_TXD1 P9_TXD2 P9_TXD3	P24 P25 R24 R25	P24 P25 R24 R25	P24 P25 R24 R25	- - - -	- - - -	O	RGMII Transmit Data Bus. In RGMII 1000Mbps, P9_TXD[3:0] runs at a double data rate with bit[3:0] presented on the rising edge of P9_TXC and bit[7:4] presented on the falling edge of P9_TXC. In RGMII 10/100Mbps, the transmitted data nibble is presented on P9_TXD[3:0] on the rising edge of P9_TXC and duplicated on the falling edge of P9_TXC.
P9_TXEN	N25	N25	N25	-	-	O	RGMII Transmit Control. The P9_TXEN indicates TXEN at rising edge of P9_TXC, and the logical derivative of TXER and TXEN at the falling edge of P9_TXC.

6.9. MII MAC Mode Interface Pins

Note. For the RTL9054AN Port 11 MII pins, refer to P5_XXX pins.

Table 11. MII MAC Mode Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_RXDV	-	-	-	P1	H2	I	RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P0_RXD0	-	-	-	V1	K2	I	RXD[3:0] Pin in MII MAC Mode,
P0_RXD1	-	-	-	U1	K1	I	MII Receive Data Bus.
P0_RXD2	-	-	-	T1	J2	I	RXD[3:0] are synchronous to RXC.
P0_RXD3	-	-	-	R1	J1	I	
P0_RXC	-	-	-	M1	G1	I	RXC Pin in MII MAC Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P0_RXER	-	-	-	N1	H1	I	RXER Pin in MII MAC Mode. MII Receive Error. When RXER and RXDV are both asserted, this indicates an error symbol was detected on the cable. RXER is synchronous to RXC.
P0_TXC	-	-	-	L1	E2	I	TXC Pin in MII MAC Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P0_TXD0	-	-	-	J1	D2	O	TXD[3:0] Pin in MII MAC Mode.
P0_TXD1	-	-	-	H1	D1	O	MII Transmit Data Bus.
P0_TXD2	-	-	-	G1	C2	O	TXD[3:0] are synchronous to TXC.
P0_TXD3	-	-	-	F1	C1	O	

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_TXEN	-	-	-	K1	E1	O	TXEN Pin in MII MAC Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P1_RXDV	-	-	-	W24	P18	I	RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P1_RXD0 P1_RXD1 P1_RXD2 P1_RXD3	- - - -	- - - -	- - - -	U24 U25 V24 V25	M18 M19 N18 N19	I	RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. RXD[3:0] are synchronous to RXC.
P1_RXC	-	-	-	Y24	R18	I	RXC Pin in MII MAC Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P1_RXER	-	-	-	W25	P19	I	RXER Pin in MII MAC Mode. MII Receive Error. When RXER and RXDV are both asserted, this indicates an error symbol was detected on the cable. RXER is synchronous to RXC.
P1_TXC	-	-	-	AA25	T19	I	TXC Pin in MII MAC Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_TXD0	-	-	-	AC24	V19		TXD[3:0] Pin in MII MAC Mode.
P1_TXD1	-	-	-	AC25	V18	O	MII Transmit Data Bus.
P1_TXD2	-	-	-	AD24	W18		TXD[3:0] are synchronous to TXC.
P1_TXD3	-	-	-	AD25	V17		
P1_TXEN	-	-	-	AB25	U19	O	TXEN Pin in MII MAC Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P4_RXDV	-	P1	P1	-	-	I	RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P4_RXD0	-	V1	V1	-	-		RXD[3:0] Pin in MII MAC Mode.
P4_RXD1	-	U1	U1	-	-	I	MII Receive Data Bus.
P4_RXD2	-	T1	T1	-	-		RXD[3:0] are synchronous to RXC.
P4_RXD3	-	R1	R1	-	-		
P4_RXC	-	M1	M1	-	-	I	RXC Pin in MII MAC Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P4_RXER	-	N1	N1	-	-	I	RXER Pin in MII MAC Mode. MII Receive Error. When RXER and RXDV are both asserted, this indicates an error symbol was detected on the cable. RXER is synchronous to RXC.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P4_TXC	-	L1	L1	-	-	I	TXC Pin in MII MAC Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P4_TXD0	-	J1	J1	-	-	O	TXD[3:0] Pin in MII MAC Mode.
P4_TXD1	-	H1	H1	-	-	O	MII Transmit Data Bus.
P4_TXD2	-	G1	G1	-	-	O	TXD[3:0] are synchronous to TXC.
P4_TXEN	-	K1	K1	-	-	O	TXEN Pin in MII MAC Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P5_RXDV	W24	W24	W24	K25	F19	I	RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P5_RXD0	U24	U24	U24	H25	D19	I	RXD[3:0] Pin in MII MAC Mode.
P5_RXD1	U25	U25	U25	J24	E18	I	MII Receive Data Bus.
P5_RXD2	V24	V24	V24	J25	E19	I	RXD[3:0] are synchronous to RXC.
P5_RXD3	V25	V25	V25	K24	F18	I	
P5_RXC	Y24	Y24	Y24	L25	G19	I	RXC Pin in MII MAC Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_RXER	W25	W25	W25	L24	G18	I	RXER Pin in MII MAC Mode. MII Receive Error. When RXER and RXDV are both asserted, this indicates an error symbol was detected on the cable. RXER is synchronous to RXC.
P5_TXC	AA25	AA25	AA25	N24	J18	I	TXC Pin in MII MAC Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P5_TXD0 P5_TXD1 P5_TXD2 P5_TXD3	AC24 AC25 AD24 AD25	AC24 AC25 AD24 AD25	AC24 AC25 AD24 AD25	P24 P25 R24 R25	K18 K19 L18 L19	O	TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. TXD[3:0] are synchronous to TXC.
P5_TXEN	AB25	AB25	AB25	N25	J19	O	TXEN Pin in MII MAC Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P9_RXDV	K25	K25	K25	-	-	I	RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P9_RXD0 P9_RXD1 P9_RXD2 P9_RXD3	H25 J24 J25 K24	H25 J24 J25 K24	H25 J24 J25 K24	- - - -	- - - -	I	RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. RXD[3:0] are synchronous to RXC.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P9_RXC	L25	L25	L25	-	-	I	RXC Pin in MII MAC Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P9_RXER	L24	L24	L24	-	-	I	RXER Pin in MII MAC Mode. MII Receive Error. When RXER and RXDV are both asserted, this indicates an error symbol was detected on the cable. RXER is synchronous to RXC.
P9_TXC	N24	N24	N24	-	-	I	TXC Pin in MII MAC Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P9_TXD0 P9_TXD1 P9_TXD2 P9_TXD3	P24 P25 R24 R25	P24 P25 R24 R25	P24 P25 R24 R25	- - - -	- - - -	O	TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. TXD[3:0] are synchronous to TXC.
P9_TXEN	N25	N25	N25	-	-	O	TXEN Pin in MII MAC Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
FE_LED0	G25	G25	G25	-	-	I	CRS pin in MII MAC Mode. This pin is Carrier sense. Half mode is for 10Mbps link speed.
FE_LED1	G24	G24	G24	-	-	I	COL pin in MII MAC Mode. This pin is Collision detect. Half mode is for 10Mbps link speed.

6.10. MII PHY Mode Interface Pins

Note. For the RTL9054AN Port 11 RMII pins, refer to P5_XXX pins.

Table 12. MII PHY Mode Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_RXDV	-	-	-	P1	H2	I	TXEN Pin in MII PHY Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P0_RXD0	-	-	-	V1	K2	I	TXD[3:0] Pin in MII PHY Mode, MII Transmit Data Bus. TXD[3:0] are synchronous to TXC.
P0_RXD1	-	-	-	U1	K1		
P0_RXD2	-	-	-	T1	J2		
P0_RXD3	-	-	-	R1	J1		
P0_RXC	-	-	-	M1	G1	O	TXC Pin in MII PHY Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P0_RXER	-	-	-	N1	H1	I	TXER Pin in MII PHY Mode. MII Transmit Coding Error input signal.
P0_TXC	-	-	-	L1	E2	O	RXC Pin in MII PHY Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_TXD0 P0_TXD1 P0_TXD2 P0_TXD3	- - - -	- - - -	- - - -	J1 H1 G1 F1	D2 D1 C2 C1	O	RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. RXD[3:0] are synchronous to RXC.
P0_TXEN	-	-	-	K1	E1	O	RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P1_RXDV	-	-	-	W24	P18	I	TXEN Pin in MII PHY Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P1_RXD0 P1_RXD1 P1_RXD2 P1_RXD3	- - - -	- - - -	- - - -	U24 U25 V24 V25	M18 M19 N18 N19	I	TXD[3:0] Pin in MII PHY Mode. MII Transmit Data Bus. TXD[3:0] are synchronous to TXC.
P1_RXC	-	-	-	Y24	R18	O	TXC Pin in MII PHY Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P1_RXER	-	-	-	W25	P19	I	TXER Pin in MII PHY Mode. MII Transmit Coding Error input signal.
P1_TXC	-	-	-	AA25	T19	O	RXC Pin in MII PHY Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_TXD0	-	-	-	AC24	V19		RXD[3:0] Pin in MII PHY Mode.
P1_TXD1	-	-	-	AC25	V18	O	MII Receive Data Bus.
P1_TXD2	-	-	-	AD24	W18		RXD[3:0] are synchronous to RXC.
P1_TXD3	-	-	-	AD25	V17		
P1_TXEN	-	-	-	AB25	U19	O	RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P4_RXDV	-	P1	P1	-	-	I	TXEN Pin in MII PHY Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P4_RXD0	-	V1	V1	-	-		TXD[3:0] Pin in MII PHY Mode.
P4_RXD1	-	U1	U1	-	-	I	MII Transmit Data Bus.
P4_RXD2	-	T1	T1	-	-		TXD[3:0] are synchronous to TXC.
P4_RXD3	-	R1	R1	-	-		
P4_RXC	-	M1	M1	-	-	O	TXC Pin in MII PHY Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P4_RXER	-	N1	N1	-	-	I	TXER Pin in MII PHY Mode. MII Transmit Coding Error input signal.
P4_TXC	-	L1	L1	-	-	O	RXC Pin in MII PHY Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P4_TXD0	-	J1	J1	-	-	O	RXD[3:0] Pin in MII PHY Mode.
P4_RXD1	-	H1	H1	-	-	O	MII Receive Data Bus.
P4_RXD2	-	G1	G1	-	-	O	RXD[3:0] are synchronous to RXC.
P4_RXD3	-	F1	F1	-	-	O	
P4_TXEN	-	K1	K1	-	-	O	RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P5_RXDV	W24	W24	W24	K25	F19	I	TXEN Pin in MII PHY Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P5_RXD0	U24	U24	U24	H25	D19	I	TxD[3:0] Pin in MII PHY Mode.
P5_RXD1	U25	U25	U25	J24	E18	I	MII Transmit Data Bus.
P5_RXD2	V24	V24	V24	J25	E19	I	TXD[3:0] are synchronous to TXC.
P5_RXD3	V25	V25	V25	K24	F18	I	
P5_RXC	Y24	Y24	Y24	L25	G19	O	TXC Pin in MII PHY Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P5_RXER	W25	W25	W25	L24	G18	I	TXER Pin in MII PHY Mode. MII Transmit Coding Error input signal.
P5_TXC	AA25	AA25	AA25	N24	J18	O	RXC Pin in MII PHY Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_TXD0 P5_RXD1 P5_RXD2 P5_RXD3	AC24 AC25 AD24 AD25	AC24 AC25 AD24 AD25	AC24 AC25 AD24 AD25	P24 P25 R24 R25	K18 K19 L18 L19	O	RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. RXD[3:0] are synchronous to RXC.
P5_TXEN	AB25	AB25	AB25	N25	J19	O	RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
P9_RXDV	K25	K25	K25	-	-	I	TXEN Pin in MII PHY Mode. MII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to TXC.
P9_RXD0 P9_RXD1 P9_RXD2 P9_RXD3	H25 J24 J25 K24	H25 J24 J25 K24	H25 J24 J25 K24	- - - -	- - - -	I	TXD[3:0] Pin in MII PHY Mode. MII Transmit Data Bus. TXD[3:0] are synchronous to TXC.
P9_RXC	L25	L25	L25	-	-	O	TXC Pin in MII PHY Mode. MII Transmit Clock. All MII transmitted outputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz
P9_RXER	L24	L24	L24	-	-	I	TXER Pin in MII PHY Mode. MII Transmit Coding Error input signal.
P9_TXC	N24	N24	N24	-	-	O	RXC Pin in MII PHY Mode. MII Receive Clock. All MII received inputs must be synchronized to this clock. The frequency depends on the link speed. 100Mbps: 25MHz 10Mbps: 2.5MHz

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P9_RXD0	P24	P24	P24	-	-	O	RXD[3:0] Pin in MII PHY Mode.
P9_RXD1	P25	P25	P25	-	-	O	MII Receive Data Bus.
P9_RXD2	R24	R24	R24	-	-	O	RXD[3:0] are synchronous to RXC.
P9_RXD3	R25	R25	R25	-	-	O	
P9_TXEN	N25	N25	N25	-	-	O	RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.

6.11. RMII Interface Pins

Note. For the RTL9054AN Port 11 RMII pins, refer to P5_XXX pins.

Table 13. RMII Mode Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_RXDV	-	-	-	P1	H2	I	CRSDV Pin in RMII Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is not idle. It is synchronous to REFCLK.
P0_RXD0 P0_RXD1	- -	- -	- -	V1 U1	K2 K1	I	RXD[1:0] Pin in RMII Mode. RMII Receive Data Bus. RXD[1:0] are synchronous to REFCLK.
P0_RXC	-	-	-	M1	G1	I/O	REFCLK Pin in RMII Mode. This pin is bi-directional and configured by the register. All transmissions must be synchronized to this 50MHz clock.
P0_TXD0 P0_TXD1	- -	- -	- -	J1 H1	D2 D1	O	TXD[1:0] Pin in RMII Mode. RMII Transmit Data Bus. TXD[1:0] are synchronous to REFCLK.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_TXEN	-	-	-	K1	E1	O	TXEN Pin in RMII Mode. RMII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to REFCLK.
P1_RXDV	-	-	-	W24	P18	I	CRSDV Pin in RMII Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is not idle. It is synchronous to REFCLK.
P1_RXD0 P1_RXD1	- -	- -	- -	U24 U25	M18 M19	I	RXD[1:0] Pin in RMII Mode. RMII Receive Data Bus. RXD[1:0] are synchronous to REFCLK.
P1_RXC	-	-	-	Y24	R18	I/O	REFCLK Pin in RMII Mode. This pin is bi-directional and configured by the register. All transmissions must be synchronized to this 50MHz clock.
P1_TXD0 P1_TXD1	- -	- -	- -	AC24 AC25	V19 V18	O	TXD[1:0] Pin in RMII Mode. RMII Transmit Data Bus. TXD[1:0] are synchronous to REFCLK.
P1_TXEN	-	-	-	AB25	U19	O	TXEN Pin in RMII Mode. RMII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to REFCLK.
P4_RXDV	-	P1	P1	-	-	I	CRSDV Pin in RMII Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is not idle. It is synchronous to REFCLK.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P4_RXD0 P4_RXD1	- -	V1 U1	V1 U1	- -	- -	I	RXD[1:0] Pin in RMII Mode. RMII Receive Data Bus. RXD[1:0] are synchronous to REFCLK.
P4_RXC	-	M1	M1	-	-	I/O	REFCLK Pin in RMII Mode. This pin is bi-directional and configured by the register. All transmissions must be synchronized to this 50MHz clock.
P4_TXD0 P4_TXD1	- -	J1 H1	J1 H1	- -	- -	O	TXD[1:0] Pin in RMII Mode. RMII Transmit Data Bus. TXD[1:0] are synchronous to REFCLK.
P4_TXEN	-	K1	K1	-	-	O	TXEN Pin in RMII Mode. RMII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to REFCLK.
P5_RXDV	W24	W24	W24	K25	F19	I	CRSDV Pin in RMII Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is not idle. It is synchronous to REFCLK.
P5_RXD0 P5_RXD1	U24 U25	U24 U25	U24 U25	H25 J24	D19 E18	I	RXD[1:0] Pin in RMII Mode. RMII Receive Data Bus. RXD[1:0] are synchronous to REFCLK.
P5_RXC	Y24	Y24	Y24	L25	G19	I/O	REFCLK Pin in RMII Mode. This pin is bi-directional and configured by the register. All transmissions must be synchronized to this 50MHz clock.
P5_TXD0 P5_TXD1	AC24 AC25	AC24 AC25	AC24 AC25	P24 P25	K18 K19	O	TXD[1:0] Pin in RMII Mode. RMII Transmit Data Bus. TXD[1:0] are synchronous to REFCLK.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_TXEN	AB25	AB25	AB25	N25	J19	O	TXEN Pin in RMII Mode. RMII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to REFCLK.
P9_RXDV	K25	K25	K25	-	-	I	CRSDV Pin in RMII Mode. Carrier Sense/Receive Data Valid. This synchronous input is asserted by the PHY when the receive medium is not idle. It is synchronous to REFCLK.
P9_RXD0 P9_RXD1	H25 J24	H25 J24	H25 J24	- -	- -	I	RXD[1:0] Pin in RMII Mode. RMII Receive Data Bus. RXD[1:0] are synchronous to REFCLK.
P9_RXC	L25	L25	L25	-	-	I/O	REFCLK Pin in RMII Mode. This pin is bi-directional and configured by the register. All transmissions must be synchronized to this 50MHz clock.
P9_TXD0 P9_TXD1	P24 P25	P24 P25	P24 P25	- -	- -	O	TXD[1:0] Pin in RMII Mode. RMII Transmit Data Bus. TXD[1:0] are synchronous to REFCLK.
P9_TXEN	N25	N25	N25	-	-	O	TXEN Pin in RMII Mode. RMII Transmit Enable. This synchronous output is asserted when valid data is driven on TXD. TXEN is synchronous to REFCLK.

6.12. LED Interface Pins

Table 14. Parallel LED IC Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_LED	D22	D22	D22	D24	H15	O	Port 0 Link/Act Indication LED. The D22 is TDO for the RTL9075AAD /RTL9072AAD. The D24 is TRST for the RTL9068AAD. The H15 is TRST for the RTL9068ABD. They are sharing pins. It can be switched by TAPSL[1:0].
P1_LED	D21	D21	D21	D25	J16	O	Port 1 Link/Act Indication LED.
P2_LED	C24	C24	C24	E24	J15	O	Port 2 Link/Act Indication LED. The E24 is shared with TDI for the RTL9068AAD. The J15 is shared with TDI for the RTL9068ABD. It can be switched by TAPSL[1:0]. Keep floating if not use LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
P3_LED	C25	C25	C25	E25	K15	O	Port 3 Link/Act Indication LED.
P4_LED	D24	D24	D24	-	-	O	Port P4 Link/Act Indication LED. This pin is shared with TRST. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_LED	D25	D25	D25	F24	L15	O	Port 5 Link/Act Indication LED. The L15 is shared with TCK for the RTL9068ABD. The F24 is shared with TCK for the RTL9068AAD. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
P6_LED	E24	E24	E24	F25	M15	O	Port 6 Link/Act Indication LED. The E24 is shared with TDI for the RTL9075AAD/RTL9072AAD. The F25 is shared with TMS for RTL9068AAD. The M15 is shared with TMS for RTL9068ABD. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
P7_LED	E25	E25	E25	-	-	O	Port 7 Link/Act Indication LED.
P9_LED	-	-	F24	-	-	O	Port 9 Link/Act Indication LED. This pin is shared with TCK. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
P10_LED	-	-	F25	-	-	O	Port 10 Link/Act Indication LED. This pin is shared with TMS. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P12_LED	F24	F24	-	-	-	O	Port 12 Link/Act Indication LED. This pin is shared with TCK. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
P13_LED	F25	F25	-	-	-	O	Port 13 Link/Act Indication LED. This pin is shared with TMS. It can be switched by TAPSL[1:0]. Keep floating if not using the LED and MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress function.
FE_LED0	G25	G25	G25	G25	N15	O	FE PHY LED0. 10 Mbps Link/Act Indication LED. This is a shared pin (CRS in MII MAC Mode) for RTL9075/72.
FE_LED1	G24	G24	G24	G24	P15	O	FE PHY LED1. 100 Mbps Link/Act Indication LED. This is a shared pin (COL in MII MAC Mode) for RTL9075/72.

6.13. I2C Pins

Table 15. I2C Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOA_1	Y1	Y1	Y1	Y1	M1	I	I2C Clock. The I2C is in slave mode for external host device access. The clock is fed into the SCK pin.
GPIOA_2	AA1	AA1	AA1	AA1	N1	I/O	I2C Data Input/Output. The I2C changes to slave mode. The external host device can access the DUT's register via I2C.

6.14. MDC/MDIO Interface Pins

Table 16. MDC/MDIO Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOA_1	Y1	Y1	Y1	Y1	M1	I	Management Data Clock.
GPIOA_2	AA1	AA1	AA1	AA1	N1	I/O	Input/Output of Management Data. Weak pull up GPIO_VDDIO0.

6.15. SPI Slave Interface Pins

Table 17. SPI Slave Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOA_0	W1	W1	W1	W1	L1	I	SPIS_CSI. Low active. Output from master.
GPIOA_1	Y1	Y1	Y1	Y1	M1	I	SPIS_CK. Serial Clock Output from master.
GPIOA_2	AA1	AA1	AA1	AA1	N1	I	SPIS_DI. Data input from master to DUT.
GPIOA_3	AB1	AB1	AB1	AB1	P1	O	SPIS_DO. Data output for master from DUT.

6.16. Miscellaneous Interface Pins

Table 18. Miscellaneous Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
XI	B25	B25	B25	B25	A13	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz \pm 50ppm tolerance crystal reference input. When a crystal is used, a loading capacitor should be connected between this pin and ground.
XO	A24	A24	A24	A24	A12	AO	25MHz Crystal Clock Output Pin.
RESETB	AD1	AD1	AD1	AD1	T1	AI	System Pin Reset Input. Weak pull the RESETB Pin low to force the RTL9054/RTL9068/RTL907x to reset all the circuits. To complete the reset function, this pin must be asserted for at least 10ms. It must be weak pulled high for normal operation.
RSET	A16	A16	A16	A16	A10	AO	Reference Resistor for PHY Bandgap. A 24K Ω (1%) resistor should be connected between RSET and GND.
RTT_CKDIG	D16	D16	D16	D16	D11	AO	Output 25Mhz/125Mhz Clock. Configured by register. Moreover, it is configurable to output slave jitter (TX_TCLK) of 100BASE-T1 PHY for UNH IOL test. <i>Note. This pin is for test only. It cannot be used as the clock source to other devices.</i>

6.17. GPIO Interface Pins

Table 19. GPIO Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOA [3:0]	AB1, AA1 Y1, W1	AB1, AA1 Y1, W1	AB1, AA1 Y1, W1	AB1, AA1 Y1, W1	P1, N1 M1, L1	I/O	General Purpose Input/output Pins. GPIOA is a shared pin with the accessing register interface.
GPIOB [2:0]	AA2, Y2 W2	AA2, Y2 W2	AA2, Y2 W2	AA2, Y2 W2	N2, M2 L2	I/O	General Purpose Output Pins. GPIOB0 is a shared pin with the INT function. The default is GPIO. It can be switched to INT via register. GPIOB1 and GPIOB2 are a shared pin with the PTP Time Application Interface (TAI) function. The default is PTP TAI function. It can be switched to GPIO via register.
GPIOC [5:0]	P4, V2 U2, T2 R2, P2	P4, V2 U2, T2 R2, P2	P4, V2 U2, T2 R2, P2	P4, V2 U2, T2 R2, P2	N5, N4 M5, M4 L5, L4	I/O	General Purpose Output Pins.
GPIOD [2:0]	T4, R5 R4	T4, R5 R4	T4, R5 R4	T4, R5 R4	R9, P5 P4	I/O	General Purpose Output Pins. GPIOD[1:0] is a shared pin with MDC/MDIO master.
GPIOE [4:0]	AA7, AB7 AB6, AA6 T5	AA7, AB7 AB6, AA6 T5	AA7, AB7 AB6, AA6 T5	AA7, AB7 AB6, AA6 T5	N8, M7 N7, R8 R7	I/O	General Purpose Output Pins.
GPIOF [4:0]	AA11, AA10 AA9, W9 AA8	AA11, AA10 AA9, W9 AA8	AA11, AA10 AA9, W9 AA8	AA11, AA10 AA9, W9 AA8	N9, J8 K8, L8 M8	I/O	General Purpose Output Pins.

6.18. CPU Interface Pins

Table 20. CPU Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOB_0	W2	W2	W2	W2	L2	I/O	Interrupt Output. Outputs the interrupt signal to inform the external host device of interrupt events. This pin is a shared pin for GPIOB_0 and INT.
GPIOB_1	Y2	Y2	Y2	Y2	M2	I/O	PTP Time Application Interface function. GPIOB_1 is a shared pin with the PTP Time Application Interface (TAI) function. The default is PTP TAI function. It can be switched to GPIO via register.
GPIOB_2	AA2	AA2	AA2	AA2	N2	I/O	PTP Time Application Interface function. GPIOB_2 is a shared pin with the PTP Time Application Interface (TAI) function. The default is PTP TAI function. It can be switched to GPIO via register.

6.19. MDC/MDIO Master Interface Pins

Table 21. MDC/MDIO Master Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOD_0	R4	R4	R4	R4	P4	O	Management Data Clock.
GPIOD_1	R5	R5	R5	R5	P5	I/O	Input/Output of Management Data. Weak pull up GPIO_VDDIO0.

6.20. SPI Master Interface Pins

Table 22. SPI master Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
SPI_CSB	AB22	AB22	AB22	AB22	L16	O	Chip Select Output. Active low.
SPI_SCK	AA20	AA20	AA20	AA20	P16	O	Serial Clock Output.
SPI_SIO0	AB20	AB20	AB20	AB20	R16	I/O (2/4 channel) O (1 channel)	2/4 channel: Serial Data Input/Output 1 channel: Data from switch to flash.
SPI_SIO1	AA21	AA21	AA21	AA21	M16	I/O (2/4 channel) I (1 channel)	2/4 channel: Serial Data Input/output 1 channel: Data from flash to switch <i>Note: Place a 0-ohm resistor to ground at SPI_SIO1 pin if flash- less mode is used. Remove this 0ohm resistor when the flash is attached.</i>
SPI_SIO2	AA22	AA22	AA22	AA22	K16	I/O (4 channel) N/A (1/2 channel)	4 channel: Serial Data Input/output 1/2 channel: No function
SPI_SIO3	AB21	AB21	AB21	AB21	N16	I/O (4 channel) N/A (1/2 channel)	4 channel: Serial Data Input/output 1/2 channel: No function

6.21. Boundary Scan Interface & Debug

Table 23. Boundary Scan Interface & Debug Interface Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
TAPSL [1:0]	AC1, AC2	AC1, AC2	AC1, AC2	AC1, AC2	R2, P2	I	Select LED or boundary scan interface & debug. TAPSEL[1:0] = 2b00: Normal function. 2b01: MBIST/LBIST/Boundary Scan/TestKompress/Parallel TestKompress 2b10: Normal function with debug interfaces. LED are debug interfaces 2b11: Normal function within boot up memory BIST
P0_LED	D22	D22	D22	D24	H15	I/O	TDO (Test Data out) for the RTL9075AAD/RTL9072AAD and data direction is I/O. TRST (Test reset) for the RTL9068AAD/RTL9068ABD and data direction is I. It can be switched by TAPSL[1:0].
TDO	-	-	-	D22	H16	I/O	TDO (Test Data out). It can be switched by TAPSL[1:0].
P2_LED	-	-	-	E24	J15	I/O	TDI (Test Data in). It can be switched by TAPSL[1:0].
P4_LED	D24	D24	D24	-	-	I	TRST (Test reset). It can be switched by TAPSL[1:0].
P5_LED	-	-	-	F24	L15	I	TCK (Test clock). It can be switched by TAPSL[1:0].
P6_LED	E24	E24	E24	F25	M15	I/O	TDI (Test Data in) for the RTL9075AAD/RTL9072AAD and data direction is I/O. TMS (Test mode select) for the RTL9068AAD/RTL9068ABD and data direction is I. It can be switched by TAPSL[1:0].
P9_LED	-	-	F24	-	-	I	TCK (Test clock). It can be switched by TAPSL[1:0].
P10_LED	-	-	F25	-	-	I	TMS (Test mode select). It can be switched by TAPSL[1:0].

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P12_LED	F24	F24	-	-	-	I	TCK (Test clock). It can be switched by TAPSL[1:0].
P13_LED	F25	F25	-	-	-	I	TMS (Test mode select). It can be switched by TAPSL[1:0].
ATN ATP	-	D19 D18	D19 D18	D19 D18	B16 B15	AO	Debug output Differential pair for 1000BASE-T1.

6.22. Automotive Related Pins

Table 24. Automotive Related Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
DISB	AD2	AD2	AD2	AD2	R1	I	Disable packet transmission. Active low.
WAKE	J4	J4	J4	J4	K4	I	Local Wake-up Input.
INH	G4	G4	G4	G4	J4	OD (PM OS)	Inhibit Output for External Voltage Switching Regulator.

6.23. Regulator Pins

Table 25. Regulator Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_LDOIN	-	-	-	K5, L5	J7, K7	P	Power input for P0 LDO. If there is no need to provide power to the P0 RGMII/MII/RMII, this still provides 3.3V to this input, and keeps floating the output pins (P0_LDOOUT).
P0_LDOO_UT	-	-	-	L4, M4	H7, H8	P	With capacitance of at least 0.1uF, to enhance the stability of output voltage connect to P0_VDDIO. If not using LDO, please keep floating for this pin.
P1_LDOIN	-	-	-	E22, F22	H13, J13	P	Power input for P1 LDO. If not using LDO, please keep floating for this pin.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_LDOO_UT	-	-	-	G22, H22	K13, L13	P	With capacitance of at least 0.1uF, to enhance the stability of output voltage connect to P1_VDDIO. If not using LDO, please keep floating for this pin.
P4_LDOIN	K5, L5	K5, L5	K5, L5	-	-	P	Power input for P4 LDO. If there is no need to provide power to the P4 RGMII/MII/RMII, this still provides 3.3V to this input and keeps floating the output pins (P4_LDOOUT).
P4_LDOOUT	L4, M4	L4, M4	L4, M4	-	-	P	With capacitance of at least 0.1uF, to enhance the stability of output voltage connect to P4_VDDIO. If not using LDO, please keep floating for this pin.
P5_LDOIN	E22, F22	E22, F22	E22, F22	E21, F21	H12, J12	P	Power input for P5 LDO. If not using LDO, please keep floating for this pin.
P5_LDOOUT	G22, H22	G22, H22	G22, H22	G21, H21	K12, L12	P	With capacitance of at least 0.1uF, to enhance the stability of output voltage connect to P5_VDDIO. If not using LDO, please keep floating for this pin.
P9_LDOIN	E21, F21	E21, F21	E21, F21	-	-	P	Power input for P9 LDO. If not using LDO, please keep floating for this pin.
P9_LDOOUT	G21, H21	G21, H21	G21, H21	-	-	P	With capacitance of at least 0.1uF, to enhance the stability of output voltage connect to P9_VDDIO. If not using LDO, please keep floating for this pin.

6.24. Power Controller Pins

Table 26. Power Controller Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
VSENSE	-	D4	D4	D4	F4	AO	Control P/N MOSFET.
PGATE	-	D5	D5	D5	H5	-	Connect P-MOSFET.
NGATE	-	D6	D6	D6	F5	-	Connect N-MOSFET.
VO09	-	E4	E4	E4	G4	P	Connect to output power from MOSFET.
AVDD33_HVD	-	E5	E5	E5	J5	P	Connect to the same analog power with P/N MOSFET Attach at least 22uF close to this pin.
AVDD33_AHV	-	E6	E6	E6	G5	P	Connect to analog 3.3V.
GND_HGD	-	F5	F5	F5	K5	G	Connect to the same ground with P/N MOSFET.

6.25. Configuration Strapping Pins

Table 27. Configuration Strapping Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOA_3	AB1	AB1	AB1	AB1	P1	I	Determines whether, after all power is stable and RESETB is released, DUT automatically enters normal function mode or not. This pin is also called ST_CHG. 1b0: Manual 1b1: Automatic
P5_TXD [2]	AD24	AD24	AD24	-	-	I	Boot selection. P5_TXD2 (RTL9075/72AA)
P1_TXD [2]	-	-	-	AD24	W18	I	P1_TXD2 (RTL9068AA/AB) 1b0: Pure Flash Mode 1b1: ROM + Patch Mode Other options reserved.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GPIOC [5:0]	P4, V2 U2, T2 R2, P2	P4, V2 U2, T2 R2, P2	P4, V2 U2, T2 R2, P2	P4, V2 -, - -, -	N5, N4 -, - -, -	I	Send remote wake up capability. 1b0: No sending remote wake up capability 1b1: Port n can send remote wake For RTL9075AAD/ RTL9072AAD GPIOC0: Port 0 GPIOC1: Port 1 GPIOC5: Port 5 For RTL9068AAD/ RTL9068ABD GPIOC4: Port 0 GPIOC5: Port 1
GPIOF [3:0]	AA10, AA9 W9, AA8	AA10, AA9 W9, AA8	AA10, AA9 W9, AA8	AA10, AA9 W9, AA8	J8, K8 L8, M8	I	Send remote wake up capability. 1b0: No sending remote wake up capability 1b1: Port n can send remote wake For RTL9075AAD/RTL9054AN GPIOF0: Port 12 GPIOF1: Port 13 GPIOF2: Port 6 GPIOF3: Port 7 For RTL9072AAD GPIOF0: Port 9 GPIOF1: Port 10 GPIOF2: Port 6 GPIOF3: Port 7 For RTL9068AAD/ RTL9068ABD GPIOF0: Port 5 GPIOF1: Port 6 GPIOF2: Port 2 GPIOF3: Port 3
P5_TXD [1:0]	AC25, AC24	AC25, AC24	AC25, AC24	-	-	I	Configures GPIOA[3:0] function.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P1_TXD [1:0]	-	-	-	AC25, AC24	V18, V19	I	2b00: GPIOA[3:0] is I ² C slave for external accesses DUT's registers 2b01: SPI slave for external accesses DUT's registers 2b10: GPIOA 2b11: MDC/MDIO slave for external accesses DUT's registers
P5_TXD [2:1]	-	-	-	R24, P25	L18, K19	I	Change both of I2C and MDC/MDIO id. Change last two bits of address. 00b: I ² C Device Address = 0x04/mdx slave ID = 0x18 01b: I ² C Device Address = 0x05/mdx slave ID = 0x19 10b: I ² C Device Address = 0x06/mdx slave ID = 0x1A 11b: I ² C Device Address = 0x07/mdx slave ID = 0x1B
P9_TXD [2:1]	R24, P25	R24, P25	R24, P25	-	-	I	00b: I ² C Device Address = 0x04/mdx slave ID = 0x18 01b: I ² C Device Address = 0x05/mdx slave ID = 0x19 10b: I ² C Device Address = 0x06/mdx slave ID = 0x1A 11b: I ² C Device Address = 0x07/mdx slave ID = 0x1B
P5_TXD [3]	AD25	AD25	AD25	-	-	I	Enable stacking boots. P5_TXD3 (RTL9075/72AA)
P1_TXD [3]	-	-	-	AD25	V17	I	P1_TXD3 (RTL9068AA/AB) 1b0: Disable 1b1: Enable
P4_TXD [0]	J1	J1	J1	-	-	I	Port S0 for stacking. P4_TXD0 (RTL9075/72AA)
P0_TXD [0]	-	-	-	J1	J1	I	P0_TXD0 (RTL9068AA/AB) 1b0: Disable 1b1: Enable
P4_TXD [1]	H1	H1	H1	-	-	I	Port S1 for stacking. P4_TXD1 (RTL9075/72AA)
P0_TXD [1]	-	-	-	H1	H1	I	P0_TXD1 (RTL9068AA/AB) 1b0: Disable 1b1: Enable
P4_TXD [2]	G1	G1	G1	-	-	I	Stacking Boot Role. P4_TXD2 (RTL9075/72AA)
P0_TXD [2]	-	-	-	G1	G1	I	P0_TXD2 (RTL9068AA/AB) 1b0: Stacking Master 1b1: Stacking Slave

6.26. Power and GND Pins

Table 28. Power and GND Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
AVDD09	B8, B9, B10			E4, E5		P	Analog Power 0.9V.
AVDD09_CMU	AB9, AB10			V8, V9		P	Analog Power 0.9V for USXGMII/HSGMII/PCI Express.
AVDD09_FE	D13, E13			A8, D8		P	Analog Power 0.9V for Fast Ethernet.
AVDD09_GIGA	B17			D16, E16		P	Analog Power 0.9V for 1000BASE-T1.
AVDD09_MCK	E19, E20			D15, E15		P	Analog Power 0.9V for 1000BASE-T1.
AVDD09_RX	AD13, AD14			V4, V5		P	Analog Power 0.9V for USXGMII/HSGMII/PCI Express.
AVDD09_SGMII	AB13, AB14, AB15			T13, T14		P	Analog Power 0.9V for SGMII.
AVDD09_TX	AB11, AA12 AB12, AD12			V10, V11		P	Analog Power 0.9V for USXGMII/HSGMII/PCI Express transmitting.
AVDD33	B2, B3, B4			D4, D5		P	Analog Power 3.3V.
AVDD33_HVD	E5			J5		P	Connect to the same analog power with P/N MOSFET. Attach at least 22uF close to this pin.
AVDD33_CEN	D17			B14		P	Analog Power 3.3V.
AVDD33_CKDIG	E16			E11		P	Analog Power 3.3V.
AVDD33_CMU	AB8, AD8			T9, T10		P	Analog Power 3.3V.
AVDD33_DIG	B5, B6, B7			D6, E6		P	Analog Power 3.3V.
AVDD33_FE	D14, E14			D7, E7		P	Analog Power 3.3V for Fast Ethernet.
AVDD33_MCK	D20			B17, B18		P	Analog Power 3.3V.
AVDD33_P2	-	-	-	B18, B19	F15, G15	P	Analog Power 3.3V for 1000BASE-T1.
AVDD33_P3	-	-	-	B20, B21	F16, G16	P	Analog Power 3.3V for 1000BASE-T1.
AVDD33_P6	B18, B19	B18, B19	B18, B19	-	-	P	Analog Power 3.3V for 1000BASE-T1.
AVDD33_P7	B20, B21	B20, B21	B20, B21	-	-	P	Analog Power 3.3V for 1000BASE-T1.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
AVDD33_AHV		E6			G5	P	Connect to analog 3.3V.
AVDD33_SGMII		AB16, AB17, AB18			T15, T16 V16	P	Analog Power 3.3V for SGMII.
AVDD33_XTAL		B23			B12, B13	P	Analog Power 3.3V for XTAL.
DVDD09	U4, V4, H5, J5, N5, P5, U5, V5, W11, J21, K21, L21, M21				G8, H9 J9, K9 L9, M10 N10, M11 N11, M12 N12	P	Digital Core Power 0.9V.
DVDD33		J22, K22			M13, N13	P	Digital IO Power 3.3V for Digital IO Interface.
GPIO0_VDDIO		AB2, N4			L7	P	GPIO digital IO power 1.8V, 2.5V or 3.3V for GPIOA[3:0], GPIOB[2:0], and GPIOC[5:0].
GPIO1_VDDIO		W7, W8			M9	P	GPIO digital IO power 1.8V, 2.5V or 3.3V for GPIOD[4:0], GPIOE[4:0], and GPIOF[4:0].
MAC_VDDIO		U7, V7			R6, T6	P	The digital IO power 1.8V, 2.5V or 3.3V for TAPSEL[1:0], RESETB, DISB, Px_PCIE_RESETB, x_LANWAKEB, x_CLKREQB, and x_ISOLATEB.
P0_VDDIO	-	-	-	J2, K2 M2, N2	B1, F1 F2	P	Digital IO Power 1.8V, 2.5V or 3.3V for P0 RGMII/MII/RMII IO.
P1_VDDIO	-	-	-	T24, AA24 T25, Y25	T18, R19	P	Digital IO Power 1.8V, 2.5V or 3.3V for P1 RGMII/MII/RMII IO. Keep supplying power even when not using this interface as P1_TXD are configurations strapping pins.
P4_VDDIO	J2, K2 M2, N2	J2, K2 M2, N2	J2, K2 M2, N2	-	-	P	Digital IO Power 1.8V, 2.5V or 3.3V for P4 RGMII/MII/RMII IO.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P5_VDDIO	T24, AA24 T25, Y25	T24, AA24 T25, Y25	T24, AA24 T25, Y25	H24, M24 M25	D18, H18 H19	P	Digital IO Power 1.8V, 2.5V or 3.3V for P5 RGMII/MII/RMII IO. Keep supplying power even when not using this interface as P5_TXD are configurations strapping pins.
P9_VDDIO	H24, M24 M25	H24, M24 M25	H24, M24 M25	-	-	P	Digital IO Power 1.8V, 2.5V or 3.3V for P9 RGMII/MII/RMII IO.
SPI_VDDIO	Y21, Y22				R15	P	SPI master IO Power 3.3V/2.5V/1.8V for SPI master IO Interface. Keep supplying power even when not using SPI Flash.
VBAT	-	H4			G7	P	12V/24V for operation mode.
V33	H4	-	-	-	-	P	Connect to independent 3.3V <i>Note. In RTL9054, the function of V33 is the same with VBAT in RTL9068/RTL907x</i>
GND	A1, D1, E1, AE1, C2, F2, G2, H2, AE2, AD3, AE3, F4, K4, G5, M5, D7, E7, G7, H7, J7, K7, L7, M7, N7, P7, R7, D8, E8, G8, H8, J8, K8, L8, M8, N8, P8, R8, T8, D9, E9, G9, H9, J9, K9, L9, M9, N9, P9, R9, T9, D10, E10, G10, H10, J10, K10, L10, M10, N10, P10, R10, T10, U10, V10, W10, D11, E11, G11, H11, J11, K11, L11, M11, N11, P11, R11, T11, U11, V11, A12, D12, E12, G12, H12, J12, K12, L12, M12, N12, P12, R12, T12, U12, V12, W12, B13, G13, H13, J13, K13, L13, M13, N13, P13, R13, T13, U13, V13, W13, G14, H14, J14, K14, L14, M14, N14, P14, R14, T14, U14, V14, W14, A15, D15, E15, G15, H15, J15, K15, L15, M15, N15, P15, R15, T15, U15, V15, W15, B16, G16, H16, J16, K16, L16, M16, N16, P16, R16, T16, U16, V16, W16, A17, E17, G17, H17, J17, K17, L17, M17, N17, P17, R17, T17, U17, V17, W17, E18, G18, H18, J18, K18, L18, M18, N18, P18, R18, T18, U18, V18, W18, G19, H19, J19, K19, L19, M19, N19, P19, R19, T19, U19, V19, W19, N21, P21, R21, T21, U21, V21, W21, A22, B22, L22, M22, N22, P22, R22, T22, U22, V22, W22, A23, B24, AE24, A25, AE25				A1,W1 B2,H4 E8,A9 B9,D9 E9,G9 B10,D10 E10,G10 H10,J10 K10,L10 R10,A11 B11,G11 H11,J11 K11,L11 R11,D12 E12,G12 R12,D13 E13,G13 R13,A14 D14,E14 R14,C18 A19,B19 C19,W19	G	Ground.

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
GND_SERDES		AD4, AE4, AD6, AD7, AD9, AD11			W2, T7, W7, T8, T11, T12	G	Ground for USXGMII/HSGMII/PCI Express.
GND_SGMII		AA13, AA14, AA15, AA16, AA17, AA18, AA19, AB19, AD23, AE23			W12, W17	G	Ground for SGMII.
GND_HGD		F5			K5	G	Ground. Connect to P/N MOSFET.

6.27. Test Pins

Table 29. Test Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
P0_TESTD	-	-	-	L2	G2	O	For 100BASE-T1 PCS testing mode. It is RXER pin in 100BASE-T1 PCS test mode. 100BASE-T1 PCS test mode is only for 100BASE-T1 PCS test. Acts like RXER.
P1_TESTD	-	-	-	AB24	U18	O	For 100BASE-T1 PCS testing mode. It is RXER pin in 100BASE-T1 PCS test mode. 100BASE-T1 PCS test mode is only for 100BASE-T1 PCS test. Acts like RXER.
P4_TESTD	L2	L2	L2	-	-	O	For 100BASE-T1 PCS testing mode. It is RXER pin in 100BASE-T1 PCS test mode. 100BASE-T1 PCS test mode is only for 100BASE-T1 PCS test. Acts like RXER.
P5_TESTD	AB24	AB24	AB24	-	-	O	For 100BASE-T1 PCS testing mode. It is RXER pin in 100BASE-T1 PCS test mode. 100BASE-T1 PCS test mode is only for 100BASE-T1 PCS test. Acts like RXER.
TESTB	F1, G1, H1, J1, K1, L1, L2, M1, N1, P1, R1, T1, U1, V1	-	-	-	-	O	Keep floating.

6.28. Other Pins

Table 30. Other Pins

Pin Name	Pin No RTL9054AN	Pin No RTL9075AAD	Pin No RTL9072AAD	Pin No RTL9068AAD	Pin No RTL9068ABD	Type	Description
NC	T7, U8, V8, U9, V9, W4, W5, Y4, Y5, AA4, AA5, AB4, AB5, AD5, AD10, AE5, AE6, AE7, AE8, AE9, AE10, AE11, AE12, AE13, AE14, AD19, AD20, AD21, AD22, AE19, AE20, AE21, AE22, D4, D5, D6 E4, E5, E6 F5	T7, U8 V8, U9 V9	T7, U8 V8, U9 V9	B1, C1 A2, D2 E2, A3 A4, A5 T7, U8 V8, U9 V9, AD19 AE19, AD20 AE20, D21 AD21, AE21 AD22, AE22 C24, C25	-	-	Not Connected.

7. Interface Function Overview

7.1. 100BASE-T1 & 1000BASE-T1 MDI Interfaces

The RTL9054/RTL9068/RTL907x integrates multiple 100BASE-T1 and 1000BASE-T1 PHY transceivers. In contrast to the conventional Ethernet MDI interfaces, 100BASE-T1 PHY / 1000BASE-T1 PHYs utilizes a single pair of wires (MDIP / MDIN) for data transmission.

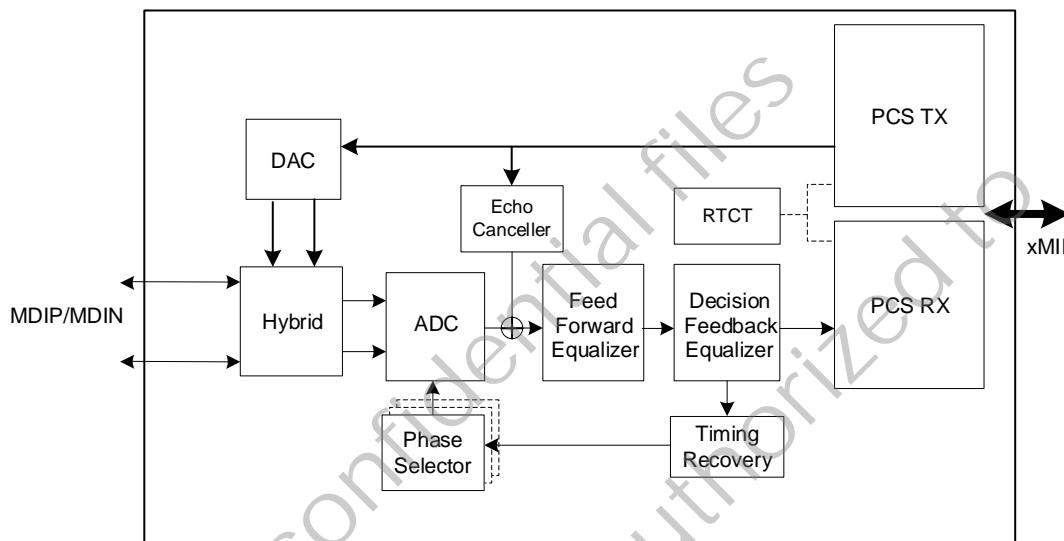


Figure 17. 100BASE-T1/1000BASE-T1 PHY Block Diagram

7.1.1. Transmitter

The PCS layer receives data bytes from the MAC through the xMII interface and performs generation of continuous code-groups through 2D-PAM3 coding technology. These code groups are transmitted onto the twisted pair cable at 750M Baud/s (for 1000BASE-T1 PHY) / 66.67M Baud/s (for 100BASE-T1 PHY) through a Digital to Analog (D/A) converter, then the analog signal passes through a filter to minimize EMI effect.

7.1.2. Receiver

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, echo cancellation, timing recovery, and 2D-PAM3 decoding. The recovered data is sent through the xMII interface to the MAC.

7.1.3. PHY Roles

Two types of PHY role, master and slave, are defined in 100BASE-T1 and 1000BASE-T1. To make the 100BASE-T1/1000BASE-T1 PHYs link up, the PHY's role needs to be the opposite at each side, i.e. a slave to a master. The user can configure the PHY's role using the RTL9054/RTL9068/RTL907x's port PHY role register.

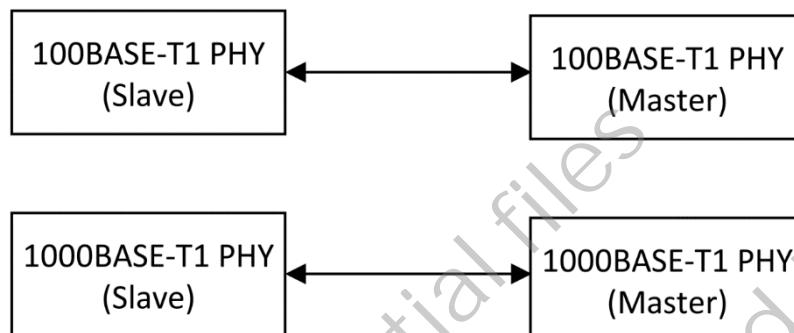


Figure 18. Master and Slave Roles in 100BASE-T1/1000BASE-T1

7.2. FE PHY MDI Interfaces

The RTL9054/RTL9068/RTL907x embeds one Fast Ethernet PHY. The Fast Ethernet PHY uses a single common MDI interface to support 100BASE-TX and 10BASE-T. This interface consists of two signal pairs Px_MDIPB/Px_MDINB, and Px_MDIPA/Px_MDINA. The MDI interface has internal termination resistors for reduced BOM cost and PCB complexity. Table 31 shows the mapping between the pairs and the RJ-45 signals.

Table 31. Mapping of Twisted-Pair Outputs to RJ-45 Connectors

Pairs	RJ-45 Pin
A	1 and 2
B	3 and 6

7.2.1. 100BASE-TX Transmitter

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.2.2. 100BASE-TX Receiver

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.2.3. 10BASE-T Transmitter

The output 10BASE-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.2.4. 10BASE-T Receiver

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.5. Auto-Negotiation for UTP

The RTL9054/RTL9068/RTL907x obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL9054/RTL9068/RTL907x advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.2.6. Crossover Detection and Auto Correction

The RTL9054/RTL9068/RTL907x automatically determines whether or not it needs to crossover between pairs (see Table 32) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary the RTL9054/RTL9068/RTL907x automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The RTL9054/RTL9068/RTL907x crossover detection and auto correction function is enabled by default. The pin mapping in MDI and MDI Crossover mode is given below.

Table 32. Media Dependent Interface Pin Mapping

Pairs	MDI		MDI Crossover	
	100BASE-TX	10BASE-T	100BASE-TX	10BASE-T
A	TX	TX	RX	RX
B	RX	RX	TX	TX

7.2.7. Polarity Correction

The RTL9054/RTL9068/RTL907x automatically corrects polarity errors on the receiver pairs in 10BASE-T mode. In 100BASE-TX mode, the polarity is irrelevant.

In 10BASE-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when the link is down.

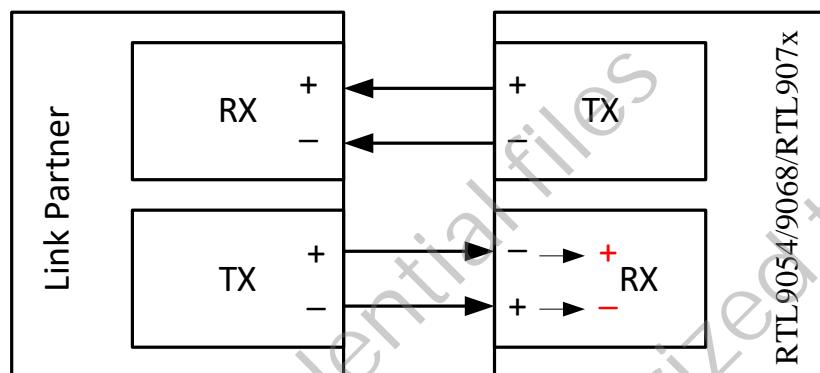


Figure 19. Conceptual Example of Polarity Correction

7.2.8. Green Ethernet

7.2.8.1 Link-On Cable Length Power Saving

The RTL9054/RTL9068/RTL907x FE PHY supports auto-detection of cable length and dynamic power adjustment according to the detected cable length on the physical link. This feature provides high performance with minimum power consumption.

7.2.8.2 Link-Down Power Saving

The RTL9054/RTL9068/RTL907x FE PHY implements link-down power saving for each PHY, greatly reducing power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

7.3. SPI (Serial Peripheral Interface)

The Serial Peripheral Interface (SPI) is used to communicate with an external SPI FLASH. The SPI FLASH stores code and data for the ARM of the RTL9054/RTL9068/RTL907x.

The RTL9054/RTL9068/RTL907x's support memory size of SPI FLASH is 8Mbit ~ 128Mbit. The SPI FLASH can be read, erased, and programmed by the ARM CPU or external CPU. The SPI clock rate can be configured from 12.5MHz to 100MHz, and the SPI channel number can also be configured as 1, 2 or 4 to access SPI FLASH. The SPI FLASH speed and channel configurations must get programmed into the SPI FLASH. The RTL9054/RTL9068/RTL907x read flash speed and channel configurations from flash are 12.5MHz while power on or reset, and then the speed and the channel will be changed to the configuration in flash content. Hence, the SPI FLASH supports 12.5MHz.

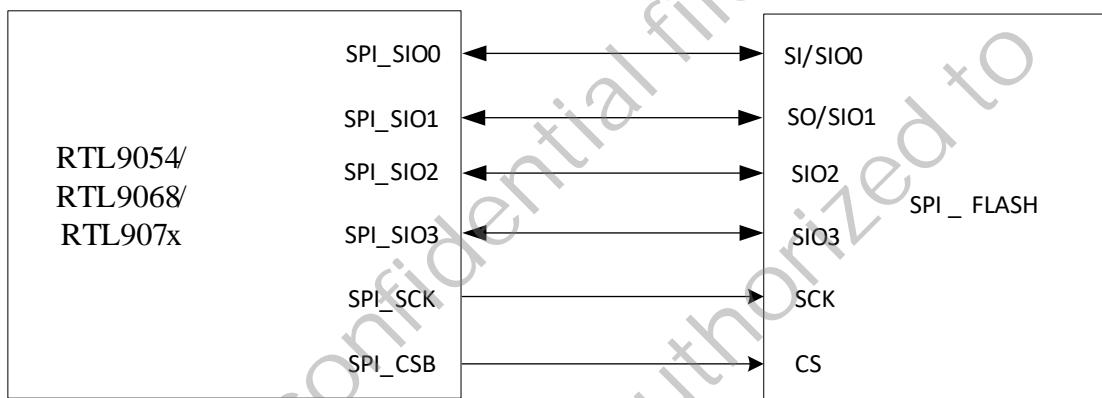


Figure 20. SPI Interface Diagram

7.4. MAC Interface

The RTL9054/RTL9068/RTL907x supports various powerful interfaces allowing the MAC to easily connect to an external CPU. The link information of the MACs and the external partner device, such as speed, duplex, and link status, should be set manually. The speed and link status of the MACs can be configured via registers or SPI FLASH. Note that the RTL9054/RTL9068/RTL907x only supports full-duplex for all interfaces except Port 9 MII 10Mbps half-duplex for the RTL9075AAD.

7.4.1. RGMII

The Reduced Gigabit Media Independent Interface (RGMII) needs less pin count than GMII. It supports 1000Mbps, 100Mbps, and 10Mbps full-duplex speeds. The RGMII RX delay and TX delay options are set by the registers.

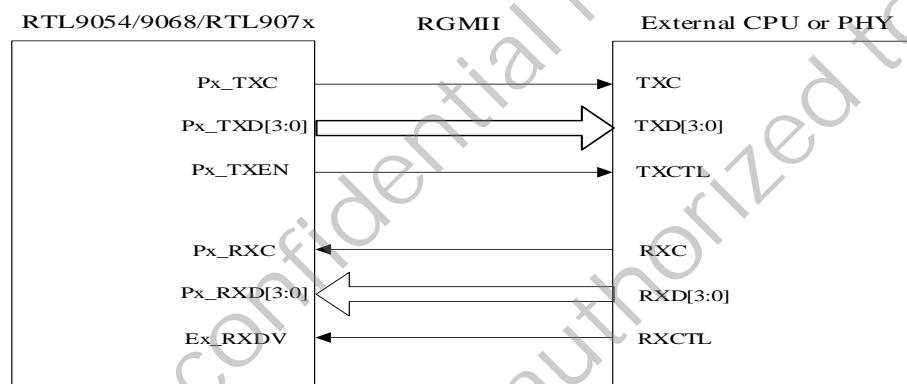


Figure 21. RGMII Signal Diagram

7.4.2. MII MAC Mode

The MII MAC mode is selected via registers. The signal diagram of MAC mode is shown in Figure 22.

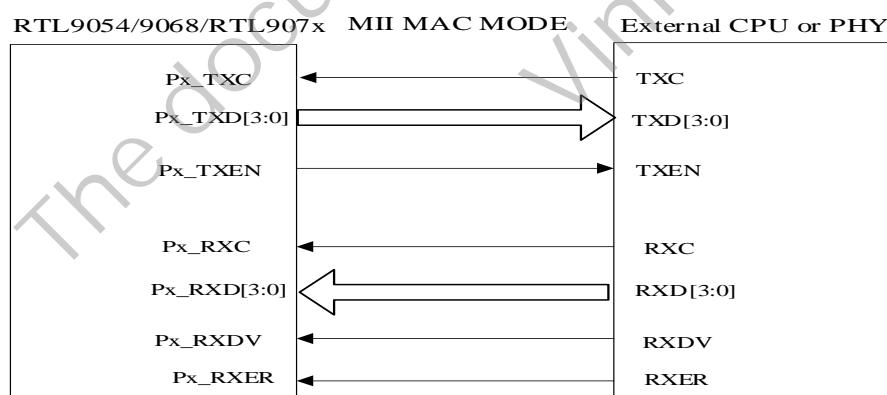


Figure 22. MII MAC Mode Signal Diagram

In MII MAC mode, TXCLK and RXCLK are the transmitting and receiving reference clock pins. The data bus width of MII is 4 bits.

7.4.3. MII PHY Mode

The MII PHY mode is selected via registers. MII at the PHY part drives the transmitting and receiving reference clock. Figure 23 shows the signal diagram for MII PHY mode.

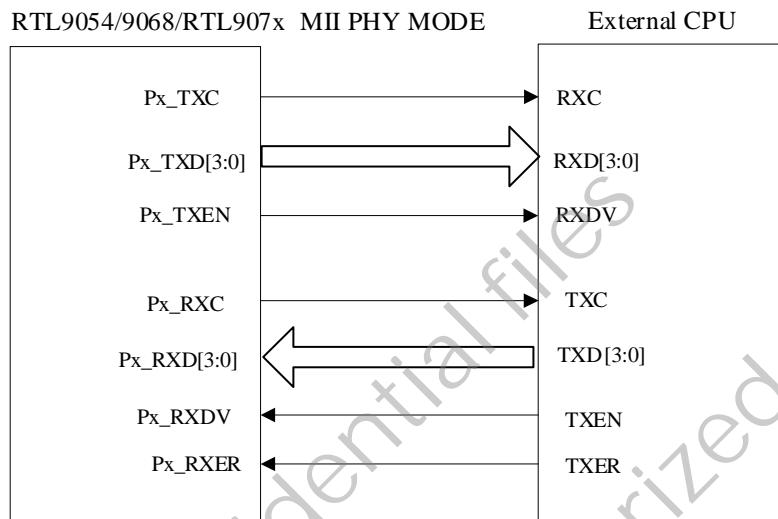


Figure 23. MII PHY Mode Signal Diagram

7.4.4. RMII

The RTL9054/RTL9068/RTL907x supports RMII (Reduced MII) 1.0 MAC mode used in 10/100Mbps full-duplex only. The reference clock pin of the RTL9054/RTL9068/RTL907x RMII can be configured to output a 50MHz clock, or be driven by an external clock source. The direction of the reference clock signal is controlled by the register.

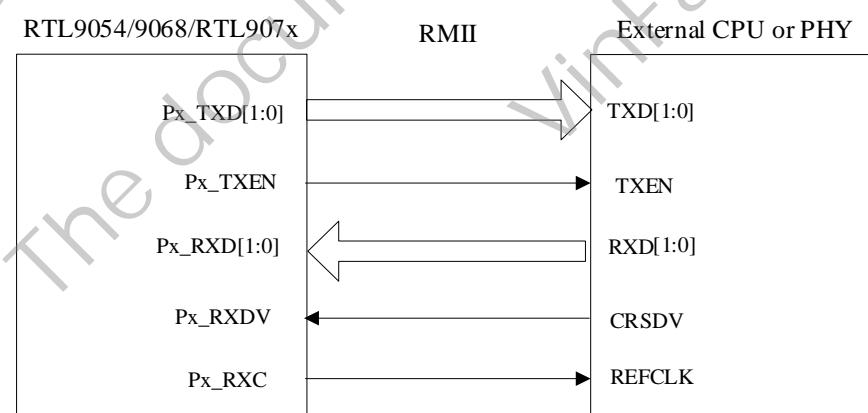


Figure 24. RMII Output Signal Diagram

7.4.5. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a follow-on from MII, a standard interface used to connect a MAC-block to a PHY. It is used for Gigabit Ethernet (Ethernet/Fast Ethernet uses MII). It differs from GMII/MII by its low-power requirements and low-pin-count serial interface (commonly referred to as SerDes).

To carry frame data and link rate information between a 10/100/1000 PHY and an Ethernet MAC, SGMII uses a differential pair for data signals, with both being present in each direction (i.e., transmit and receive). The data signals operate at 1.25G. Due to the high speed of operation, the use of differential pairs provides signal integrity while minimizing system noise. Only CML mode is supported in RTL9068/RTL907x.

The following diagram refers to the Serial-GMII Specification of Cisco, to help understand the usage of Auto-Negotiation in both MAC and PHY mode.

Figure 25 illustrates the simple connections in a system utilizing SGMII.

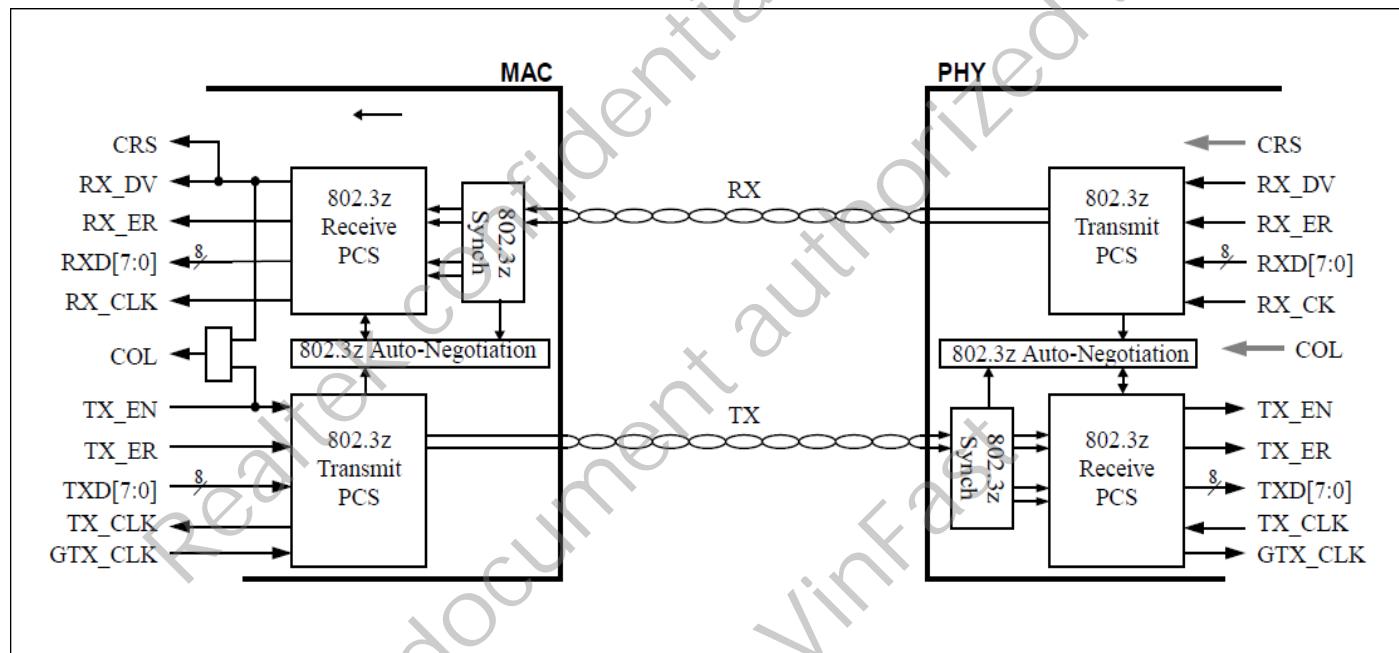


Figure 25. SGMII Connectivity

The transmit and receive data paths leverage the 1000BASE-SX PCS defined in the IEEE802.3z specification (clause 36). The traditional GMII data signals (TXD/RXD), data valid signals (TX_EN/RX_DV), and error signals (TX_ER/RX_ER) are encoded, serialized and output with the appropriate DDR clocking. Thus it is a 1.25G baud interface with a 625 MHz clock. Carrier Sense (CRS) is derived/inferred from RX_DV, and Collision (COL) is logically derived in the MAC when RX_DV and TX_EN are simultaneously asserted.

Control information, as specified in Table 33, is transferred from the PHY to the MAC to signal the change of the control information. This is achieved by using the Auto-Negotiation functionality defined in Clause 37 of the IEEE Specification 802.3z.

Instead of the ability advertisement, the PHY sends the control information via its tx_config_Reg[15:0] as specified in Table 1 whenever the control information changes. Upon receiving control information, the MAC acknowledges the update of the control information by asserting bit 14 of its tx_config_reg{15:0} as specified in Table 1.

SGMII details source synchronous clocking; however, specific implementations may desire to recover the clock from the data rather than use the supplied clock. This operation is allowed; however, all sources of data must generate the appropriate clock regardless of how they clock receive data.

Table 33. Definition of Control Information Passed Between Links Via tx_config_Reg[15:0]

Bit Number	tx_config_Reg[15:0] sent from the PHY to the MAC	tx_config_Reg[15:0] sent from the MAC to the PHY
15	Link: 1 = link up, 0 = link down	0: Reserved for future use
14	Reserved for Auto-Negotiation acknowledge as specified in 802.3z	1
13	0: Reserved for future use	0: Reserved for future use
12	Duplex mode: 1 = full duplex, 0 = half duplex	0: Reserved for future use
11:10	Speed: Bit 11, 10: 1 1 = Reserved 1 0 = 1000 Mbps: 1000BASE-TX, 1000BASE-X 0 1 = 100 Mbps: 100BASE-TX, 100BASE-FX 0 0 = 10 Mbps: 10BASET, 10BASE2, 10BASE5	0: Reserved for future use
9:1	0: Reserved for future use	0: Reserved for future use
0	1	1

Clearly, SGMII's 1.25G baud transfer rate is excessive for interfaces operating at 10 or 100 Mbps. When these situations occur, the interface “elongates” the frame by replicating each frame byte 10 times for 100 Mbps and 100 types for 10 Mbps. This frame elongation takes place “above” the 802.3z PCS layer, thus the start frame delimiter only appears once per frame.

7.4.6. HSGMII

The High Serial Gigabit Media Independent Interface (HSGMII) is an enhanced clock rate from SGMII, a standard interface used to connect a MAC-block to a PHY. It is used for Gigabit Ethernet (Ethernet/Fast Ethernet uses MII). It differs from GMII/MII by its low-power requirements and low-pin-count serial interface (commonly referred to as SerDes).

To carry frame data and link rate information between a 2500 PHY and an Ethernet MAC, HSGMII uses a differential pair for data signals, with both being present in each direction (i.e., transmit and receive). The data signals operate at 3.125G. Due to the high speed of operation, the use of differential pairs provides signal integrity while minimizing system noise.

For Auto-Negotiation behavior similar to SGMII, please refer to 7.4.5.

7.4.7. USXGMII

USXGMII uses two data signals in each direction to convey frame data and link rate information between a single or multi-port PHY and the Ethernet MAC(s). The data signals operate at 5.15625G/baud. Due to the high speed of operation, each of these signal pairs are realized as differential pairs thus optimizing signal integrity while minimizing system noise.

USXGMII leverages the 64B/66B PCS defined in IEEE 803.2ae Clause 49. The PCS is unchanged with additional functionality being added via the “ordered set” mechanism defined by IEEE.

For Auto-Negotiation behavior similar to SGMII, please refer to 7.4.5.

7.4.8. PCI-Express (PCI-E)

The RTL9068/RTL907x complies with Peripheral Component Interconnect Express (PCI-E) Base 3.0 Specification with X1 link width, i.e., one transmit and one receive differential pair. PCI-E 3.0 carries a bit rate of 8 GT/s, and it is backward compatible with existing PCI-E implementations. PCI-E 3.0 improves the encoding scheme from the previous 8b/10b to 128b/130b encoder. It reduces the bandwidth overhead from 20% of PCI-E 2.0 to approximately 1.54%.

The RTL9068/RTL907x’s PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 128B/130B coding technology. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 128B/130B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system. The data code groups are passed through its serializer for packet framing. The generated 8 GT/s serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

The RTL9068/RTL907x’s PCI Express block receives 8 GT/s serial data from its upstream device to generate parallel data. The receiver’s PLL circuits are re-synchronized to maintain bit and symbol lock. Through 128B/130B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL9068/RTL907x’s internal Ethernet MAC to be transmitted onto the Ethernet media.

The RTL9068/RTL907x uses PCI-E 3.0 interface to support up to 5 Gbps Ethernet throughput.

The diagram below shows how the RTL9068/RTL907x connects with the external SoC pin-by-pin.

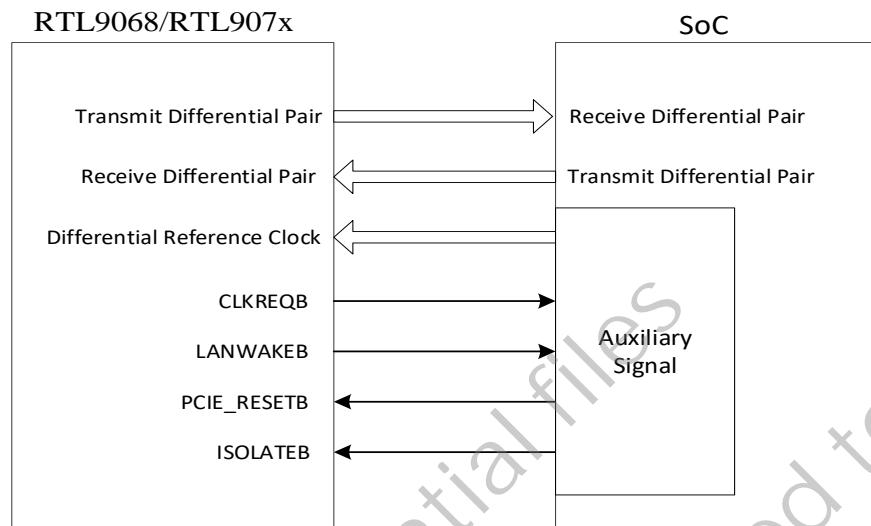


Figure 26. PCI-E Signal Diagram

In PCI-E architecture, the RTL9068/RTL907x acts as a PCI-E endpoint which is connected to the PCI-E root complex of the PCI-E host. The RTL9068/RTL907x Linux driver is provided and integrated on the PCI-E host for accessing the RTL9068/RTL907x. The main task of the driver is to communicate between the user applications and the RTL9068/RTL907x by passing the packets, controlling The RTL9068/RTL907x, and retrieving the RTL9068/RTL907x's status and so on.

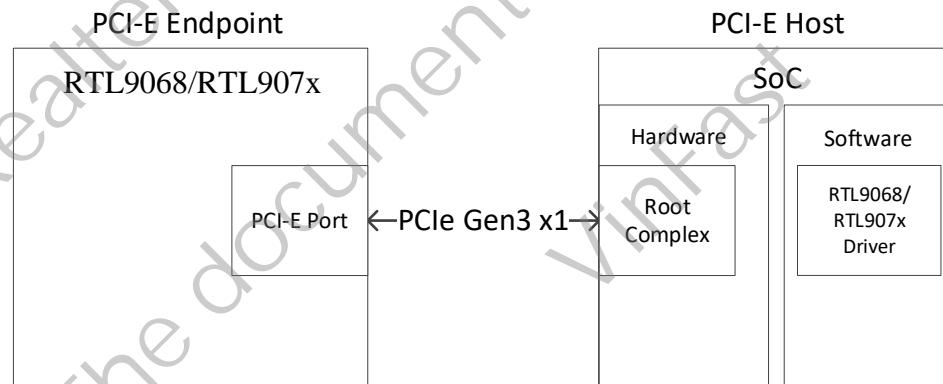


Figure 27. PCI-E End Point and Host

7.5. I2C Slave Mode for External CPU Access

The RTL9054/RTL9068/RTL907x supports a serial CPU interface (I2C slave mode) to access the internal registers (including all MAC and PHY configuration registers). The device address is 3 bytes, and the LSB 2bit must be ignored. There are two I/O pins (SDA and SCK) for the I2C. SDA is the access data signal, and SCK is the clock signal. The read/write data sequence is shown in Figure 28. It consists of a control byte (1 byte) + address bytes (3 bytes) + data bytes (4N pieces, N: Integer, N ≠ 0).

When the external CPU wants to read/write data from/to the RTL9054/RTL9068/RTL907x, it must set the read/write bit (read is 1, and write is 0) correspondingly.

Note: Use the indirect channel to access the OPFSM register as the register response time in the OPFSM domain is longer. Refer to section 7.8 for details.

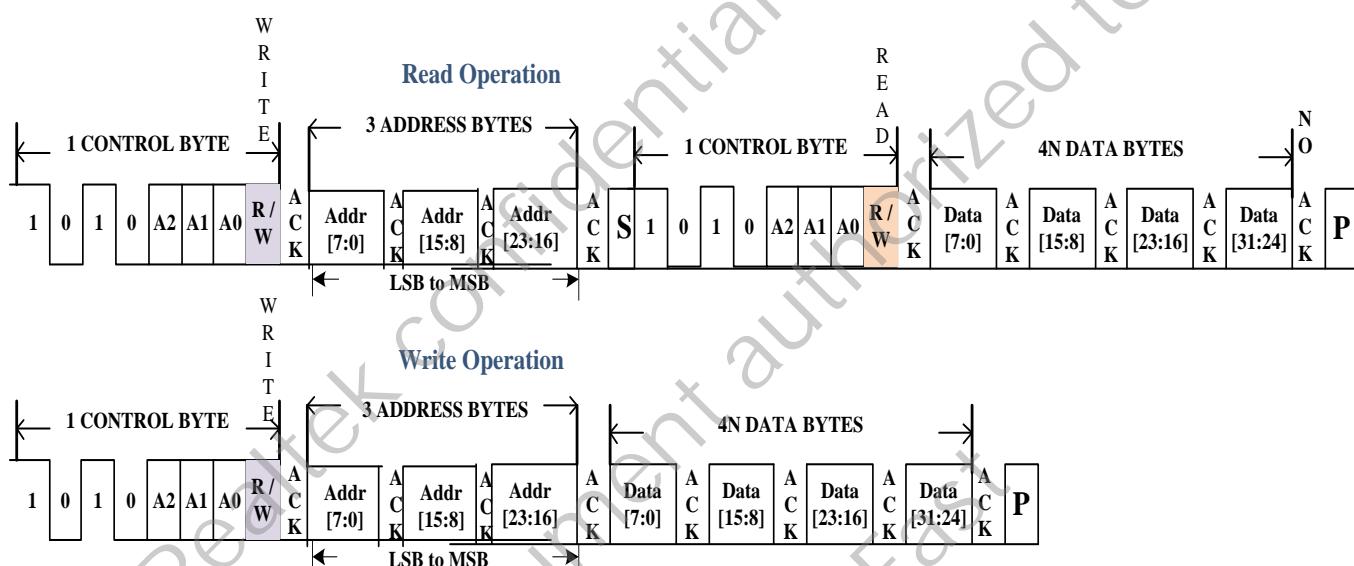


Figure 28. Serial CPU Interface Access Data Sequence

7.6. MDC/MDIO Slave for External CPU Access

The RTL9054/RTL9068/RTL907x supports a standard MDC/MDIO interface to access the internal registers. There are two pins in this interface protocol, MDC and MDIO. MDC is the clock to synchronize two side devices, and the MDIO is the data signal.

7.6.1. Protocol Operation

The read/write data sequence consists of a preamble which is at least a 32 bit 1'b. After the preamble we have the start pattern and OP code. The read and write operation depends on the OP code. The register access channel consists of a 3 byte address and 4 byte data. As it is the same as the two-wire serial interfaces; the LSB 2bit of the address must be ignored.

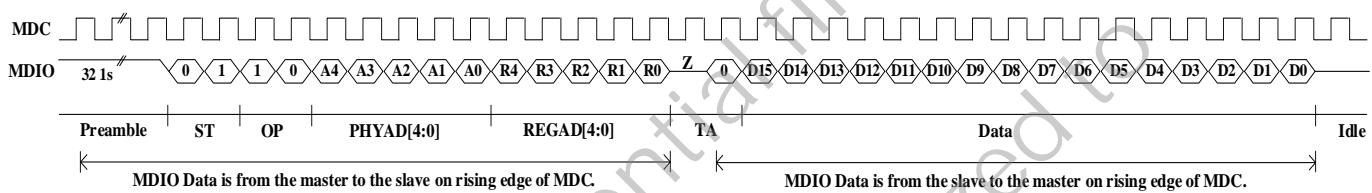


Figure 29. MDC/MDIO Read Operation Timing

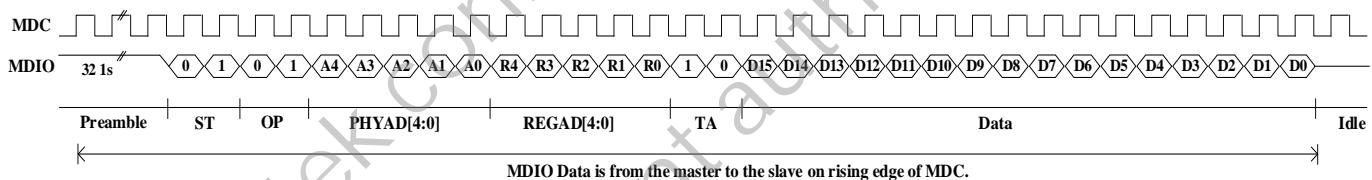


Figure 30. MDC/MDIO Write Operation Timing

7.6.2. Register Access

The MDC/MDIO provides a pseudo PHY register list to access internal switch registers (Table 34), and the default pseudo PHY ID is 0x18 which is configurable to other values. During a read register operation, the external CPU uses standard MDC/MDIO protocols to write the address to MDC_Reg_Addr and set MDC_Reg_Wr to READ.

The MDC/MDIO data is limited to 2 bytes. If there is data larger than 2 bytes, multiple MDC/MDIO commands need to be issued. To set the switch register data (4 bytes) through the MDC/MDIO protocol, two MDC/MDIO commands need to be issued. For example, write LSB 2 bytes to REGAD 0 and MSB 2 bytes to REGAD 2. The read flow is shown below:

1. Set MDC_Reg_Data to 0. Write 0 to REGAD 0 and 2.
2. Set switch's register address, command, and enable bit. Set switch address. Write LSB two bytes to REGAD 4. The MSB switch's register address, MDC_Reg_Wr and Enable bit must be written with the same MDC/MDIO command. For example, if the switch address is 0x123456, we write 0x3456 to REGAD 4, and 0x8012 to REGAD 6.
3. Wait for MDC_Reg_En to change to 0. This signals that the hardware finished the operation.
4. Read MDC_Reg_Data (4 bytes). It again requires two MDC/MDIO commands. LSB 2 bytes are stored at REGAD 0, and the MSB 2 bytes are stored at REGAD 2.

The write switch register flow is as follows:

1. Set data to MDC_Reg_Data. Set LSB 2 bytes to REGAD 0, and MSB 2 bytes to REGAD 2.
2. Set the switch's register address, command, and enable bit. For example, if the switch address is 0x123456, we write 0x3456 to REGAD 4 and 0x8112 to REGAD 6.
3. Wait for MDC_Reg_En to change to 0.

Table 34. Pseudo PHY Register for MDC/MDIO Access

REGAD	Bit	Name	Description	Mode	Default
6	15	MDC_Reg_En	MDC/MDIO interface access Enable bit. When Test IO access trigger Set = 1, wait until the switch moves data and clean it.	R/W	0
	[14:9]	Reserved	-	R/W	0
	8	MDC_Reg_Wr	0: Read operation 1: Write operation	R/W	-
	[7:0]	MDC_Reg_Addr	Switch register address the MSB.	R/W	0
4	[15:0]		Switch register address, 3bytes length, 4byte alignment, and the LSB 2bit is ignored.	R/W	0
2	[15:0]	MDC_Reg_Data	Switch register MSB 2 bytes data.	R/W	0
0	[15:0]		Switch register LSB 2 bytes data.	R/W	0

7.7. SPI Slave for External CPU Access

The RTL9054/RTL9068/RTL907x supports an SPI-Slave Management Interface that can be enabled via Pin configuration. An External CPU can configure or manage the RTL9054/RTL9068/RTL907x's internal register through the SPI interface.

When the CPU writes data to the RTL9054/RTL9068/RTL907x's internal register via the SPI interface, the first 8-bits are OP code, and the write command OP codes are 8h'02 (Write command) or 8h'03 (Read command). The following three bytes are the address bytes of the register. After the address bytes, there are four bytes for the data to be read or written.

Since the RTL9054/RTL9068/RTL907x's bus structure causes the slave delay to access register, the read operation needs to use the dummy cycle to match the delay time.

Note: Use the indirect channel to access the OPFSM register as the register response time in the OPFSM domain is longer. Refer to section 7.8 for details.

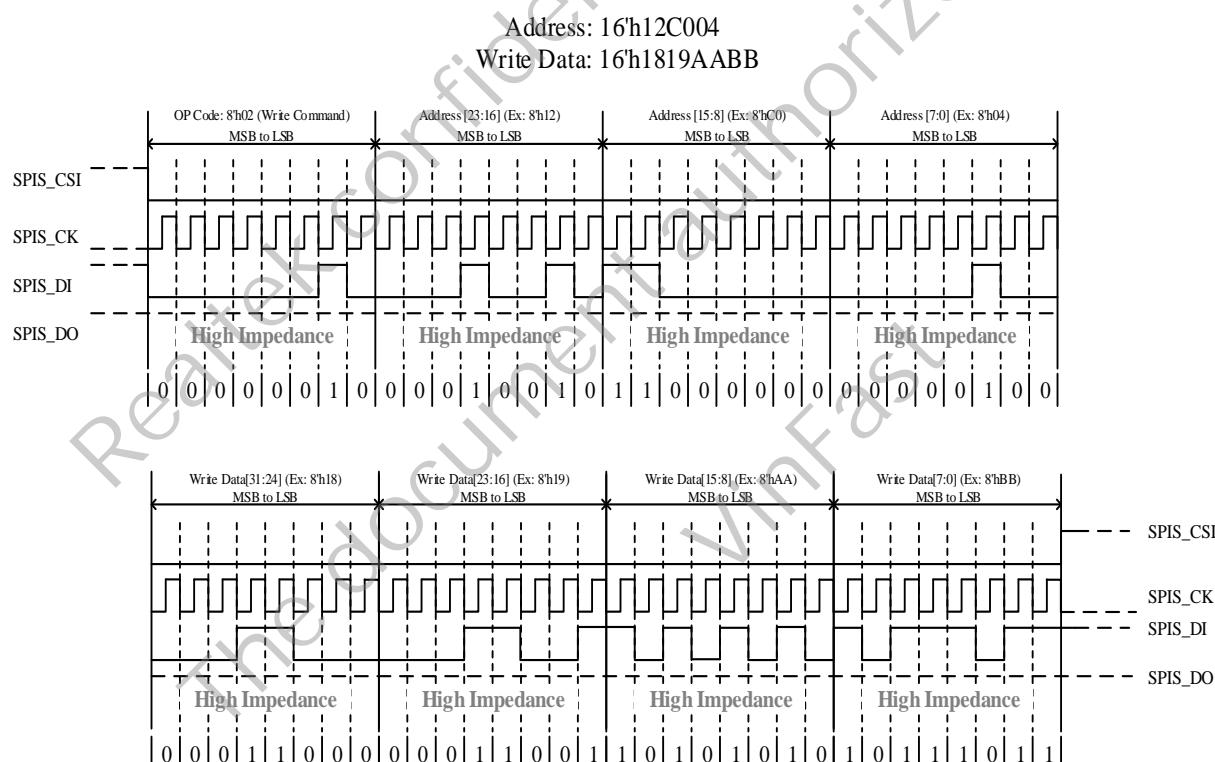


Figure 31. SPI-Slave Write Command Access Format

Address: 16'h12C004
Read Data 16'h1819AABB

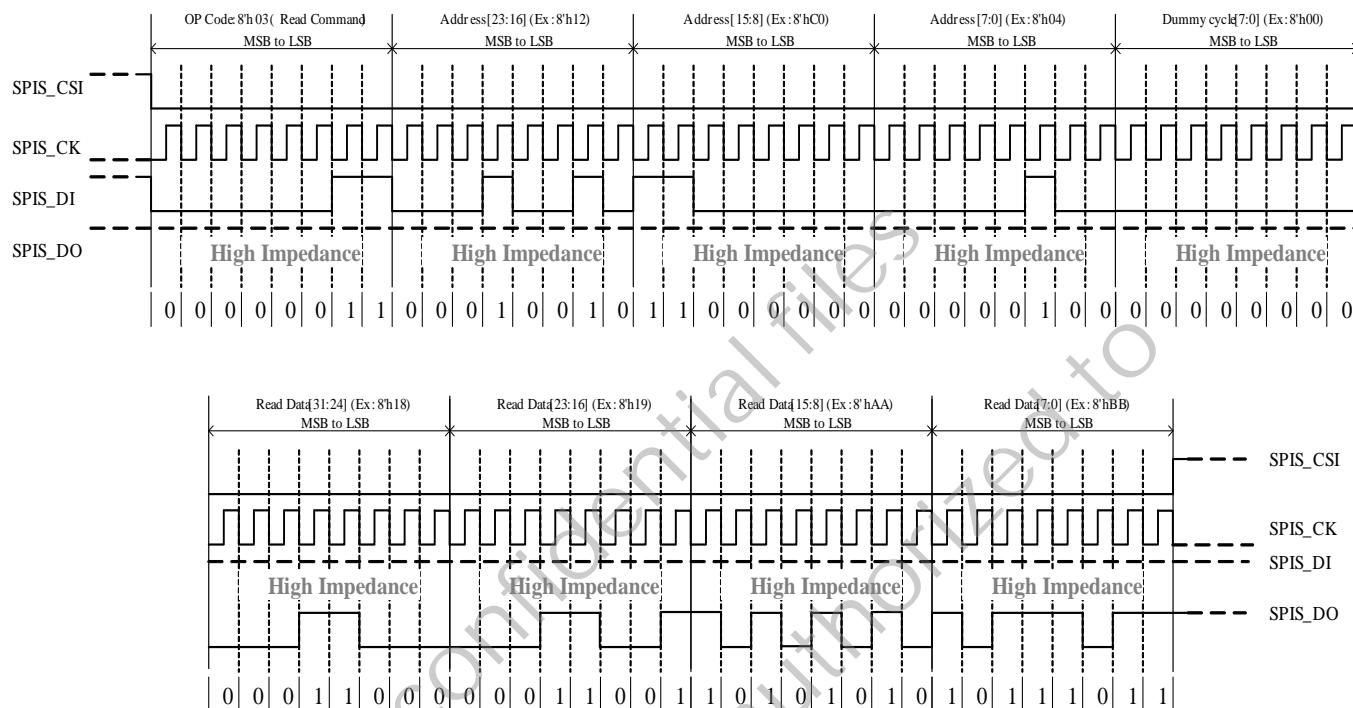


Figure 32. SPI-Slave Read Command Access Format

7.8. I2C/SPI Slave Indirect Access

The OPFSM domain register (Address 0x4A001000 ~ 0x4A0017FF) response time is longer than other registers. Therefore, to access the OPFSM domain register through I2C and SPI, use the indirect channel instead of direct access. The read flow is shown below:

1. Set Reg_Data to 0. Write 0 to address 0xFFFF15.
2. Set switch's register address, read operation, and enable bit. Set switch address. The Reg_Addr, Reg_RW, Reg_Byte_En and Reg_En must be written with the same access. For example, if the switch address is 0x1620, we write 0x3D001620 to address 0xFFFF11.
3. Wait for Reg_Access_Ack to change to 1. This signals the hardware finished the operation.
4. Read Reg_Data at address 0xFFFF15.

The write switch register flow is as follows:

1. Set data to Reg_Data at address 0xFFFF15.
2. Set switch's register address, write operation, and enable bit. For example, if switch address is 0x1620, we write 0x3F001620 to address 0xFFFF11.
3. Wait for Reg_Access_Ack to change to 1.

Table 35. Pseudo Register for I2C/SPI Indirect Access

Address	Bit	Name	Description	Mode	Default
0xFFFF11	31	Reg_Access_Ack	It means process is finished. 0: Not finished 1: Finished	RO	0
	30	Reserved	-	RO	0
	[29:26]	Reg_Byte_En	Byte enable. 4'b1111: Select 4-byte data to transmit/receive from byte 0 4'b0001: Select 1-byte data to transmit/receive from byte 0 (only used in SPI controller)	R/W	0x0
	25	Reg_RW	It means read/write operation to access register. 0: Read operation 1: Write operation	R/W	0
	24	Reg_En	Indirect access Enable bit. 0: Complete access 1: Execute access	R/W	0
	[23:0]	Reg_Addr	Switch register address, 3bytes length, 4byte alignment.	R/W	0
0xFFFF15	[31:0]	Reg_Data	Switch register address, 3bytes length, 4byte alignment, the LSB 2bit are ignored.	R/W	0

7.9. Unused Pin Layout Guide

The following table shows how to layout pins when not using an interface.

Table 36. Unused Pin Layout Guide

Interface	Pin Name	Action
Px 100BASE-T1/1000BASE-T1	Px_MDIP	Floating.
	Px_MDIN	Floating.
SGMII/USXGMII/HSGMII/PCI-E	Px_HSON	Floating.
	Px_HSOP	Floating.
	P6/P7/P8/P9_HSIN	Weak pull low (ex. 10kohm) to ground.
	P6/P7/P8/P9_HSIP	Weak pull low (ex. 10kohm) to ground.
	P10/P11_HSIN	Weak pull high (ex. 10kohm) to 0.9V domain.
	P10/P11_HSIP	Weak pull high (ex. 10kohm) to 0.9V domain.
	Px_REFCLK_N	Weak pull low (ex. 10kohm) to ground.
	Px_REFCLK_P	Weak pull low (ex. 10kohm) to ground.
	PCIE_RESETB	Weak pull to GND.
	CLKREQB	Float this pin.
	LANWAKEB	Float this pin.
	ISOLATEB	Weak pull to GND.
	Px_RXD[4:0]	Weak pull to GND.
RGMII/MII/RMII	Px_RXDV	Weak pull to GND.
	Px_RXER	Weak pull to GND.
	Px_RXC	Weak pull to GND.
	Px_TXD[3:0]	TXD are also strapping pins. Please configure them according to section 6.25.
	Px_TXEN	Floating.
	Px_TXC	Floating.
	Px_MDINA	Floating.
FE PHY	Px_MDIPA	Floating.
	Px_MDINB	Floating.
	Px_MDIPB	Floating.
	Px_LED	Floating.
LED	FE_LEDx	Floating when in LED mode. Weak pull to GND when configured as CRS and COL.
	Px_LDOIN	Floating except P0 LDO and P4 LDO.
Regulator Pins	Px_LDOOUT	Floating.
	DISB	Weak pull to high (MAC_VDDIO domain).
Automotive Related Pins	WAKE	Weak pull low or high.
	INH	Floating.
	XO	Floating.
Miscellaneous Interface Pins	RESETB	Weak pull to high (MAC_VDDIO domain).
	RTT_CKDIG	Floating.
	GPIOx	Floating. Some GPIOs are strapping pins. Please configure them according to section 6.25.

Interface	Pin Name	Action
Power controller	PGATE/NGATE/VO09	Floating.
	AVDD33_HVD	Connect to 3.3V power.
	AVDD33_AHV	Connect to 3.3V power.
	GND_HGD	Connect to GND.
SPI master	SPI_CSB	Floating.
	SPI_SCK	Floating.
	SPI_SIO0	Floating.
	SPI_SIO1	Place a 0-ohm resistor to ground at SPI_SIO1 pin if flash-less mode is used. (Remove this 0ohm resistor when the flash is attached).
	SPI_SIO2	Floating.
	SPI_SIO3	Floating.

Note: In the above table the port ID (P_x) is described based on the RTL9072/75AAD. For the RTL9068AAD/ABD, lower the port ID by 4 to apply the un-used pin rule (ex: rule for P10 of the RTL9072/75AAD = P6 of the RTL9068AAD/ABD, P11 of the RTL9072/75AAD = P7 of the RTL9068AAD/ABD).

7.10. Latency of Interfaces

The following table shows latency of interfaces. The latency values are measured by LIFO (Last bit In, First bit Out) method.

Table 37. Latency of Interfaces

Interface	Latency (us)
100BASE-T1 (Non-combo) in, 100BASE-T1 (Non-combo) out. For RTL907XA: Port0, 1, 2, 3, 4, 12, 13 RTL906XA: Port5 ~ 6	6.19
100BASE-T1 (Combo) in, 100BASE-T1 (Combo) out. For RTL907XA: Port6 ~ 7 RTL906XA: Port2 ~ 3	4.22
100BASE-TX in, 100BASE-TX out	4.86
MII in, MII out	1.68
1000BASE-T1 in, 1000BASE-T1 out	6.39
RGMII in, RGMII out	0.74
SGMII (Non-combo) in, SGMII (Non-combo) out. For RTL907XA: Port6 ~ 9 RTL906XA: Port2 ~ 5	1.11
SGMII (Combo) in, SGMII (Combo) out. For RTL907XA: Port10 ~ 11 RTL906XA: Port6 ~ 7	1.03
HSGMII in, HSGMII out	0.81
USXGMII in, USXGMII out	1.60
100BASE-T1 (Non-combo) in, 100BASE-TX out 100BASE-TX in, 100BASE-T1 (Non-combo) out	5.40
RGMII in, SGMII (Non-combo) out SGMII (Non-combo) in, RGMII out	0.95
RGMII in, SGMII (Combo) out SGMII (Combo) in, RGMII out	0.88
1000BASE-T1 in, RGMII out RGMII in, 1000BASE-T1 out	3.56
1000BASE-T1 in, SGMII (Non-combo) out SGMII (Non-combo) in, 1000BASE-T1 out	3.72
1000BASE-T1 in , SGMII (combo) out SGMII (combo) in, 1000BASE-T1 out	3.69

8. General Function Description

8.1. Power Sequence

Three different power domains are required for the RTL9054/RTL9068/RTL907x's normal operation, 3.3V, 0.9V and VBAT/V33. The 0.9V is either sourced by external supplies or internal switching control with external P/NMOS components. The constraints shown below should be complied with for reliable power-on initialization.

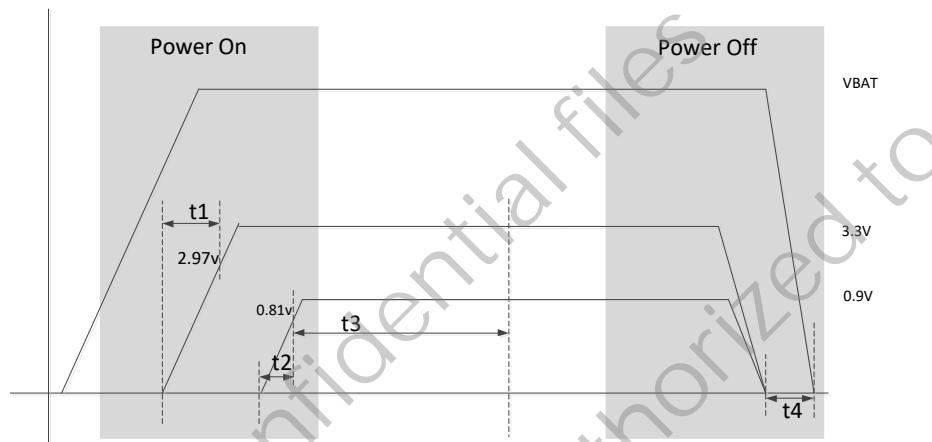


Figure 33. Power Sequence for Supplying 0.9V from External SWR/LDO

Table 38. Power On Sequence Parameter from External SWR/LDO

Symbol	Description	Min	Typ.	Max	Unit
t1	3.3V Rise Time.	0.15	-	10	ms
t2	0.9V Rise Time.	0.15	-	10	ms
t3	Link Up Time.	-	-	100	ms
t4	Power Off Time.	0	-	-	ms

*VBAT/V33 shall be ready before 3.3V and 3.3V shall be ready before 0.9V starts to rise.

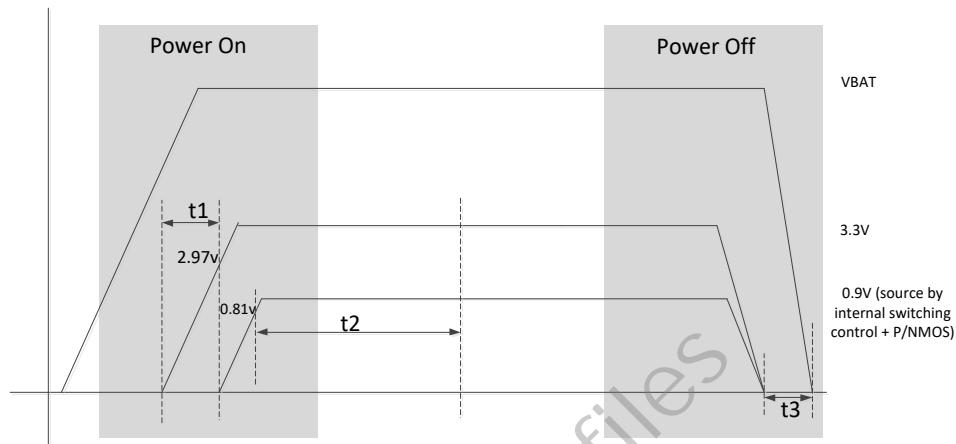


Figure 34. Power Sequence for Internal Switching Control + External P/NMOS

Table 39. Power on Sequence Parameters for Internal Switching Control + External P/NMOS

Symbol	Description	Min	Typ.	Max	Unit
t1	3.3V Rise Time.	0.15	-	10	ms
t2	Link Up Time.	-	-	100	ms
t3	Power Off Time.	0	-	-	ms

*VBAT shall be ready before 3.3V and 0.9V starts to rise when 3.3V is ready.

*Note 1: Please make sure the powering-off order is correct, as if the 3.3V goes lower than 0.9V, it will cause the IC to enter unknown status, which may damage the IC.

*Note 2: The 3.3V can't be lower than 0.9V when doing a power off sequence, so the user needs to maintain the relative relationship between 3.3V and 0.9V.

*Note 3: If VBAT support is not necessary for the user system, please connect VBAT directly to a 3.3V power source.

8.2. Reset Function

8.2.1. Power On Reset

The RTL9054/RTL9068/RTL907x monitors the voltage of both 0.9V and 3.3V power. The RTL9054/RTL9068/RTL907x will initiate a power on reset when either of these is lower than the pre-set threshold (for 3.3V power the threshold is 3.06v; for 0.9V power the threshold is 0.81v). A power on reset will complete the reset initialization procedures below:

- Initialize the TX and RX packet buffer descriptors and the output queue. The TX and RX packet buffer descriptors point to the specific packet buffer in the packet buffer pool. The output queue records the TX packet buffer descriptor for sending the packet out
- Complete the BIST process
- Determine the settings of the strapping pins at the end of the RESETB signal
- Initialize the internal CPU, which also indirectly triggers the following events:
 - Auto load the program from SPI FLASH if the corresponding mode is selected
 - Auto load the register configuration from SPI FLASH if SPI FLASH is enabled and detected

8.2.2. Pin Reset

A Pin reset is triggered by pulling the RESETB pin low. A logic low will always be below 2.0V. The Pin reset forces the RTL9054/RTL9068/RTL907x to reset all the circuits and complete the power on as described in the Power on Reset section above.

The requirements are:

1. Time period between T1 and T2 shall be at least 10ms. If the time is less than 10ms, the reset operation will be invalid.
2. Reset signal rising time between T2 to T3 shall not be more than 5ms. The rising voltage is from 0 to 2.0V.

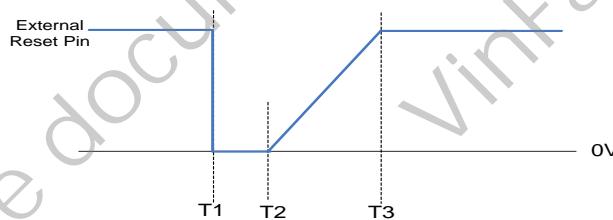


Figure 35. Power-On Sequence

8.2.3. Reset Command via Register

The RTL9054/RTL9068/RTL907x supports a chip reset by calling rtk_sys_chip_reset() to reset itself. A chip reset can achieve similar to a pin reset.

Chip Reset

A chip reset forces the RTL9054/RTL9068/RTL907x to start the initial reset sequence and reset most of the circuits. It will strap pins to give all default values when the 'RESET' signal terminates, and runs the

SRAM BIST (Built-In Self Test) process. The next configuration is auto-loaded from the SPI FLASH (if the SPI FLASH is detected). The reset bit will be self-cleared once set to ‘0’.

8.3. Clock Circuit

The crystal circuit needs a 25MHz crystal reference or oscillator input. When using a crystal, the RTL9054/RTL9068/RTL907x should connect a loading capacitor from each pin to ground.

Table 40. Crystal Requirements

Parameter	Condition	Min	Typ.	Max	Unit
Frequency	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
Frequency Tolerance*Note1	Ta = -40°C ~ 105°C	-100	-	100*Note2	ppm
Equivalent Series Resistance of Crystal	-	-	-	100*Note 3	ohm
Duty Cycle	-	40	-	60	%
RMS Jitter	-	-	-	1	ps
Crystal Output High Level	-	1.4	-	-	V
Crystal Output Low Level	-	-	-	0.4	V

Note 1: Frequency Tolerance includes effects of aging for the years, external crystal capacitors, and PCB layout.

Note 2: If the frequency tolerance for the RGMII interface needs to be considered, the frequency tolerance of crystal shall be +/- 50ppm.

Note 3: The maximum value of ESR depends on the ‘shunt capacitance’ specified by the crystal manufacturer and the two ‘load capacitors’ (20pF recommended as in the latest reference schematic). As a result, the feasible max shunt capacitance is 5pF.

Table 41. Oscillator/External Clock Requirements

Parameter	Condition	Min	Typ.	Max	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance*Note1	Ta = -40°C ~ 105°C	-100	-	100*Note2	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter	-	-	-	1	ps
V _{IH}	-	1.4	-	-	V
V _{IL}	-	-	-	0.4	V
Rise Time (10% ~ 90%)	-	-	-	10	ns
Fall Time (10% ~ 90%)	-	-	-	10	ns
Operating Temperature Range	-	-40	-	105	°C

Note 1: Frequency Tolerance includes effects of aging for the years.

Note 2: If the frequency tolerance for the RGMII interface needs to be considered, the frequency tolerance of crystal shall be +/- 50ppm.

8.4. Lookup Table (LUT)

The lookup table consists of a 4K-entry L2 table, a 256-entry CAM and a 128-entry IP Multicast Group Table.

Received packets are forwarded according to the destination port in the LUT. The RTL9054/RTL9068/RTL907x can retrieve the source MAC to learn from the LUT, and use the destination MAC as an index to find the destination port.

8.4.1. Address Searching & Forwarding

The frames received will be forwarded according to the information learned or written into the Lookup Table (LUT) table. Address processing needs to update the information, including the age field and source port number, and assign the destination port for the frame. When a packet is received, the RTL9054/RTL9068/RTL907x uses the bits of the destination MAC address with a VLAN ID or Filter ID as an index to lookup the 4k-entry lookup table and compares the destination MAC address with the contents of the 256-entry CAM. If the indexed entry in the lookup/CAM table is found, the received packet is forwarded to the corresponding destination port. Otherwise, the RTL9054/RTL9068/RTL907x executes the corresponding operation according to Table 42.

Table 42. ADDRESS_TABLE_LOOKUP_MISS_CONTROL_REGISTER

Reg bit	Name	Description	Mode	Default
n.[9:8]	L2BMISSOP	Layer2 broadcast lookup miss packet operation. 00: Drop 01: To CPU 1x: Flood	RW	0x2
n.[7:6]	L2MMISSOP	Other multicast lookup miss packet operation. 00: Drop 01: To CPU 10: Flood in VLAN 11: Flood to all ports	RW	0x2
n.[1:0]	L2UMISSOP	Layer2 unicast lookup miss packet operation. 00: Drop 01: To CPU 10: Flood in VLAN, ppi.crvlan = 0 11: Flood to all ports, ppi.crvlan = 1	RW	0x2

8.4.2. Hash Algorithm

The RTL9054/RTL9068/RTL907x's hash algorithms are used to resolve the key from the frame's MAC address and VID or FID in order to locate the Lookup Table (LUT) entry and avoid hash collisions. If there are multiple end devices with a similar MAC address, key collisions happen frequently. To solve this problem, the RTL9054/RTL9068/RTL907x provides two hash algorithms such as the following:

$$\text{Index[08]} = \text{KEY08} \oplus \text{KEY17} \oplus \text{KEY26} \oplus \text{KEY35} \oplus \text{KEY44} \oplus \text{KEY53}$$

$$\text{Index[07]} = \text{KEY07} \oplus \text{KEY16} \oplus \text{KEY25} \oplus \text{KEY34} \oplus \text{KEY43} \oplus \text{KEY52}$$

$$\text{Index[06]} = \text{KEY06} \oplus \text{KEY15} \oplus \text{KEY24} \oplus \text{KEY33} \oplus \text{KEY42} \oplus \text{KEY51}$$

$$\text{Index[05]} = \text{KEY05} \oplus \text{KEY14} \oplus \text{KEY23} \oplus \text{KEY32} \oplus \text{KEY41} \oplus \text{KEY50} \oplus \text{KEY59}$$

Index[04] = KEY04⊕KEY13⊕KEY22⊕KEY31⊕KEY40⊕KEY49⊕KEY58
 Index[03] = KEY03⊕KEY12⊕KEY21⊕KEY30⊕KEY39⊕KEY48⊕KEY57
 Index[02] = KEY02⊕KEY11⊕KEY20⊕KEY29⊕KEY38⊕KEY47⊕KEY56
 Index[01] = KEY01⊕KEY10⊕KEY19⊕KEY28⊕KEY37⊕KEY46⊕KEY55
 Index[00] = KEY00⊕KEY09⊕KEY18⊕KEY27⊕KEY36⊕KEY45⊕KEY54

Table 43. Mapping Between Key and <mac address, filter ID> hash0

KEY00	KEY01	KEY02	KEY03	KEY04	KEY05	KEY06	KEY07	KEY08
MAC00	MAC01	MAC02	MAC03	MAC04	MAC05	MAC06	MAC07	MAC08
KEY09	KEY10	KEY11	KEY12	KEY13	KEY14	KEY15	KEY16	KEY17
MAC09	MAC10	MAC11	MAC12	MAC13	MAC14	MAC15	MAC16	MAC17
KEY18	KEY19	KEY20	KEY21	KEY22	KEY23	KEY24	KEY25	KEY26
MAC18	MAC19	MAC20	MAC21	MAC22	MAC23	MAC24	MAC25	MAC26
KEY27	KEY28	KEY29	KEY30	KEY31	KEY32	KEY33	KEY34	KEY35
MAC27	MAC28	MAC29	MAC30	MAC31	MAC32	MAC33	MAC34	MAC35
KEY36	KEY37	KEY38	KEY39	KEY40	KEY41	KEY42	KEY43	KEY44
MAC36	MAC37	MAC38	MAC39	MAC40	MAC41	MAC42	MAC43	MAC44
KEY45	KEY46	KEY47	KEY48	KEY49	KEY50	KEY51	KEY52	KEY53
MAC45	MAC46	MAC47	FID00	FID01	FID02	FID03	FID04	FID05
KEY54	KEY55	KEY56	KEY57	KEY58	KEY59			
FID06	FID07	FID08	FID09	FID10	FID11			

Table 44. Mapping Between Key and <mac address, filter ID> hash0

KEY00	KEY01	KEY02	KEY03	KEY04	KEY05	KEY06	KEY07	KEY08
MAC00	MAC01	MAC02	MAC03	MAC04	MAC05	MAC06	MAC07	MAC08
KEY09	KEY10	KEY11	KEY12	KEY13	KEY14	KEY15	KEY16	KEY17
MAC11	MAC12	MAC13	MAC14	MAC15	MAC16	MAC17	MAC09	MAC10
KEY18	KEY19	KEY20	KEY21	KEY22	KEY23	KEY24	KEY25	KEY26
MAC21	MAC22	MAC23	MAC24	MAC25	MAC26	MAC18	MAC19	MAC20
KEY27	KEY28	KEY29	KEY30	KEY31	KEY32	KEY33	KEY34	KEY35
MAC31	MAC32	MAC33	MAC34	MAC35	MAC27	MAC28	MAC29	MAC30
KEY36	KEY37	KEY38	KEY39	KEY40	KEY41	KEY42	KEY43	KEY44
MAC41	MAC42	MAC43	MAC44	MAC36	MAC37	MAC38	MAC39	MAC40
KEY45	KEY46	KEY47	KEY48	KEY49	KEY50	KEY51	KEY52	KEY53
FID03	FID04	FID05	MAC45	MAC46	MAC47	FID00	FID01	FID02
KEY54	KEY55	KEY56	KEY57	KEY58	KEY59			
FID11	FID06	FID07	FID08	FID09	FID10			

8.4.3. Hash Conflict and Overflow Handler

Each entry is stored in the hash bucket. If there are 8 entries in the same hash bucket, new MAC address entries cannot be learned in the bucket, which is how a collision occurs. To notify the external/internal CPU about the collision, the RTL9054/RTL9068/RTL907x provides a hash conflict interrupt and an overflow interrupt.

(1) Hash Conflict Interrupt

If the 8 spaces in the bucket have been written, no new entries can be learned, which is a hash conflict. When a collision occurs, the hardware looks for the first valid bit field from VALID_BUCKET_IDX0 to VALID_BUCKET_IDX7 and logs the bucket index. In addition, an interrupt signal is sent to notify the internal CPU and/or the external CPU.

(2) Overflow Interrupt

When a hash conflict occurs, new L2 entries will be stored in the BCAM. If the BCAM is full, new entries cannot be stored, which causes an overflow. An interrupt signal is sent to notify the internal CPU and/or the external CPU.

8.4.4. Address Learning

The RTL9054/RTL9068/RTL907x provides a 4K 8-way hash table to store Layer-2 MAC addresses. Address learning is the process of collecting and storing information from the received packets in order to forward frames to the correct port instead of flooding. This table mainly stores SA, VID or FID, the incoming port and age. The SA and VID/FID are used to calculate the entry index to find the incoming port. For example, when a packet enters the switch through port 0, the SA, port 0 and FID/VID will be stored in the first empty entry. Otherwise, the age of the indexed entry will be updated to MAX.

8.4.5. Address Table Aging

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The lookup engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged-out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging timer of the MAC address lookup table can be configured to between 0.01 ~ 1757497 seconds (default value is approximately 360s) as shown in Table 45.

The RTL9054/RTL9068/RTL907x also supports a powerful flushing function for the table that can flush the entire table or only the entries learned on specific ports, or with specific VID or FID.

Table 45. SOURCE_MAC_LEARNING_CONTROL_REGISTER0

Reg bit	Name	Description	Mode	Default
n.[18:0]	AGEUNIT	Aging bits reduce one every AGEUNIT*0.0032768 second. Disable aging when AGEUNIT == 0.	RW	0x6B

8.4.6. MAC Constraint

The RTL9054/RTL9068/RTL907x supports an MAC constraint function that limits the number of learned MAC addresses. The function related parameters are as follows:

- MAC_CRT_CUR: The number of MAC addresses currently learned
- MAC_CRT_MAX: The maximum number that can be learned
- MAC_CRT_ACT: The action that occurred when MAC_CRT_CUR > MAC_CRT_MAX
- MAC_CRT_RESET: Reset MAC_CRT_CUR to 0
- MAC_CRT_SYS_MERG_MASK: Port mask selecting which ports to merge to the function

8.5. Flow Control

8.5.1. IEEE 802.3x Flow Control

The switch supports auto-negotiation and IEEE 802.3x flow control. If a port's receive buffer is over the pause-on threshold, a pause-on frame is sent to the link partner to stop the transmission. When the port's receive buffer drops below the pause-off threshold, it sends a pause-off frame. The pause frame format is shown in Figure 36.

When full duplex flow control is enabled, the RTL9054/RTL9068/RTL907x will only recognize IEEE 802.3x flow control PAUSE ON/OFF frames with DA = 01-80-C2-00-00-01, type = 0x8808, OP-code = 0x01, PAUSE Time = maximum to zero, and with a good CRC.

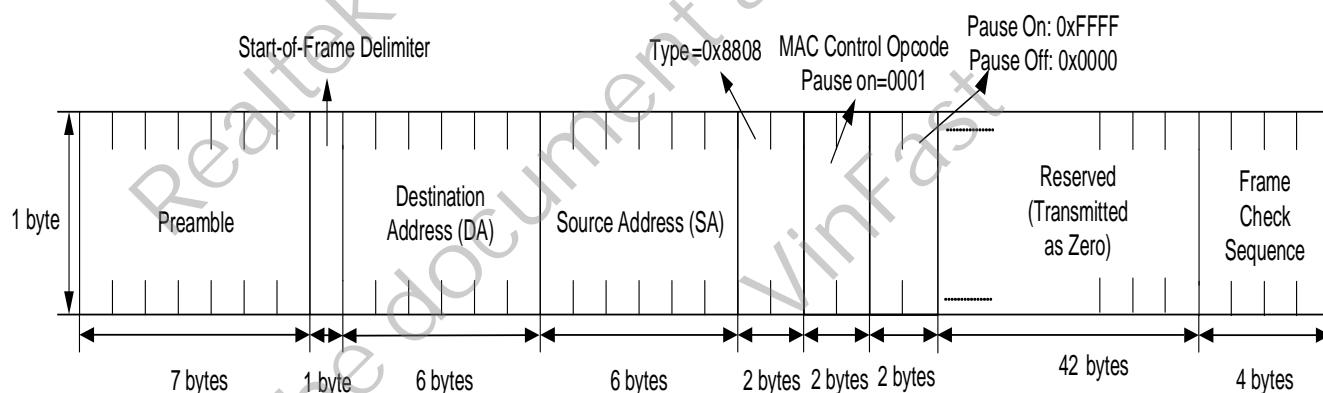


Figure 36. Tx Pause Frame Format

The flow control mechanism of the RTL9054/RTL9068/RTL907x is implemented on the receiving side. It counts the received pages on the receiving side in order to determine which port it should send out Pause On/Off packets.

When the RTL9054/RTL9068/RTL907x flow control is enabled, the initial state is ‘Non-Congest’. The state is monitored continuously. If a pause-on trigger condition occurs, it enters the ‘Congest’ state. When in the ‘Congest’ state, it is also continuously monitored. When a pause-off trigger condition occurs it re-enters the ‘Non-Congest’ state. Figure 37 shows the flow control state machine.

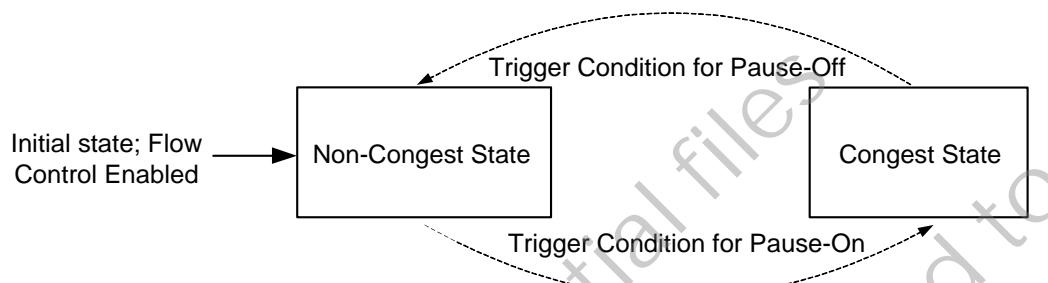


Figure 37. Flow Control State Machine

8.5.1.1 Collision-Based Backpressure (Jam Mode)

If the input buffer is about to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

1. The RTL9054/RTL9068/RTL907x will drive TXEN to high and send a 4-byte Jam signal (pattern is 0x55), then it will drive TXEN to low.
2. When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is 0xFF), then it will drive RXDV to low.
3. The link partner waits for a random back-off time and then re-sends the packet.

8.5.1.2 Carrier-Based Backpressure (Defer Mode)

If the input buffer is about to overflow, this mechanism will send a 0x55 pattern to defer the other station’s transmission. The RTL9054/RTL9068/RTL907x will continuously send the defer signal until the input buffer overflow is resolved.

8.6. Real-M500 Function Description

An ARM base CPU Real-M500 is embedded in the RTL9054/RTL9068/RTL907x to support some advanced network management functions. The Real-M500 can access all of the registers in the RTL9054/RTL9068/RTL907x through the internal bus. With the Network Interface Circuit (NIC) acting as the data path, the Real-M500 connects to the MAC of the switch core and can transmit frames to or receive frames from the Ethernet network. With the internal memory controller, the RTL9054/RTL9068/RTL907x supports internal OC_ROM/SPI FLASH as boot memory.

A 416K-Byte internal OC_ROM is embedded in the RTL9054/RTL9068/RTL907x. The code programmed in the internal ROM implements:

- RSTP, compatible with STP
- IGMP V1&V2&V3 Snooping
- IEEE 802.1X authentication mechanism
- AVB protocol stack: Grandmaster, E2E TC, P2P TC, 802.1AS, 802.1Qav

With these, the RTL9054/RTL9068/RTL907x can completely support RSTP, IGMP V1/V2/V3 snooping function, IEEE 802.1X, and AVB protocol stack without any effort from the external host device.

The external SPI FLASH as boot memory can be used when the program with customized functions are added. When the Real-M500 boots up from the boot_rom, only the 32KB code in the first program space is executed and the internal OC_ROM and external SPI FLASH is also available in this mode. Just note that currently the development based on internal Real-M500 is only for Realtek, and not open to the external user.

The internal Real-M500 and the external host device can communicate with each other. There are some essential parameters of the STP/RSTP, IGMP V1/V2/V3 snooping function, IEEE 802.1X and AVB protocol stack for the host device to instruct the Real-M500. The Real-M500 can also be held, started, and reset by the external host device via register configuration.

8.7. Loop Detection and Prevention (STP/RSTP/MSTP) Functions

This function is used to eliminate potential loops in the network. The RTL9054/RTL9068/RTL907x supports 802.1d/1w/1s (STP/RSTP/MSTP) protocol and contains 15 spanning tree instances. The RSTP function is fully implemented by the internal ARM CPU, which follows the IEEE 802.1D-2004 standard. The MSTP function is implemented with the assistance of an external CPU.

The RTL9054/RTL9068/RTL907x supports four port states for the Spanning Tree Protocol.

Disable State

In this state the port will not receive or transmit any packet, and all frames are discarded. Addresses are not learned by ports in Disable state.

Blocking/Listening State

In this state the port only forwards BPDU packets. Addresses will not be learned and other types of frames will be discarded.

Learning State

In this state all frames will be received, but only BPDU frames will be forwarded. All other frames will be discarded. The addresses can be learned in this state.

Forwarding State

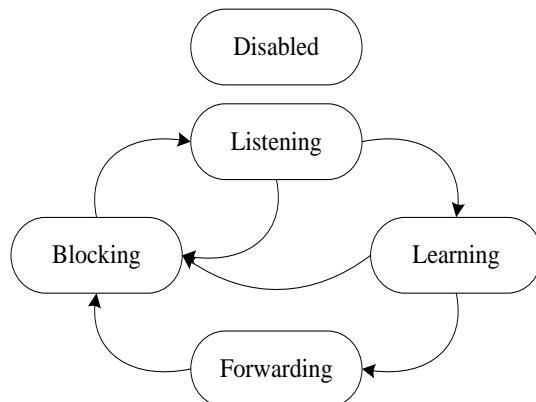
In this state all the frames can be forwarded and all receiving frames' addresses can be learned.

Since the port states of Rapid Spanning Tree Protocol are Discarding, Learning, and Forwarding, the state mapping for Rapid Spanning Tree Protocol is:

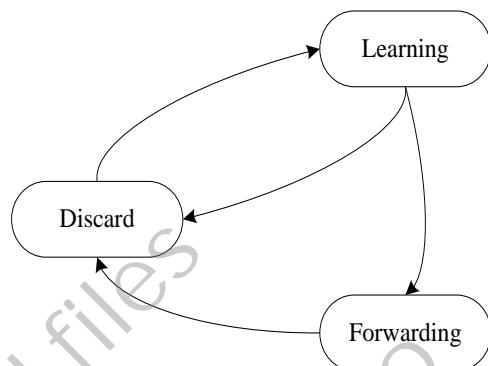
- Discarding → Blocking
- Learning → Learning
- Forwarding → Forwarding

When the BPDU frame is received from the network, it can be trapped to the internal ARM CPU (or external CPU). The internal ARM CPU (or external CPU) will analyze the BPDU and run the state machine of the protocol.

Port States of Spanning Tree



Port States of Rapid Spanning Tree



	Receive BPDUs	Transmit BPDUs	Learn Addresses	Forward Frame
Disable	No	No	No	No
Blocking	Yes	No	No	No
Listening	Yes	Yes	No	No
Learning	Yes	Yes	Yes	No
Forwarding	Yes	Yes	Yes	Yes

	Receive BPDUs	Transmit BPDUs	Learn Addresses	Forward Frame
Discard	Yes	No	No	No
Learning	Yes	Yes	Yes	No
Forwarding	Yes	Yes	Yes	Yes

Figure 38. Port States Relationship for Spanning Tree & Rapid Spanning Tree

RSTP/STP related configuration parameters of the internal ARM CPU are shown below. These parameters can be modified via flash or the management interface (two-wire serial, MDC/MDIO, and SPI). They can be dynamically updated and the internal ARM CPU can detect the changes.

System Parameters:

- Enable/Disable
- STP Type
- Bridge Priority
- Max Age Time
- Hello Time
- Forward Delay Time

Port Parameters:

- Port Priority
- Port Path Cost
- Port Auto Edge Attribution
- Port Admin Edge Attribution
- Port P2P Attribution
- Migration Check Bit

8.8. IGMP/MLD Snooping Function

The RTL9054/RTL9068/RTL907x supports IGMP v1/v2/v3 snooping and MLD v1 snooping.

When the IGMP/MLD Snooping functions of the internal Real-M500 are enabled, the RTL9054/RTL9068/RTL907x monitors all received traffic for IGMP/MLD packets. The IGMP/MLD packets will be trapped to the internal Real-M500. The forwarding entries for IP multicast in the Lookup Table (LUT) and 128-entry group table will be created, updated, or deleted by the internal Real-M500 according to the information in these packets. The IP multicast packet will be forwarded according to the forwarding entries rather than simply flooded.

The IGMP/MLD Snooping functions can also be implemented by the external CPU. In that case, the RTL9054/RTL9068/RTL907x will trap the IGMP/MLD packets to the external CPU and the external CPU will maintain the forwarding table according to the information in the IGMP/MLD packets.

8.9. Port-based IEEE802.1X Authentication Function

The RTL9054/RTL9068/RTL907x supports three different types of IEEE 802.1X authentication as below:

- EAP-MD5
- EAP-TLS
- EAP-PEAP

In the RTL9054/RTL9068/RTL907x, IEEE 802.1X is completely implemented via the internal Real-M500, and after IEEE 802.1X port authentication has been completed, hardware will determine which packets should be dropped/forwarded.

When a supplicant connects to the RTL9054/RTL9068/RTL907x, the RTL9054/RTL9068/RTL907x will ask the supplicant for authentication. The RTL9054/RTL9068/RTL907x will transmit the information sent by the host to the authentication server for authenticating. Port-based Access Control means any physical port can be authorized or unauthorized. When a physical port is unauthorized, the ingress, or both the ingress and egress (determined by register) traffic on this port will be denied.

When IEEE 802.1X is enabled, the forwarding path can be classified into the controlled path and the uncontrolled path. All traffic related to IEEE 802.1X protocol packets will be trapped to the Real-M500. The Real-M500 will forward those packets between supplicant and authentication server; and this path we call the uncontrolled path.

After IEEE 802.1X has completed all protocol handshaking in the uncontrolled path, the Real-M500 will receive an authentication result. This result will be used to determine the forwarding rule. The following illustrates this authentication concept between Supplicant and Authentication Server.

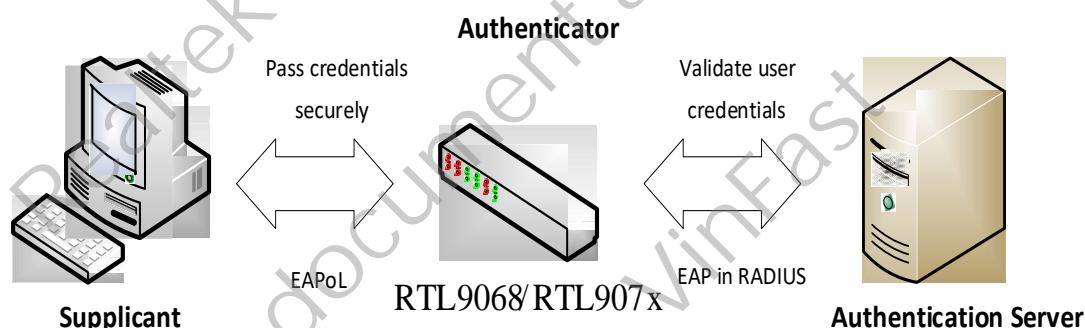


Figure 39. IEEE802.1X Architecture

IEEE 802.1X functions can also be implemented by the external CPU. In that case, the RTL9054/RTL9068/RTL907x will trap IEEE 802.1X packets to the external CPU, and the external CPU will implement the forwarding rule according to the information in the authentication result.

We also provide three different methods to find the authentication server:

- Send an ARP request to all RTL9068/RTL907x's ports
- Only send an ARP request to the radius server port
- Only send an ARP request to IEEE 802.1X's authentication port

8.10. ACL Function

There are 512 ACL entries that enable strong and flexible traffic control ability for the RTL9054/RTL9068/RTL907x. When the ACL function is enabled, information in received packets will be extracted to compare with the template of valid ACL entries. The 192-bit template supports multiple compare keys, such as DMAC and SMAC address, Layer-2/Layer-3/Layer-4 protocol type, Inner/Outer VLAN Tag, DIP and SIP address, Group IP address, TCP/UDP port, source physical port, packet length, and even specific packet payload, allowing a powerful traffic identification function. If the filter field in the packet header is very special, we still design a flexible “ANY OFFSET” to support this requirement. When using “User Define Offset (UDF)”, it only configures the start address from L2/L3/L4 and offsets values to reach any field in the incoming packets.

We also support “RANGE CHECK” and “GROUP MEMBER CHECK” in case a lot of rules are similar. For “RANGE CHECK”, upper bound and lower bound are configured to cover a range of IP/PORT/VLAN_ID. For “GROUP MEMBER CHECK”, discontinuous IP/PORT/VLAN_ID can be configured.

The action specified by the matched entry will go into effect on the received packet. The available actions are listed below:

- Redirect packets to a single port or multiple ports
- Drop packets, trap packets to CPU, copy packets to CPU
- Permit Packet forwarding
- Modify format and fields of outer VLAN tag and inner VLAN tag
- Flow-based mirroring
- DSCP (IPv4 or IPv6) remarking
- Change IP ToS field and change CoS queue based on modification of 802.1p priority field
- VLAN priority and DEI remarking
- Flow-based policing, flow-based statistics, flow number assignment
- Action withdraw
- Bypass rate limit
- Rule hit interrupt

8.10.1. ACL General Description

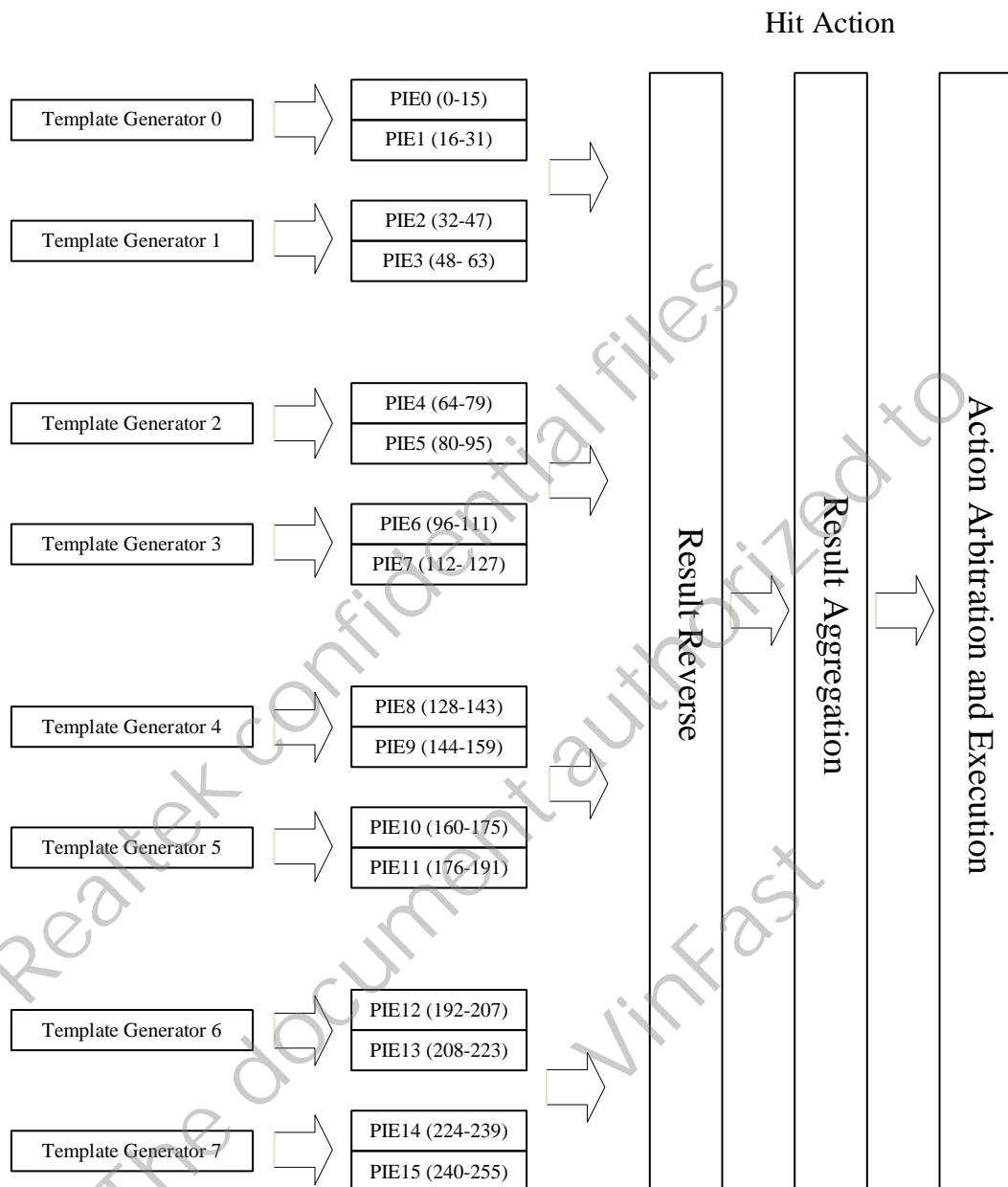
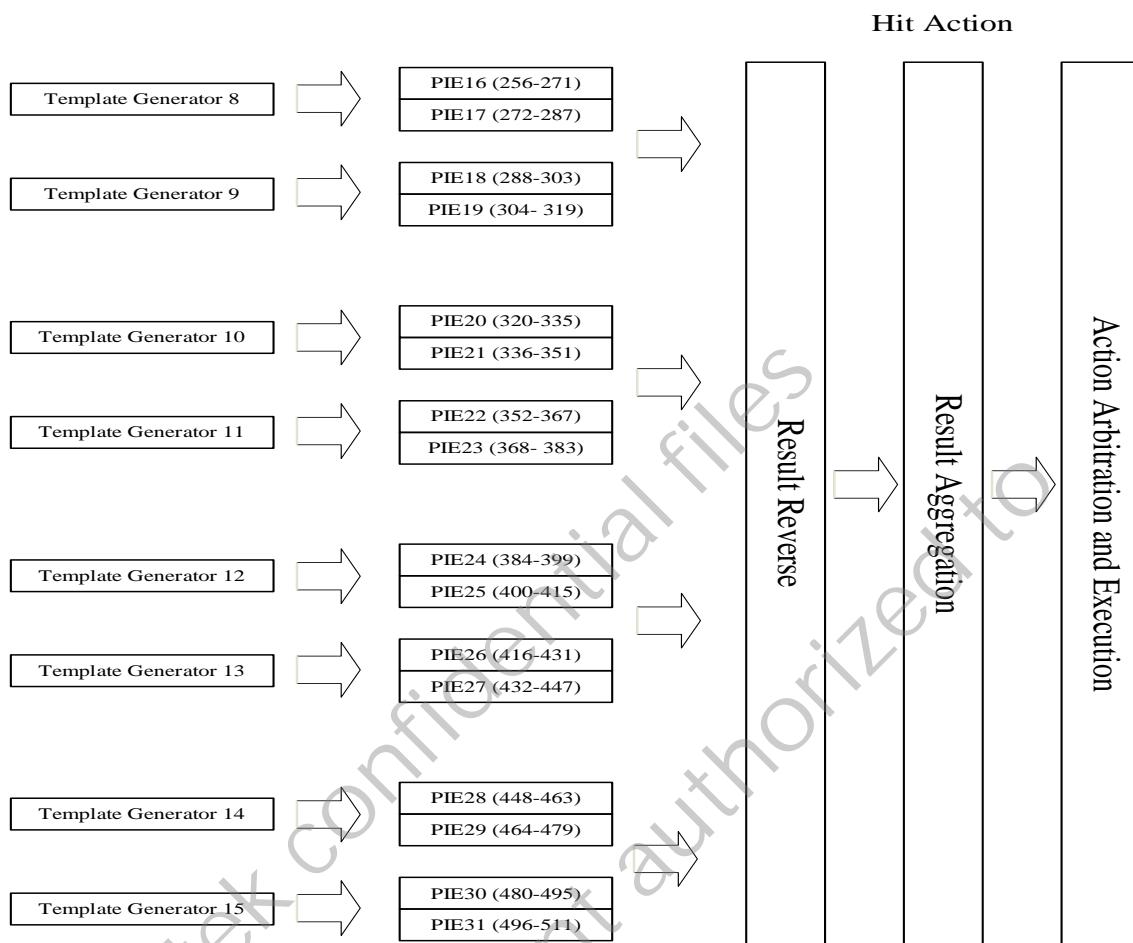


Figure 40. ACL Architecture (1/2)


Figure 41. ACL Architecture (2/2)

This is our ACL architecture and the total hardware block can be divided into five-process areas. When a packet receives by port#, all packets will be processed in the same sequence as the above hardware block.

Table 46. Summary of ACL Resource

Total Number of Template Generators	16
Number of files in one Template Generator	12
Number of Packet Inspection Engines in one Template Generator	2
Total Number of Packet Inspection Engines	$16 \times 2 = 32$
Number of TCAM Entries in one Packet Inspection Engine	16
Number of files in one Packet Inspection Engine	12
Number of Bytes in one Field	2
Total Filter Entry	$32 \times 16 = 512$

8.10.2. Template Generator

Template Generator is the first ACL packet process stage (see Figure 40 and Figure 41) and it was designed with flexible user requirements. The user can define which combination of packet fields need to be filtered. In the RTL9054/RTL9068/RTL907x, there are sixteen Template Generators and each Template Generator includes twelve 2byte fields.

Every Template Generator field can be configured by the specific content of an Ethernet packet header. When a packet enters into a switch, the internal RX parser will extract packet related fields according to the key type configuration of each field of Template Generator. 32 ACL entries is one block which corresponds to one TG, and these 32 ACL entries use the same key type under TG configuration. The purpose of partitioning different ACL entries into different blocks is to provide the user with a different combination of key types.

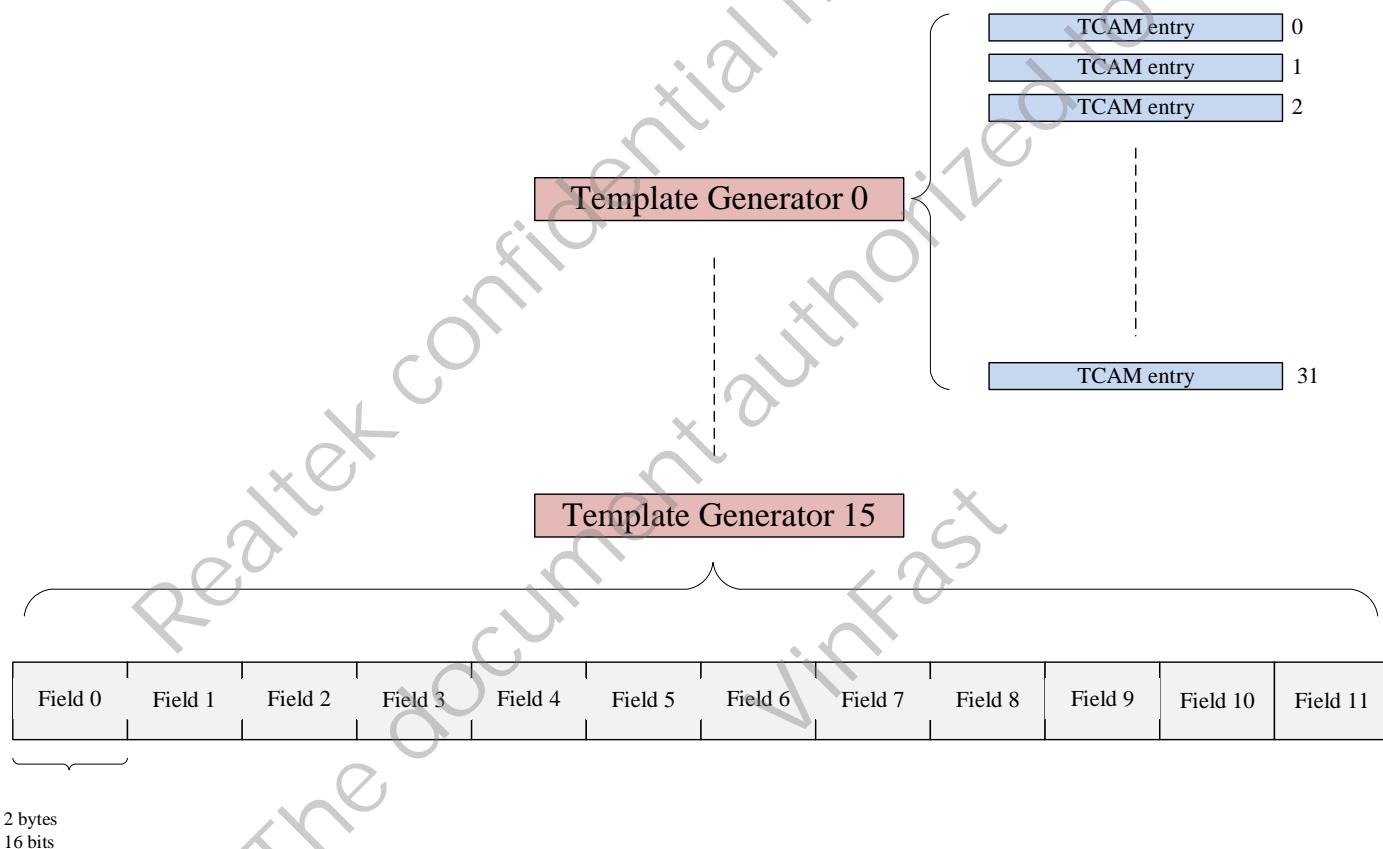


Figure 42. Template Format

8.10.3. Packet Inspection Engine

There are 32 PIEs (Packet Inspection Engines) in the RTL9054/RTL9068/RTL907x, and each PIE includes 16 ACL entries. Each entry format (see Figure 44) and PIE (0 ~ 31) priority can be set individually to fit user requirements. Every PIE can output a hit result and can have a maximum of 32 hit results at any one time. Multiple action arbitration will be introduced in 2.8.

PIE 0/1 belongs to Template Generator 0 (TG 0) and PIE2/3 belongs to Template Generator 1 (TG 1) and so on. All Template Generators have the same hardware block model as in 8.10.2. If the content of the TG (which is set in the same field position as TG) matches one of the contents of the ACL rules in the PIE, it will output a “Hit” event to the next stage. If not, it will output a “miss” event.

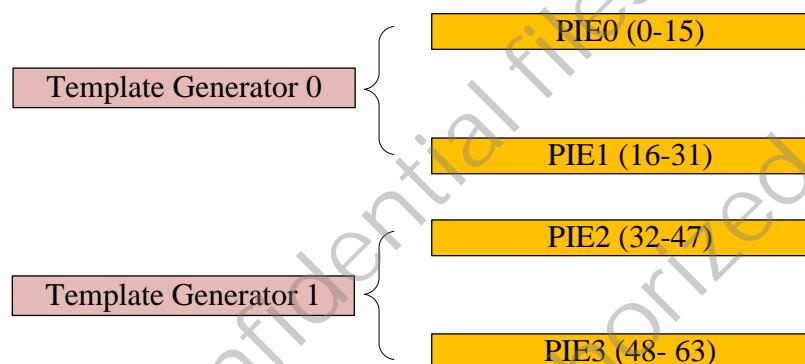


Figure 43. Mapping rule of Template and Packet Inspection Engine

The RTL9054/RTL9068/RTL907x PIE block includes 16 ACL entries which index from $0+16*n \sim 15+16*n$ for $PIEn$ ($n = 0 \sim 15$). The ACL entry has a similar format to TG. The small index number has higher priority within the same PIE. A different PIE that can configure priority values is used for multiple PIEs hit with the same action type. For Example, if PIE 0 and PIE 1 both output a hit event and perform the redirect action, the PIE priority can help to judge which redirect action can be performed.

One ACL rule has a total of 385 bits (192 Data + 192 Mask + 1 Valid). The entire Data area in the ACL entry will be compared by TG, except for the bit value ‘0’ of the Care area (‘1’ = care, ‘2’ = don’t care) corresponding to the Data area.

A packet received by the RTL9054/RTL9068/RTL907x can be configured by 12 conditions (12 fields) at the same time, and these conditions will be considered in operation with each other (e.g., Match result = MAC address & IP address & TCP port).

If all the ACL rules match TG, but the valid bit of the ACL entry is ‘0’, the result will still output a “mismatch”.

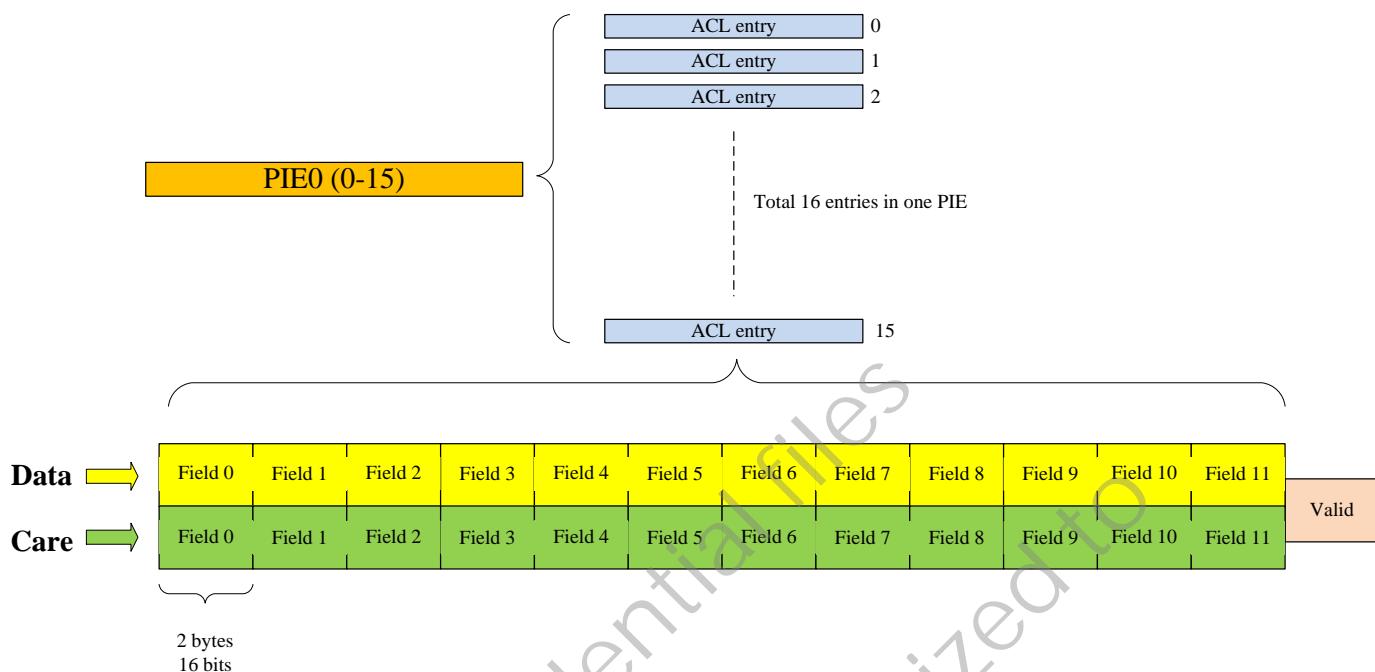


Figure 44. Packet Inspection Engine

8.10.4. Result Reverse

The PIE output result will be reversed. The output results “match” and “mismatch” will be exchanged.

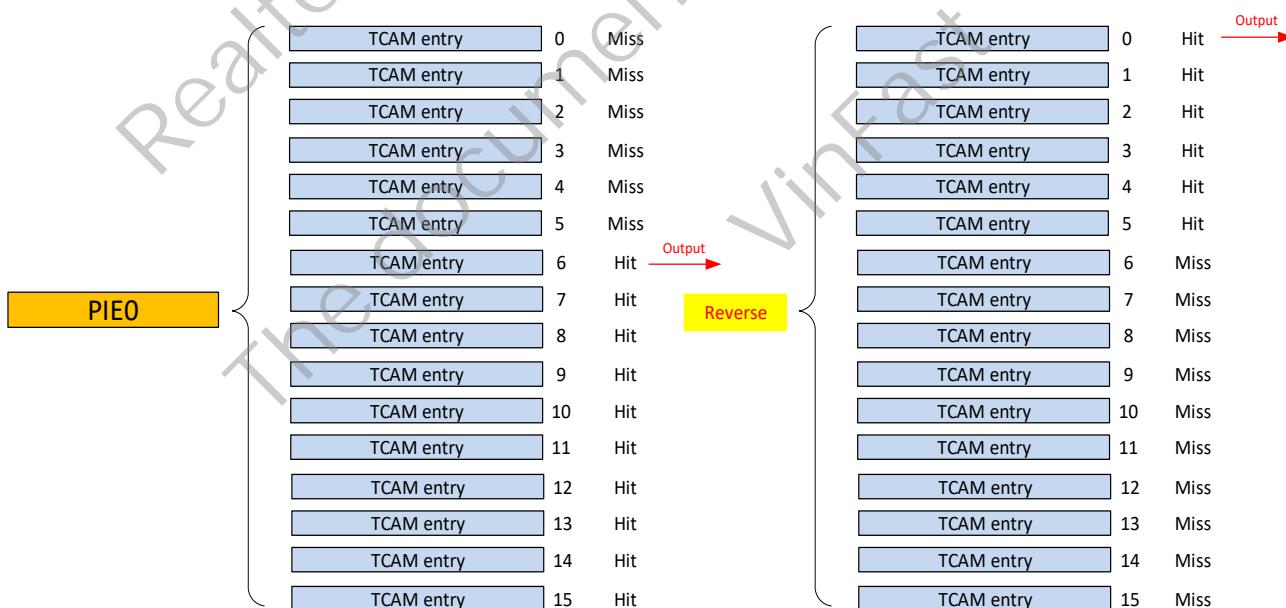


Figure 45. Example of Result Reverse

8.10.5. Result Aggregation

If you need more than 12 conditions to achieve incoming packet filtering at one time, 2 ACL entries can be merged. For example, PIE0 can be combined with PIE 2, PIE1 can be combined with PIE 3, PIE13 can be combined with PIE 15 and so on.

- Two Template Generators can be combined into one Template Generator with more entries.
- When two TGs are merged, the first PIE of TG0 will connect to the first PIE of TG1, and the second PIE of TG0 will connect to the second PIE.
- The action will use the PIE 0 configuration as the result of the combination of TG0 and TG1.
- When merging two TGs, the field is doubled, but the entry will be decreased by 32. If all TGs are merged, the total number of entries becomes 256 ($512 - 32^*8$).

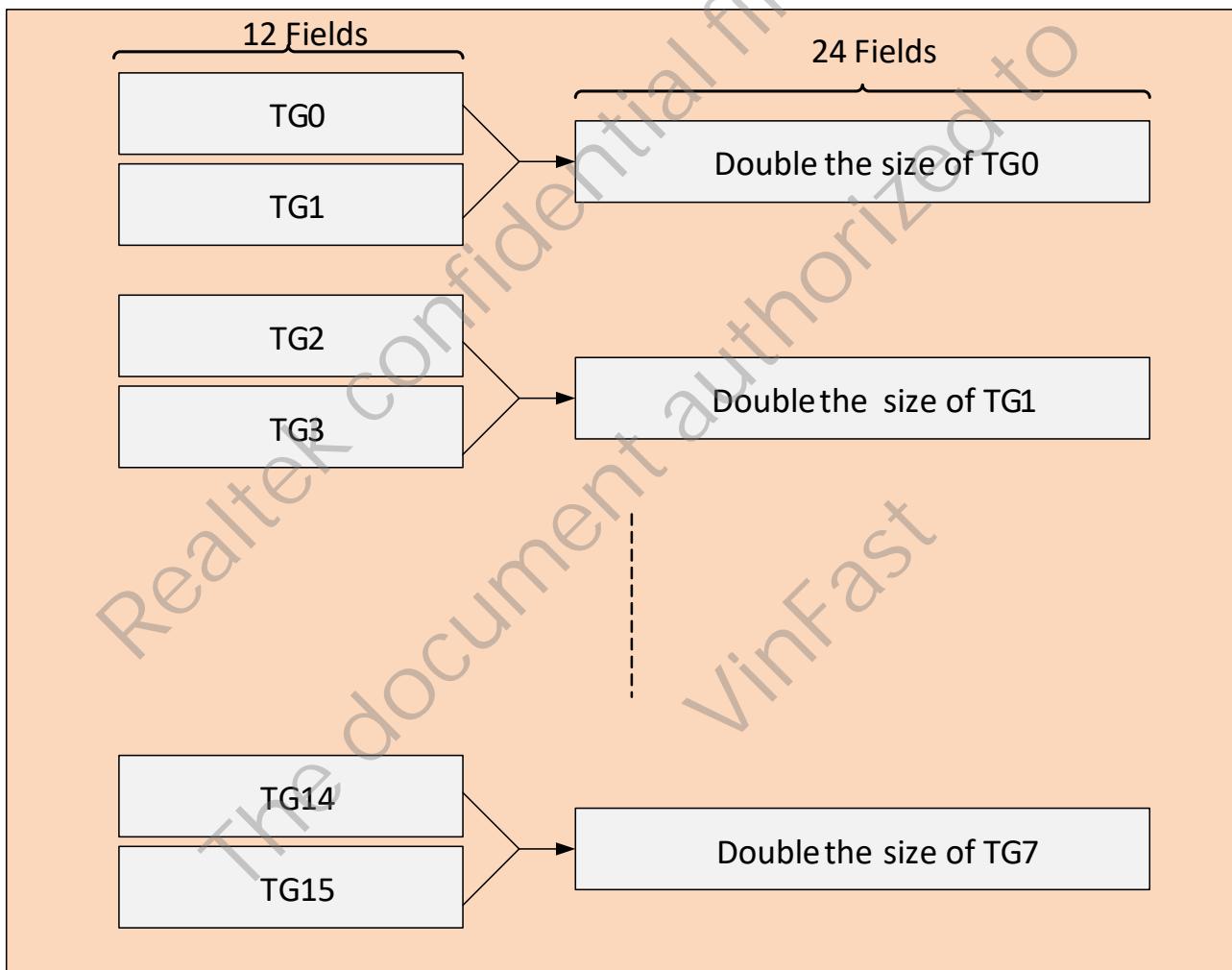


Figure 46. Template Generator Combination

8.10.6. User Define Field (UDF)

Let the user filter any 2byte field within the packet by specifying the base and offset values. There are 32 sets of Offset configurations that can be applied to template generators.

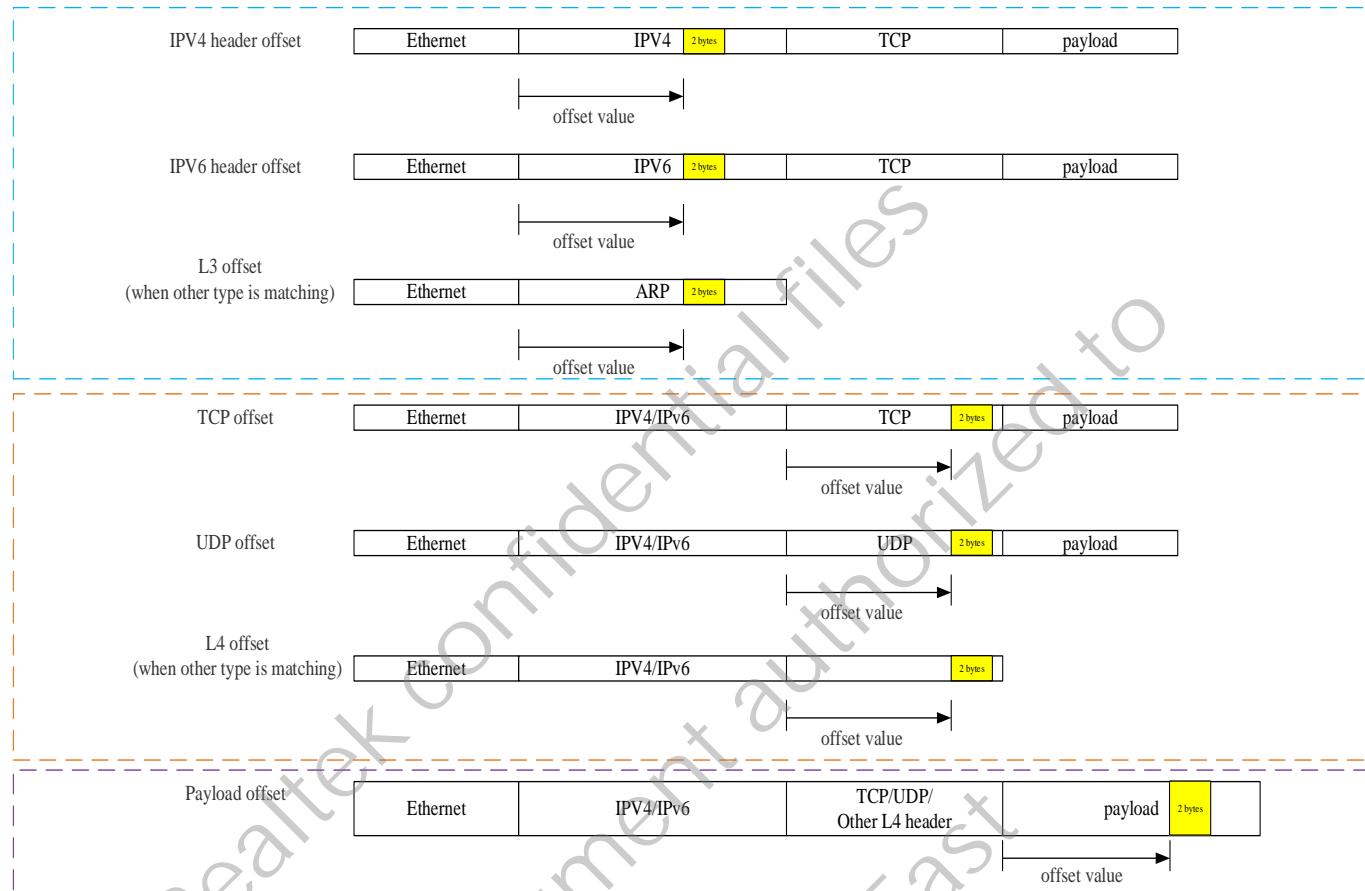


Figure 47. All Supported UDF Types

Table 47. Offset_Type Filed List

Header Type	Filter Range	Number
IPv4	Start of IPv4 header ~ End of IPv4 header	0
IPv6	Start of IPv6 header ~ End of IPv6 header	1
L3(others)	Start of L3 header (but includes EtherType) ~ Start of L3 header + 2048	2
TCP	Start of TCP header ~ End of TCP header	3
UDP	Start of UDP header ~ End of UDP header	4
L4 (others)	Start of L4 header ~ Start of L4 header + 2048	5
Payload	Start of Payload ~ Start of Payload + 2048	6

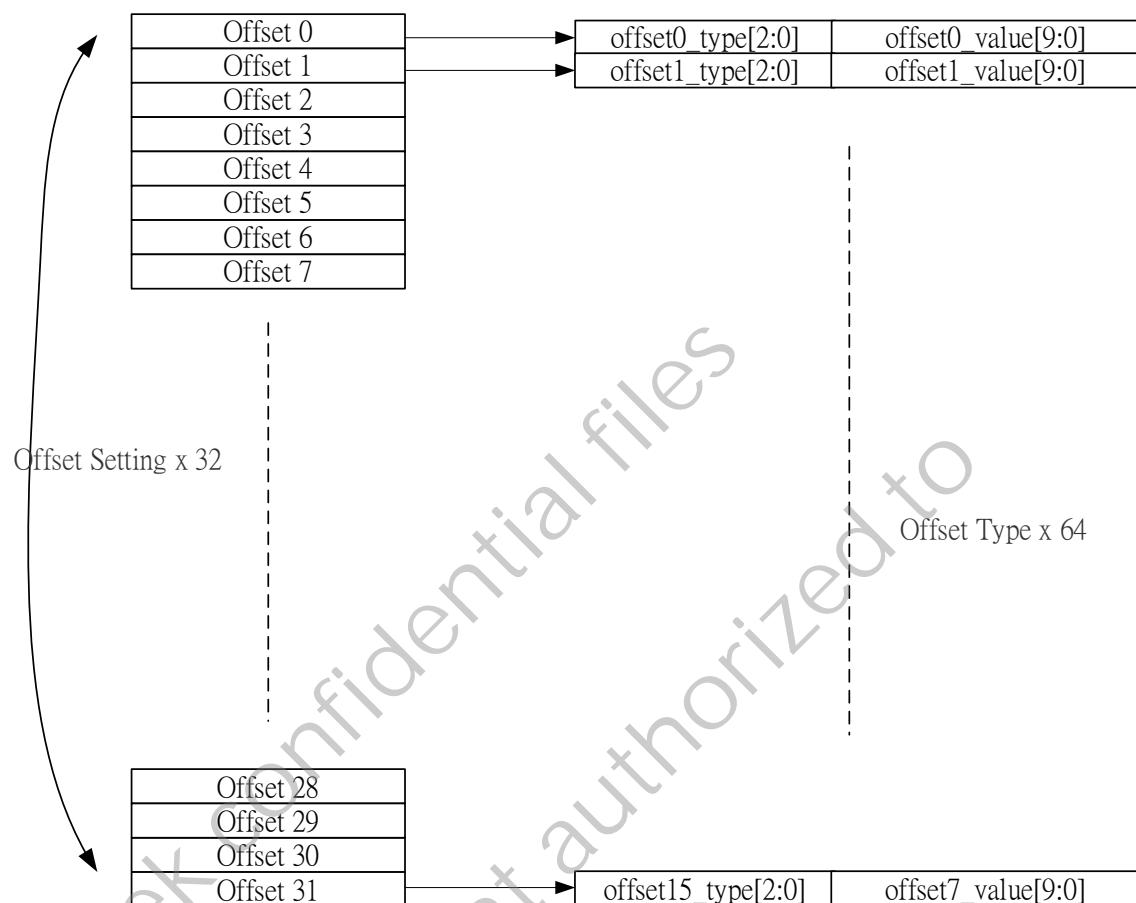


Figure 48. Allocation of Offset and Register Setting

8.10.7. Range Check

One field inside the TCAM can contain a range of continuous values that reduces the number of entries used.

- IPv4 (source/destination IP): 8 sets
- Layer 4 Port (source/destination/TCP/UDP Ports): 4 sets
- VLAN ID (inner/outer VID): 8 sets
- Packet length: 4 sets



Set 0:
 Upper Address: 192.168.1.1
 Lower Address: 192.168.1.255
 All IPv4 packets between upper and lower will be received, such as 192.168.1.1 ~ 192.168.1.255

Figure 49. IPv4 Range Check Example

8.10.8. Group Member Check

One field inside the TCAM can contain several discontinuous values that reduces the number of entries used.

- IPv4 (source/destination IP): 16 sets
- Layer 4 Port (source/destination/TCP/UDP Port): 16 sets
- VLAN ID (inner/outer VID): 16 sets
- Physical Source Port: 4 sets

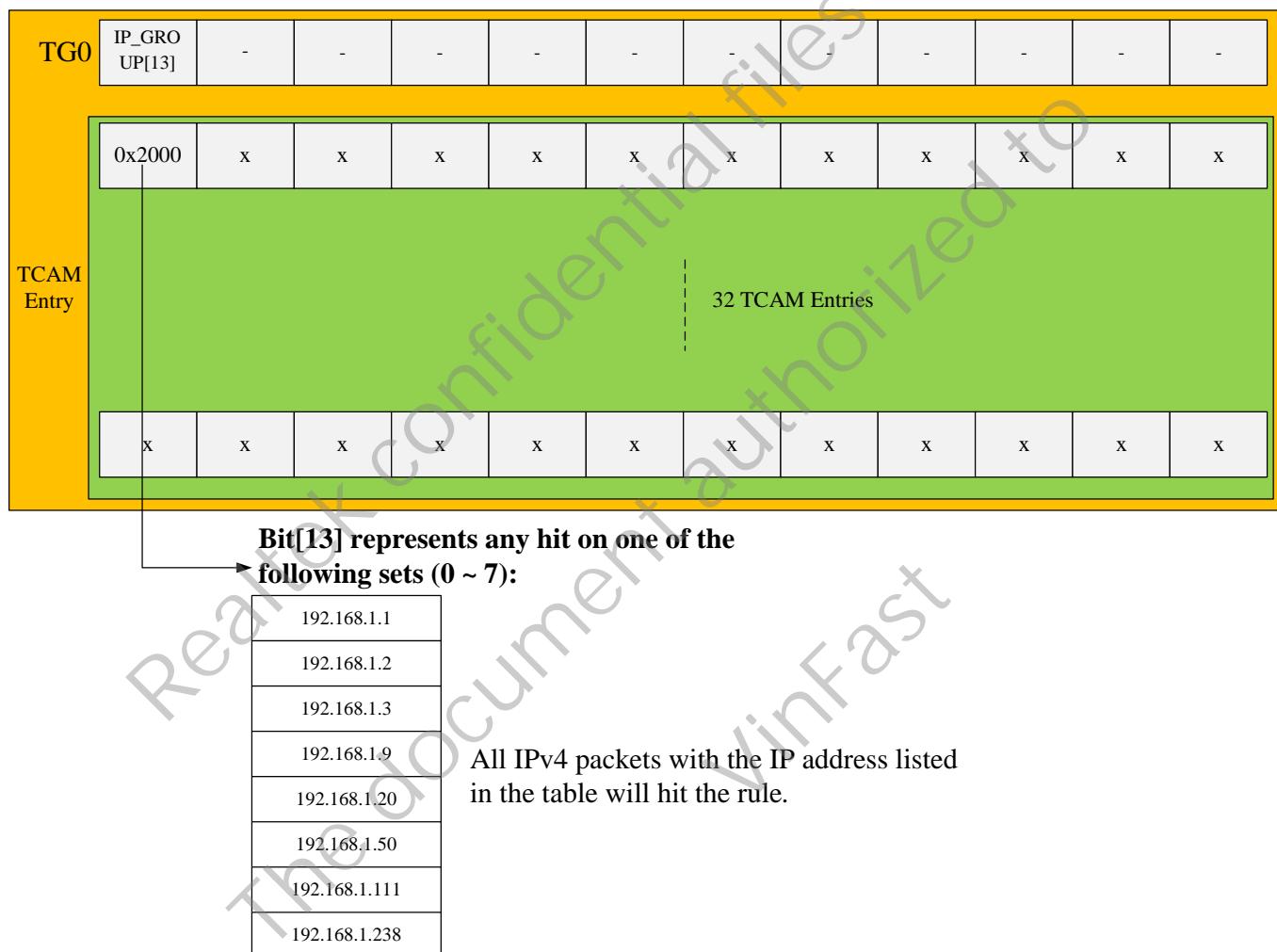


Figure 50. IPv4 Group Member Example

8.10.9. Action Arbitration

The RTL9054/RTL9068/RTL907x supports multiple actions and each PIE entry has an action table as seen in Table 48. You can select any bits from the Action Selection Field to complete your need, however only a maximum of 3 actions which require an “Action Information Field” (AFI) can be supported at the same time.

Most parts of these actions need extra information to be fully functional and this information we call “Action Information Field” (AFI).

When an ACL entry has matched and its output is a “drop action”, other entries that have matched at the same time, but use a different action, will also output a “drop action” unless a “withdraw drop” action be selected from other actions. This is the result of a priority that is set as: “withdraw drop” > Drop >Trap (redirect with opcode = 1) > other actions.

Due to action entries having limitations, information being provided on every action simultaneously is limited. As in Figure 52, each action information field contains a total of 96-bits and up to 3 different types of action entries. Up to three actions which need AIF are selected. Software shall avoid configuring more than three actions that need AIF at the same time.

FNO	DROPI	DROP0	CP2CPU	MIRROR 0	MIRROR 1	OTAG	ITAG	PRI RMK	REDIR	DSCP	PRIO	BYRATE LMT	UC	MC
-----	-------	-------	--------	-------------	-------------	------	------	------------	-------	------	------	---------------	----	----

Figure 51. Action Selector Format (15-bits)



Figure 52. Action Information Fields Format (96-bits)

Every PIE block can be given a priority level. The level of priority will impact the corresponding action entry. In general, only the highest priority will be selected to execute when multiple hit actions are of the same action type.

Some actions are automatically given higher priority. For example, Drop Priority is higher than other action types. If a rule is configured with a drop action and no other rule is set to withdraw the drop, the packet will be dropped regardless of what other rules state.

For any similar type of action, it only follows the information provided by one of the action items and ignores the other actions. However, different types of action information may be taken from different action items. In most cases, the action information in the action Entry with a higher PIE block priority will be used first. Most action types have a corresponding withdraw function to cancel the action of that type of action. The withdrawal priority will be higher than other action types. In other words, if the type of action is Output Withdraw, the same type of other action entry will not be executed.

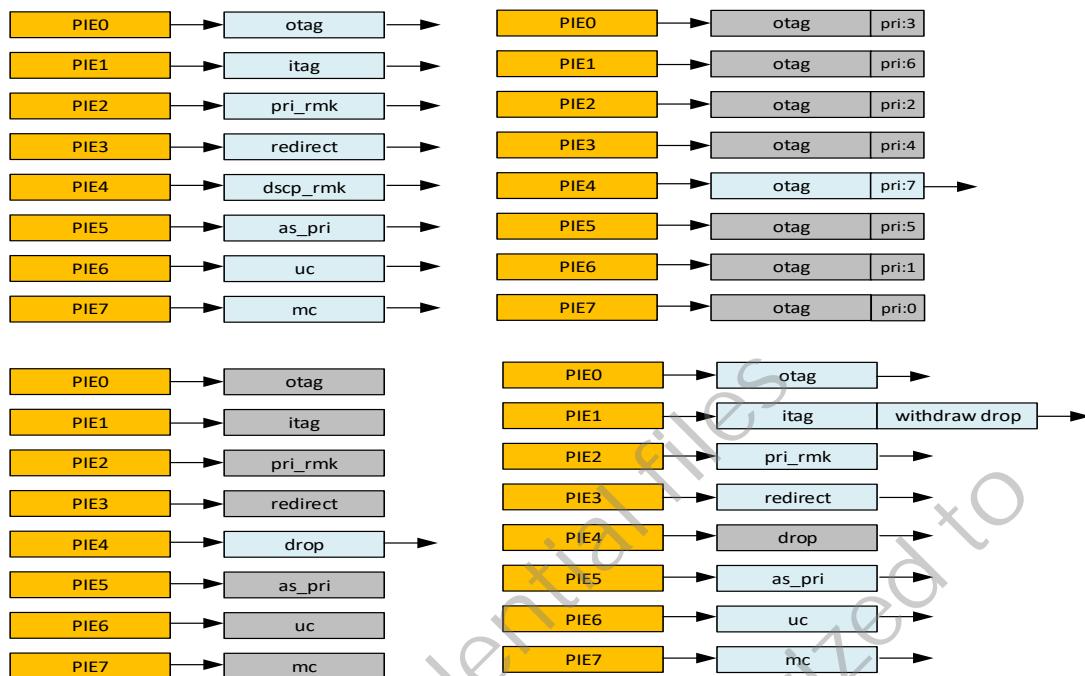


Figure 53. Example Action Arbitration

- If the action is the same in different PIE output, then use the PIE priority to choose which action of PIE can be performed.
- Any action has a withdraw bit to cancel the same action from other PIE output.
- The final Switch forwarding rule is drop > trap > normal forward.

Table 48. ACL Action Table

Bit Allocation	Parameter	Description
W0[31]	Action Selector	flow Ingress Bandwidth Slow Rate.
W0[30:29]		drop 00: Permit 01: Drop 10: Withdraw drop 11: Reserved
W0[28]		copy2cpu Copy Packet to CPU.
W0[27]		mirror1 Mirror1 Packet.
W0[26]		mirror0 Mirror0 Packet.
W0[25]		otag Outer tag vid.
W0[24]		itag Inner tag vid.
W0[23]		pri_rmk 802.1p Priority Remark.
W0[22]		redirect Redirect Packet.
W0[21]		dscp DSCP Remark.
W0[20]		pri Packet pri.
W0[19]		byratelmt Bypass Rate Limit.
W1[31:0]	AIF1	Action Information Fields 1.
W2[31:0]	AIF2	Action Information Fields 2.
W3[31:0]	AIF3	Action Information Fields 3.

8.11. Routing Function

Routing is the process of forwarding packets hop by hop on Layer 3. It primarily includes finding an outgoing interface, and modifying the packets' SMAC, DMAC, VID (if provided), TTL and L3 header checksum (for IPv4) and forwarding.

There are global options determining whether IPv4 unicast, IPv6 unicast, IPv4 multicast and IPv6 multicast packets are routed individually or not. Each ingress L3 interface also provides similar options.

IPv4/IPv6 Routing Capability:

- 64 - Different Interface and each entry can filter DPORt/SPORt/VID to build the firewall for its routing function
- 4K - Host routing table for IPv6
- 256 - Network routing table (subnet) for IPv6
- 4K - Host/Router SA learning (It is the internal L2 table, which provides more efficiency than the NDP/ARP cache)
- 64 - Multicast collision table
- Supports Host NDP/ARP address resolution
- Modifies DA/SA/VID in Unicast and SA/VID in Multicast
- Hop Limit check/decrement
- Checksum recalculated (IPv4)
- MTU check
- uRPF check

Host Routing

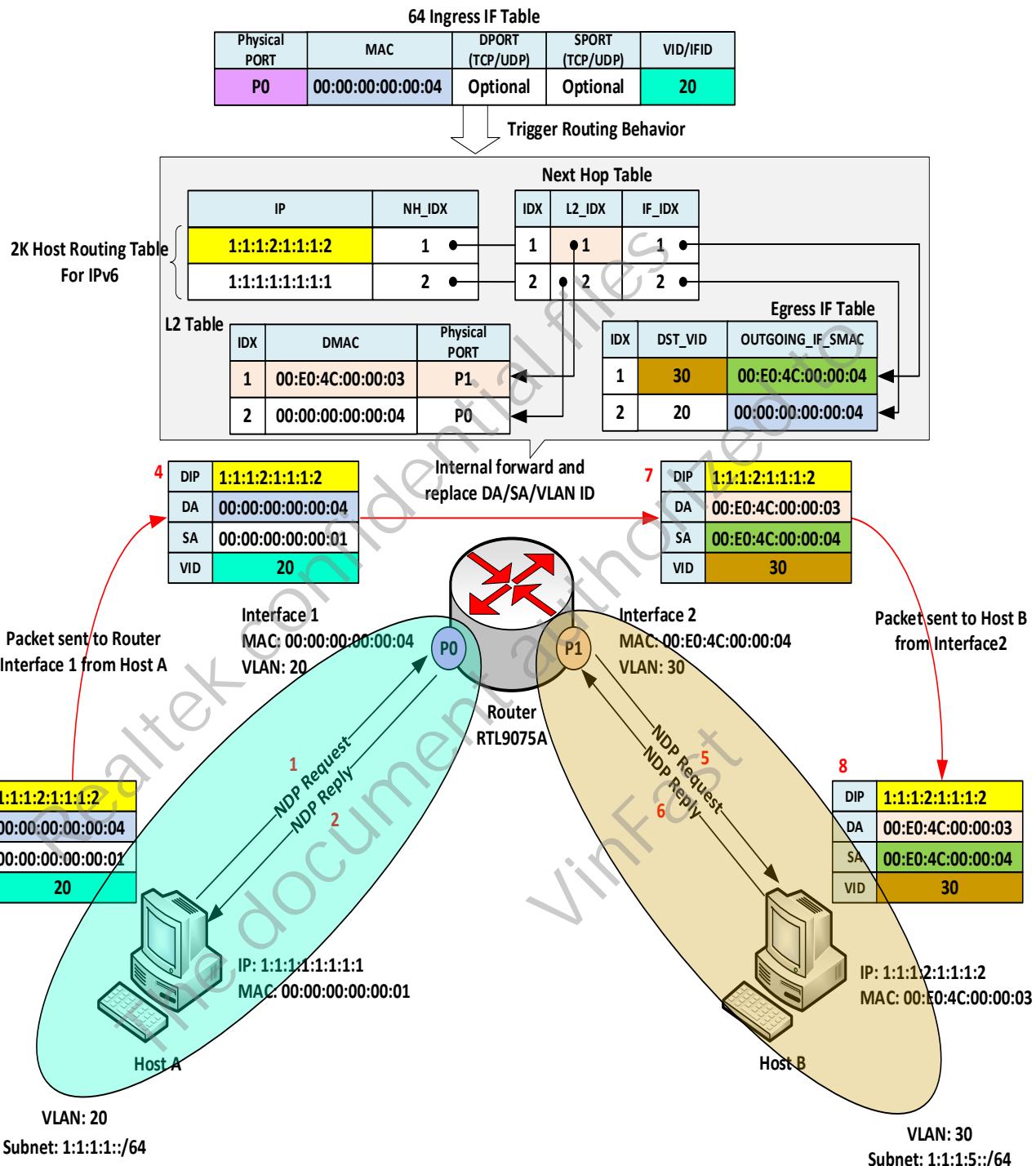


Figure 54. Host Routing Behavior

The following illustrates the host's routing behavior:

1. Host A uses the IP address of Interface 1 and sends an NDP request to the RTL9054/RTL9068/RTL907x.
2. The RTL9054/RTL9068/RTL907x (based on the available interface table) receives this packet and uses an NDP reply telling Host A the IP address of Interface 1.
3. Host A uses this MAC address as the destination address which is received in step2, and then sends the packet to the RTL9054/RTL9068/RTL907x.
4. The RTL9054/RTL9068/RTL907x checks whether the incoming packet from Host A is consistent with the Ingress IF Table or not, and triggers the routing flow.
5. The RTL9054/RTL9068/RTL907x uses the DIP in the IP header to look up the hit entry of the host's routing table. After a successful lookup, the three important pieces of information (DA, SA, VLAN ID) can be obtained from the hit entry. In this entry, the RTL9054/RTL9068/RTL907x will already know the packet egress interface's destination VLAN ID (DST_VID), MAC address (OUTGOING_IF_SMAC) and physical destination port. The RTL9054/RTL9068/RTL907x shall use the DIP of this packet to send an NDP/ARP request via the corresponding physical port.

Note: In a static routing environment, the user needs to configure the DIP and outgoing interface. Every interface includes the MAC address/VLAN ID/physical port.

6. Host B will provide its MAC address after receiving the NDP/ARP address resolution request packet. When the RTL9054/RTL9068/RTL907x receives this packet, SA learning will also be carried out (Host B MAC address is now recorded in the RTL9054/RTL9068/RTL907x's L2 table).
7. As we now have Host B's MAC address in the L2 table, the NDP/ARP cache will be unnecessary. What the RTL9054/RTL9068/RTL907x still needs is to indicate where the entry in the L2 table is, and link it to the corresponding hit entry of the host's routing table. The RTL9054/RTL9068/RTL907x shall generate a new packet which contains a new SA and VLAN ID from step 5, and a new DA from step 7.
8. The packet can now be sent to the correct destination. All packets with the same DIP (after the above routing procedures) are forwarded according to the host's routing table. Wire speed can be reached by a complete host routing table entry.

Network Routing:

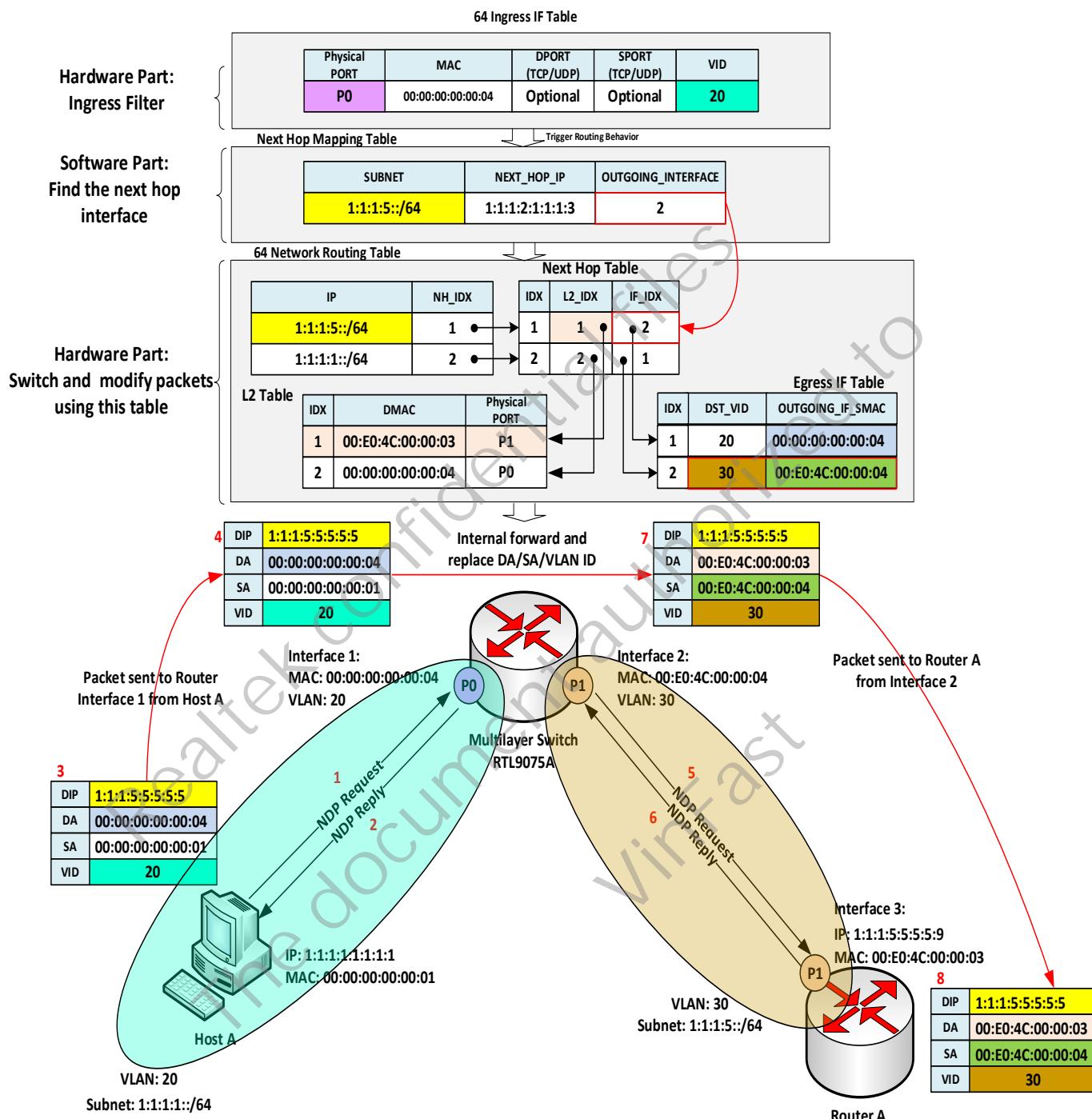


Figure 55. Network Routing Behavior

The network route behavior is similar to Host Routing, but we can take advantage of “TCAM don’t care” to represent the subnet group.

The following illustrates the network routing behavior:

1. Host A uses the IP address of Interface 1 and sends an NDP request to the RTL9054/RTL9068/RTL907x.
2. The RTL9054/RTL9068/RTL907x receives this packet and uses an NDP reply providing Host A with the MAC’s interface address.
3. Host A uses the received MAC address as the destination address from step2, and sends the packet to the RTL9054/RTL9068/RTL907x.
4. The RTL9054/RTL9068/RTL907x checks whether the incoming packet from Host A is consistent with the Ingress IF Table or not and triggers a routing flow. The RTL9054/RTL9068/RTL907x’s internal processor finds out which interface can reach the next hop router by the mapping of “NEXT_HOP_IP” and outgoing interface in the Next Hop Mapping Table. Finally, a subnet is mapped to an outgoing interface and it is configured in the Network Routing Table.
5. Use the DIP IP header to look up the entry of the Network Routing Table. After a successful lookup, the three important pieces of information (DA, SA, VLAN ID) can be obtained from the hit entry. In this entry, the RTL9054/RTL9068/RTL907x will already know the packet egress interface’s destination VLAN ID (DST_VID), MAC address (OUTGOING_IF_SMAC) and physical destination port. The RTL9054/RTL9068/RTL907x shall use the DIP of this packet to send an NDP/ARP request via the corresponding physical port.
6. Note: In a static routing environment, the user needs to configure the DIP and outgoing interfaces. Every interface includes the MAC address/VLAN ID/physical port.
7. Host B will provide its MAC address after receiving the NDP/ARP address resolution request packet. When the RTL9054/RTL9068/RTL907x receives this packet, SA learning will also be carried out (Host B MAC address is now recorded in the RTL9054/RTL9068/RTL907x’s L2 table).
8. Because of step 6, we will now have Host B’s MAC address in the L2 table. Therefore, the NDP/ARP cache is unnecessary. What the RTL9054/RTL9068/RTL907x still needs is to indicate where the entry in the L2 table is, and link it to the corresponding hit entry of the host’s routing table. The RTL9054/RTL9068/RTL907x shall generate a new packet which contains a new SA and VLAN ID from step 5, and a new DA from step 7.
9. The packet can now be sent to the correct destination. All packets with the same DIP (after the above routing procedures) are forwarded according to the host’s routing table. Wire speed can be reached by a complete host routing table entry.

Multicast Routing:

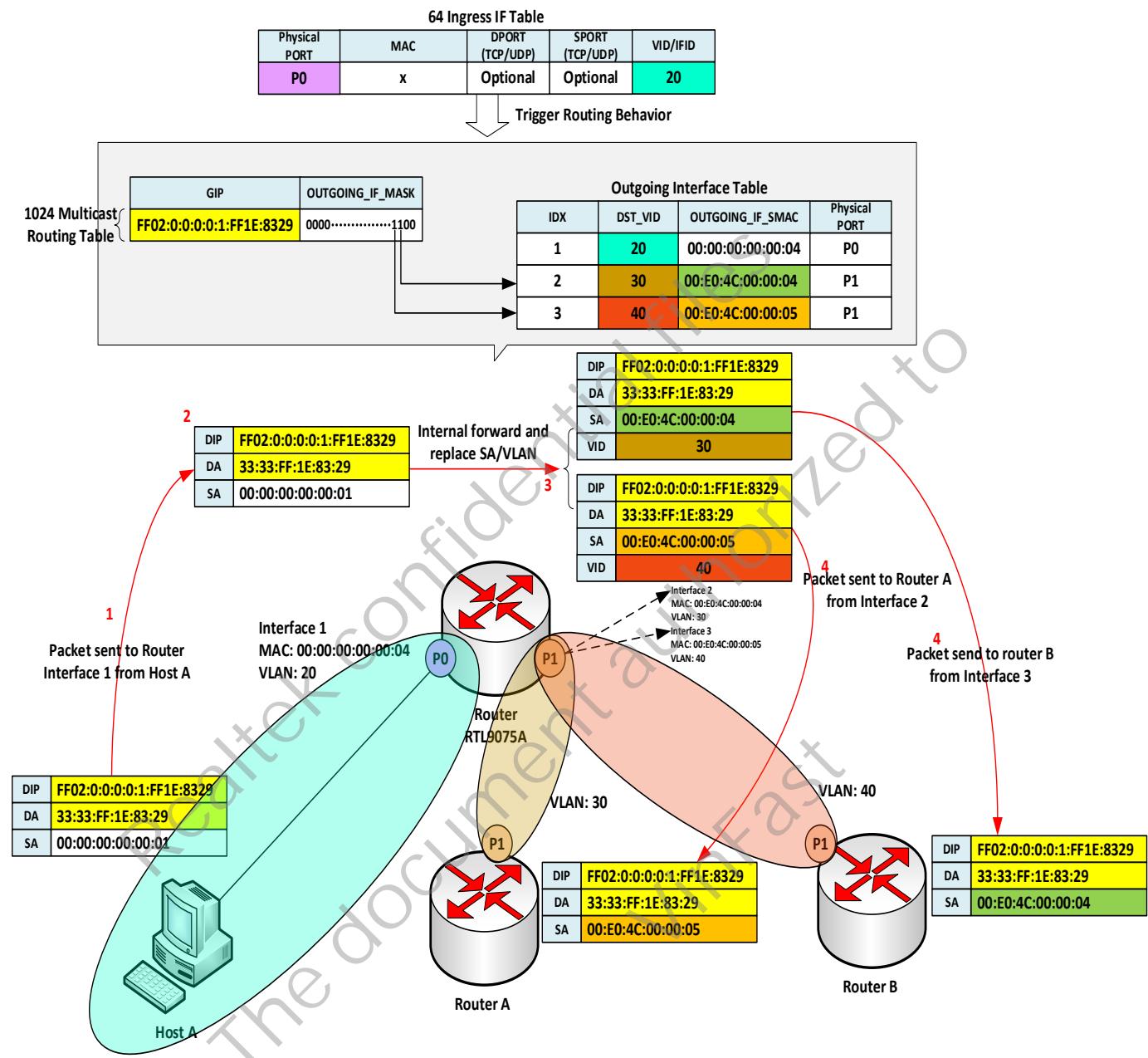


Figure 56. Multicast Routing Behavior

The following illustrates the Multicast routing behavior:

1. Host A sends a multicast packet.
2. When the RTL9054/RTL9068/RTL907x receives this packet and identifies this packet as a multicast packet, the multicast routing flow will begin. The RTL9054/RTL9068/RTL907x uses the group IP address in the IP header to lookup the multicast routing table. If one entry is hit, the RTL9054/RTL9068/RTL907x shall know how many interfaces need to flood this packet from the entry corresponding with the outgoing interface mask (OUTGOING_IF_MASK), and each bit in this field represents an interface.
3. The RTL9054/RTL9068/RTL907x shall generate all required multicast packets with different VLAN IDs and MAC addresses from an outgoing interface table.
4. Note: In a static routing environment, the user needs to configure the group IP and outgoing interfaces. Every interface includes the MAC address/VLAN ID/physical port.
5. In this case, there are two interfaces in one physical port and these two interfaces are requested with this multicast service. The RTL9054/RTL9068/RTL907x shall send the packet twice with a different SA/VID to hosts A and B via the physical port.

8.12. Mirroring

Traffic mirroring is helpful in network traffic analysis and monitoring. The RTL9054/RTL9068/RTL907x supports port mirroring, allowing ingress and/or egress traffic to be monitored by a single port that is defined as the mirror port. A copy of the mirrored packet will be routed to the mirror port. The mirror port can be any port of the RTL9054/RTL9068/RTL907x.

The RTL9054/RTL9068/RTL907x supports port-based and flow-based mirroring functions. In port-based mirroring, all ingress and egress of mirrored ports can be selected independently as mirrored traffic. When a port is ingress mirrored, any packet received on that port is copied to the mirroring port. When a port is egress mirrored, any packet transmitted from that port is copied to the mirroring port. However in flow-based mirroring, only specific packets are copied to the mirroring port. It is defined through ACL rules and configured ACL action as mirrored before mirroring.

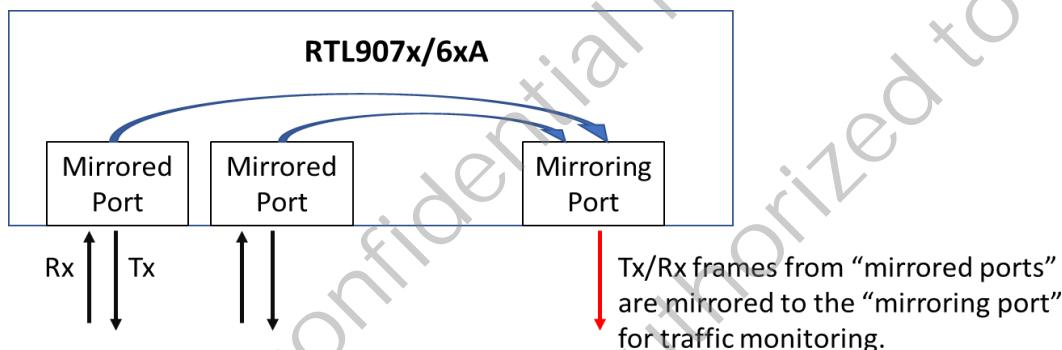


Figure 57. Mirrored and Mirroring Ports

The RTL9054/RTL9068/RTL907x supports the following mirroring configurations:

- Monitors multiple mirrored ports simultaneously
- Each mirrored port can be ingress or egress mirroring independently
- Mirrored packets can be broadcast, multicast or unicast
- Both good packets and CRC error packets can be mirrored
- Mirroring across VLAN
- Filters forwarded traffic to the mirroring port
- Remote Switch Port Analyzer (RSPAN): This function enables cross-switch packet monitoring by mirroring the packet at any Port A (mirrored port) of switch X to any Port B (mirroring port) of switch Y
- Mirrors original packets or modified packets. Modified packets are the packets being processed inside the switch, for example, the packets being tagged or de-tagged

8.13. Quality of Service (QoS)

The RTL9054/RTL9068/RTL907x provides these features to support QoS:

- Supports port-based, innertag-based, outertag-based, hybrid-based, and DSCP-based priority
- Supports various bandwidth control mechanisms, such as ingress bandwidth control, egress queue rate control, and egress port rate control
- Supports various traffic schedulers, such as Strict Priority (SP), Weighted Round Robin (WRR), Weighted Fair Queuing (WFQ), and Credit-based Shaper (CBS)
- Supports priority remarking
- Supports 8 TX queues per port

The QoS process flow of the RTL9054/RTL9068/RTL907x is shown in Figure 58. In the following sections, we are going to introduce how the switch does traffic classification, traffic scheduling, traffic priority remarking, bandwidth control, and bandwidth reservation within the QoS function.

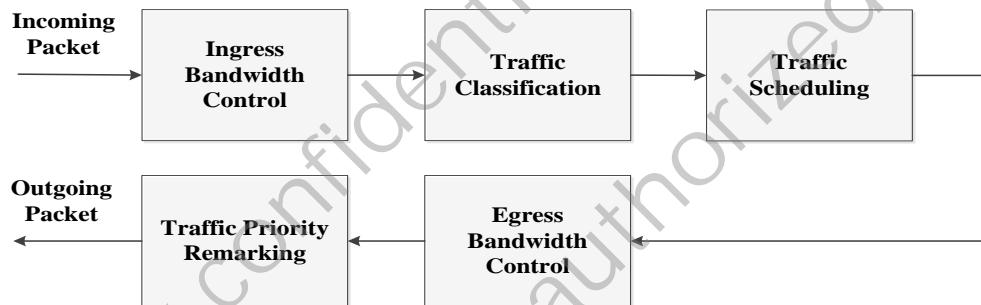


Figure 58. QoS Process Flow

8.13.1. Ingress Bandwidth Control

When packets come from any of the physical ports of the switch, the RTL9054/RTL9068/RTL907x provides two leaky buckets for each port at the beginning of packet reception, which are Leaky Bucket 0 (LB0) and Leaky Bucket 1 (LB1), to support ingress bandwidth control. Users can set a preferred bandwidth rate for each leaky bucket to limit the data rate of incoming packets. This feature can help users to prevent a best-effort or some other unwanted traffic from storming the network.

By default, all incoming packets are put into the LB0 of the incoming port. Incoming packets can be put into the LB1 by using the Access Control List (ACL) function.

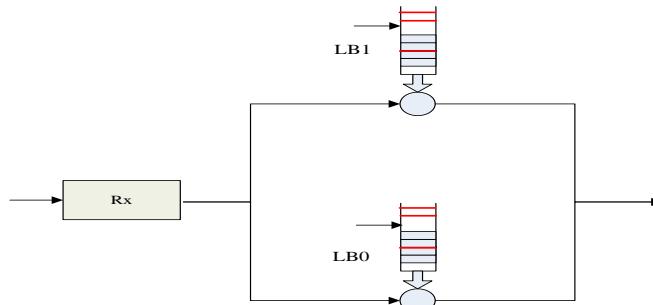


Figure 59. Ingress Bandwidth Control

8.13.2. Traffic Classification

The purpose of this stage is to classify incoming packets into 8 different traffic classes and enqueue packets. It is composed of two essential parts, priority extraction and traffic queuing. Priority extraction is the process of mapping priorities coming from different priority sources to an internal priority. Once the internal priority is decided, the traffic is going to be enqueued to one of the TX queues of an outgoing port. Traffic queuing is another way to map the internal priority to a final traffic class. The final traffic class is also the queue number where the packets should go.

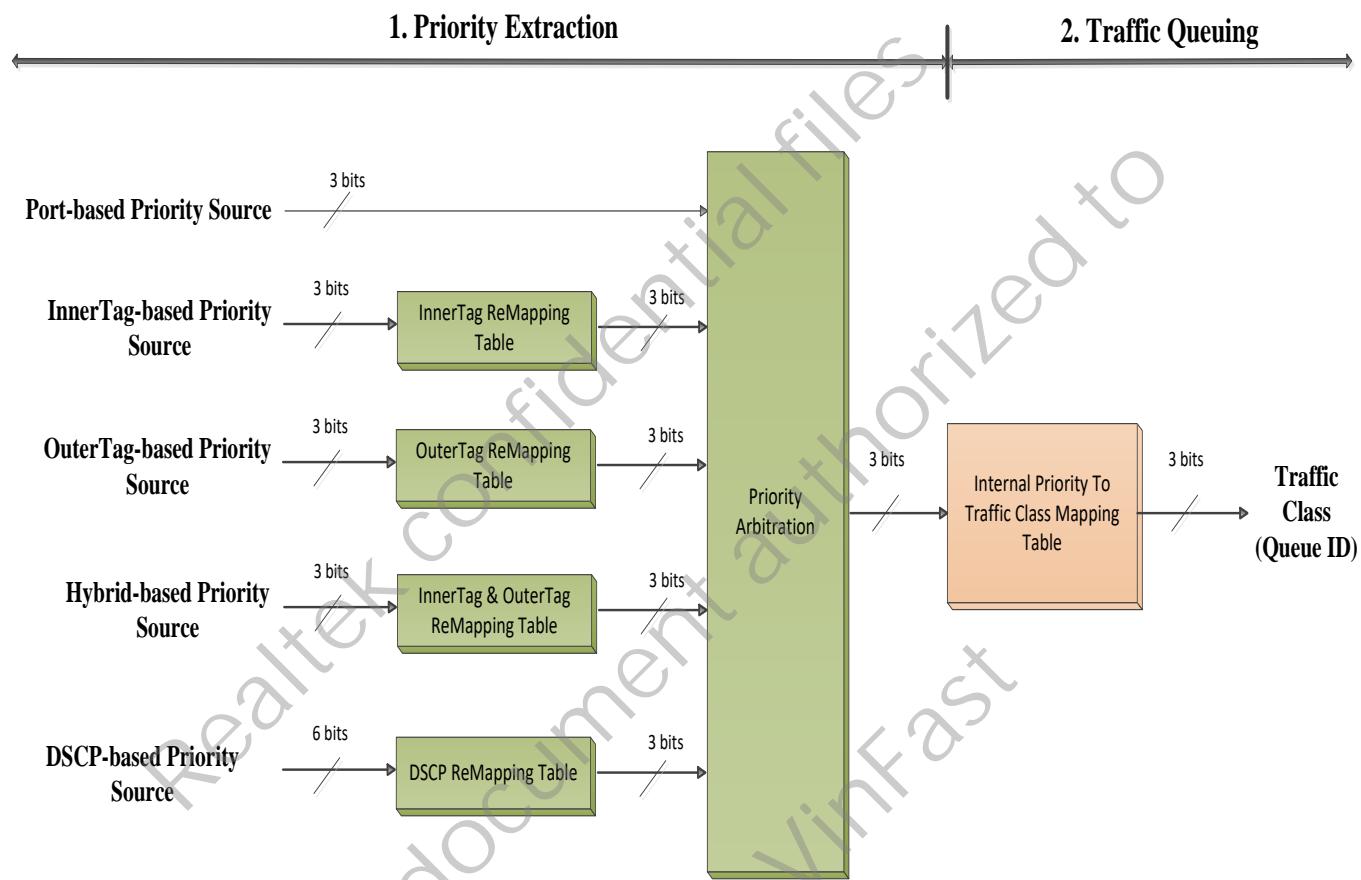


Figure 60. Traffic Classification Process Flow

8.13.2.1 Priority Extraction

As Figure 60 shows, the RTL9054/RTL9068/RTL907x allows five different priority sources. They are port-based, innertag-based, outertag-based, hybrid-based, and DSCP-based separately.

The port-based priority source uses the pre-configured innertag or outertag priority value for the incoming port of a packet as its internal priority. Choosing either a pre-configured innertag or outertag priority value depends on which VLAN tag is the current forwarding based tag of the switch.

The innertag-based priority source uses the priority field of the inner VLAN packet's tag as its temporary priority. If the packet does not have an inner VLAN tag, this priority source gets 0 as its temporary priority.

Then, the temporary priority will be remapped to an internal priority according to an innertag remapping table.

The outertag-based priority source uses the priority field of the outer VLAN packet's tag as its temporary priority. If the packet does not have an outer VLAN tag, this priority source gets 0 as its temporary priority. Then, the temporary priority will be remapped to an internal priority according to an outertag remapping table.

The hybrid-based priority source combines port-based, innertag-based, and outertag-based priority sources together. The switch sees which VLAN tag is the current forwarding based tag of the switch. If the inner VLAN tag is the current forwarding based tag of the switch, and

1. If the packet has an inner VLAN tag, the hybrid-based priority source works exactly as the innertag-based priority source.
2. If the packet does not have an inner VLAN tag, the hybrid-based priority source works exactly as the port-based priority source.

On the contrary, if the outer VLAN tag is the current forwarding based tag of the switch, and

1. If the packet has an outer VLAN tag, the hybrid-based priority source works exactly as the outertag-based priority source.
2. If the packet does not have an outer VLAN tag, the hybrid-based priority source works exactly as the port-based priority source.

The DSCP-based priority source uses the DSCP field of the IP header of the packet as its temporary priority. If the packet does not have an IP header, this priority source gets 0 as its temporary priority. Then, the temporary priority will be remapped to an internal priority according to a DSCP remapping table.

Once each priority source gets its own internal priority, a priority arbitrator is used to choose one of those internal priorities as the final internal priority. The RTL9054/RTL9068/RTL907x allows users to assign a weight value for each priority source, and then the priority arbitrator chooses the internal priority of a priority source with the highest weight value. If two or more priority sources have the same weight value, the priority arbitrator chooses the highest internal priority value.

8.13.2.2 Traffic Queuing

In the previous stage, the switch gets an internal priority for the packet. The next step is to map the internal priority to a traffic class (which is also known as a TX queue ID) according to the internal priority to a traffic class mapping table, and then enqueue the packet into the associated TX queue of the outgoing port. The RTL9054/RTL9068/RTL907x supports 8 TX queues per port.

8.13.3. Traffic Scheduling

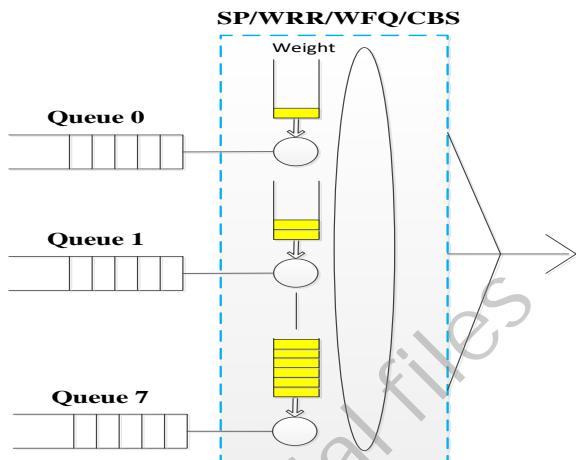


Figure 61. Traffic Scheduler

The RTL9054/RTL9068/RTL907x provides four types of traffic scheduler to achieve traffic scheduling, bandwidth control, and bandwidth reservation. They are Strict Priority (SP), Weighted Round Robin (WRR), Weighted Fair Queuing (WFQ), and Credit-based Shaper (CBS) separately. Basically, each queue can be configured to use any one of these traffic schedulers. However, in a single port, it is forbidden to use WRR, WFQ, and CBS together at the same time. In other words, the possible combinations of traffic scheduler in a single port are all SP, all WRR, all WFQ, all CBS, SP+WRR, SP+WFQ, or SP+CBS. Others such as WRR+WFQ and WRR+CBS are not allowed.

While scheduling traffic, the higher number queue always gets higher priority to be selected if other conditions are the same. That means queue 7 has the highest priority and queue 0 has the lowest priority. Besides, different traffic schedulers also have different priorities. In the RTL9054/RTL9068/RTL907x, CBS and SP are in the same scheduling group. While WRR/WFQ are in a different scheduling group, the CBS&SP group is serviced and selected before the WRR/WFQ group is serviced and selected.

If a queue is configured as WRR or WFQ, it is able to adjust the queue weight. The queue weight is the priority among queues using WRR or WFQ.

8.13.4. Egress Bandwidth Control

The RTL9054/RTL9068/RTL907x provides capabilities to egress bandwidth control from the perspective of a queue or a port. If a queue is configured as SP or WRR, it is able to set a queue rate limit for the queue to control the throughput of the queue. Similarly, it is able to set a port rate limit for a port to control the throughput of the port. The queue rate limit and the port rate limit must be a multiple of 8Kbps.

8.13.5. Traffic Priority Remarking

The purpose of this stage is to replace the priority field of the VLAN header of the packet with a remarked priority value before transmitting it out of the switch, according to the inner tag priority, outer tag priority, or DSCP.

8.14. Reserved Multicast Address Handling

The RTL9054/RTL9068/RTL907x supports Reserved Multicast Address (RMA) as defined in the IEEE 802.1 standard. For each RMA, the actions include, Forward, Drop, Redirect, Trap, or Copy to CPU. The action priority is higher than the results of a Layer-2 Table lookup. The default actions are shown in Table 49.

Table 49. Reserved Multicast Address Default Actions

Name	Address	Default
Bridge Group Address	01-80-C2-00-00-00	Forward
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	Drop
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02	Drop
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03	Forward
Reserved for future protocol standards	01-80-C2-00-00-04 – 01-80-C2-00-00-0D, 01-80-C2-00-00-0F	Drop
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	Forward
All LANs Bridge Management Group Address	01-80-C2-00-00-10	Forward
GMRP	01-80-C2-00-00-20	Drop
GVRP	01-80-C2-00-00-21	Forward
Reserved for use by Multiple Registration Protocol (MRP) Applications	01-80-C2-00-00-22 – 01-80-C2-00-00-2F	Drop
IEEE 802.1ag PDU CCM/LTM	01-80-C2-00-00-31 – 01-80-C2-00-00-3F	Forward

8.15. Interrupt Function

The RTL9054/RTL9068/RTL907x supports an interrupt function that is used to inform the external CPU or internal CPU should important network events relevant to the host device occur.

An INT pin and internal signal are implemented to interrupt the external CPU and internal CPU respectively when the defined interrupt event occurs. The INT pin can be programmed to output low level, high level, positive pulse, or negative pulse as an interrupt signal.

Interrupt events include: GPIO pin pre-defined input, ACL entry hit, source port of a MAC address change (SA moving), MIB counter overflow, link status change, packet drop by switch, and source MAC learning constraint.

8.16. LED Function

The RTL9054/RTL9068/RTL907x provides a flexible LED display to show the port link status and other information for indication and diagnosis purposes. There are ten LED pins for each 100BASE-T1 or 1000BASE-T1 port and two LED pins for FE ports. They indicate the port link status by default. All LED pin statuses are represented as active-low or high depending on flash configurations.

- The LED function supports two hardware modes, PHY mode and MAC mode. We can configure different modes by register
- In MAC mode, LED blinking time can be set to 32ms or 128ms. Each LED can be individually controlled via registers to indicate customized information
- PHY mode is the same as MAC mode except the blinking times are 20ms, 40ms, and 60ms
- In MAC mode, the RTL9054/RTL9068/RTL907x's LED power on blinking is enabled by default. When the RTL9054/RTL9068/RTL907x is powered on or the hardware is reset, all the LEDs blink at 1.5 second intervals (on 1.5s and then off 1.5s), and finally indicate the current LED status. Power on blinking can be disabled via flash configuration
- In PHY mode, the RTL9054/RTL9068/RTL907x has Realtek Cable Test (RTCT) mode for cable diagnosis. It can detect 100BASE-T1 port cable status' such as open and short

8.17. Port Isolation

Port isolation (also known as private VLAN) allows the RTL9054/RTL9068/RTL907x to restrict traffic flow flexibly. The traffic in both directions between any two physical ports can be blocked independently and simultaneously even within the same VLAN. With regard to a switch connect to end users, Port Isolation is a useful feature for network resource management. Typically, all ports except the port connected to a server, router or firewall are configured as isolated to each other. Then all packets are transmitted to the specific port and forwarded in the normal way afterwards. Note that the mirrored traffic and packets trapped to the CPU cannot be isolated by this function.

8.18. VLAN

The RTL9054/RTL9068/RTL907x provides these features to support the IEEE 802.1Q VLANs:

- Supports port-based and tag-based VLAN
- Supports VLAN tag parsing, insertion, and removal
- Supports a 4096-entry VLAN table
- Supports double tagging
- Supports a flexible ingress packet filtering based on the VLAN tag status
- Supports the IEEE 802.1Q ingress filtering and egress filtering functions
- Supports a flexible VLAN retagging function

The VLAN process flow of the RTL9054/RTL9068/RTL907x is shown in Figure 62. In the following sections, we are going to introduce each part from the aspect of how the switch handles, filters, and forwards incoming packets within the VLAN function.

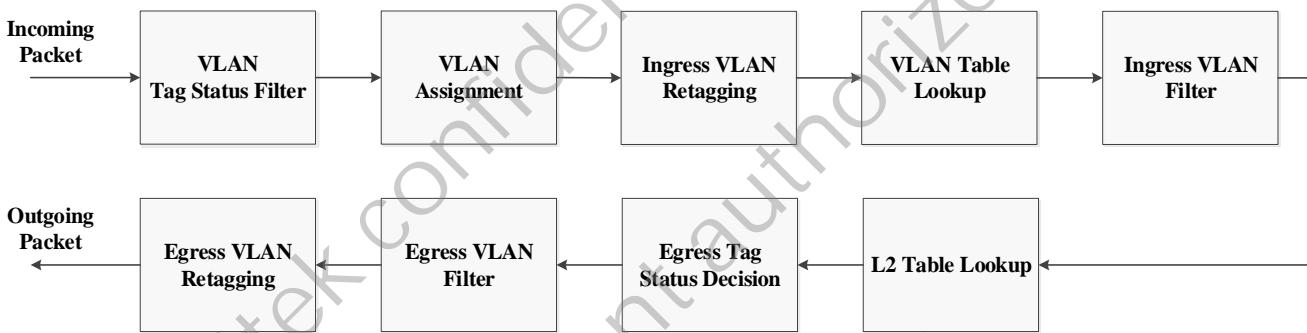


Figure 62. VLAN Process Flow

8.18.1. VLAN Tag Status Filter

When a packet comes from any one of physical ports of the switch, the switch firstly tries to recognize whether or not it has VLAN tags or parse VLAN tags. That means the switch knows the tag status of the incoming packet. For example, if it is a double-tagged packet, an inner-tagged packet, an outer-tagged packet, or an untagged packet, then the RTL9054/RTL9068/RTL907x will provide a VLAN tag status filter here to filter the incoming packet according to its tag status. The packet can be forwarded to the next stage only if the VLAN tag status filter gets a ‘permit’ action for the incoming packet.

The VLAN tag status filter classifies the tag status into the following five types, and allows users to configure a ‘permit’ or ‘drop’ action for each type tag status individually.

- Inner-tagged packet
- Inner untagged or inner priority-tagged frame
- Outer-tagged packet
- Outer untagged or outer priority-tagged frame
- Double-tagged packet

For example, users can use this feature to drop inner-tagged and double-tagged packets, but permit others.

However, the incoming packet possibly belongs to two or more types of the above tag status classifications at the same time. For example, a double-tagged packet is also an inner-tagged packet and an outer-tagged packet. Once the action of any one of its belonging types is a ‘drop’ action, the incoming packet should be dropped immediately by the switch.

8.18.2. VLAN Assignment

Once the incoming packet passes the VLAN tag status filter, the switch needs to know which VLAN the incoming packet will forward in. Therefore, the next thing to do is to assign a VLAN ID for the incoming packet. In the RTL9054/RTL9068/RTL907x, there are two ways to do this, which are Port-based and Tag-based.

When using Port-based, the VLAN ID of a packet comes from a pre-configured VLAN ID value of an incoming port of the packet. In other words, it is necessary to pre-configure a VLAN ID for each port while using this mode.

When using Tag-based, if a packet is a tagged packet, the VLAN ID of the packet comes from the VLAN ID field of the VLAN header of the packet. Otherwise, if the packet is an untagged packet, the VLAN ID of the packet still comes from the pre-configured VLAN ID value of the incoming port of the packet.

8.18.3. VLAN Table Lookup

Next, the switch needs to identify the VLAN member ports, untagged ports, and the following VLAN parameters of the VLAN by looking up the VLAN table:

- Filtering database ID (FID)
- Independent VLAN Learning (IVL) or Shared VLAN Learning (SVL) configuration
- VLAN based forwarding configuration

These parameters affect how the switch forwards the packet, how the switch looks up the L2 table, and where the packet goes.

If the VLAN based forwarding of the VLAN is set as ALE_BASED_FWD, the destination ports of the incoming packet will be decided by looking up the L2 table in the next stage. Otherwise, if it is set as VLAN_BASED_FWD, the incoming packet will be forwarded to all the member ports of the VLAN except the incoming port of the incoming packet.

When the VLAN is set to IVL mode, the switch will use the VID + Source MAC Address of the incoming packet as the key to lookup the L2 table in the ‘L2 Table Lookup’ stage. When the VLAN is set as SVL mode, the switch will use the FID + Source MAC Address of the incoming packet as the key to lookup the L2 table in the ‘L2 Table Lookup’ stage.

Besides, the RTL9054/RTL9068/RTL907x provides a 4096-entry VLAN table to fully support the maximum number of possible VLANs.

8.18.4. Ingress VLAN Filter

The RTL9054/RTL9068/RTL907x supports the IEEE 802.1Q ingress filtering function here to provide the capability to discard the incoming packet if its incoming port is not a member port of the VLAN.

For example, a packet with a VLAN tag (VID = 100) is received from port 0. If the tag-based mode is used and the member ports of VLAN 100 do not include port 0, the packet will be discarded when the ingress VLAN filter is enabled.

8.18.5. Ingress VLAN Retagging

The RTL9054/RTL9068/RTL907x also supports a flexible ingress VLAN retagging function to provide the capability to change the VLAN ID of the incoming packet; then, the packet can be forwarded in the new VLAN. Users can define up to 32 rules on demand to control packets belonging to a given VLAN ID or sending to which port to change the VLAN ID.

Table 50. Ingress VLAN Retagging Parameters

Bit Width	Field	Description
13	PBM	Affected Ingress Port Mask.
12	NEW_VID	New VLAN ID.
12	ORIGINAL_VID	Original VLAN ID to be replaced.
1	VALID	Entry valid or not. 0: Invalid 1: Valid

8.18.6. L2 Table Lookup

As mentioned in the ‘VLAN Table Lookup’ stage, the switch knows the key to lookup the L2 table. The purpose of looking up the L2 table is to identify destination ports which the incoming packet will be forwarded to.

8.18.7. Egress Tag Status Decision

Once the destination ports for the incoming packet are confirmed, the switch will forward the packet to the destination ports. Before sending the packet out, the switch needs to check if the destination port is an untagged port or a tagged port in the VLAN and egress tag status configuration of the destination port, to decide the tag status of the outgoing packet for each destination port.

Table 51. Egress Tag Status Decision

Egress Tag Status Configuration \ VLAN Table Configuration	Double Tagged	Outer Tagged	Inner Tagged	Untagged
VLAN Table Configuration \ Untagged Port	Untagged	Untagged	Untagged	Untagged
VLAN Table Configuration \ Tagged Port	Double Tagged	Outer Tagged	Inner Tagged	Untagged

8.18.8. Egress VLAN Filter

The RTL9054/RTL9068/RTL907x supports the IEEE 802.1Q egress filtering function here to provide a capability to discard the outgoing packet if its destination port is not a member port of the VLAN.

8.18.9. Egress VLAN Retagging

The RTL9054/RTL9068/RTL907x supports a flexible egress VLAN retagging function here to provide the capability to change the VLAN ID of the outgoing packet. Users can define up to 32 rules on demand to control packets belonging to a given VLAN ID or sending to which port to change the VLAN ID.

Table 52. Egress VLAN Retagging Parameters

Bit Width	Field	Description
13	PBM	Affected Egress Port Mask.
12	NEW_VID	New VLAN ID.
12	ORIGINAL_VID	Original VLAN ID to be replaced.
1	VALID	Entry valid or not. 0: Invalid 1: Valid

8.19. Layer 2 Traffic Suppression (Storm Control)

A traffic storm generated when unnecessary packets flood the LAN, occupies the network resource, which in turn leads to poor network performance, and on occasion even a complete shutdown of the network service. The RTL9054/RTL9068/RTL907x supports a storm control function to monitor ingress traffic levels and discarded broadcast, multicast and unknown unicast packets when the specific traffic level is exceeded. Four types of traffic storms can be controlled.

- Broadcast storm: Treats destination address = FF-FF-FF-FF-FF-FF packets as storm
- Multicast storm: Treats destination with I/G bit 1 packets as storm, including known and unknown multicast packets
- Unknown unicast storm: Treats destination lookup miss with I/G bit 0 packets as storm
- Unknown multicast storm: Treats destination lookup miss with I/G bit 1 packets as storm

Each port of the RTL9054/RTL9068/RTL907x can limit different types of traffic storms independently and dynamically.

8.20. Management Information Base (MIB) Counter

The RTL9054/RTL9068/RTL907x implements various MIB (Management Information Base) counters for network monitoring, analysis, or debug purposes. The RTL9054/RTL9068/RTL907x MIB (Management Information Base) counters include:

- RFC2819 – RMON MIB Group 1, 2, 3, 9
- RFC3635 – Ethernet-like MIB
- RFC2863 – Interface Group MIB
- RFC1213 – MIB II
- RFC4188 – Bridge MIB
- RFC4363 – Bridge MIB Extension
- Realtek Defined MIB Counter

Table 53. MIB per Port Counter List

Name	Definition	RFC
ifOutOctets [31:0] (32-bit)	The total number of good octets transmitted out of the interface, including framing characters. This counter indicates from bit 0 to bit 31.	CTC RFC1213 RFC2863
ifOutOctets [63:32] (32-bit)	The total number of good octets transmitted out of the interface, including framing characters. This counter indicates from bit 32 to bit 63.	CTC RFC1213 RFC2863
dot1dTpPortOutFrames (32-bit)	The number of frames which size are larger than 64 byte (>= 64 byte) that have been transmitted by this port to its segment.	CTC
dot3OutPauseFrames (32-bit)	A count of MAC Control frames transmitted on this interface with an opcode indicating the PAUSE operation. This counter does not increment when the interface is operating in half-duplex mode.	CTC RFC3635
ifOutUcastPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted to a subnetwork-unicast address, not including those that were discarded or not sent.	-
ifOutMulticastPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a multicast address at this sub-layer, not including those that were discarded or not sent. For a MAC layer protocol, this includes both Group and Functional addresses.	-
ifOutBroadcastPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a broadcast address at this sub-layer, not including those that were discarded or not sent.	-
dot3StatsSingleCollisionFrames (32-bit)	A count of frames that are involved in a single collision and are subsequently transmitted successfully. (half duplex)	CTC RFC3635
dot3StatsMultipleCollisionFrames (32-bit)	A count of frames that are involved in more than one collision and are subsequently transmitted successfully. (half duplex)	CTC RFC3635
etherStatsCollisions (32-bit)	The number of collisions experienced in a port during packet transmissions.	RFC2819
dot3StatsDeferredTransmissions (32-bit)	A count of frames for which the first transmission attempt on a particular interface is delayed because the medium is busy. (half duplex)	CTC RFC3635

Name	Definition	RFC
dot3StatsLateCollisions (32-bit)	The number of times that a collision is detected on a particular interface later than one slotTime into the transmission of a packet. (half duplex)	RFC3635
dot3StatsExcessiveCollisions (32-bit)	A count of frames for which transmission on a particular interface exceeds 16 collisions (>16 collisions).	RFC3635
TxPkt (32-bit)	The number of frames that have been transmitted by this port to its segment.	-
ifInOctets [31:0] (32-bit)	The total number of octets received on the interface in good packets (excluding SFD but including FCS octets). This counter indicates from bit 0 to bit 31.	CTC RFC1213 RFC2863
ifInOctets [63:32] (32-bit)	The total number of octets received on the interface in good packets (excluding SFD but including FCS octets). This counter indicates from bit 32 to bit 63.	CTC RFC1213 RFC2863
etherStatsOctets [31:0] (32-bit)	The total number of octets of data (including those in bad packets) received on the network (excluding SFD but including FCS octets). This counter indicates from bit 0 to bit 31.	RFC2819
etherStatsOctets [63:32] (32-bit)	The total number of octets of data (including those in bad packets) received on the network (excluding SFD but including FCS octets). This counter indicates from bit 32 to bit 63.	RFC2819
dot1dTpPortInFrames (32-bit)	The number of frames that have been received by this port from its segment.	CTC RFC4188
dot3InPauseFrames (32-bit)	A count of MAC Control frames received on this interface with an opcode indicating the PAUSE operation (DA = 0180C2000001, etherType = 8808, opcode = 0001). This counter does not increment when the interface is operating in half-duplex mode.	CTC RFC3635
ifInUcastPkts (32-bit)	The number of subnetwork-unicast packets delivered to a higher-layer protocol.	CTC RFC1213 RFC2863
etherStatsMulticastPkts (32-bit)	The total number of good packets received that were directed to a multicast address. Note that this number does not include packets directed to the broadcast address.	CTC RFC2819
etherStatsBroadcastPkts (32-bit)	The total number of good packets received that were directed to the broadcast address. Note that this does not include multicast packets.	CTC RFC2819
etherStatsFragments (32-bit)	The total number of packets received that were less than 64 octets in length (excluding framing bits but including FCS octets) and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).	RFC2819
RxPktBelow64 (32-bit)	The number of frames that have been received by this port and the size are under 64 byte (<64byte) and frame include tag.	-
EtherStatsJabbers (32-bit)	The total number of packets received that were longer than 1518 octets (excluding framing bits, but including FCS octets), and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).	RFC2819
dot3StatsFrameTooLongs (32-bit)	A count of frames received on a particular interface that exceed the maximum permitted frame size.	CTC RFC3635
dot3StatsFCSErrors (32-bit)	A count of frames received on a particular interface that are an integral number of octets in length but do not pass the FCS check.	CTC RFC3635

Name	Definition	RFC
dot3StatsAlignmentErrors (32-bit)	A count of frames received on a particular interface that are not an integral number of octets in length and do not pass the FCS check.	RFC3635
dot3StatsSymbolErrors (32-bit)	For an interface operating at 100Mb/s, the number of times there was an invalid data symbol when a valid carrier was present (1 packet count once). For an interface operating in full-duplex mode at 1000Mb/s, the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that caused the PHY to indicate a ‘Data reception error’ on the GMII. The count represented by an instance of this object is incremented at most once per carrier event, even if multiple symbol errors occur during the carrier event. This count does not increment if a collision is present. This counter does not increment when the interface is operating at 10Mb/s.	RFC3635
dot3ControlInUnknownOpcodes (32-bit)	A count of MAC Control frames received on this interface that contain an opcode that is not supported by this device. Number of received MAC control frames (ether type = 8808) with an unknown opcode (! = 0001).	RFC3635
EtherStatsDropEvents (32-bit)	The total number of events in which packets were dropped by the probe due to lack of resources (frame buffer). Note that this number is not necessarily the number of packets dropped; it is just the number of times this condition has been detected. DSC drop, DSC runout.	RFC2819
dot1dTpPortInDiscards (32-bit)	Count of received valid frames that were discarded (i.e., filtered) by the Forwarding Process. Ingress and egress filter.	RFC1493 RFC2674
ifOutDiscards (32-bit)	The count of frames drained out packet including drop packet by Late Collision or Excessive Collision.	-
etherStatsPkts64Octets (32-bit)	The total number of packets (including bad packets) received that were 64 octets in length (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsPkts65to127Octets (32-bit)	The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsPkts128to255Octets (32-bit)	The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsPkts256to511Octets (32-bit)	The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsPkts512to1023Octets (32-bit)	The total number of packets (including bad packets) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsPkts1024to1518 (32-bit)	The total number of packets (including bad packets) received that were between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets).	CTC RFC2819
etherStatsOversizePkts (32-bit)	The total number of packets received that were longer than 1518 octets (excluding framing bits, but including FCS octets) and were otherwise well formed.	CTC RFC2819

Name	Definition	RFC
etherStatsUndersizePkts (32-bit)	The total number of packets received that were less than 64 octets long (excluding framing bits, but including FCS octets) and were otherwise well formed.	CTC RFC2819
etherStatsPkts (32-bit)	The total number of packets (including bad packets, broadcast packets, and multicast packets) received.	RFC2819
dot3StatsCRCAlignErrors (32-bit)	A count of frames received on a particular interface that had a length (excluding framing bits, but including FCS octets) of between 64 and 1518 octets, inclusive, but had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error), or a bad FCS with a non-integral number of octets (Alignment Error).	RFC2819
PortOutUcastPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted to a subnetwork-unicast address, including those that were discarded or not sent. This counter is the same as ifOutUcastPkts in RFC2863.	CTC RFC1213 RFC2863
PortOutMultiPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a multicast address at this sub-layer, including those that were discarded or not sent. For a MAC layer protocol, this includes both Group and Functional addresses. This counter is the same as ifOutMulticastPkts in RFC2863.	CTC RFC1213 RFC2863
PortOutBroadPkts (32-bit)	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a broadcast address at this sub-layer, including those that were discarded or not sent. This counter is the same as ifOutBroadcastPkts in RFC2863.	CTC RFC1213 RFC2863
PortOutDiscards (32-bit)	The number of outbound packets which were chosen to be discarded even though no errors had been detected to prevent their being transmitted. One possible reason for discarding such a packet could be to free up buffer space. This counter is the same as ifOutDiscards in RFC2863.	RFC2863
ALEBWLimDropPktCnt (32-bit)	The number of frames discarded due to switch bandwidth limitation.	-
48pass1DropPktCnt MIB (32-bit)	Half duplex congestion condition counter.	-
IOLLenErrDropPktCnt (32-bit)	The number of frames that field length don't match field Payload in frames.	-
IOLMaxLenDropPktCnt (32-bit)	The number of frames where the frame size was larger than 1518byte (>1518byte) without tag.	-
FlowCtrlOnRxDropPktCnt (32-bit)	The number of receive frames that dropped in full-duplex mode because congestion occurs and reaching the drop threshold in switch.	-
PnShortIFGRRxDropPktCnt (32-bit)	The number of frames where the IPG is shorter than 11 byte.	-
EgressDropPktCnt (32-bit)	The number of transmit frames that dropped in half-duplex mode because of congestion caused by back-off mechanism (back-off over 16 times).	-
Q0TxPktcnt (32-bit)	The total number of packets that transmitted through queue 0.	-
Q1TxPktcnt (32-bit)	The total number of packets that transmitted through queue 1.	-
Q2TxPktcnt (32-bit)	The total number of packets that transmitted through queue 2.	-

Name	Definition	RFC
Q3TxPktcnt (32-bit)	The total number of packets that transmitted through queue 3.	-
Q4TxPktcnt (32-bit)	The total number of packets that transmitted through queue 4.	-
Q5TxPktcnt (32-bit)	The total number of packets that transmitted through queue 5.	-
Q6TxPktcnt (32-bit)	The total number of packets that transmitted through queue 6.	-
Q7TxPktcnt (32-bit)	The total number of packets that transmitted through queue 7.	-
LinkDownTxDropCnt (32-bit)	For packet-oriented interfaces, the number of outbound packets that could not be transmitted because of errors. For character-oriented or fixed-length interfaces, the number of outbound transmission units that could not be transmitted because of errors.	RFC2863
Q0TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q0 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q0TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q0 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q1TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q1 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q1TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q1 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q2TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q2 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q2TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q2 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q3TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q3 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q3TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q3 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q4TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q4 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q4TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q4 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q5TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q5 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-

Name	Definition	RFC
Q5TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q5 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q6TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q6 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q6TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q6 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
Q7TOVERRUNCNT [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. Q7 TransmissionOverrun MIB Counter. This counter indicates from bit 0 to bit 31.	-
Q7TOVERRUNCNT [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. Q7 TransmissionOverrun MIB Counter. This counter indicates from bit 32 to bit 63.	-
STConfigChangeError [31:0] (32-bit)	IEEE 802.1Qbv Function Counter. STConfigChangeError MIB Counter. This counter indicates from bit 0 to bit 31.	-
STConfigChangeError [63:32] (32-bit)	IEEE 802.1Qbv Function Counter. STConfigChangeError MIB Counter. This counter indicates from bit 32 to bit 63.	-
TXOCTETS [31:0] (32-bit)	Routing Protocol Counter. Routing EPP packet byte counter. This counter indicates from bit 0 to bit 31.	-
TXOCTETS [63:32] (32-bit)	Routing Protocol Counter. Routing EPP packet byte counter. This counter indicates from bit 0 to bit 31.	-
TXUNICASTPKTS (32-bit)	Routing Protocol Counter. Routing EPP unicast packet counter.	-
TXMULTICASTPKTS (32-bit)	Routing Protocol Counter. Routing EPP multicast packet counter.	-
ROUTE_MC_RPF_DROP (32-bit)	Routing Protocol Counter. Routing EPP MC RPF drop.	-
ROUTE_MC_MTU_FAIL_DROP (32-bit)	Routing Protocol Counter. Routing EPP MC MTU fail drop.	-
ROUTE_MC_TTLHL_FAIL_DROP (32-bit)	Routing Protocol Counter. Routing EPP MC TTL HL fail drop.	-
ROUTE_UC_ICMP_REDIR_DROP (32-bit)	Routing Protocol Counter. Routing EPP UC ICMP redir drop.	-
ROUTE_UC_MTU_DROP (32-bit)	Routing Protocol Counter. Routing EPP UC MTU fail drop.	-

Table 54. MIB System Counter List

Name	Definition	RFC
PortLinkDownDrop (32-bit)	PortLinkDownDrop MIB Counter. The total number of packets that dropped by all destination ports link down.	-
FlowCtrlDrop (32-bit)	Flow Control Function Counter. FlowCtrlDrop MIB Counter.	-
TxDisableDrop (32-bit)	RLDP Function Counter. TxDisableDrop MIB Counter.	-
MirrorEgressFilterDrop (32-bit)	Mirror Function Counter. MirrorEgressFilterDrop MIB Counter.	-
LinkAggrLinkDownDrop (32-bit)	Link Aggregation Function Counter. LinkAggrLinkDownDrop MIB Counter.	-
CPUPortSelfFilterDrop (32-bit)	Lookup Table (LUT) Function. CPUPortSelfFilterDrop MIB Counter.	-
PortIsolationDrop (32-bit)	Port Isolation Function Counter. PortIsolationDrop MIB Counter.	-
SpanTreeEgressDrop (32-bit)	STP/RSTP/MSTP Function Counter. SpanTreeEgressDrop MIB Counter.	-
EgressVLANFilterDrop (32-bit)	VLAN Function Counter. EgressVLANFilterDrop MIB Counter.	-
StormSuppressionDrop (32-bit)	Storm Control Function. StormSuppressionDrop MIB Counter.	-
SourcePortSelfFilterDrop (32-bit)	Lookup Table (LUT) Function. SourcePortSelfFilterDrop MIB Counter.	-
MulticastEgressFilterDrop (32-bit)	Lookup Table (LUT) Function. MulticastEgressFilterDrop MIB Counter.	-
MACConstrainDrop (32-bit)	Lookup Table (LUT) Function. MACConstrainDrop MIB Counter.	-
SAMovingDrop (32-bit)	Lookup Table (LUT) Function. SAMovingDrop MIB Counter.	-
SABlockDrop (32-bit)	Lookup Table (LUT) Function. SABlockDrop MIB Counter.	-
InvalidSADrop (32-bit)	Lookup Table (LUT) Function. InvalidSADrop MIB Counter.	-
LookupMissDrop (32-bit)	Lookup Table (LUT) Function. LookupMissDrop MIB Counter.	-
DABlockDrop (32-bit)	Lookup Table (LUT) Function. DABlockDrop MIB Counter.	-
L2MulticastDMACMulticasIPDrop (32-bit)	Lookup Table (LUT) Function. L2MulticastDMACMulticasIPDrop MIB Counter.	-
L2UnicastDMACMulticastIPDrop (32-bit)	Lookup Table (LUT) Function. L2UnicastDMACMulticastIPDrop MIB Counter.	-
TTLDrop (32-bit)	Routing Function Counter. TTLDrop MIB Counter.	-
IGMPMLDDrop (32-bit)	IGMP Function Counter. IGMPMLDDrop MIB Counter.	-
SwitchOwnMACDrop (32-bit)	Lookup Table (LUT) Function. SwitchOwnMACDrop MIB Counter.	-

Name	Definition	RFC
SpanTreeIngressDrop (32-bit)	STP/RSTP/MSTP Function Counter. SpanTreeIngressDrop MIB Counter.	-
Dot1XegressFilterDrop (32-bit)	IEEE 802.1X Function Counter. Dot1XEgressFilterDrop MIB Counter.	-
Dot1XingressFilterDrop (32-bit)	IEEE 802.1X Function Counter. Dot1XIngressFilterDrop MIB Counter.	-
VLANIngressFilterDrop (32-bit)	VLAN Function Counter. VLANIngressFilterDrop MIB Counter.	-
VLANTableLookupMissDrop (32-bit)	VLAN Function Counter. VLANTableLookupMissDrop MIB Counter.	-
VLANAcceptTagDrop (32-bit)	VLAN Function Counter. VLANAcceptTagDrop MIB Counter.	-
IngressBandwidthCtrlDrop (32-bit)	QOS Funciton Counter. IngressBandwidthCtrlDrop MIB Counter.	-
ACLLookupMissDrop (32-bit)	ACL Function Counter. ACLLookupMissDrop MIB Counter.	-
ACLPoliceDrop (32-bit)	ACL Function Counter. ACLPoliceDrop MIB Counter.	-
ACLDropActionDrop (32-bit)	ACL Function Counter. ACLDropActionDrop MIB Counter.	-
ACLRedirectActionDrop (32-bit)	ACL Function Counter. ACLRedirectActionDrop MIB Counter.	-
RMADrop (32-bit)	RMA Function Counter. RMADrop MIB Counter.	-
CFIDrop (32-bit)	VLAN Function Counter. CFIDrop MIB Counter.	-
RLDPTxFrames (32-bit)	Realtek Internal Debug Counter. RLDP Function Counter. RLDPTxFrames MIB Counter.	-
RLDPRxFrames (32-bit)	Realtek Internal Debug Counter. RLDP Function Counter. RLDPRxFrames MIB Counter.	-
dot1dTpLearnedEntryDiscards (32-bit)	Lookup Table (LUT) Function. dot1dTpLearnedEntryDiscards MIB Counter.	-
ROUTE_MC_HDR_OPT (32-bit)	Routing Function Counter. MC Header option extension.	-
ROUTE_MC_ILLEGAL_IP (32-bit)	Routing Function Counter. MC illegal IP drop.	-
ROUTE_MC_DMAC_MISMATCH (32-bit)	Routing Function Counter. MC DIP DMAC mismatch drop.	-
ROUTE_MC_HDR_ERR (32-bit)	Routing Function Counter. MC Header error drop.	-
ROUTE_UC_URPF (32-bit)	Routing Function Counter. UC uRPF drop.	-
ROUTE_UC_HDR_OPT (32-bit)	Routing Function Counter. UC Header option extension drop.	-
ROUTE_UC_ILLEGAL_IP (32-bit)	Routing Function Counter. UC illegal IP drop.	-

Name	Definition	RFC
ROUTE_UC_DMAC_MISMATCH (32-bit)	Routing Function Counter. UC DIP/DMAC mismatch drop.	-
ROUTE_UC_HDR_ERR (32-bit)	Routing Function Counter. UC Header error drop.	-
ROUTE_UC_TTLHL (32-bit)	Routing Function Counter. UC TTL HL fail drop.	-
ROUTE_UC_ROUTE_DIS (32-bit)	Routing Function Counter. UC route disable drop.	-
ROUTE_UC_DIP_ACT (32-bit)	Routing Function Counter. UC hit action drop.	-
ROUTE_UC_LKMISS (32-bit)	Routing Function Counter. UC lookup miss.	-
QMAXSDU_P0Q0_DROP ~ QMAXSDU_P15Q0_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0 ~ Port15 Queue 0 Max SDU drop.	-
QMAXSDU_P0Q1_DROP ~ QMAXSDU_P15Q1_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0 ~ Port15 Queue 1 Max SDU drop.	-
QMAXSDU_P0Q2_DROP ~ QMAXSDU_P15Q2_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0 ~ Port15 Queue 2 Max SDU drop.	-
QMAXSDU_P0Q3_DROP ~ QMAXSDU_P15Q3_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0 ~ Port15 Queue 3 Max SDU drop.	-
QMAXSDU_P0Q4_DROP ~ QMAXSDU_P15Q4_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0 ~ Port15 Queue 4 Max SDU drop.	-
QMAXSDU_P0Q5_DROP ~ QMAXSDU_P15Q5_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0~Port15 Queue 5 Max SDU drop.	-
QMAXSDU_P0Q6_DROP ~ QMAXSDU_P15Q6_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0~Port15 Queue 6 Max SDU drop.	-
QMAXSDU_P0Q7_DROP ~ QMAXSDU_P15Q7_DROP (32-bit)	IEEE 802.1Qbv Function Counter. Port0~Port15 Queue 7 Max SDU drop.	-
LAG0OCTETSTXOK_LSB ~ LAG7OCTETSTXOK_LSB (32-bit)	Link Aggregation Function Counter. aAggOctetsTxOK MIB Counter [31:0].	-
LAG0OCTETSTXOK_MSB ~ LAG7OCTETSTXOK_MSB (32-bit)	Link Aggregation Function Counter. aAggOctetsTxOK MIB Counter [63:32].	-
LAG0FRAMESTXOK ~ LAG7FRAMESTXOK (32-bit)	Link Aggregation Function Counter. aAggFramesTxOK MIB Counter.	-
LAG0MULTICASTFRAMESTXOK ~ LAG7MULTICASTFRAMESTXOK (32-bit)	Link Aggregation Function Counter. aAggMulticastFramesTxOK MIB Counter.	-

Name	Definition	RFC
LAG0BROADCASTFRAMESTXOK ~ LAG7BROADCASTFRAMESTXOK (32-bit)	Link Aggregation Function Counter. aAggBroadcastFramesTxOK MIB Counter.	-
LAG0FRAMESDISCATDEDONTX ~ LAG7FRAMESDISCATDEDONTX (32-bit)	Link Aggregation Function Counter. aAggFramesDiscardedOnTx MIB Counter.	-
LAG0FRAMESWITHTXERRORS ~ LAG7FRAMESWITHTXERRORS (32-bit)	Link Aggregation Function Counter. aAggFramesWithTxErrors MIB Counter.	-
LAG0OCTETSRXOK_LSB ~ LAG7OCTETSRXOK_LSB (32-bit)	Link Aggregation Function Counter. aAggOctetsRxOK MIB Counter [31:0].	-
LAG0OCTETSRXOK_MSB ~ LAG7OCTETSRXOK_MSB (32-bit)	Link Aggregation Function Counter. aAggOctetsRxOK MIB Counter [63:32].	-
LAG0FRAMESRXOK ~ LAG7FRAMESRXOK (32-bit)	Link Aggregation Function Counter. aAggFramesRxOK MIB Counter.	-
LAG0MULTICASTFRAMESRXOK ~ LAG7MULTICASTFRAMESRXOK (32-bit)	Link Aggregation Function Counter. aAggMulticastFramesRxOK MIB Counter.	-
LAG0BROADCASTFRAMESRXOK ~ LAG7BROADCASTFRAMESRXOK (32-bit)	Link Aggregation Function Counter. aAggBroadcastFramesRxOK MIB Counter.	-
LAG0FRAMESDISCATDEDONRX ~ LAG7FRAMESDISCATDEDONRX (32-bit)	Link Aggregation Function Counter. aAggFramesDiscardedOnRx MIB Counter.	-
LAG0FRAMESWITHRXERRORS ~ LAG7FRAMESWITHRXERRORS (32-bit)	Link Aggregation Function Counter aAggFramesWithRxErrors MIB Counter.	-
LAG0UNKNOWNPROTOCOLFRAMES ~ LAG7UNKNOWNPROTOCOLFRAMES (32-bit)	Link Aggregation Function Counter aAggUnknownProtocolFrames MIB Counter	-

8.21. Link Aggregation

Link aggregation or trunking allows one or more physical links to be bundled together to form a single logical link. It is an economical and effortless implementation providing a high-speed link by multiple low-speed links in a device. Also the network performance is only lost, not completely stopped, even if one of the operational links fail. However, all physical links which enable link aggregation are always configured for full-duplex and operate at the same data rate.

The performance of link aggregation depends on the frame distribution function which chooses the link to be used for the transmission of outgoing packets. The RTL9054/RTL9068/RTL907x supports two modes of frame distributions to provide a wide variety of distribution and load balancing.

Hash Mode

A hash value is computed for each packet based on a programmable combination of specific packet fields and shifting bits. According to the value, the RTL9054/RTL9068/RTL907x picks the final egress port from all operational ports in a trunk group.

Here are the packet fields that can be used for hash arithmetic:

- Ingress port number
- MAC destination address
- MAC source address
- IP destination address
- IP source address
- L4 destination port
- L4 source port

Balance Mode

In this mode, the RTL9054/RTL9068/RTL907x filters specific packets and distributes them by round-robin to members in a trunk group. For a network with a single type application, it is a more efficient way to balance bandwidth with lower computations. Note that the packets not specified are distributed by the hash mode described above.

Here are the packet fields that can be specified for round-robin:

- Ether type
- L4 protocol
- L4 destination port

8.22. Under Voltage & Over Temperature

- The RTL9054/RTL9068/RTL907x is configurable to automatically deal with under voltage and over temperature events
- The RTL9054/RTL9068/RTL907xx supports VBAT/V33 detection, analog 3.3V, digital 3.3 V, digital 0.9V, and three individual RGMII/(R)MII power under voltages
- The under voltage level value is calibrated and is under voltage at approximately -7% ~ -10%. The Over Temperature Level is about 150°C. (The Under Voltage Level and Over Temperature Level is calibrated on a Formal chip)

The RTL9054/RTL9068/RTL907x offers over temperature detection. When the RTL9054/RTL9068/RTL907x is over temperature, it can automatically turn off transmit and receive packets and notify the external CPU, or only notify the external CPU.

Table 55. Under Voltage & Over Temperature

Interrupt Type	Description
Over temperature	The RTL9054/RTL9068/RTL907x turns off TX/RX when over temperature occurs, and turns back on TX/RX after it is back to normal (over temperature not occurring). The default value for over temperature detection of these domains is ON.
Under voltage: AVDD33/DVDD33/AVDD09/ DVDD09	When AVDD33/DVDD33/AVDD09/DVDD09 under voltage occurs, the RTL9054/RTL9068/RTL907x goes to sleep. The default value for under voltage detection of these domains is ON.
Under voltage: SGMII, HSGMII, USXGMII, PCI-E	If the power source to SGMII, HSGMII, USXGMII, PCI-E is sourced directly from the external regulator, when GMII, HSGMII, USXGMII, PCI-E under voltage occurs, the RTL9054/RTL9068/RTL907x goes to sleep. Otherwise, if the power source to RGMII/(R)MII is NOT sourced directly from the external regulator, when GMII, HSGMII, USXGMII, PCI-E under voltage occurs, the RTL9054/RTL9068/RTL907x turns off TX and RX for this port. The default value of under voltage detection of these domains is OFF.
Under voltage: RGMII/(R)MII	If the power source to RGMII/(R)MII is sourced directly from the external regulator, when RGMII/(R)MII, PCI-E under voltage occurs, the RTL9054/RTL9068/RTL907x goes to sleep. Otherwise, if the power source of RGMII/(R)MII is NOT sourced directly from the external regulator, when RGMII/(R)MII under voltage occurs, the RTL9054/RTL9068/RTL907x turns off TX and RX for this port. The default value of under voltage detection of these domains is OFF.

8.23. Operating Modes (OP)

8.23.1. Operating Modes

Figure 63 shows the transitions of the RTL9054/RTL9068/RTL907x's Global Operating Modes (OP). There are various modes in the RTL9054/RTL9068/RTL907x, including Power-Off, Sleep, Safety, Normal and Standby modes. Each operating mode has differences in power dissipation (refer to section 9.4) whether the availability of establishing the link and the MDIO command is accessible or not.

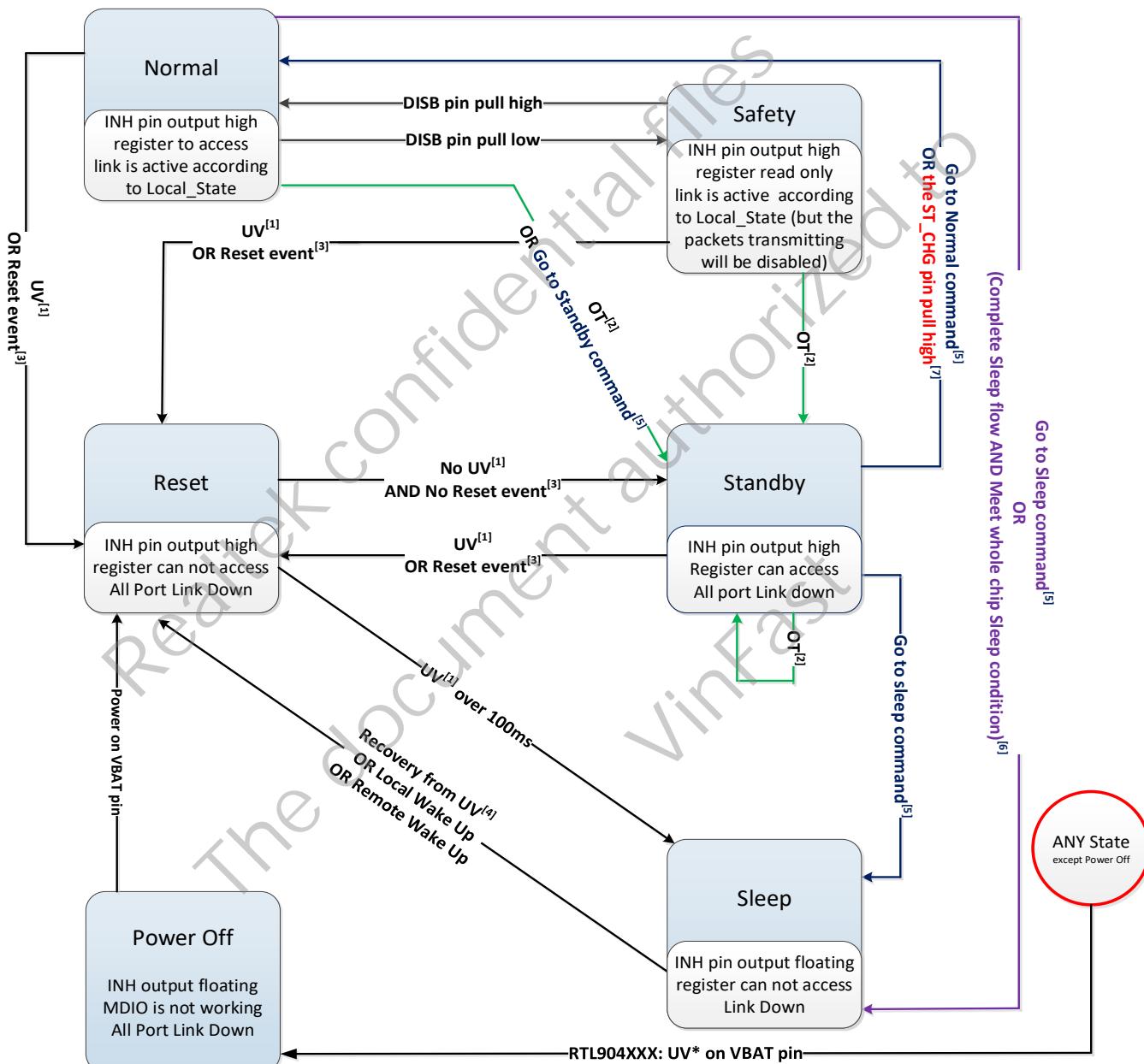


Figure 63. Operating Mode Transitions

*UV means under voltage.

[1] For the RTL9054/RTL9068/RTL907x, UV on one of the power supplies AVDD33_XXX, Px_VDDIO, AVDD09_XXX, DVDD09, or DVDD33.

[2] OT means over-temperature.

[3] Reset event means “Assert the RESETB pin low”, or “the MDIO reset command” (call API rtl906x_op_state_set with parameter OP_ST_RESET).

Note that when the MDIO reset command completes the Reset event, it will be self-cleared.

[4] Recovery from UV means Re-Power Up the under voltage power supply pin.

[5] The details of Go to Normal/Standby/Sleep command can refer to section 8.23.1 and API rtl906x_op_state_set.

[6] Complete Sleep Mechanism can refer to section 8.24.

[7] The value of ST_CHG is decided only during the hardware configuration procedure on Power On/Wake Up/assert RESETB to low by the external resister.

Power-Off Mode

The RTL9054/RTL9068/RTL907x remains in Power-off mode when the voltage on the VBAT/V33 pin is below the under voltage (UV) threshold. When in Power off mode, all functions of the RTL9054/RTL9068/RTL907x are disabled.

Sleep Mode

The RTL9054/RTL9068/RTL907x can be turned to Sleep mode for low power consumption by “Go to sleep command” (call API rtk_op_glob_cmd(OP_ST_WHOLE_CHIP_SLEEP)) or “Complete sleep flow AND meet whole chip sleep condition”. The UV events can also cause the RTL9054/RTL9068/RTL907x to enter Sleep mode. When the RTL9054/RTL9068/RTL907x is in Sleep mode, the data transmit and receive functions are disabled which means that the twisted-pair lines cannot transmit any signal. Also the transmit requests from non-100BASE-T1 MDI will be ignored. The MDIO read/write command cannot access the RTL9054/RTL9068/RTL907x in Sleep mode.

According to the method to supply AVDD33 power, there are two kinds of Sleep modes. The first one is the Deep Sleep mode that turns off the source for the AVDD33 power, and optimizes the system by having the VBAT/V33 pin permanently connected to the car battery for ultra-low power consumption; the other is Lite Sleep mode which is permanently the supply VBAT/V33 pin and AVDD33 power. The RTL9054/RTL9068/RTL907x supports both Deep Sleep mode and Lite Sleep mode.

There are two implementations for Deep Sleep mode. The first is the INH pin turns off the 3.3V external regulator of the AVDD33 and only the VBAT/V33 pin is powered by the car battery. The other is when the RTL9054/RTL9068/RTL907x is in Deep Sleep mode, the supply AVDD33 power is turned off, and power is supplied to the VBAT/V33 pin and main power separately. For the RTL9054/RTL9068/RTL907x, the INH pin will output floating in Sleep mode.

When the device is in Sleep mode, it can be woken up by a local wake up (assert the WAKE pin, see section 8.25.1) or remote wake up (receive Wake Up Pattern (WUP) from its link partner, see section 8.25.2). Note that when the supply power of the AVDD33 is recovered, the RTL9054/RTL9068/RTL907x will also be

woken up from Deep Sleep mode. When the RTL9054/RTL9068/RTL907x wakes up, the INH pin will output high and the RTL9054/RTL9068/RTL907x will switch to Normal mode (pull ST_CHG pin high, refer to section 6.25) or Standby mode (pull the ST_CHG pin low, refer to section 6.25).

Reset Mode

The RTL9054/RTL9068/RTL907x will enter Reset mode when the pull RESETB pin is low, or it receives an MDIO reset command (call API `rtl906x_op_state_set` with the parameter `OP_ST_RESET`). When the RTL9054/RTL9068/RTL907x is reset, it means all registers will be set to a default value except for the OP registers. Note that when the MDIO rest command completes the Reset event, it will be self-cleared. In Reset Mode, the link can no longer be established and the MDIO command will not have access.

Standby Mode

If the RTL9054/RTL9068/RTL907x is set to manual mode (pull the ST_CHG pin low, refer to section 6.25), when it powers-on/wakes up, it will remain in Standby mode. When the RTL9054/RTL9068/RTL907x is in Standby mode, the link cannot be established but the RTL9054/RTL9068/RTL907x can be accessed by an MDIO command. The User can also set a “Go to Normal /Sleep mode” command to allow the RTL9054/RTL9068/RTL907x to transit to other states. To do this, it can refer to API `rtl906x_op_state_set`. In addition, the OT event will allow the RTL9054/RTL9068/RTL907x to go from Normal or Safety mode to Standby mode.

Normal Mode

To establish a valid link with the link partner, the RTL9054/RTL9068/RTL907x must be operated in Normal mode. If the RTL9054/RTL9068/RTL907x is set to auto mode (pull the ST_CHG pin high, refer to section 6.25), it will transfer to Normal mode automatically and activate the link after power on/wake up.

Safety Mode

When the DISB pin is pulled low, the RTL9054/RTL9068/RTL907x will transfer from Normal mode to Safety mode. In Safety mode, the link is active but both of the packets transmitting and the MDIO write function will be disabled. That is to say, the RTL9054/RTL9068/RTL907x can be read only by the MDIO. The RTL9068/RTL907x enters Safety Mode in 18.2us after the DISB is pulled low. Due to the storage and forwarding architecture, packets are stored in a switch's packet buffer. It takes a while to empty them, hence, the total time is 18.2us + Packet empty time. The worst case is if the packet buffer is full and the link speed is 10Mbps of the switch (link speed for one of the used interfaces). The following table shows the maximum time DISB should be pulled low in order to empty packets.

Table 56 Time Required to Empty Packets when DISB is Activated

Link Speed	Time Required to Empty Packets
10Mbps	242ms
100Mbps	24.2ms
1000Mbps	2.42ms
5000Mbps	484us

Note: If the DISB is released before a packet buffer is empty, the malformed packet may be sent out of the switch. If the system has one interface which is operated at 10Mbps, the DISB should be pulled low to 18.2us + 242ms.

Table 57 presents an overview of the status of the RTL9068/RTL907x functional blocks in each operating mode.

Table 57. Overview of the Operating States

	Power-Off	Sleep	Reset	Standby	Normal	Safety
MDI Impedance	Open/High impedance	100ohm	100ohm	100ohm	100ohm	100ohm
Link Status	Passive	Passive	Passive	Passive	Active	Active
WUP Detection*	Off	On	On	On	Off	Off
OT Detection	Off	Off	Off	On	On	On
INH Pin Output	Floating (Pull low by external 1M-ohm)	Floating (Pull low by external 1M-ohm)	High	High	High	High
MDIO Command	Not accessible	Not accessible	Not accessible	▲ Read/Write in general condition ▲ Read only when DISB pin pulled low	Read/Write	Read only
Reset Registers	Yes	Yes	Yes	No	No	No

8.23.2. Operating Mode Transition

The following events, listed in order of priority, are trigger mode transitions:

1. **RTL9068/RTL907x:** Under voltage on VBAT pin
RTL9054: Under voltage on V33 pin
2. Under voltage on other Power pin
3. Reset event
4. OT event
5. Local wake up, Remote wake up
6. Go to Sleep/Normal/Standby command (refer to rtk_op_glob_cmd)
7. Hardware strapping pin (The ST_CHG pin, refer to section 6.25)

As an example, if the ST_CHG pin is high, and then gives a “Go to Standby Mode” command to the RTL9054/RTL9068/RTL907x, the RTL9054/RTL9068/RTL907x will go to Standby mode but will not go back to Normal mode automatically, as the “Go to Standby Mode” command was prior to the strap pin (pull the ST_CHG pin high).

OP Global State Goes to Sleep/Normal/Standby command (Refer to API rtk_op_glob_cmd):

The OP Global State Goes to Sleep/Normal/Standby command is cleared in the following conditions:

- The RTL9054/RTL9068/RTL907x goes to Sleep mode
- A UV event occurs in Normal/Safety mode
- A Reset event occurs in Normal/Safety mode
- An OT event occurs in Normal/Safety mode
- A Wake Up event occurs in any state
(refer to API rtl906x_op_port_wakeByRemoteWakeUpPulse_flag_get)

OP Local State Goes to Sleep/Normal/Standy command (Refer to API rtk_op_port_loc_cmd):

The OP Local State Goes to Sleep/Normal/Standy command is cleared in the following conditions:

- The RTL9054/RTL9068/RTL907x goes to Sleep mode
- UV event occurs in Normal/Safety mode
- Reset event occurs in Normal/Safety mode
- OT event occurs in Normal/Safety mode
- A Wake Up event occurs in any state
(refer to API rtl906x_op_port_wakeByRemoteWakeUpPulse_flag_get)

OP event flags:

The RTL9054/RTL9068/RTL907x supports UV / UV recovery / Wake up / Sleep / OT Power On flags, and these flags can refer to OP Control Register 3, OP Interrupt Status Register 1 and OP Interrupt Status Register. In order to ensure the next wake up event can be detected, note that lwake_flag and rwake_flag (in OP Interrupt Status Register) will be cleared if the following events happen:

- The RTL9054/RTL9068/RTL907x goes to Reset or Standby from Normal mode
- The RTL9054/RTL9068/RTL907x goes to Reset or Standby from Safety mode
- The RTL9054/RTL9068/RTL907x goes to Sleep mode from any state

In addition to Global State, there is another OP state called Local State. The following explains Global State (for whole chip) and Local State (for per-port):

Global State:

- Global Normal (Codenamed = 0x30, refer to API rtk_op_global_state_get)
All 100/1000BaseT1 ports can link-up and transmit packets. (according to Local State)
- Global Standby (Codenamed = 0x20, refer to API rtk_op_global_state_get)
All 100/1000BaseT1 ports cannot link-up and transmit packets
- Global Reset (Register cannot access)
Whole chip is reset, all 100/1000BaseT1 ports cannot link-up and transmit packets, the register cannot be accessed, but the INH pin stays high
- Global Sleep (Register cannot access)
Whole chip is Sleep, 100/1000BaseT1 ports cannot link-up and transmit packets, the register cannot be accessed and the INH pin is low (to turn off the external power source for power saving)

Local State:

- Local Normal (Codenamed = 0x30, refer to API rtk_op_local_status_get)
The 100 or 1000BaseT1 port can link-up and transmit packets
- Local Standby (Codenamed = 0x20, refer to API rtk_op_local_status_get)
The 100 or 1000BaseT1 port cannot link-up and transmit packets
- Local Sleep (Codenamed = 0x10, refer to API rtk_op_local_status_get)
The 100 or 1000BaseT1 port cannot link-up and transmit packets
(After a successful sleep handshake, the 100 or 1000BaseT1 port will go to this state.)

The relationship between Global and Local state:

- Global State is Global Normal
Per port Local State can be Local Normal / Local Standby / Local Sleep
- Global State is Global Standby
Per port Local State can only be Local Standby
- Global State is Global Reset or Sleep
Per port Local State can only be Local Sleep

Figure 64 is a simple example of OPFSM:

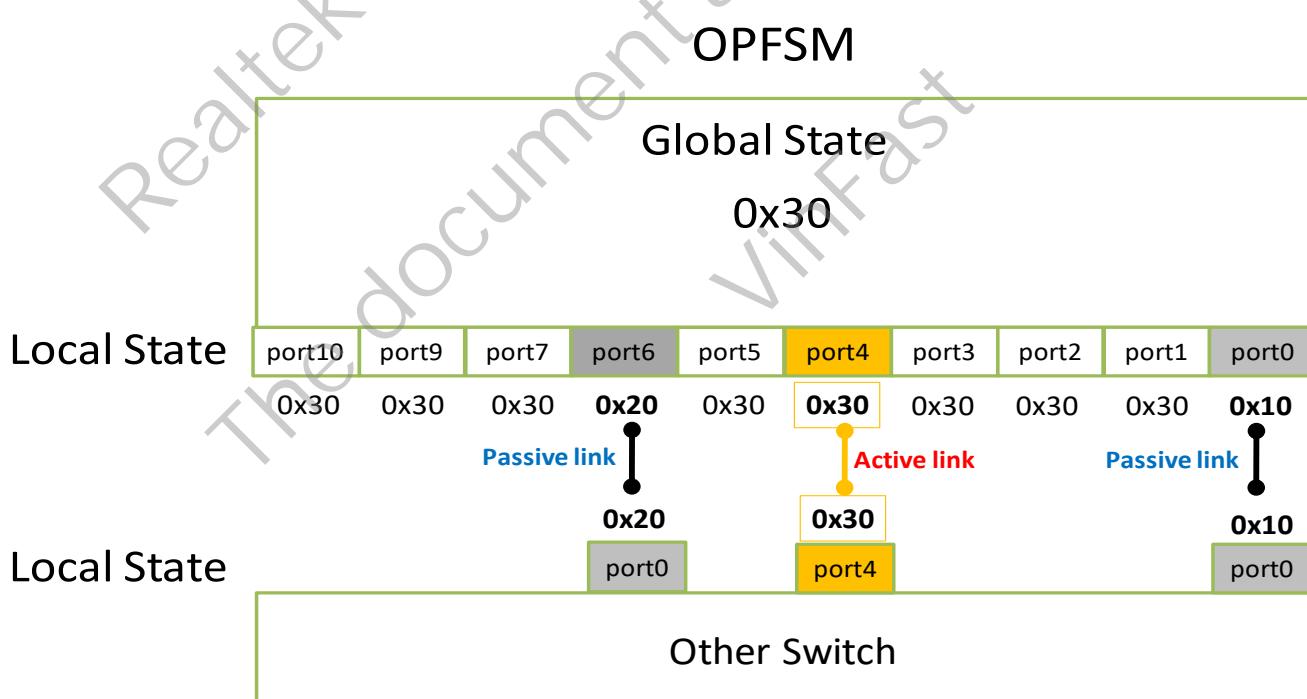


Figure 64. RTL9068/RTL907x OPFSM Example

8.24. Sleep Mechanism

The RTL9054/RTL9068/RTL907x supports OPEN Alliance TC10 Sleep/Wake-up function for automotive Ethernet. The Sleep function makes the RTL9054/RTL9068/RTL907x enter Sleep mode which has lower power consumption (refer to section 9.4).

When MAC gives a sleep request (refer to API `rtk_op_port_send_SleepRequest`) to the RTL9054/RTL9068/RTL907x (called Sleep Initiator), the RTL9054/RTL9068/RTL907x will start to do a sleep handshaking flow with its link partner (called Sleep Responder). Note that the sleep handshaking flow is available only when both sides (Sleep Initiator and Sleep Responder) are in Normal mode and their link is active. The sleep flow is successful if both PHYs finish sleep handshaking (transmitted and received sleep signal on the MDI) properly, and then both of them can enter Sleep mode together.

This sleep mechanism is able to reject sleep flow and deal with the sleep fail case as well. At the beginning of the sleep flow, the Sleep Initiator transmits the sleep signal to the Sleep Responder. The Sleep Responder will indicate its upper layer (namely MAC) through pulling the INTB pin low. If the MAC does not want the Sleep Responder to enter Sleep mode because of a unfinished transmission, the MAC can continuously set `stop_sleep` to 1 for 16ms, but the interval for each `stop_sleep` command must not exceed 8ms. Then the Sleep handshaking flow will be rejected and both the Sleep Initiator and Sleep Responder will stay in Normal mode, and the link between them will remain active. If the link between the Sleep Initiator and Sleep Responder are accidentally interrupted while the sleep flow handshaking is in progress, the sleep flow will fail and both the Sleep Initiator and Sleep Responder will stay in Normal mode.

The RTL9054/RTL9068/RTL907x supports TC10 Sleep flow. Sleep flow is an OPEN Sleep/Wake-up function for Automotive Ethernet. It supports a controlled link shutdown and a fast global wake-up within an Ethernet network. The sleep flow is completed only if both switch ports support this feature and finish Sleep handshaking (transmitted and received sleep request signal) properly. Then the switch port will enter local sleep state. After the switch port enters local sleep mode, it can be woken up by detecting a ‘Local wake-up’ (Lwake refer to 8.25.1) event on the WAKE pin, or by detecting a ‘Remote wake-up’(Refer to 8.25.2) (Rwake) on the MDI. Also, the switch port has the ability to reject the Sleep request from a link partner and stay in Normal operation mode. (refer to API `rtk_op_AccpetSleepRequest_cap_set`)

The RTL9054/RTL9068/RTL907x also supports the sleep forward function. When a port receives a sleep request from its link partner, the RTL9054/RTL9068/RTL907x can also trigger the other port to forward this sleep request. For example, when port0 receives a sleep request from a link partner, the RTL9054/RTL9068/RTL907x can send a sleep request to port1 and port2 and trigger another sleep handshake by configuration. (refer to API `rtk_op_Txsleepportmsk_set`)

Figure 65 is a simple example of Sleep function:

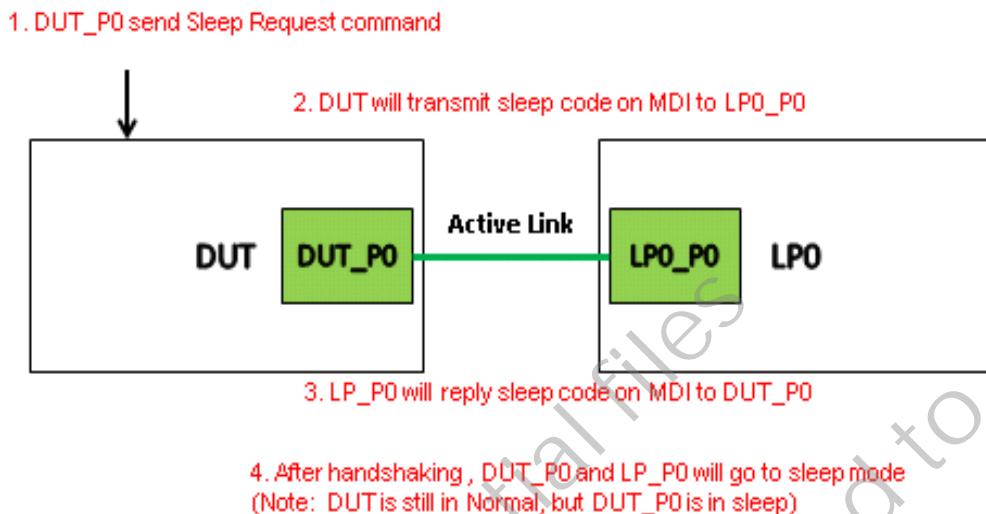


Figure 65. Sleep Mechanism

Description:

- DUT shall be connected to an active link partner (LP0) with opposite MASTER/SLAVE configuration
- A stable link-up condition shall be present the moment the test is started

Start:

1. DUT_P0 and LP_P0 are in Normal mode, the MDI link between them is active.
2. Set up some initialization to DUT and LP, then DUT sends a sleep handshaking command to LP.

End:

3. After Sleep handshaking, both port0 of DUT and port0 of LP will enter local_sleep mode.

Note: Switch is still in Normal mode while port0 of DUT can go to local_sleep mode.

8.25. Wake-Up

8.25.1. Local Wake-Up

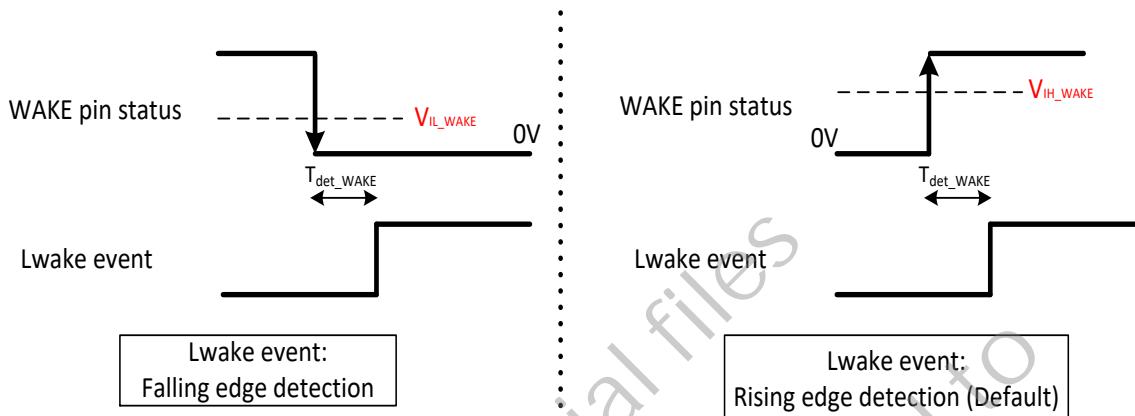


Figure 66. RTL9054/RTL9068/RTL907X Local Wake Up (Lwake) Event Detection

When the RTL9054/RTL9068/RTL907x is in Sleep mode, it can be woken up by detecting a local wake pulse on the WAKE pin. There are two methods of detection for a local wake up event (Lwake event), one is rising edge detection; and the other is falling edge detection. The rising/falling edge detection can be configured by setting the specified register (API `rtl906x_op_lwakeEdgeSel_set`). Note that the default is set as rising edge detection.

As shown in Figure 66, in the RTL9054/RTL9068/RTL907x, if Rising Edge Detection is chosen, the RTL9054/RTL9068/RTL907x detects a Lwake event when the voltage on the WAKE pin is higher than the detective high-level voltage V_{IH_WAKE} (rising edge on the WAKE pin) for longer than detective time T_{det_WAKE} . If Falling Edge Detection is chosen, the RTL9054/RTL9068/RTL907x detects a Lwake event when the voltage on the WAKE pin is lower than the detective low-level voltage V_{IL_WAKE} (falling edge on the WAKE pin) for longer than the detective time T_{det_WAKE} .

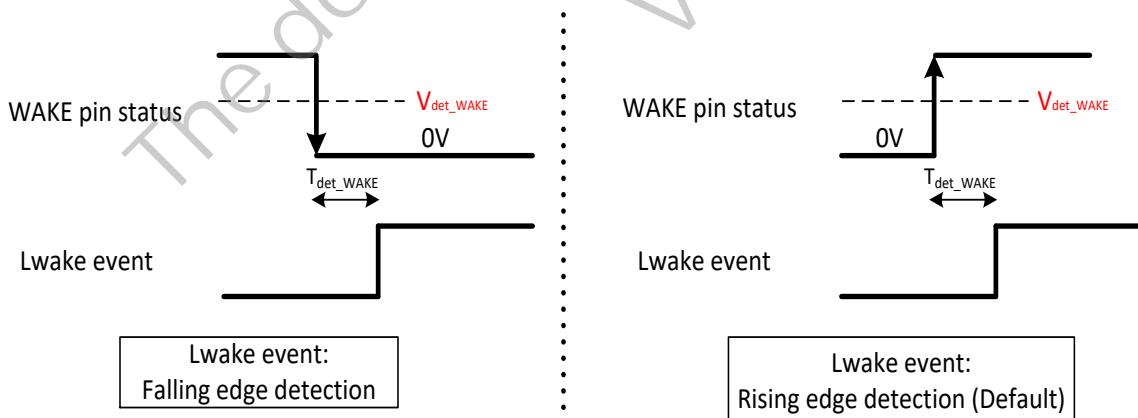


Figure 67. RTL9054/RTL9068/RTL907x Local Wake Up (Lwake) Event Detection

8.25.2. Remote Wake-Up

The RTL9054/RTL9068/RTL907x detects a ‘Remote wake-up’ (Rwake) event when it detects a WUP on the MDI pins. In the application of RTL9068/RTL907x’s Deep Sleep mode, after detecting a WUP on the MDI pins, the INH pin rises and then turns on the external regulator. Thus, the whole chip is powered on by the 3.3V output from the external regulator. In the application of Lite Sleep mode in both the RTL9068 and RTL907x, after detecting a WUP on the MDI pins, the functions which are disabled in Sleep mode will recover.

If the RTL9054/RTL9068/RTL907x is in Standby mode and wants to remote wake up its link partner which in the Sleep mode, setting call API rtk_op_disable_rwake_set will make the RTL9054/RTL9068/RTL907x remote wake-up its link partner.

When Local_State is in Local_Normal mode and the link has been established, setting call API rtk_op_disable_rwake_set will make the RTL9054/RTL9068/RTL907x send WUR to its link partner. When Local_state is in Local_Sleep mode (Passive mode), setting call API rtk_op_disable_rwake_set will make the RTL9054/RTL9068/RTL907x send a WUP to its link partner.

The RTL9054/RTL9068/RTL907x supports Wake Forward (refer to rtk_op_rwake_forward_pcfg_set). When the RTL9054/RTL9068/RTL907x receives a WUP or WUR, it can decide which port should be woken or forwarded.

The following is a simple example of a Wake_forward:

WAKE Px Configuration

For each port , it has its own configuration call wake_px, in this case when port0 receive WUP or WUR , it would forward wake to port2 and port4.

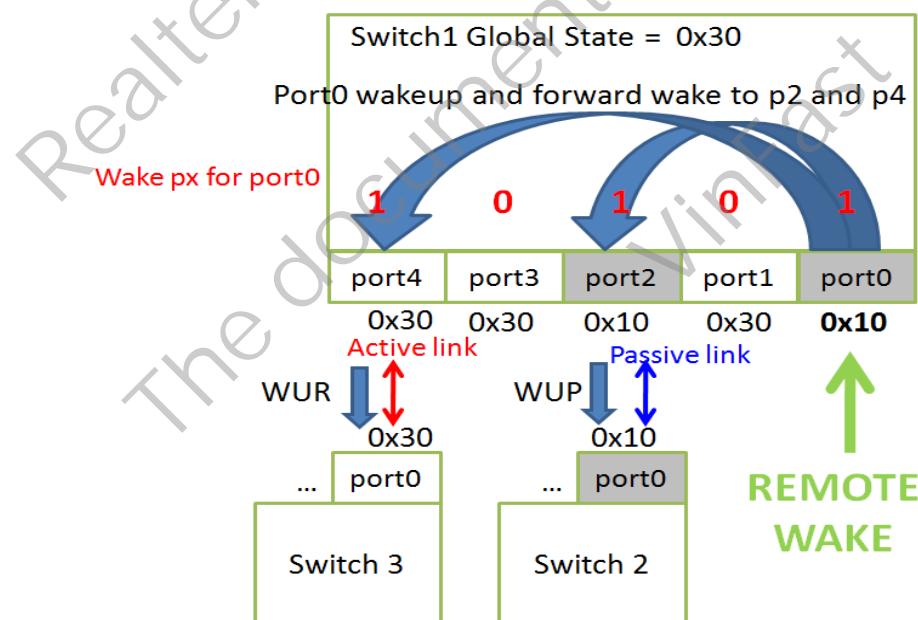


Figure 68. RTL9054/RTL9068/RTL907x Wake Px Example

8.26. Partial Network

Partial Network helps reduce power dissipation by turning off unused elements. This idea is applied by automotive networks such as CAN. The under layer implementation of the automotive Ethernet is defined at OPEN alliance TC10.

TC10 defines not only how two devices go to sleep and remote wake up, but also defines forwarding remote wake signals in the intranet. The upper layer has the same system level set-up ability of sleep and wake. The hardware obeys user configurations to accept or reject sleep and wake events and to notify the upper layer if needed. The under layer implementations (sleep and wake) of the RTL9054/RTL9068/RTL907x comply with OPEN Sleep/Wake-up Specification version 1.0.

All you need to do is enable sleep and wake capability through APIs (or enable them as default configurations) and how you want to forward a wake-up signal.

There are simple steps to enter into Sleep mode. The first one is “Accept Sleep request”. When a Sleep request is received, the RTL9054/RTL9068/RTL907x can notify the upper layer, and then (or not) wait for the upper layer to grant it Sleep mode (or automatic). It’s also convenient to host a sleep request by setting call API rtk_op_port_send_SleepRequest and then checking if it has entered Sleep mode by setting call rtk_op_local_status_get.

The partial network of CAN defines selective wake up. Another method is to “wake up all”, and then only sleep unused parts while the system resumes. The RTL9054/RTL9068/RTL907x supports two wake-up concepts in the automotive Ethernet. There are hardware pins and registers to configure which ports are sending a wake-up pattern. If the system cannot decide which ports to wake up the next time, it is useful to have this design. APIs are responsible for configuring this. For more information, please refer to rtk_op_rwake_forward_pxcfg_set functions.

The RTL9054/RTL9068/RTL907x supports forward local wake to remote wake. After the RTL9054/RTL9068/RTL907x resumes from Sleep via Local wake-up line, it wakes up all/selective wake ports and sends a wake-up signal. The related function request is rtk_op_lwake_to_rwake_set.

Figure 69 illustrates the partial network use case. There are two domains in this system. ECU1, ECU3, and ECU5 are the members of domain 1, while ECU2, ECU4, and ECU5 are the members of domain 2. ECU5 is a cross domain ECU. ECU7 controls whole system power state.

The RTL9054/RTL9068/RTL907x provides I2C, SPI, and MDC/MDIO as the register accessing interface. For exchanging data between the RTL9054/RTL9068/RTL907x and ECU7/SoC, use either RGMII, (R)MII, or PCI-E/HISGMII/SGMII. The WAKE pin provides a local wake feature (see section 8.25.1, page 152). The INH pin goes low while the RTL9054/RTL9068/RTL907x enters Sleep mode. After car ignition, the whole system is powered and functions normally. All interfaces are active as user pre-defined.

If ECU1 ~ ECU5 are not in operation, ECU7 issues a sleep mechanism to all ECUs. After all ECUs enter sleep mode, ECU7 uses the register accessing interface to issue a ‘Go-to-sleep’ command to the RTL9054/RTL9068/RTL907x and then the RTL9068/RTL907 turns off the external SWR/LDO via the INH pin when it enters Sleep state.

The RTL9054/RTL9068/RTL907x provides remote wake and local wake (WAKE pin). ECU7 uses the WAKE pin to wake up the RTL9054/RTL9068/RTL907x. ECU1~ECU5 use Remote Wake to wake up the RTL9054/RTL9068/RTL907x. For example, ECU1 is a keyless system, and when a keyless module detects a signal, it powers on ECU1. ECU1 sends a WUP to the RTL9054/RTL9068/RTL907x. The remote wake event passes to ECU7 via an interrupt pin if needed. The RTL9054/RTL9068/RTL907x sends a WUP to domain 1 nodes (ECU3 and ECU5) and wakes up the ECUs that can be pre-configured by strapping pins (GPIOC [5:0], GPIOF [3:0]) or OP configurations in the flash.

ECU7 also wakes up the RTL9054/RTL9068/RTL907x via a local wake pin if needed.

The RTL9054/RTL9068/RTL907x supports local wake to remote wake. When the RTL9054/RTL9068/RTL907x boots up from Sleep state by local-wake up, it sends WUPs to 100BASE-T1 ports whose strapping pins are set to On.

GPIOC[5:0]/GPIOF[3:0] could be weak pull high/low on the PCB or direct pull high/low via ECU. The ECU must pull the correct voltage for the RTL9054/RTL9068/RTL907x before the RTL9054/RTL9068/RTL907x determines the settings of the strapping pins (refer to section 6.25).

For example, if GPIOC[0] and GPIOC[1] hardware strapping values are set high while GPIOC[2], GPIOC[3], GPIOC[4], and GPIOC[5] hardware strapping values are set low, when the RTL9054/RTL9068/RTL907x boots up from Sleep state, the RTL9054/RTL9068/RTL907x sends a WUP to port0 and port1, but does not send a WUP to port2, port3 or port4.

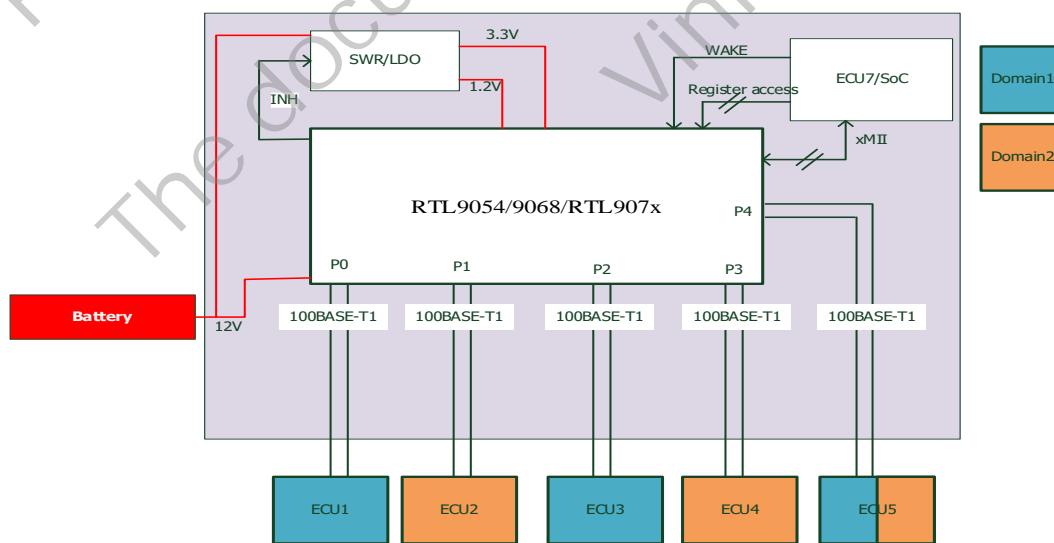


Figure 69. System Topology

Figure 70 shows a scenario when powering off some nodes in order to save power. The red line represents powered nodes. When ECU1 wants to wake up all domain 1 nodes, it sends a wake up request to the RTL9054/RTL9068/RTL907x. Then the RTL9054/RTL9068/RTL907x sends a WUR to ECU3 and a WUP to ECU5 as user pre-configured. Then, the whole system wakes up.

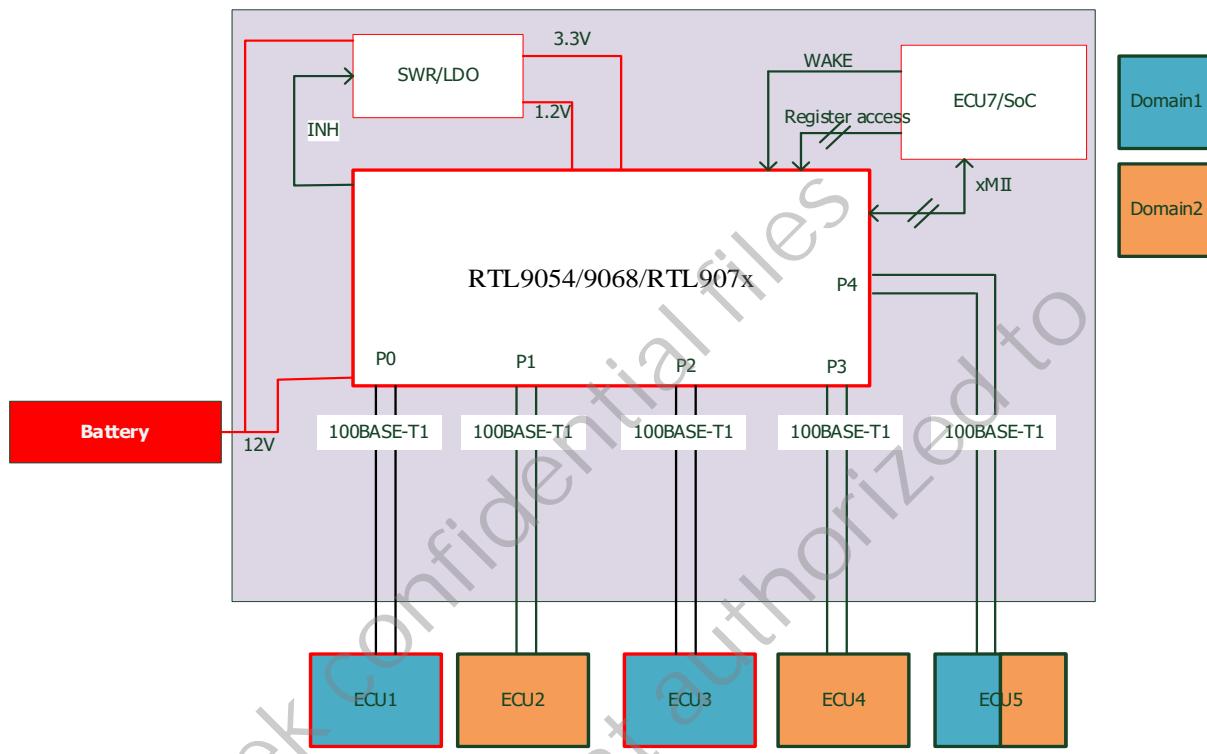


Figure 70. The System Status for Partial Network

8.26.1. Sleep Parameter and Use Case

AcceptSleepCmdMsk:

This sets whether each port should respond or reject a Sleep request from LP.

AcceptSleepCmdMsk is a port mask that decides if a port should accept a Sleep request or reject it whenever a port receives a Sleep request from its link partner.

- If the target port's AcceptSleepCmdMsk = 1, it means this port can accept a Sleep request from other devices. Furthermore, if the port receives a Sleep request and a handshake is done successfully, this port goes into Sleep mode
- If the target port's AcceptSleepCmdMsk = 0, it means this port will reject any Sleep request from another device

Figure 71 is a simple example of AcceptSleepCmdMsk:

AcceptSleepCmdMsk example

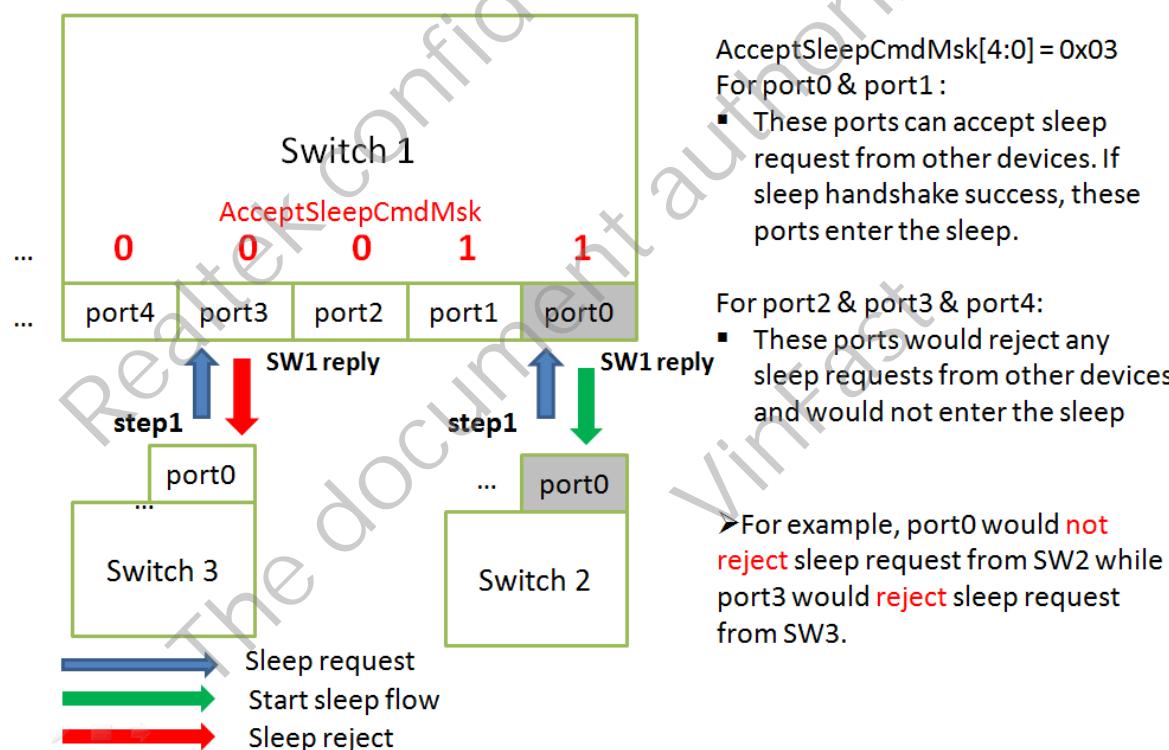


Figure 71. RTL9054/9068/RTL907x Example of AcceptSleepCmdMsk

TXSleepPortMsk:

This parameter sets which port will forward a Sleep request.

TXSleepPortMsk is a port mask that decides whether the received sleep request should be forwarded to the other port or not.

When any of the RTL9054/RTL9068/RTL907x's ports receive a sleep request:

1. Whether a certain port's AcceptSleepCmdMsk is set to either 0 or 1, the RTL9054/RTL9068/RTL907x (switch) will still forward the sleep request if those ports TXSleepPortMsk is set to 1.
2. The port that receives the sleep request does NOT send the sleep request again.
(For example, when Port3 receives a sleep request, Port3 will not send a sleep request even if port3's TXSleepPortMsk is set to 1.)

Figure 72 is a simple example of TXSleepPortMsk:

TXSleepPortMsk example

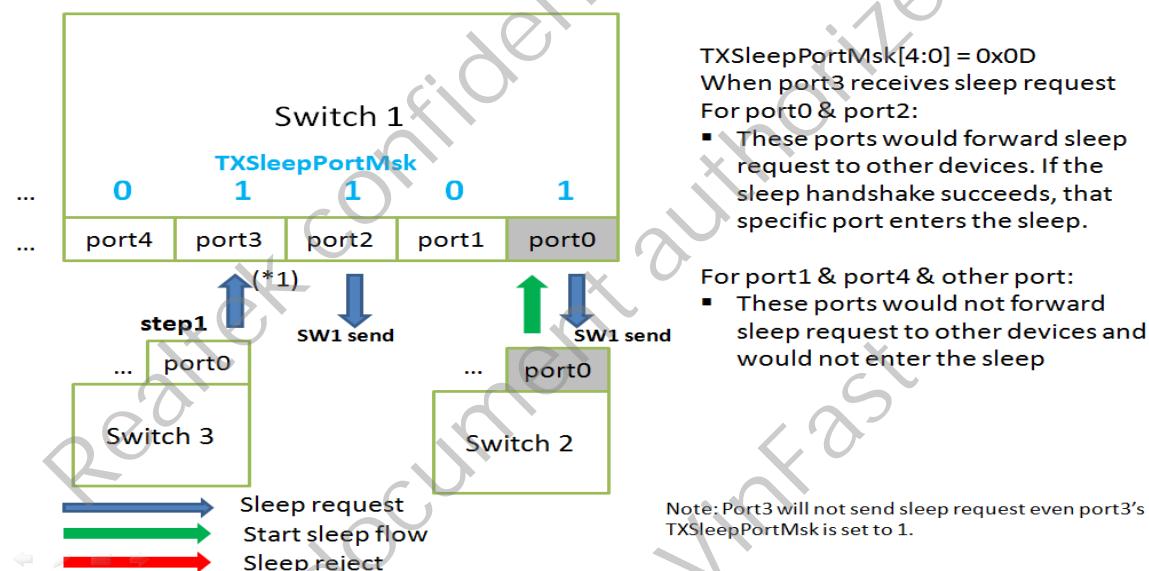


Figure 72. RTL9054/9068/RTL907x Example of TXSleepPortMsk

For 2 port parameters, there are 4 cases as shown below:

Case1: TXSleepPortMsk = 0, AcceptSleepCmdMsk = 0

- This port will reject any Sleep request from another device
- This port does not forward a Sleep request when any of the switch's ports receive a Sleep request

Case2: TXSleepPortMsk = 0, AcceptSleepCmdMsk = 1

- This port will not reject any Sleep request from another device
- This port forwards a Sleep request when any of the switch's ports receive a Sleep request

Case3: TXSleepPortMsk = 1, AcceptSleepCmdMsk = 0

- This port will reject any Sleep request from another device
- This port forwards a Sleep request when any of the switch's ports receive a Sleep request

Case4: TXSleepPortMsk = 1, AcceptSleepCmdMsk = 1

- This port will not reject any Sleep request from another device
- This port forwards a Sleep request when any of the switch's ports receive a Sleep request

WholeChipSleepMask and WholeChipSleepEnable

- WholeChipSleepEnable is a bit which enables the whole chip Sleep function
- WholeChipSleepMask is a port mask that decides whether a chip should be given WHOLE_CHIP_SLEEP or not

When any of the RTL9054/RTL9068/RTL907x's PHYs receive a sleep request, and after a sleep handshake is finished, the RTL9075 will check the WholeChipSleepMask to see if the Mask (The whole chip sleep criteria) has contacted all the sleeping ports. If the WholeChipSleepMask has contacted all the sleeping ports, the RTL9075 enters Whole Chip Sleep.

Figures 73 ~ 75 are simple examples of a WholeChipSleepMask:

WholeChipSleep example flow 1

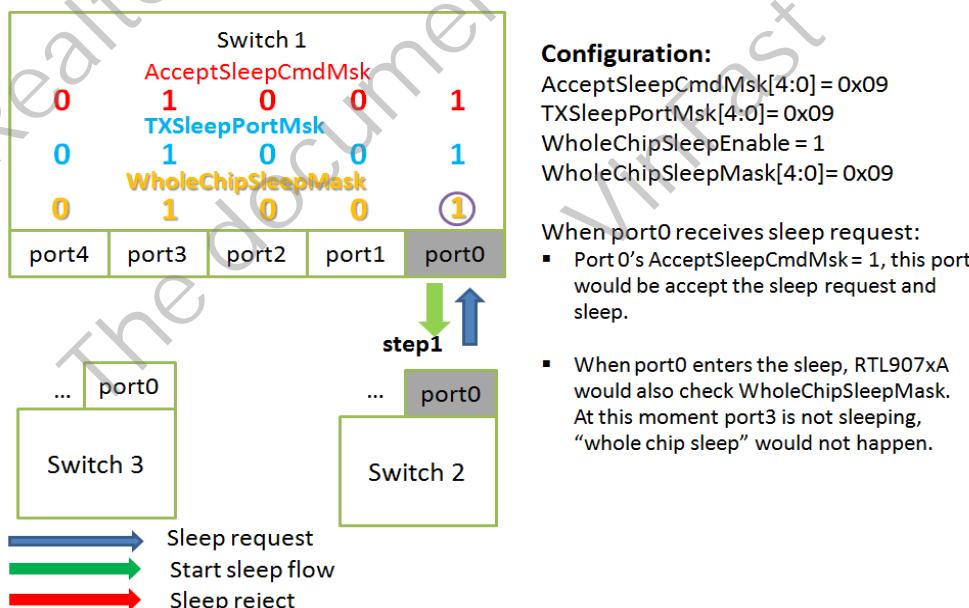


Figure 73. RTL9054/9068/RTL907x Example of WholeChipSleepMask Flow 1

WholeChipSleep example flow 2

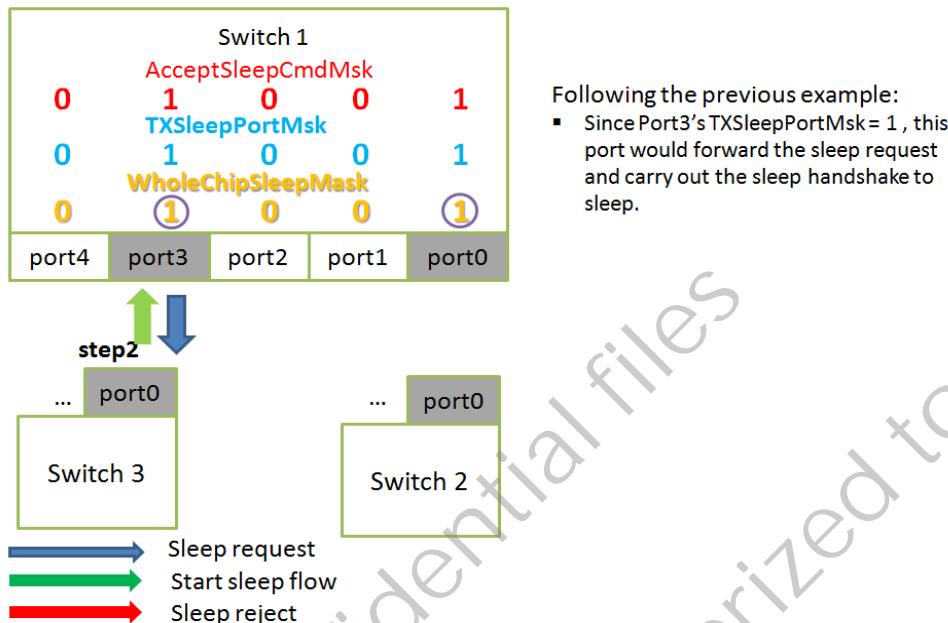


Figure 74. RTL9054/9068/RTL907x Example of WholeChipSleepMask Flow 2

WholeChipSleep example flow 3

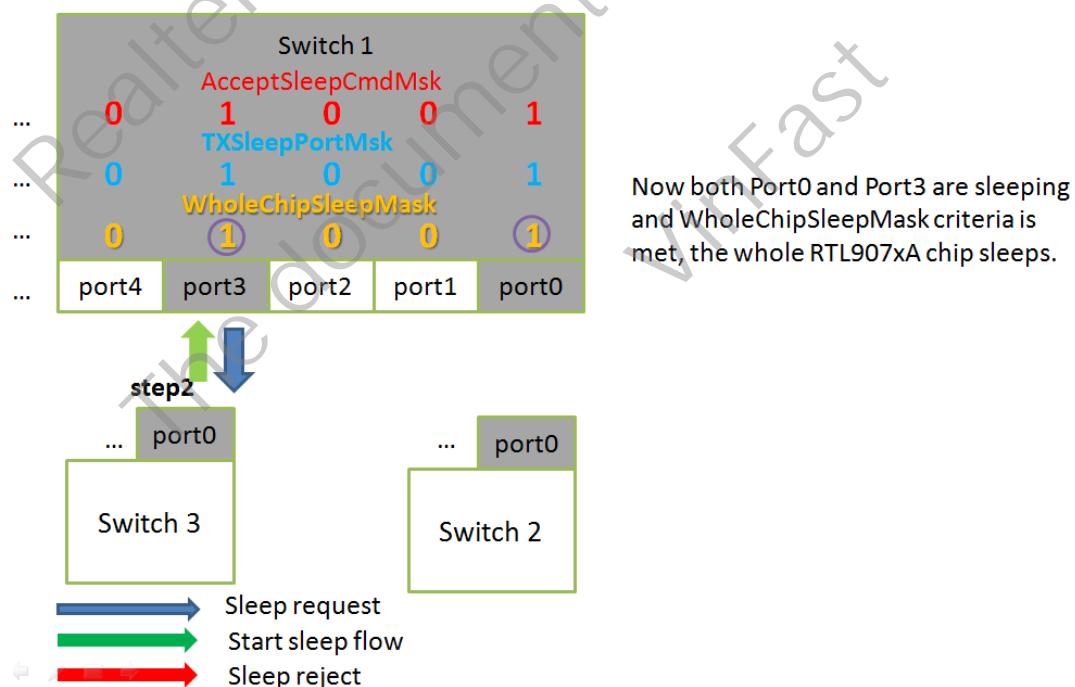


Figure 75. RTL9054/9068/RTL907X Example of WholeChipSleepMask Flow 3

8.27. Realtek Cable Test Diagnostics (RTCT)

Realtek Cable Test Diagnostics (RTCT) is a function to figure out whether the cable is open, short, or normal.

The figure below shows the setup flow of the RTCT Configuration and a detailed description is shown in the following sub section with the corresponding steps.

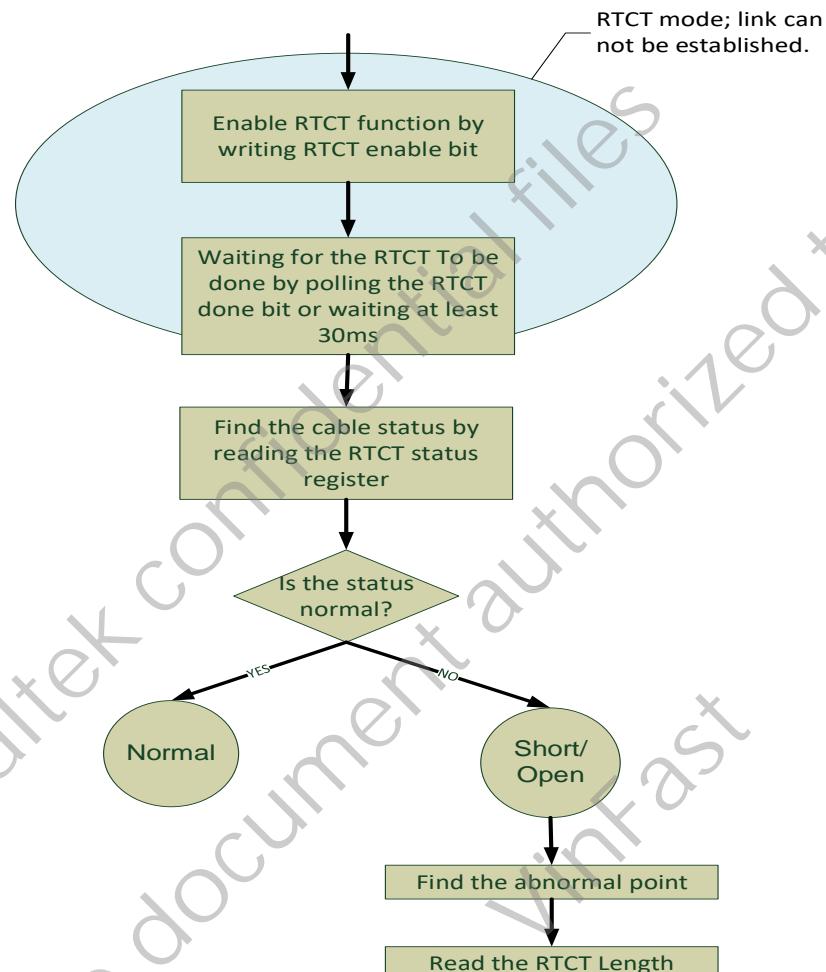


Figure 76. RTCT Steps Flow

The RTCT function is enabled by setting the register and making the PHY enter RTCT mode. Note that once RTCT is enabled, the link cannot be established in this mode.

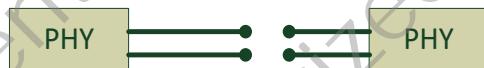
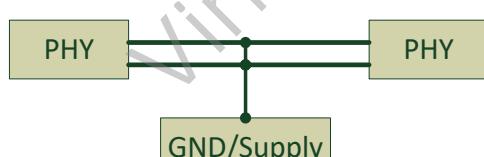
Step1: Wait until the RTCT is done - 5ms for 1000BASE-T1/100BASE-T1 ports

Polling the register until the RTCT_done field is 1. If a value of '1' is returned, it means the RTCT test is finished. If a value of '0' is returned, the test is still running. Note that the test will be done in 5ms.

Step2: Result is shown by the register

Read the RTCT status register and it will provide the cable status. The status can be mapped using the table below to indicate whether the cable status is in Normal Operation, Cable Open, or Cable Short. If the result is not Normal Operation, the next step can indicate the abnormal point.

Table 58. RTCT Cable Status Indication

Cable Status	Register Value (in Hex)	Description
Normal	0x60XX	<p>The cable is indicated to be normal in the following situation:</p> <p>In Normal operation</p> 
Open	0x48XX	<p>The cable is indicated to be open in the following situations:</p> <p>Both of the wires are Open</p>  <p>One of the wires is Open</p> 
Short	0x50XX	<p>The cable is indicated to be short in the following situations:</p> <p>The wires are Short</p>  <p>Both of the wires are Short to GND or Supply</p> 

Step3: Find the abnormal point

Read the RTCT Length Register. By transforming the returned hexadecimal value into the decimal value, and then dividing by 7.5 in 1000BaseT1 port or 80 in 100BaseT1 port, the calculated result indicates the distance from the chip side to the defect point of the cable in meters with resolution +/-1m.

8.28. Signal Quality Indexes (SQI)

The RTL9054/RTL9068/RTL907x provides two signal quality indexes (SQI) which indicate the real-time MDI signal quality information from 1000BASE-T1 PHY or 100BASE-T1 PHY. These indexes are listed as follows:

8.28.1. Signal Quality Index (SNR)

The signal quality index is determined by signal to noise ratio (SNR), and the range is from levels 0 to 7. The higher the SNR value, the greater the performance of the communication system. The following table is the mapping of the SQI index and SNR values. The SQI will be zero if the link is not established.

For 1000BASE-T1 PHY:

Table 59. SQI Classification for 1000BASE-T1 Ports

SQI Value	snr_o value
0	0x0616 < snr_o
1	0x04d6 < snr_o = < 0x0616
2	0x03d7 < snr_o = < 0x04d6
3	0x030d < snr_o = < 0x03d7
4	0x026c < snr_o = < 0x030d
5	0x01ed < snr_o = < 0x026c
6	0x0187 < snr_o = < 0x01ed
7	snr_o = < 0x0187

For 100BASE-T1 PHY:

Table 60. SQI Classification for 100BASE-T1 Ports

SQI Value	snr_o value
0	0x0f00 < snr_o
1	0x0c00 < snr_o = < 0x0f00
2	0x09b0 < snr_o = < 0x0c00
3	0x07b0 < snr_o = < 0x09b0
4	0x0610 < snr_o = < 0x07b0
5	0x04d0 < snr_o = < 0x0610
6	0x03d0 < snr_o = < 0x04d0
7	snr_o = < 0x03d0

8.28.2. Mean Square Error

Mean Square Error (MSE) of the slicer measures the average of the squares of the errors. The higher the signal-to-noise ratio (SNR), the lower the MSE. MSE worst case can also be obtained since the last read. MSE is defined as valid only under link status.

8.29. Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN)

Time-Sensitive Networking (TSN) is the latest IEEE 802.1 standard which extends the Audio Video Bridge (AVB). The RTL9054/RTL9068/RTL907x supports the following features:

8.29.1. Precision Time Protocol

The RTL9054/RTL9068/RTL907x supports both IEEE 802.1 AS-rev and IEEE 1588 v2. Precision Time Protocol (PTP) is a protocol used to synchronize time information across a local network with precision in less than 1 micro-second. The RTL9054/RTL9068/RTL907x acts as an ordinary clock within multi-ports and uses layer 2 communication methods to exchange time synchronized messages. The RTL9054/RTL9068/RTL907x is based on the IEEE802.1AS-rev and supports 1-Step time sync (From IEEE1588, Sync/Follow-up). When it operates in Grandmaster mode, the RTL9054/RTL9068/RTL907x sends Sync/Follow-up to reconfigured ports. When it works as a transparent clock (TC, PTP relay), it synchronizes time from preconfigured slave ports and forwards the sync/follow-up with correctionFiled updates to master ports.

The IEEE 1588 defines PTP protocol to synchronize time using the IEEE 802.3 Ethernet, but the protocol is generic and is not limited to the Ethernet. The protocol defines the mechanism to synchronize time by exchanging the PTP message and the message format. The IEEE 802.1AS defines specific behavior to ensure the interoperation compatibility of time sensitive applications. The IEEE 802.1AS references mechanisms and message formats from the IEEE 1588, and extends the network interface to include more transmission mediums. Both standards are used to synchronize time throughout the network.

The PTP is a master/slave architecture. Each port has a specific port state, which is either master, slave, or disabled. The time source is called the grandmaster, an all port state in master state. There is only one grandmaster in a PTP domain, and the other devices connected to the network will have a slave port and multiple master ports. The port in master state is responsible to send the time information. The port in slave state will receive time information from a port in master state, and synchronize the time. The best master clock algorithm is not executed; and the grandmaster and port state are configured statically to minimize the ready to work time after boot up.

Time synchronization is done by exchanging a PTP message to distribute the synchronized time, to measure network latency, and to compute the clock rate ratio. The synchronized time is carried by a sync message; and the target is to distribute time information to all PTP devices in the same domain from grandmaster to each slave. The network latency is measured by a pdelay request and a pdelay response, and the target is to compensate the propagation time of the message. The rate ratio is computed by the elapsed interval between the master port and slave port, and the target is to compensate the time drift caused by the different clock frequencies.

The IEEE 802.1AS revision extends its functionality to support multiple PTP instances. The primary objective is for a PTP device with multiple PTP instances to synchronize time between different time sources independently. This enables more applications to be possible. For example, it helps integrate new deployed modules into existing systems, or can be used as redundant clock.

The RTL9054/RTL9068/RTL907x supports up to 3 PTP instances, and each instance can be enabled/disabled independently. When enabled, operation mode is configurable between IEEE 802.1AS gPTP mode, and IEEE 1588 transparent clock. When operating in gPTP mode, the RTL9054/RTL9068/RTL907x supports configurable alternative behavior defined in the Avnu automotive profile.

The RTL9054/RTL9068/RTL907x supports full function with built-in hardware and firmware, including 1-step/2-step PTP Sync message and 1-step/2-step pdelay response. The RTL9054/RTL9068/RTL907x can complete time synchronization independently without an external controller.

Once time synchronization is stable, there are several ways to use the time information such as: read time information directly through a management interface (read registers), use the time with a GPIO, use as common time for other TSN modules.

A time application interface in the RTL9054/RTL9068/RTL907x allows an external device to utilize time information using a GPIO. There are four modes in the time application interface. The first configures the GPIO to generate output at the target time. The output can be configured to be rising/falling edge, a pulse with a specific width, or a periodic pulse with a configured period and width. The second monitors the input, and timestamps the input event. The input event can be configured to be rising/falling edge. The third preloads the time information on a data register, and monitors the input. The time information on the register will be latched when an input event is detected. The input event can be configured to be rising/falling edge. For the RTL9054/RTL9068/RTL907x, this minimizes the latency to configure time when used as a grandmaster. The fourth references clock input (square waveform), and the PTP module will synchronize with the clock automatically. This is similar when using the input clock as the clock of a PTP module. The common time information for other TSN modules is configurable and can be selected from any one of the PTP instances.

A possible use case is to integrate existing systems and new systems and use as redundant clock.

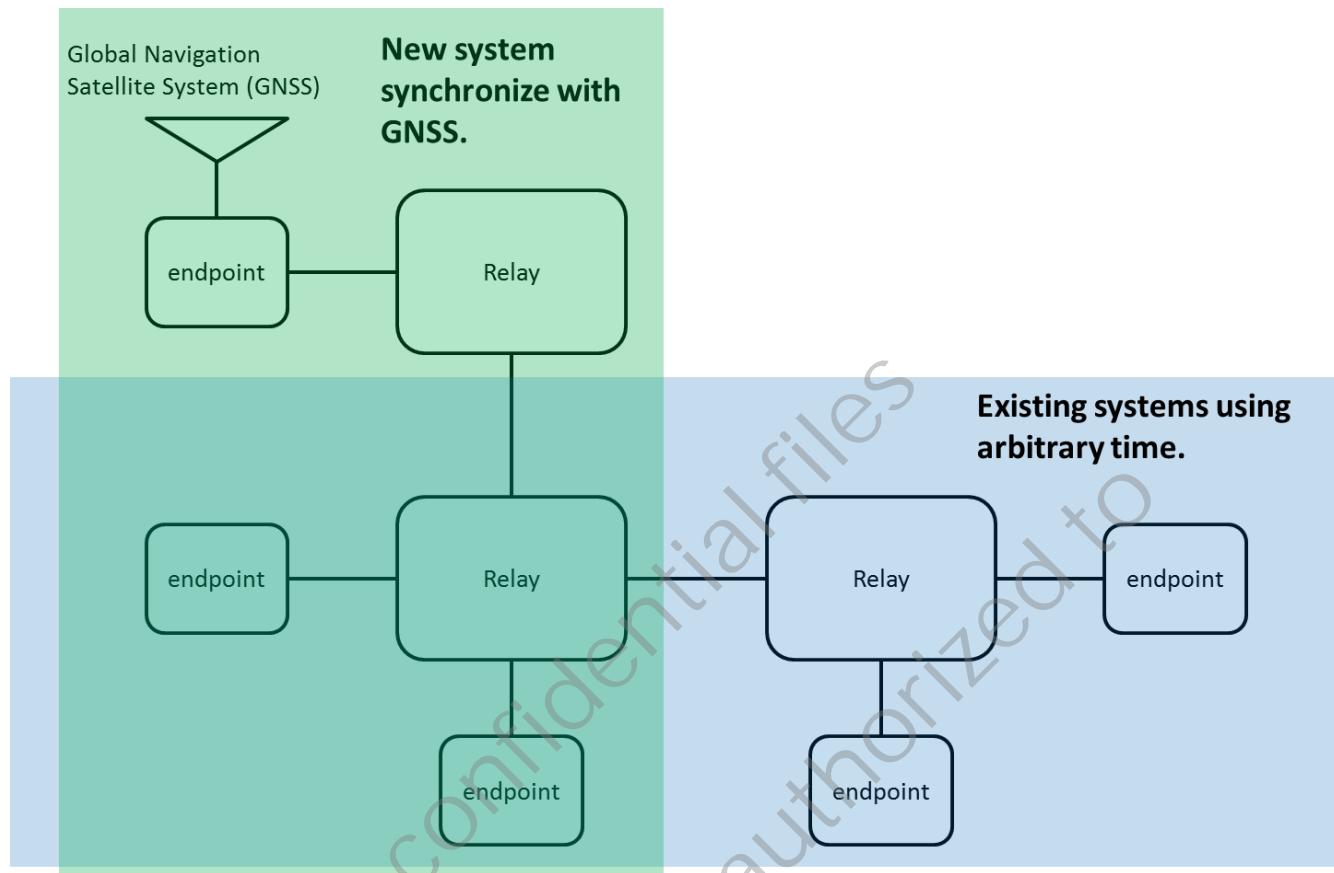


Figure 77. Multiple Independent Clocks

Figure 77 shows an example of multiple independent clocks. The relay and endpoint in the blue block is the existing system, which uses arbitrary time as its reference time. The arbitrary time could be up time since engine start. This is the general case if systems just want to synchronize to the same reference time, but the relation to the time in the real world is not important. As time passes, a new system emerges, but the system needs to link the time to the real world, which is covered in the green block. With multiple PTP instances, these two systems can be integrated together with minimum effort by using one PTP instance for each time domain (the blue/green blocks).

Use as Redundant Clock

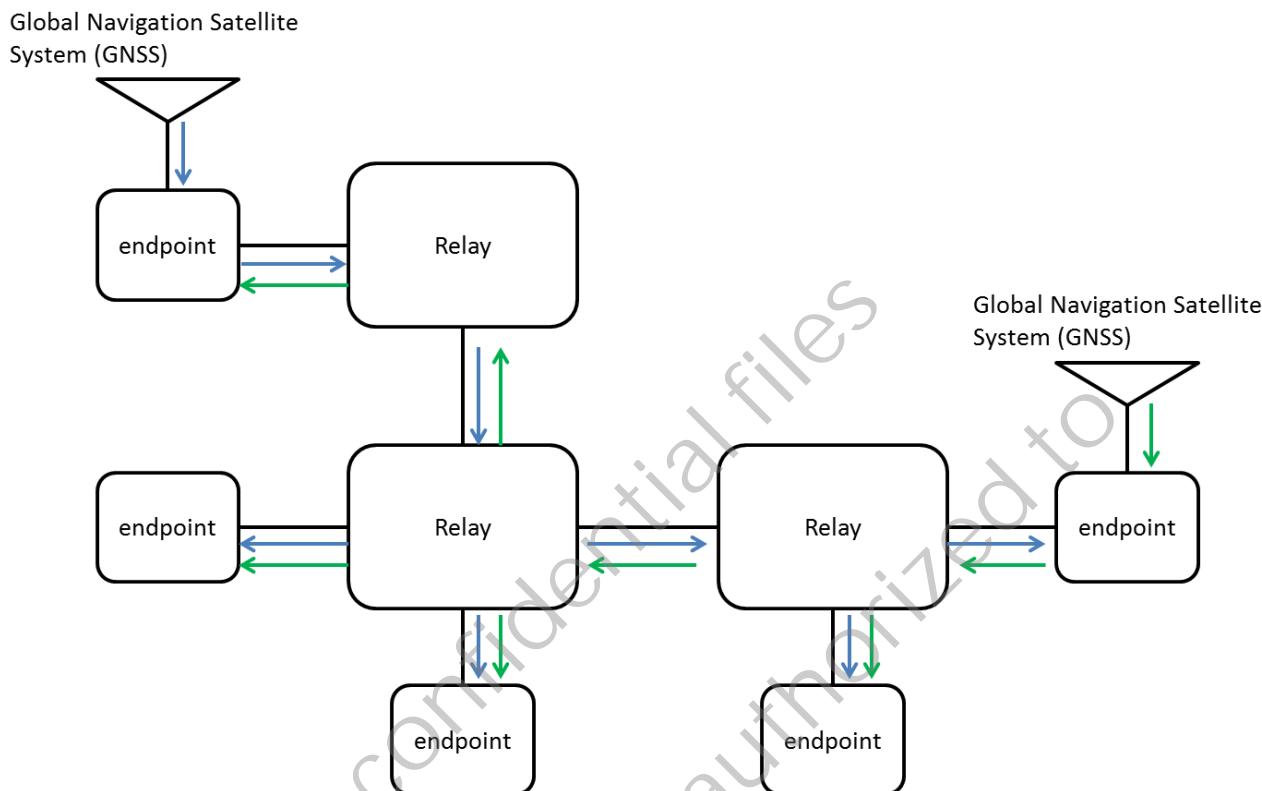


Figure 78. Use as Redundant Clock

In this example, the time in both domains is synchronized with the Global Navigation Satellite System (GNSS). Without multiple PTP instances support in one device, a system needs the redundant clocks to have one PTP network (relays and endpoints port) to get the primary time, and a redundant network (another set of relays and another endpoints port) to get the hot standby time. Having multiple PTP instances in one device solves the problem. This figure illustrates an example of how to use multiple PTP instances as redundant clocks for fault tolerance or for functional safety considerations. The endpoint can use one of the domains as the primary time, and another domain as the hot standby time. If primary time fails, the endpoint can use the hot standby time to maintain system operation with zero down time.

8.29.2. Traffic Shaper and Scheduler

The RTL9054/RTL9068/RTL907x supports IEEE 802.1Qav. The primary function is to achieve bounded latency by reserving bandwidth for the time-sensitive streams on a queue basis.

The RTL9054/RTL9068/RTL907x supports IEEE 802.1Qbv. The primary function is to achieve deterministic latency by scheduling frame transmission on a queue basis.

The time sensitive stream will carry priority information with a VLAN tag (if VLAN is not used, the VLAN identifier will be 0, also called the priority tag). A priority will be set for a traffic class mapping table to map the frame to a corresponding traffic class, and there will be a queue for each traffic class. In general, time sensitive streams will use priority value mapping to high priority traffic classes, while normal traffic uses the values with lower priority traffic classes. To prevent the interference from having unexpected traffic, the port that is not in the domain will modify the priority of ingress frames to lower traffic classes.

When there are frames in a queue, the transmission selection will select the frames according to a priority and transmission selection algorithm. The IEEE 802.1Qav defines the credit based shaper algorithm. The credit based shaper can be configured to reserve a specific bandwidth. The credit starts with 0. The transmission selection starts from the highest priority and checks if credit is greater or equal to 0. If it is, the frame is selected for transmission and upon transmission, the credit will decrease. The credit only affects the decision, so once a frame is selected for transmission, the frame can continue transmission until complete even if the credit falls to less than 0. If a frame's credit is lower than 0 before the decision, the transmission selection will not select this frame and will continue to check the next queue for available frames. The credit increases with reserved bandwidth as long as the queue is not transmitting and is not empty. If the queue is empty, and the credit is greater than 0, the credit is reset to 0. With a credit based shaper, if there is no interference frame, then the highest priority traffic is sent uniformly. With interference (in a worst case scenario), the highest priority traffic only waits one max frame to start the transmission. Thus, the latency is bound at a known value by using the credit based shaper.

IEEE 802.1Qbv defines the transmission gates to control available queues during transmission selection. There is one gate for each corresponding queue, and these gates are controlled by one control list on port based filters. The control list records the gate state and time interval for each entry. The gate state denotes the gate state for each queue in this operation, while the time interval denotes how long it will be maintained in this state.

During configuration, the base time is specific. The transmission gate references the PTP as common time, and the operation is aligned for all devices in the system. If the base time is some time in the future, this will be the start time. The transmission gate will start with the first entry of the control list when the start time is reached. After the time interval has elapsed, the transmission gate continues with the next entry until it reaches the end of the list. The total time interval from the first entry to the last configured entry is called the cycle time. When it reaches the end of the list, the transmission gate will jump back and start with the first entry as its next operation. If the base time is already in the past before the operation begins, the transmission gate will automatically compute the start time to the closest future time to align the execution of other ports or other devices, where the start time is equal to the base time plus the nearest multiple integer of the cycle time.

When the gate state is closed, the frame will not be selected from that queue. When the gate state is open, the corresponding queue is ready to be selected for transmission. The transmission selection algorithm (configured by the user) will select the frame for transmission from a queue with open gate state only. When

a gate goes from open to closed, this is called a close event. If the frame cannot complete the transmission before the close event, the frame will not be selected. The frame transmission can cross consecutive operations as long as the gate state is open. With a transmission gate, the user can configure which timeslot transmits with which queue, and then there will be no interference if open gates are mutually exclusive, hence the transmission gate can achieve deterministic latency.

The traffic shaper and scheduler are generally used in real-time applications.

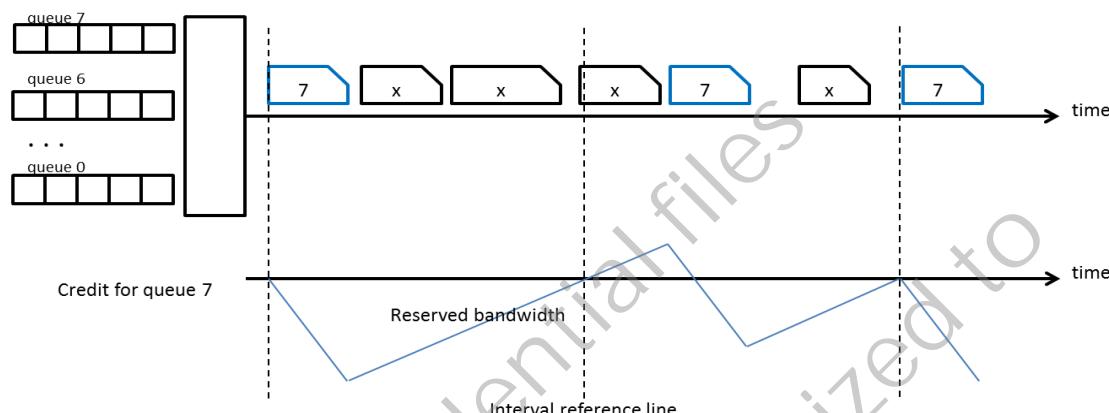


Figure 79. The Credit Based Shaper

The traffic shaper can be used for soft real-time traffic, e.g. audio and video. The frame with the highest priority will have a bounded latency per hop. The max latency is the sum of the transmission time of one interference frame plus the transmission time of frames in the same priority. If the max latency meets the requirement of hard real-time, the traffic shaper can also be applied.

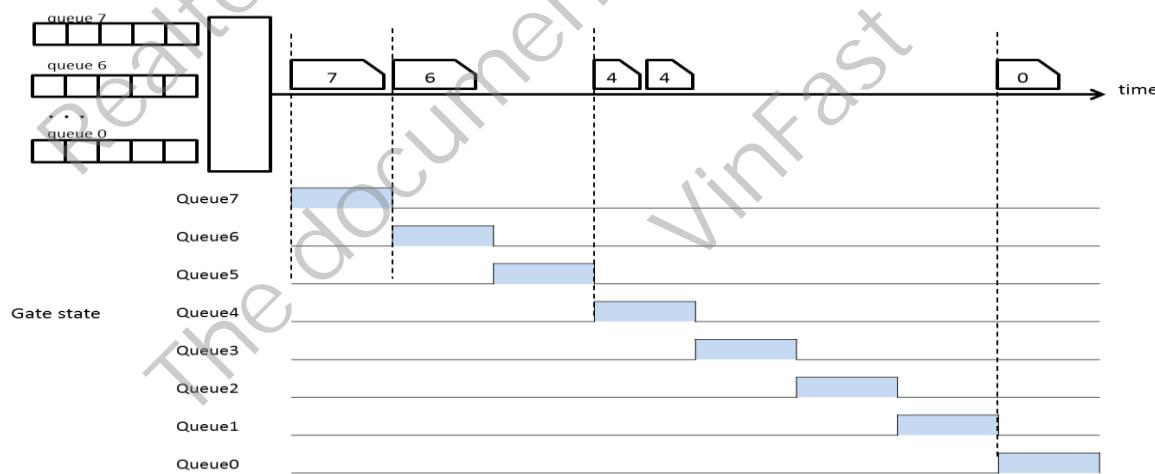


Figure 80. Transmission Gate Control

The scheduler can be applied to a control system. The priority is scheduled according to the transmission gate control list. With a transmission gate, one queue will not affect another queue as long as they are open exclusively. The scheduler provides more accurate control of a transmission, but also leads to some complexities to properly configure the control list.

8.29.3. Per-Stream Filtering and Policing

The RTL9054/RTL9068/RTL907x supports IEEE 802.1Qci. The primary function is to filter the ingress frame and enforce the bandwidth policies on a stream basis.

The RTL9054/RTL9068/RTL907x can examine the Layer2 header (Destination MAC address, Source MAC address, VLAN tag, and in addition EtherType.) and Layer3/4 header (Destination IP, Source IP, DSCP/TC, NextHeader, source port, destination port) to identify the specific stream.

The identified stream will be directed to a stream filter, which will match the stream to find the specific rule for this stream, and then check the stream's max payload size. If the payload size exceeds the limit, the frame will be discarded, and it can block all following frames in this stream if configured. If the payload size meets the limit, the stream is directed to an assigned stream gate and assigned flow meter, which are included in the rules.

The stream gate is stream based filtering, and each stream gate is controlled by an independent control list. The following are the fields that control each entry to the gate state: time interval, internal priority, interval octet max. The gate state determines whether the gate is open or closed and the time interval determines how long the state is maintained. When a frame reaches the stream gate, if the gate is open, the frame can pass. However, if the gate is closed, the frame is discarded, and it will block all the following frames in this stream if it is configured. The internal priority can change the forwarding priority dynamically based on the execution of the control list, as the switch will forward the frame as it is (internally) without changing the content of the frame. When a frame passes through the gate, the number of octets is counted, and if the accumulated octets during the interval exceed the interval octet max, the frame is discarded, and it will block all the following frames in this stream if it is configured.

The flow meter is stream based filtering. Each flow meter is controlled by a set of parameters as follows (reference MEF 10.3):

- Committed Information Rate (CIR), in bits per second
- Committed Burst Size (CBS), in octets
- Excess Information Rate (EIR), in bits per second
- Excess Burst Size (EBS) per bandwidth profile flow, in octets
- Coupling Flag (CF), which takes the value false (0) or true (1)
- Color Mode (CM), which takes the value color-blind or color-aware

The approach is similar to leaky bucket. There are two buckets in a per stream flow meter. Committed bucket credit starts with the value of the committed burst size, and excess bucket credit starts with the value of the excess burst size.

When a frame is filtered through the flow meter, if the committed credit is greater than the frame size, the frame is classified as a green frame and the committed credit is subtracted to match the frame size. If committed credit is less than the frame size, excess credit is checked. If excess credit is greater than the frame size, the frame is classified as a yellow frame and the excess credit is subtracted to match the frame size. If the excess credit is less than the frame size, the frame is classified as a red frame. If the committed/excess credit is less than the committed/excess burst size, it is increased at a committed/excess information rate, and bounded at the committed/excess burst size.

The coupling flag determines if the overflow credit is added to the excess credit when the committed credit has reached the committed burst size.

The color mode determines if the flow meter recognizes the frame color in previous hops. . If color mode is color-blind, the frame always starts a check with the committed credit. If color mode is color-aware, the flow meter will check the frame mark first. If it was a yellow frame in previous hops, the frame will check the excess bucket. If the frame is not marked in previous hops, the frame will check the committed bucket.

After a frame is classified, the green frame passes the flow meter, the yellow frame is configurable to set mark or discard, and the red frame is discarded. It will block all the following frames in this stream if it is configured.

A possible use case is fault isolation.

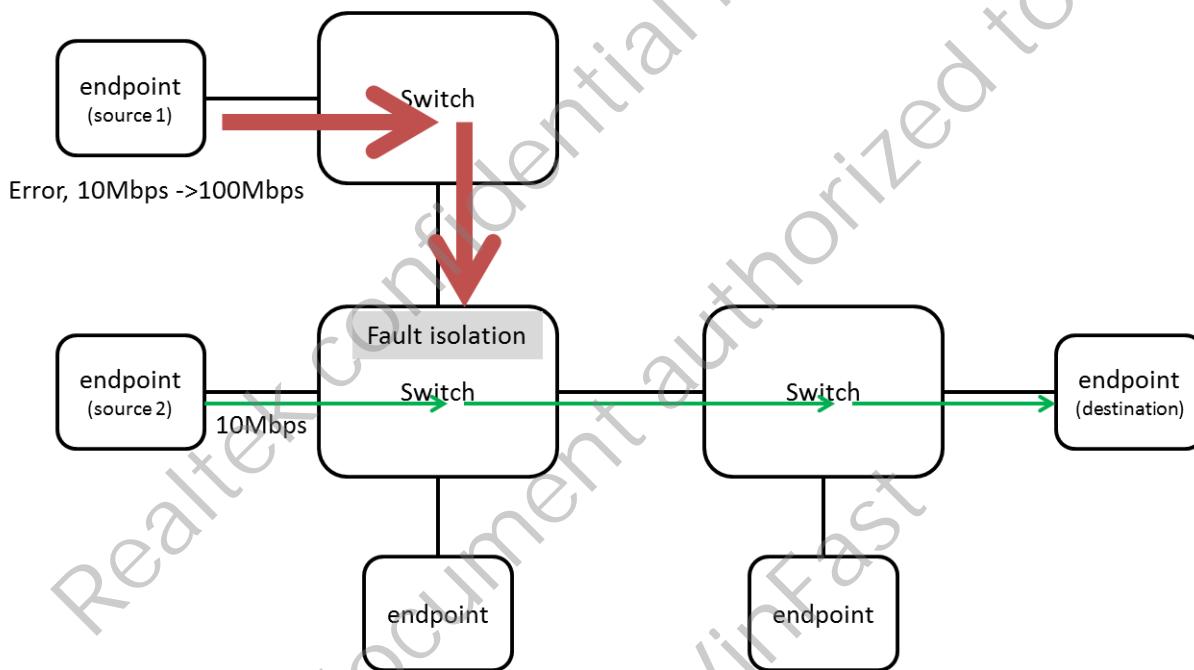


Figure 81. Per Stream Policing and Filtering Case

In the figure above, there are 2 traffic sources and 1 destination. In a normal situation, each source sends 10 Mbps traffic to the destination. However, if random failure happens on one of the traffic sources, it may send garbage traffic with line speed continuously, indicated by the bold red arrow in the above figure. Without filtering and policing, the garbage traffic will be forwarded by switch and affect other normal traffic, as shown in the top left switch. When implementing filtering and policing, the garbage traffic can be filtered out, and the fault will be isolated to the limited device only. In a best case scenario, if the immediate hop of a failure device supports filtering and policing, the fault will be limited to the failure device only.

8.30. Stacking

The RTL9068/RTL907x supports stacking for up to 4 switches. Stackable switch is a standalone network switch with full functions that can be setup to operate together with one or more other switches. Within a group of stackable switches, it is characterized as a single switch, but the port capacity is the sum of combined switches.

Figure 82 shows a usual stacking situation. No matter how many stacking switches there are, the configuration and management is only seen as one interface by the network administrator. The host (for example, the SoC) can access the stacking switches through one register interface (SPI/I2C/MDCMDIO) and then transmit and receive packets through one high bandwidth bus (such as RGMII, USXGMII, PCI Express). In a stacking switch, the external storage flash memory for configuration and firmware can be reduced to one only.

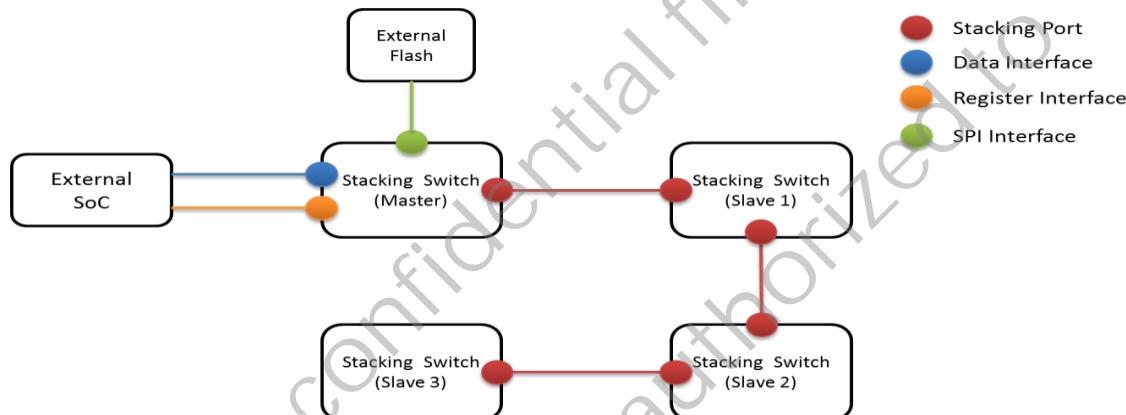


Figure 82. Stacking Switches

8.31. Packet Offload on PCI-Express

The RTL9068/RTL907x supports the following Linux based offload features through the PCI-E Interface:

8.31.1. TX/RX Checksum Offload

Checksum needs to be calculated for IP and TCP/UDP packets. However, the checksum calculation has a fixed and repeated behavior, so the RTL9068/RTL907x implements a hardware circuit to calculate it. Thus, the CPU can offload a checksum calculation to the RTL9054/RTL9068/RTL907x to reduce its computing efforts.

8.31.2. VLAN TX RX Offload

The RTL9068/RTL907x supports inserting C-Tag into Tx 802.1q packets. Also, the RTL9068/RTL907x supports extracting C-Tag from Rx 802.1q packets.

8.31.3. TCP Segmentation Offload

If the TCP message is longer than the maximum segment size (MSS), it should be segmented before being transmitted. The RTL9068/RTL907x supports TCP segmentation to increase Tx throughput by reducing CPU overhead.

8.32. Single Root I/O Virtualization on PCI-Express

The RTL9068/RTL907x's single root I/O virtualization (SR-IOV) is a feature of the PCIe. The purpose of SR-IOV is to allow multiple virtual functions to exist under a single physical function. In other words, one physical PCIe device can simulate multiple virtual PCIe devices for the use of multiple virtual machines. Traditionally, software-based virtualization is used for multiple virtual machines to access one PCIe device concurrently without SR-IOV. Software-based virtualization may cause high loading of a CPU and low efficiency when using the PCIe device. However, SR-IOV offloads the main effort of virtualization to the PCIe device. One virtual function of the RTL9068/RTL907x is to support the packet transmitting and receiving function of one virtual machine. Compared to a physical function, the virtual function requires less configuration space and I/O space. The virtual function's only task is to transmit and receive packets correctly. The rest of the tasks have to be done by physical functions. The RTL9068/RTL907x provides a virtual function driver for the virtual machine in order to access the virtual function of the PCIe device. Also, the RTL9068/RTL907x provides a physical function driver to access the physical function of the PCIe device. The figure below illustrates the system architecture of SR-IOV.

The RTL9068/RTL907x supports 1 physical function and 7 virtual functions in SR-IOV mode. Each function has 8 transmission queues supporting credit-based shaping TxQoS.

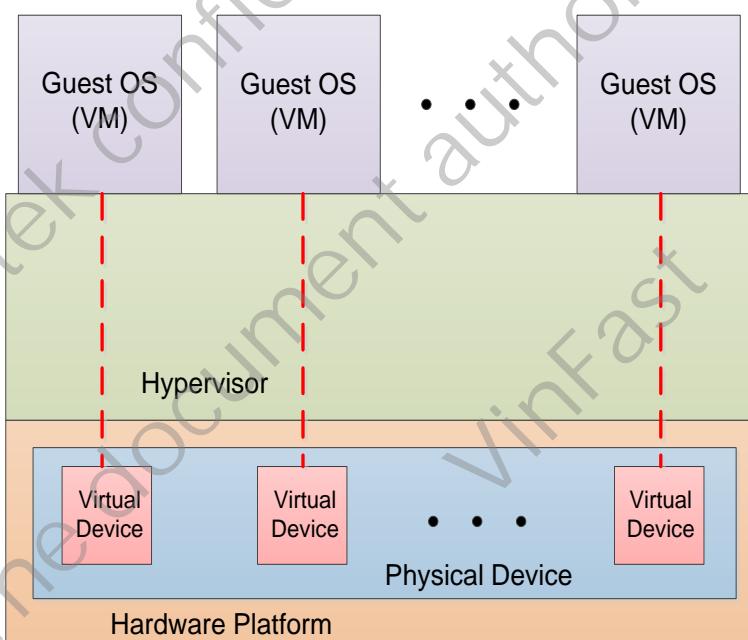


Figure 83. System Architecture of SR-IOV

8.33. Secure Boot

8.33.1. Embedded Secure Module (ESM)

Secure boot requires support from hardware encryption engines. In the RTL9054/RTL9068/RTL907x, security related hardware is called Embedded Secure Module (ESM). It contains true random number generators, hash algorithm engines such as MD5 and SHA1, asymmetric cryptography engines such as RSA, symmetric cryptography engines such as AES and secure One-Time-Programmable (OTP) memory. There is also a software stack to control these engines. The architecture of the ESM is shown in Figure 84:

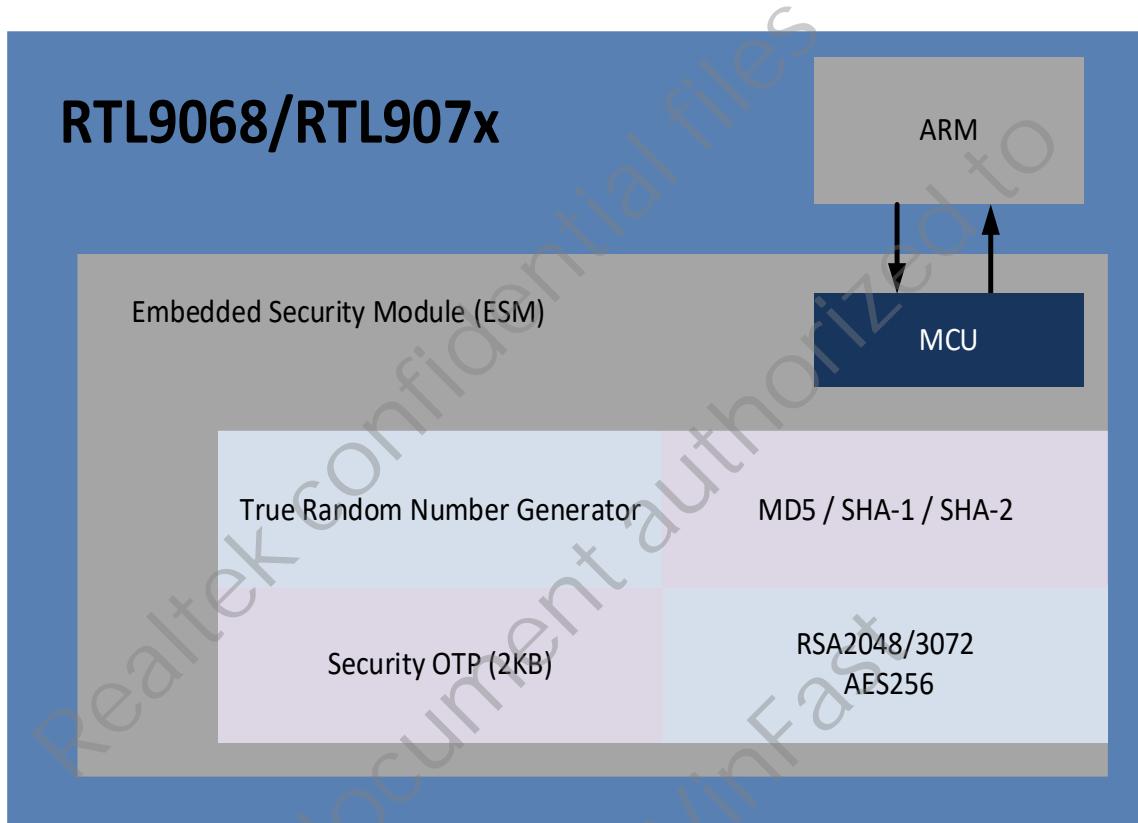


Figure 84. The Architecture of ESM

8.33.2. Secure Boot System Block

Secure boot is used in flash boot-up mode to prevent damage caused from maliciously replacing a tampered flash placed on the PCB to alter the switch functions. The switch obtains data that is encrypted from flash via the SPI interface, and when the data is received, the switch decrypts it. The data stored in flash includes the firmware code and the signature of the publisher for the configuration file. When the decryption is complete, the switch will compare the outcome with this signature. If it is legal, the switch will boot up from flash, otherwise, it will return to ROM mode.

In order to remain flexible, the user can use 2bits in OTP to determine secure boot mode. These modes include:

- Firmware is decrypted by AES256 and applies hash and RSA
- Firmware is not decrypted by AES and only uses the hash and RSA
- Disable mode

Table 61 shows the bits definition for security boot.

Table 61. Bit Definition for Security Boot

Reg.bit	Name
11	Disable mode
00	RAS, hash only
01	Reserved
10	Security mode AES256 with RSA hash

8.33.3. Initialize Keys

In the RTL9054/RTL9068/RTL907x, there is no key in OTP by default. When the product is in the production stage, it needs a black box function (provided by Realtek) to insert the keys. Figure 85 shows the timing when writing the RSA key and the AES key.

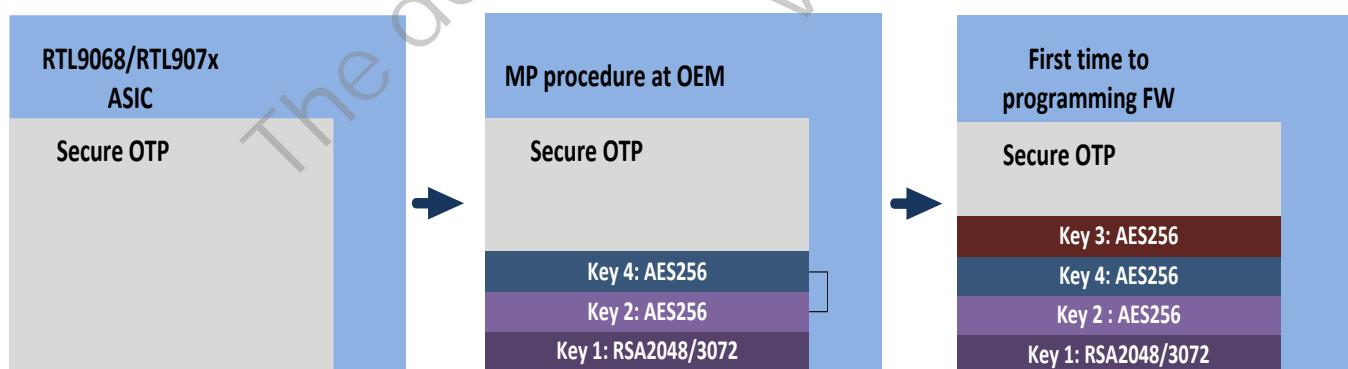


Figure 85. Keys Initialization Stages

8.33.4. Flash Layout Stack

Figure 86 shows the flash layout stack. There are two partitions in a flash layout stack. One is a protected firmware code partition, and the other is a protected configuration partition. These partitions include a firmware code encrypted by AES, a hashed firmware code encrypted by RSA, a configuration encrypted by AES and a hashed configuration encrypted by RSA. There are three sizes of configuration partition, 128KB, 256KB and 512KB and the size will be determined by specific bits in the flash.

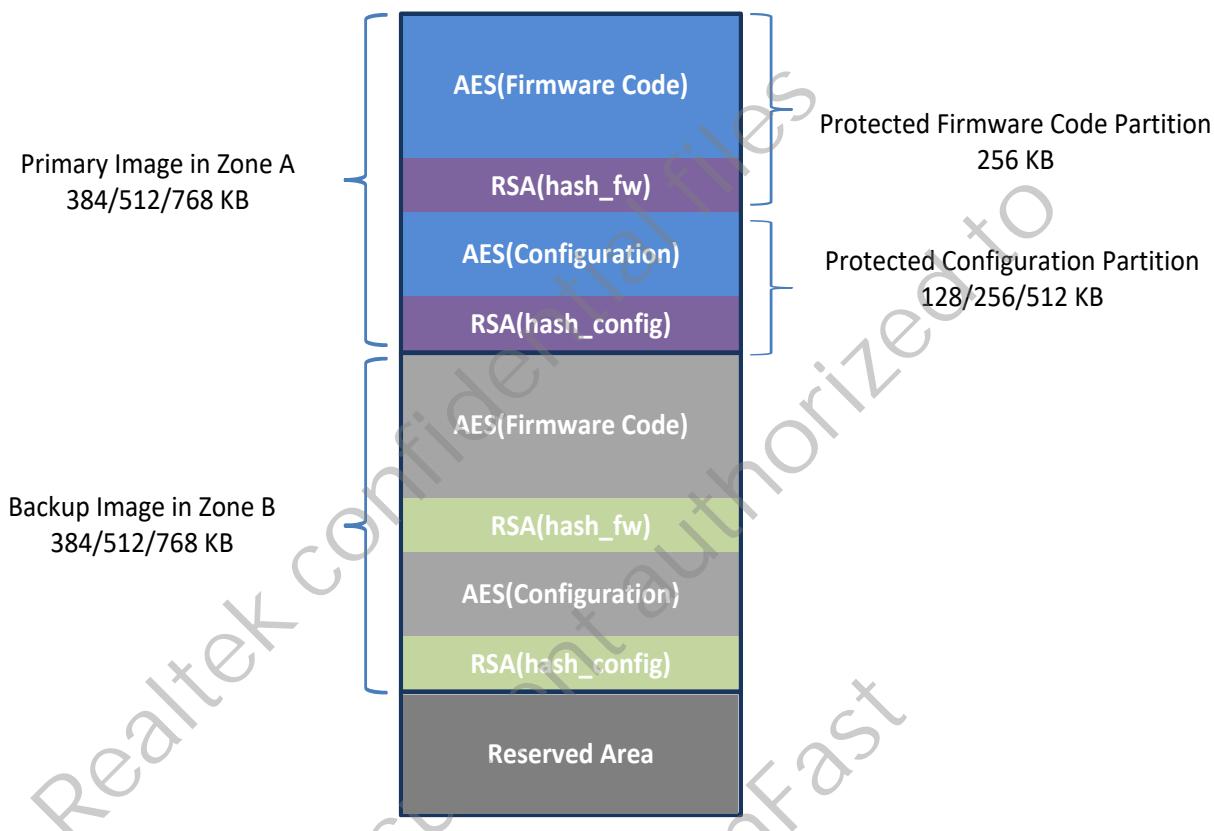


Figure 86. Flash Layout Stack

8.33.5. Boot-Up Flow

The boot-up flow steps are as follows:

First, the switch will determine if the secure boot is enabled or not. If secure boot is disabled, the switch will load a plaintext code into SRAM and begin to execute a boot-up flow. If secure boot is enabled, the switch will execute the flow depending on which mode is selected. If mode 1 is selected (mentioned in section 8.33.2), the switch will load the plaintext of the firmware code and verify the hash with RSA. If mode 0 or 2 is selected, the switch will load the cipher text of the firmware code and decrypt it with the AES key. After the decryption, the switch will verify the hash with RSA. If the hash is verified, the switch will load the firmware code to SRAM and begin to execute the boot-up flow. If the verification fails, the switch will stay in fail-safe mode where the switch cannot forward packets and will only be able to update the flash again.

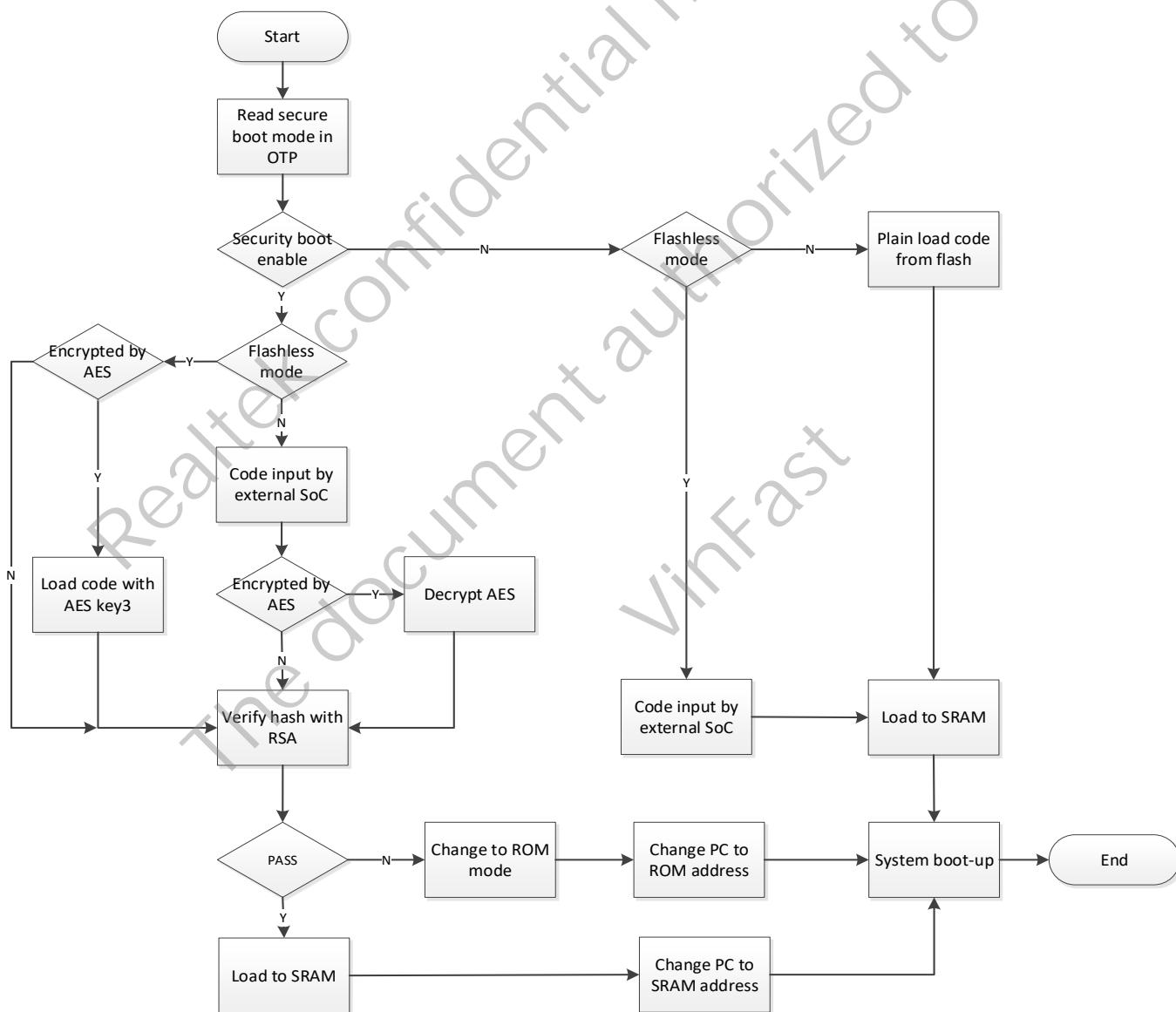


Figure 87. Security Boot-up Flow

8.34. Attack Prevention

8.34.1. Layer 2/3/4 Malicious Packet Filter

The switch supports layer 2 (Data Link Layer), layer 3 (Network Layer) and layer 4 (Transport Layer) malicious packet filter and drop. It contains malicious packet patterns such as unreasonable source address and destination address, unreasonable combination of source address and destination address, unreasonable source IP, unreasonable destination IP, unreasonable IP fragment, fragment size, unreasonable TCP flag, TCP source port, UDP source port and payload size. The attack prevention filter types are as follows:

- DAEQSA: Source Address is equal to Destination Address
- ZERO_MAC: Source Address and Destination Address are zero
- MCSA: Source Address is a Multicast MAC
- LAND: Source IP is equal to Destination IP
- UDPBLAT: Source UDP port is equal to the Destination UDP port
- TCPBLAT: The TCP port is also the destination TCP port
- POD: Uses packets larger than 64K bytes through fragments
- ICMP_FRAG_PKTS: Fragmented ICMP packets
- ICMPv4_PING_MAX: ICMPV4 ping packets with payload size greater than the programmable value
- ICMPv6_PING_MAX: ICMPV6 ping packets with payload size greater than the programmable value
- SMURF: ICMP ping request to a broadcast Destination IP (x.x.x.255)
- TCPHDR_MIN: First TCP fragments that don't have the full TCP header
- SYNSPORTL1024: SYN packets with a port less than 1024 and ACK = 0
- NULLSCAN: TCP sequence number is zero and all control bits (Flags) are zeroes
- XMAS: Sequence number is zero and the FIN, URG, and PSH bits are set
- SYNFIN: SYN and FIN bits set in the TCP packet
- SYNRST: SYN and RST bits set in the TCP packet
- IPV4_MIN_FRAG_SIZE_ENABLE: Minimum size of IPV4 fragments
- IPV6_MIN_FRAG_SIZE_ENABLE: Minimum size of IPV6 fragments
- TCP_FRAG_ERR_DENY: IP header fragment_offset = 1, and next protocol is TCP
- Elastic Mechanism

9. Electrical AC/DC Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 62. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	150	°C
VBAT	-0.3	58	V
V33	-0.3	3.63	V
AVDD33, AVDD33_HVD, AVDD33_CEN, AVDD33_CKDIG, AVDD33_CMU, AVDD33_DIG, AVDD33_FE, AVDD33_MCK, AVDD33_P2, AVDD33_P3, AVDD33_AHV, AVDD33_SGMII, AVDD33_XTAL, DVDD33	GND-0.3	+3.63	V
AVDD09, AVDD09_CMU, AVDD09_FE, AVDD09_GIGA, AVDD09_MCK, AVDD09_RX, AVDD09_SGMII, AVDD09_TX, DVDD09	GND-0.3	+0.99	V
Voltage on pins x_MDIP, x_MDIN of 100BASE-T1 and 100BASE-TX x_MDIPx, x_MDIPNx	GND-0.3	3.63	V
INH (RTL9068/RTL907x)	GND-0.3	VBAT+0.3	V
INH (RTL9054)	GND-0.3	V33+0.3	
WAKE (RTL9068/RTL907x)	GND-0.3	VBAT+0.3	V
WAKE (RTL9054)	GND-0.3	V33+0.3	
XI, XO	GND-0.3	1.98	V
Voltage on output pins of RGMII/MII/RMI, GPIO_Domain, and MAC_VDDIO (Configured as 3.3V IO)	GND-0.3	+3.63	V
Voltage on output pins of RGMII/MII/RMI, GPIO_Domain, and MAC_VDDIO (Configured as 2.5V IO)	GND-0.3	+2.8	V
Voltage on output pins of RGMII/MII/RMI, GPIO_Domain, and MAC_VDDIO (Configured as 1.8V IO)	GND-0.3	+2.3	V
Voltage on other pins	GND-0.3	+3.63	V

Note: Refer to the most updated schematic circuit for correct configuration.

Note2: Transient voltage on VBAT, MDIP, MDIN, and WAKE pins. Confirmed by FTZ.

9.2. Recommended Operating Range

Table 63. Recommended Operating Range

Parameter	Min	Typ.	Max	Units
Ambient Operating Temperature (Ta)	-40	-	105	°C
AVDD33, AVDD33_HVD, AVDD33_CEN, AVDD33_CKDIG, AVDD33_CMU, AVDD33_DIG, AVDD33_FE, AVDD33_MCK, AVDD33_P2, AVDD33_P3, AVDD33_AHV, AVDD33_SGMII, AVDD33_XTAL, DVDD33 Supply Voltage Range	3.135	3.3	3.465	V
P0_VDDIO, P1_VDDIO, P4_VDDIO, P5_VDDIO, P9_VDDIO, GPIO0_VDDIO, GPIO1_VDDIO, MAC_VDDIO, SPI_VDDIO Supply Voltage Range (Configured as 3.3V IO)	3.135	3.3	3.465	V
P0_VDDIO, P1_VDDIO, P4_VDDIO, P5_VDDIO, P9_VDDIO, GPIO0_VDDIO, GPIO1_VDDIO, MAC_VDDIO, SPI_VDDIO Supply Voltage Range (Configured as 2.5V IO)	2.375	2.5	2.625	V
P0_VDDIO, P1_VDDIO, P4_VDDIO, P5_VDDIO, P9_VDDIO, GPIO0_VDDIO, GPIO1_VDDIO, MAC_VDDIO, SPI_VDDIO Supply Voltage Range (Configured as 1.8V IO)	1.71	1.8	1.89	V
AVDD09, AVDD09_CMU, AVDD09_FE, AVDD09_GIGA, AVDD09_MCK, AVDD09_RX, AVDD09_SGMII, AVDD09_TX, DVDD09 Supply Voltage Range	0.855	0.9	0.945	V
VBAT	3.135	12/24	40	V
V33	2.4	3.3	3.46	V

Note: Considering for the maximum voltage ripple, the ripple and noise on AVDD33 domain should be within 66mVpp (+/-1% AVDD33), within 30mVpp (+/-1.67% AVDD09/DVDD09) on 0.9V domain, and the VDDIO should be within +/- 2% VDDIO. Plus the DC inaccuracy, the summation of the power variation cannot exceed +/-5%.

9.3. DC Characteristics

9.3.1. DC IO Characteristics

Table 64. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Pin WAKE						
V _{IH_WAKE}	Detected Level Input Voltage 1 ^{*Note1}	Sleep mode	2.4	2.55	3.0	V
V _{IL_WAKE}	Detected Level Input Voltage 1 ^{*Note1}	Sleep mode	2.0	2.15	2.7	V
V _{IH_WAKE}	Detected Level Input Voltage 2 ^{*Note1}	Sleep mode	2	-	-	V
V _{IL_WAKE}	Detected Level Input Voltage 2 ^{*Note1}	Sleep mode	-	-	0.8	V
I _{IH_WAKE}	HIGH-Level Input Current	V _{IO} = 3.3V	-	-	100	uA
I _{IL_WAKE}	LOW-Level Input Current	V _{IO} = 0V	-	-	100	uA
T _{det_WAKE}	Local WAKE Event Detection Time 1 ^{*Note2}	Sleep mode	-	20	-	us
T _{det_WAKE}	Local WAKE Event Detection Time 2 ^{*Note2}	Sleep mode	10	-	-	ms
Pin INH						
V _{OH_INH}	HIGH-Level Output Voltage	I _{INH} = 3mA RTL9068/RTL907x	V _{BAT} -2	-	V _{BAT}	V
V _{OH_INH}	HIGH-Level Output Voltage	I _{INH} = 3mA RTL9054	V ₃₃ -0.3	-	V ₃₃	V
V _{OL_INH}	LOW-Level Output Voltage	-	-	0	0.4	V
I _{OH_INH}	HIGH-Level Output Current	V _{INH} = High, INH pin tie to 0V	-5.97	-	-1.61	mA
Pin XI						
V _{IH_XI}	HIGH-Level Input Voltage	V _{IO} = 3.3V	1.4	-	-	V
V _{IL_XI}	LOW-Level Input Voltage	V _{IO} = 3.3V	-	-	0.4	V
Pin XO						
V _{OH_XO}	HIGH-Level Output Voltage	V _{IO} = 3.3V	1.4	1.5	-	V
V _{OL_XO}	LOW-Level Output Voltage	V _{IO} = 3.3V	-	0	0.4	V
V _{IH_XO}	HIGH-Level Input Voltage	V _{IO} = 3.3V	1.4	-	-	V
V _{IL_XO}	LOW-Level Input Voltage	V _{IO} = 3.3V	-	-	0.4	V
Pins TXD[3:0], TESTD, and TXC						
V _{OH}	HIGH-Level Output Voltage	V _{IO} = 3.3V	2.4	-	-	V
V _{OL}	LOW-Level Output Voltage	V _{IO} = 3.3V	-	0	+0.4	V
I _{OH}	HIGH-Level Output Current	V _{IO} = 0.9*3.3V	6	-	-	mA
I _{OL}	LOW-Level Output Current	V _{IO} = 0.1*3.3V	6	-	-	mA
V _{IH}	HIGH-Level Input Voltage	V _{IO} = 3.3V	2	-	-	V
V _{IL}	LOW-Level Input Voltage	V _{IO} = 3.3V	-	-	+0.8	V
I _{IH}	HIGH-Level Input Current	V _{IO} = 3.3V	-	-	100	uA
I _{IL}	LOW-Level Input Current	V _{IO} = 0V	-	-	100	uA
I _L	Leakage Current	Power off; V _{IO} = 3.3V	-	0.1	5	uA
V _{OH}	HIGH-Level Output Voltage	V _{IO} = 2.5V	2.0	-	-	V
V _{OL}	LOW-Level Output Voltage	V _{IO} = 2.5V	-	-	+0.4	V

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
I_{OH}	HIGH-Level Output Current	$V_{IO} = 0.9*2.5V$	2	-	-	mA
I_{OL}	LOW-Level Output Current	$V_{IO} = 0.1*2.5V$	2	-	-	mA
V_{IH}	HIGH-Level Input Voltage	$V_{IO} = 2.5V$	1.7	-	-	V
V_{IL}	LOW-Level Input Voltage	$V_{IO} = 2.5V$	-	-	+0.7	V
I_{IH}	HIGH-Level Input Current	$V_{IO} = 2.5V$	-	-	100	uA
I_{IL}	LOW-Level Input Current	$V_{IO} = 0V$	-	-	100	uA
I_L	Leakage Current	Power off; $V_{IO} = 3.3V$	-	0.1	5	uA
V_{OH}	HIGH-Level Output Voltage	$V_{IO} = 1.8 V$	$0.9*VDD18$	-	-	V
V_{OL}	LOW-Level Output Voltage	$V_{IO} = 1.8 V$	-	-	$0.1*VDD18$	V
I_{OH}	HIGH-Level Output Current	$V_{IO} = 0.9*1.8V$	1.5	-	-	mA
I_{OL}	LOW-Level Output Current	$V_{IO} = 0.1*1.8V$	1.5	-	-	mA
V_{IH}	HIGH-Level Input Voltage	$V_{IO} = 1.8 V$	1.2	-	-	V
V_{IL}	LOW-Level Input Voltage	$V_{IO} = 1.8 V$	-	-	+0.5	V
I_{IH}	HIGH-Level Input Current	$V_{IO} = 1.8 V$	-	-	100	uA
I_{IL}	LOW-Level Input Current	$V_{IO} = 0V$	-	-	100	uA
I_L	Leakage Current	Power off; $V_{IO} = 3.3V$	-	0.1	5	uA
Pins GPIOx						
V_{OH}	HIGH-Level Output Voltage	$V_{IO} = 3.3V$	2.4	-	-	V
V_{OL}	LOW-Level Output Voltage	$V_{IO} = 3.3V$	-	0	+0.4	V
I_{OH}	HIGH-Level Output Current	$V_{IO} = 0.9*3.3V$	6	-	-	mA
I_{OL}	LOW-Level Output Current	$V_{IO} = 0.1*3.3V$	6	-	-	mA
V_{IH}	HIGH-Level Input Voltage	$V_{IO} = 3.3V$	2	-	-	V
V_{IL}	LOW-Level Input Voltage	$V_{IO} = 3.3V$	-	-	+0.8	V
I_{IH}	HIGH-Level Input Current	$V_{IO} = 3.3V$	-	-	100	uA
I_{IL}	LOW-Level Input Current	$V_{IO} = 0V$	-	-	100	uA
I_L	Leakage Current	Power off; $V_{IO} = 3.3V$	-	0.1	5	uA
V_{OH}	HIGH-Level Output Voltage	$V_{IO} = 2.5V$	2.0	-	-	V
V_{OL}	LOW-Level Output Voltage	$V_{IO} = 2.5V$	-	-	+0.4	V
I_{OH}	HIGH-Level Output Current	$V_{IO} = 0.9*2.5V$	2	-	-	mA
I_{OL}	LOW-Level Output Current	$V_{IO} = 0.1*2.5V$	2	-	-	mA
V_{IH}	HIGH-Level Input Voltage	$V_{IO} = 2.5V$	1.7	-	-	V
V_{IL}	LOW-Level Input Voltage	$V_{IO} = 2.5V$	-	-	+0.7	V
I_{IH}	HIGH-Level Input Current	$V_{IO} = 2.5V$	-	-	100	uA
I_{IL}	LOW-Level Input Current	$V_{IO} = 0V$	-	-	100	uA
I_L	Leakage Current	Power off; $V_{IO} = 3.3V$	-	0.1	5	uA
V_{OH}	HIGH-Level Output Voltage	$V_{IO} = 1.8 V$	$0.9*VDD18$	-	-	V
V_{OL}	LOW-Level Output Voltage	$V_{IO} = 1.8 V$	-	-	$0.1*VDD18$	V
I_{OH}	HIGH-Level Output Current	$V_{IO} = 0.9*1.8V$	1.5	-	-	mA
I_{OL}	LOW-Level Output Current	$V_{IO} = 0.1*1.8V$	1.5	-	-	mA
V_{IH}	HIGH-Level Input Voltage	$V_{IO} = 1.8 V$	1.2	-	-	V

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V _{IL}	LOW-Level Input Voltage	V _{IO} = 1.8 V	-	-	+0.5	V
I _{IH}	HIGH-Level Input Current	V _{IO} = 1.8 V	-	-	100	uA
I _{IL}	LOW-Level Input Current	V _{IO} = 0V	-	-	100	uA
I _L	Leakage Current	Power off; V _{IO} = 3.3V	-	0.1	5	uA
Pins FE_LED0, FE_LED1, P0_LED, P10_LED, P1_LED, P2_LED, P3_LED, P4_LED, P5_LED, P6_LED, P7_LED, P9_LED, P10_LED, P12_LED, P13_LED						
V _{OH}	HIGH-Level Output Voltage	V _{IO} = 3.3V	2.4	-	-	V
V _{OL}	LOW-Level Output Voltage	V _{IO} = 3.3V	-	-	+0.4	V
I _{OH}	HIGH-Level Output Current	V _{IO} = 0.9*3.3V	8	-	-	mA
I _{OL}	LOW-Level Output Current	V _{IO} = 0.1*3.3V	8	-	-	mA
Pins MDC, RESETB, RXER, RXDV, RXC, RXD[3:0], and DISB						
V _{IH}	HIGH-Level Input Voltage	V _{IO} = 3.3V	2	3.3	-	V
V _{IL}	LOW-Level Input Voltage	V _{IO} = 3.3V	-	0	+0.8	V
V _{IH}	HIGH-Level Input Voltage	V _{IO} = 2.5V	1.7	-	-	V
V _{IL}	LOW-Level Input Voltage	V _{IO} = 2.5V	-	-	+0.7	V
V _{IH}	HIGH-Level Input Voltage	V _{IO} = 1.8 V	1.2	-	-	V
V _{IL}	LOW-Level Input Voltage	V _{IO} = 1.8 V	-	-	+0.5	V

Note 1: Positive currents flow into the chip.

Note 2: The default setting is V_{IH_WAKEI} and V_{IL_WAKEI}. The detecting level can be changed by the register.

Note 3: The default setting is T_{det_WAKEI}. The detecting time can be changed by the register.

9.4. Power Dissipation

The following power consumptions are maximum values estimated under operating conditions as in Sec.9.2, with VBAT-rail = 12V, 3.3V-rail = 3.3V to 3.465V, and 0.9V-rail = 0.9V to 0.945V. The ambient temperature is from 25 °C to 105°C.

Table 65. Interface Configurations for Power Dissipation Estimation

Product Name	Interfaces
RTL9075AAD	Port0 ~ 3: 100BASE-T1 Port4 ~ 5: RGMII 3.3V Port6 ~ 7: Combo PHY with 1000BASE-T1 Port8 ~ 9: SGMII Port10: USXGMII Port11: PCI-E3.0 Port12 ~ 13: 100BASE-T1 Port14: 100BASE-TX
RTL9072AAD	Port0 ~ 3: 100BASE-T1 Port4 ~ 5: RGMII 3.3V Port6 ~ 7: Combo PHY with 1000BASE-T1 Port8: 100BASE-TX Port9: SGMII Port10: USXGMII Port11: PCI-E3.0
RTL9068AAD	Port0 ~ 1: RGMII 3.3V

Product Name	Interfaces
RTL9068ABD	Port2 ~ 3: Combo PHY with 1000BASE-T1 Port4: 100BASE-TX Port5: SGMII Port6: USXGMII Port7: PCI-E3.0
RTL9054AN	Port0 ~ 3: 100BASE-T1 Port4 ~ 5: 100BASE-T1 Port6 ~ 7: 100BASE-T1 Port8 ~ 9: SGMII Port10: N/A Port11: RGMII Port12 ~ 13: 100BASE-T1 Port14: 100BASE-TX

Table 66. Power Consumption

Product Name/Mode	VBAT-Rail (mA)		3.3V-Rail (mA)		0.9V-Rail (mA)	
	Typ.	Max	Typ.	Max	Typ.	Max
RTL9075AAD Traffic	2.5	4.5	486	512	1030	1895
RTL9072AAD Traffic	2.5	4.5	448	479	990	1786
RTL9068AAD RTL9068ABD Traffic	2.5	4.5	388	418	963	1706
Sleep Mode	0.03	0.08	-	-	-	-
RTL9054AN	-	-	312	372	586	1191

9.5. Over Temperature Protection

Table 67. Over Temperature Protection

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
T _{otp_det}	Over Temperature Protection Detection Junction Temperature	-	-	145	-	°C
T _{otp_rec}	Over Temperature Protection Recovery Junction Temperature	-	-	135	-	°C
T _{otp_hys}	Over Temperature Protection Hysteresis Temperature	-	-	10	-	°C

9.6. ESD

The ESD tolerance of the RTL9068/RTL907x is listed in Table 68.

Table 68. RTL9054/9068/RTL907x ESD Criteria

Feature Description	Value	Comment
HBM – MDIP, MDIN, VBAT and WAKE pins	$\pm 6\text{kV}$	-
HBM – Others	$\pm 2\text{kV}$	-
CDM	Corner pins $\pm 750\text{V}$ Other pins $\pm 500\text{V}$	-
Open Alliance - Unpowered / Powered ESD Contact discharge on MDIP, MDIN, VBAT and WAKE pins	$\pm 6\text{kV}$	(1) The test method is referred to Open Alliance EMC test. (IEEE 1000BASE-T1 EMC Test Specification for Transceivers) (2) The test equipment set-up is referred to IEC61000-4-2.
Latch Up	Power: $1.5*\text{VDD}$ I: 100mA	-

9.7. Power Controller

The RTL9054/RTL9068/RTL907x offers a power controller, which operates at 1Mhz, to control external P/N MOSFET in order to covert power from 3.3V (or higher, depends on P/N MOSFET ability) to 0.9V. The 0.9V power is only for the RTL9054/RTL9068/RTL907x's 0.9V domain.

9.7.1. Inductor Requirements

Table 69. Inductor Requirements

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$L_{1\text{Mhz}}$	Inductance value at 1Mhz	1Mhz	1.76	2.2	2.64	uH
R_{DC}	DC resistance	-	-	-	30	$\text{m}\Omega$
I_{SR}	Saturated or Rated current	-	5	-	-	A

Note 1: AEC-Q200 is required.

Note 2: Needs to be qualified by Realtek.

9.7.2. Power MOSFET Requirements

The following component DMC1015UPD is used for Realtek internal testing. $R_{DS(ON)}$ of PMOS and NMOS are lower than the DMC1015UPD part, and the ID current value of PMOS and NMOS remaining higher than the DMC1015UPD part is recommended. AEC-Q101 qualified is required and needs to be qualified by Realtek.

9.8. AC Characteristics

9.8.1. RGMII Timing

Figure 88 shows the effect of adding an additional delay to TXC by PC board (upper side) or by transmitter internally (lower side) in RGMII mode.

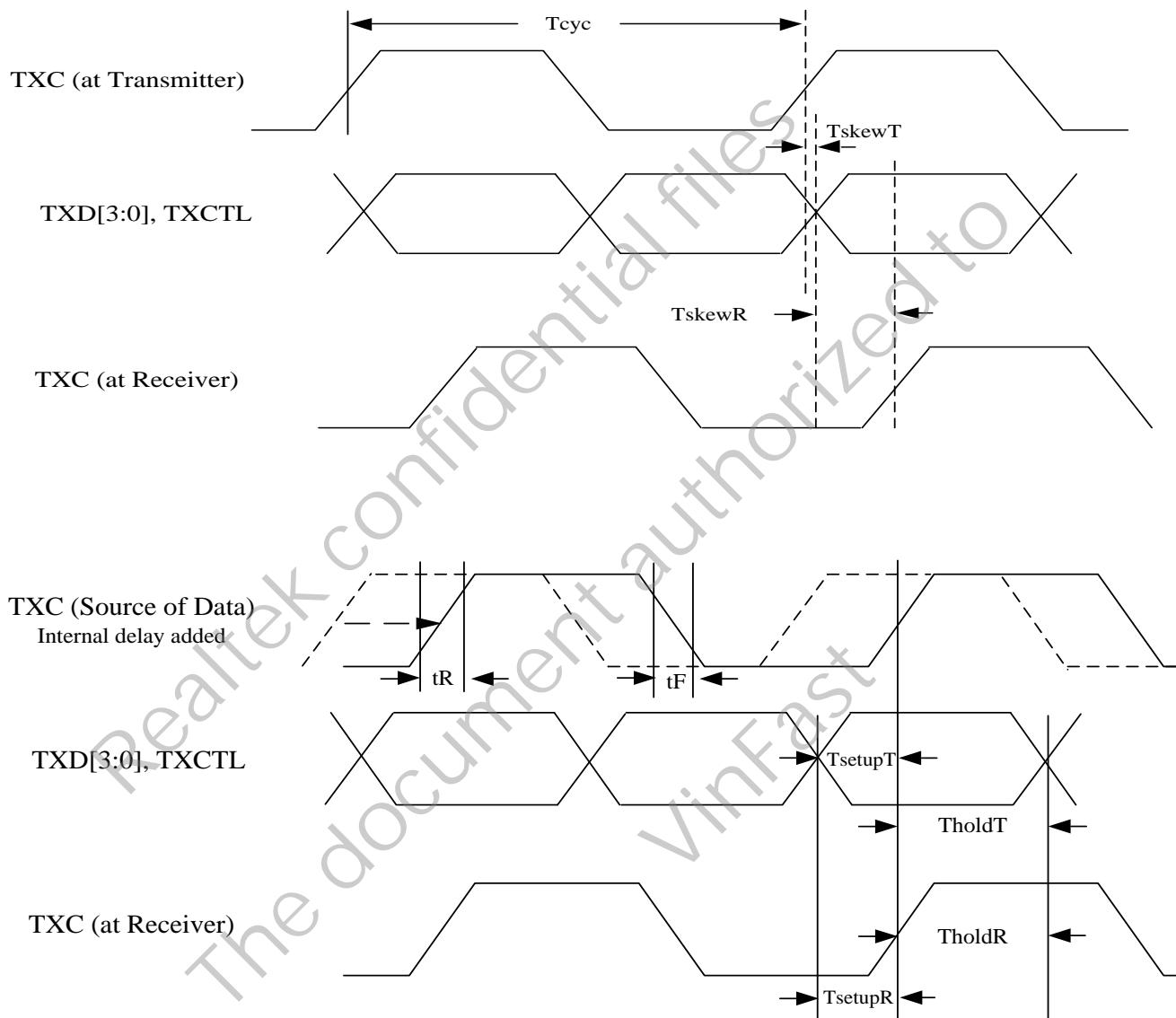


Figure 88. RGMII Timing for TXC

Figure 89 shows the effect of adding an additional delay to RXC by PC board (upper side) or by transmitter internally (lower side) in RGMII mode.

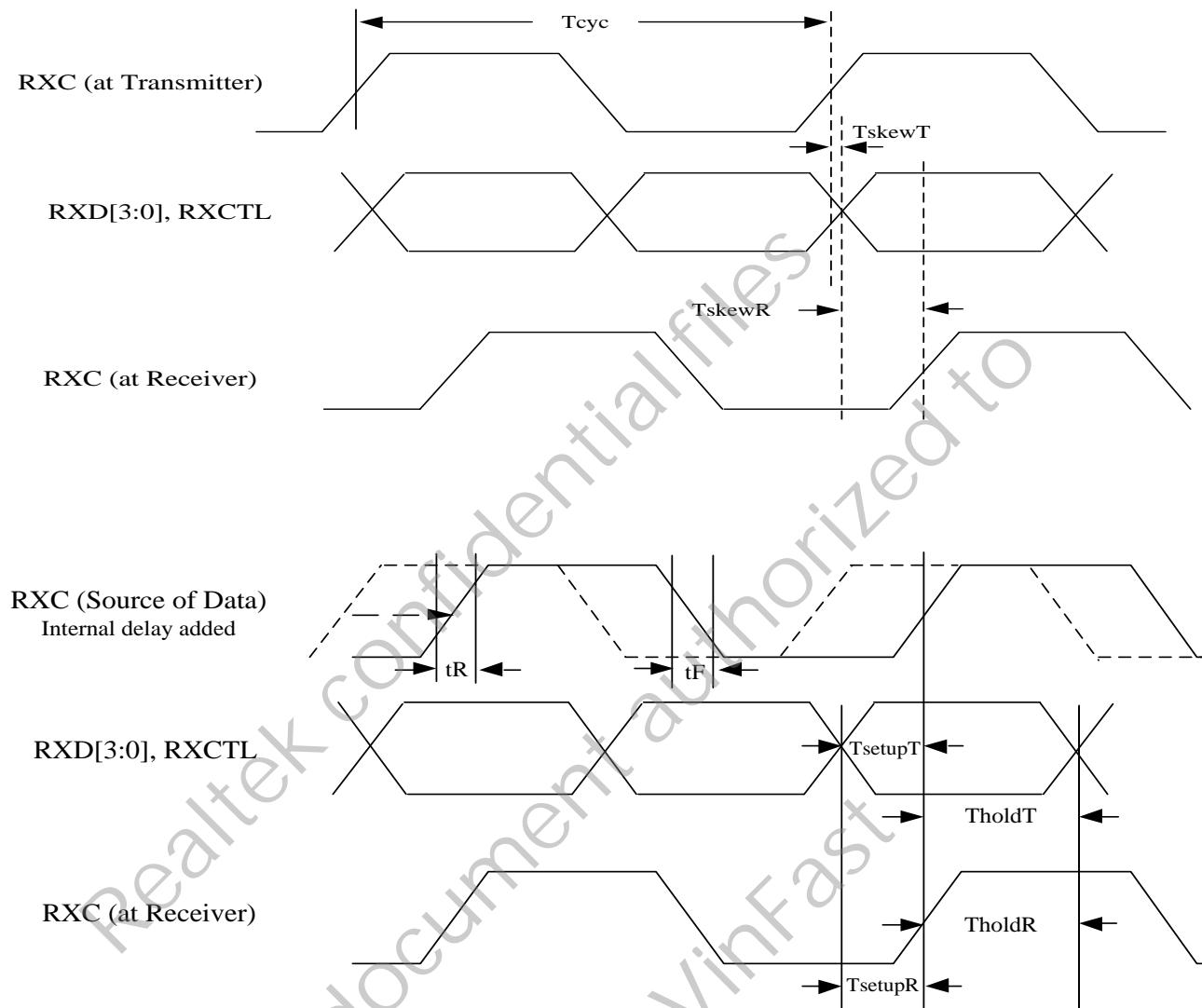


Figure 89. RGMII Timing for RXC

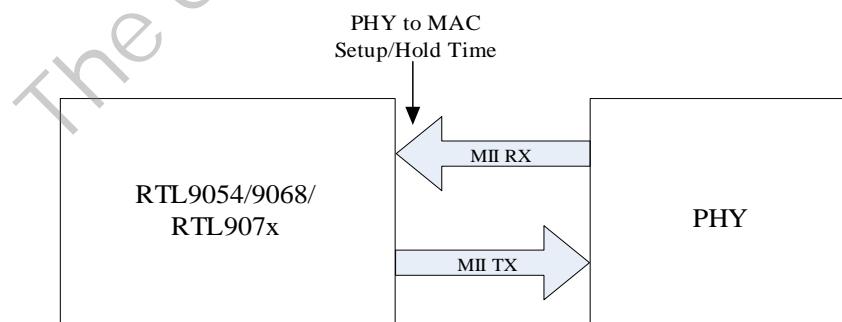
Table 70. RGMII Timing Parameter

Symbol	Description	Min	Typ.	Max	Units
Tcyc	Clock Cycle Duration 1000 Mbps	7.2	8	8.8	ns
	Clock Cycle Duration 100 Mbps	36	40	44	ns
	Clock Cycle Duration 10 Mbps	360	400	440	ns
Duty_T *	Duty Cycle 1000 Mbps	45	50	55	%
	Duty Cycle 100 Mbps	40	50	60	%
	Duty Cycle 10 Mbps	40	50	60	%
tR	TXC/RXC Rise Time (20% ~ 80%)	-	-	0.75	ns
tF	TXC/RXC Fall Time (20% ~ 80%)	-	-	0.75	ns
TsetupT	Data to Clock Output Setup Time at Transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TholdT	Clock to Data Output Hold Time at Transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TsetupR	Data to Clock Input Setup Time at Receiver (with delay integrated at transmitter)	1	2	-	ns
TholdR	Clock to Data Input Hold Time at Receiver (with delay integrated at transmitter)	1	2	-	ns
TskewT **	Data to Clock Output Skew Time at Transmitter (without delay integrated)	-0.5	0	0.5	ns
TskewR **	Data to Clock Input Skew Time at Receiver (with PCB delay integrated) This implies that the PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal.	1	1.8	2.6	ns

*Note: The duty cycle may be stretched / shrunk during speed changes or while transitioning to a received packet's clock domain as long as the minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

9.8.2. MII/RMII Timing

Figure 90 shows an example of a packet transferred from PHY to MAC on the MII interface.


Figure 90. MII Interface Setup/Hold Time Definitions

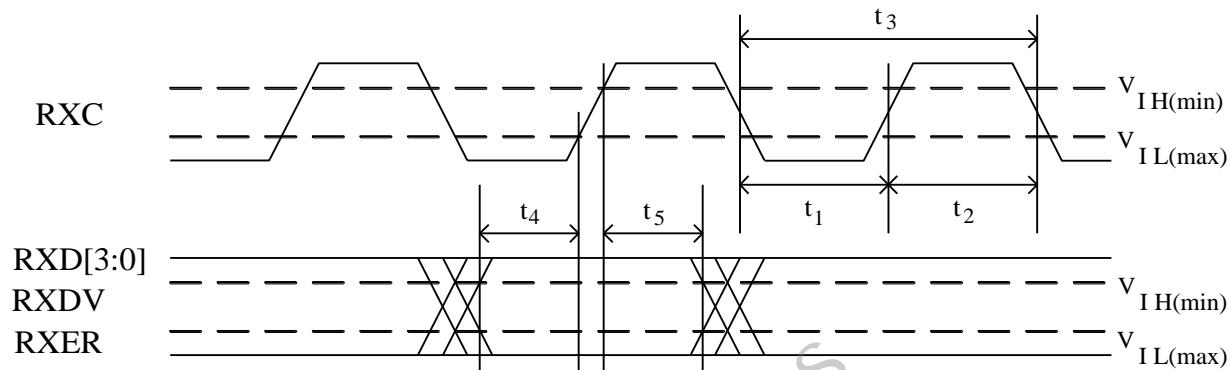


Figure 91. Reception Data Timing of MII Interface

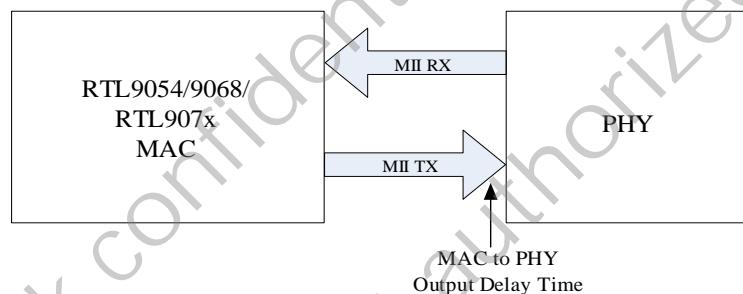


Figure 92. MII Interface Output Delay Time Definitions

The above figure shows another example of a packet transferred from MAC to PHY on the MII interface.

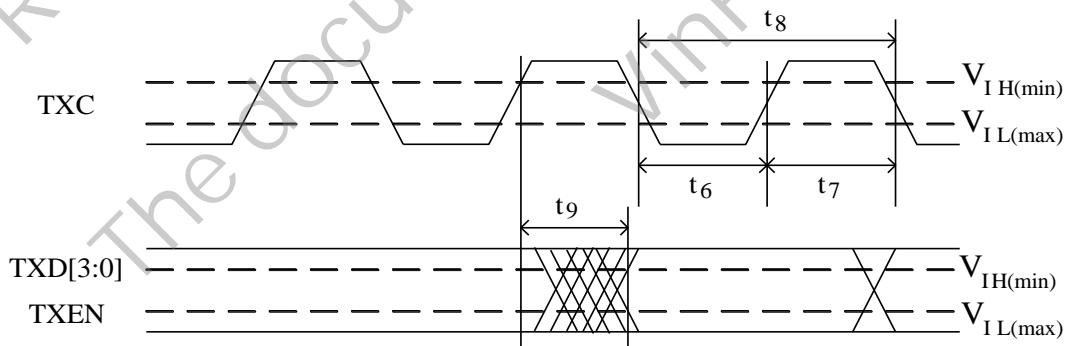
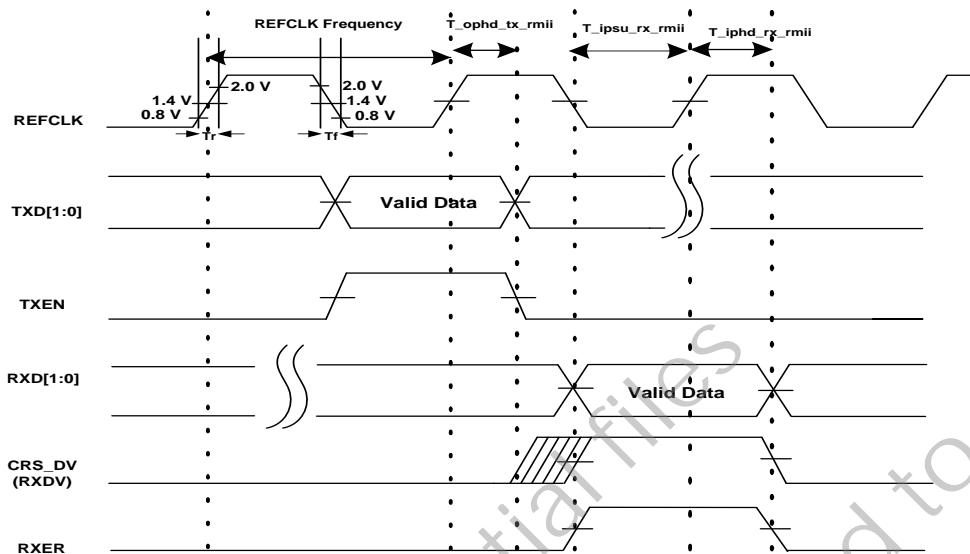


Figure 93. Transmission Data Timing of MII Interface


Figure 94. Transmission Data Timing of RMII Interface
Table 71. MII/RMII Timing

Parameter	SYM	Description	I/O	Min	Typ.	Max	Units
MII Reception Timing							
RXC Duty Cycle	t ₁ , t ₂	RXC Duty Cycle	I	40	50	60	%
RXC Period	t ₃	RXC Period 100Mbps RXC Period 10Mbps	I	-	40	-	ns
RXER, RXDV, RXD[3:0] Setup to RXC Rising Edge	t ₄	RXER, RXDV, RXD[3:0] Setup to RXC Rising Edge	I	10	-	-	ns
RXER, RXDV, RXD[3:0] Hold After RXC Rising Edge	t ₅	RXER, RXDV, RXD[3:0] Hold After RXC Rising Edge	I	10	-	-	ns
MII Transmission Timing							
TXCLK Duty Cycle	t ₆ , t ₇	TXCLK Duty Cycle	O	40	50	60	%
TXCLK Period	t ₈	TXCLK Period 100Mbps TXCLK Period 10Mbps	O	-	40	-	ns
TXEN, TXD[0:3] Output Delay Time from TXC	t ₉	TXEN, TXD[0:3] Output Delay Time from TXC	O	0	-	25	ns
RMII Transmission and Reception Timing							
REFCLK Frequency	-	Frequency of Reference Clock	O	-	50	-	MHz
REFCLK Duty Cycle	-	Duty Cycle of Reference Clock	O	35	-	65	%
REFCLK Rise time	T _r	Rise time of Reference Clock	O	1	-	5	ns
REFCLK Fall time	T _f	Fall time of Reference Clock	O	1	-	5	ns
T _{ipsu_rx_rmii}	-	RXD[1:0]/RX_DV/RXER Setup Time to REFCLK	O	4	-	-	ns
T _{iphd_rx_rmii}	-	RXD[1:0]/RX_DV/RXER Hold Time from REFCLK	O	2	-	-	ns
T _{ophd_tx_rmii}	-	TXD[1:0]/TXEN Output Delay Time from REFCLK	I	2	-	-	ns

9.8.3. SGMII Timing

Table 72. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	800	-	ps	$800\text{ps} \pm 100\text{ppm}$
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	150	-	-	mV	-
T_Y2	Eye Mask	-	-	400	mV	-
V _{TX-DIFFp-p}	Output Differential Voltage	300	-	800	-	-
T _{TX-EYE}	Minimum Differential Width	0.7	-	-	UI	-
T _{TX-JITTER}	Output Jitter	-	-	0.3	UI	CDR BW = 1.25G/1667 @ 1st order
T _{TX-RISE}	Output Rise Time	0.125	-	0.25	UI	20% ~ 80%
T _{TX-FAIL}	Output Fail Time	0.125	-	0.25-	UI	20% ~ 80%
R _{TX}	Differential Resistance	80	100	120	ohm	-
C _{TX}	AC Coupling Capacitor	80	100	120	nF	-
L _{TX}	Transmit Length in PCB	-	-	10	inch	-

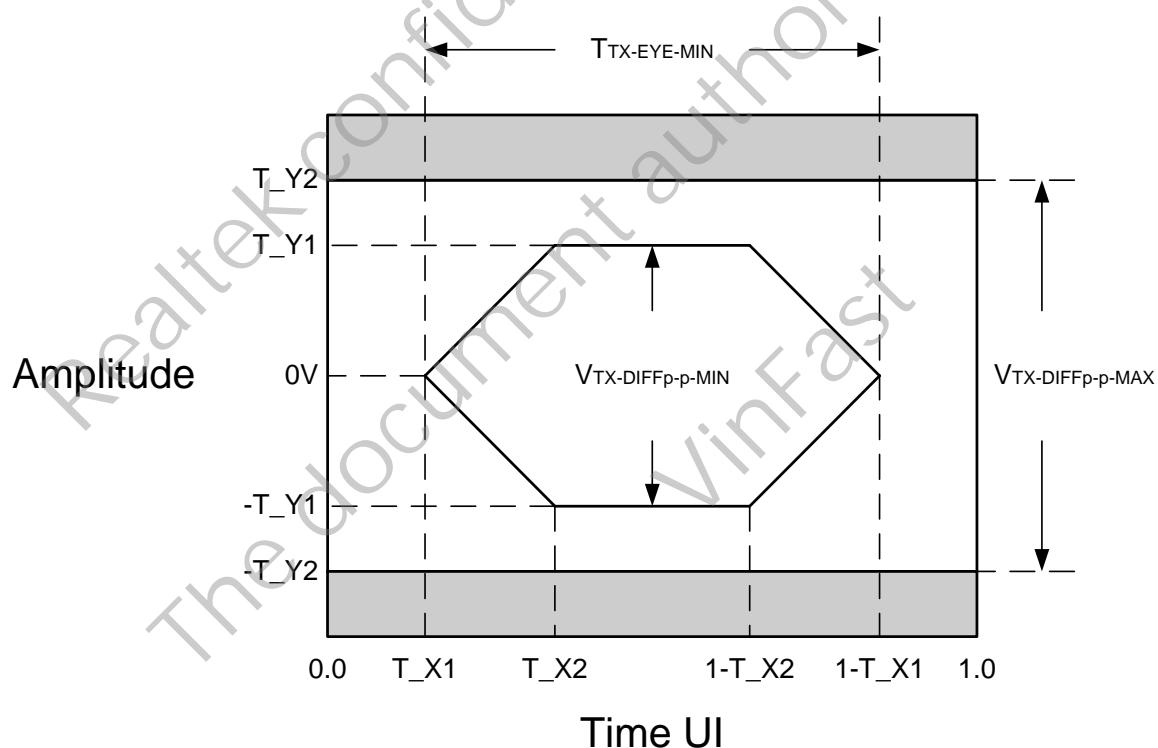
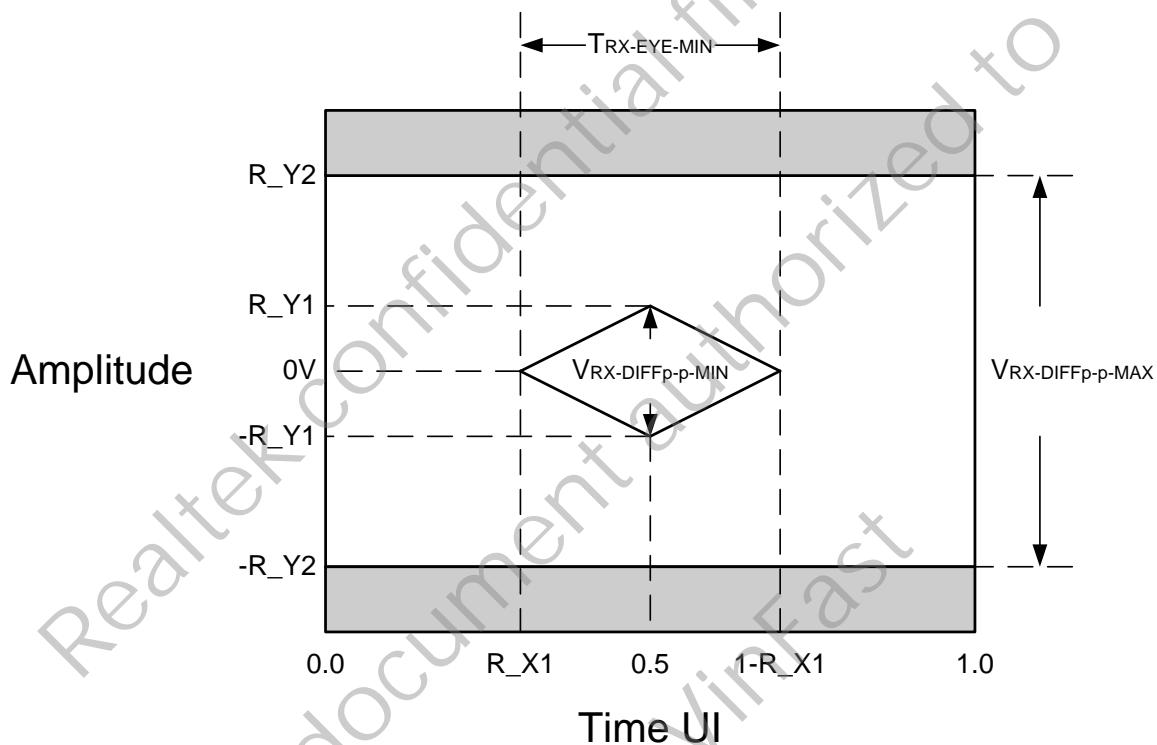


Figure 95. SGMII Differential Transmitter Eye Diagram

Table 73. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	800	-	ps-	800ps ±100ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
V _{RX-DIFFp-p}	Input Differential Voltage	100	-	800	mV	-
T _{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-
T _{RX-JITTER}	Input Jitter Tolerance	-	-	0.6	UI	-
R _{RX}	Differential Resistance	80	100	120	ohm	-


Figure 96. SGMII Differential Receiver Eye Diagram

9.8.4. HSGMII Timing

Table 74. HSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	320	-	ps	$320\text{ps} \pm 100\text{ppm}$
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	150	-	-	mV	-
T_Y2	Eye Mask	-	-	400	mV	-
V _{TX-DIFFp-p}	Output Differential Voltage	300	-	800	-	-
T _{TX-EYE}	Minimum Differential Width	0.7	-	-	UI	-
T _{TX-JITTER}	Output Jitter	-	-	0.3	UI	CDR BW = 3.125G/1667 @1st order
T _{TX-RISE}	Output Rise Time	0.125	-	0.25	UI	20% ~ 80%
T _{TX-FAIL}	Output Fail Time	0.125	-	0.25-	UI	20% ~ 80%
R _{TX}	Differential Resistance	80	100	120	ohm	-
C _{TX}	AC Coupling Capacitor	80	100	120	nF	-
L _{TX}	Transmit Length in PCB	-	-	5	inch	-

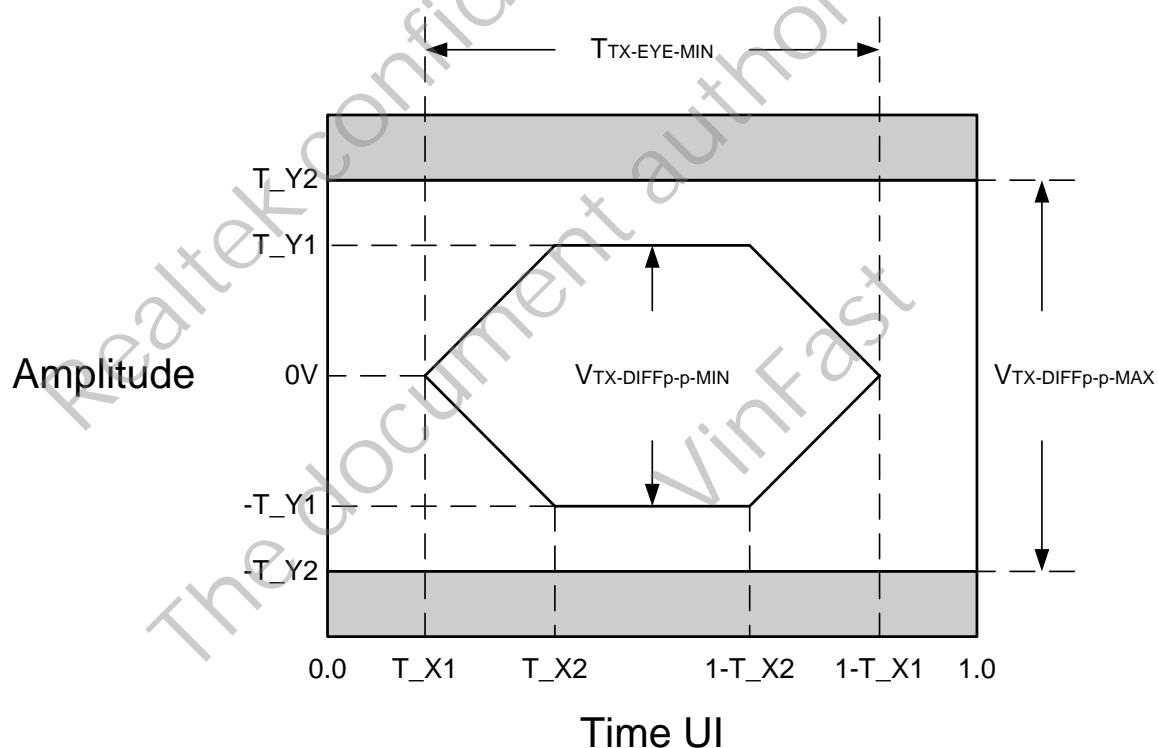
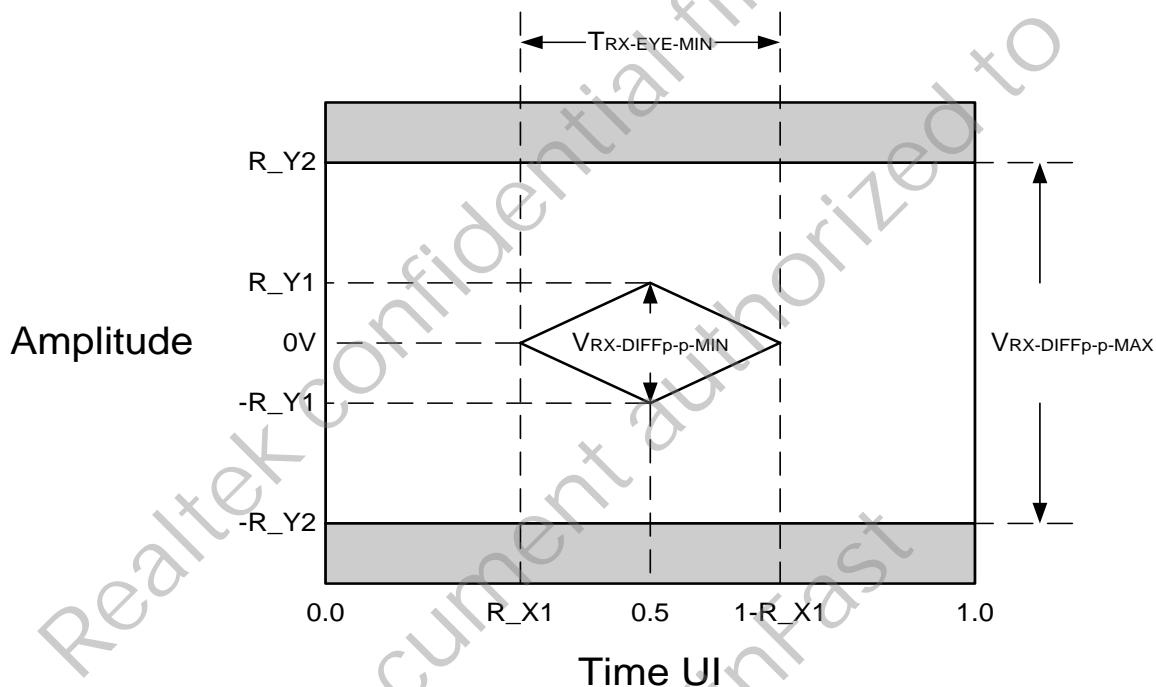


Figure 97. HSGMII Differential Transmitter Eye Diagram

Table 75. HSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	320	-	ps-	$320\text{ps} \pm 100\text{ppm}$
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
V_RX-DIFFp-p	Input Differential Voltage	100	-	800	mV	-
T_RX-EYE	Minimum RX Eye Width	0.4	-	-	UI	-
T_RX-JITTER	Input Jitter Tolerance	-	-	0.6	UI	-
R_RX	Differential Resistance	80	100	120	ohm	-


Figure 98. HSGMII Differential Receiver Eye Diagram

9.8.5. USXGMII Timing

Table 76. USXGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	193.94	-	ps	$193.94\text{ps} \pm 100\text{ppm}$
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
V _{TX-DIFFp-p}	Output Differential Voltage	400	700	900	-	-
T _{TX-EYE}	Minimum Differential Width	0.7	-	-	UI	-
T _{TX-JITTER}	Output Jitter	-	-	0.4	UI	Test method: 1) Use eye mask as jitter peak to peak histogram 2) CDR Bandwidth: 1st 5.15625G/1667 3) Memory Depth: 1M 4) Sampling Rate: 20Gs/s 5) UI: > 1MUI
T _{TX-RISE}	Output Rise Time	0.15	-	-	UI	20% ~ 80%
T _{TX-FAIL}	Output Fail Time	0.15	-	-	UI	20% ~ 80%
R _{TX}	Differential Resistance	80	100	120	ohm	-
C _{TX}	AC Coupling Capacitor	80	100	120	nF	-
L _{TX}	Transmit Length in PCB	-	-	5	inch	-

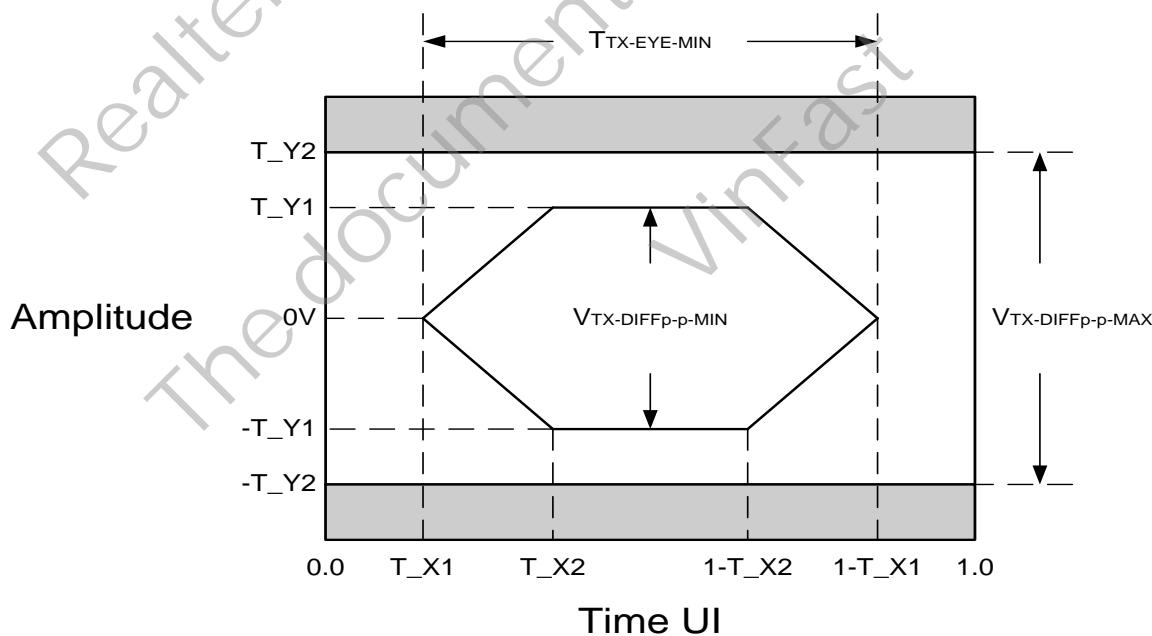
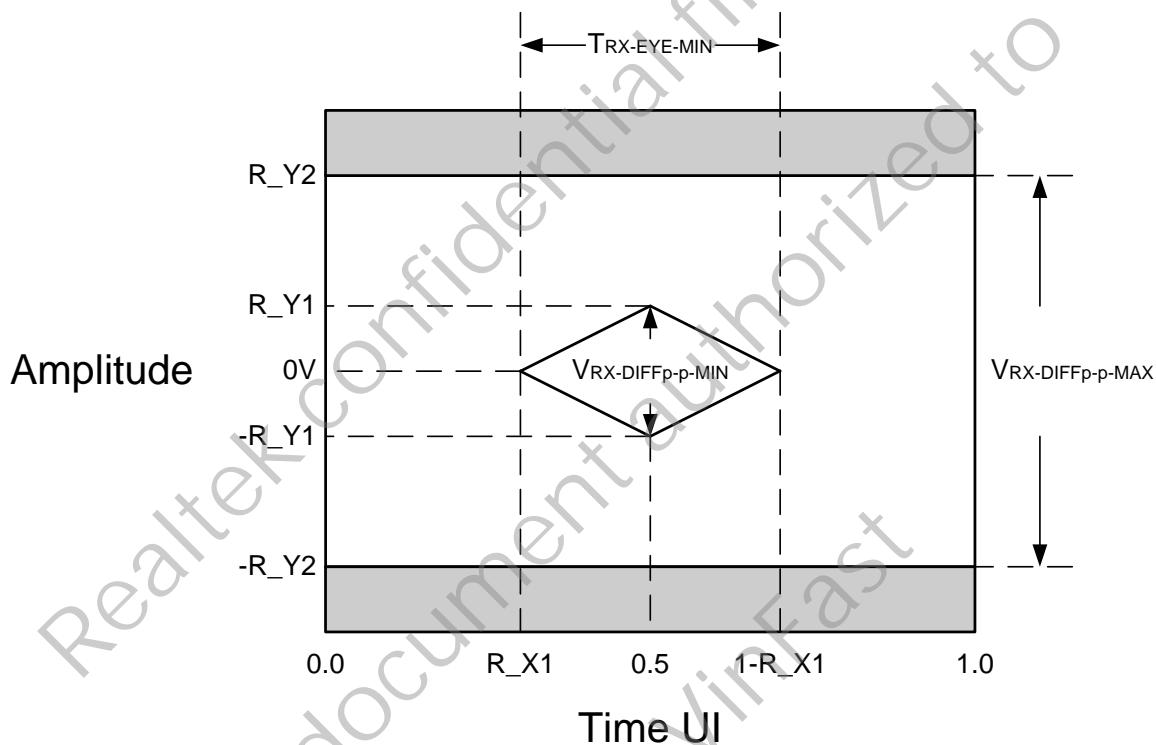


Figure 99. USXGMII Differential Transmitter Eye Diagram

Table 77. USXGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Note
UI	Unit Interval	-	193.94	-	ps-	$193.94\text{ps} \pm 100\text{ppm}$
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
V_RX-DIFFp-p	Input Differential Voltage	200	-	1200	mV	-
T_RX-EYE	Minimum RX Eye Width	0.4	-	-	UI	-
T_RX-JITTER	Input Jitter Tolerance	-	-	0.6	UI	-
R_RX	Differential Resistance	80	100	120	ohm	-


Figure 100. USXGMII Differential Receiver Eye Diagram

9.8.6. SPI Master Interface Timing

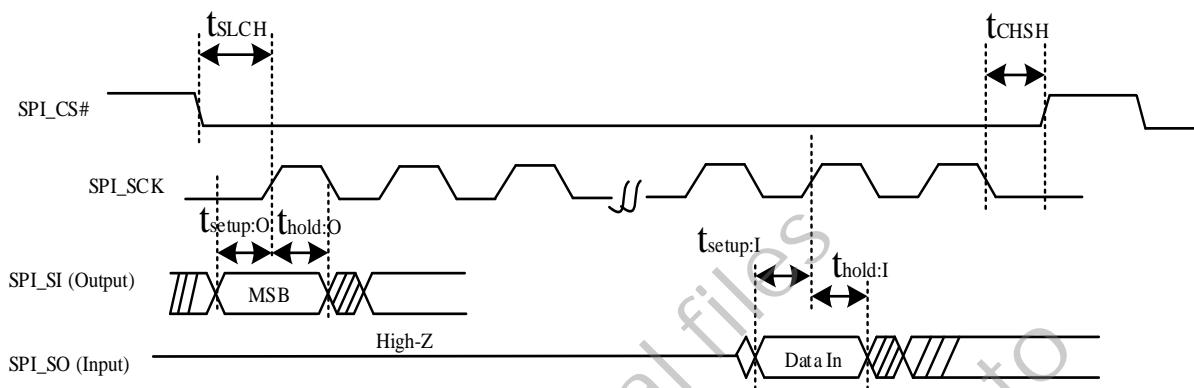


Figure 101. SPI Interface Timing

Table 78. SPI Master Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
fSPI_SCK	Clock Frequency of the SPI_SCK.	12.5	-	100	MHz
Duty	Duty Cycle of the SPI_SCK.	-	50	-	%
tSLCH	CS# Active Setup Time.	-	1/(2 × SPI_SCK)	-	us
tCHSH	CS# Active Hold Time.	-	1/SPI_SCK	-	us
tsetup:O	Data Output Setup Time.	-	1/(2 × SPI_SCK)	-	us
thold:O	Data Output Hold Time.	-	1/(2 × SPI_SCK)	-	us
tsetup:I	Data Input Setup Time.	3	-	-	ns
thold:I	Data Input Hold Time.	1/(2 × SPI_SCK)	-	-	us

9.8.7. I2C Slave for External CPU Access Timing

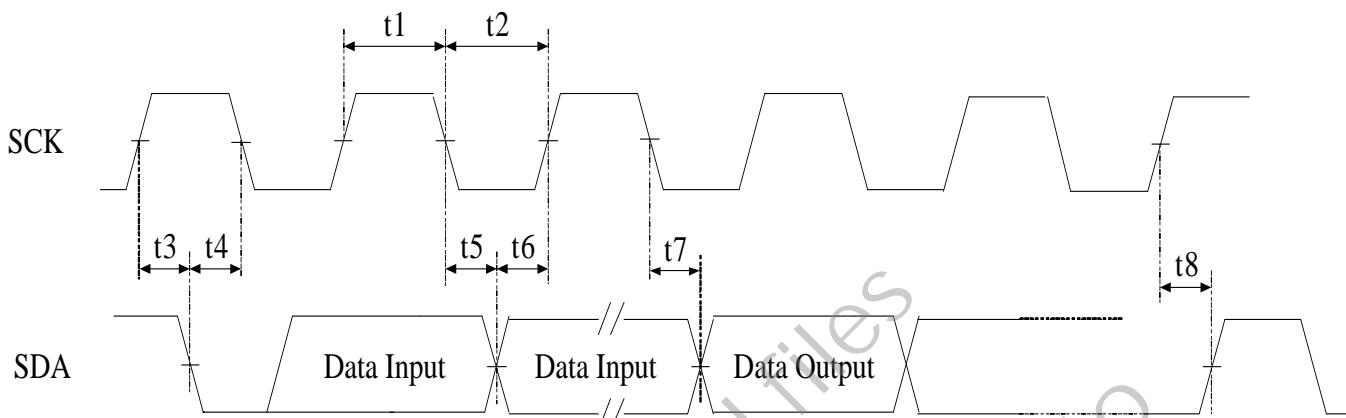


Figure 102. External CPU Access Timing

Table 79. External CPU Access Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
t1	SCK High Time.	50	-	-	ns
t2	SCK Low Time.	50	-	-	ns
t3	START Condition Setup Time.	34	-	-	ns
t4	START Condition Hold Time.	33	-	-	ns
t5	Data Hold Time.	0	-	-	ns
t6	Data Setup Time.	18	-	-	ns
t7	Clock to Data Output Delay.	42	-	-	ns
t8	STOP Condition Setup Time.	34	-	-	ns

9.8.8. MDC/MDIO Slave for External CPU Access Timing

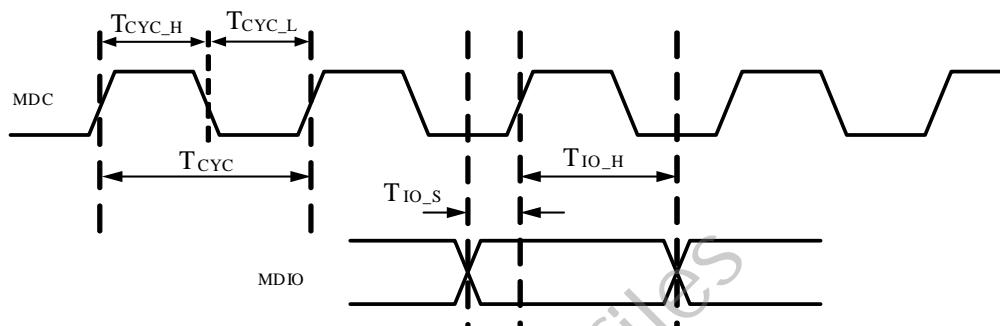


Figure 103. MDC/MDIO Write Operation Timing

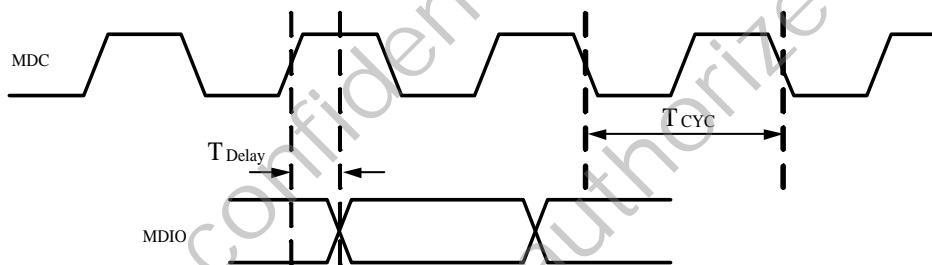


Figure 104. MDC/MDIO Read Operation Timing

Table 80. External CPU Access Timing Characteristics

Parameter	SYM	Condition	Min	Typ.	Max	Units
MDC Clock Input Cycle	T_CYC	MDC Clock Input Cycle	80	-	-	ns
MDC Clock High Time	T_CYC_H	MDC Clock High Time	40	-	-	ns
MDC Clock Low Time	T_CYC_L	MDC Clock Low Time	40	-	-	ns
MDIO to MDC Rising Input Setup Time	T_IO_S	MDIO to MDC Rising Input Setup Time	10	-	-	ns
MDIO to MDC Rising Input Hold Time	T_IO_H	MDIO to MDC Rising Input Hold Time	10	-	-	ns
MDIO Output Delay	T_Delay	MDC to MDIO Rising Output Delay	0	40	60	ns

9.8.9. SPI Slave Interface Timing

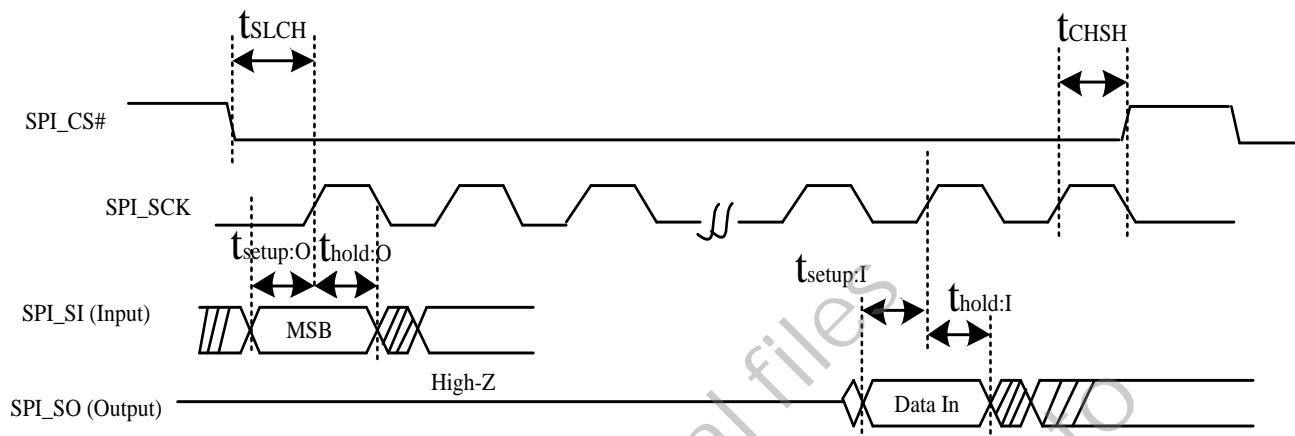


Figure 105. SPI Interface Timing

Table 81. SPI Slave Interface Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
fSPI_SCK	Clock Frequency of the SPI_SCK.	-	-	25	MHz
Duty	Duty Cycle of the SPI_SCK.	47	50	53	%
tSLCH	CS# Active Setup Time.	15	-	-	ns
tCHSH	CS# Active Hold Time.	15	-	-	ns
tsetup: O	Data Output Setup Time.	15	-	-	ns
thold: O	Data Output Hold Time.	16	-	-	ns
tsetup: I	Data Input Setup Time.	6	-	-	ns
thold: I	Data Input Hold Time.	0	-	-	ns

9.9. PCI Express Bus Parameters

Table 82. 100MHz input REFCLK Parameters

Symbol	Parameter	Min	Max	Units	Note
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	$2*(V_{CROSS})$	-	mV	2
V_{IL}	Differential Input Low Voltage	-	$-2*(V_{CROSS})$	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1
V_{MIN}	Absolute Minimum Input Voltage	-0.1	0.1	V	1
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1

Note 1: Measurement taken from single-ended waveform.

Note 2: Measurement taken from differential waveform.

Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK- (see Figure 1).

Note 5: Refer to PCI Express Card Electromechanical Specification, rev.3.0, for the correct measurement environment setting of each parameter.

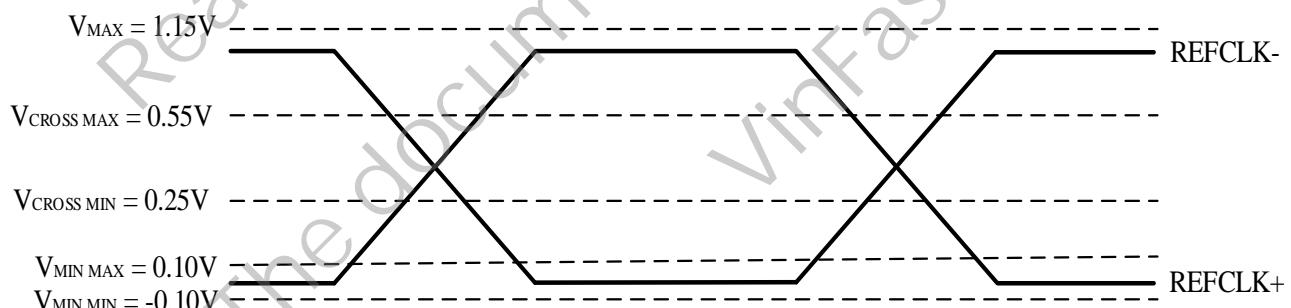


Figure 106. Single-Ended Measurement Points for Absolute Cross Point and Swing

Table 83. Differential Transmitter Parameters

Parameter	Description	Gen1			Gen2			Gen3			Units
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	124.9625	125	125.0375	ps
TTXA ¹	Min Eye Width	287	-	-	123	-	-	41.25 ^{2,3}	-	-	ps

Parameter	Description	Gen1			Gen2			Gen3			Units
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
JTXA-MEDIAN-to-MAX-JITTER ¹	Maximum median-to-max jitter	-	-	56.5	-	-	-	-	-	-	ps
VTXA	Transition bits differential peak-peak output voltage	514	-	1200	380	-	1200	34 ^{2,3}	-	1200	mV
VTXA_d	Non-Transition bits differential peak-peak output voltage	360	-	1200	380	-	1200	34 ^{2,3}	-	1200	mV
ZTX-DIFF-DC	DC Differential TX Impedance	80	100	120	-	100	120	-	100	120	Ω
CTX	AC Coupling Capacitor	75	-	265	75	-	265	176	220	265	nF

Note 1: The recommended sample size for this measurement is at least 106 UI.

Note 2: The values are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel.

Note 3: The eye diagram requirements are evaluated after the behavioral CDR defined in the PCI Express Base Specification, Revision 3.0, Section 4.4.2.1.3 and the behavioral RX Equalization Algorithm defined in the PCI Express Base Specification, Revision 3.0, Section 4.4.2.1.4 are applied.

Note 4: Refer to PCI Express Card Electromechanical Specification, rev.3.0, for the correct measurement environment setting of each parameter.

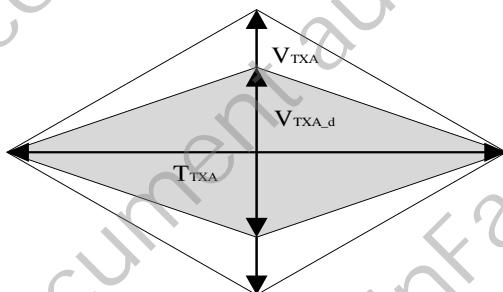


Figure 107. Add-in Card Transmitter Path Compliance Eye Diagram

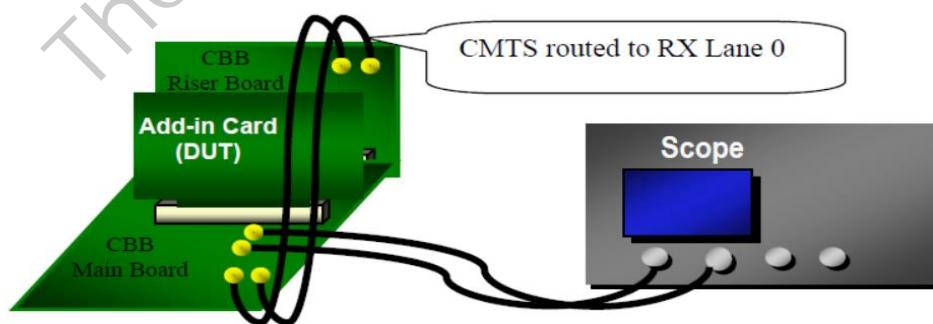


Figure 108. Transmitter Compliance Test Using the CBB3.0

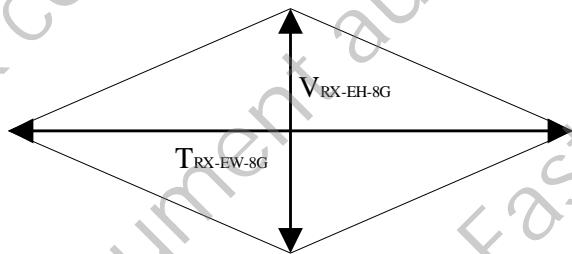
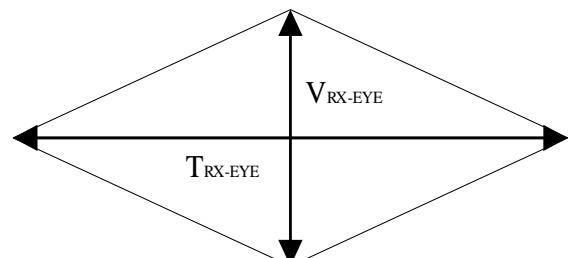
Table 84. Differential Receiver Parameters

Parameter	Description	Gen1			Gen2			Gen3			Unit
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	124.962	125	125.037	ps
T_{RX-EYE}^2	Eye Width at TP2	0.4	-	-	0.32	-	-	-	-	-	UI
$T_{RX-EW-8G}^{1,3}$	Eye Width at TP2P	-	-	-	-	-	-	0.33	-	-	UI
V_{RX-EYE}^2	Eye Height at TP2	238	-	1200	100	-	1200	-	-	-	mV
$V_{RX-EH-8G}^{1,3}$	Eye Height at TP2P	-	-	-	-	-	-	34	-	-	mV
$Z_{RX-DIFF-DC}^2$	DC differential impedance	80	100	120	-	-	-	-	-	-	Ω

Note 1: $V_{RX-EH-8G}$ and $T_{RX-EW-8G}$ are referenced to TP2P and are obtained after post processing data captured at TP2. $V_{RX-EH-8G}$ and $T_{RX-EW-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.

Note 2: Refer to PCI Express Base Specification, rev.3.0, for the correct measurement environment setting of each parameter.

Note 3: Refer to PCI Express Card Electromechanical Specification, rev.3.0, for the correct measurement environment setting of each parameter.


Figure 109. Gen3 Add-in Card Receiver Path TP2P Eye Diagram

Figure 110. Gen1 and Gen2 Add-in Card Receiver Path TP2 Eye Diagram

10. Thermal Characteristics

10.1.1. PCB Descriptions

Table 85. PCB Descriptions for LFBGA 20.2x20.2

Dimension (L×W)	101.5 x 114.5 mm ²
Thickness	1.6 mm
PCB Layer	4

Table 86. PCB Descriptions for LFBGA 17x17

Dimension (L×W)	101.5 x 114.5 mm ²
Thickness	1.6 mm
PCB Layer	4

10.1.2. Condition Descriptions

Table 87. Condition Descriptions for LFBGA 20.2x20.2

Max. Power	3524 mW
Control Condition	Air Flow = 0,100,200,400 (ft/min)

Table 88. Condition Descriptions for LFBGA 17x17

Max. Power	3088 mW
Control Condition	Air Flow = 0,100,200,400 (ft/min)

10.1.3. Thermal Characteristics Results

Table 89. Thermal Characteristics Results for LFBGA 20.2x20.2

Ambient Temperature (°C)	105			
Air Flow (ft/ms)	0	100	200	400
T_J (°C)	149.17	145.31	143.25	140.73
θ_{JA} (°C/W)	12.42	11.34	10.76	10.06
ψ_{JT} (°C/W)	2.22	2.26	2.28	2.31
ψ_{JB} (°C/W)	4.77	4.71	4.67	4.62
θ_{JB} (°C/W)	4.81			
θ_{JC} (°C/W)	4			
Max. Junction Temperature (°C)	150			

Note:

θ_{JA}: Junction-to-ambient thermal resistance.

ψ_{JT}: Junction-to-top-center thermal characterization parameter.

ψ_{JB}: Junction-to-board thermal-characterization parameter.

θ_{JB}: Junction-to-board thermal resistance.

θ_{JC}: Junction-to-case thermal resistance.

Table 90. Thermal Characteristics Results for LFBGA 17x17

Ambient Temperature (°C)	105			
Air Flow (ft/ms)	0	100	200	400
T _J (°C)	150.11	147.45	145.49	143.29
θ _{JA} (°C/W)	14.62	13.65	13.02	12.31
ψ _{JT} (°C/W)	2.919	2.965	2.992	3.032
ψ _{JB} (°C/W)	6.595	6.511	6.459	6.381
θ _{JB} (°C/W)	6.576			
θ _{JC} (°C/W)	5.058			
Max. Junction Temperature (°C)	150			

Note:

θ_{JA}: Junction-to-ambient thermal resistance.

ψ_{JT}: Junction-to-top-center thermal characterization parameter.

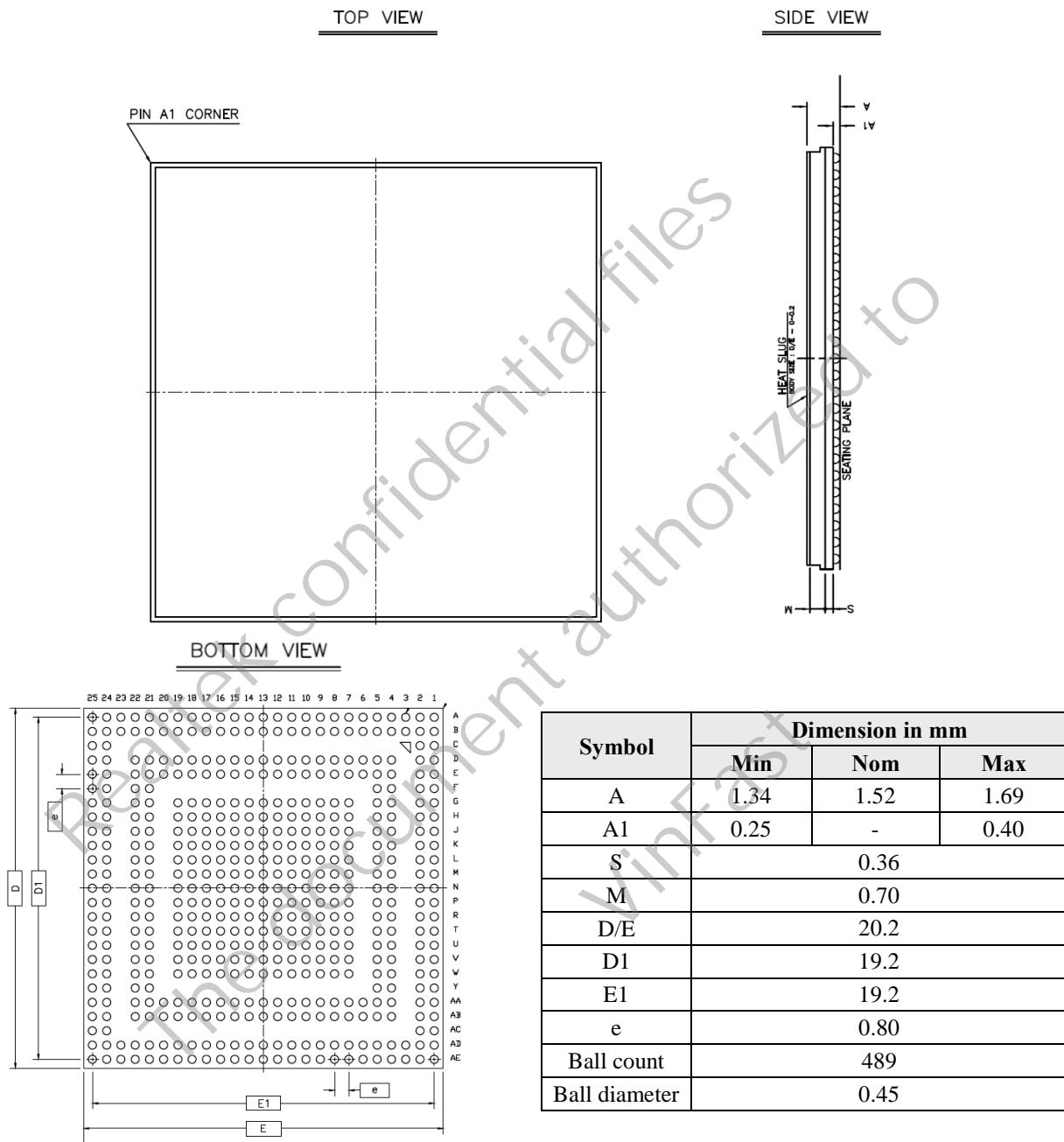
ψ_{JB}: Junction-to-board thermal-characterization parameter.

θ_{JB}: Junction-to-board thermal resistance.

θ_{JC}: Junction-to-case thermal resistance.

11. Mechanical Dimensions

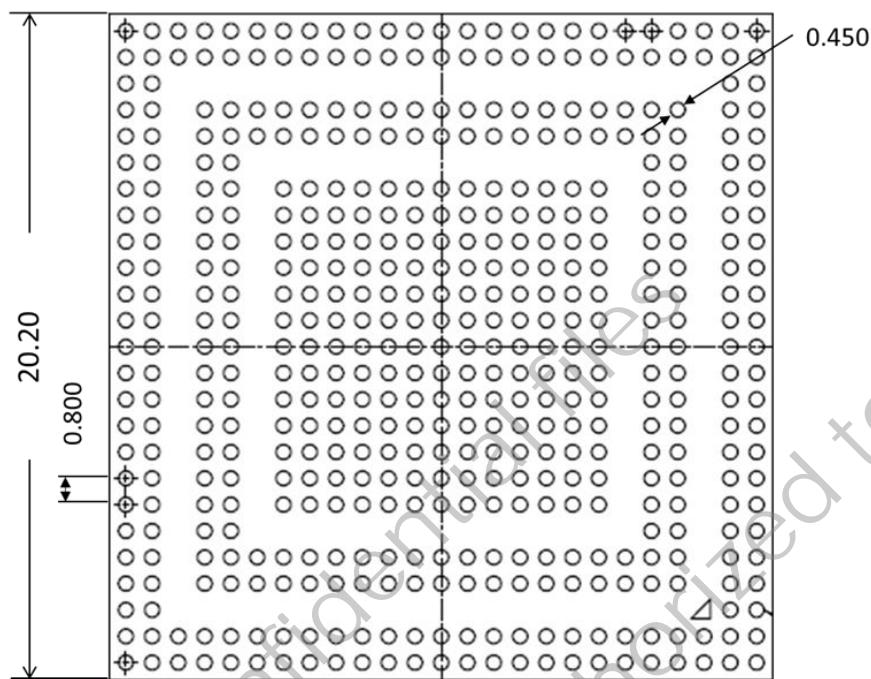
11.1. 489L LFBGA 20.2 x 20.2



Notes:

1. Controlling Dimension: Millimeter(mm)
2. Reference Document: JEDEC MO-219

11.1.1. PCB OUTLINE



PCB Design:

Note 1:

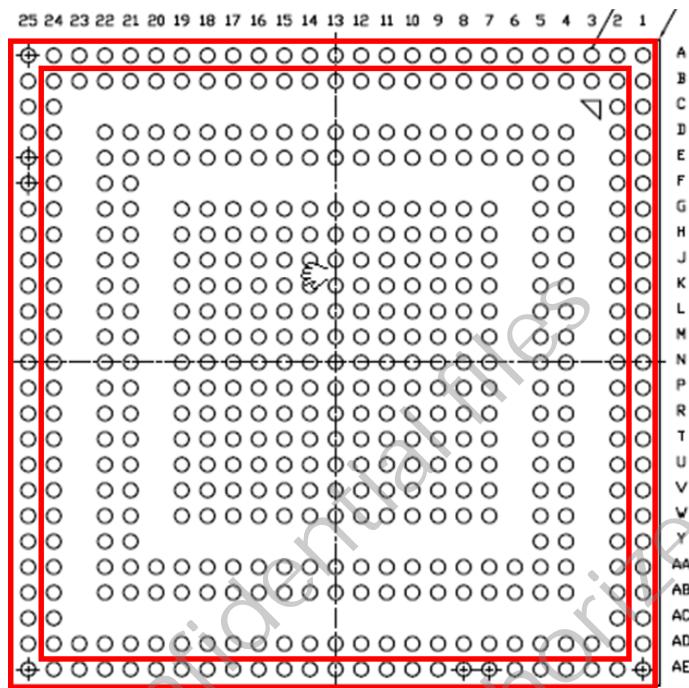
- a. Pitch: 0.8mm
- b. Ball Diameter: 0.45mm

Note 2:

- a. Non solder masks defined is preferred
- b. Controlling Dimension: Millimeter(mm)
- c. Reference Document: IPC-7351

Note 3: Recommend to use underfill in SMT process.

11.1.2. STENCIL DESIGN



Stencil Design:

Note 1:

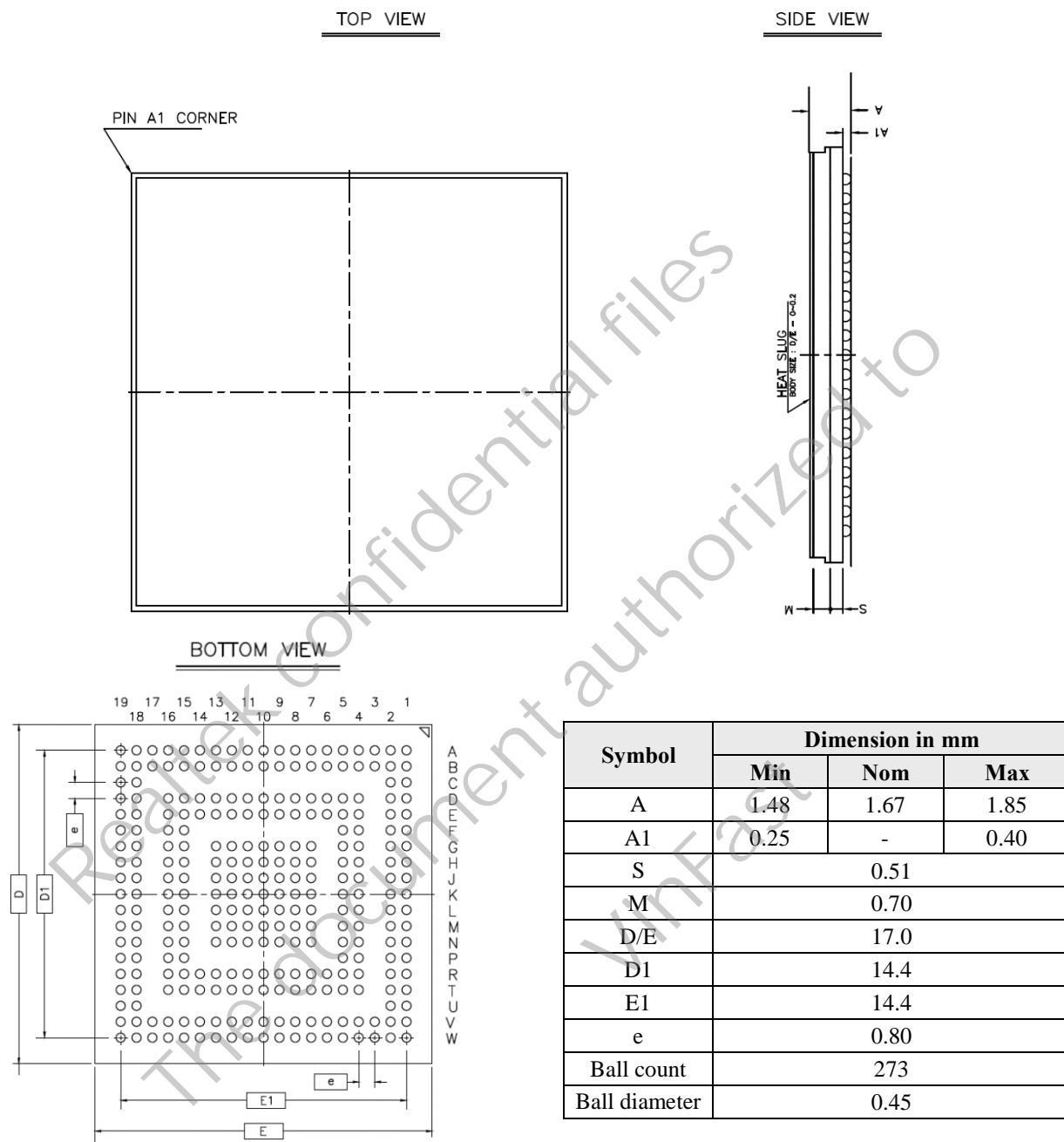
- a. Pitch: 0.8mm
- b. Ball Diameter: 0.45mm
- c. Opening dimension for stencil in red area: 0.50mm; in other area: 0.40mm

Note 2:

- a. Controlling Dimension: Millimeter(mm)
- b. Base on 0.1mm thick stencil
- c. Reference Document: IPC-7525

Note 3: Recommend to use underfill in SMT process.

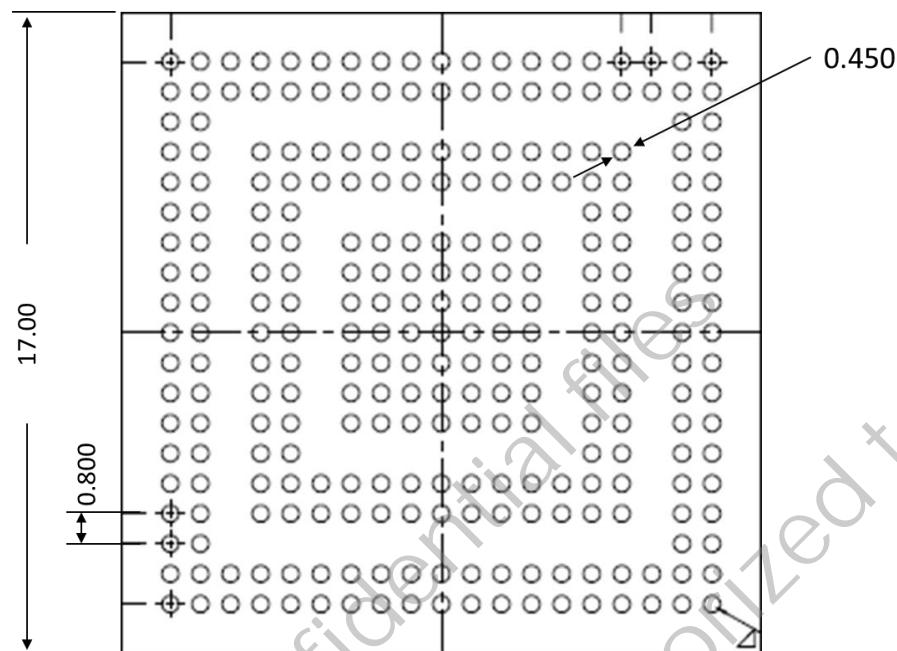
11.2. 273L LFBGA 17x17



Notes:

1. Controlling Dimension: Millimeter(mm)
2. Reference Document: JEDEC MO-219

11.2.1. PCB OUTLINE



PCB Design

Note 1:

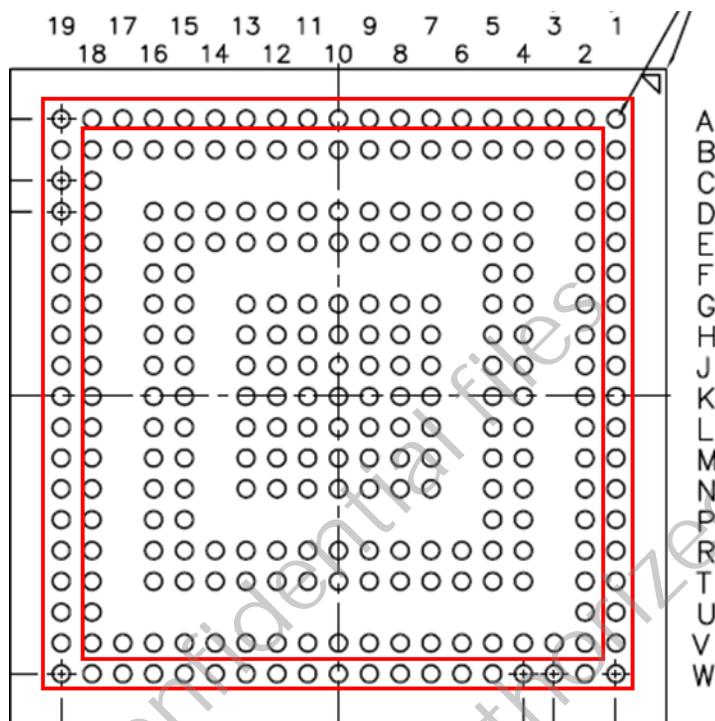
- a. Pitch: 0.8mm
- b. Ball Diameter: 0.45mm

Note 2:

- a. Non solder masks defined is preferred
- b. Controlling Dimension: Millimeter(mm)
- c. Reference Document: IPC-7351

Note 3: Recommend to use underfill in SMT process.

11.2.2. STENCIL DESIGN



Stencil Design:

Note 1:

- a. Pitch: 0.8mm
- b. Ball Diameter: 0.45mm
- c. Opening dimension for stencil in red area: 0.50mm; in other area: 0.40mm

Note 2:

- a. Controlling Dimension: Millimeter(mm)
- b. Base on 0.1mm thick stencil
- c. Reference Document: IPC-7525

Note 3: Recommend to use underfill in SMT process.

12. Ordering Information

Table 91. Ordering Information

Part Number	Package type	Packing type	Status	Weight (g)
RTL9075AAD-VA-CG	489L LFBGA with 'Green' Package	Tray	MP	1.545
RTL9072AAD-VA-CG	489L LFBGA with 'Green' Package	Tray	MP	1.545
RTL9068AAD-VA-CG	489L LFBGA with 'Green' Package	Tray	MP	1.545
RTL9068ABD-VA-CG	273L LFBGA with 'Green' Package	Tray	MP	1.187
RTL9068ABD-VA1-CG	273L LFBGA with 'Green' Package	Tray	MP	1.187
RTL9054AN-VA-CG	489L LFBGA with 'Green' Package	Tray	ES	1.563
RTL9075AAD-VA-CGT	489L LFBGA with 'Green' Package	Tape & Reel	ES	1.545
RTL9072AAD-VA-CGT	489L LFBGA with 'Green' Package	Tape & Reel	ES	1.545
RTL9068AAD-VA-CGT	489L LFBGA with 'Green' Package	Tape & Reel	ES	1.545
RTL9068ABD-VA-CGT	273L LFBGA with 'Green' Package	Tape & Reel	ES	1.187
RTL9068ABD-VA1-CGT	273L LFBGA with 'Green' Package	Tape & Reel	ES	1.187
RTL9054AN-VA-CGT	489L LFBGA with 'Green' Package	Tape & Reel	ES	1.563
MSL (Moisture Sensitivity Level)			Level 3	-

Note: See section 5 for package identification.

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