

# REALTEK

**RTL9000AA-VC  
RTL9000AN-VC**

## **INTEGRATED PRECISION AUTOMOTIVE PHY WITH 100BASE-T1 TRANSCEIVER**

**PRELIMINARY DATASHEET**  
**(CONFIDENTIAL: Development Partners Only)**

**Rev. 1.4  
2017-08-25**



**Realtek Semiconductor Corp.**  
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan  
Tel.: +886-3-578-0211. Fax: +886-3-577-6047  
[www.realtek.com](http://www.realtek.com)

## COPYRIGHT

© 2015 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

## DISCLAIMER

Realtek provides this document ‘as is’, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

## TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

## USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## REVISION HISTORY

Revision	Release Date	Summary
Draft 1.0	2016/12/21	Draft First Release
Draft1.1	2017/03/21	Revised 10.4. Power Dissipation Revised 7.13 Realtek Cable Test Diagnostics Revised 7.15.UNH IOL Test Revised 8.2.5.PHYCR (PHY Control Register, Address 0x09) Revised Table 97. Digital IO Characteristics Revised the 7.3 Wake up Change the order of Operating Modes, Sleep Mechanism and Wake up as 7.3 Operating Modes, 7.4 Sleep Mechanism and 7.5 Wake up Added the MSL and Weight into the 12. Ordering Information
Draft1.2	2017/04/25	Moved the 7.11 to 7.13 Revised 7.12. Realtek Cable Test Diagnostics (RTCT) Revised 7.15 UNH IOL Test Revised Table 9. Hardware Strapping Configuration Revised Table15. Configuration Register Definitions Revised Table 35. LKTCR (Link Timer Control Register, Page 0xa42, Address 0x16) Added Table 90 Parameter setting for I/O Power Selection Re-named Figure 11 and 12 Revised 7.4. Sleep Mechanism Revised 7.11. Spread Spectrum Clock (SSC) Revised 8.2.26. SSCCR (SSC Control Register, Page 0xd01, Address 0x11)

<b>Revision</b>	<b>Release Date</b>	<b>Summary</b>
Draft 1.3	2017/05/22	Move PHY FSR to 8.2.9 Revised Figure 30 Revised 7.5.1 Remote Wake-up Revised Figure 1 Revised 7.9.4. Management Interface Revised 8.2.1. BMCR (Basic Mode Control Register, Address 0x00) Revised 9.1. Power Sequence Revised 9.2. Reset
Draft 1.4	2017/08/25	Revised 1 General Description to claim the difference between RTL9000AA-VC and RTL9000AN-VC Revised 5 Pin Assignments Revised 6.4 RGMII Revised 6.9 Hardware Strapping Configuration Revised 6.7 Management Interface Revised 7.3 Operating Modes Revised 7.4 Sleep Mechanism Revised 7.5 Wake-up Revised 7.6 Precision Time Protocol Revised 7.8 Hardware Configuration Revised 7.9.5 Register Access Revised 7.10 Polarity Correction Revised 7.12 Realtek Cable Test Diagnostics (RTCT) Revised 7.13 Signal Quality Indexes Revised 7.14 LED Removed 8.1. IEEE Standard Register Mapping and Definitions Revised 8.2 General Register Tables Revised 8.3 PTP Register Tables Revised 8.4 OP Register Tables Revised 9 Power Sequence and Regulators Revised 11. Mechanical Dimensions Added RTL9000AN General Application Diagram in 3. Added RTL9000AN Pin Assignment in 5.2. Added RTL9000AN absolute maximum ratings in 10.1. Added RTL9000AN Recommended Operating Conditions in 10.2. Added RTL9000AN power dissipation table in 10.4. Added RTL9000AN DC Characteristics in 10.5. Added RTL9000AN ESD Criteria in 10.7.

## Table of Contents

<b>1. GENERAL DESCRIPTION .....</b>	<b>1</b>
<b>2. FEATURES .....</b>	<b>2</b>
<b>3. APPLICATION DIAGRAM .....</b>	<b>3</b>
3.1. GENERAL APPLICATION DIAGRAM .....	3
3.2. PTP APPLICATION DIAGRAM .....	4
<b>4. BLOCK DIAGRAM .....</b>	<b>5</b>
<b>5. PIN ASSIGNMENTS .....</b>	<b>6</b>
5.1. RTL9000AA PIN ASSIGNMENTS (QFN-36).....	6
5.2. RTL9000AN PIN ASSIGNMENTS (QFN-36).....	7
<b>6. PIN DESCRIPTIONS .....</b>	<b>8</b>
6.1. TRANSCEIVER INTERFACE.....	8
6.2. CLOCK .....	8
6.3. MII .....	8
6.4. RMII.....	9
6.5. RGMII.....	10
6.6. LED / PTP APPLICATION INTERFACE.....	10
6.7. MANAGEMENT INTERFACE .....	10
6.8. POWER AND GROUND .....	11
6.9. HARDWARE STRAPPING CONFIGURATION.....	12
<b>7. FUNCTION DESCRIPTION .....</b>	<b>13</b>
7.1. TRANSMITTER.....	13
7.2. RECEIVER.....	13
7.3. OPERATING MODES (OP).....	14
7.3.1. <i>Operating Modes</i> .....	14
7.3.2. <i>Operating Mode Transition</i> .....	16
7.4. SLEEP MECHANISM .....	18
7.5. WAKE-UP .....	21
7.5.1. <i>Local Wake-up</i> .....	21
7.5.2. <i>Remote Wake-up</i> .....	23
7.6. PRECISION TIME PROTOCOL (PTP) .....	26
7.6.1. <i>Synchronized PTP Clock</i> .....	26
7.6.2. <i>Packet Time Stamping</i> .....	27
7.6.3. <i>Time Application Interface (TAI)</i> .....	27
7.6.4. <i>PTP Function Configuration</i> .....	27
7.6.5. <i>Flow of PTP Sample</i> .....	34
7.7. INTERRUPT .....	42
7.8. HARDWARE CONFIGURATION .....	45
7.9. MAC/PHY INTERFACE .....	46
7.9.1. <i>MII</i> .....	46
7.9.2. <i>RMII</i> .....	46
7.9.3. <i>RGMII</i> .....	46
7.9.4. <i>Management Interface</i> .....	46
7.9.5. <i>Register Access</i> .....	47
7.10. POLARITY CORRECTION .....	49
7.11. SPREAD SPECTRUM CLOCK (SSC) .....	49
7.12. REALTEK CABLE TEST DIAGNOSTICS (RTCT).....	49
7.12.1. <i>RTCT Method</i> .....	49

7.12.2. <i>Cable length Checking Method (in Normal Operating Mode Only)</i> .....	50
7.13. SIGNAL QUALITY INDEXES (SQI).....	51
7.13.1. <i>Signal-to-Noise-Ratio (SNR)</i> .....	51
7.13.2. <i>Maximum Error</i> .....	51
7.14. LED .....	51
7.15. UNH IOL TEST.....	52
7.15.1. <i>Test mode 1</i> .....	52
7.15.2. <i>Test mode 2</i> .....	53
7.15.3. <i>Test mode 4</i> .....	53
7.15.4. <i>Test mode 5</i> .....	53
7.15.5. <i>SLAVE Jitter</i> .....	53
<b>8. REGISTER DESCRIPTIONS.....</b>	<b>54</b>
8.1. IEEE STANDARD REGISTER MAPPING AND DEFINITIONS .....	54
8.2. GENERAL REGISTER TABLES .....	55
8.2.1. <i>BMCR (Basic Mode Control Register, Page 0x0, Reg 0x00)</i> .....	55
8.2.2. <i>BMSR (Basic Mode Status Register, Page 0x0, Reg 0x01)</i> .....	56
8.2.3. <i>PHYID1 (PHY Identifier Register 1, Page 0x0, Reg 0x02)</i> .....	56
8.2.4. <i>PHYID2 (PHY Identifier Register 2, Page 0x0, Reg 0x03)</i> .....	56
8.2.5. <i>PHYCR (PHY Control Register, Page 0x0, Reg 0x09)</i> .....	57
8.2.6. <i>PHYSR1 (PHY Status Register 1, Page 0x0, Reg 0x0A)</i> .....	57
8.2.7. <i>MACR (MMD Access Control Register, Page 0x0, Reg 0x0D)</i> .....	58
8.2.8. <i>MAADDR (MMD Access Address Data Register, Page 0x0, Reg 0xE)</i> .....	58
8.2.9. <i>PHYSFR (PHY Status Sub-flag Register, Page 0xa42, Reg 0x10)</i> .....	58
8.2.10. <i>RTCTCR (RTCT Control Register, Page 0xa42, Reg 0x11)</i> .....	59
8.2.11. <i>GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12)</i> .....	59
8.2.12. <i>GINMR (General Interrupt Mask Register, Page 0xa42, Reg 0x14)</i> .....	60
8.2.13. <i>SLPCR (Sleep Control Register, Page 0xa42, Reg 0x15)</i> .....	60
8.2.14. <i>LKTCR (Link Timer Control Register, Page 0xa42, Reg 0x16)</i> .....	60
8.2.15. <i>PHYCR (PHY Specific Control Register, Page 0xa43, Reg 0x18)</i> .....	60
8.2.16. <i>PHYSR2 (PHY Status Register 2, Page 0xa43, Reg 0x1A)</i> .....	61
8.2.17. <i>PHYSRAD (PHY SRAM Address Register, Page 0xa43, Reg 0x1B)</i> .....	61
8.2.18. <i>PHYSRD (PHY SRAM Data Register, Page 0xa43, Reg 0x1C)</i> .....	61
8.2.19. <i>GINSR (General Interrupt Status Register, Page 0xa43, Reg 0x1D)</i> .....	62
8.2.20. <i>PAGSR (Page Select Register, Page 0xa43, Reg 0x1F)</i> .....	62
8.2.21. <i>GPSFR (General Purpose Sub-flag Register, Page 0xa47, Reg 0x15)</i> .....	62
8.2.22. <i>SLPCAP (Sleep Capability Register, Page 0xa5a, Reg 0x14)</i> .....	62
8.2.23. <i>SLR (Scrambler Lock Register, Page 0xa60, Reg 0x11)</i> .....	63
8.2.24. <i>PCR (Polarity Correction Register, Page 0xa60, Reg 0x14)</i> .....	63
8.2.25. <i>LKTR(Link Timer Register, Page 0xa61, Reg 0x10)</i> .....	63
8.2.26. <i>SNRR(Signal to Noise Ratio Register, Address 0xa8c0)</i> .....	63
8.2.27. <i>MERR(Maximum Error Register, Address 0xa8e0)</i> .....	64
8.2.28. <i>CLENR (Cable Length Register, Address 0xa890)</i> .....	64
8.2.29. <i>SSCCR (SSC Control Register, Address 0xd012)</i> .....	64
8.2.30. <i>RXDVCR (RXDV Control Register, Address 0xd050)</i> .....	64
8.2.31. <i>LEDCR (LED Control Register, Address 0xd040)</i> .....	64
8.2.32. <i>LED_PTP (LED/PTP_GPIO Select Register, Address 0xd42a)</i> .....	65
8.3. PTP REGISTER TABLES .....	66
8.3.1. <i>PTP_CTL (PTP Control Register, Address 0xe400)</i> .....	66
8.3.2. <i>PTP_INER (PTP Interrupt Enable Register, Address 0xe402)</i> .....	66
8.3.3. <i>PTP_INSR (PTP Interrupt Status Register, Address 0xe404)</i> .....	67
8.3.4. <i>PTP_CLK_CFG (PTP Clock Config Register, Address 0xe410)</i> .....	67
8.3.5. <i>PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Address 0xe412)</i> .....	68
8.3.6. <i>PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Address 0xe414)</i> .....	68
8.3.7. <i>PTP_CFG_S_LO (PTP Time Config Sec Low Register, Address 0xe416)</i> .....	68

8.3.8.	<i>PTP_CFG_S_MI</i> (PTP Time Config Sec Mid Register, Address 0xe418) .....	68
8.3.9.	<i>PTP_CFG_S_HI</i> (PTP Time Config Sec High Register, Address 0xe41A) .....	68
8.3.10.	<i>PTP_TAI_CFG</i> (PTP Application I/F Config Register, Address 0xe420) .....	69
8.3.11.	<i>PTP_TRIG_CFG</i> (PTP Trigger Config Register, Address 0xe422) .....	70
8.3.12.	<i>PTP_TAI_STA</i> (PTP Application I/F Status Register, Address 0xe424) .....	70
8.3.13.	<i>PTP_TAI_TS_NS_LO</i> (PTP TAI Timestamp Nano-Sec Low Register, Address 0xe426) .....	70
8.3.14.	<i>PTP_TAI_TS_NS_HI</i> (PTP TAI Timestamp Nano-Sec High Register, Address 0xe428) .....	71
8.3.15.	<i>PTP_TAI_TS_S_LO</i> (PTP TAI Timestamp Sec Low Register, Address 0xe42a) .....	71
8.3.16.	<i>PTP_TAI_TS_S_HI</i> (PTP TAI Timestamp Sec High Register, Address 0xe42c) .....	71
8.3.17.	<i>PTP_TRX_TS_STA</i> (PTP TxRx Timestamp Status Register, Address 0xe430) .....	71
8.3.18.	<i>PTP_TRX_TS_INFO</i> (PTP TxRx Timestamp Info Register, Address 0xe440) .....	72
8.3.19.	<i>PTP_TRX_TS_SH</i> (PTP TxRx Timestamp Source Hash Register, Address 0xe442) .....	72
8.3.20.	<i>PTP_TRX_TS_SID</i> (PTP TxRx Timestamp Seq ID Register, Address 0xe444) .....	73
8.3.21.	<i>PTP_TRX_TS_NS_LO</i> (PTP TxRx Timestamp Nano-Sec Low Register, Address 0xe446) .....	73
8.3.22.	<i>PTP_TRX_TS_NS_HI</i> (PTP TxRx Timestamp Nano-Sec High Register, Address 0xe448) .....	73
8.3.23.	<i>PTP_TRX_TS_S_LO</i> (PTP TxRx Timestamp Sec Low Register, Address 0xe44a) .....	73
8.3.24.	<i>PTP_TRX_TS_S_MI</i> (PTP TxRx Timestamp Sec Mid Register, Address 0xe44c) .....	74
8.3.25.	<i>PTP_TRX_TS_S_HI</i> (PTP TxRx Timestamp Sec High Register, Address 0xe44e) .....	74
8.4.	OP REGISTER TABLES .....	75
8.4.1.	<i>OPCR1</i> (OP Control Register 1, Address 0xDC0C) .....	75
8.4.2.	<i>OPCR2</i> (OP Control Register 2, Address 0xDD00) .....	75
8.4.3.	<i>OPCR3</i> (OP Control Register 3, Address 0xDD02) .....	76
8.4.4.	<i>OPINSR1</i> (OP Interrupt Status Register 1, Address 0xDD08) .....	76
8.4.5.	<i>OPINER1</i> (OP Interrupt Enable Register 1, Address 0xDD0C) .....	77
8.4.6.	<i>OPINMR1</i> (OP Interrupt Mask Register 1, Address 0xDD0E) .....	78
8.4.7.	<i>OPINSR2</i> (OP Interrupt Status Register 2, Address 0xDD10) .....	78
8.4.8.	<i>OPINER2</i> (OP Interrupt Enable Register 2, Address 0xDD14) .....	79
8.4.9.	<i>OPINMR2</i> (OP Interrupt Mask Register 2, Address 0xDD16) .....	79
8.4.10.	<i>OPINSR3</i> (OP Interrupt Status Register 3, Address 0xDD18) .....	80
8.4.11.	<i>OPINER3</i> (OP Interrupt Enable Register 3, Address 0xDD1C) .....	80
8.4.12.	<i>OPINMR3</i> (OP Interrupt Mask Register 3, Address 0xDD1E) .....	81
8.4.13.	<i>OPCR4</i> (OP Control Register 4, Address 0xDD20) .....	81
9.	POWER SEQUENCE AND REGULATORS .....	82
9.1.	POWER SEQUENCE .....	83
9.2.	RESET .....	83
10.	CHARACTERISTICS .....	85
10.1.	ABSOLUTE MAXIMUM RATINGS .....	85
10.2.	RECOMMENDED OPERATING CONDITIONS .....	85
10.3.	THERMAL CHARACTERISTICS .....	86
10.4.	POWER DISSIPATION .....	86
10.5.	DC CHARACTERISTICS .....	87
10.6.	OVER TEMPERATURE PROTECTION .....	90
10.7.	ESD .....	91
10.8.	CRYSTAL REQUIREMENTS .....	92
10.9.	OSCILLATOR/EXTERNAL CLOCK REQUIREMENTS .....	92
10.10.	AC CHARACTERISTICS .....	93
10.10.1.	<i>MDC/Mdio Timing</i> .....	93
10.10.2.	<i>MII Transmission Cycle Timing</i> .....	94
10.10.3.	<i>MII Reception Cycle Timing</i> .....	95
10.10.4.	<i>RMII Transmission and Reception Cycle Timing</i> .....	95
10.10.5.	<i>RGMII Timing Modes</i> .....	97
11.	MECHANICAL DIMENSIONS .....	100

11.1. MECHANICAL DIMENSIONS NOTES .....	100
<b>12. ORDERING INFORMATION .....</b>	<b>101</b>

## List of Tables

TABLE 1. TRANSCEIVER INTERFACE .....	8
TABLE 2. CLOCK .....	8
TABLE 3. MII .....	8
TABLE 4. RMII.....	9
TABLE 5. RGMII.....	10
TABLE 6. PTP APPLICATION INTERFACE.....	10
TABLE 7. MANAGEMENT INTERFACE .....	10
TABLE 8. POWER AND GROUND .....	11
TABLE 9. HARDWARE STRAPPING CONFIGURATION .....	12
TABLE 10. OVERVIEW OF THE OPERATING STATES .....	16
TABLE 11. SUMMARY OF PTP PACKET TYPES .....	31
TABLE 12. GENERAL INTERRUPTS AND SUB-FLAGS .....	43
TABLE 13. CONFIG PINS VS. CONFIGURATION REGISTER.....	45
TABLE 14. CONFIGURATION REGISTER DEFINITIONS .....	45
TABLE 15. MANAGEMENT FRAME FORMAT .....	46
TABLE 16. MANAGEMENT FRAME DESCRIPTION.....	46
TABLE 17. METHOD OF ACCESSING REGISTERS .....	48
TABLE 18. RTCT CABLE STATUS INDICATION.....	50
TABLE 19. SQI CLASSIFICATION .....	51
TABLE 20. LED.....	51
TABLE 21. REGISTER ACCESS TYPES .....	54
TABLE 22. IEEE STANDARD REGISTER MAPPING AND DEFINITIONS .....	54
TABLE 23. BMCR (BASIC MODE CONTROL REGISTER, PAGE 0x0, REG 0x00).....	55
TABLE 24. BMSR (BASIC MODE STATUS REGISTER, PAGE 0x0, REG 0x01).....	56
TABLE 25. PHYID1 (PHY IDENTIFIER REGISTER 1, PAGE 0x0, REG 0x02).....	56
TABLE 26. PHYID2 (PHY IDENTIFIER REGISTER 2, PAGE 0x0, REG 0x03).....	56
TABLE 27. PHYCR (PHY CONTROL REGISTER, PAGE 0x0, REG 0x09).....	57
TABLE 28. PHYSR1 (PHY STATUS REGISTER 1, PAGE 0x0, REG 0x0A).....	57
TABLE 29. MACR (MMD ACCESS CONTROL REGISTER, PAGE 0x0, REG 0x0D).....	58
TABLE 30. MAADR (MMD ACCESS ADDRESS DATA REGISTER, PAGE 0x0, REG 0x0E).....	58
TABLE 31. PHYSFR (PHY STATUS SUB-FLAG REGISTER, PAGE 0XA42, REG 0X10).....	58
TABLE 32. RTCTCR (RTCT CONTROL REGISTER, PAGE 0XA42, REG 0X11) .....	59
TABLE 33. GINER (GENERAL INTERRUPT ENABLE REGISTER, PAGE 0XA42, REG 0X12) .....	59
TABLE 34. GINMR (GENERAL INTERRUPT MASK REGISTER, PAGE 0XA42, REG 0X14) .....	60
TABLE 35. SLPPCR (SLEEP CONTROL REGISTER, PAGE 0XA42, REG 0X15).....	60
TABLE 36. LKTCR (LINK TIMER CONTROL REGISTER, PAGE 0XA42, REG 0X16) .....	60
TABLE 37. PHYCR (PHY SPECIFIC CONTROL REGISTER, PAGE 0XA43, REG 0X18).....	60
TABLE 38. PHYSR2 (PHY STATUS REGISTER 2, PAGE 0XA43, REG 0X1A) .....	61
TABLE 39. PHYSRAD (PHY SRAM ADDRESS REGISTER, PAGE 0XA43, REG 0X1B) .....	61
TABLE 40. PHYSRD (PHY SRAM DATA REGISTER, PAGE 0XA43, REG 0X1C) .....	61
TABLE 41. GINSR (GENERAL INTERRUPT STATUS REGISTER, PAGE 0XA43, REG 0X1D) .....	62
TABLE 42. PAGSR (PAGE SELECT REGISTER, PAGE 0XA43, REG 0X1F) .....	62
TABLE 43. GPSFR (GENERAL PURPOSE SUB-FLAG REGISTER, PAGE 0XA47, REG 0X15) .....	62

TABLE 44. SLPCAP (SLEEP CAPABILITY REGISTER, PAGE 0XA5A, REG 0X14) .....	62
TABLE 45. PLCR (SCRAMBLER LOCK REGISTER, PAGE 0XA60, REG 0X11) .....	63
TABLE 46. PLCR (POLARITY CORRECTION REGISTER, PAGE 0XA60, REG 0X14) .....	63
TABLE 47. LKTR (LINK TIMER REGISTER, PAGE 0XA61, REG 0X10) .....	63
TABLE 48. SNRR (SIGNAL TO NOISE RATIO REGISTER, ADDRESS 0XA8C0) .....	63
TABLE 49. MERR (MAXIMUM ERROR REGISTER, ADDRESS 0XA8E0) .....	64
TABLE 50. CLENR (CABLE LENGTH REGISTER, ADDRESS 0XA890) .....	64
TABLE 51. SSCCR (SSC CONTROL REGISTER, ADDRESS 0XD012) .....	64
TABLE 52. RXDVCR (RXDV CONTROL REGISTER, ADDRESS 0XD050) .....	64
TABLE 53. LEDCR (LED CONTROL REGISTER, ADDRESS 0XD040) .....	64
TABLE 54. LED_PTP (LED/PTP_GPIO SELECT REGISTER, ADDRESS 0XD42A) .....	65
TABLE 55. PTP_CTL (PTP CONTROL REGISTER, ADDRESS 0XE400) .....	66
TABLE 56. PTP_INER (PTP INTERRUPT ENABLE REGISTER, ADDRESS 0XE402) .....	66
TABLE 57. PTP_INSR (PTP INTERRUPT STATUS REGISTER, ADDRESS 0XE404) .....	67
TABLE 58. PTP_CLK_CFG (PTP CLOCK CONFIG REGISTER, ADDRESS 0XE410) .....	67
TABLE 59. PTP_CFG_NS_LO (PTP TIME CONFIG NANO-SEC LOW REGISTER, ADDRESS 0XE412) .....	68
TABLE 60. PTP_CFG_NS_HI (PTP TIME CONFIG NANO-SEC HIGH REGISTER, ADDRESS 0XE414) .....	68
TABLE 61. PTP_CFG_S_LO (PTP TIME CONFIG SEC LOW REGISTER, ADDRESS 0XE416) .....	68
TABLE 62. PTP_CFG_S_MI (PTP TIME CONFIG SEC MID REGISTER, ADDRESS 0XE418) .....	68
TABLE 63. PTP_S_HI (PTP TIME CONFIG SEC HIGH REGISTER, ADDRESS 0XE41A) .....	68
TABLE 64. PTP_TAI_CFG (PTP APPLICATION I/F CONFIG REGISTER, ADDRESS 0XE420) .....	69
TABLE 65. PTP_TRIG_CFG (PTP TRIGGER CONFIG REGISTER, ADDRESS 0XE422) .....	70
TABLE 66. PTP_TAI_STA (PTP APPLICATION I/F STATUS REGISTER, ADDRESS 0XE424) .....	70
TABLE 67. PTP_TAI_TS_NS_LO (PTP TAI TIMESTAMP NANO-SEC LOW REGISTER, ADDRESS 0XE426) .....	70
TABLE 68. PTP_TAI_TS_NS_HI (PTP TAI TIMESTAMP NANO-SEC HIGH REGISTER, ADDRESS 0XE428) .....	71
TABLE 69. PTP_S_LO (PTP TIME CONFIG SEC LOW REGISTER, ADDRESS 0XE42A) .....	71
TABLE 70. PTP_S_MI (PTP TIME CONFIG SEC MID REGISTER, ADDRESS 0XE42C) .....	71
TABLE 71. PTP_TRX_TS_STA (PTP TxRx TIMESTAMP STATUS REGISTER, ADDRESS 0XE430) .....	71
TABLE 72. PTP_TRX_TS_INFO (PTP TxRx TIMESTAMP INFO REGISTER, ADDRESS 0XE440) .....	72
TABLE 73. PTP_TRX_TS_SH (PTP TxRx TIMESTAMP SOURCE HASH REGISTER, ADDRESS 0XE442) .....	72
TABLE 74. PTP_TRX_TS_SID (PTP TxRx TIMESTAMP SEQ ID REGISTER, ADDRESS 0XE444) .....	73
TABLE 75. PTP_TRX_TS_NS_LO (PTP TxRx TIMESTAMP NANO-SEC LOW REGISTER, ADDRESS 0XE446) .....	73
TABLE 76. PTP_TRX_TS_NS_HI (PTP TxRx TIMESTAMP NANO-SEC HIGH REGISTER, ADDRESS 0XE448) .....	73
TABLE 77. PTP_TRX_TS_S_LO (PTP TxRx TIMESTAMP SEC LOW REGISTER, ADDRESS 0XE44A) .....	73
TABLE 78. PTP_TRX_TS_S_MID (PTP TxRx TIMESTAMP SEC MID REGISTER, ADDRESS 0XE44C) .....	74
TABLE 79. PTP_TRX_TS_S_HI (PTP TxRx TIMESTAMP SEC HIGH REGISTER, ADDRESS 0XE44E) .....	74
TABLE 80. OPCR1 (OP CONTROL REGISTER 1, ADDRESS 0xDC0C) .....	75
TABLE 81. OPCR2 (OP CONTROL REGISTER 2, ADDRESS 0xDD00) .....	75
TABLE 82. OPCR3 (OP CONTROL REGISTER 3, ADDRESS 0xDD02) .....	76
TABLE 83. OPINSR1 (OP INTERRUPT STATUS REGISTER 1, ADDRESS 0xDD08) .....	76
TABLE 84. OPINER1 (OP INTERRUPT ENABLE REGISTER 1, ADDRESS 0xDD0C) .....	77
TABLE 85. OPINMR1 (OP INTERRUPT MASK REGISTER 1, ADDRESS 0xDD0E) .....	78
TABLE 86. OPINSR2 (OP INTERRUPT STATUS REGISTER 2, ADDRESS 0xDD10) .....	78
TABLE 87. OPINER2 (OP INTERRUPT ENABLE REGISTER 2, ADDRESS 0xDD14) .....	79
TABLE 88. OPINMR2 (OP INTERRUPT MASK REGISTER 2, ADDRESS 0xDD16) .....	79
TABLE 89. OPINSR3 (OP INTERRUPT STATUS REGISTER 3, ADDRESS 0xDD18) .....	80
TABLE 90. OPINER3 (OP INTERRUPT ENABLE REGISTER 3, ADDRESS 0xDD1C) .....	80
TABLE 91. OPINMR3 (OP INTERRUPT MASK REGISTER 3, ADDRESS 0xDD1E) .....	81
TABLE 92. OPCR4 (OP CONTROL REGISTER 4, ADDRESS 0xDD20) .....	81
TABLE 93. PARAMETER SETTING FOR I/O POWER SELECTION .....	82
TABLE 94. POWER SEQUENCE PARAMETERS .....	83
TABLE 95. PHY RESET SIGNAL TIMING PARAMETER .....	84
TABLE 96. ABSOLUTE MAXIMUM RATINGS .....	85
TABLE 97. RECOMMENDED OPERATING CONDITIONS .....	85
TABLE 98. THERMAL CHARACTERISTICS .....	86

TABLE 99. RTL9000AA-VC POWER DISSIPATION .....	86
TABLE 100. RTL9000AN-VC POWER DISSIPATION .....	87
TABLE 101. DC CHARACTERISTICS.....	87
TABLE 102. DIGITAL IO CHARACTERISTICS.....	89
TABLE 103. OVER TEMPERATURE PROTECTION .....	90
TABLE 104. RTL9000AA-VC ESD CRITERIA.....	91
TABLE 105. RTL9000AN-VC ESD CRITERIA.....	91
TABLE 106. CRYSTAL REQUIREMENTS.....	92
TABLE 107. OSCILLATOR/EXTERNAL CLOCK REQUIREMENTS.....	92
TABLE 108. MDC/Mdio MANAGEMENT TIMING PARAMETERS .....	93
TABLE 109. MII TRANSMISSION CYCLE TIMING .....	94
TABLE 110. MII RECEPTION CYCLE TIMING .....	95
TABLE 111. RMII TRANSMISSION AND RECEPTION CYCLE TIMING .....	96
TABLE 112. RGMII TIMING PARAMETERS.....	99
TABLE 113. ORDERING INFORMATION .....	101

## List of Figures

FIGURE 1. RTL9000AA GENERAL APPLICATION DIAGRAM .....	3
FIGURE 2. RTL9000AN GENERAL APPLICATION DIAGRAM .....	3
FIGURE 3. PTP APPLICATION DIAGRAM.....	4
FIGURE 4. BLOCK DIAGRAM .....	5
FIGURE 5. RTL9000AA PIN ASSIGNMENTS (QFN-36) .....	6
FIGURE 6. RTL9000AN PIN ASSIGNMENTS (QFN-36) .....	7
FIGURE 7. OPERATING MODE TRANSITIONS .....	14
FIGURE 8. FLOW CHART OF SLEEP MECHANISM OF SLEEP INITIATOR .....	19
FIGURE 9. FLOW CHART OF SLEEP MECHANISM OF SLEEP RESPONDER .....	20
FIGURE 10. RTL9000AA LOCAL WAKE UP (LWAKE) EVENT DETECTION .....	21
FIGURE 11. RTL9000AN LOCAL WAKE UP (LWAKE) EVENT DETECTION .....	21
FIGURE 12. RTL9000AA WAKE FLOW FOR LOCAL WAKE UP WITH THE INH PIN .....	22
FIGURE 13. RTL9000AA WAKE FLOW FOR LOCAL WAKE UP WITHOUT THE INH PIN .....	23
FIGURE 14. RTL9000AN WAKE FLOW FOR LOCAL WAKE UP .....	23
FIGURE 15. RTL9000AA WAKE FLOW FOR REMOTE WAKE UP WITH THE INH PIN .....	24
FIGURE 16. RTL9000AA WAKE FLOW FOR REMOTE WAKE UP .....	25
FIGURE 17. RTL9000AN WAKE FLOW FOR REMOTE WAKE UP .....	25
FIGURE 18. TWO-STEP PTP SYNCHRONIZATION.....	28
FIGURE 19. ONE-STEP PTP SYNCHRONIZATION .....	29
FIGURE 20. CALCULATION OF NEIGHBORRATERATIO .....	30
FIGURE 21. 802.1AS TWO-STEP PROTOCOL .....	34
FIGURE 22. PTPv2 ONE-STEP PROTOCOL .....	35
FIGURE 23. MASTER FLOW CHART OF 802.1AS TWO-STEP SAMPLE .....	36
FIGURE 24. RESPONDER FLOW CHART OF 802.1AS TWO-STEP SAMPLE.....	37
FIGURE 25. SLAVE FLOW CHART OF 802.1AS TWO-STEP SAMPLE .....	38
FIGURE 26. MASTER FLOW CHART OF PTPv2 ONE-STEP SAMPLE .....	39
FIGURE 27. RESPONDER FLOW CHART OF PTPv2 ONE-STEP SAMPLE .....	40
FIGURE 28. SLAVE FLOW CHART OF PTPv2 ONE-STEP SAMPLE .....	41
FIGURE 29. INTERRUPT AND MASK BEHAVIOR .....	43
FIGURE 30. MDC/Mdio READ TIMING.....	47
FIGURE 31. MDC/Mdio WRITE TIMING .....	47
FIGURE 32. SPREAD SPECTRUM CLOCK .....	49

---

FIGURE 33. LED BEHAVIOR.....	52
FIGURE 34. POWER SEQUENCE.....	83
FIGURE 35. PHY RESET TIMING .....	84
FIGURE 36. MDC/Mdio SETUP, HOLD TIME, AND VALID FROM MDC RISING EDGE TIME DEFINITIONS .....	93
FIGURE 37. MDC/Mdio MANAGEMENT TIMING PARAMETERS .....	93
FIGURE 38. MII INTERFACE SETUP/HOLD TIME DEFINITIONS .....	94
FIGURE 39. MII TRANSMISSION CYCLE TIMING .....	94
FIGURE 40. MII RECEPTION CYCLE TIMING.....	95
FIGURE 41. RMII INTERFACES SETUP, HOLD TIME, AND OUTPUT DELAY TIME DEFINITIONS .....	95
FIGURE 42. RMII TRANSMISSION AND RECEPTION CYCLE TIMING.....	96
FIGURE 43. RGMII TIMING MODES (FOR TXC) .....	97
FIGURE 44. RGMII TIMING MODES (FOR RXC) .....	98

## 1. General Description

This document is jointly used for RTL9000AA-VC and RTL9000AN-VC. These two devices have almost the same features, except for the INH pin, WAKE pin and pin9. The difference of Direct Current (DC) Characteristics of the INH pin and WAKE pin can refer to section 10.5. Besides, the pin9 of RTL9000AA-VC is VBAT pin which supports the car battery; the pin9 of RTL9000AN-VC is a no connection pin which can't support car battery (12V/24V). This document specifically annotates the different features between RTL9000AA-VC and RTL9000AN-VC. If there has no specific notation said it is for RTL9000AA-VC or RTL9000AN-VC, it means that this feature is the same for these two devices.

The RTL9000AA-VC/RTL9000AN-VC is a highly integrated automotive transceiver that complies with IEEE 802.3bw 100BASE-T1 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over single Unshielded Twisted Pair (UTP) cable for Automotive Electronics.

Data transfer between Medium Access Control (MAC) and the RTL9000AA-VC/RTL9000AN-VC PHY is via the Media Independent Interface (MII), Reduced Media Independent Interface (RMII), or Reduced Gigabit Media Independent Interface (RGMII). The RTL9000AA-VC/RTL9000AN-VC support 3.3V/2.5V/1.8V I/O signaling of MII/RMII/RGMII. The digital input pins including MDC, MDIO, DISB PHYRSTB, RXC (in RMII Input Mode), TXC, TXEN, TXD[3:0], and PTP\_GPIO/LED pins of the RTL9000AA-VC/RTL9000AN-VC that are connected with the microcontroller are 5V-friendly (up to 5.25 V).

Both of the RTL9000AA-VC/RTL9000AN-VC support OPEN Alliance TC10 Sleep/Wake function for the automotive Ethernet, refer to section 7.4 and 7.5. The Sleep function implements the PHY into the Sleep mode which has lower power consumption. The Wake function can let the PHY be efficiently woken up to the normal operation mode from the Sleep mode.

Furthermore, the RTL9000AA-VC/RTL9000AN-VC provides full hardware support for high-precision clock synchronization based on the Precision Time Protocol (PTP) of IEEE 1588 and 802.1AS standard. The integrated PTP functionality accurately timestamps each PTP packet on Tx/Rx path, and the upper layer software can take this timing information to determine the timing offset to the 1588 master's clock. The device also equips the General Purpose Input/Output (GPIO) as the PTP application interface.

The RTL9000AA-VC/RTL9000AN-VC uses state-of-the-art Digital Signal Processor (DSP) technology and the Analog Front End (AFE) to enable robust and high-speed data transmission and reception. It offers high Electro-Static Discharge (ESD) protection as well as excellent Electromagnetic Compatibility (EMC) performance. The Under-voltage and Temperature monitoring built into the RTL9000AA-VC/RTL9000AN-VC will continuously monitor the operating condition of the chip, take corresponding action, and show status or error information to the upper layer.

## 2. Features

### ● 100BASE-T1 Transceiver

- ◆ Fully standard compliant with 100BASE-T1 IEEE 802.3bw standards over single-pair copper cable
- ◆ Data transfer up to 100Mbps
- ◆ Rapid link-up time (< 100ms)
- ◆ Full-duplex supported

### ● Interfaces

- ◆ Supports MII/RMII/RGMII with optional internal delay on Tx and Rx path
- ◆ High-speed MDC/MDIO interface
- ◆ Supports I/O power as 1.8V/2.5V/3.3V
- ◆ Interrupt notifications
- ◆ PTP GPIO

### ● Power Supply

- ◆ Can be directly connected to 12 / 24V Car Battery (RTL9000AA Only)
- ◆ An Embedded LDO which switches voltages and provides 1.2V power for digital/analog core power

### ● Clocking

- ◆ Supports 25 MHz crystal /external clock

### ● Power Saving

- ◆ Open Alliance Standard Sleep mechanism
- ◆ Ultra-low power consumption during Sleep mode (35uA) (RTL9000AA Only)
- ◆ Supports Remote/Local Wake-up

### ● Precision Time Protocol (PTP)

- ◆ Complete hardware support for Precision Time Protocol, including IEEE1588v1, v2, and 802.1AS)
- ◆ PTP Packet parser supports Layer 2 Ethernet, IPv4/UDP, IPv6/UDP packets
- ◆ One-Step operation supported

- ◆ Adjustable PTP clock for synchronization
- ◆ 8ns timestamp resolution
- ◆ Deterministic and low transmission latency for PTP mechanism
- ◆ Programmable Time Application Interfaces through the PTP GPIO
- ◆ Selectable PTP clock input from the external reference clock source

### ● Performance

- ◆ Conform to AEC-Q100 Grade 1 (-40~125° C)
- ◆ Low Electro-Magnetic Emission (EMC)
- ◆ HBM ESD protection level:
  - \* ±4KV for MDI and global pins
  - \* ±2KV for other pins
- ◆ IEC 61000-4-2 ESD protection level:
  - \* ±6KV for MDI and global pins
- ◆ MDI pins are tolerant of transient conditions according to ISO 7637 class C
- ◆ Supports at least 15m for single-pair cable
- ◆ Baseline Wander Correction feature
- ◆ Echo Cancellation mechanism

### ● Diagnosis

- ◆ Realtek Cable Test Diagnostics (RTCT) detects open/short status and distance of the cable (resolution: ±1m) and status indication
- ◆ Under-voltage detection
- ◆ Over-temperature detection
- ◆ IEEE 1149.1 JTAG testing and build-in self-testing (BIST) mode supported

### ● Process and Packages

- ◆ 65nm LP process
- ◆ 36-pin QFN package (6\*6)

### 3. Application Diagram

#### 3.1. General Application Diagram

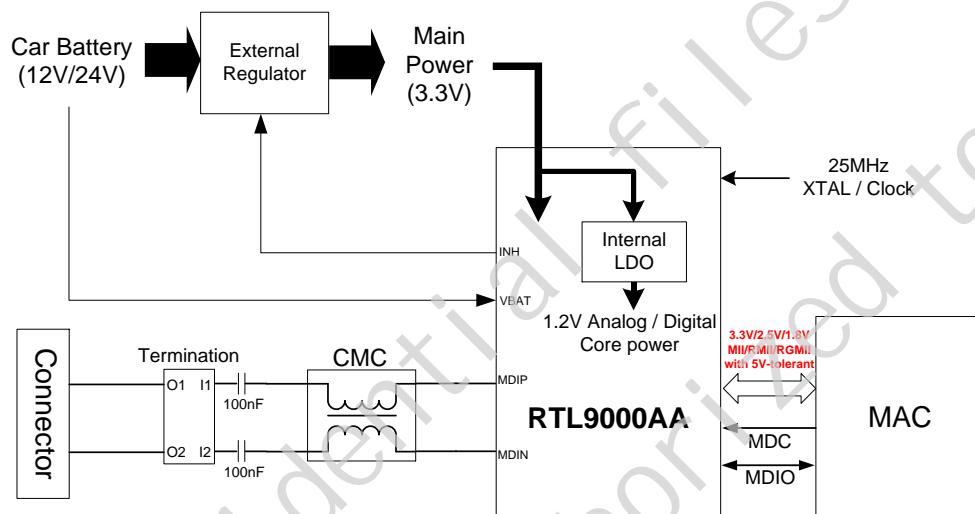


Figure 1. RTL9000AA General Application Diagram

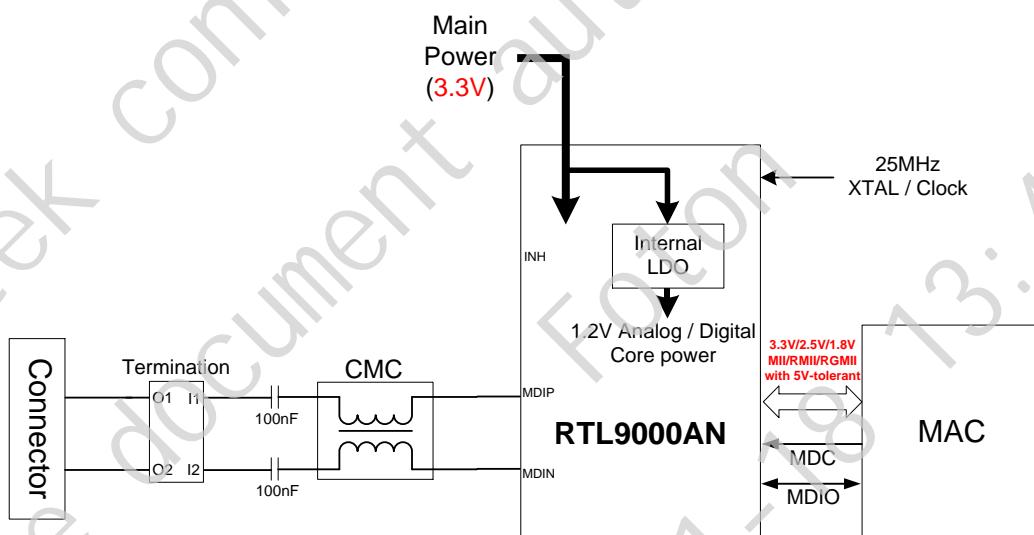
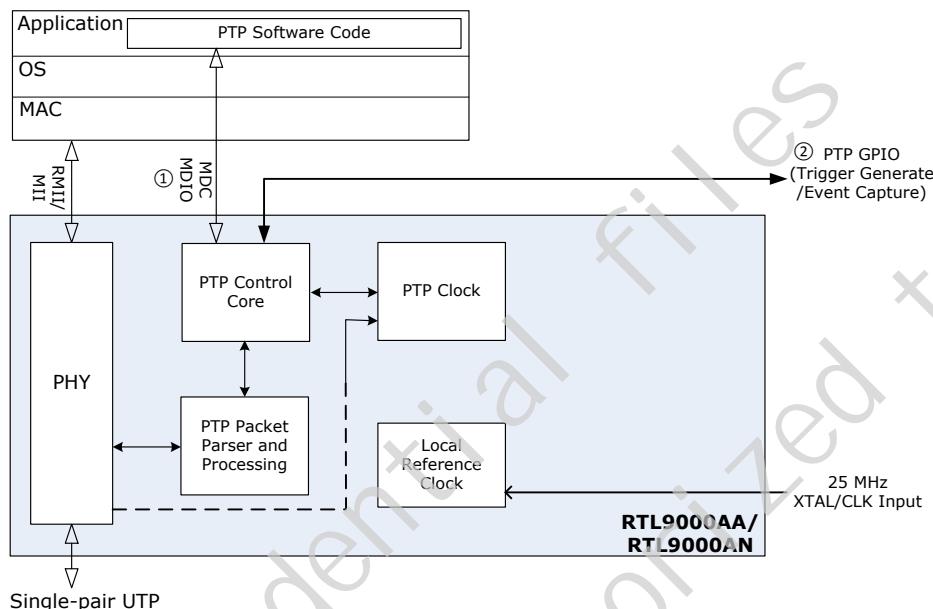


Figure 2. RTL9000AN General Application Diagram

### 3.2. PTP Application Diagram



**Figure 3. PTP Application Diagram**

- ①. By setting the PTP registers through the MDIO interface, the local PTP clock can be adjusted and synchronized according to the timing offset calculated by the upper layer software
- ②. A PTP GPIO provides Time Application Interfaces (TAI) to upper layer or external utilization. The TAI include Trigger Generate (supports periodic trigger with nanosec-level jitter) and Event Capture functions.

## 4. Block Diagram

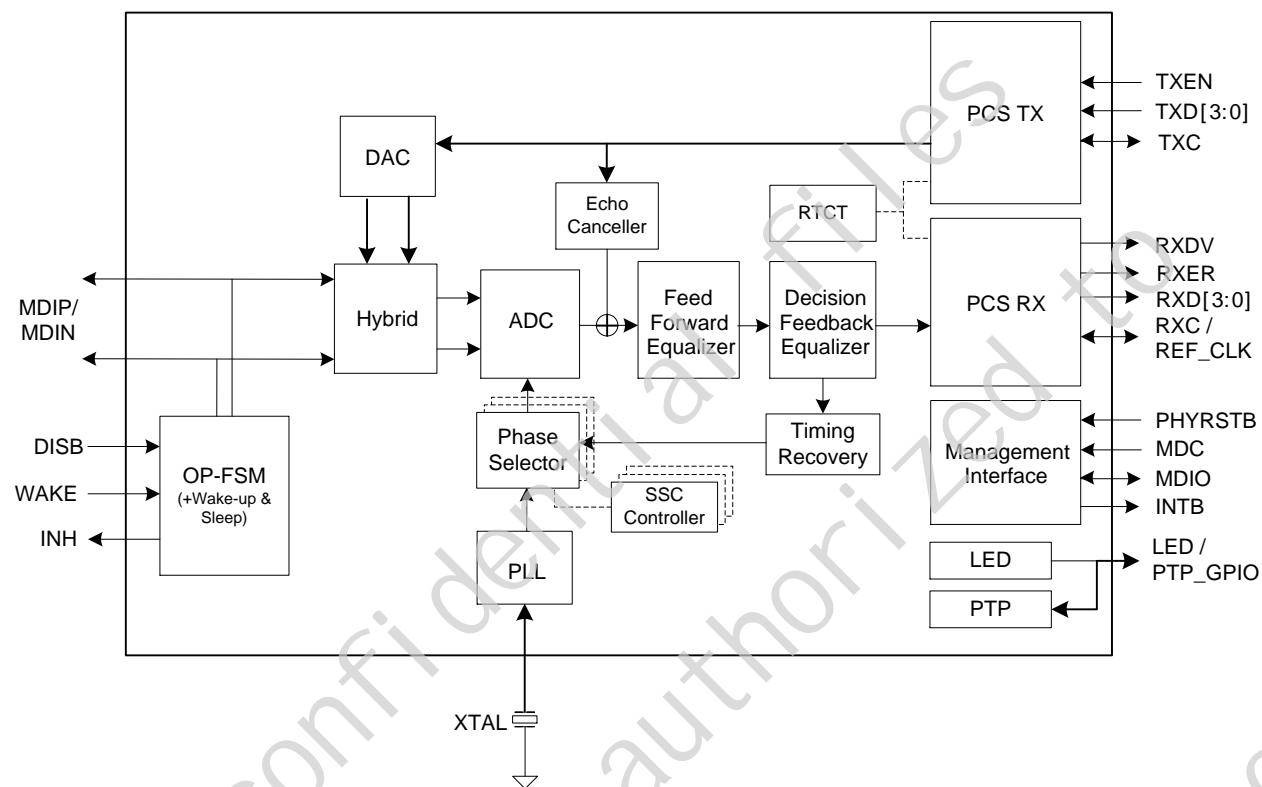


Figure 4. Block Diagram

## 5. Pin Assignments

### 5.1. RTL9000AA Pin Assignments (QFN-36)

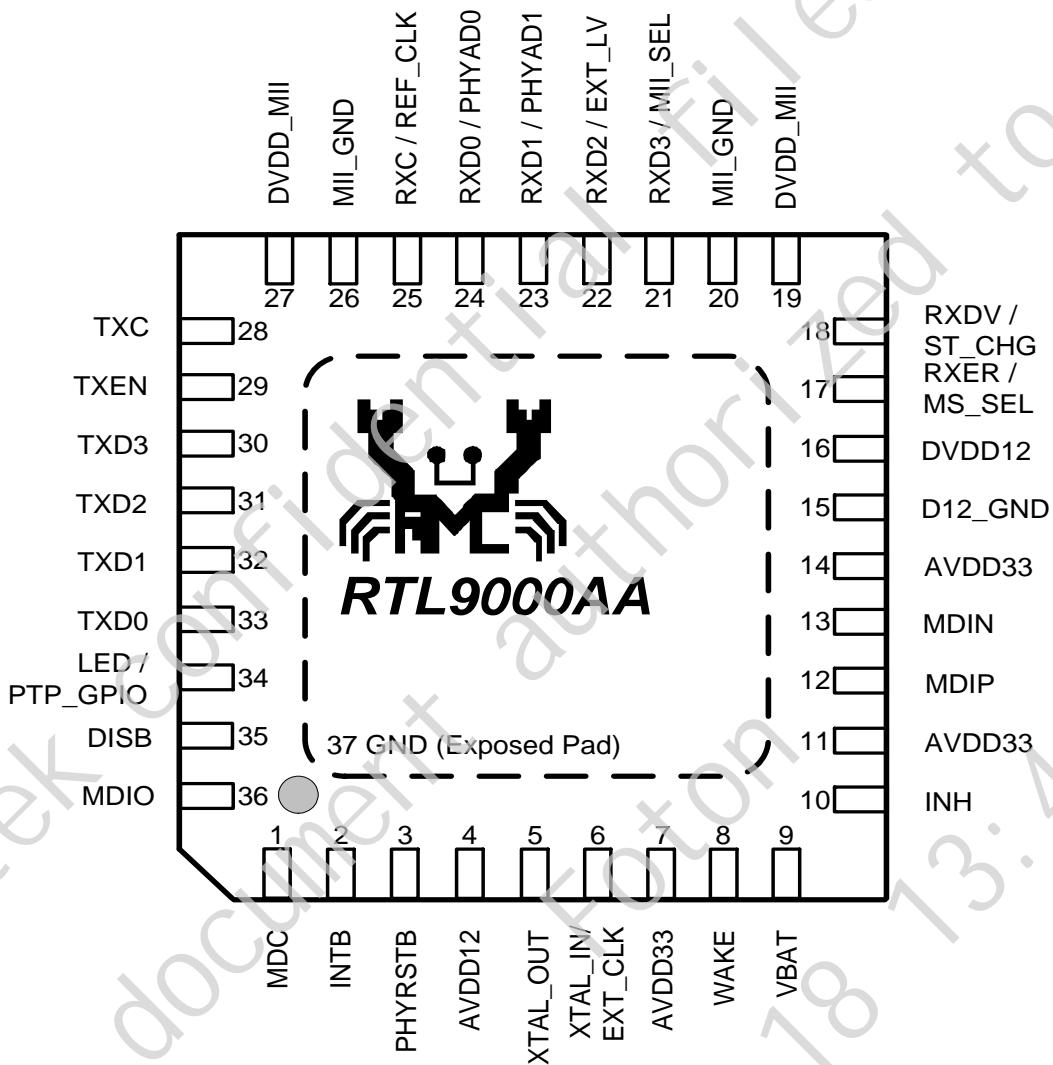


Figure 5. RTL9000AA Pin Assignments (QFN-36)

## 5.2. *RTL9000AN Pin Assignments (QFN-36)*

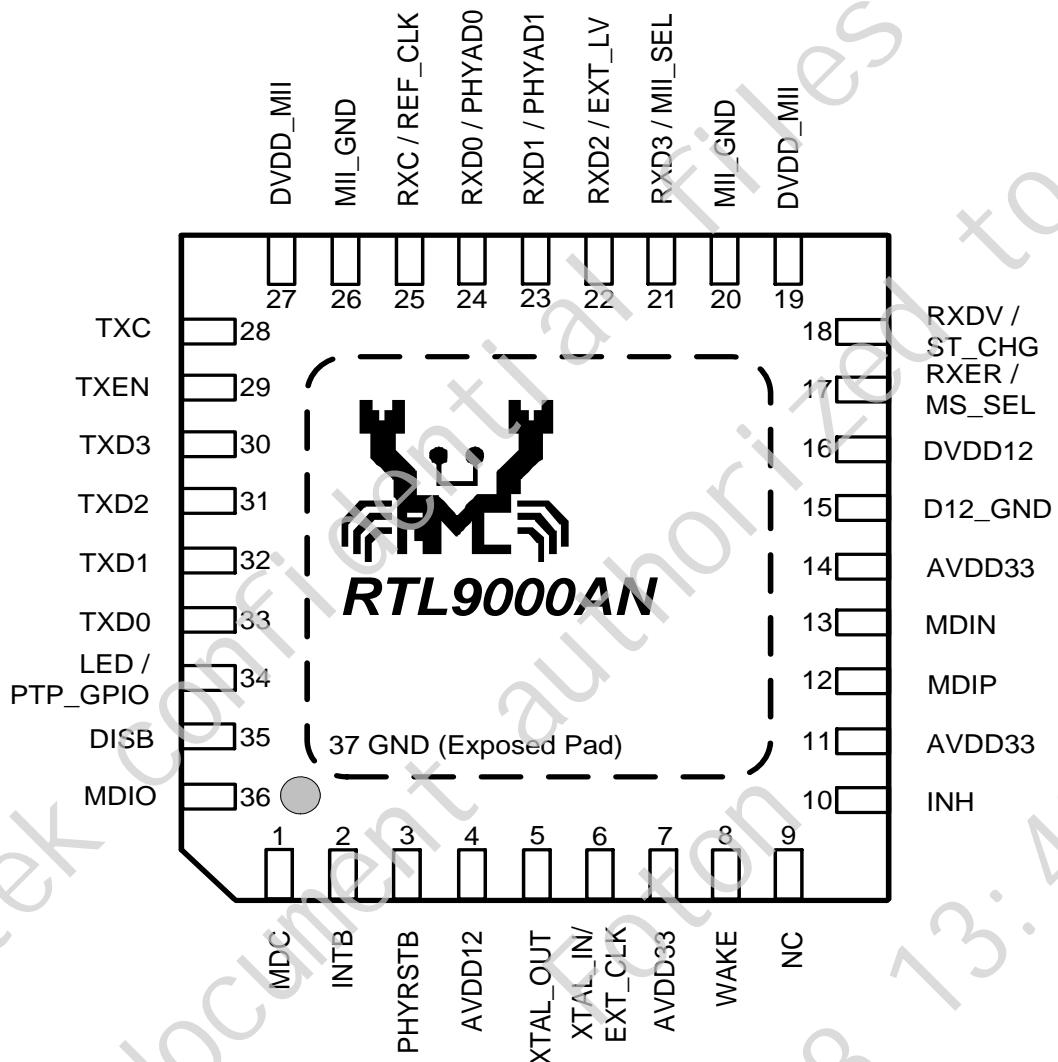


Figure 6. RTL9000AN Pin Assignments (QFN-36)

## 6. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignments figure on page 6 for a graphical representation.

I:	Input	LI:	Latched Input During Power up or Reset
O:	Output	IO:	Bi-Directional Input and Output
P:	Power	PD:	Internal Pull Down During Power On Reset
PU:	Internal Pull Up During Power On Reset	OD:	Open Drain
G:	Ground		

### 6.1. Transceiver Interface

**Table 1. Transceiver Interface**

Pin No.	Pin Name	Type	Description
12	MDIP	IO	Transceiver + / -.
13	MDIN	IO	

### 6.2. Clock

**Table 2. Clock**

Pin No.	Pin Name	Type	Description
6	XTAL_IN/ EXT_CLK	I	25MHz Crystal Input. / External Clock Input.  If a 25MHz oscillator is used, connect this pin to the oscillator's output (see section 10.9, page 92 for clock source specifications)
5	XTAL_OUT	O	25MHz Crystal Output

### 6.3. MII

**Table 3. MII**

Pin No.	Pin Name	Type	Description
28	TXC	O	Transmit Clock. The transmit reference clock will be 25MHz. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN signals. This pin is 5V-friendly (up to 5.25 V).
33	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0]. These pins are 5V-friendly (up to 5.25 V).
32	TXD1	I	
31	TXD2	I	
30	TXD3	I	

Pin No.	Pin Name	Type	Description
29	TXEN	I	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD[3:0]. This pin is 5V-friendly (up to 5.25 V).
25	RXC	O	Receive Clock.
24	RXD0	O/LI/PU	Receive Data.
23	RXD1	O/LI/PD	Data is transmitted from PHY to MAC via RXD[3:0].
22	RXD2	O/LI/PU	
21	RXD3	O/LI/PU	
18	RXDV	O/LI/PU	Receive Data Valid. This pin is asserted high when received data are present on RXD[3:0]. This signal is valid on the rising edge of RXC.
17	RXER	O/LI/PD	Receive Error. RXER is a required output from the PHY, but is an optional input to the MAC.

## 6.4. RMII

**Table 4. RMII**

Pin No.	Pin Name	Type	Description
28	TXC	Un-used	This pin is un-used in RMII mode, keep floating.
33	TXD0	I	Transmit Data.
32	TXD1	I	Data is transmitted from MAC to PHY via TXD[1:0]. These pins are 5V-friendly (up to 5.25 V).
31	TXD2	Un-used	This pin is un-used in RMII mode, keep floating.
30	TXD3	Un-used	This pin is un-used in RMII mode, keep floating.
29	TXEN	I	Transmit Enable. This pin is 5V-friendly (up to 5.25 V).
25	REF_CLK	IO	Synchronous 50MHz Reference Clock for Transmit, Receive, and Control Interfaces. When operating at RMII Output mode, this pin will output the 50MHz Reference clock. When operating at RMII Input mode, the Reference Clock should be inputted to this pin. In the RMII Input mode, this pin is 5V-friendly (up to 5.25 V).
24	RXD0	O/LI/PU	Receive Data.
23	RXD1	O/LI/PD	Data is transmitted from PHY to MAC via RXD[1:0].
22	RXD2	Un-used	This pin is un-used in RMII mode, keep floating.
21	RXD3	Un-used	This pin is un-used in RMII mode, keep floating.
17	RXER	O/LI/PD	Receive Error. RXER is a required output from the PHY, but is an optional input to the MAC.
18	RXDV	O/LI/PU	Receive Data Valid This pin is asserted high when received data are present on RXD[1:0]. This signal is asserted asynchronously to REF_CLK.

## 6.5. RGMII

**Table 5. RGMII**

Pin No.	Pin Name	Type	Description
28	TXC	I	Transmit Clock. The transmit reference clock should be supplied by 25MHz. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXCTL signals. This pin is 5V-friendly (up to 5.25 V).
33	TXD0	I	Transmit Data.
32	TXD1	I	Data is transmitted from MAC to PHY via TXD[3:0].
31	TXD2	I	These pins are 5V-friendly (up to 5.25 V).
30	TXD3	I	
29	TXEN	I	Transmit Control Signal from the MAC (i.e. TXCTL).
25	RXC	O	Receive Clock. This pin provides a continuous clock as a timing reference for RXD[3:0] and RXCTL signals.
24	RXD0	O/LI/PU	Receive Data.
23	RXD1	O/LI/PD	Data is transmitted from PHY to MAC via RXD[3:0].
22	RXD2	O/LI/PD	
21	RXD3	O/LI/PD	
17	RXER	Un-used	This pin is un-used in RGMII mode, keep floating.
18	RXDV	O/LI/PU	Receive Control Signal to the MAC (i.e. RXCTL).

## 6.6. LED / PTP Application Interface

**Table 6. PTP Application Interface**

Pin No.	Pin Name	Type	Description
34	LED / PTP_GPIO	IO	1. Debug LED (default) 2. PTP GPIO 3. PTP clock input from the external reference clock source. When as an input pin, this pin is 5V-friendly (up to 5.25 V). Keep this pin floating if the function is not used. Note: The function priority of pin 34 is as the above order when all of the functions are enabled. This pin will function as PTP GPIO by setting Address 0xD42A, bit[0] = 0 (see section 8.2.32, page 65); while setting Address 0xE410, bit[4] = 1 (see section 8.3.4, page 67), the PTP clock input function will take over.

## 6.7. Management Interface

**Table 7. Management Interface**

Pin No.	Pin Name	Type	Description
1	MDC	I	Management Data Clock. (MDC) Refer to section 10.10.1 MDC/MDIO Timing. This pin is 5V-friendly (up to 5.25 V).

36	MDIO	IO/PU	<p>Input/ Output of Management Data. (MDIO) Pull up to DVDD_MII. Register access can refer to 7.9.5 Register Access and 10.10.1 MDC/MDIO Timing. This pin is 5V-friendly (up to 5.25 V).</p>
2	INTB	O/OD	<p>Interrupt. Set low if status changed; active low. Keep this pin floating if the function is not used. <i>Note: The behavior of this pin is level-triggered.</i></p>
3	PHYRSTB	I/PU	<p>Hardware Reset. Active low. For a complete a PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after this hardware reset. This pin is 5V-friendly (up to 5.25 V).</p>
35	DISB	I/PD	<p>Disable packet transmission and MDIO will be read-only. Active low. Note that this pin is active low and internal pull down, there must to place a pull up resistor or the transmission will be disabled. This pin is 5V-friendly (up to 5.25 V).</p>
10	INH	O	<p>Output low when PHY is in the Sleep mode. The application of the INH pin can refer to section 7.3.1, Sleep mode. Keep this pin floating if the function is not used. The DC Characteristics of the INH pin is different between <b>RTL9000AA-VC</b> and <b>RTL9000AN-VC</b>, please refer to section 10.5.</p>
8	WAKE	I	<p>Local Wake-up Input. The edge detection can refer to section 7.5. The default setting is raising edge detection hence it is active high. The level of detection can be selected by OPCR1, section 8.4.1. The DC Characteristics of the WAKE pin is different between <b>RTL9000AA-VC</b> and <b>RTL9000AN-VC</b>, please refer to section 10.5.</p>

## 6.8. Power and Ground

**Table 8. Power and Ground**

Pin No.	Pin Name	Type	Description
9	VBAT ( <b>RTL9000AA-VC</b> )	P	<p>Connect to 12V/24V Car Battery. On the other hand, for application cases without 12V/24V power, this pin should be connected to main power 3.3V.</p>
	NC ( <b>RTL9000AN-VC</b> )	-	No connection pin.
7,11,14	AVDD33	P	<p>Analog 3.3V Power. Connect to main power 3.3V.</p>
4	AVDD12	P	<p>Analog 1.2V Power. Connect to pin 16 (DVDD12). See reference schematic of the RTL9000AA-VC/RTL9000AN-VC.</p>
16	DVDD12	P	<p>Digital 1.2V Power and Internal LDO Output. The digital 1.2V power is supplied by the internal LDO output directly inside the RTL9000AA-VC/RTL9000AN-VC.</p>

Pin No.	Pin Name	Type	Description
19,27	DVDD_MII	P	I/O Pad Power. Connect to main power 3.3V if configured as 3.3V I/O. The 2.5V/1.8V power could be supplied by the internal LDO output directly inside the RTL9000AA-VC/RTL9000AN-VC, refer to section 9.
20,26	MII_GND	G	Ground for I/O Pad Domain.
15	D12_GND	G	Ground for Digital Power Domain.
37	GND	G	Ground by Exposed Pad (E-Pad).

## 6.9. Hardware Strapping Configuration

Table 9. Hardware Strapping Configuration

Pin No.	Configuration	Type	Description
17 (RXER)	MS_SEL	O/LI/PD	Master / Slave Mode Configuration. 1: Master 0: Slave
21 (RXD3) 22 (RXD2)	MII_SEL_0 MII_SEL_1	O/LI/PD O/LI/PD	MII Mode Configuration. 2'b00: MII mode 2'b01: RMII mode (OUT) 2'b10: RGMII mode 2'b11: RMII mode (IN)
23 (RXD1) 24 (RXD0)	PHYAD_1 PHYAD_0	O/LI/PD O/LI/PU	PHY Address [1:0] Configuration.
18 (RXDV)	ST_CHG	O/LI/PU	Operating Modes (OP) State Change Condition Configuration The application for the ST_CHG can refer to section 7.3 Standby mode. 1: Auto mode, the PHY goes to Normal Mode automatically, when it power on/wake up/assert PHYRSTB to low. 0: Manual mode, the PHY goes to Normal Mode manually, when it power on/wake up/assert PHYRSTB to low. (The OP goes to sleep/normal command, refer to section 7.3.2.)

## 7. Function Description

### 7.1. Transmitter

The RTL9000AA-VC/RTL9000AN-VC's PCS layer receives data bytes from the MAC through the MII/RMII interface and performs generation of continuous code-groups through 2D-PAM3 coding technology. These code groups are transmitted onto the 1-pair CAT.5 cable at 66.67M Baud/s through a D/A converter, then the analog signal passes through a filter to minimize EMI effect.

### 7.2. Receiver

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, echo cancellation, timing recovery, and 2D-PAM3 decoding. The 8-bit-wide data is recovered and is sent to the MII/RMII interface at a clock speed of 25/50MHz. The Rx MAC retrieves the packet data from the receive MII/RMII interface and sends it to the Rx Buffer Manager.

## 7.3. Operating Modes (OP)

### 7.3.1. Operating Modes

The Figure 7 shows the transitions of the RTL9000AA-VC/RTL9000AN-VC's Operating Modes (OP). There are various modes in the PHY, including the Power-off, Sleep, Safety, Normal and Standby modes. Each operating mode has difference on power consumption (refer to section 10.4.), the availability of establishing the link and the MDIO command is accessible or not.

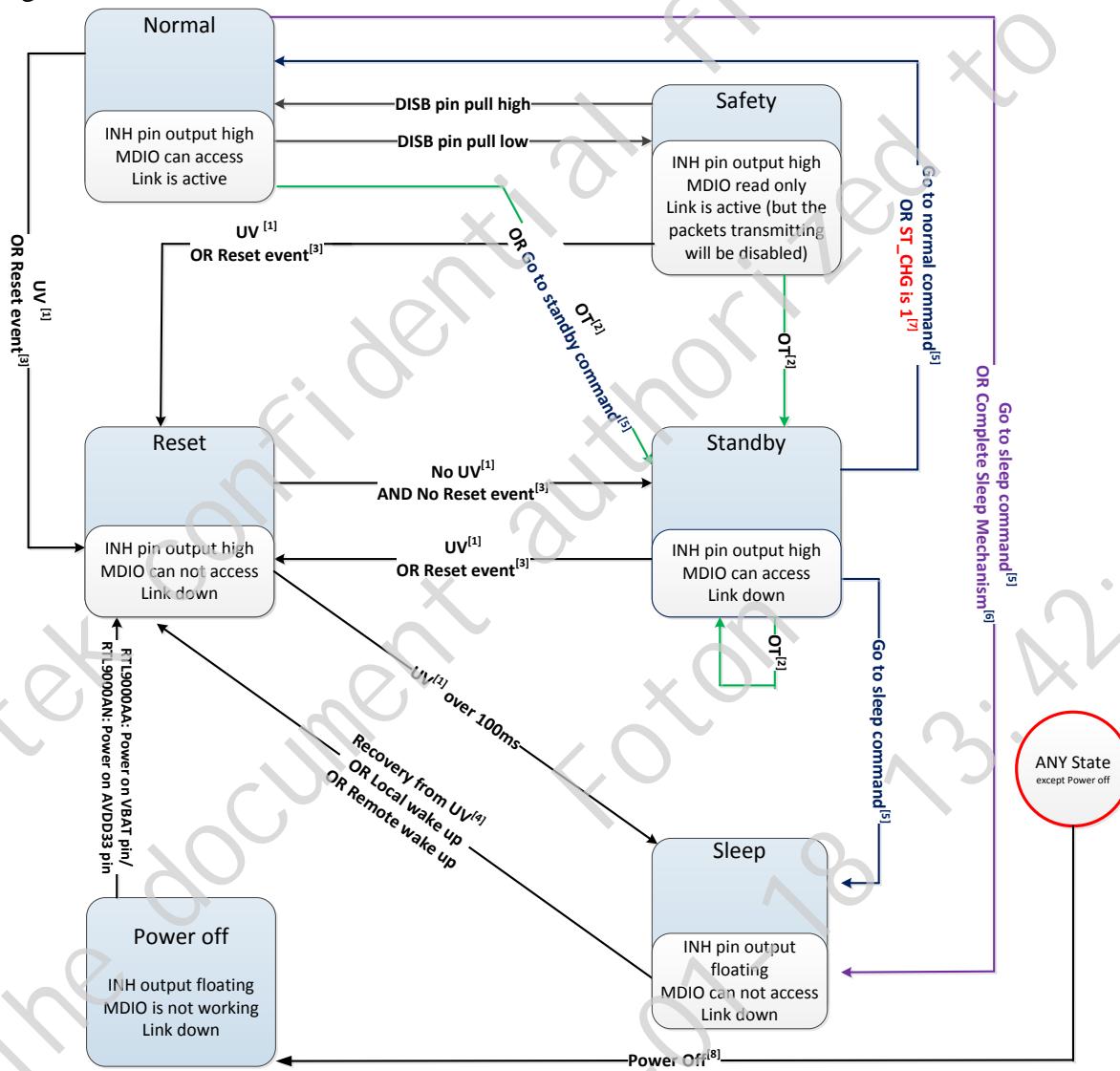


Figure 7. Operating mode transitions

## Power-off mode

RTL9000AA-VC remains in Power-off mode when the voltage on the VBAT pin is below the undervoltage (UV) threshold. For the RTL9000AN-VC, it will be in Power-off mode when the UV event happens on AVDD33 pins. When in Power off mode, all functions of PHY are disabled. When the PHY is power on, it goes to the Reset mode first.

## Sleep mode

RTL9000AA-VC/RTL9000AN-VC can be turned to Sleep mode for lower power consumption by “Go to sleep command” (section 8.4.2.) or “Complete sleep flow” (section 7.4). The UV events can also cause the PHY to enter Sleep mode. When the PHY is in Sleep mode, the data transmit and receive functions are disabled which means that the MDI twisted-pair lines can't transmit any signal. Also the transmit requests from the MII interface will be ignored. The MDIO read/write command can't access PHY in the Sleep mode.

According to the power supplied domain, there have two kinds of the Sleep modes, the one is the Deep Sleep mode which is to turn off the supply power of AVDD33 but keep that supply power of the VBAT pin to the car battery and optimize the system with ultra-low power consumption; the other is the Lite Sleep mode which is to supply the AVDD 33 and VBAT power permanently namely no power domain will be turned off. RTL9000AA-VC supports both of the Deep Sleep mode and the Lite Sleep mode. RTL9000AN-VC supports the Lite Sleep mode only because the RTL9000AN-VC has no the VBAT pin.

There are two implementations for the Deep Sleep mode, the first is the INH pin turns off the 3.3V external regulator of AVDD33 and only the VBAT pin is powered by car battery; the other is to supply the VBAT pin and main power separately and the supply AVDD33 power is turned off when the PHY is in the Deep Sleep mode. For RTL9000AA-VC, the INH pin will output floating in Sleep mode. For RTL9000AN-VC, the INH pin will be pulled low in Sleep mode. Note that the INH pin can't connect to the 3.3V external regulator of AVDD33 in RTL9000AN-VC, once the INH pin output low to turn off the AVDD33 power, the chip is power off in this case. The difference of DC Characteristics for the INH pin between RTL9000AA-VC and RTL9000AN-VC can refer to section 10.5.

When the device is in the Sleep mode, it can be woken up by local wake up (assert the WAKE pin, see section 7.5.1) or remote wake up (receive Wake Up Pattern (WUP) from its link partner, see section 7.5.2). Note that when the supply power of AVDD33 is recovered, the PHY will also be woken up from the Deep Sleep mode. When PHY wakes up, the INH pin will output high and the PHY will switch to Normal mode (set ST\_CHG to 1, refer to section 7.8) or Standby mode (set ST\_CHG to 0, refer to section 7.8).

## Reset mode

RTL9000AA-VC/RTL9000AN-VC will go to Reset mode when assert PHYRSTB pin low or receive the MDIO reset command (set Address 0xDD00, bit [5] = 1, refer to section 8.4.2). The PHY will be reset, that means all registers will be set to default value except for the OP registers in section 8.4. Note that when the MDIO Reset command complete Reset event, it will be self-cleared. The link can't be established and the MDIO command can't access when the PHY is in Reset mode.

### Standby mode

If the RTL9000AA-VC/RTL9000AN-VC is set as the manual mode (set ST\_CHG to 0, refer to section 7.8), when it power on/wake up, it will stay in the Standby mode. When the PHY is in the Standby mode, the link can't be established but the PHY can be accessed by the MDIO command. User can also set “Go to Normal /Sleep mode command to let PHY transit to other states, it can refer to section 8.4.2. In addition, the OT event will let PHY leave from the Normal or Safety to the Standby mode.

### Normal mode

To establish a valid link with the link partner, RTL9000AA-VC/RTL9000AN-VC must be operated in the Normal mode. If the PHY is set as the auto mode (set ST\_CHG to 0, refer to section 7.8), it will transfer to Normal mode automatically and activate the link after the power on/wake up.

### Safety mode

When the DISB pin is pulled low, RTL9000AA-VC/RTL9000AN-VC will transfer from the Normal to the Safety mode. In the Safety mode, the link is active but both of the packets transmitting and the MDIO write function would be disabled. That is to say, the PHY can be read only by the MDIO.

Table 10 presents an overview of the status of RTL9000AA-VC/RTL9000AN-VC functional blocks in each operating mode.

**Table 10. Overview of the Operating States**

	<b>Power-off</b>	<b>Sleep</b>	<b>Reset</b>	<b>Standby</b>	<b>Normal</b>	<b>Safety</b>
<b>MDI Impedance</b>	Open/High impedance	100ohm	100ohm	100ohm	100ohm	100ohm
<b>Link status</b>	passive	passive	passive	passive	active	active
<b>WUP detection</b>	off	on	on	On	off	off
<b>OT detection</b>	off	off	off	On	on	on
<b>INH pin output</b>	Floating/Low	Floating/Low	High	High	High	High
<b>MDIO command</b>	Not accessible	Not accessible	Not accessible	▲ Read/Write in general condition ▲ Read only when DISB pin pull low	Read/Write	Read only
<b>PHY be Reset or not</b>	Yes	Yes	Yes	No	No	No

### 7.3.2. Operating Mode Transition

- The following events, listed in order of priority, trigger mode transitions:
  - RTL9000AA-VC:** Undervoltage on VBAT pin  
**RTL9000AN-VC:** Undervoltage on A VDD33 pin
  - Undervoltage on other power pin.
  - Reset event

4. OT event
5. Local wake up, Remote wake up
6. Go to sleep/normal/Standby command (Refer to section 8.4.2.)
7. Hardware strapping pin (The setting of ST\_CHG, refer to section 7.8.)

As an example, if the ST\_CHG is set to 1 then set the PHY go to Standby mode command, the PHY will go to the Standby mode but will not go back to Normal mode automatically. Because the go to Standby mode command is prior to strap pin (set the ST\_CHG to 1).

- **OP Go to Sleep/Normal/Standby command (Refer to section 8.4.2):**

The register table shown in the section 8.4.2 states all of Go to Sleep/Normal/Standby commands, please be aware that only the OP go to Normal command must be combined with op\_cmd\_2 in section 8.4.13. Furthermore, the OP Go to Sleep/Normal/Standby command would be cleared in the following conditions:

1. The PHY goes to the Sleep mode.
2. UV event occurs in the Normal/Safety mode.
3. Reset event occurs in the Normal/Safety mode.
4. OT event occurs in the Normal/Safety mode.
5. Wake up event occurs in any state. (Option to set OCPR3 at section 8.4.3.)

- **OP event flags:**

The RLT9000AA-VC/RTL9000AN-VC support the flags of UV/ UV recovery/ Wake up/ Sleep/ OT Power on and these flags can refer to section 8.4.4, section 8.4.7 and section 8.4.10. In order to ensure the next wake up even can be detected, note that lwake\_flag and rwake\_flag (in section 8.4.10) will be cleared if the following events happen.

1. PHY goes to the Reset or Standby from the Normal mode.
2. PHY goes to the Reset or Standby from the Safety mode.
3. PHY goes to the Sleep mode from any state.

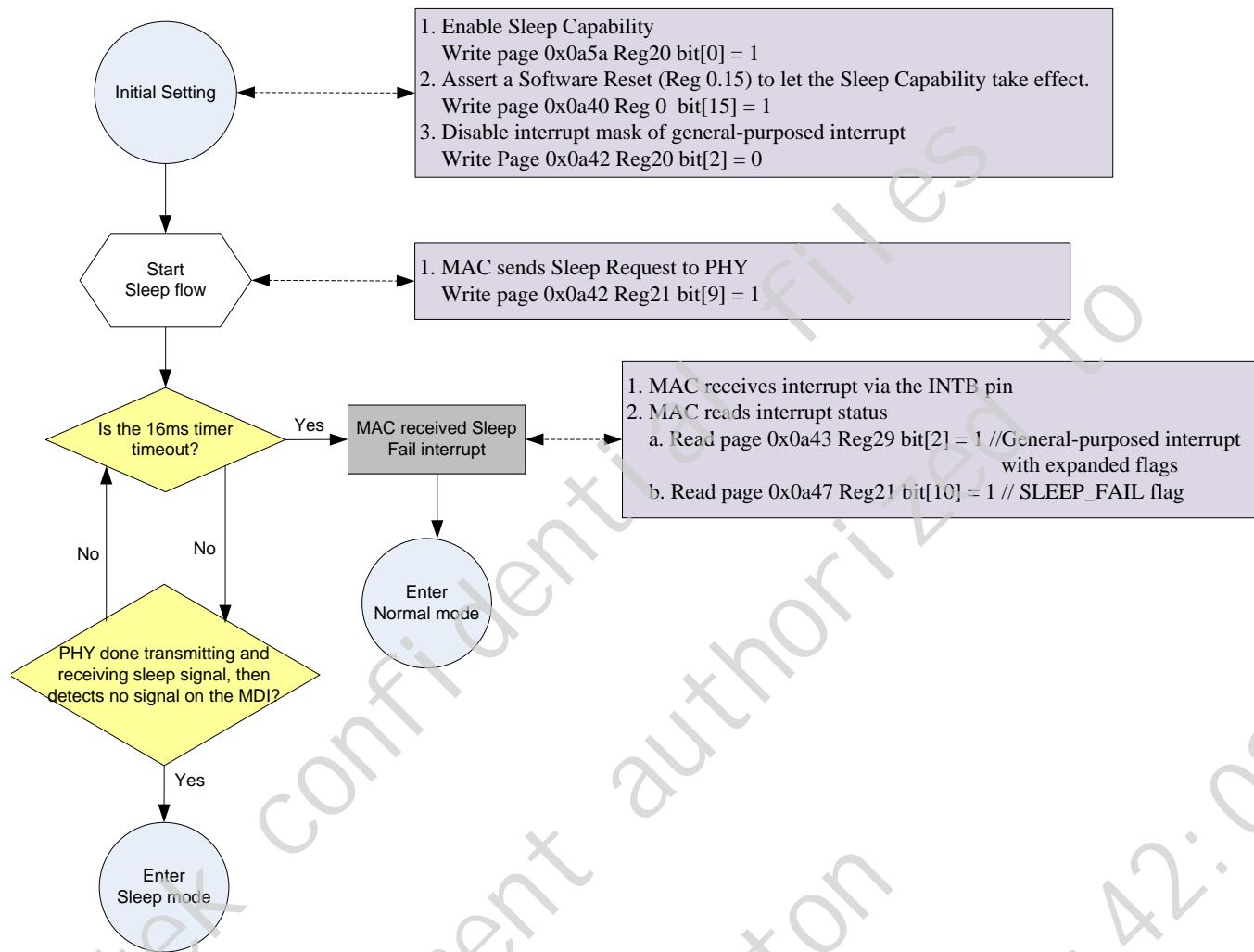
## 7.4. Sleep Mechanism

The RTL9000AA-VC/RTL9000AN-VC support OPEN Alliance TC10 Sleep/Wake-up function for automotive Ethernet. The Sleep function implements the PHY into the Sleep mode which has lower power consumption, refer to section 10.4.

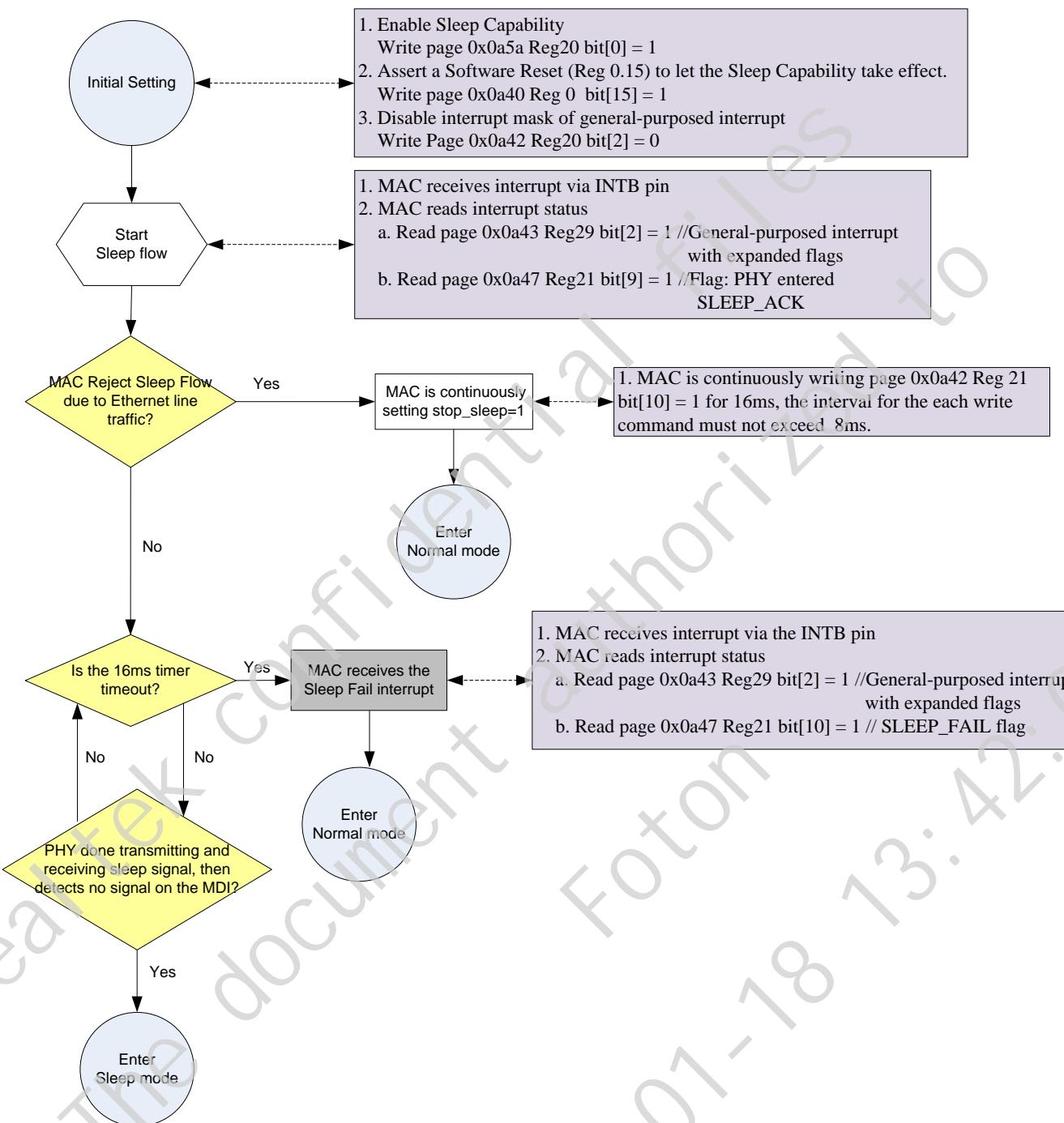
To enable the Sleep function, the register at Page 0xA5A Reg 20 bit [0] must be set to 1, refer to section 8.2.22 and assert a software reset at Page 0x0 Reg 0x0 bit [15] as 1 to let the Sleep capability to take effect. When the MAC gives a sleep request (refer to section 8.2.13) to the PHY (called Sleep Initiator), the PHY will start to do sleep handshaking flow with its link partner (called Sleep Responder). Note that the sleep handshaking flow is available only when both of PHYs (Sleep Initiator and Sleep Responder) are in the Normal mode and their link is active. The sleep flow is success if both PHYs finish the sleep handshaking (transmitted and received sleep signal on the MDI) properly, then both of them can enter the Sleep mode together.

This sleep mechanism is able to reject sleep flow and deal with the sleep fail case as well. At the beginning of the sleep flow, the Sleep Initiator transmits the sleep signal to Sleep Responder. The Sleep Responder will indicate its upper layer (namely MAC) through pulling the INTB pin low. If the MAC don't want the Sleep Responder to go to Sleep mode because of the unfinished transmission, the MAC can continuously set stop\_sleep to 1 (see section 8.2.13) for 16ms, the interval for each stop\_sleep command must not exceed 8ms. Then the sleep handshaking flow will be rejected and both of the Sleep Initiator and the Sleep Responder will stay in the Normal mode, the link between them will remain active. If the link between the Sleep Initiator and the Sleep Responder is accidentally interrupted while the handshaking of the sleep flow is in progress, the sleep flow will fail and both Sleep Initiator and Sleep Responder will stay in Normal mode.

Figure 8 shows the flow chart for the Sleep Initiator, and Figure 9 shows the flow chart for the Sleep Responder. The transition and status of the Sleep mode can refer to section 7.3.1.



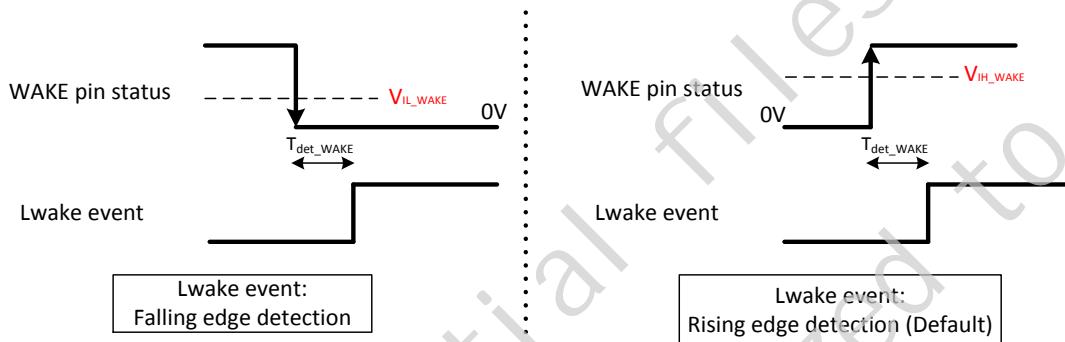
**Figure 8. Flow Chart of Sleep Mechanism of Sleep Initiator**



**Figure 9. Flow Chart of Sleep Mechanism of Sleep Responder**

## 7.5. Wake-up

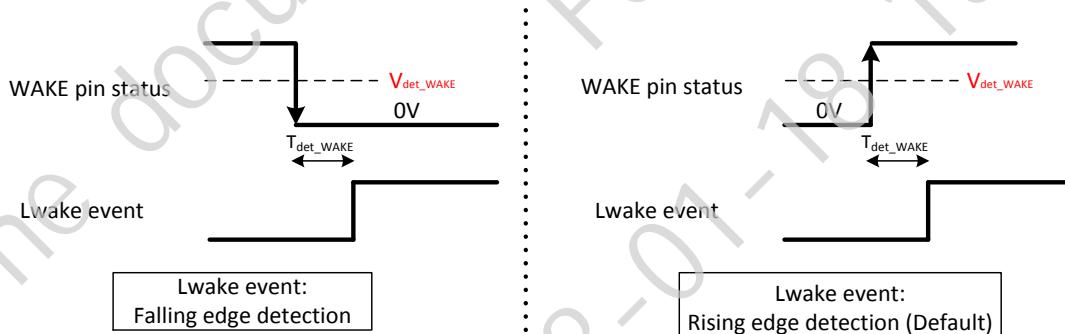
### 7.5.1. Local Wake-up



**Figure 10. RTL9000AA Local Wake Up (Lwake) Event Detection**

When RTL9000AA-VC/RTL9000AN-VC is in Sleep mode, they can be woken up by detecting local wake pulse on the WAKE pin. There have two kinds of detection for the local wake up event (Lwake event), the one is rising edge detection; the other is falling edge detection. The rising/falling edge detection can be configured by setting specified register (Address 0xDC0C, bit [5] = 0 for the rising edge detection; set to 1 for falling edge detection, see section 8.4.1, page 75). Note that the default is set as rising edge detection. The DC Characteristics of the WAKE pin is different between RTL9000AA-VC and RTL9000AN-VC, please refer to section 10.5.

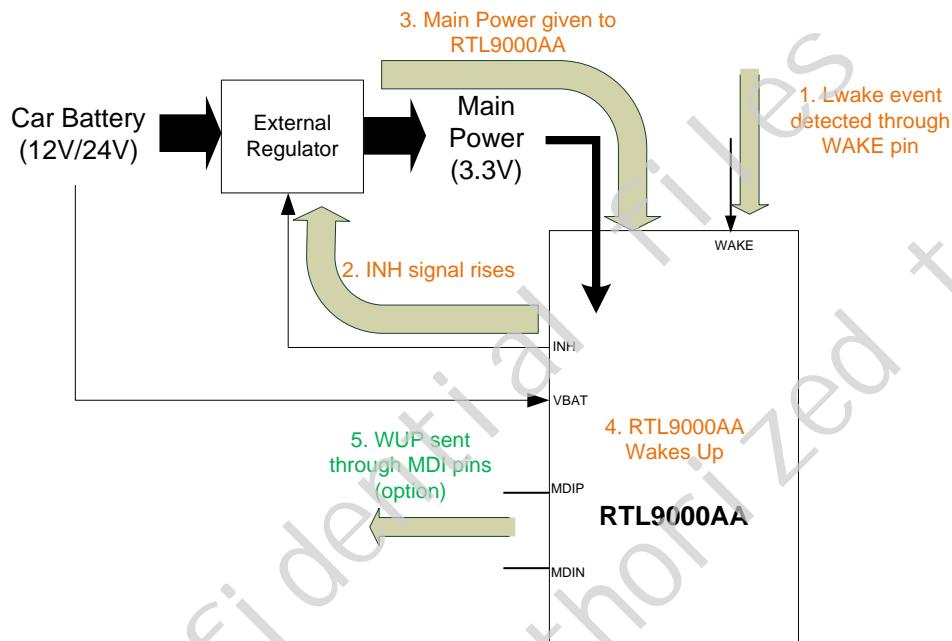
As shown in Figure 10, in the RTL9000AA-VC, if the rising edge detection is chosen, the RTL9000AA-VC detects a Lwake event when the voltage on the WAKE pin is higher than detective high-level voltage  $V_{ih\_WAKE}$  (rising edge on the WAKE pin) for longer than detective time  $T_{det\_WAKE}$ . If the falling edge detection is chosen, the RTL9000AA-VC detects a Lwake event when the voltage on the WAKE pin is lower than detective low-level voltage  $V_{il\_WAKE}$  (falling edge on the WAKE pin) for longer than detective time  $T_{det\_WAKE}$ .



**Figure 11. RTL9000AN Local Wake Up (Lwake) Event Detection**

As shown in Figure 11, in the RTL9000AN-VC, there only has a detective level voltage  $V_{det\_wake}$  for both rising and falling edge. If the rising edge detection is chosen, the RTL9000AN-VC detects a Lwake event when the voltage on the WAKE pin is higher than detective level voltage  $V_{det\_WAKE}$  (rising edge on the WAKE pin) for longer than detective time  $T_{det\_WAKE}$ . If the falling edge detection is chosen, the

RTL9000AN-VC detects a Lwake event when the voltage on the WAKE pin is lower than detective level voltage  $V_{det\_WAKE}$  (falling edge on the WAKE pin) for longer than detective time  $T_{det\_WAKE}$ .



**Figure 12. RTL9000AA Wake Flow for Local Wake up with the INH pin**

As shown in Figure 12, in the application of the Deep Sleep mode of RTL9000AA-VC, after detecting local wake pulse on the WAKE pin, the INH signal rises and then turns on the external regulator. Thus, the whole chip is powered on by the 3.3V voltage output from the external regulator.

As shown in Figure 13 and Figure 14, in the application of the Lite Sleep mode in both of RTL9000AA-VC/RTL9000AN-VC, after detecting local wake up pulse, the functions which are disabled in Sleep mode will recover.

After a local wake up, RTL9000AA-VC/RTL9000AN-VC will remote wake up its link partner automatically by sending the WUP on the MDI pins. If the application does not want the PHY to remote wake up its link partner automatically, user can set register at Address 0xDC0E, bit [0] to 0 and pull low the ST\_CHG pin, then the PHY will stay in Standby mode and its link partner won't be woken up.

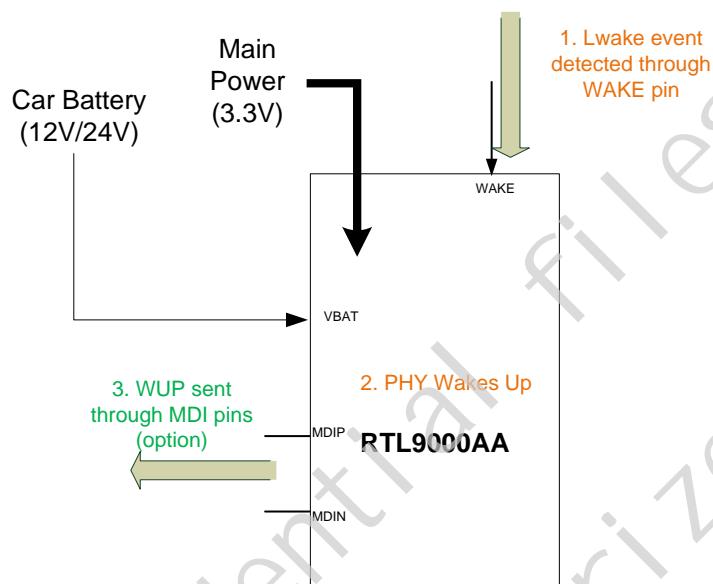


Figure 13. RTL9000AA Wake Flow for Local Wake up without the INH pin

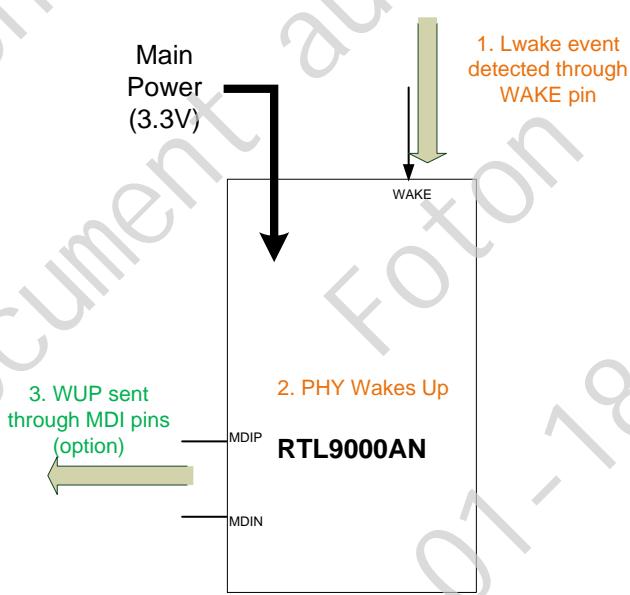


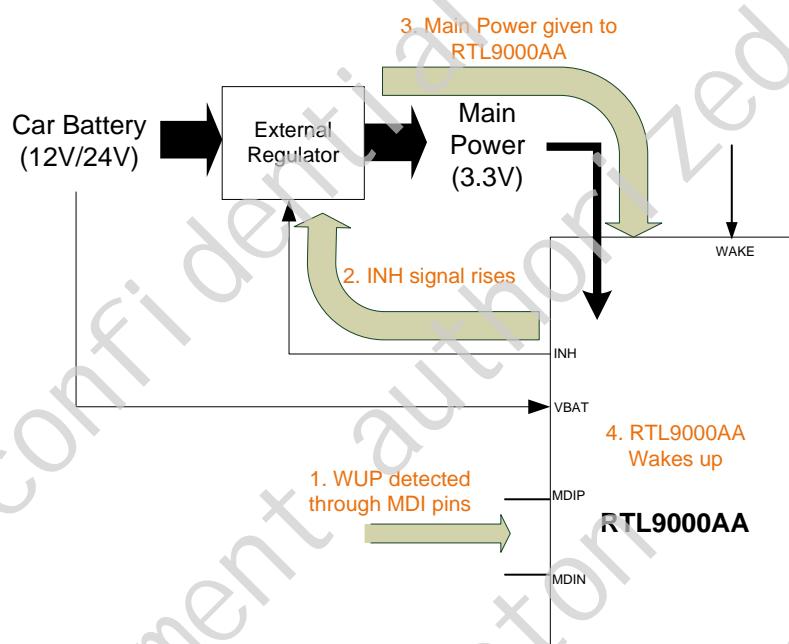
Figure 14. RTL9000AN Wake Flow for Local Wake up

### 7.5.2. Remote Wake-up

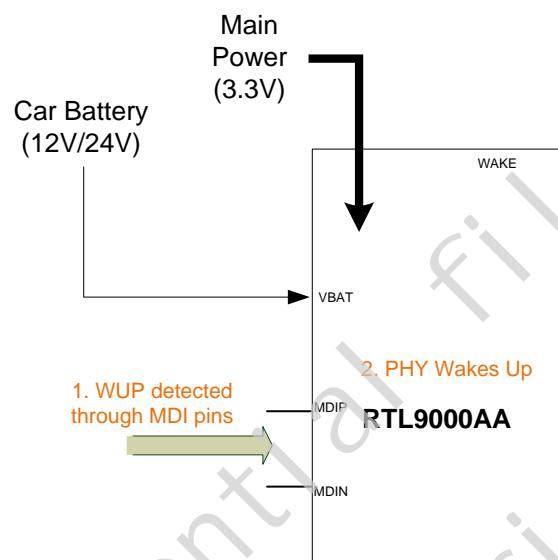
The RTL9000AA-VC/ RTL9000AN-VC detects a ‘Remote wake-up’ (Rwake) event when it detects the WUP on the MDI pins. By the similar sequence as the local wake up as shown in Figure 15 and

Figure 16 and Figure 17, RTL9000AA-VC/RTL9000AN-VC are woken up by a remote wake up which is woken up by the WUP detected through MDI interface instead of the WAKE pin. In the application of the Deep Sleep mode of RTL9000AA-VC, after detecting the WUP on the MDI pins, the INH pin rises and then turns on external regulator. Thus, the whole chip is powered on by the 3.3V voltage output from the external regulator. In the application of the Lite Sleep mode in both of RTL9000AA-VC/RTL9000AN-VC, after detecting WUP on the MDI pins, the functions which are disabled in Sleep mode will recover.

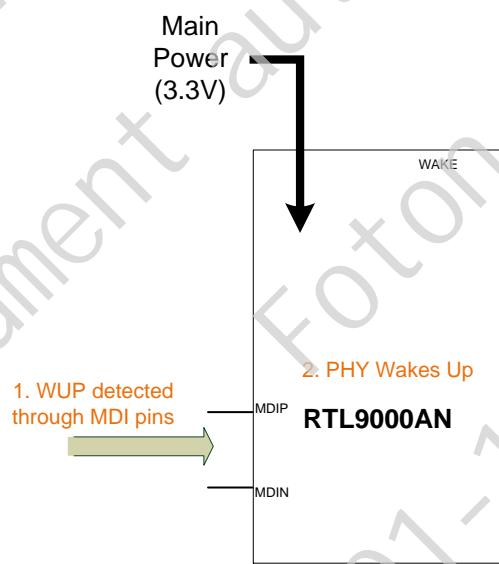
If the PHY is staying the Standby mode and wants to remote wake up its link partner which in the sleep mode, by setting register at Address 0xDD20, bit [4] to 1 will make the PHY to remote wake-up its link partner in this case.



**Figure 15. RTL9000AA Wake Flow for Remote Wake Up with the INH pin**



**Figure 16. RTL9000AA Wake Flow for Remote Wake Up**



**Figure 17. RTL9000AN Wake Flow for Remote Wake Up**

## 7.6. Precision Time Protocol (PTP)

Precision Time Protocol (PTP) stands for a series of IEEE specifications, including IEEE 1588 Ver. 1, IEEE 1588 Ver. 2, and IEEE 802.1AS, that synchronize the time of the day or a standard time across a network system. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is time-stamping specified PTP frames with high precision as close to the transmission media as possible. Time stamping in the PHY provides increased accuracy compared to time-stamping in the MAC or higher layers.

The PTP core in the RTL9000AA-VC/RTL9000AN-VC consists of three main blocks:

- Packet Time Stamping
- Synchronized PTP Clock
- Time Application Interface (TAI)
- Hardware offload timestamp update (one-step and two-step mode)

By combining the above functions, the RTL9000AA-VC/RTL9000AN-VC provides complete and accurate support for applications in a time-synchronous system.

### 7.6.1. Synchronized PTP Clock

Based on the PTP specification requirements, the integrated PTP clock of the RTL9000AA-VC/RTL9000AN-VC consists of the following time fields: seconds (48 bits), nanoseconds (30 bits), and fractional nanoseconds (in units of  $2^{-32}$  ns).

The RTL9000AA-VC/RTL9000AN-VC provides several ways to access and update this internal PTP clock. The methods are listed below:

- Direct Read/Write
- Step Adjustment
- Rate Adjustment

A **Direct Write** of the time value is done by setting a new value to all time fields. This function may be used when initializing a PTP synchronization that need an immediate setting to the time value due to the local PTP time being far apart from the Master clock time. Also for the PTP Master, it can be used to assign the standard time directly.

A **Step Adjustment** is an alternative method for making a quick compensation to the PTP clock time. Note that the adjustment can be incremented and decremented.

When the local time is close enough to the PTP Master, **Rate Adjustment** is a better way to fine-tune the time and frequency drift. The Rate Adjustment allows for correction on the order of  $2^{-32}$  ns per clock cycle, it can correct the offset over time accurately.

Refer to section 8.3, page 66, for detailed register settings.

## 7.6.2. Packet Time Stamping

The PTP packet parser in the RTL9000AA-VC/RTL9000AN-VC continually monitors transmit/receive packet data in order to detect IEEE 1588 Ver. 1, Ver 2 or 802.1AS Event Messages. The PTP packets transported in Layer 2 Ethernet, IPv4/UDP, or IPv6/UDP packet formats will be recognized automatically. Upon detection of a PTP Event Message, the RTL9000AA-VC/RTL9000AN-VC will capture the specific transmit/receive timestamp and provide it to the software at the upper layer through PTP\_TRX\_TS registers (see section 8.3.17 to 8.3.25, page 71~74). A PTP interrupt can be generated, if enabled, upon a transmit/receive timestamp ready.

### 7.6.2.1 One-Step and Hardware-assisted Two-Step Operation

In some transmission cases, the RTL9000AA-VC/RTL9000AN-VC supports One-Step operation: The egress timestamp of a Sync message is on-the-fly inserted to the Sync itself, with no need for Follow-Up messages.

Furthermore, a Hardware-assisted Timestamp Insertion feature is imbedded, which will insert receive timestamps directly into the next Follow-Up/Delay-Response packets via hardware; software does not need to access timestamp registers.

After gathering the timestamp information, the upper layer software can compute the difference between the local time and the PTP Master's central clock time, and use the three methods in section 7.6.1 to tune the local PTP clock, in order to sync the local PTP clock to the master clock.

## 7.6.3. Time Application Interface (TAI)

When the end-point's PTP clock is synchronized to the PTP Master clock, its time information and local clock can be provided to peripheral time applications that need to work simultaneously with the central clock. The RTL9000AA-VC/RTL9000AN-VC features these time application interfaces in the following, via the PTP\_GPIO pin:

### Event Capture interface:

- Monitors the PTP\_GPIO pin, and records the timestamp of incoming pulses, edges, or time alignment signals, similar to a stopwatch.

### Trigger Generate interface:

- Arms the PTP\_GPIO pin to generate a pulse, edge, or periodic clock signal at a specific time, similar to an alarm clock. The periodic clock has configurable period and duty cycles.
- PTP clock input from the external reference clock source with 10M/25M/125MHz via the PTP\_GPIO.

The related TAI configurations can be set by PTP\_TAI registers (section 8.3.10 to 8.3.16, page 69~71).

## 7.6.4. PTP Function Configuration

### 7.6.4.1 Enable & Disable PTP Function

PTP capability configuration is defined in the section 8.3.1, including protocol support types and PTP enable register. It is usually set the capability at the initial stage of the PTP program.

After setting the PTP capability, a PHY reset must be issued (Page 0, Reg 0, bit [15] = 1). Then the PTP function will start working.

#### 7.6.4.2 PTP Synchronization mechanism

- Two-step PTP Synchronization:

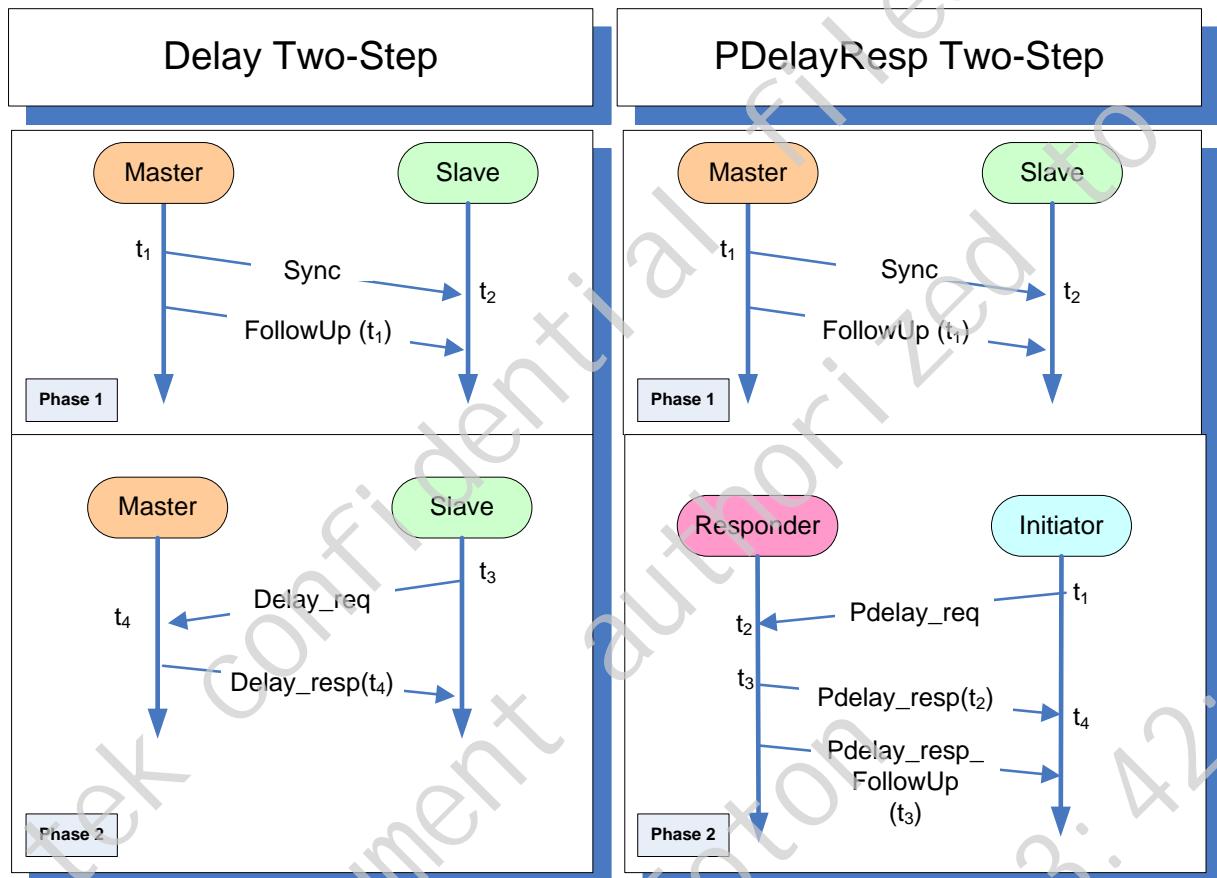
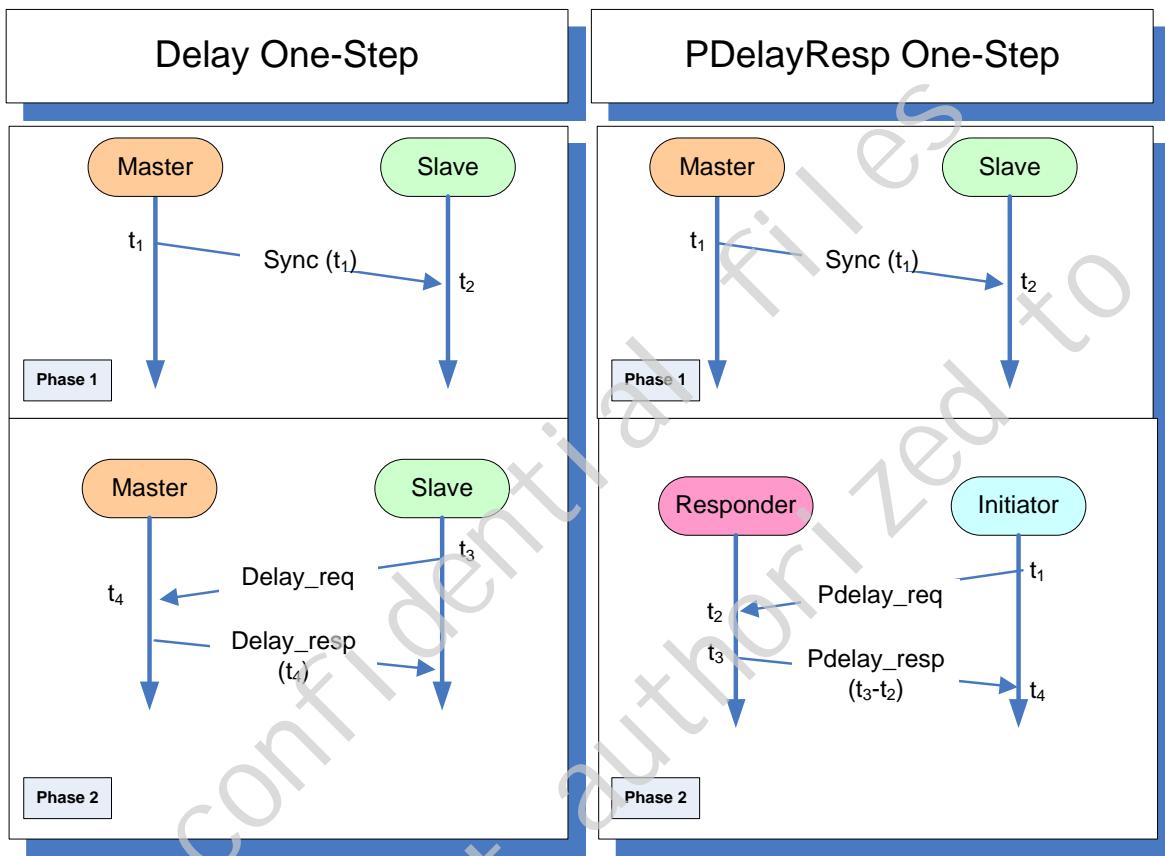


Figure 18. Two-step PTP Synchronization

- One-step PTP Synchronization:



**Figure 19. One-step PTP Synchronization**

#### **Calculation of Offset\_from\_Master :**

The time offset between a Slave and a Master clock is defined as follows:

$$\text{Offset\_from\_Master} = t_2 - t_1 - \text{MeanPathDelay}$$

#### **Calculation of Mean\_Path\_Delay :**

For delay between Master and Slave –

Calculate the timestamp at both phase 1 & phase 2 stage

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

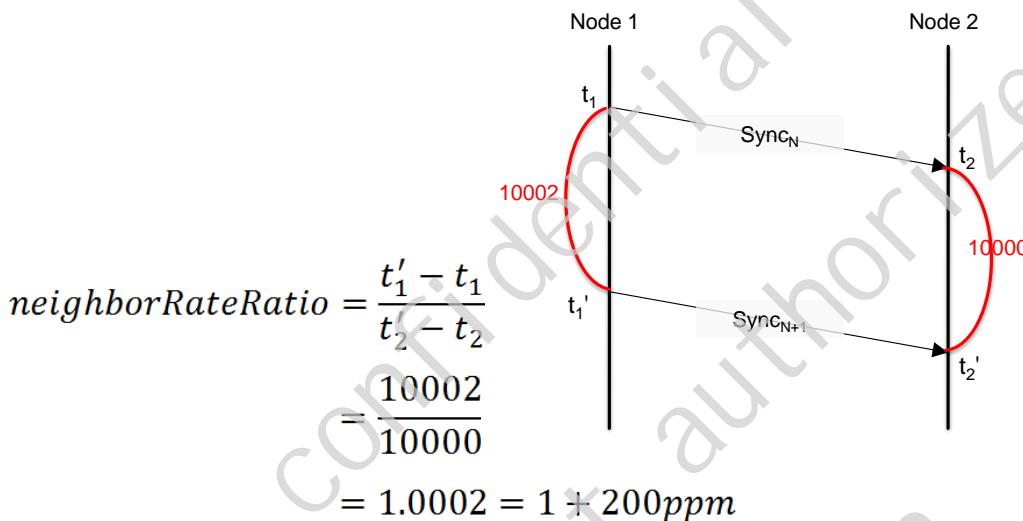
For delay between Responder and Initiator –

Calculate the timestamp at phase 2 stage

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

\*Note: For the RTL9000AA-VC/RTL9000AN-VC, PDelayResp one-step correctionField update will not exactly match <PDelayResp Egress Timestamp (t3) > - <PDelayReq Ingress Timestamp (t2) >. Because a more accurate timer with resolution  $2^{-3}$  ns is used to calculate the value. The difference would be smaller than 1ns compared to the result of <PDelayResp Egress Timestamp (t3) > - <PDelayReq Ingress Timestamp (t2) >.

### **Calculation of Frequency\_Drift:**



**Figure 20. Calculation of neighborRateRatio**

### **Read Tx/Rx TimeStamp**

The time stamp is recorded by the chip after receiving or transmitting a PTP message packet.

Before read the time stamp value, the READY flags should be checked first. If the READY flag is set, it means the timestamp is prepared and recorded completely. The flags are read-cleared type, and defined at bit [15:8] in section 7.9.5.2.

After checking the READY flag of time stamp, we must select the protocol message type and the message direction (Transmit/Receive) for corresponding time stamp. Then set Transmit/Receive Timestamp Read Enable bit. These registers are defined in bit[4:0] of section 7.9.5.2.

The time stamp information is shown on PTP TxRx Timestamp registers (see section 8.3.18 to 8.3.25, page 72~74).

The PTP version is shown by ‘trxts\_ptpver’ and ‘trxts\_transpec’ fields in Table 72, page 72.

\*IEEE 1588 v1: ptpver = 1

\*IEEE 1588 v2: ptpver = 2 , transpec = 0

\*802.1AS: ptpver = 2; transpec = 1

Furthermore, the PTP packet type will be indicated by of ‘trxts\_msgtype’ in Table 72, which is summarized as the table below:

**Table 11. Summary of PTP Packet Types**

Value of 'trxts_msgtype' (in HEX)	IEEE 1588 v1 Packet Type	IEEE 1588 v2 & 802.1AS Packet Type
0	Sync	Sync
1	Delay_Req	Delay_Req
2	Follow_Up	Pdelay_Req
3	Delay_Resp	Pdelay_Resp
4-7	Management	Reserved
8	-	Follow_Up
9	-	Delay_Resp
A	-	Pdelay_Resp_Follow_Up
B	-	Announce
C	-	Signaling
D	-	Management
E-F	-	Reserved

The Source Port ID of each the PTP packet will be indicated by a 16-bit 'trxts\_srchash' field by RTL9000AA-VC/RTL9000AN-VC in order for the software to distinguish the packet sender (see Table 73, page 72). The rule of transforming Source Port ID into its Hash Value (trxts\_srchash) is listed in the following example:

#### For IEEE 1588 v1:

SourcePortIdentity (8-byte, in HEX) = 11 22 33 44 55 66 AA BB

Hash Value Computation:

*Step 1.* Convert to a 10-byte SourcePortIdentity (in HEX) = 11 22 33 **00 00** 44 55 66 AA BB

*Step 2.* Sum the SourcePortIdentity every 2 bytes:

$$0x1122 + 0x3300 + 0x0044 + 0x5566 + 0xAABB = 0x0001\_4487$$

*Step 3.* Add high 16-bit with low 16-bit:

$$\text{Hash Value (trxts_srchash[15:0])} = 0x0001 + 0x4487 = \underline{\underline{0x4488}}$$

#### For IEEE 1588 v2 & 802.1AS:

SourcePortIdentity (10-byte, in HEX) = 11 22 33 **FF FE** 44 55 66 AA BB

Hash Value Computation:

*Step 1.* Sum the SourcePortIdentity every 2-byte:

$$0x1122 + 0x33FF + 0xFE44 + 0x5566 + 0xAABB = 0x0002\_4386$$

*Step 2.* Add high 16-bit with low 16-bit:

$$\text{Hash Value (trxts_srchash[15:0])} = 0x0002 + 0x4386 = \underline{\underline{0x4388}}$$

## Set PTP Clock Time

There are three modes for PTP clock adjustment to PTP Local Time through PTP Time Config registers:

- (1) Direction Read/ Write clock,
- (2) Increment / Decrement step adjustment
- (3) Read/ Write rate adjustment

The register is defined at section 8.3.4 PTP\_CLK\_CFG (PTP Clock Config Register, Address 0xe410) – bit [3:1].

In addition, the desired adjustment value should be filled in PTP Time Config registers (section 8.3.5 to 8.3.9 , page 68~68).

After setting the PTP Clock adjustment value, set the PTP clock adjustment Activate bit. The register bit is defined at bit [0] of PTP\_CLK\_CFG register (i.e. set Address 0xE410, bit [0] = 1).

*\*Note 1: It is suggested that the time differences from the Egress Timestamp point to the MDI, and from the MDI to the Ingress Timestamp point should all be taken into account in order to attain more accurate PTP clock tuning.*

*\*Note 2: The Direct Write would be another suitable method for the very initialization, where a setup with a whole new time value is needed.*

*\*Note 3: For the case that the value of Offset\_from\_Master is greater than 100us, we suggest the Step Adjustment should be utilized instead of Rate Adjustment for more efficient clock tuning.*

## Read PTP Clock Time

To read the local PTP clock, set bit [3:1] = 3'b010, and then issue the Activate bit (bit[ 0]) in PTP\_CLK\_CFG register. After these settings, the PTP Clock is shown in PTP Time Config registers (section 8.3.5 to 8.3.9 , page 68~68).

### **7.6.4.3 PTP TAI configuration**

RTL9000AA-VC/RTL9000AN-VC series support four PTP GPIO pins as the Time Application Interface (TAI), and four modes for PTP TAI configuration.

The PTP TAI configuration modes are shown as bellows:

- (1) Disable function
- (2) Trigger Generate
- (3) Event Capture
- (4) Trigger start time / Event timestamp read (according to current PTP\_GPIO settings)

The configuration can be set by bit [2:1] of PTP\_TAI\_CFG (PTP Application I/F Config Register, Address 0xe420), page 69.

## Read PTP TAI Timestamp

The PTP TAI Time stamp registers are defined in section 8.3.13 to 8.3.16, page 70~71. The value can be read or write, depending on the PTP TAI interface configuration.

## Set PTP TAI Interface

### **● If the PTP TAI interface configuration mode is Trigger Generate :**

The Trigger start at time is specified in PTP TAI Timestamp registers (section 8.3.13 to 8.3.16, page 70~71).

The Trigger Generate mode can be by Address 0xE420, [9:8] (PTP\_TAI\_CFG register, Table 64, page 69) for edge, pulse or periodic type selection.

The duty cycle, unit and period of a trigger pulse also can be specified in the register PTP\_TRIG\_CFG (Table 65, page 70). When ‘pulse\_amt’ is set < 8, the RTL9000AA-VC/RTL9000AN-VC only support ‘50%’ duty cycle configuration for periodic trigger function due to the limitation of clock frequency.

After the PTP TAI Activate bit is set (Address 0xE420, bit [0] = 1), the GPIO trigger function will start working.

Note that due to time needed for hardware to process the trigger setting, some fixed latency would be induced from specified ‘trigger start time’ to the trigger actually start. The value is 6 \* PTP\_CLK period, that is, 90 ns. It is suggested that user takes this offset into account when setting the ‘trigger start time’.

### **● If the PTP TAI interface configuration mode is Event Capture :**

We can set the Event Generate mode at Address 0xE420, bit [6] for edge type selection.

After the PTP TAI Activate bit is set (Address 0xE420, bit [0] = 1), the Event Capture function will start working.

*\*Note 1: Users should always disable the current function of the PTP\_GPIO pin before setting a new TAI function.*

*\*Note 2: If a PHY reset is asserted during the PTP\_GPIO armed (e.g. periodic pulses are toggling), after the reset, PTP TAI Activate bit (Address 0xE420, bit [0]) should be set again in order to restart the same PTP\_GPIO configuration.*

### **7.6.4.4 PTP Reference Clock Input**

RTL9000AA-VC/RTL9000AN-VC provides the option that the local PTP clock can be sourced from an external reference clock, e.g. a GPS-based clock, with frequencies of 10M, 25M, and 125MHz supported.

To enable the reference clock input mode, please follow the steps below:

- (1) Disable the TAI function armed at PTP\_GPIO of the RTL9000AA-VC/RTL9000AN-VC.
- (2) Connect the external reference clock to the PTP\_GPIO pin.

(3) Select the frequency of the input reference clock by bit[6:5] of PTP\_CLK\_CFG register (see Table 58, page 67), and enable the clock input function by asserting bit[4]=1.

(4) After that, issue a PHY reset (Page 0, Reg 0, bit [15]=1) to let the setting take effect.

*Note: The maximum jitter of the external clock should be within 400 ps.*

### 7.6.5. Flow of PTP Sample

The following figures show the PTP handshaking protocol - 802.1AS and PTPv2 One-step protocol.

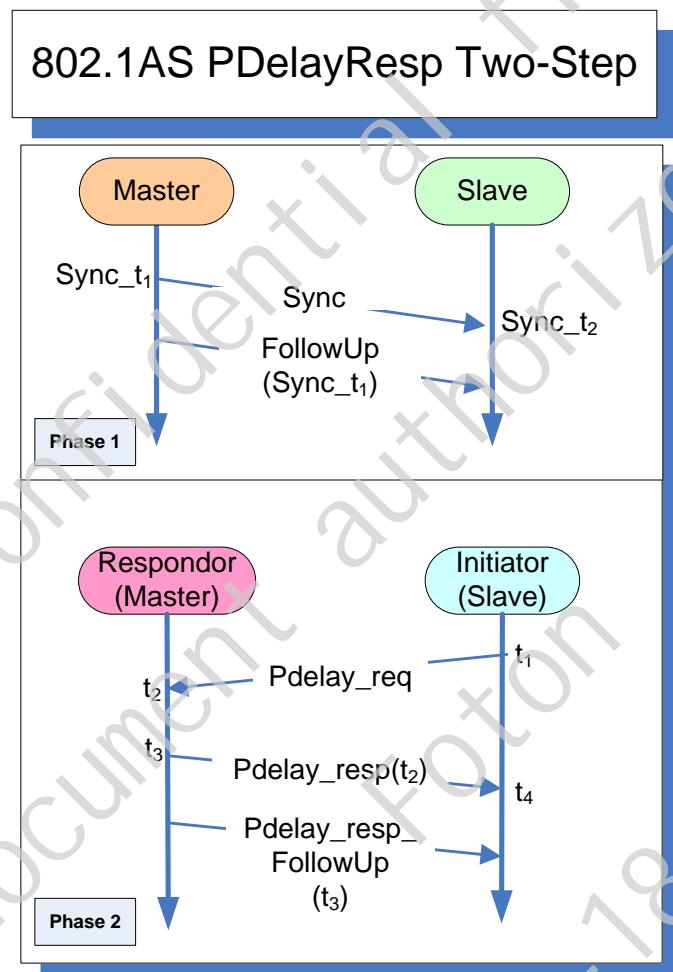


Figure 21. 802.1AS Two-Step Protocol

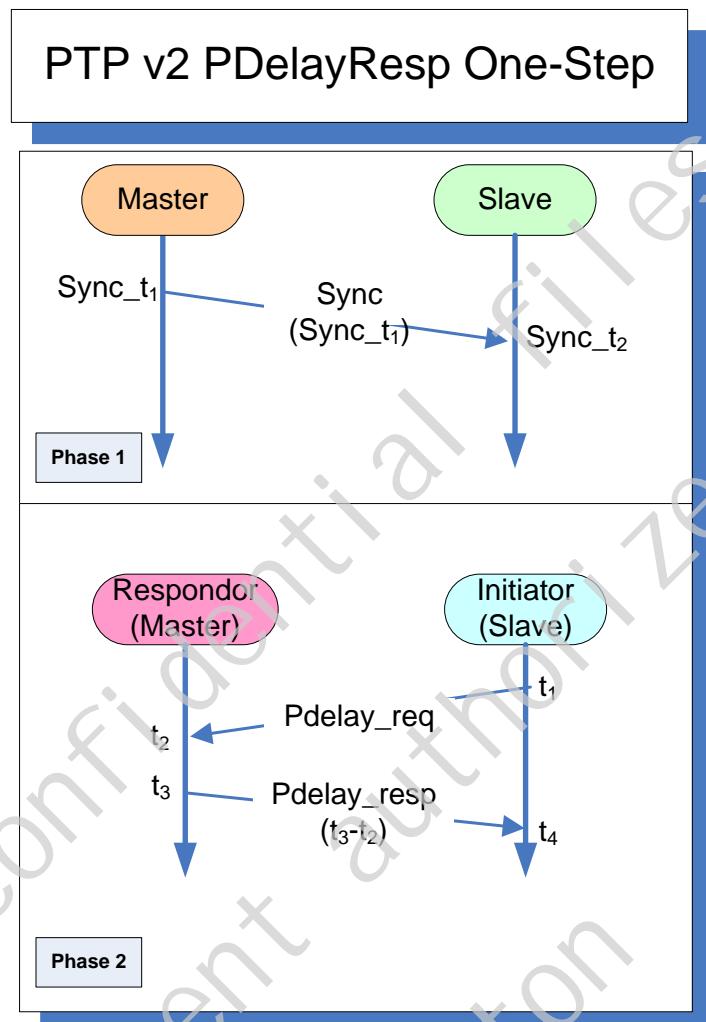
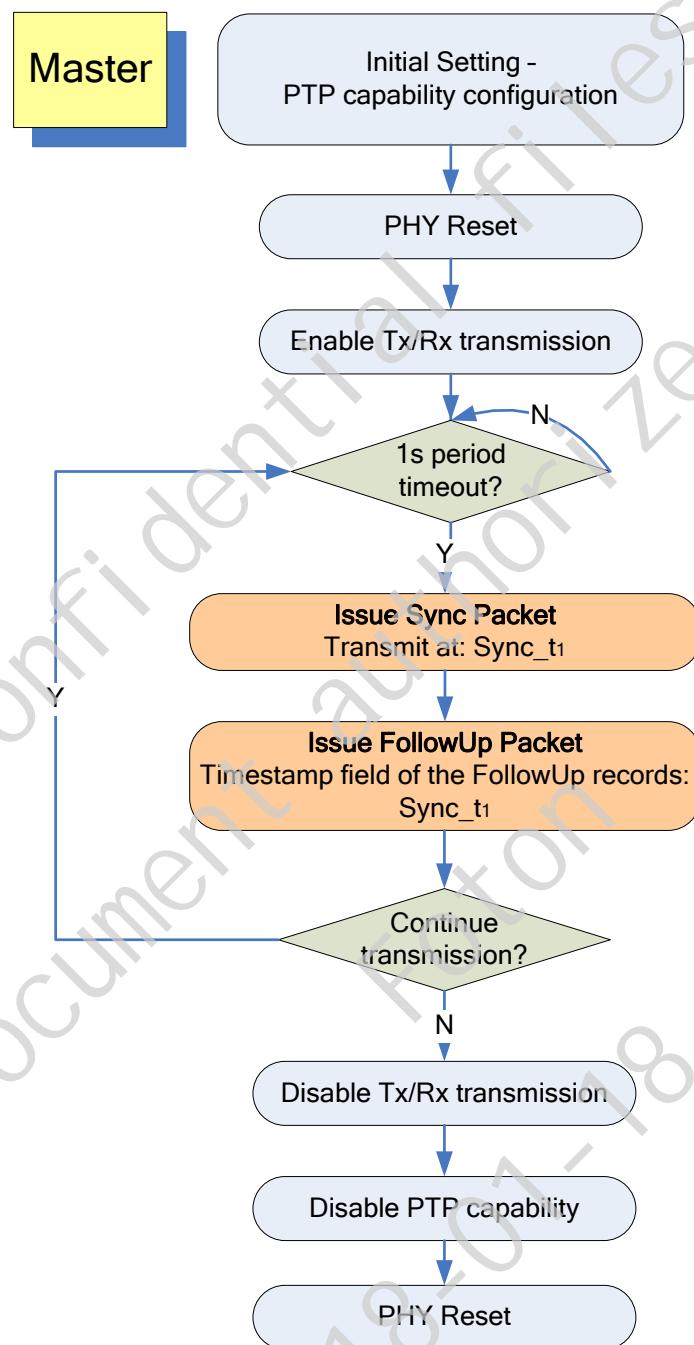


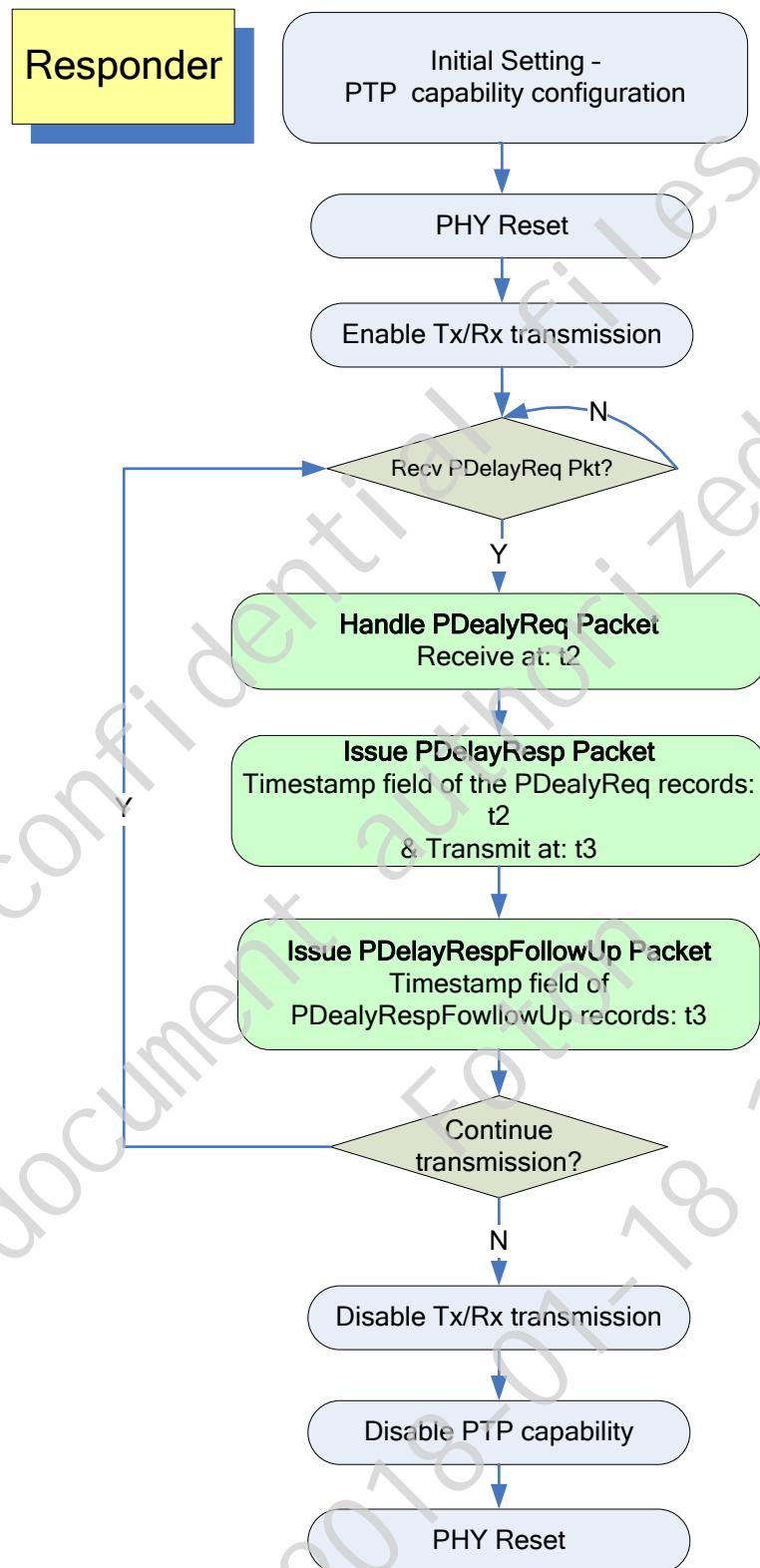
Figure 22. PTPv2 One-Step Protocol

### 7.6.5.1 802.1AS Two-Step Sample Flow Chart

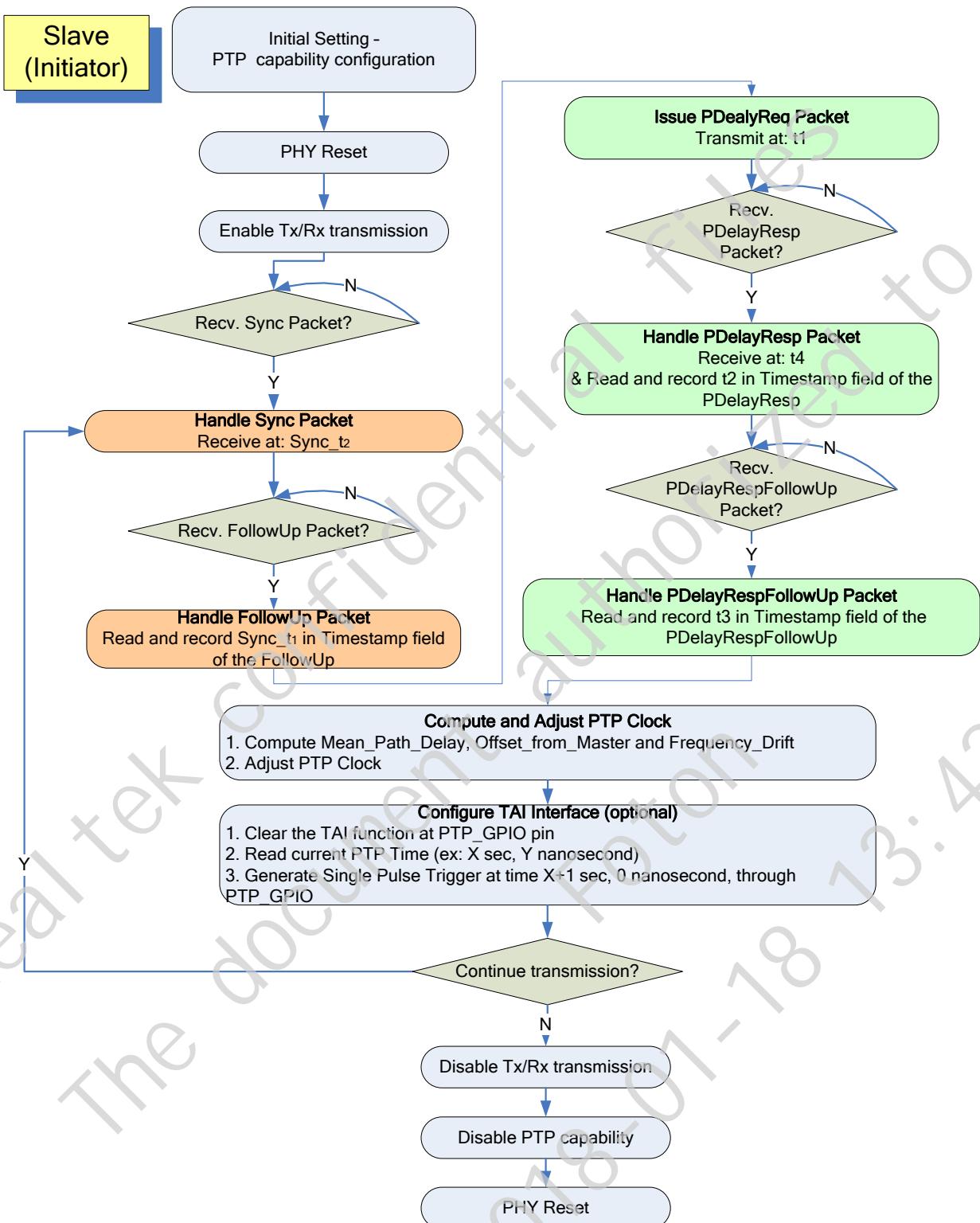
The following PTP sample is based on Two-step 802.1AS protocol, the Master transmits PTP message per second, that is, Sync interval = 1 second.



**Figure 23. Master Flow Chart of 802.1AS Two-Step Sample**



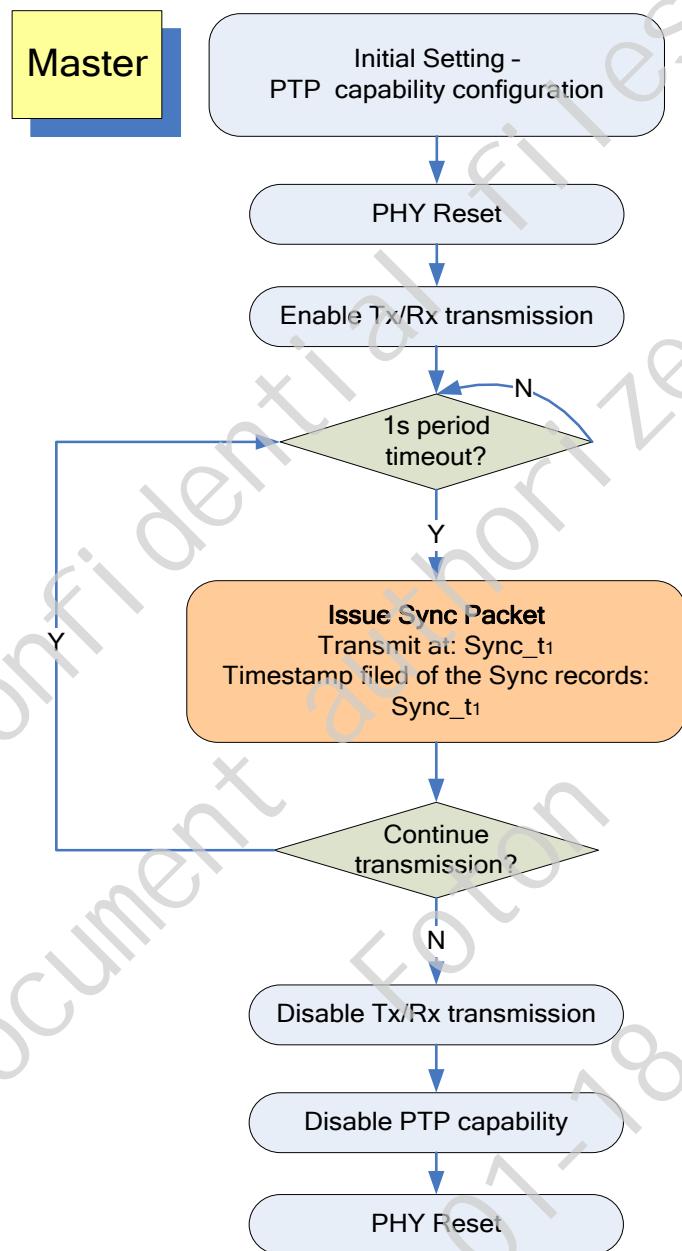
**Figure 24. Responder Flow Chart of 802.1AS Two-Step Sample**



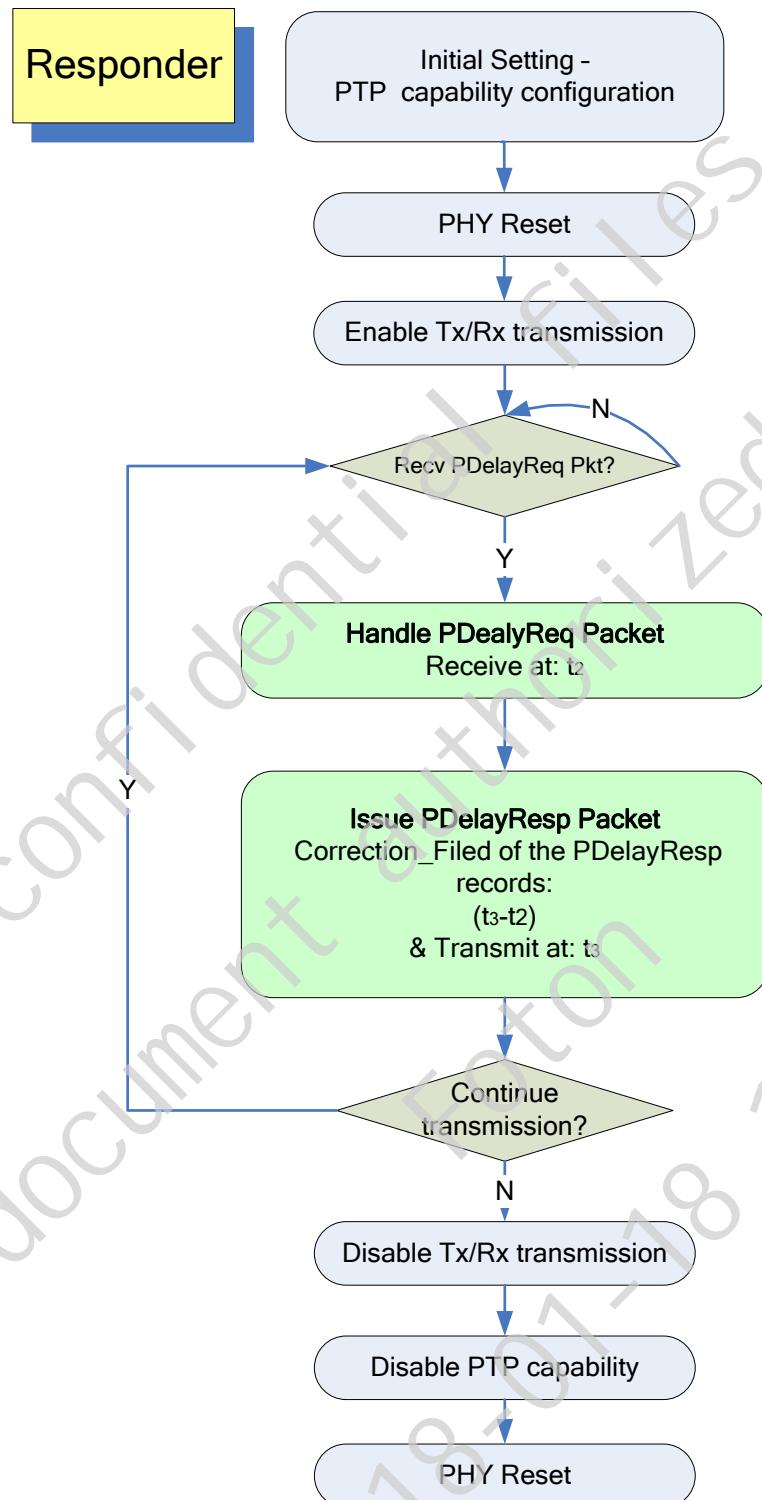
**Figure 25. Slave Flow Chart of 802.1AS Two-Step Sample**

### 7.6.5.2 PTPv2 One-Step Sample Flow Chart

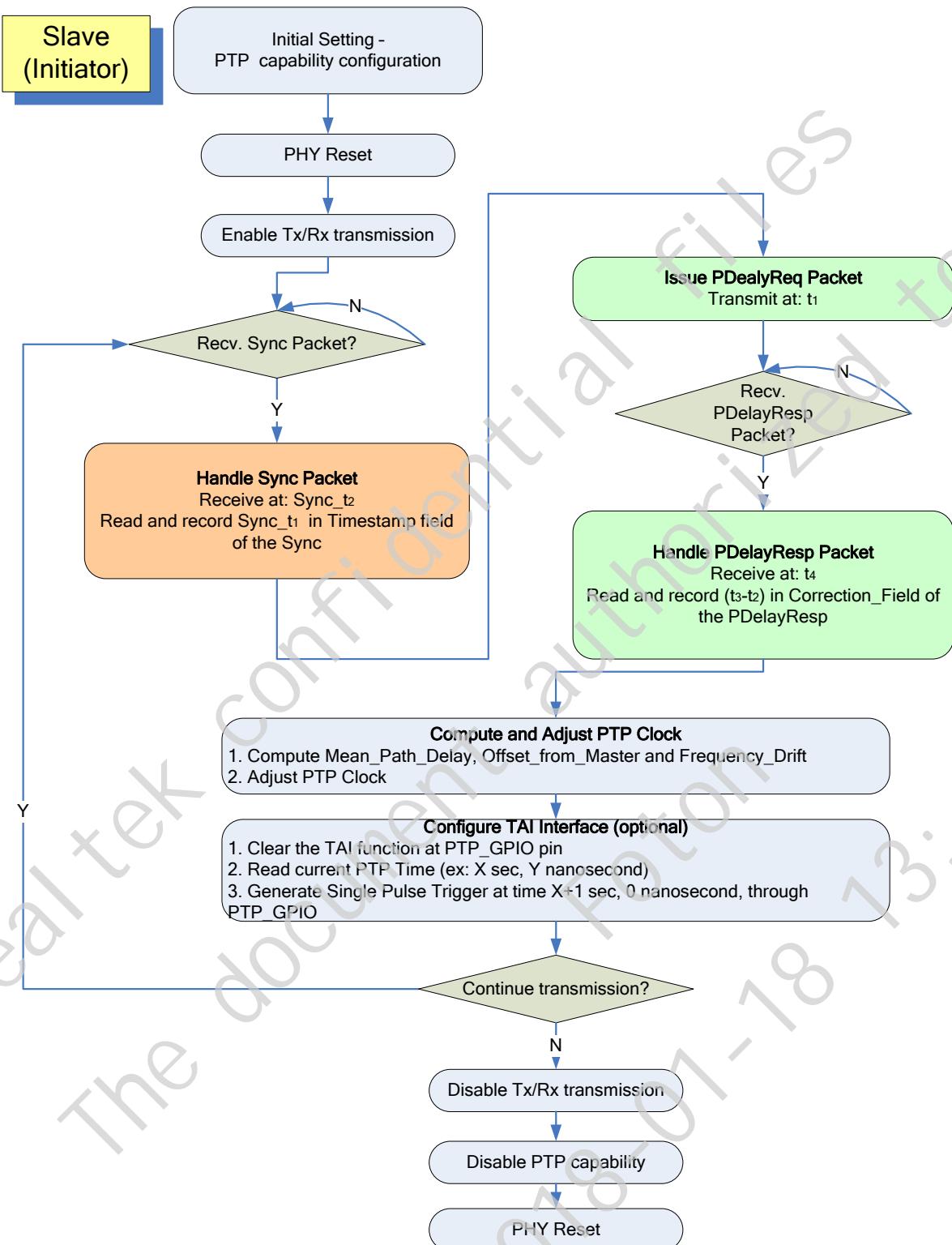
The following PTP sample is based on One – Step PTPv2 protocol, the Master transmits PTP message per second, that is, Sync interval = 1 second.



**Figure 26. Master Flow Chart of PTPv2 One-Step Sample**



**Figure 27. Responder Flow Chart of PTPv2 One-Step Sample**



**Figure 28. Slave Flow Chart of PTPv2 One-Step Sample**

## 7.7. Interrupt

The RTL9000AA-VC/RTL9000AN-VC provides the interrupt function with an active low interrupt output pin (INTB) to inform the MAC about some changes of the PHY status. It is noted that the interrupt function of the RTL9000AA-VC/RTL9000AN-VC uses a level-triggered mechanism. To use the interrupt function of the RTL9000AA-VC/RTL9000AN-VC properly, three types of interrupt control should be taken into account:

### 1. Interrupt Enable Register

The interrupts can be individually enabled or disabled by setting or clearing bits in the following interrupt enable registers:

- General Interrupt enable register – GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12), page 59.
- OP Interrupt enable registers – OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C), OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14), and OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C).

With a dedicated interrupt enabled, the corresponding interrupt status register bit will be recorded ‘1’ if the event happens.

### 2. Interrupt Mask

The interrupt mask function provides more flexible usages. With the ‘mask’ of the specified interrupt enabled while the corresponding event happens, it will be recorded in the interrupt status register of the RTL9000AA-VC/RTL9000AN-VC, but the MAC will not be informed through the INTB pin until the mask is disabled.

Default settings of all interrupt masks are enabled. They can be changed through the following interrupt mask registers:

- General Interrupt mask register – GINMR (General Interrupt Mask Register, Page 0xa42, Reg 0x14), page 60.
- OP Interrupt mask registers – OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E), OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16), and OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E).

### 3. Interrupt Status Register

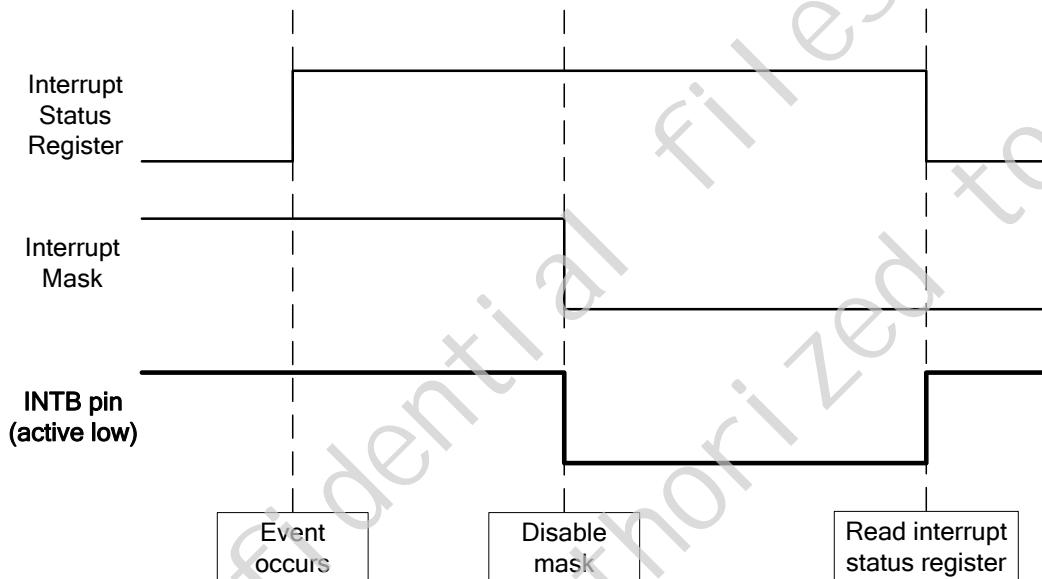
Every General Interrupt condition is represented by the general interrupt status register; while the Operating Mode related statuses are represented by the OP interrupt status register. The interrupt status registers are ‘read-only’ and ‘read-cleared’ type:

- General Interrupt status register – GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12), page 59).
- OP Interrupt status registers – OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08), OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10), and OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18).

The index of the particular interrupt is the same among interrupt enable, mask, and status registers. If an enabled interrupt event occurs, the INTB pin will be driven low accordingly (with mask disabled). This

interrupt will be self-cleared (INTB pin de-asserted) by reading the corresponding interrupt status registers through MDC/Mdio interface. Figure 29 summarizes the behavior stated above.

If more than one interrupt occurs simultaneously, the INTB pin will keep low until all of the interrupt status registers are read by the upper layer.



**Figure 29. Interrupt and Mask Behavior**

Furthermore, some sub-flags of General Interrupt are presented in order to provide detailed event information: such as the PHY fatal errors, PTP events, and general purpose events are summarized by one of the General Interrupts. When the upper layer is informed by the INTB pin and come to access the General Interrupt status register for these types of events, then it is required to check the related sub-flag registers accordingly. The relation of the General Interrupts and its sub-flags are listed in Table 12.

**Table 12. General Interrupts and Sub-flags**

Index	General Interrupts	Sub-flags of General Interrupts
	<b>Enable Register:</b> GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12), page 59 <b>Status Register:</b> GINSR (General Interrupt Status Register, Page 0xa43, Reg 0x1D), page 61 <b>Mask Register:</b> GINMR (General Interrupt Mask Register, Page 0xa42, Reg 0x14), page 60	
<b>15:12</b>	Reserved	
<b>11</b>	PHY fatal errors occur: Which means PHY internal SRAM or clock fail.	
<b>10</b>	Jabber detected	
<b>9</b>	Reserved	
<b>8</b>	PTP events occur	<b>Sub-flags Enable Register:</b> PTP_INER (PTP Interrupt Enable Register, Address 0xe402), page 66 <b>Sub-flags Register:</b> PTP_INSR (PTP Interrupt Status Register, Address 0xe404)

<b>7:5</b>	Reserved	
<b>4</b>	Link status change	
<b>3</b>	Reserved	
<b>2</b>	General purpose events occur	<b>Sub-flags Register:</b> GPSFR (General Purpose Sub-flag Register, Page 0xa47, Reg 0x15), page 62
<b>1</b>	Reserved	
<b>0</b>	PHY status change	<b>Sub-flags Register:</b>

## 7.8. Hardware Configuration

The PHY address, Master/Slave setting, MII interface and state change setting can be set by the CONFIG pins, the corresponding configuration will be strapped and set as the default value whenever the following three events happen: power on, wake up and assert the PHYRSTB pin to low. The respective value mapping of CONFIG with the configurable vector is listed in Table 13. To set the CONFIG pins, an external pull-high or pull-low via resistor is required.

**Table 13. CONFIG Pins vs. Configuration Register**

CONFIG Pin	Configuration
RXD0	PHYAD[0]
RXD1	PHYAD[1]
RXER	MS_SEL
RXD2	MII_SEL[1]
RXD3	MII_SEL[0]
RXDV	ST_CHG

**Table 14. Configuration Register Definitions**

Configuration	Description
PHYAD[1:0]	<p>PHY Address. PHYAD sets the PHY address for the device. The RTL9000AA-VC/RTL9000AN-VC supports PHY addresses from 01 to 11.</p> <p><i>Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xA43, Reg 0x18, bit[13]=0 (See section 8.2.15, page 60).</i></p> <p><i>Note 2: The RTL9000AA-VC/RTL9000AN-VC with PHYAD[1:0]=00 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xA43, Reg 0x18, bit[6]=1 (See section 8.2.15, page 60).</i></p>
MS_SEL	<p>PHY Master / Slave Mode Configuration.</p> <p>1: Master (via 4.7k-ohm to GND)</p> <p>0: Slave (via 4.7k-ohm to DVDD_MII power)</p>
MII_SEL[1:0]	<p>MII/RMII/RGMII Mode Configuration.</p> <p>2'b00: MII mode</p> <p>2'b01: RMII mode (OUT)</p> <p>2'b10: RGMII mode</p> <p>2'b11: RMII mode (IN)</p>
ST_CHG	<p>Operating Modes (OP) State Change Condition Configuration</p> <p>The application for the ST_CHG can refer to section 7.3, Standby mode.</p> <p>1: Auto mode, the PHY goes to Normal Mode automatically, when it power on/wake up/assert PHYRSTB to low. (via 4.7k-ohm to DVDD_MII power)</p> <p>0: Manual mode, the PHY goes to Normal Mode manually, when it power on/wake up/assert PHYRSTB to low. (Wait for OP go to sleep/normal command, refer to section 7.3.2.) (via 4.7k-ohm to GND)</p>

## 7.9. MAC/PHY Interface

The RTL9000AA-VC/RTL9000AN-VC supports automotive standards and is suitable for most off-the-shelf MACs with an MII/RMII/RGMII interface.

### 7.9.1. MII

If MII (Media Independent Interface) mode is selected, TXC and RXC sources are 25MHz. TXC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions.

### 7.9.2. RMII

The purpose of the RMII (Reduced Media Independent Interface) interface is to provide a low cost alternative to the MII. Architecturally, the RMII provides for an additional reconciliation layer on either side of the MII but can be implemented in the absence of an MII. The RMII sources from the only reference clock REF\_CLK, which can be provided either by the PHY or the MAC. TXD[1:0] and RXD[1:0] signals are used for data transitions.

### 7.9.3. RGMII

Among the RGMII interface in 100BASE-T1, TXC and RXC sources are 25MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on the rising and falling edge of the clock.

### 7.9.4. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 4.7k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

The RTL9000AA-VC/RTL9000AN-VC can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the management registers, see section8, page 54.

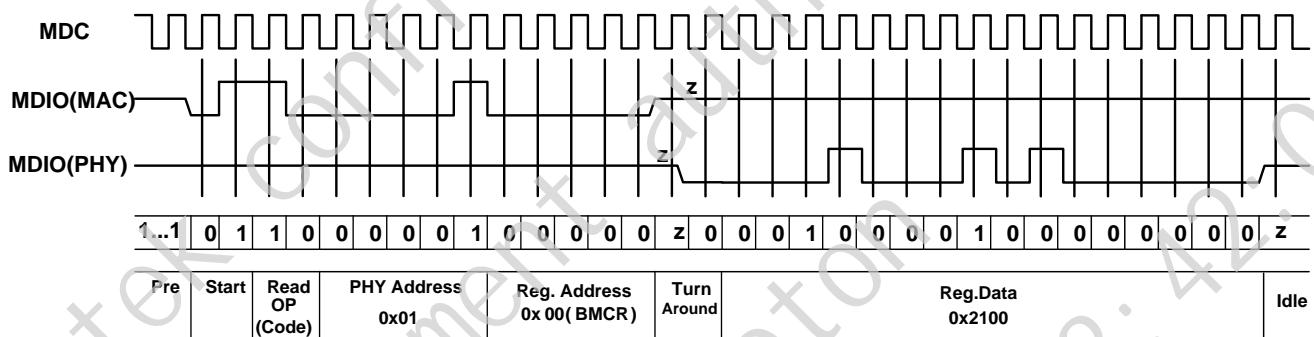
**Table 15. Management Frame Format**

	Management Frame Fields							
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1...1	01	10	AAAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
Write	1...1	01	01	AAAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

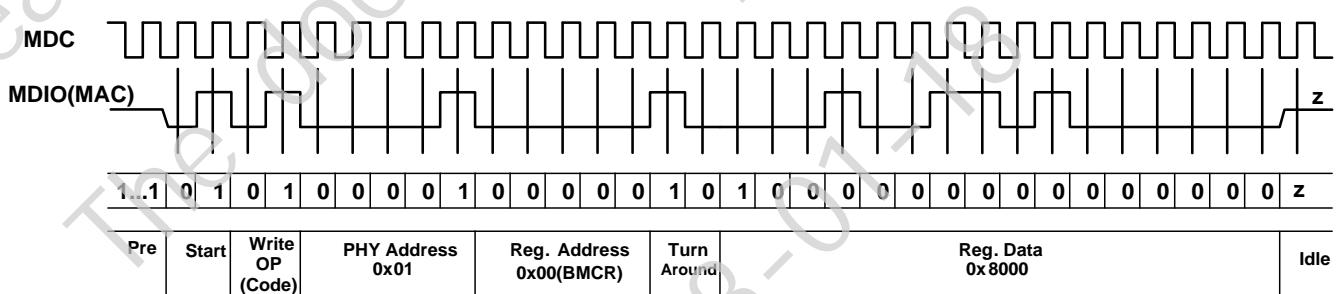
**Table 16. Management Frame Description**

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.

Name	Description
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.



**Figure 30. MDC/MDIO Read Timing**



**Figure 31. MDC/MDIO Write Timing**

### 7.9.5. Register Access

RTL9000AA-VC/RTL9000AN-VC have the two methods for accessing the registers. The one is called Normal Register Access which is for the most of IEEE standard registers; the other is Special Register

Access which is especially for the OP register and others. The table should be followed while accessing the registers by the corresponding accessing way.

**Table 17. Method of Accessing registers**

Register Table	Method of accessing registers
General Register Table Section 8.2.1- Section 8.2.25.	7.9.5.1 Normal Register Access
General Register Table Section 8.2.26 - 8.2.32.	7.9.5.2 Special Register Access
8.3 PTP Register Tables	
8.4 OP Register Tables	

### **7.9.5.1 Normal Register Access**

In Normal Register Access, the Page should be set to the target register's page first then read/ write the target register with its register address (Reg 0xAB). The MDIO commands and the example are shown below.

Take the register at Page 0WXYZ (in Hex), Reg 0xAB as an example.

1. Write Register 31 Data = 0WXYZ (switch to Page 0WXYZ)
2. Read/Write Register 0xAB (target register's Reg 0xAB) Data directly.
3. Write Register 31 Data = 0xA42 (switch back to IEEE Standard Registers)

### **7.9.5.2 Special Register Access**

In Special Register Access, by reading/writing the register 27 and register 28 to read/write the target register with its address (Address 0WXYZ). The Page switching is no need. The MDIO commands and the example are shown below.

Take the register with Address 0WXYZ as an example.

1. Write Register 27 Data = 0WXYZ (Register with Address 0WXYZ)
2. Read/Write the target Register Data through Register 28

*\*Note: Writing the 'register address' should always be done (Step 1) each time when accessing registers, even for access to the same register.*

## 7.10. Polarity Correction

The RTL9000AA-VC/RTL9000AN-VC automatically corrects polarity errors on the receive pairs. Received polarity errors are automatically corrected based on the sequence of idle symbols. Read the register at section 0 to know if the polarity is swapped or not. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

## 7.11. Spread Spectrum Clock (SSC)

The clock could be a very likely source of EMI noise. Spread Spectrum Clock (SSC) spreads the signal across a wider bandwidth, reducing the peak radiated energy at any one frequency, and lowering unwanted EMI noise. For the RTL9000AA-VC/RTL9000AN-VC, Spread Spectrum Clock (SSC) is supported in three clock domains: system clock, RXC of MII, and REF\_CLK (output mode) of RMII. Note that the SSC function is open in RTL9000AA-VC/RTL9000AN-VC default.

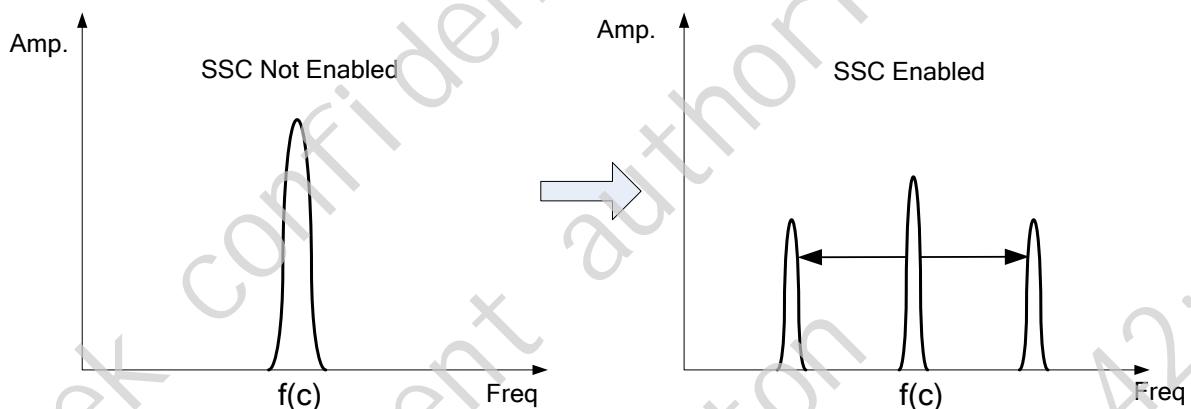


Figure 32. Spread Spectrum Clock

## 7.12. Realtek Cable Test Diagnostics (RTCT)

The RTL9000AA-VC/RTL9000AN-VC has integrated a DSP engine to detect the cable status, which is described as “Realtek Cable Test Diagnostics (RTCT)”. As a result, RTL9000AA-VC/RTL9000AN-VC has internal registers to indicate abnormal linking cable status and linking cable length in normal operation mode. By accessing the register to read the cable status, two different abnormal phenomena can be detected - cable open and cable short. Moreover, not only linking cable status can be detected by RTCT, but also the location of abnormal point can be indicated. For instance, the linking cable is open and the point where the cable is open can be detected by accessing RTL9000AA-VC/RTL9000AN-VC’s internal register. On the other hand, the cable length can also be retrieved by the registers in normal operation scenario.

### 7.12.1. RTCT Method

Follow the steps below to utilize RTCT to do some cable diagnostics for RTL9000AA-VC/RTL9000AN-VC. For the detailed register description, see Table 32.

#### Step 1: Enable RTCT

Set Reg 17, bit[0] = 1(rtct\_en, enable RTCT and start to test)

### Step 2: Waiting for finishing of RTCT

Read Reg 17, bit [15] (rtct\_done, cable tester finish indicator), if value ‘1’ is returned, it means the test of RTCT is finished. On the contrary, if value ‘0’ is returned, the test is still under processing.

### Step 3: Read channel status and cable length

- I. Write Reg 31 Data = 0xA43 (Swap to page 0xA43)
- II. Write Reg 27 Data = 0x8022
- III. Read Reg 28, this value means cable status. The status can be translated by using table below to indicate cable status to be cable in normal operation, cable open, or cable short:

**Table 18. RTCT Cable Status Indication**

Cable Status	Register Value (in Hex)	Description
Normal	0x60XX	Cable is indicated to be normal in the following situation. <ul style="list-style-type: none"> <li>● In the normal operating:</li> </ul> 
Open	0x48XX	Cable is indicated to be open in the following situations. <ul style="list-style-type: none"> <li>● Both of the wires are open:</li> </ul>  <ul style="list-style-type: none"> <li>● One of the wires open:</li> </ul> 
Short	0x50XX	Cable is indicated to be short in the following situations. <ul style="list-style-type: none"> <li>● Wires are short:</li> </ul>  <ul style="list-style-type: none"> <li>● Both of the wires short to GND or Supply:</li> </ul> 

\*Note: These cable statuses can also be indicated by the LED pin, see section 7.14, page 51.

If cable is NOT in ‘normal operating mode’, the defect point can be indicated by following operation:

- i. Write Reg 31 Data = 0xA43 (Swap to page 0xA43)
- ii. Write Reg 27 Data = 0x8023
- iii. Read Reg 28 bit [15:0]. The value can be read by transforming the hexadecimal value into decimal value then divided by 80. The result means the distance from the RTL9000AA-VC/RTL9000AN-VC to the defect point of cable in meter.

### 7.12.2. Cable length Checking Method (in Normal Operating Mode Only)

The cable length checking can be only executed in Normal Operating Mode. The cable length can be read by accessing the following registers.

1. Write Reg 31 Data = 0xA89 (Swap to page 0xA89)
2. Read Reg 16, bit[7:0] and transform it into decimal and the value is linking cable length in meter.

## 7.13. Signal Quality Indexes (SQI)

The RTL9000AA-VC/RTL9000AN-VC provides two signal quality indexes (SQI), which indicate the real-time MDI signal quality information. These indexes are listed as follows:

### 7.13.1. Signal-to-Noise-Ratio (SNR)

This measure compares the level of a desired signal to the level of background noise in an average manner. It is defined as the ratio of mean signal power to the mean noise power, expressed in decibels (dB). The value is higher the better, and can be computed by:

$$\text{SNR} = -10 \log_{10} [\text{SNR\_Reg\_Value} \text{ (in decimal)} / (3 * 2^{17})]$$

The register SNR\_Reg\_Value can refer to Table 48.

The SNR can be implied to the following SQI classification. The higher level of classification means the better SQI.

**Table 19. SQI Classification**

SQI Classification	SNR (dB)	SNR_Reg_Value (in decimal)
0	SNR < 20.1 dB	SNR_Reg_Value > 3840
1	20.1 dB ≤ SNR ≤ 21.07 dB	3840 ≥ SNR_Reg_Value ≥ 3072
2	21.07 dB ≤ SNR ≤ 22.0 dB	3072 ≥ SNR_Reg_Value ≥ 2480
3	22.0 dB ≤ SNR ≤ 23.0 dB	2480 ≥ SNR_Reg_Value ≥ 1968
4	23.0 dB ≤ SNR ≤ 24.03 dB	1968 ≥ SNR_Reg_Value ≥ 1552
5	24.03 dB ≤ SNR ≤ 25.04 dB	1552 ≥ SNR_Reg_Value ≥ 1232
6	25.04 dB ≤ SNR ≤ 26.5 dB	1232 ≥ SNR_Reg_Value ≥ 976
7	26.0 dB ≤ SNR	976 ≥ SNR_Reg_Value

### 7.13.2. Maximum Error

In contrast to the SNR which evaluates signal quality averagely, the Maximum Error represents the instant maximum difference between the expecting level of signal and the decoded result by the PHY. This is to say, this value record the Maximum Error during a time interval and it will be refreshed periodically. The value is lower the better, and can be computed by:

$$\text{Max Error} = \text{MaxErr_Reg_Value} \text{ (in decimal)} / 2^6$$

The register MaxErrReg\_Value can refer to Table 49.

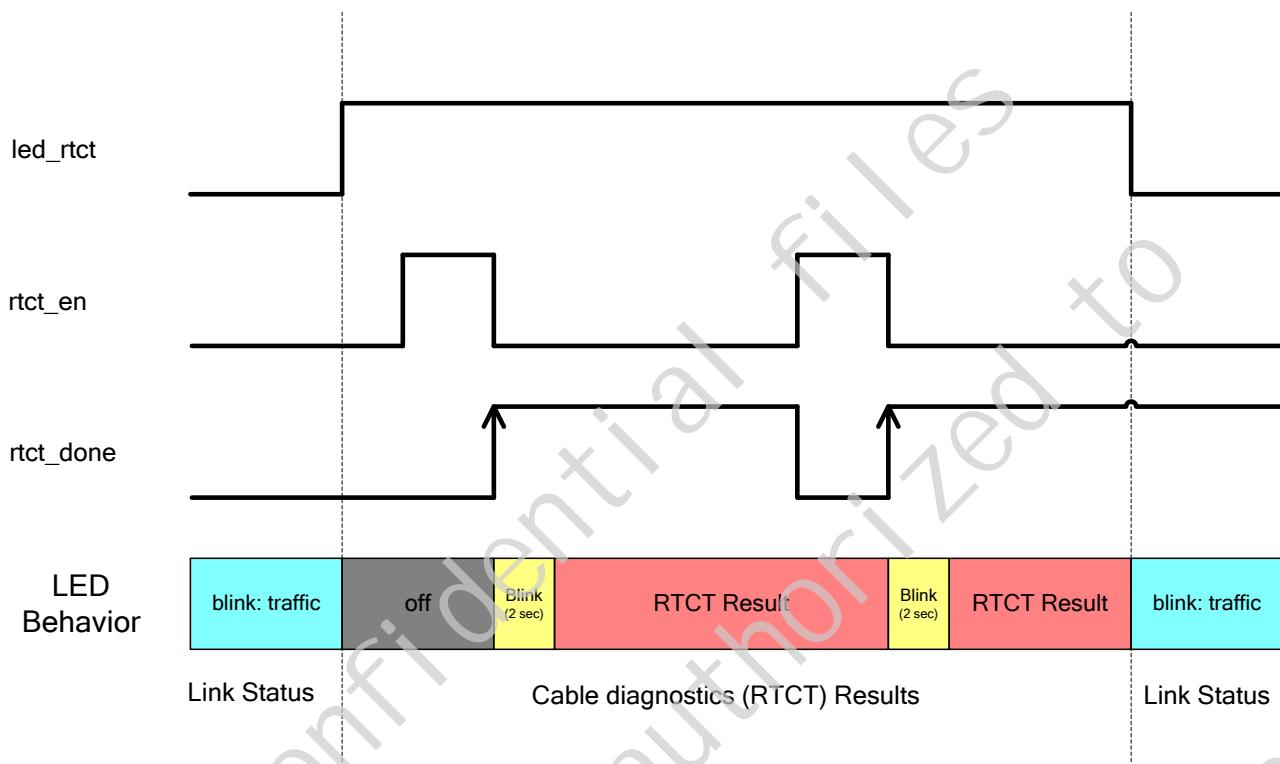
## 7.14. LED

The RTL9000AA-VC/RTL9000AN-VC provides an LED pin as an indication for debugging use, its functions are listed as Table 20 below.

**Table 20. LED**

	Link Status	Cable diagnostics (RTCT) Results
LED Behavior	<ul style="list-style-type: none"> <li>• On: Link up</li> <li>• Off: Link down</li> <li>• Blinking: Traffic transmitting</li> </ul>	<ul style="list-style-type: none"> <li>• On: Cable Open</li> <li>• Off: Cable Normal</li> <li>• Off for 1 sec followed by On for 3s: Cable Short</li> </ul>
Register Settings	Address 0xD040, bit[0] = 1 (led_link) Address 0xD040, bit[1] = 1 (led_act) Address 0xD040, bit[13] = 0 (led_rtct)	Address 0xD040, bit[13] = 1 (led_rtct)
Note		The LED behavior above will be presented in the

'RTCT Result' interval in Figure 33.



**Figure 33. LED Behavior**

Note 1: For the definitions of 'rtct\_en' and 'rtct\_done', please refer to section 7.12 Realtek Cable Test Diagnostics (RTCT), page 49, and section 8.2.10 RTCTCR (RTCT Control Register, Page 0xa42, Reg 0x11), page 59.

Note 2: For detailed LED setting, please refer to section 8.2.31, page 64.

## 7.15. UNH IOL Test

The five test modes of IEEE 802.3bw<sup>[1]</sup> are supported by RTL9000AA-VC/RTL9000AN-VC. The five test mode can be selected independently and the test signal will present at MDI pins (MDIP and MDIN) in the Normal mode while the link is disabled. To enable the UNH IOL Test Modes excepting for Test Mode 3, please set the Page 0, Reg 0, bit [15:13], see Table 27.

The PTP\_GPIO pin can be used as a clock output in test modes that need a reference clock by the following steps.

1. Write Address 0xd41E, bit [15:13]=0
2. Write Address 0xd42A, bit [0]=0
3. Write Address 0xa42C, bit [0]=1 // To output the clock to PTP\_GPIO pin

### 7.15.1. Test mode 1

The test mode 1 is measurement of the Transmit droop. When the test mode 1 is enabled, the PHY shall transmit greater than 500ns “+1” symbols followed by greater than 500 ns “-1” symbols. This sequence is repeated continually.

### 7.15.2. Test mode 2

The test mode 2 is measurement of the Transmit jitter in MASTER mode. When the test mode 2 is enabled, the PHY shall transmit the data symbol sequence  $\{+1, -1\}$  repeatedly. The transmitter shall time the transmitted symbols from a  $66.666 \text{ MHz} \pm 100 \text{ ppm}$  clock in the MASTER timing mode.

### 7.15.3. Test mode 4

The test mode 4 is measurement of Transmit distortion. When the test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the scrambler generator polynomial, bit generation, and level mappings as equation 96-1 in [1]. The transmitter shall time the transmitted symbols from a  $66.666 \text{ MHz} \pm 100 \text{ ppm}$  clock in the MASTER timing mode.

### 7.15.4. Test mode 5

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask. When test mode 5 is enabled, the PHY shall transmit a pseudo-random sequence of PAM3 symbols.

### 7.15.5. SLAVE Jitter

With the steps above to output the reference clock to the PTP\_GPIO pin to measure the transmit jitter in SLAVE mode. However the SSC should be turned off by the additional step 4 while measuring SLAVE Jitter.

4. Write Address 0xd012, bit [2:0] =0 // Turn off SSC (Refer to section 8.2.29.)

After finishing the test, RTL9000AA-VC/RTL9000AN-VC should be reset by the PHYRSTB.

[1] IEEE Standard for Ethernet Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1), 26 October, 2015.

## 8. Register Descriptions

The registers of the RTL9000AA-VC/RTL9000AN-VC are classified into three categories:

- General registers – Section 8.2
- PTP registers – Section 8.3
- OP registers – Section 8.4

*Note: For each register, it has its own corresponding method should be used to access them. Please refer to Table 17. Method of Accessing registers.*

The register access types are listed in Table 21:

**Table 21. Register Access Types**

Type	Description
LH	Latch high. If the status is high, this field is set to '1' and remains set.
RC	Read-cleared. The register field is cleared after read.
RO	Read only.
RW	Read and Write
SC	Self-cleared. Writing a '1' to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0'.

### 8.1. IEEE Standard Register Mapping and Definitions

**Table 22. IEEE Standard Register Mapping and Definitions**

Offset	Access	Name	Description
0	RW	BMCR	Basic Mode Control Register.
1	RO	BMSR	Basic Mode Status Register.
2	RO	PHYID1	PHY Identifier Register 1.
3	RO	PHYID2	PHY Identifier Register 2.
4~8	RO	RSVD	Reserved.
9	RW	PHYCR	PHY Control Register.
10	RO	PHYSR	PHY Status Register.
13	WO	MACR	MMD Access Control Register
14	RW	MAADR	MMD Access Address Data Register
11,12,15	RO	RSVD	Reserved.

## 8.2. General Register Tables

### 8.2.1. BMCR (Basic Mode Control Register, Page 0x0, Reg 0x00)

**Table 23. BMCR (Basic Mode Control Register, Page 0x0, Reg 0x00)**

Bit	Name	Type	Default	Description															
0.15	Reset	RW, SC	0	<p>Reset. 1: PHY reset 0: Normal operation</p> <p>Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit15 to 1). This action may change the internal the PHY state and the state of the physical link associated with the PHY. When a software Reset is done by setting Reset (0.15) to 1, polling until Reset (0.15) to 0 to make sure the reset procedure is finished. Then the other PHY registers are accessible after the reset procedure.</p>															
0.14	Loopback	RW	0	<p>Loopback Mode. 1: Enable PCS loopback mode 0: Disable PCS loopback mode</p> <p>The loopback function enables MII/RMII/RGMII transmit data to be routed to the MII/RMII/RGMII receive data path.</p>															
0.13	Speed[0]	RO	1	<p>Speed Select Bit 0. In forced mode, bits 6 and 13 determine device speed selection.</p> <table border="1"> <thead> <tr> <th>Speed[1]</th> <th>Speed[0]</th> <th>Speed Enabled</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>100Mbps</td> </tr> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table>	Speed[1]	Speed[0]	Speed Enabled	1	1	Reserved	1	0	Reserved	0	1	100Mbps	0	0	Reserved
Speed[1]	Speed[0]	Speed Enabled																	
1	1	Reserved																	
1	0	Reserved																	
0	1	100Mbps																	
0	0	Reserved																	
0.12	RSVD	RO	0	Reserved.															
0.11	PWD	RW	0	<p>Power Down. 1: Power down (only Management Interface and logic are active; link is down) 0: Normal operation</p>															
0.10	Isolate	RW	0	<p>Isolate. 1: MII/RMII/RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL9000AA-VC/RTL9000AN-VC ignores TXD[3:0], and TXEN inputs, and presents a high impedance on TXC, RXC, RXDV, RXER, RXD[3:0]. 0: Normal operation</p>															
0.9	RSVD	RO	0	Reserved.															
0.8	Duplex	RO	1	Duplex Mode. 1: Full Duplex operation															
0.7	RSVD	RO	0	Reserved.															
0.6	Speed[1]	RW	0	Speed Select Bit 1. Refer to bit 0.13.															
0.5	RSVD	RO	0	Reserved.															

Bit	Name	Type	Default	Description
0:4:0	RSVD	RO	00000	Reserved.

Note 1: When the RTL9000AA-VC/RTL9000AN-VC is switched from power down to normal operation, a software reset is performed, even if bits Reset (Page 0x0 Reg 0 bit[15]=1) is not set by the user.

## 8.2.2. BMSR (Basic Mode Status Register, Page 0x0, Reg 0x01)

Table 24. BMSR (Basic Mode Status Register, Page 0x0, Reg 0x01)

Bit	Name	Type	Default	Description
1.15:7	RSVD	RO	000000000	Reserved.
1.6	Preamble Suppression	RO	0	1: PHY will accept mdc/mdio frames with preamble suppressed. 0: PHY will not accept mdc/mdio frames with preamble suppressed.
1.5:3	RSVD	RO	000	Reserved.
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, read this register twice.
1.1	Jabber Detect	RC, LH	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

## 8.2.3. PHYID1 (PHY Identifier Register 1, Page 0x0, Reg 0x02)

Table 25. PHYID1 (PHY Identifier Register 1, Page 0x0, Reg 0x02)

Bit	Name	Type	Default	Description
2.15:0	OUI_MSB	RO	00000000000011100	Organizationally Unique Identifier Bit 3:18. Always 00000000000011100.

Note: Realtek OUI is 0x000732.

## 8.2.4. PHYID2 (PHY Identifier Register 2, Page 0x0, Reg 0x03)

Table 26. PHYID2 (PHY Identifier Register 2, Page 0x0, Reg 0x03)

Bit	Name	Type	Default	Description
3.15:10	OUI_LSB	RO	110010	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	TBD	Manufacture's Model Number
3.3:0	Revision Number	RO	0000	Revision Number

### 8.2.5. PHYCR (PHY Control Register, Page 0x0, Reg 0x09)

**Table 27. PHYCR (PHY Control Register, Page 0x0, Reg 0x09)**

Bit	Name	Type	Default	Description
9.15:13	Test Mode	RW	000	Test Mode Select. 000: Normal mode 001: Test Mode 1 – Transmit droop Test 010: Test Mode 2 – Transmit Jitter Test (MASTER mode) 100: Test Mode 4 – Transmit Distortion Test 101: Test Mode 5 – Normal operation at full power. (for PSD mask) 011, 110, 111: Reserved The test signal presents at MDI pins. (MDIP and MDIN)
9.12	RSVD	RO	0	Reserved.
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
9.10:0	RSVD	RO	11'b0	Reserved.

*Note: A Software Reset (Page 0x0 Reg 0 bit[15]=1) should be asserted in order to let the change of bit 9.11 take effect.*

### 8.2.6. PHYSR1 (PHY Status Register 1, Page 0x0, Reg 0x0A)

**Table 28. PHYSR1 (PHY Status Register 1, Page 0x0, Reg 0x0A)**

Bit	Name	Type	Default	Description
10.15	RSVD	RO	0	Reserved.
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK
10.11:8	RSVD	RO	0000	Reserved.
10.7:0	Idle Error Count	RO, RC	0x00	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xff.

### 8.2.7. MACR (MMD Access Control Register, Page 0x0, Reg 0x0D)

**Table 29. MACR (MMD Access Control Register, Page 0x0, Reg 0x0D)**

Bit	Name	Type	Default	Description
13.15:14	Function	WO	0	00: Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	000000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

*Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.*

*Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.*

*Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.*

### 8.2.8. MAADR (MMD Access Address Data Register, Page 0x0, Reg 0x0E)

**Table 30. MAADR (MMD Access Address Data Register, Page 0x0, Reg 0x0E)**

Bit	Name	Type	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14 = 00 → MMD DEVAD's address register 13.15:14 = 01, 10, or 11 → MMD DEVAD's data register as indicated by the contents of its address register

*Note: This register is used in conjunction with the MACR (Register 13; Table 29) to provide access to the MMD address space.*

### 8.2.9. PHYSFR (PHY Status Sub-flag Register, Page 0xa42, Reg 0x10)

**Table 31. PHYSFR (PHY Status Sub-flag Register, Page 0xa42, Reg 0x10)**

Bit	Name	Type	Default	Description
16.15:3	RSVD	RO	0xc	Reserved.
16.2:0	PHY Status sub-flag	RO	0	PHY status indicator: 3'b000: Reserved 3'b001: PHY Initialization 3'b010: Reserved 3'b011: PHY Ready 3'b100: IEEE Std. Reset (Page 0x0 Reg 0 bit[15]) 3'b101: PHY Power Down (Page 0x0 Reg 0 bit[1])

## 8.2.10. RTCTCR (RTCT Control Register, Page 0xa42, Reg 0x11)

Table 32. RTCTCR (RTCT Control Register, Page 0xa42, Reg 0x11)

Bit	Name	Type	Default	Description
17.15	RTCT Done	RW	0	1: Indicate RTCT finished
17.14:1	RSVD	RO	0	Reserved.
17.0	RTCT Enable	RW	0	RTCT enable

## 8.2.11. GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12)

Table 33. GINER (General Interrupt Enable Register, Page 0xa42, Reg 0x12)

Bit	Name	Type	Default	Description
18.15:12	RSVD	RO	1111	Reserved.
18.11	PHY Fatal Error Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event. Page 0xA43, Reg29 Bit[11] always reflects the jabber interrupt behavior.
18.10	Jabber Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event. Page 0xA43, Reg29 Bit[10] always reflects the jabber interrupt behavior.
18.9	RSVD	RO	1	Reserved.
18.8	PTP Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PTP interrupt event. Page 0xA43, Reg29 Bit[8] always reflects the PTP interrupt behavior.
18.7:5	RSVD	RO	111	Reserved.
18.4	Link Status Change Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the link status change interrupt event. Page 0xA43, Reg29 Bit[4] always reflects the link change interrupt behavior.
18.3	RSVD	RO	1	Reserved.
18.2	General Purpose Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the general purpose interrupt event. Page 0xA43, Reg29 Bit[2] always reflects the general purpose interrupt behavior.
18.1	RSVD	RO	1	Reserved.
18.0	PHY Status Change Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PHY status change interrupt event. Page 0xa43, Reg29 Bit[0] always reflects the PHY status change interrupt behavior.

## 8.2.12. GINMR (General Interrupt Mask Register, Page 0xa42, Reg 0x14)

**Table 34. GINMR (General Interrupt Mask Register, Page 0xa42, Reg 0x14)**

Bit	Name	Type	Default	Description
20.15:12	RSVD	RO	1111	Reserved.
20.11	MASK: PHY Fatal Error Interrupt	RW	1	1: Mask Enable 0: Mask Disable
20.10	MASK: Jabber Interrupt	RW	1	1: Mask Enable 0: Mask Disable
20.9	RSVD	RO	1	Reserved.
20.8	MASK: PTP Interrupt	RW	1	1: Mask Enable 0: Mask Disable
20.7:5	RSVD	RO	111	Reserved.
20.4	MASK: Link Status Change Interrupt	RW	1	1: Mask Enable 0: Mask Disable
20.3	RSVD	RO	1	Reserved.
20.2	MASK: General Purpose Interrupt	RW	1	1: Mask Enable 0: Mask Disable
20.1	RSVD	RO	1	Reserved.
20.0	MASK: PHY Status Change Interrupt	RW	1	1: Mask Enable 0: Mask Disable

## 8.2.13. SLPCR (Sleep Control Register, Page 0xa42, Reg 0x15)

**Table 35. SLPCR (Sleep Control Register, Page 0xa42, Reg 0x15)**

Bit	Name	Type	Default	Description
21.15:11	RSVD	RO	00000	Reserved.
21.10	Stop_sleep	RW	0	1: Reject sleep flow
21.9	Sleep_Request	RW	0	1: Send Sleep Request to PHY and start sleep flow
21.8:0	RSVD	RO	0x36	Reserved.

## 8.2.14. LKTCR (Link Timer Control Register, Page 0xa42, Reg 0x16)

**Table 36. LKTCR (Link Timer Control Register, Page 0xa42, Reg 0x16)**

Bit	Name	Type	Default	Description
22.15:3	RSVD	RO	0x0000	Reserved.
22.2	Link_timer_stop_point	RW	0	1: The Link-timer will be stopped when both the link status of the DUT and the link partner are up. 0: The Link-timer will be stopped when only the link status of the DUT is up.
22.1:0	RSVD	RO	00	Reserved.

## 8.2.15. PHYCR (PHY Specific Control Register, Page 0xa43, Reg 0x18)

**Table 37. PHYCR (PHY Specific Control Register, Page 0xa43, Reg 0x18)**

Bit	Name	Type	Default	Description
24.15:14	RSVD	RO	00	Reserved.

Bit	Name	Type	Default	Description
24.13	PHYAD_0 Enable	RW	1	1: A broadcast from MAC (A command with the PHY address = 0) is valid. MDC/MDIO will respond to this command.
24.12:11	RSVD	RO	00	Reserved.
24.10	MDI Loopback	RW	0	1: Enable MDI Loopback mode
24.9:8	RSVD	RO	00	Reserved.
24.7	TX CRS Enable	RW	1	1: Assert CRS on transmit 0: Never assert CRS on transmit
24.6	PHYAD Non-zero Detect	RW	0	1: The RTL9000AA-VC/RTL9000AN-VC with PHYAD[2:0] = 000 will latch the first non-zero PHY address as its own PHY address
24.5	RSVD	RO	0	Reserved.
24.4	Preamble Check Enable	RW	1	1: Check preamble when receiving an MDC/MDIO command
24.3	Jabber Detection Enable	RW	1	1: Enable Jabber Detection
24.2:0	RSVD	RO	000	Reserved.

### 8.2.16. PHYSR2 (PHY Status Register 2, Page 0xa43, Reg 0x1A)

Table 38. PHYSR2 (PHY Status Register 2, Page 0xa43, Reg 0x1A)

Bit	Name	Type	Default	Description
26.15:3	RSVD	RO	0x0000	Reserved
26.2	Real-time Link Status	RO	0	Real-time Link Status. 1: Link 0: Not Link
26.1:0	RSVD	RO	00	Reserved

### 8.2.17. PHYSRAD (PHY SRAM Address Register, Page 0xa43, Reg 0x1B)

Table 39. PHYSRAD (PHY SRAM Address Register, Page 0xa43, Reg 0x1B)

Bit	Name	Type	Default	Description
27.15:0	PHY SRAM addr	RW	0x0000	PHY internal SRAM address

### 8.2.18. PHYSRD (PHY SRAM Data Register, Page 0xa43, Reg 0x1C)

Table 40. PHYSRD (PHY SRAM Data Register, Page 0xa43, Reg 0x1C)

Bit	Name	Type	Default	Description
28.15:0	PHY SRAM data	RW	0x0000	PHY internal SRAM data

## 8.2.19. GINSR (General Interrupt Status Register, Page 0xa43, Reg 0x1D)

**Table 41. GINSR (General Interrupt Status Register, Page 0xa43, Reg 0x1D)**

Bit	Name	Type	Default	Description
29.15:12	RSVD	RO	0000	Reserved.
29.11	PHY Fatal Error	RO, RC	0	1: PHY Fatal Error occurs 0: No PHY Fatal Error occurs
29.10	Jabber	RO, RC	0	1: Jabber detected 0: No jabber detected
29.9	RSVD	RO	0	Reserved.
29.8	PTP Interrupt	RO, RC	0	1: PTP event occurs 0: No PTP event occurs
29.7:5	RSVD	RO	000	Reserved.
29.4	Link Status Change	RO, RC	0	1: Link status changed 0: Link status not changed
29.3	RSVD	RO	0	Reserved.
29.2	General Purpose Interrupt	RO, RC	0	1: General purpose event occurs 0: No general purpose event occurs
29.1	RSVD	RO	0	Reserved.
29.0	PHY Status Change	RO, RC	0	1: PHY status changed 0: PHY status not changed

## 8.2.20. PAGSR (Page Select Register, Page 0xa43, Reg 0x1F)

**Table 42. PAGSR (Page Select Register, Page 0xa43, Reg 0x1F)**

Bit	Name	Type	Default	Description
31.15:12	RSVD	RO	0	Reserved.
31.11:0	PageSel	RW	0xa42	Page Select (in Hex). 0xa42: Page 0xa42 (default page)

## 8.2.21. GPSFR (General Purpose Sub-flag Register, Page 0xa47, Reg 0x15)

**Table 43. GPSFR (General Purpose Sub-flag Register, Page 0xa47, Reg 0x15)**

Bit	Name	Type	Default	Description
21.15:13	RSVD	RO	000	Reserved.
21.12	intr_LPS_WUR_encode	RO, RC	0	Sub-flag: LPS and WUR encoded at the same time
21.11	intr_sleep_fail	RO, RC	0	Sub-flag: PHY has once entered SLEEP_FAIL state
21.10	intr_sleep_ack	RO, RC	0	Sub-flag: PHY has once entered SLEEP_ACK state
21.9:0	RSVD	RO	0x00	Reserved.

## 8.2.22. SLPCAP (Sleep Capability Register, Page 0xa5a, Reg 0x14)

**Table 44. SLPCAP (Sleep Capability Register, Page 0xa5a, Reg 0x14)**

Bit	Name	Type	Default	Description
20.15:1	RSVD	RO	0	Reserved.

Bit	Name	Type	Default	Description
20.0	Sleep Cap	RW	0	1: Enable Sleep capability.

A Software Reset (Page 0x0 Reg 0 bit[15]=1) should be asserted in order to let the change of bit 20.0 take effect.

### 8.2.23. SLR (Scrambler Lock Register, Page 0xa60, Reg 0x11)

**Table 45. PLCR (Scrambler Lock Register, Page 0xa60, Reg 0x11)**

Bit	Name	Type	Default	Description
20.15:5	RSVD	RO	-	Reserved.
18.4	Scrambler_ok	RO	0	1: Scrambler locked 0: Scrambler unlocked
18.3:0	RSVD	RO	-	Reserved

### 8.2.24. PCR (Polarity Correction Register, Page 0xa60, Reg 0x14)

**Table 46. PLCR (Polarity Correction Register, Page 0xa60, Reg 0x14)**

Bit	Name	Type	Default	Description
20.15:7	RSVD	RO	0	Reserved.
20.8	Polarity Swap	RO	0	1: Polarity Swap
20.7:0	RSVD	RO	-	Reserved

### 8.2.25. LKTR(Link Timer Register, Page 0xa61, Reg 0x10)

**Table 47. LKTR (Link Timer Register, Page 0xa61, Reg 0x10)**

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0x00	Reserved.
16.7:0	Link_timer	RO	0x00	To derive the link-up time, please follow the steps in order: a. Set the stop point by writing Page 0xA42, Reg 22, bit [2] to 1. (Please refer to Section 8.2.12) b. Write Page 0x0, Reg 0, bit [15:0] to 0x8000. (SW Reset) c. Read the value of Page 0xA61, Reg 16, bit [7:0]. d. Calculation: Multiply the value of Page 0xA61, Reg 16, bit [7:0] (in decimal) to 983 (Resolution). The result is in $\mu$ c order.

### 8.2.26. SNRR(Signal to Noise Ratio Register, Address 0xa8c0)

**Table 48. SNRR (Signal to Noise Ratio Register, Address 0xa8c0)**

Bit	Name	Type	Default	Description
16.15:0	SNR_Reg_Value	RO	0x00	$SNR = -10 \log_{10} [SNR\_Reg\_Value \text{ (in decimal)} / (3 * 2^{17})]$ Refer to section 7.13.1.

### 8.2.27. MERR(Maximum Error Register, Address 0xa8e0)

**Table 49. MERR (Maximum Error Register, Address 0xa8e0)**

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0x00	Reserved.
16.7:0	MaxErr_Reg_Value	RO	0x00	Max Error = MaxErr_Reg_Value (in decimal) / $2^6$ Refer to section 7.13.2.

### 8.2.28. CLENR (Cable Length Register, Address 0xa890)

**Table 50. CLENR (Cable Length Register, Address 0xa890)**

Bit	Name	Type	Default	Description
16.15:8	RSVD	RO	0x00	Reserved.
16.7:0	cab_len	RO	0x00	Show result of linking cable length in meter.

### 8.2.29. SSCCR (SSC Control Register, Address 0xd012)

**Table 51. SSCCR (SSC Control Register, Address 0xd012)**

Bit	Name	Type	Default	Description
17.15:3	RSVD	RO	0	Reserved.
17.2	RMII REF_CLK SSC Enable	RW	1	1: Enable RMII REF_CLK spread spectrum clocking.
17.1	RSVD	RO	0	Reserved.
17.0	System Clock SSC Enable	RW	1	1: Enable system clock spread spectrum clocking.

### 8.2.30. RXDVCR (RXDV Control Register, Address 0xd050)

**Table 52. RXDVCR (RXDV Control Register, Address 0xd050)**

Bit	Name	Type	Default	Description
16.15:3	RSVD	RO	0x0000	Reserved
16.2	RMII_CRS_SEL	RO	0	1: The RXDV signal is sent with CRS signal 0: The RXDV signal is sent without CRS signal
16.1:0	RSVD	RO	00	Reserved

### 8.2.31. LEDCR (LED Control Register, Address 0xd040)

**Table 53. LEDCR (LED Control Register, Address 0xd040)**

Bit	Name	Type	Default	Description
16.15	led_enable	RW	1	1: LED enable

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Default</b>	<b>Description</b>
16.14	led_polar	RW	1	LED polarity bit. 1: Active high 0: Active low
16.13	led_rtct	RW	0	Switch LED modes between link status & cable diagnostics (RTCT) results. 0: Link status 1: RTCT results
16.12:6	RSVD	RO	0011000	Reserved.
16.5:4	led_blink_duty	RW	10	LED blink duty cycle. 2'b00: 12.5% 2'b01: 25% 2'b10: 50% 2'b11: 75%
16.3:2	led_blink_freq	RW	01	LED blink frequency control. 2'b00: 20ms 2'b01: 40ms 2'b10: 60ms 2'b11: Reserved
16.1	led_act	RW	1	1: LED blinks when in traffic
16.0	led_link	RW	1	1: LED turns ON when link-up

### 8.2.32. LED\_PTP (LED/PTP\_GPIO Select Register, Address 0xd42a)

Table 54. LED\_PTP (LED/PTP\_GPIO Select Register, Address 0xd42a)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Default</b>	<b>Description</b>
21.15:1	RSVD	RO	0x7ff	Reserved.
21.0	rg_led_thru_ptp_pin	RW	1	1: Pin 34 acts as LED pin 0: Pin 34 acts as PTP_GPIO pin

## 8.3. PTP Register Tables

### 8.3.1. PTP\_CTL (PTP Control Register, Address 0xe400)

**Table 55. PTP\_CTL (PTP Control Register, Address 0xe400)**

Bit	Name	Type	Default	Description
16.15:13	RSVD	RO	000	Reserved.
16.12	UDP_CHKSUM Update	RW	0	Enable auto-correction of UDP Checksum if One-Step Timestamp Insertion is enabled. Only effective to IPv6/UDP packets. 0: Set 0x0000 to the UDP Checksum field 1: Re-compute the UDP Checksum
16.11	P_DRFU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp_Follow_Up messages.
16.10	P_DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp messages.
16.9	DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Delay_Resp messages.
16.8	FU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Follow_Up messages.
16.7	P_DR_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t3-t2) to Pdelay_Response messages.
16.6	SYNC_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t1) to Sync messages.
16.5	AVB_802.1AS Support	RW	1	1: AVB 802.1AS standard support.
16.4	PTPv2_Layer2 Support	RW	1	1: PTPv2 Layer 2 packets support.
16.3	PTPv2_UDPIPv4 Support	RW	1	1: PTPv2 UDP/IPv4 packets support.
16.2	PTPv2_UDPIPv6 Support	RW	1	1: PTPv2 UDP/IPv6 packets support.
16.1	PTPv1 Support	RW	1	1: PTPv1 packets support.
16.0	PTP_Enable	RW	1	PTP function enable <i>Note: Issue a Software Reset (Page 0x0 Reg 0 bit[15]=1) after setting this bit in order to enable/disable PTP function.</i>

### 8.3.2. PTP\_INER (PTP Interrupt Enable Register, Address 0xe402)

**Table 56. PTP\_INER (PTP Interrupt Enable Register, Address 0xe402)**

Bit	Name	Type	Default	Description
17.15:4	RSVD	RO	0x000	Reserved.
17.3	Tx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Transmit Timestamp ready interrupt.
17.2	Rx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Receive Timestamp ready interrupt.
17.1	TrigGen Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Trigger Generate complete interrupt.
17.0	EventCap Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Event Capture timestamp ready interrupt.

### 8.3.3. PTP\_INSR (PTP Interrupt Status Register, Address 0xe404)

**Table 57. PTP\_INSR (PTP Interrupt Status Register, Address 0xe404)**

Bit	Name	Type	Default	Description
18.15:4	RSVD	RO	0x000	Reserved.
18.3	Tx Timestamp Interrupt	RO, RC	0	1: Transmit Timestamp ready interrupt detected.
18.2	Rx Timestamp Interrupt	RO, RC	0	1: Receive Timestamp ready interrupt detected.
18.1	TrigGen Interrupt	RO, RC	0	1: Trigger Generate complete interrupt detected.
18.0	EventCap Interrupt	RO, RC	0	1: Event Capture timestamp ready interrupt detected.

### 8.3.4. PTP\_CLK\_CFG (PTP Clock Config Register, Address 0xe410)

**Table 58. PTP\_CLK\_CFG (PTP Clock Config Register, Address 0xe410)**

Bit	Name	Type	Default	Description
16.15:7	RSVD	RO	0	Reserved.
16.6:5	ptp_clkin_freq_sel	RW	0	PTP CLKIN Frequency Select. 00: 125MHz 01: 25MHz 10: 10MHz 11: Reserved <i>Note: Issue a Software Reset (Page 0x0 Reg 0 bit[15]=1) in order to allow the setting to take effect.</i>
16.4	ptp_clkin_en	RW	0	1: Enable PTP CLKIN function at PTP_GPIO pin <i>Note: Issue a Software Reset (Page 0x0 Reg 0 bit[15]=1) in order to allow the setting to take effect.</i>
16.3:1	ptp_clkadj_mod	RW	0	PTP Clock Adjustment Mode Select. 000: No function 001: Reserved - Issue Direct Read/Write to PTP_Local_Time through PTP_Time_Config registers 010: Direct Read 011: Direct Write - Issue Step Adjustment to PTP_Local_Time through PTP_Time_Config registers 100: Increment Step 101: Decrement Step - Issue Rate Adjustment Read/Write to PTP_Rate_Adj_Amt through PTP_Time_Config_ns registers [24:0]. A 2's complement representation should be used if a negative rate adjustment is needed. 110: Rate Read 111: Rate Write
16.0	ptp_clkadj_mod_set	RW, SC	0	PTP Clock Adjustment Mode Set. 1: Activate the selected clock adjustment mode as related parameters are properly inserted.

### 8.3.5. PTP\_CFG\_NS\_LO (PTP Time Config Nano-Sec Low Register, Address 0xe412)

**Table 59. PTP\_CFG\_NS\_LO (PTP Time Config Nano-Sec Low Register, Address 0xe412)**

Bit	Name	Type	Default	Description
17.15:0	PTP_Time_Config_ns[15:0]	RW	0x0000	Time configuration nano-sec field [15:0] / Rate adjustment multiplier field [15:0] A 2's complement representation should be used if a negative rate adjustment is needed.

### 8.3.6. PTP\_CFG\_NS\_HI (PTP Time Config Nano-Sec High Register, Address 0xe414)

**Table 60. PTP\_CFG\_NS\_HI (PTP Time Config Nano-Sec High Register, Address 0xe414)**

Bit	Name	Type	Default	Description
18.15:14	RSVD	RO	00	Reserved.
18.13:0	PTP_Time_Config_ns[29:16]	RW	0	Time configuration nano-sec field_ns [29:16]/ Rate adjustment multiplier field [24:16]; [24]: Rate adjustment Sign bit (1: higher rate; 0: lower rate); [29:25]: No effect when write, Reflect Sign Extension result when read. A 2's complement representation should be used if a negative rate adjustment is needed.

### 8.3.7. PTP\_CFG\_S\_LO (PTP Time Config Sec Low Register, Address 0xe416)

**Table 61. PTP\_CFG\_S\_LO (PTP Time Config Sec Low Register, Address 0xe416)**

Bit	Name	Type	Default	Description
19.15:0	PTP_Time_Config_s[15:0]	RW	0x0000	Time configuration sec field [15:0].

### 8.3.8. PTP\_CFG\_S\_MI (PTP Time Config Sec Mid Register, Address 0xe418)

**Table 62. PTP\_CFG\_S\_MI (PTP Time Config Sec Mid Register, Address 0xe418)**

Bit	Name	Type	Default	Description
20.15:0	PTP_Time_Config_s[31:16]	RW	0x0000	Time configuration sec field [31:16].

### 8.3.9. PTP\_CFG\_S\_HI (PTP Time Config Sec High Register, Address 0xe41A)

**Table 63. PTP\_S\_HI (PTP Time Config Sec High Register, Address 0xe41A)**

Bit	Name	Type	Default	Description
21.15:0	PTP_Time_Config_s[47:32]	RW	0x0000	Time configuration sec field [47:32].

### 8.3.10. PTP\_TAI\_CFG (PTP Application I/F Config Register, Address 0xe420)

**Table 64. PTP\_TAI\_CFG (PTP Application I/F Config Register, Address 0xe420)**

Bit	Name	Type	Default	Description
16.15:10	RSVD	RO	000000	Reserved.
16.9:8	trig_mod_sel	RW	00	Trigger Generate mode select. Trigger(s) start at time specified in TAI_TS_RW registers. Valid if tai_func_sel = 01. 00: Single rising edge 01: Single falling edge (The high/low level of the GPIO will be adjusted by HW automatically.) 10: Single pulse. The pulse width can be set by pulse_amt fields 11: Periodic pulses. The pulse period and duty cycle can be set by pulse_amt (Address 0xe422, bit[9:0]) and pulse_dc (Address 0xe422, bit[13:12]) fields, see section 8.3.11.
16.7	trig_iflate	RW	0	Trigger-if-Late Control. Valid if tai_func_sel (Bit 16.2:1) = 01. 1: Allow an immediate Trigger when setting a time value which is earlier than the current time.
16.6	evnt_rf_det	RW	0	Event Capture rising/falling edge detects selection. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Detection of a rising edge 1: Detection of a falling edge SW should take care of the high/low level of GPIO with this setting.
16.5	evnt_overwr_en	RW	1	Event Capture timestamp overwrite enables. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Keep the old value, 1: Cause the event timestamp to be overwritten if a new event is detected at the specific GPIO if the upper layer has not yet read the old event timestamp.
16.4:3	tai_gpio_num	RW	00	The GPIO number that is going to be armed.
16.2:1	tai_func_sel	RW	00	PTP Application Interface function select of selected GPIO. 00: Disable function 01: Trigger Generate 10: Event Capture 11: Trigger start time/Event timestamp read (according to current GPIO settings)
16.0	tai_cfg_set	RW, SC	0	PTP Application Interface configuration set. Setting this bit will issue a TAI Configuration ‘Set’ to the selected GPIO via tai_gpio_num

### 8.3.11. PTP\_TRIG\_CFG (PTP Trigger Config Register, Address 0xe422)

**Table 65. PTP\_TRIG\_CFG (PTP Trigger Config Register, Address 0xe422)**

Bit	Name	Type	Default	Description
17.15:14	RSVD	RO	00	Reserved.
17.13:12	pulse_dc	RW	00	Duty Cycle of a Trigger Pulse. Valid if tai_func_sel (Address 0xe420, bit[2:1]) = 01. Takes effect only on GPIO 0/1. 00: 0% 01: 25% 10: 50% 11: 75%. <i>Note: The options of 0%, 25%, and 75% are available only when pulse_amt &gt;= 8.</i>
17.11:10	pulse_amt_unit	RW	00	The unit of pulse_amt field. 00: 10 nano-second (10 ns) 01: 1.25 micro-second (1.25 $\mu$ s) 10: 1.25 milli-second (1.25 ms) 11: 1.25 second (1.25 sec)
17.9:0	pulse_amt	RW	0	Period of periodic pulses/Width of the single pulse. <i>Note: pulse_amt should be greater than 0.</i>

### 8.3.12. PTP\_TAI\_STA (PTP Application I/F Status Register, Address 0xe424)

**Table 66. PTP\_TAI\_STA (PTP Application I/F Status Register, Address 0xe424)**

Bit	Name	Type	Default	Description
18.15	tai_gpio_func	RO	0	Indicate PTP_GPIO's TAI function 0: Trigger Generate 1: Event Capture
18.14	tai_gpio_en	RO	0	TAI function is enabled at PTP_GPIO.
18.13	tai_gpio_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at PTP_GPIO.
18.12	tai_gpio_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept.
18.11:0	RSVD	RO	0x000	Reserved.

### 8.3.13. PTP\_TAI\_TS\_NS\_LO (PTP TAI Timestamp Nano-Sec Low Register, Address 0xe426)

**Table 67. PTP\_TAI\_TS\_NS\_LO (PTP TAI Timestamp Nano-Sec Low Register, Address 0xe426)**

Bit	Name	Type	Default	Description
19.15:0	TAI_TS_ns[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface nanosec field [15:0].

### 8.3.14. PTP\_TAI\_TS\_NS\_HI (PTP TAI Timestamp Nano-Sec High Register, Address 0xe428)

**Table 68. PTP\_TAI\_TS\_NS\_HI (PTP TAI Timestamp Nano-Sec High Register, Address 0xe428)**

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TAI_TS_ns[29:16]	RW	0	PTP Application Interface timestamp Read/Write interface nanosec field [29:16].

### 8.3.15. PTP\_TAI\_TS\_S\_LO (PTP TAI Timestamp Sec Low Register, Address 0xe42a)

**Table 69. PTP\_S\_LO (PTP Time Config Sec Low Register, Address 0xe42a)**

Bit	Name	Type	Default	Description
21.15:0	TAI_TS_s[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [15:0].

### 8.3.16. PTP\_TAI\_TS\_S\_HI (PTP TAI Timestamp Sec High Register, Address 0xe42c)

**Table 70. PTP\_S\_MI (PTP Time Config Sec Mid Register, Address 0xe42c)**

Bit	Name	Type	Default	Description
22.15:0	TAI_TS_s[31:16]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [31:16].

### 8.3.17. PTP\_TRX\_TS\_STA (PTP TxRx Timestamp Status Register, Address 0xe430)

**Table 71. PTP\_TRX\_TS\_STA (PTP TxRx Timestamp Status Register, Address 0xe430)**

Bit	Name	Type	Default	Description
16.15	txts_sync_rdy	RO	0	Sync message Transmit timestamp ready.
16.14	txts_dlyreq_rdy	RO	0	Delay_Request Transmit timestamp ready.
16.13	txts_pdlyreq_rdy	RO	0	PDelay_Request Transmit timestamp ready.
16.12	txts_pdlyrsp_rdy	RO	0	PDelay_Response Transmit timestamp ready.
16.11	rxts_sync_rdy	RO	0	Sync message Receive timestamp ready.
16.10	rxts_dlyreq_rdy	RO	0	Delay_Request Receive timestamp ready.
16.9	rxts_pdlyreq_rdy	RO	0	PDelay_Request Receive timestamp ready.
16.8	rxts_pdlyrsp_rdy	RO	0	PDelay_Response Receive timestamp ready.
16.7:5	RSVD	RO	000	Reserved.

Bit	Name	Type	Default	Description
16.4	trxts_overwr_en	RW	1	Transmit/Receive timestamp overwrite enable. When a new PTP packet comes that needs to be time stamped, HW will 0: Keep the old timestamp value, 1: Overwrite the old timestamp value if the older one has not been read by the upper layer.
16.3:2	trxts_msgrtype_sel	RW	00	Message Type of Transmit/Receive timestamp select. 00: Sync 01: Delay_Request 10: PDelay_Request 11: PDelay_Response
16.1	trxts_sel	RW	0	Transmit/Receive timestamp read select. 0: Tx 1: Rx
16.0	trxts_rd	RW, SC	0	Transmit/Receive timestamp read enable. Issue a ‘Read’ for Transmit/Receive timestamp.

### 8.3.18. PTP\_TRX\_TS\_INFO (PTP TxRx Timestamp Info Register, Address 0xe440)

Table 72. PTP\_TRX\_TS\_INFO (PTP TxRx Timestamp Info Register, Address 0xe440)

Bit	Name	Type	Default	Description
16.15:12	trxts_transspec	RO	0000	Transmit/Receive timestamp Transport Specific field
16.11:8	trxts_msgrtype	RO	0000	Transmit/Receive timestamp Message Type field
16.7:4	RSVD	RO	0000	Reserved
16.3:0	trxts_ptpver	RO	0000	Transmit/Receive timestamp PTP Version field

### 8.3.19. PTP\_TRX\_TS\_SH (PTP TxRx Timestamp Source Hash Register, Address 0xe442)

Table 73. PTP\_TRX\_TS\_SH (PTP TxRx Timestamp Source Hash Register, Address 0xe442)

Bit	Name	Type	Default	Description
17.15:0	trxts_stchash	RO	0x0000	Transmit/Receive timestamp Source Port ID Hash field.

### 8.3.20. PTP\_TRX\_TS\_SID (PTP TxRx Timestamp Seq ID Register, Address 0xe444)

**Table 74. PTP\_TRX\_TS\_SID (PTP TxRx Timestamp Seq ID Register, Address 0xe444)**

Bit	Name	Type	Default	Description
18.15:0	trxts_seqid	RO	0x0000	Transmit/Receive timestamp Sequence ID field.

### 8.3.21. PTP\_TRX\_TS\_NS\_LO (PTP TxRx Timestamp Nano-Sec Low Register, Address 0xe446)

**Table 75. PTP\_TRX\_TS\_NS\_LO (PTP TxRx Timestamp Nano-Sec Low Register, Address 0xe446)**

Bit	Name	Type	Default	Description
19.15:0	TXRX_TS_ns[15:0]	RO	0x0000	Transmit/Receive timestamp nanosec field [15:0]

### 8.3.22. PTP\_TRX\_TS\_NS\_HI (PTP TxRx Timestamp Nano-Sec High Register, Address 0xe448)

**Table 76. PTP\_TRX\_TS\_NS\_HI (PTP TxRx Timestamp Nano-Sec High Register, Address 0xe448)**

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosec field [29:16]

### 8.3.23. PTP\_TRX\_TS\_S\_LO (PTP TxRx Timestamp Sec Low Register, Address 0xe44a)

**Table 77. PTP\_TRX\_TS\_S\_LO (PTP TxRx Timestamp Sec Low Register, Address 0xe44a)**

Bit	Name	Type	Default	Description
21.15:0	TXRX_TS_s[15:0]	RW	0x0000	Transmit/Receive timestamp sec field [15:0].

### 8.3.24. PTP\_TRX\_TS\_S\_MI (PTP TxRx Timestamp Sec Mid Register, Address 0xe44c)

**Table 78. PTP\_TRX\_TS\_S\_MI (PTP TxRx Timestamp Sec Mid Register, Address 0xe44c)**

Bit	Name	Type	Default	Description
22.15:0	TXRX_TS_s[31:16]	RW	0x0000	Transmit/Receive timestamp sec field [31:16].

### 8.3.25. PTP\_TRX\_TS\_S\_HI (PTP TxRx Timestamp Sec High Register, Address 0xe44e)

**Table 79. PTP\_TRX\_TS\_S\_HI (PTP TxRx Timestamp Sec High Register, Address 0xe44e)**

Bit	Name	Type	Default	Description
23.15:0	TXRX_TS_s[47:32]	RW	0x0000	Transmit/Receive timestamp sec field [47:32].

## 8.4. OP Register Tables

\*Note: For registers listed in this section, a special method should be used to access them. Please refer to section 7.9.5.2 Special Register Access, page 48.

### 8.4.1. OPCR1 (OP Control Register 1, Address 0xDC0C)

**Table 80. OPCR1 (OP Control Register 1, Address 0xDC0C)**

Bit	Name	Type	Default	Description
15:6	RSVD	RO	0	Reserved.
5	lwake_edge_sel	RW	0	Edge selection for local wake-up detection. 1: Falling edge detection 0: Rising edge detection
4:0	RSVD	RO	0	Reserved.

### 8.4.2. OPCR2 (OP Control Register 2, Address 0xDD00)

**Table 81. OPCR2 (OP Control Register 2, Address 0xDD00)**

Bit	Name	Type	Default	Description
15:6	RSVD	RO	0x5B	Reserved.
5	swrst_pulse	RW, SC	0	1: Software reset
4:0	op_cmd	RW	0x0	10010: go to Standby mode 10011: go to Normal mode * 10100: go to Sleep mode Others : Reserved  <small>*Note: To let PHY go to Normal mode, op_cmd_2 should be also adopted, refer to 8.4.13.</small> The OP Go to Sleep/Normal/Standby command would be cleared in the following conditions: 1. PHY goes to the Sleep mode. 2. UV event occurs at the Normal/Safety mode. 3. Reset event occurs at the Normal/Safety mode. 4. OT event occurs at the Normal/Safety mode. 5. Wake up event occurs at any state. (Option to set OPCR3 at section 8.4.3.)

### 8.4.3. OPCR3 (OP Control Register 3, Address 0xDD02)

**Table 82. OPCR3 (OP Control Register 3, Address 0xDD02)**

Bit	Name	Type	Default	Description
15:7	RSVD	RO	0x3D	Reserved.
6	wake_event_clr_op_cmd_valid_en	RW	1	1: wake event is able to clear OP go to Sleep/Normal/Standby command Valid bit
5	rg_rst	RW, SC	0	1: The PHY will be reset, that means all registers will be set to default value except for the OP registers. Note that when the reset is completed, it will be self-cleared.
4:0	RSVD	RO	0x21	Reserved.

### 8.4.4. OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08)

**Table 83. OPINSR1 (OP Interrupt Status Register 1, Address 0xDD08)**

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0x00	Reserved.
7	sleep_by_opcmd_flag	RO, RC	0	1: Transition to Sleep mode by OP go to Sleep command.
6	RSVD	RO	0	Reserved
5	sleep_by_uv_avdd33_flag*	RO, RC	0	1: Transition to Sleep mode by undervoltage on AVDD33.
4	sleep_by_uv_dvdd33_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD33.
3	sleep_by_uv_avdd12_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on AVDD12.
2	sleep_by_uv_dvdd12_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD12.
1	sleep_by_uv_mii1_flag	RO, RC	0	1: Transition to Sleep mode by undervoltage on DVDD_MII.
0	RSVD	RO	0	Reserved.

\* For RTL9000AN-VC, if the UV event happens in AVDD33 domain which means the main power is cut off, all of the flag will be reset to default value, hence there has no any record for AVDD33 UV event. That is to say, when AVDD33 UV event happens, it is impossible to read sleep\_by\_uv\_avdd33\_flag and rec\_avdd33\_flag is 1

### 8.4.5. OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C)

Table 84. OPINER1 (OP Interrupt Enable Register 1, Address 0xDD0C)

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0x00	Reserved.
7	sleep_by_hostcmd_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by OP go to Sleep command 0: Disable the interrupt of the transition to Sleep mode by OP go to Sleep command
6	RSVD	RO	1	Reserved
5	sleep_by_uv_avdd33_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on AVDD33 0: Disable the interrupt of the transition to Sleep mode by undervoltage on AVDD33
4	sleep_by_uv_dvdd33_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD33. 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD33
3	sleep_by_uv_avdd12_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on AVDD12 0: Disable the interrupt of the transition to Sleep mode by undervoltage on AVDD12
2	sleep_by_uv_dvdd12_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD12 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD12
1	sleep_by_uv_mii1_intr_en	RW	1	1: Trigger an interrupt of the transition to Sleep mode by undervoltage on DVDD_MII 0: Disable the interrupt of the transition to Sleep mode by undervoltage on DVDD_MII
0	RSVD	RO	0	Reserved.

### 8.4.6. OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E)

**Table 85. OPINMR1 (OP Interrupt Mask Register 1, Address 0xDD0E)**

Bit	Name	Type	Default	Description
15:8	RSVD	RO	0x00	Reserved.
7	sleep_by_cmd_intr_msk	RW	1	1: Transition to Sleep mode by OP go to Sleep command interrupt MASK enable
6	Reserved	RO	1	Reserved.
5	sleep_by_uv_avdd33_intr_msk	RW	1	1: Transition to Sleep mode by undervoltage on AVDD33 interrupt MASK enable
4	sleep_by_uv_dvdd33_intr_msk	RW	1	1: Transition to Sleep mode by undervoltage on DVDD33 interrupt MASK enable
3	sleep_by_uv_avdd12_intr_msk	RW	1	1: Transition to Sleep mode by undervoltage on AVDD12 interrupt MASK enable
2	sleep_by_uv_dvdd12_intr_msk	RW	1	1: Transition to Sleep mode by undervoltage on DVDD12 interrupt MASK enable
1	sleep_by_uv_mii1_intr_msk	RW	1	1: Transition to Sleep mode by undervoltage on DVDD_MII interrupt MASK enable
0	RSVD	RO	0	Reserved.

### 8.4.7. OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10)

**Table 86. OPINSR2 (OP Interrupt Status Register 2, Address 0xDD10)**

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0000	Reserved.
11	ot_flag	RO, RC	0	1: Over-temperature event occurs
10:5	RSVD	RO	000000	Reserved.
4	evnt_mii1_flag	RO, RC	0	1: Indicate recovery of undervoltage on DVDD_MII ever happened
3	rec_dvdd12_flag	RO, RC	0	1: Indicate recovery of undervoltage on DVDD12 ever happened
2	rec_avdd12_flag	RO, RC	0	1: Indicate recovery of undervoltage on AVDD12 ever happened
1	rec_dvdd33_flag	RO, RC	0	1: Indicate recovery of undervoltage on DVDD33 ever happened
0	rec_avdd33_flag*	RO, RC	0	1: Indicate recovery of undervoltage on AVDD33 ever happened

\* For **RTL9000AN-VC**, if the UV event happens in AVDD33 domain which means the main power is cut off, all of the flag will be reset to default value, hence there has no any record for AVDD33 UV event. That is to say, when AVDD33 UV event happens, it is impossible to read sleep\_by\_uv\_avdd33\_flag and rec\_avdd33\_flag is 1

### 8.4.8. OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14)

**Table 87. OPINER2 (OP Interrupt Enable Register 2, Address 0xDD14)**

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0000	Reserved.
11	ot_intr_en	RW	1	1: Enable the OT to trigger a interrupt 0: Disable the OT to trigger a interrupt
10:5	RSVD	RO	000000	Reserved.
4	evnt_mii1_intr_en	RW	1	1: Enable the UV recovery on DVDD_MII to trigger a interrupt 0: Disable the UV recovery on DVDD_MII to trigger a interrupt
3	rec_dvdd12_intr_en	RW	1	1: Enable the UV recovery on DVDD12 to trigger a interrupt 0: Disable the UV recovery on DVDD12 to trigger a interrupt
2	rec_avdd12_intr_en	RW	1	1: Enable the UV recovery on AVDD12 to trigger a interrupt 0: Disable the UV recovery on AVDD12 to trigger a interrupt
1	rec_dvdd33_intr_en	RW	1	1: Enable the UV recovery on DVDD33 to trigger a interrupt 0: Disable the UV recovery on DVDD33 to trigger a interrupt
0	rec_avdd33_intr_en	RW	1	1: Enable the UV recovery on AVDD33 to trigger a interrupt 0: Disable the UV recovery on AVDD33 to trigger a interrupt

### 8.4.9. OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16)

**Table 88. OPINMR2 (OP Interrupt Mask Register 2, Address 0xDD16)**

Bit	Name	Type	Default	Description
15:12	RSVD	RO	0000	Reserved.
11	ot_intr_msk	RW	1	1: OT interrupt MASK enable
10:5	RSVD	RO	000000	Reserved.
4	evnt_mii1_intr_msk	RW	1	1: UV recovery on DVDD_MII interrupt MASK enable
3	rec_dvdd12_intr_msk	RW	1	1: UV recovery on DVDD12 interrupt MASK enable
2	rec_avdd12_intr_msk	RW	1	1: UV recovery on AVDD12 interrupt MASK enable
1	rec_dvdd33_intr_msk	RW	1	1: UV recovery on DVDD33 interrupt MASK enable
0	rec_avdd33_intr_msk	RW	1	1: UV recovery on AVDD33 interrupt MASK enable

### 8.4.10. OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18)

**Table 89. OPINSR3 (OP Interrupt Status Register 3, Address 0xDD18)**

Bit	Name	Type	Default	Description
15	rec_rg_rst_flag	RO, RC	0	1: Reset is active by the MDIO command
14	rec_pin_rst_flag	RO, RC	0	1: Reset is active by the PHYRSTB pin
13	a33_pwon_flag	RO, RC	0	1: AVDD33 is power on
12	vbat_pwon_flag (RTL9000AA-VC only)	RO, RC	0	1: VBAT is power on
11	pwon_flag	RO, RC	0	<b>RTL9000AA-VC</b> 1: PHY is power on by VBAT <b>RTL9000AN-VC</b> 1: PHY is power on by AVDD33
10	lwake_flag	RO, RC	0	1: PHY is woken up by local wake up This flag will be cleared if the following events happen. 1. PHY goes to the Reset or Standby from the Normal mode. 2. PHY goes to the Reset or Standby from the Safety mode. 3. PHY goes to the Sleep mode from any state.
9:6	RSVD	RO	0000	Reserved.
5	wur_flag	RO, RC	0	1: PHY received WUR
4:1	RSVD	RO	0000	Reserved.
0	rwake_flag	RO, RC	0	1: PHY is woken up by remote wake up This flag will be cleared if the following events happen. 1. PHY goes to the Reset or Standby from the Normal mode. 2. PHY goes to the Reset or Standby from the Safety mode. 3. PHY goes to the Sleep mode from any stat

### 8.4.11. OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C)

**Table 90. OPINER3 (OP Interrupt Enable Register 3, Address 0xDD1C)**

Bit	Name	Type	Default	Description
15	rec_rg_rst_intr_en	RO	1	1: enable reset by the register to trigger interrupt
14	rec_pin_rst_intr_en	RO	1	1: enable reset by the pin to trigger interrupt
13	RSVD	RO	0	Reserved
12	RSVD	RO	0	Reserved
11	pwon_intr_en	RO	1	1: enable power on event to trigger interrupt
10	lwake_intr_en	RO	1	1: enable local wake up to trigger interrupt
9:6	RSVD	RO	0000	Reserved.
5	wur_intr_en	RO	1	1: enable wakeup request to trigger interrupt
4:1	RSVD	RO	0000	Reserved.
0	rwake_intr_en	RO	1	1: enable remote wake up to trigger interrupt

### 8.4.12. OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E)

**Table 91. OPINMR3 (OP Interrupt Mask Register 3, Address 0xDD1E)**

Bit	Name	Type	Default	Description
15	rec_rg_rst_intr_msk	RO	1	1: reset by register interrupt MASK enable
14	rec_pin_rst_intr_msk	RO	1	1: reset by the PHYRSTB pin interrupt MASK enable
13	RSVD	RO	0	Reserved
12	RSVD	RO	0	Reserved
11	pwon_intr_msk	RO	1	1: power on interrupt MASK enable
10	lwake_intr_msk	RO	1	1: local wake up interrupt MASK enable
9:6	RSVD	RO	0000	Reserved.
5	wur_intr_msk	RO	1	1: WUR interrupt MASK enable
4:1	RSVD	RO	0000	Reserved.
0	rwake_intr_msk	RO	1	1: remote wake up interrupt MASK enable

### 8.4.13. OPCR4 (OP Control Register 4, Address 0xDD20)

**Table 92. OPCR4 (OP Control Register 4, Address 0xDD20)**

Bit	Name	Type	Default	Description
15:5	RSVD	RW	0	Reserved.
4	wupr_tx	RW, SC	0	1: Enable WUP / WUR Request
2:0	op_cmd_2	RW	000	1011: go to Normal mode* Others: Reserved <p>*Note: To let the PHY go to Normal mode, op_cmd should be also adopted, refer to 8.4.2.  The OP Go to Sleep/Normal/Standy command would be cleared in the following conditions:  1. PHY goes to the Sleep mode.  2. UV event occurs at the Normal/Safety mode.  3. Reset event occurs at the Normal/Safety mode.  4. OT event occurs at the Normal/Safety mode.  5. Wake up event occurs at any state. (Option to set OCPR3 at section 8.4.3.)</p>

## 9. Power Sequence and Regulators

The RTL9000AA-VC/RTL9000AN-VC incorporates linear low-dropout regulators (LDO) that features high power supply ripple rejection and low output noise. Power inductors are not needed for the RTL9000AA-VC/RTL9000AN-VC; only an output capacitor is required between the 1.2V outputs and the analog ground for phase compensation, which saves cost and PCB real estate.

Use an X5R/X7R low-ESR ceramic capacitor, with capacitance of at least 0.1uF, to enhance the stability of output voltage. The bypass capacitors should be placed as close as possible to power pins (AVDD12 and DVDD12) for adequate filtering.

The regulator 1.2V output pin (AVDD12 and DVDD12) should be connected only to the ground via the output capacitors (do not provide this power source to other devices).

The RTL9000AA-VC/RTL9000AN-VC supports 3.3V I/O voltage of the MI/RMII/RGMII interface, this 3.3V power source should be provided by the external power source. The RTL9000AA-VC/RTL9000AN-VC also supports internal LDO for 1.8V/2.5V I/O voltage with some changes of settings, this 1.8V/2.5V power source could also be provided by external power source. Table 93 shows the parameter setting for I/O Power selection while using different power sources.

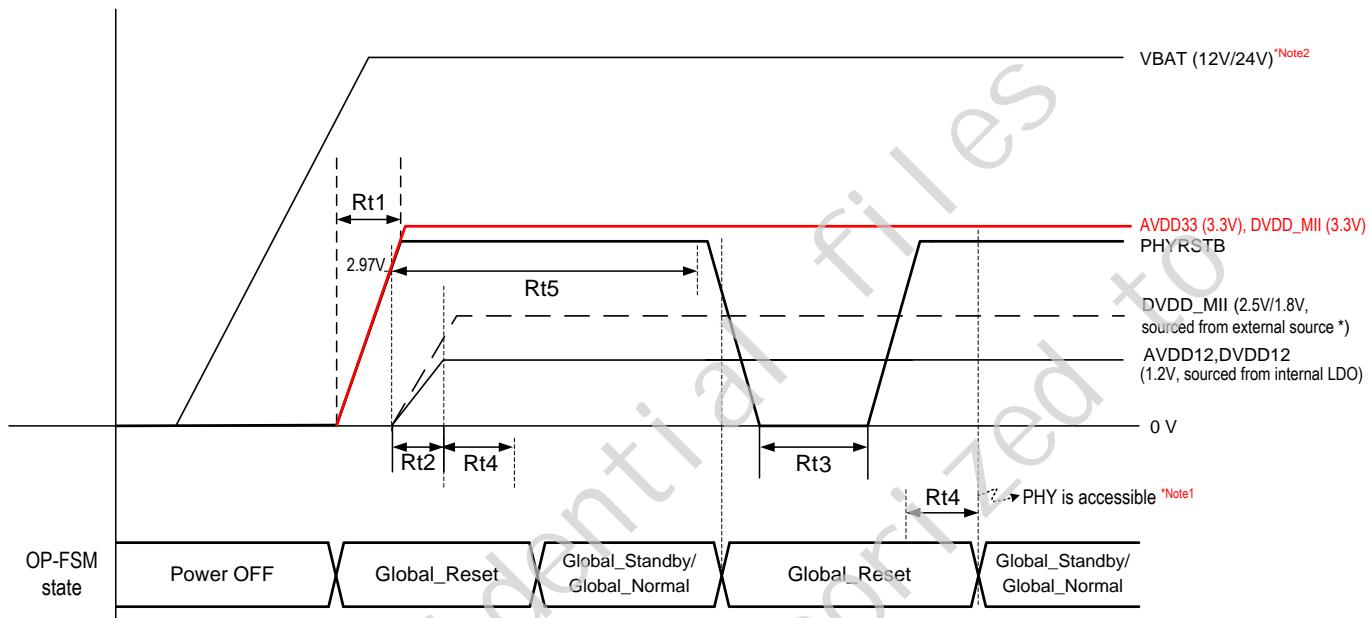
**Table 93. Parameter setting for I/O Power Selection**

I/O Power Selection	Parameter setting
External 3.3V	1. Write Reg 31 Data = 0x0A43 2. Write Reg 27 Data = 0xDC06 3. Write Reg 28 Data = 0x0DF8
Internal LDO 2.5V	1. Write Reg 31 Data = 0x0A43 2. Write Reg 27 Data = 0xDC06 3. Write Reg 28 Data = 0x5DF9
External 2.5V	1. Write Reg 31 Data = 0x0A43 2. Write Reg 27 Data = 0xDC06 3. Write Reg 28 Data = 0xDDF9
Internal LDO 1.8V	1. Write Reg 31 Data = 0x0A43 2. Write Reg 27 Data = 0xDC06 3. Write Reg 28 Data = 0xADFA
External 1.8V	1. Write Reg 31 Data = 0x0A43 2. Write Reg 27 Data = 0xDC06 3. Write Reg 28 Data = 0xEDFA

\*Note that after writing these registers for selecting the different I/O power, cycling the PHYRSTB should be performed.

The VBAT pin of the RTL9000AA-VC/RTL9000AN-VC should be connected to either the 12V/24V car battery or the 3.3V power.

## 9.1. Power Sequence



**Figure 34. Power Sequence**

\*Note1: Please confirm PHY is accessible by polling the value of PHY Status Sub-flag Register, Page 0xa42, Reg 0x10, bit [2:0], see 8.2.9, is equal to 0x3 first before accessing the other PHY register.

\*Note2: RTL9000AN-VC doesn't have the VBAT pin.

**Table 94. Power Sequence Parameters**

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.15	-	100	ms
Rt2	3.3V ready to 1.2V ready time	0.15	-	0.46	ms
Rt3	3.3V Off Time (PHYRSTB active time)	10			ms
Rt4	Core Logic Ready Time	4	-	-	ms
Rt5	Link-up time	-	-	100	ms

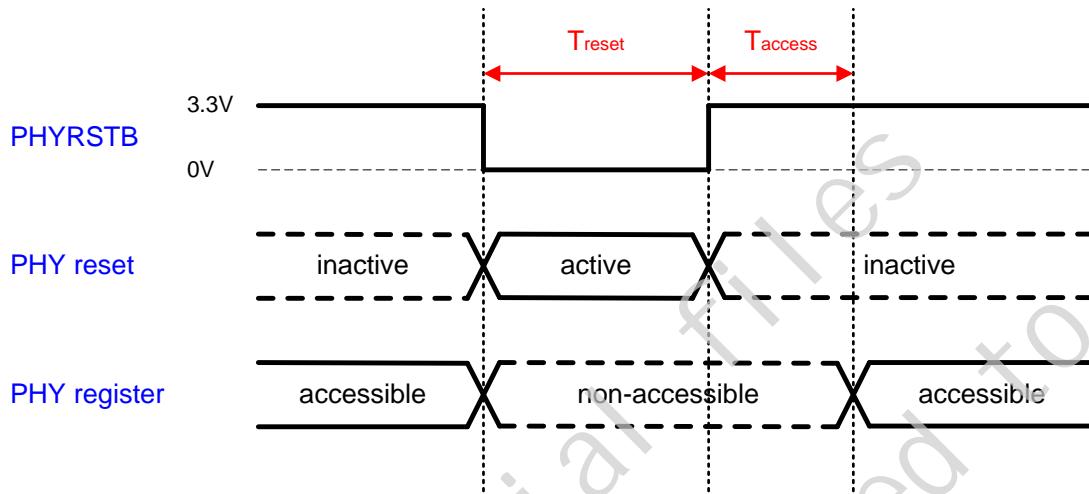
\*Note: The external power for I/O has to be given before Rt2.

## 9.2. Reset

The RTL9000AA-VC/RTL9000AN-VC implements two methods to reset the chip:

- Hardware Reset:

The RTL9000AA-VC/RTL9000AN-VC has a **PHYRSTB** pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (as shown in Figure 35) to return to a pre-defined reset state. After the de-assertion of **PHYRSTB**, wait for at least 4ms (for internal circuits settling time; see Figure 35). Please poll until the value of PHY Status Sub-flag Register, Page 0xa42, Reg 0x10, bit [2:0], see 8.2.9, is equal to 0x0003 first before accessing the PHY register. All registers except for OP registers will return to default values after a hardware reset.



**Figure 35. PHY Reset Timing**

**Table 95. PHY Reset Signal Timing Parameter**

Symbol	Parameter	Min	Max	Units
T <sub>reset</sub>	PHY reset active time	10	-	ms
T <sub>access</sub>	Timing from PHYRSTB de-asserted to access PHY registers	-	4	ms

- Software Reset:

Use the BMCR reset command at Page 0x0, Reg 0x00, bit[15] = 1, see 8.2.1, to reset the chip. When a software reset is done, please poll the value of Page 0x0, Reg 0x00 is equal to 0x2100 first before accessing the other registers of the PHY.

## 10. Characteristics

### 10.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 96. Absolute Maximum Ratings**

Symbol	Description	Minimum	Maximum	Unit
VBAT (RTL9000AA-VC)	Supply Voltage 12V/24V	-0.3	60	V
AVDD33, DVDD_MII	Supply Voltage 3.3V	-0.3	3.63	V
AVDD12, DVDD12	Supply Voltage 1.2V	-0.3	1.32	V
MDIP, MDIN	Voltage on pins MDIP, MDIN	-0.3	3.63	V
INH	Voltage on pin INH	RTL9000AA-VC	-0.3	VBAT+0.3V
		RTL9000AN-VC	-0.3	3.63V
WAKE	Voltage on pin WAKE	RTL9000AA-VC	-0.3	VBAT+0.3V
		RTL9000AN-VC	-0.3	3.63V
XTAL_IN, XTAL_OUT	Voltage on pins XTAL_IN, XTAL_OUT	-0.3	3.63	V
RXD[3:0], RXDV, RXER, INTB	Voltage on digital output pins (configured as 3.3V I/O)	-0.3	3.63	V
	Voltage on digital output pins (configured as 2.5V I/O)	-0.3	2.8	V
	Voltage on digital output pins (configured as 1.8V I/O)	-0.3	2.3	V
Other Pins	Voltage on other pins	-0.3	5.25	V
V <sub>TR</sub>	Transient voltage: pulse 1	-100	-	V
	Transient voltage: pulse 2a	-	75	V
	Transient voltage: pulse 3a	-150	-	V
	Transient voltage: pulse 3b	-	100	V
T <sub>STG</sub>	Storage temperature	-55	150	°C

*Note1: Refer to the most updated schematic circuit for correct configuration.*

*Note2: Transient voltage on VBAT, MDIP, MDIN, WAKE pins. Confirmed by FTZ.*

### 10.2. Recommended Operating Conditions

**Table 97. Recommended Operating Conditions**

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage 12V/24V (RTL9000AA-VC)	VBAT	2.8	12 / 24	-	V
Supply Voltage 3.3V	AVDD33	3.14	3.3	3.46	V
Supply Voltage 1.2V	AVDD12, DVDD12	1.14	1.2	1.26	V
Supply Voltage I/O Power (configured as 3.3V I/O)	DVDD_MII	3.14	3.3	3.46	V
Supply Voltage I/O Power (configured as 2.5V I/O)	DVDD_MII	2.38	2.5	2.63	V

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage I/O Power (configured as 1.8V I/O)	DVDD_MII	1.71	1.8	1.89	V
Ambient Operating Temperature, T <sub>AMB</sub>	-	-40	-	125	°C

## 10.3. Thermal Characteristics

**Table 98. Thermal Characteristics**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R <sub>th(j-a)</sub>	Thermal Resistance (junction to ambient)	-	34.18	-	K/W
R <sub>th(j-c)</sub>	Thermal Resistance (junction to case)	-	10.41	-	K/W

## 10.4. Power Dissipation

The following data were measured under temperature from 25°C to 125°C, VADD33 voltage is 3.3V ~ 3.63V, AVDD12 is 1.2V ~ 1.32V and DVDD\_MII is 3.3V MII mode.

**Table 99. RTL9000AA-VC Power Dissipation**

Power pin	Minimum	Typical	Maximum	Unit
<b>Normal mode</b>				
VBAT	-	1.47	1.55	mA
AVDD33	-	44.7	45.2	mA
DVDD33	-	5.81	5.9	mA
AVDD12	-	16.5	18.5	mA
DVDD12	-	15.8	17.3	mA
<b>Standby mode</b>				
VBAT	-	1.37	1.4	mA
AVDD33	-	12.2	14.8	mA
DVDD33	-	4.38	4.9	mA
AVDD12	-	9.3	10.9	mA
DVDD12	-	9	10.5	mA
<b>Reset mode</b>				
VBAT	-	1.37	1.5	mA
AVDD33	-	12.4	14.8	mA
DVDD33	-	0.6	0.63	mA
AVDD12	-	8.81	10.3	mA
DVDD12	-	1.07	1.59	mA
<b>Deep Sleep mode</b>				
VBAT	-	33.8	45.2	µA
AVDD33	-	0	0	mA
DVDD33	-	0	0	mA
AVDD12	-	0	0	mA
DVDD12	-	0	0	mA

**Table 100. RTL9000AN-VC Power Dissipation**

Power pin	Minimum	Typical	Maximum	Unit
<b>Normal mode</b>				
AVDD33	-	46.17	46.75	mA
DVDD33	-	5.81	5.9	mA
AVDD12	-	16.5	18.5	mA
DVDD12	-	15.8	17.3	mA
<b>Standby mode</b>				
AVDD33	-	13.57	16.2	mA
DVDD33	-	4.38	4.9	mA
AVDD12	-	9.3	10.9	mA
DVDD12	-	9	10.5	mA
<b>Reset mode</b>				
AVDD33	-	13.77	16.3	mA
DVDD33	-	0.6	0.63	mA
AVDD12	-	8.81	10.3	mA
DVDD12	-	1.07	1.59	mA
<b>Lite Sleep mode</b>				
AVDD33	-	12.88	14.20	mA
DVDD33	-	0	0.01	mA
AVDD12	-	8.35	10.66	mA
DVDD12	-	0.68	1.79	mA

## 10.5. DC Characteristics

**Table 101. DC Characteristics**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
<b>Pin VBAT (RTL9000AA-VC)</b>						
V <sub>uvd_VBAT</sub>	Under voltage detection voltage on VBAT pin		2.65	2.8	2.81	V
V <sub>uvr_VBAT</sub>	Under voltage recovery voltage on VBAT pin		2.77	2.85	2.86	V
V <sub>uvhys_VBAT</sub>	Under voltage hysteresis voltage on VBAT pin		45.7	50	89.5	mV
<b>Pin AVDD33 (RTL9000AA-VC)</b>						
V <sub>uvd_AVDD33</sub>	Under voltage detection voltage on AVDD33 pin		2.85	3.03	3.15	V
V <sub>uvr_AVDD33</sub>	Under voltage recovery voltage on AVDD33 pin		2.90	3.07	3.20	V
V <sub>uvhys_AVDD33</sub>	Under voltage hysteresis voltage on AVDD33 pin		35	40	43	mV
T <sub>uvd_AVDD33</sub>	Under voltage detection time		16	32	54	μs
T <sub>uvr_AVDD33</sub>	Under voltage recovery time		3	8	23	μs
T <sub>tout_AVDD33</sub>	Under voltage timeout to Global_Sleep			100		ms

Pin AVDD33 (RTL9000AN-VC)						
V <sub>uvd_AVDD33</sub>	Under voltage detection voltage on AVDD33 pin		2.53	2.6	2.66	V
V <sub>uvr_AVDD33</sub>	Under voltage recovery voltage on AVDD33 pin		2.56	2.64	2.69	V
V <sub>uvphys_AVDD33</sub>	Under voltage hysteresis voltage on AVDD33 pin		26.70	-	30.26	mV
T <sub>uvd_AVDD33</sub>	Under voltage detection time		16	32	54	μs
T <sub>uvr_AVDD33</sub>	Under voltage recovery time		3	8	23	μs
T <sub>tout_AVDD33</sub>	Under voltage timeout to Global_Sleep			100		ms
Pin DVDD_MII						
V <sub>uvd_DVDD_MII</sub>	Under voltage detection voltage on DVDD_MII pin		3.003	3.03	3.051	V
V <sub>uvr_DVDD_MII</sub>	Under voltage recovery voltage on DVDD_MII pin		3.043	3.07	3.089	V
V <sub>uvphys_DVDD_MII</sub>	Under voltage hysteresis voltage on DVDD_MII pin		35.534	40	44.463	mV
T <sub>uvd_DVDD_MII</sub>	Under voltage detection time		200		525	ns
T <sub>uvr_DVDD_MII</sub>	Under voltage recovery time		165		555	ns
T <sub>tout_DVDD_MII</sub>	Under voltage timeout to Global_Sleep			100		ms
Pin AVDD12						
V <sub>uvd_AVDD12</sub>	Under voltage detection voltage on AVDD12 pin		1.088	1.10	1.116	V
V <sub>uvr_AVDD12</sub>	Under voltage recovery voltage on AVDD12 pin		1.107	1.12	1.136	V
V <sub>uvphys_AVDD12</sub>	Under voltage hysteresis voltage on AVDD12 pin		17.673	20	21.326	mV
T <sub>uvd_AVDD12</sub>	Under voltage detection time on AVDD12 pin		200		525	ns
T <sub>uvr_AVDD12</sub>	Under voltage recovery time on AVDD12 pin		165		555	ns
T <sub>tout_AVDD12</sub>	Under voltage timeout to Global_Sleep on AVDD12 pin			100		ms
Pin INH (RTL9000AA-VC)						
V <sub>OH_INH</sub>	HIGH-level output voltage	I <sub>INH</sub> = 3mA V <sub>BAT</sub> = 12V	V <sub>BAT</sub> - 2		V <sub>BAT</sub>	V
V <sub>OL_INH</sub>	LOW-level output voltage		-0.3	0	+0.4	V
I <sub>OH_INH</sub>	HIGH-level output current	INH Pin = HIGH V <sub>BAT</sub> = 12V	-4.51		-2.20	mA
I <sub>Leakage</sub>	Leakage current	Power off			4	μA
Pin INH (RTL9000AN-VC)						
V <sub>OH_INH</sub>	HIGH-level output voltage	With capacitance loading max. 20pF only <sup>Note3</sup>	2.4		-	V
V <sub>OL_INH</sub>	LOW-level output voltage		-	0	0.4	V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I <sub>OH_INH</sub>	HIGH-level output current	V <sub>INH</sub> = High, INH pin tied to 0V.	-5.97		-1.61	mA
I <sub>leakage</sub>	Leakage current	Power off			4	µA
<b>Pin WAKE (RTL9000AA-VC)</b>						
V <sub>IH_WAKE</sub>	HIGH-level input voltage	Sleep mode	1.20		2.55	V
V <sub>IL_WAKE</sub>	LOW-level input voltage	Sleep mode	0.55		1.07	V
V <sub>hys_WAKE</sub>	Hysteresis input voltage	Sleep mode	0.76		1.37	V
T <sub>det_WAKE</sub>	Local WAKE event detection time	Sleep mode	14.5		60.0	µs
<b>Pin WAKE (RTL9000AN-VC)</b>						
V <sub>det_WAKE</sub>	Detective level input voltage	Sleep mode	1.065		1.682	V
T <sub>det_WAKE</sub>	Local WAKE event detection time	Sleep mode	14.5		60.0	µs
<b>Pin XTAL_IN</b>						
V <sub>IH_XTAL_IN</sub>	HIGH-level input voltage		2	3.3	3.63	V
V <sub>IL_XTAL_IN</sub>	LOW-level input voltage		-0.3	0	+0.8	V
<b>Pin XTAL_OUT</b>						
V <sub>OH_XTAL_OUT</sub>	HIGH-level output voltage		2.4	3.3	3.63	V
V <sub>OL_XTAL_OUT</sub>	LOW-level output voltage		-0.3	0	+0.4	V
V <sub>IH_XTAL_OUT</sub>	HIGH-level input voltage		1.4			V
V <sub>IL_XTAL_OUT</sub>	LOW-level input voltage				0.4	V
<b>Pins PHYRSTB, DISB</b>						
V <sub>DET</sub>	Detection time		12.5		43.5	µs
<b>Pins MDIP and MDIN</b>						
Z <sub>O_MDI</sub>	Output impedance	Normal mode	40	50	60	Ω

Note1: Pins not mentioned above remain at 3.3V.

Note2: Positive currents flow into the chip.

Note3: For INH pin of RTL9000AN-VC, any resistance loading is not allowed, including the resistors on the PCB and weak pull resistors inside the connected pin.

**Table 102. Digital IO Characteristics**

Parameter	SYM	Condition	Min	Typical	Max	Units
Input Current	I <sub>in</sub>	-	0	-	100	µA
Leakage Current	I <sub>L</sub>	Power off; V <sub>IO</sub> = 3.3V		0	2.5	µA
HIGH-level input voltage	V <sub>IH</sub>	Power Supply for Digital IO=3.3V	2.0	-	VDD33+0.3	V
LOW-level input voltage	V <sub>IL</sub>	Power Supply for Digital IO=3.3V	-0.3	-	0.8	V
HIGH-level output voltage	V <sub>OH</sub>	Power Supply for Digital IO=3.3V; I <sub>OH</sub> = 8mA	2.4	-	-	V
LOW-level ouput voltage	V <sub>OL</sub>	Power Supply for Digital IO=3.3V; I <sub>OL</sub> = 8mA	-	-	0.4	V
HIGH-level input voltage	V <sub>IH</sub>	Power Supply for Digital IO=2.5V	1.7	-	VDD25+0.3	V
LOW-level input voltage	V <sub>IL</sub>	Power Supply for Digital IO=2.5V	-0.3	-	0.7	V
HIGH-level output voltage	V <sub>OH</sub>	Power Supply for Digital IO=2.5V; I <sub>OH</sub> = 4mA	2.0	-	-	V
LOW-level ouput voltage	V <sub>OL</sub>	Power Supply for Digital IO=2.5V; I <sub>OL</sub> = 4mA	-	-	0.4	V
HIGH-level input voltage	V <sub>IH</sub>	Power Supply for Digital IO=1.8V	1.2	-	VDD18+0.3	V

Parameter	SYM	Condition	Min	Typical	Max	Units
LOW-level input voltage	V <sub>IL</sub>	Power Supply for Digital IO=1.8V	-0.3	-	0.5	V
HIGH-level output voltage	V <sub>OH</sub>	Power Supply for Digital IO=1.8V; I <sub>OH</sub> = 2mA	0.9*VDD18	-	-	V
LOW-level ouput voltage	V <sub>OL</sub>	Power Supply for Digital IO=1.8V; I <sub>OL</sub> = 2mA	-	-	0.1*VDD18	V

Note: Digital IO pins include MDC, MDIO, INTB, PHYRSTB, DISB, LED/PTP\_GPIO, TXC, TXEN, TXD[3:0], RXC, RXDV, RXER, RXD[3:0]

## 10.6. Over Temperature Protection

Table 103. Over Temperature Protection

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T <sub>otp_det</sub>	Over temperature protection detection junction temperature			145		°C
T <sub>otp_rec</sub>	Over temperature protection recovery junction temperature			135		°C
T <sub>otp_hys</sub>	Over temperature protection hysteresis temperature			10		°C

## 10.7. ESD

The ESD tolerance of RTL9000AA-VC and RTL9000AN-VC are listed in Table 104 and Table 105 individually:

**Table 104. RTL9000AA-VC ESD Criteria**

<b>Feature description</b>		<b>Value</b>	<b>Comment</b>
HBM – MDIP, MDIN pins		$\pm 4\text{kV}$	Model 4
HBM – Other global pins		$\pm 4\text{kV}$	Other global pins: VBAT, WAKE, and INH pin (connected directly to wiring harness)
HBM – Others		$\pm 2\text{kV}$	
MM		$\pm 200\text{V}$	
CDM – Corner pins		$\pm 750\text{V}$	
CDM – Others		$\pm 500\text{V}$	
Un-powered ESD	Contact discharge: E-Gun - MDIP, MDIN, and other global pins.	$\pm 6\text{kV}$	
Powered ESD	Contact discharge: E-Gun - MDIP, MDIN	$\pm 6\text{kV}$	
Latch Up		P: $1.5 \times \text{VDD}$ ; I: 100mA	

**Table 105. RTL9000AN-VC ESD Criteria**

<b>Feature description</b>		<b>Value</b>	<b>Comment</b>
HBM – MDIP, MDIN pins		$\pm 4\text{kV}$	Model 4
HBM – Others		$\pm 2\text{kV}$	
MM		$\pm 200\text{V}$	
CDM – Corner pins		$\pm 750\text{V}$	
CDM – Others		$\pm 500\text{V}$	
Un-powered ESD	Contact discharge: E-Gun - MDIP, MDIN.	$\pm 6\text{kV}$	
Powered ESD	Contact discharge: E-Gun - MDIP, MDIN.	$\pm 6\text{kV}$	
Latch Up		P: $1.5 \times \text{VDD}$ ; I: 100mA	

## 10.8. Crystal Requirements

**Table 106. Crystal Requirements**

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F <sub>ref</sub>	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F <sub>ref</sub> Tolerance <sup>[2]</sup>	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T <sub>a</sub> =0°C~70°C.	-100	-	+100	ppm
F <sub>ref</sub> Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	100 <sup>[3]</sup>	Ω
DL	Drive Level.	-	-	0.2	mW
Jitter	RMS Jitter <sup>[1]</sup>	-	3	-	ps
V <sub>ih</sub> _CKXTAL	Crystal Output High Level	1.4	-	-	V
V <sub>il</sub> _CKXTAL	Crystal Output Low Level	-	-	0.4	V

Note 1: Phase noise 25kHz to 25MHz RMS < 3ps.

Note 2: F<sub>ref</sub> Tolerance +/- 50ppm including effects of aging for the first year, external crystal capacitors, and PCB layout.

Note 3: The maximum value of ESR depends on the 'shunt capacitance' specified by the crystal manufacturer and the two 'load capacitors'. As a result, the feasible max shunt capacitance is 5 pF.

## 10.9. Oscillator/External Clock Requirements

**Table 107. Oscillator/External Clock Requirements**

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance <sup>[2]</sup>	T <sub>a</sub> =-40°C~125°C	-100	-	100	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter <sup>[1]</sup>	-	-	3	30 <sup>[3]</sup>	ps
V <sub>ih</sub>	-	1.4	-	-	V
V <sub>il</sub>	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	-40	-	125	°C

Note 1: Phase noise 25kHz to 25MHz RMS < 3ps.

Note 2: Frequency Tolerance +/- 100ppm including effects of aging for the first year, external crystal capacitors, and PCB layout.

Note 3: The external input clock with RMS jitter 30ps is the worst case. Any degradation factors on the RMS jitter of external clock source should be taken into consideration, including the supply voltage, temperature, aging, process ... etc..

## 10.10. AC Characteristics

### 10.10.1. MDC/MDIO Timing

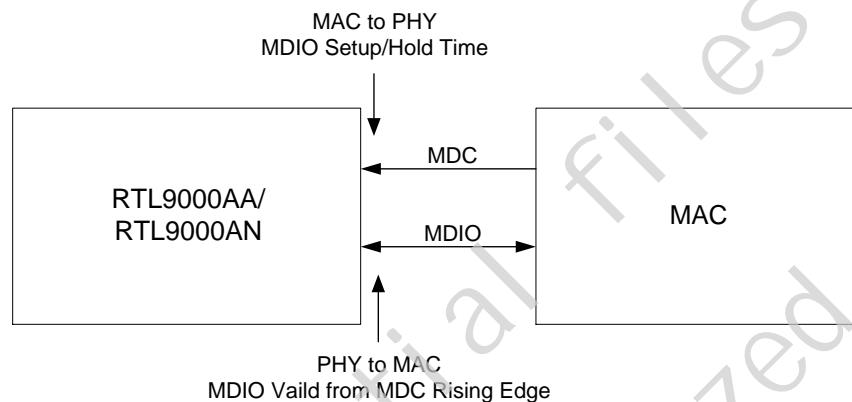


Figure 36. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

#### MDC/MDIO Timing – Management Port

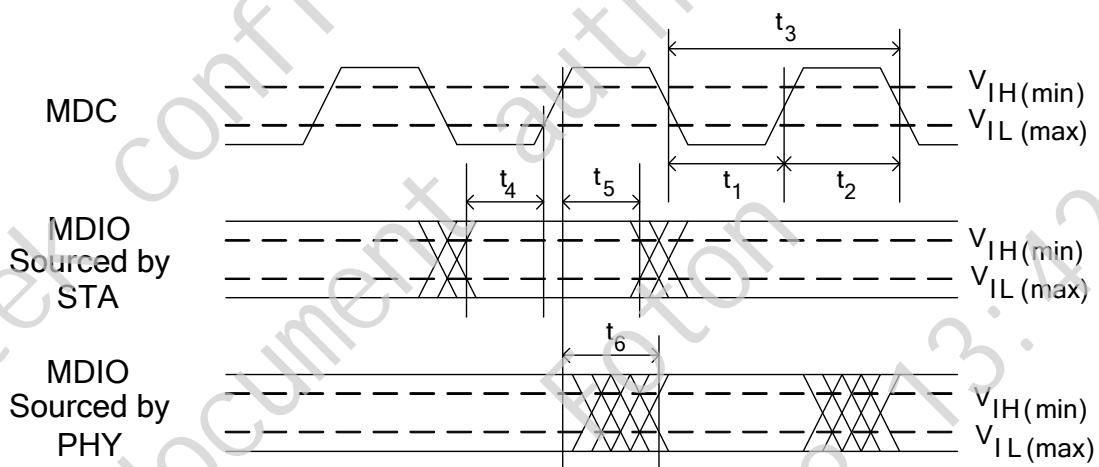
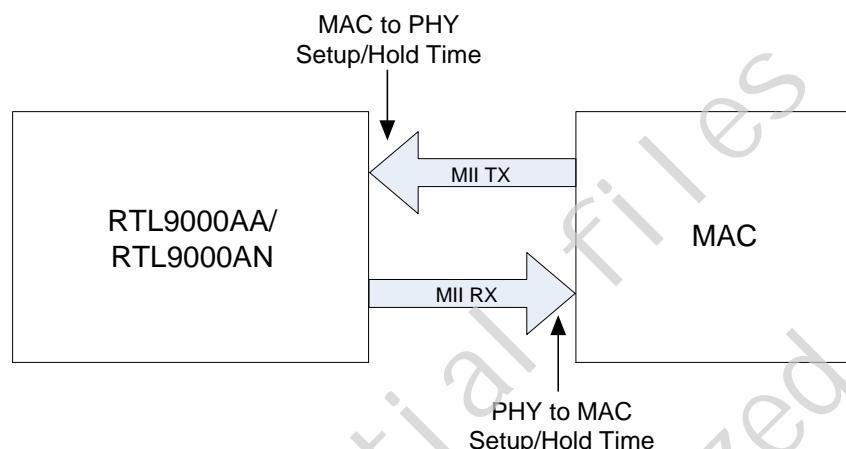


Figure 37. MDC/MDIO Management Timing Parameters

Table 108. MDC/MDIO Management Timing Parameters

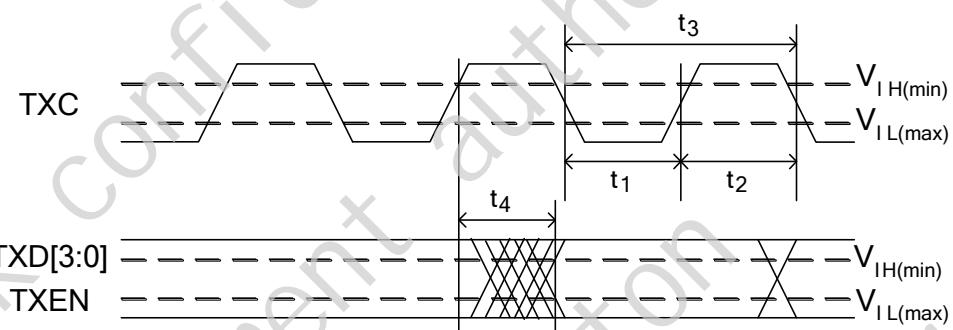
Symbol	Description	Minimum	Maximum	Unit
$t_1$	MDC Low Pulse Width	160	-	ns
$t_2$	MDC High Pulse Width	160	-	ns
$t_3$	MDC Period	400	-	ns
$t_4$	MDIO Setup to MDC Rising Edge	10	-	ns
$t_5$	MDIO Hold Time from MDC Rising Edge	10	-	ns
$t_6$	MDIO Valid from MDC Rising Edge	0	300	ns

### 10.10.2. MII Transmission Cycle Timing



**Figure 38. MII Interface Setup/Hold Time Definitions**

Figure 39 shows an example of a packet transfer from MAC to PHY on the MII interface.



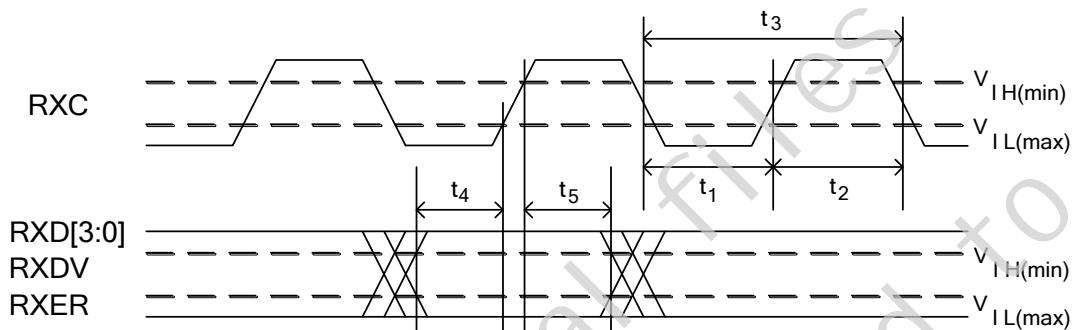
**Figure 39. MII Transmission Cycle Timing**

**Table 109. MII Transmission Cycle Timing**

Symbol	Description	Minimum	Typical	Maximum	Unit
$t_1, t_2$	TXCLK Duty Cycle	40	50	60	%
$t_3$	TXCLK Period	-	40	-	ns
$t_4$	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	0	-	25	ns

### 10.10.3. MII Reception Cycle Timing

Figure 40 shows an example of a packet transfer from PHY to MAC on the MII interface.

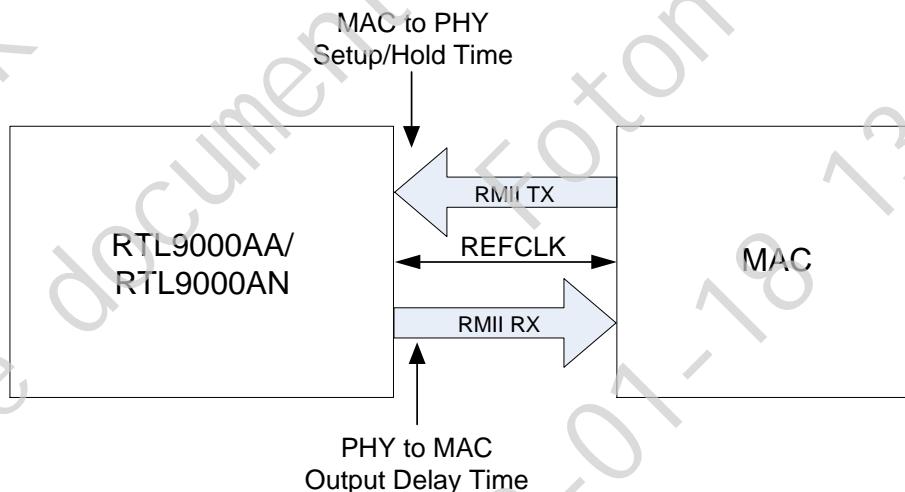


**Figure 40. MII Reception Cycle Timing**

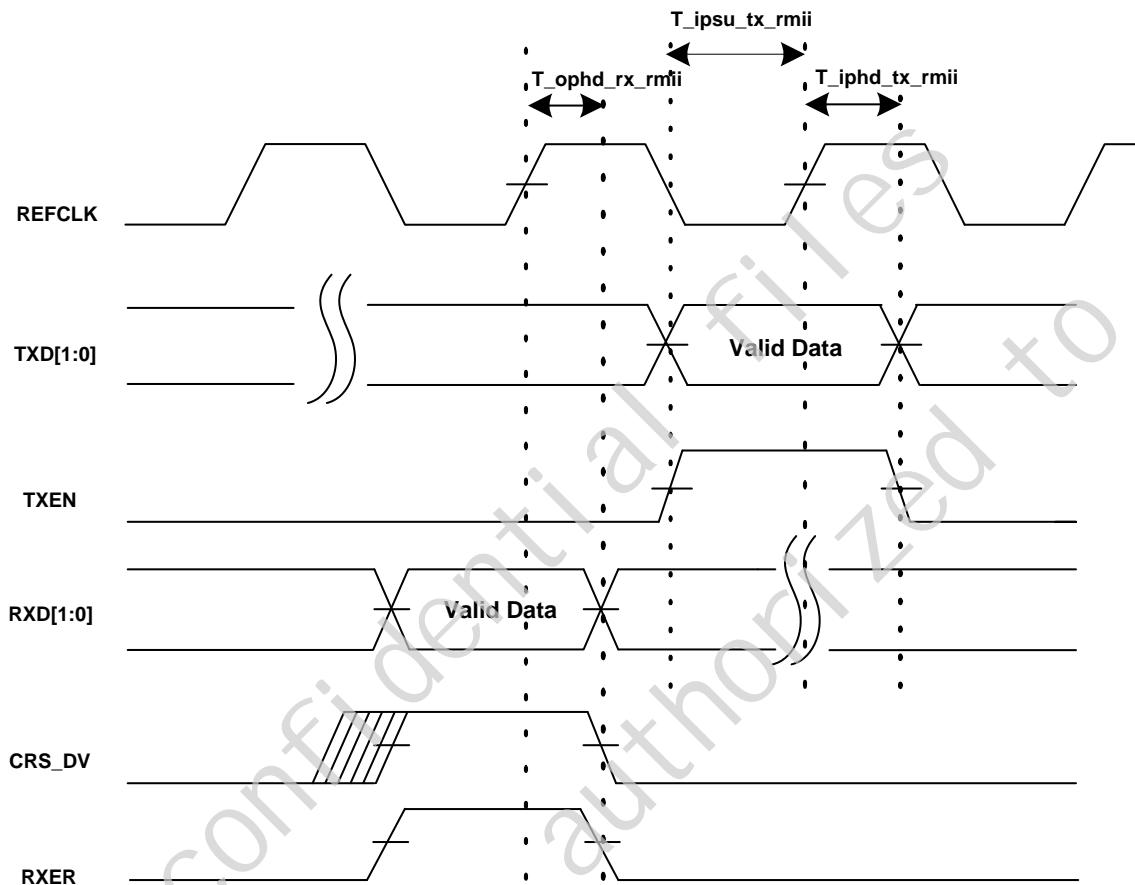
**Table 110. MII Reception Cycle Timing**

Symbol	Description	Minimum	Typical	Maximum	Unit
$t_1, t_2$	RXC Duty Cycle	40	50	60	%
$t_3$	RXC Period	-	40	-	ns
$t_4$	RXER, RXDV, RXD[3:0] Setup to RXC Rising Edge	10	-	-	ns
$t_5$	RXER, RXDV, RXD[3:0] Hold After RXC Rising Edge	10	-	-	ns

### 10.10.4. RMII Transmission and Reception Cycle Timing



**Figure 41. RMII Interfaces Setup, Hold Time, and Output Delay Time Definitions**



**Figure 42. RMII Transmission and Reception Cycle Timing**

**Table 111. RMII Transmission and Reception Cycle Timing**

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns

Note1: RMII TX timing can be adjusted by setting page7, register16[11:8]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

Note2: RMII RX timing can be adjusted by setting page7, register16[7:4]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

### 10.10.5. RGMII Timing Modes

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation.

Figure 43 shows the effect of adding an additional delay to TXC by PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.

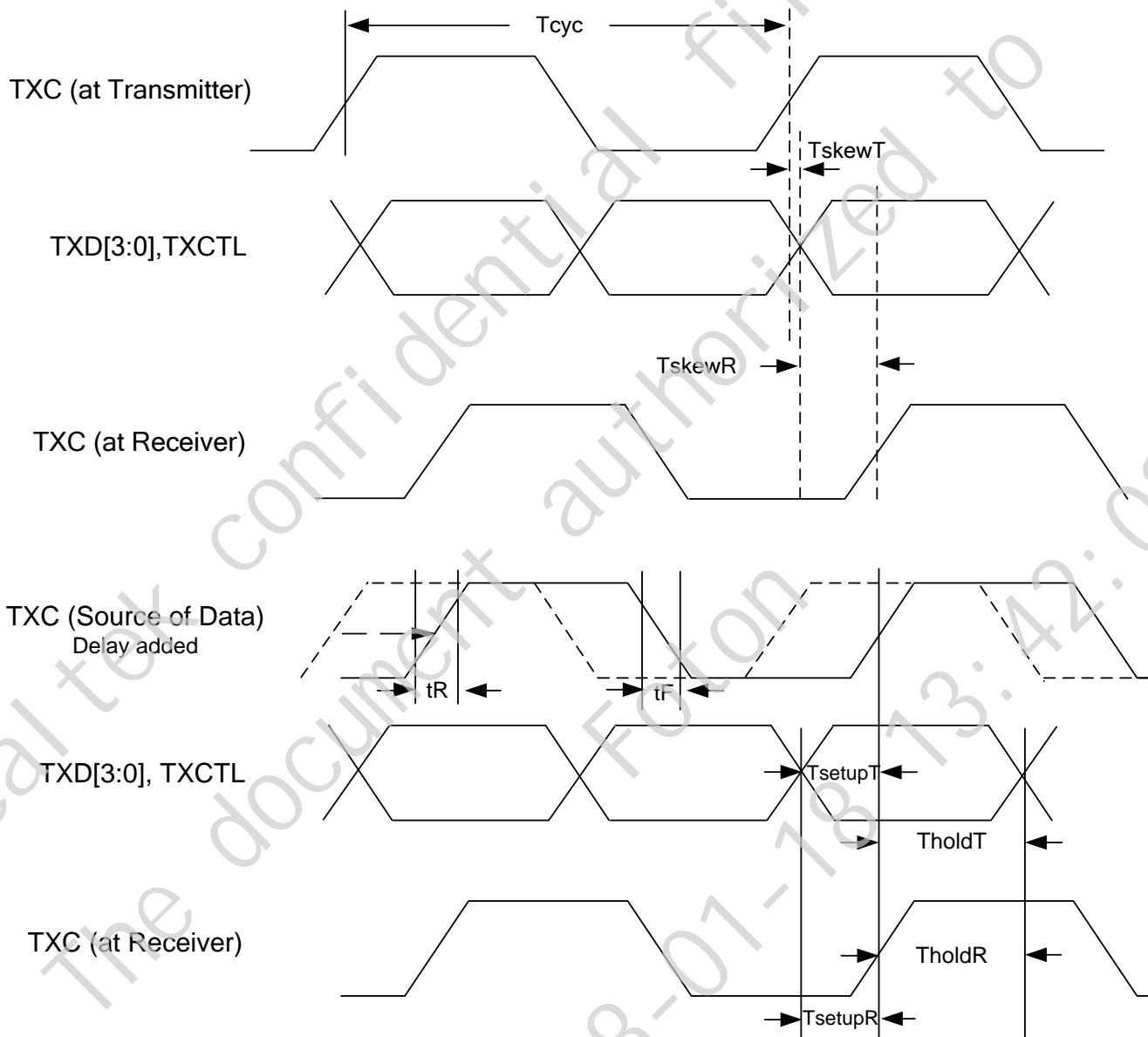
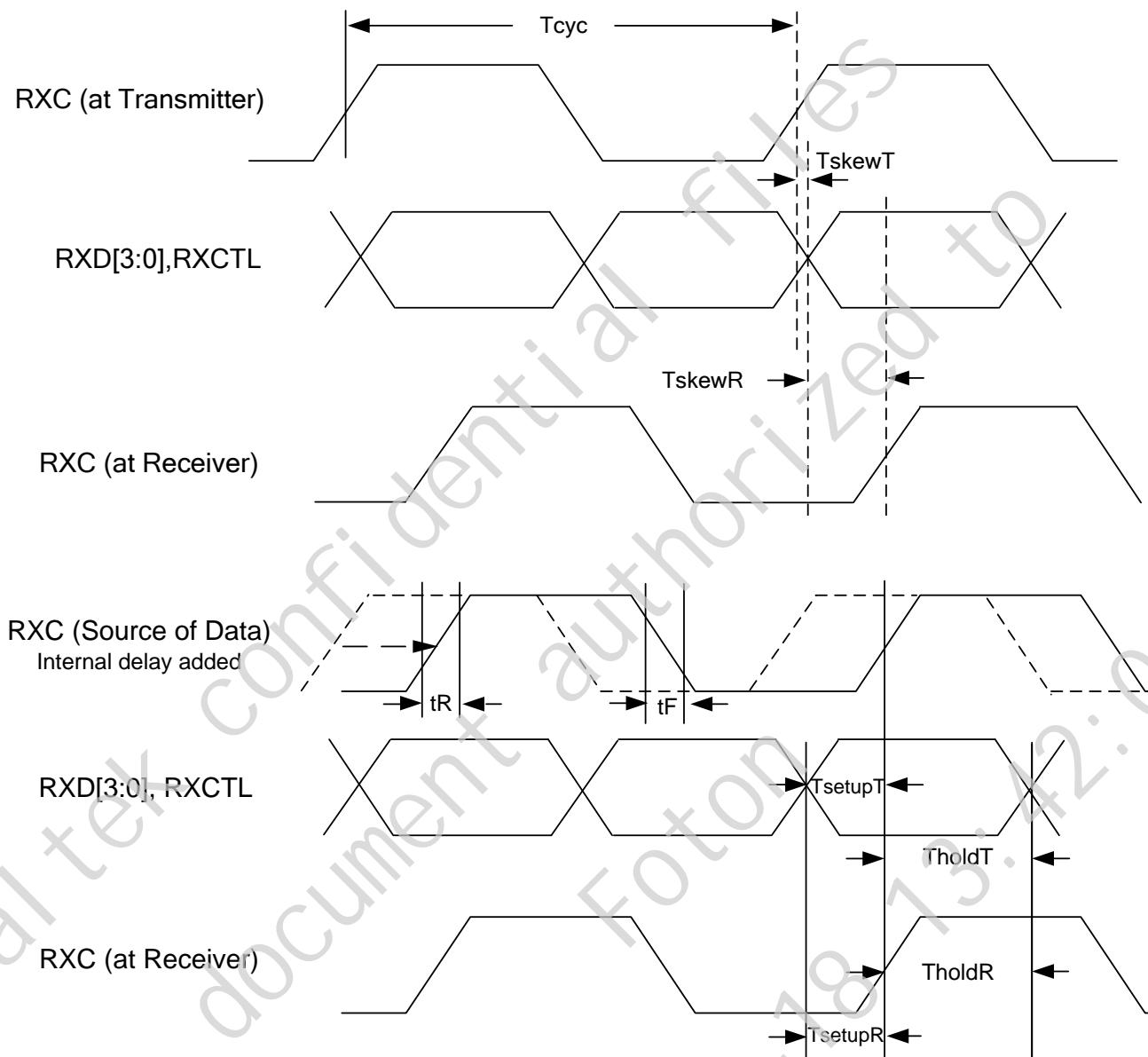


Figure 43. RGMII Timing Modes (For TXC)

Figure 44 shows the effect of adding an additional delay to RXC by PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.



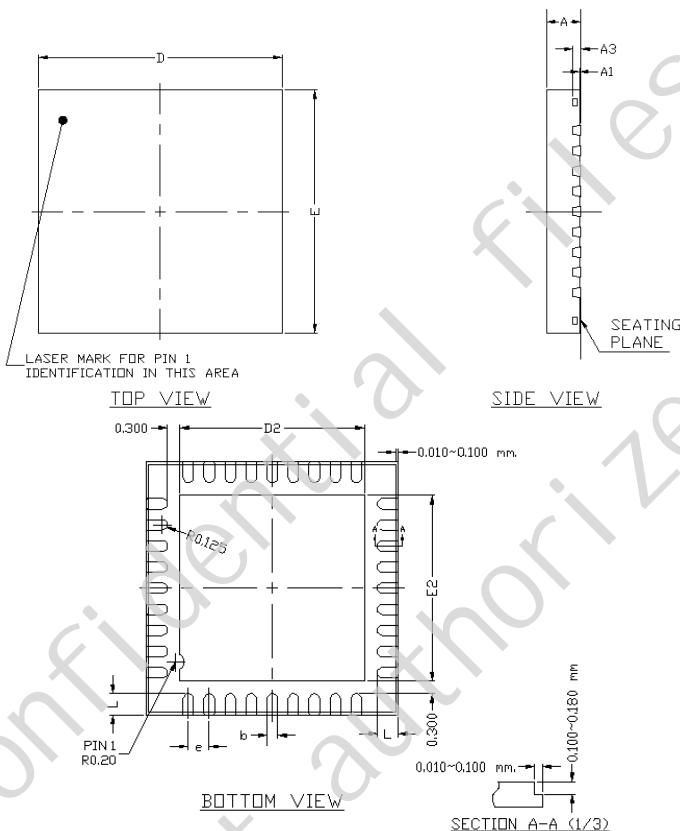
**Figure 44. RGMII Timing Modes (For RXC)**

**Table 112. RGMII Timing Parameters**

Symbol	Description	Min	Typical	Max	Units
Tcyc *	Clock Cycle Duration (100Mbps)	36	40	44	ns
Duty_T	Duty Cycle	40	50	60	%
tR	TXC/RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	TXC/RXC Fall Time (20%~80%)	-	-	0.75	ns
TsetupT	Data to Clock Output Setup Time at transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TholdT	Clock to Data Output Hold Time at transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TsetupR	Data to Clock Input Setup Time at receiver (with delay integrated at transmitter)	1.0	2	-	ns
TholdR	Clock to Data Input Hold Time at receiver (with delay integrated at transmitter)	1.0	2	-	ns
TskewT **	Data to Clock Output Skew Time at transmitter (without delay integrated)	-0.5	0		ns
TskewR **	Data to Clock Input Skew Time at receiver (with PCB delay integrated) This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal.	1	1.8		ns

\*Note: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

## 11. Mechanical Dimensions



### 11.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.00 BSC			0.236 BSC		
D2	4.30	4.40	4.50	0.169	0.173	0.177
E2	3.95	4.05	4.15	0.156	0.159	0.163
e	0.50 BSC			0.020 BSC		
L	0.50	0.55	0.60	0.020	0.022	0.024

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

## 12. Ordering Information

Table 113. Ordering Information

Part Number	Package	Status
RTL9000AA-VC	36-Pin QFN with 'Green' Package	ES
<b>MSL (Moisture Sensitivity Level)</b>		Level 3
<b>Weight</b>		0.12g

---

**Realtek Semiconductor Corp.****Headquarters**

No. 2, Innovation Road II

Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211 Fax: +886-3-577-6047

[www.realtek.com](http://www.realtek.com)