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RTL8411-CG

PCI EXPRESS 10/100/1000M ETHERNET CONTROLLER WITH INTEGRATED 1-LUN CARD READER CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/04/20	First Release.
1.1	2011/07/13	Revised Figure 1 Pin Assignments, page 5. Revised Table 5 Clock, page 7. Revised Table 23 Oscillator Requirements, page 29. Revised Table 25 DC Characteristics, page 30.
1.2	2011/08/09	Revised Table 8 Card Reader, page 8. Revised section 6.2.5 Customizable LED Configuration, page 13. Added section 6.2.6 LED Blinking Frequency Control, page 15. Added section 6.13 XTAL-Less Wake-On-LAN, page 24. Revised section 9.8.4 Auxiliary Signal Timing Parameters, page 38.
1.3	2011/12/01	Revised Table 19 Power Sequence Parameter, page 25.
1.4	2012/03/02	Revised section 6.13 XTAL-Less Wake-On-LAN, page 24. Revised Table 19 Power Sequence Parameter, page 25. Added section 7.2 Power Sequence Parameters, page 26. Revised Table 25 DC Characteristics, page 30.

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1. General Description

The Realtek RTL8411-CG 10/100/1000M Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded One-Time-Programmable (OTP) memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8411 offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization and timing recovery are implemented to provide robust transmission and reception capability at high speeds.

The RTL8411 supports the PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also features a built-in PCI Express 1.1 compliant card reader controller; integrating a PCI Express Transceiver, switching regulator, LDO regulator and memory card access units into a single ship.

The RTL8411 supports Memory Stick, Memory Stick Pro, Memory Stick PRO-HG Duo, Secure Digital, Secure Digital eXtended Capacity, Multi-Media Card, and xD-Picture Card in a 1-LUN (Logical Unit Number) configuration (which means only one of these memory cards can be inserted into the RTL8411 system at one time). The device also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8411 features embedded One-Time-Programmable (OTP) memory to replace the external EEPROM (TWSI).

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, AMD Magic Packet and Microsoft® Wake-Up frame are supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8411.

The RTL8411 supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious Wake-Up and further reduce power consumption. The RTL8411 can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8411 supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8411 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8411 is fully compliant with Microsoft® NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8411 supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput. Header Data Split (HDS) support enables faster processing of TCP/IP networking protocols for improved network performance.

Virtual Machine Queue (VMQ) is a hardware virtualization technology for the efficient transfer of network traffic to a virtualized host OS. VMQ uses hardware packets filtering to deliver packet data from an external virtual machine network directly to virtual machines, which reduces the overhead of routing packets and copying them from the management operating system to the virtual machine.

Note: RTL8411 Virtual Machine Queue (VMQ) is only functional in computers running Windows Server 2008 R2 with the Hyper-V server role installed.

The device also features interconnect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI, and also maintains software compatibility with existing PCI infrastructure. The device embeds an adaptive equalizer in the PCIe PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 20 centimeters.

The RTL8411 is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

- Integrated 10/100/1000M transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-On-LAN support
- XTAL-Less Wake-On-LAN
- Customizable LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
- Support EMAC-393 ECMA ProxZzzy Standard for sleeping hosts
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports jumbo frame to 9K bytes
- Fully complies with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- Embedded OTP memory can replace the external EEPROM
- Transmit/Receive on-chip buffer support
- Supports IEEE 802.3az-2010 (EEE)
- Supports power down/link down power saving/PHY disable mode/LAN disable mode
- Built-in switching regulator
- Built-in LDO regulator
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports Quad Core Receive-Side Scaling (RSS), Header Data Split (HDS), and Virtual Machine Queue (VMQ)
- 64-pin QFN package (Green package)
- Embeds an adaptive equalizer in PCI Express PHY (PCB traces to reach up to 20cm)
- Supports 1-Lane 2.5Gbps PCI Express Bus

- Supports memory card interfaces
  - Secure Digital (SD v3.0, UHS mode), SDHC (up to 32GB), SDXC (up to 2TB), Mini-SD, Micro-SD (T-flash)
  - MultiMediaCard (MMC v4.2), RS-MMC, Mobile-MMC, MMC-micro, and MMC-plus
  - Memory Stick (MS v1.43), Memory Stick PRO (MS-PRO v1.03), MS Duo, MS-PRO Duo, Micro-MS (M2), MS PRO-HG Duo v1.01 8-bit mode, and MSXC (up to 2TB)
  - xD-Picture Card (xD v1.2) including Type M+, Type M, and Type H
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function
- On chip MOSFET with 800mA capability for direct power control of all types memory cards

3. System Applications

- PCI Express 10/100/1000M Ethernet on Motherboard, Notebook, or Embedded system

4. Pin Assignments

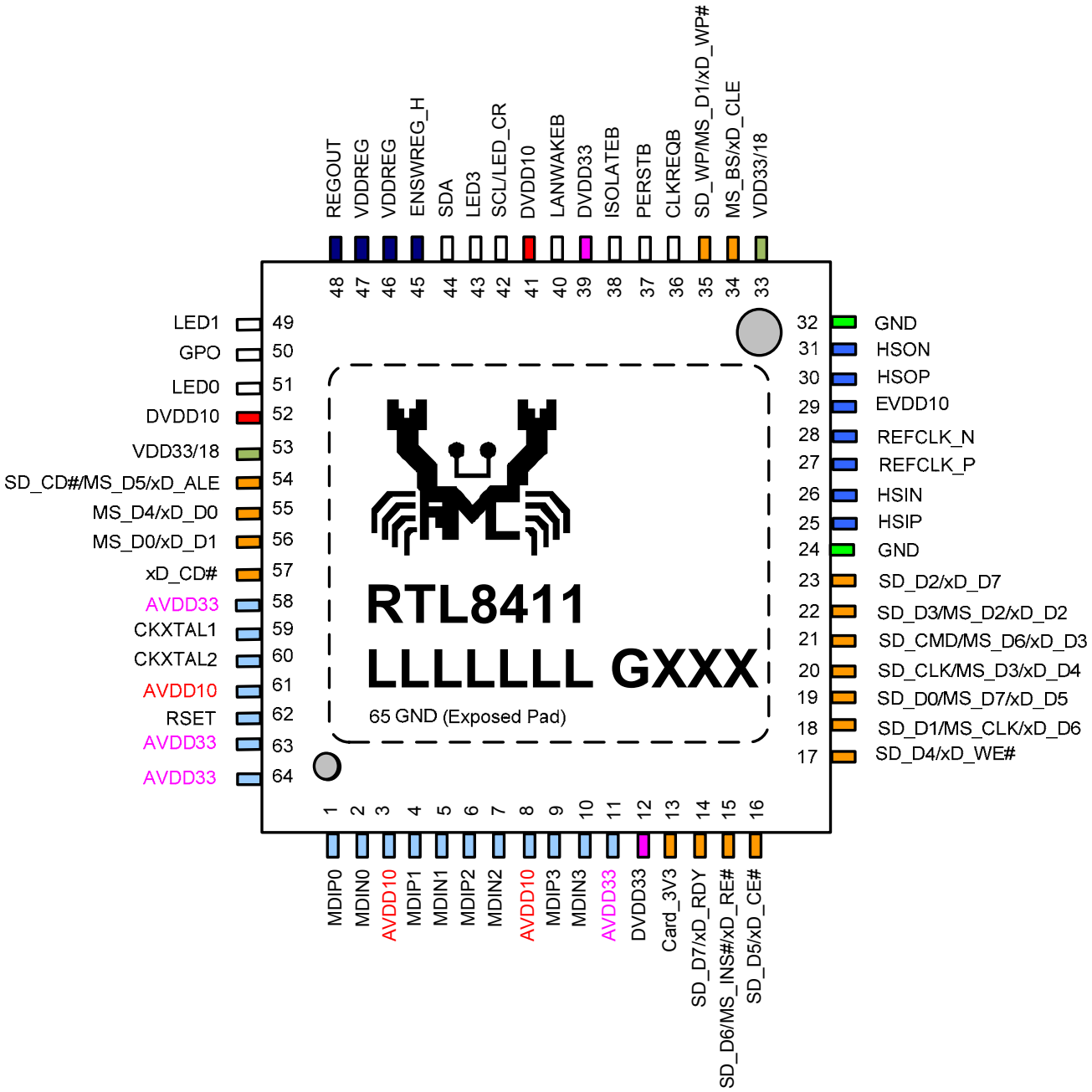


Figure 1. Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXX (Figure 1).

5. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State Bi-Directional Input/Output Pin	P:	Power

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	40	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	38	Isolate Pin: Active low. Used to isolate the RTL8411 from the PCI Express bus. The RTL8411 will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	27	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	28	
HSOP	O	30	PCI Express Transmit Differential Pair.
HSON	O	31	
HSIP	I	25	PCI Express Receive Differential Pair.
HSIN	I	26	
PERSTB	I	37	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8411 returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	36	Reference Clock Request Signal. This signal is used by the RTL8411 to request starting of the PCI Express reference clock.

5.3. EEPROM (TWSI)

Table 3. EEPROM (TWSI)

Symbol	Type	Pin No	Description
SCL/LED_CR	O	42	SCL: Clock interface for TWSI EEPROM.
SDA	IO	44	SDA: Data interface for TWSI EEPROM.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	1	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	2	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	4	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIP2	IO	6	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair.
MDIN2	IO	7	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIP3	IO	9	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair.
MDIN3	IO	10	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	59	Input of 25MHz Clock Reference.
CKXTAL2	IO	60	Input of External Clock Source. Output of 25MHz Clock Reference.

5.6. Regulator and Reference

Table 6. Regulator and Reference

Symbol	Type	Pin No	Description
REGOUT	O	48	Switching Regulator and LDO Regulator 1.0V Output.
ENSWREG_H	I	45	3.3V: Enable Switching Regulator 0V: Enable LDO Regulator
VDDREG	P	46, 47	Digital 3.3V Power Supply for Switching Regulator and LDO Regulator.
RSET	I	62	Reference. External resistor reference.

Note: See section 7, page 25 for additional switching regulator information.

5.7. LEDs

Table 7. LEDs

Symbol	Type	Pin No	Description
SCL/LED_CR	O	42	See Section 6.2.5 Customizable LED Configuration, Page 13 for Details.
LED0	O	51	
LED1	O	49	
LED3	O	43	

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the TWSI.
If there is no TWSI, the default value of the (LEDS1, LEDS0) = (1, 1).

5.8. Card Reader

Table 8. Card Reader

Symbol	Type	Pin No	Description
SD_D0/MS_D7/xD_D5	IO	19	SD Data 0 (SD_DAT0), MS_Data 7 (MS_D7), and xD Data 5 (xD_D5).
SD_D1/MS_CLK/xD_D6	IO	18	SD Data 1 (SD_DAT1), MS Clock (MS_CLK), and xD Data 6 (xD_D6).
SD_D2/xD_D7	IO	23	SD Data 2 (SD_DAT2) and xD Data 7 (xD_D7).
SD_D3/MS_D2/xD_D2	IO	22	SD Data 3 (SD_DAT3), MS_Data 2 (MS_D2), and xD Data 2 (xD_D2).
SD_D4/xD_WE#	IO	17	SD Data 4 (SD_DAT4) and xD Write Enable (xD_WE#).
SD_D5/xD_CE#	IO	16	SD Data 5 (SD_DAT5) and xD Chip Select (xD_CE#).
SD_D6/MS_INS#/xD_RE#	IO	15	SD Data 6 (SD_DAT6), MS Card Detect (MS_INS#), and xD Read Enable (xD_RE#).
SD_D7/xD_RDY	IO	14	SD Data 7 (SD_DAT7) and xD Ready Signal (xD_RDY).
SD_CLK/MS_D3/xD_D4	IO	20	SD Clock (SD_CLK), MS_Data 3 (MS_D3), and xD Data 4 (xD_D4).
SD_CMD/MS_D6/xD_D3	IO	21	SD Serial Protocol Command, and Response Signal, MS_Data 6 (MS_D6), and xD Data 3 (xD_D3).
SD_WP/MS_D1/xD_WP#	IO	35	SD Write Protect (SD_WP), MS_Data 1 (MS_D1), and xD Write Protect (xD_WP#).

Symbol	Type	Pin No	Description
SD_CD#/MS_D5/xD_ALE	IO	54	SD Card Detect (SD_CD#), MS_Data 5 (MS_D5), and xD Address Latch Enable (xD_ALE).
MS_BS/xD_CLE	IO	34	MS_BS and xD Command Latch Enable (xD_CLE).
MS_D4/xD_D0	IO	55	MS_Data 4 (MS_D4) and xD Data 0 (xD_D0).
MS_D0/xD_D1	IO	56	MS_Data 0 (MS_D0) and xD Data 1 (xD_D1).
xD_CD#	I	57	xD Card Detect (xD_CD).

Note: MMC uses 4 pins more than SD 3.0 (SD_D4~D7).

5.9. GPO Pin

Table 9. GPO Pin

Symbol	Type	Pin No	Description
GPO	IO	50	General Purpose IO Pin (Used for Power Saving Feature).

5.10. Power and Ground

Table 10. Power and Ground

Symbol	Type	Pin No	Description
DVDD33	P	12, 39	Digital 3.3V Power Supply.
DVDD10	P	41, 52	Digital 1.0V Power Supply.
AVDD33	P	11, 58, 63, 64	Analog 3.3V Power Supply.
AVDD10	P	3, 8, 61	Analog 1.0V Power Supply.
EVDD10	P	29	Analog 1.0V Power Supply.
Card_3V3	P	13	3.3V Power for All Cards.
VDD33/18	P	33, 53	SD UHS Mode Power Supply.
GND	P	24, 32	Ground.
GND	P	65	Ground (Exposed Pad).

Note: Refer to the most updated schematic circuit for correct configuration.

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8411 complies with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8411 supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal is also supported.

6.1.1. PCI Express Transmitter

The RTL8411's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8411's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8411's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8411 supports three LED signals in four different configurable operation modes. The SCL pin can be shared with the LED_CR pin for card reader function. The following sections describe the various Ethernet Controller LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. RX LED

In 10/100/1000M mode, blinking of the RX LED indicates that receive activity is occurring.

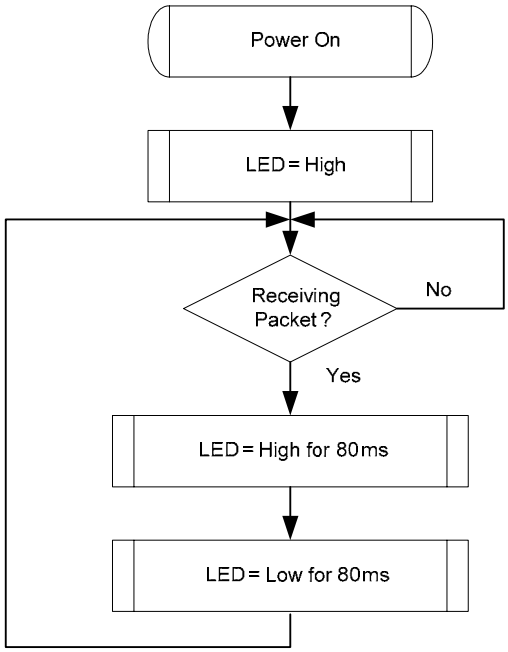


Figure 2. RX LED

6.2.3. TX LED

In 10/100/1000M mode, blinking of the TX LED indicates that transmit activity is occurring.

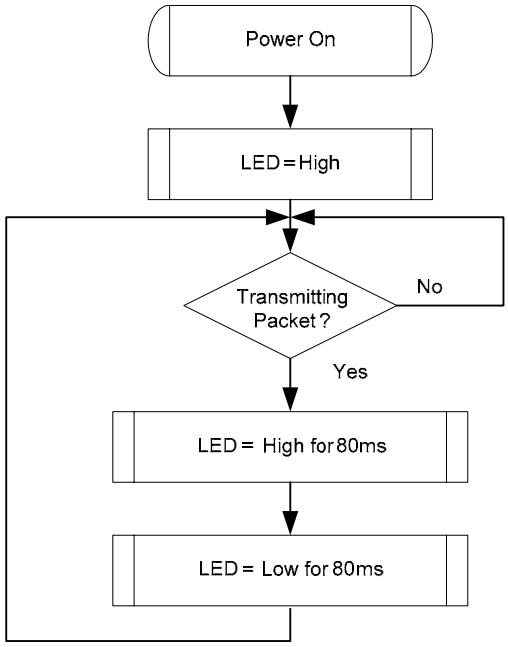


Figure 3. TX LED

6.2.4. TX/RX LED

In 10/100/1000M mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

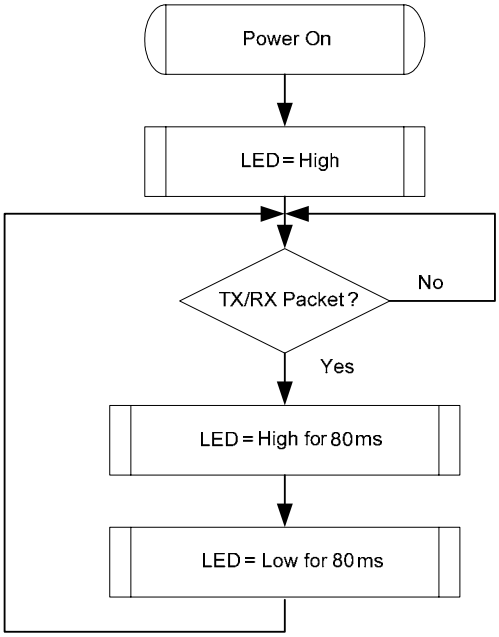


Figure 4. TX/RX LED

6.2.5. Customizable LED Configuration

The RTL8411 supports customizable LED operation modes via IO register offset 18h~19h. Table 11 describes the different LED actions.

Table 11. LED Select (IO Register Offset 18h~19h)

Bit	Symbol	RW	Description
15:12	Feature	RW	LED Feature Control
11:8	LEDSEL3	RW	LED Select for PINLED3
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 3: On only in 1000M mode, with blinking during TX/RX

Table 12. Customized LEDs

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 3	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

Note: There are two special modes:
LED OFF Mode: Set all bits to 0. All LED pin output become floating (power saving).
Fixed LED Mode: Set Option 1 LED table Mode: LED0=LED1=LED3=1 or 2 (see Table 13).

Table 13. Fixed LED Mode

Bit31~Bit0 Value	LED0	LED1	LED3
1XXX 0001 0001 0001	ACT	LINK	Full Duplex + Collision
1XXX 0010 0010 0010	Transmit	LINK	Receive

Note: 'X' indicates 'irrelevant'.

Table 14. LED Feature Control-1

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	LED3 Low Active	Indicates Option 1 of Table 16 is selected
1	LED0 High Active	LED1 High Active	LED3 High Active	Indicates Option 2 of Table 16 is selected

Table 15. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 16): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 16): Selected Speed LINK+ All Speed ACT

Table 16. LED Option 1 & Option 2 Settings

Link Bit			Active Bit	Description		
10	100	1000		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	LED Off		
0	0	0	1	-	Act^{10}+Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
0	0	1	0	$Link^{1000}$	-	-
0	0	1	1	$Link^{1000}$	Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
0	1	0	0	$Link^{100}$	-	-
0	1	0	1	$Link^{100}$	Act^{100}	Act^{10}+Act^{100}+Act^{1000}
0	1	1	0	$Link^{100}$+$Link^{1000}$	-	-
0	1	1	1	$Link^{100}$+$Link^{1000}$	Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
1	0	0	0	$Link^{10}$	-	-
1	0	0	1	$Link^{10}$	Act^{10}	Act^{10}+Act^{100}+Act^{1000}
1	0	1	0	$Link^{10}$+$Link^{1000}$	-	-
1	0	1	1	$Link^{10}$+$Link^{1000}$	Act^{10}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
1	1	0	0	$Link^{10}$+$Link^{100}$	-	-
1	1	0	1	$Link^{10}$+$Link^{100}$	Act^{10}+Act^{100}	Act^{10}+Act^{100}+Act^{1000}
1	1	1	0	$Link^{10}$+$Link^{100}$+$Link^{1000}$	-	-
1	1	1	1	$Link^{10}$+$Link^{100}$+$Link^{1000}$	Act^{10}+Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}

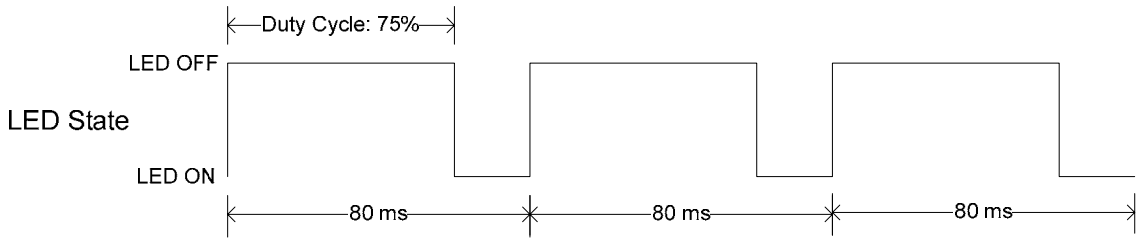
Note:
Act^{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act^{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act^{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
$Link^{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link^{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link^{1000}$ = LED lit when Ethernet connection established at 1000Mbps.

6.2.6. LED Blinking Frequency Control

The RTL8411 supports LED blinking frequency control via IO register offset 1Ah to control user's LED blinking frequency and duty cycle (see Table 17). If the IO offset 0x1A is 0x0B (00001011b), the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 5.

Table 17. LED Blinking Frequency Control (IO Offset 1Ah)

Bit	RW	Description
3:2	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
1:0	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assume the LED is in low active.

Figure 5. LED Blinking Frequency Example

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8411 operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), and CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8411's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3.3. Link Down Power Saving Mode

The RTL8411 implements link-down power saving, greatly cutting power consumption when the network cable is disconnected. The RTL8411 automatically enters link down power saving mode ten seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6.3.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.4. EEPROM Interface

The RTL8411 can use internal eFUSE memory or an external EEPROM. The Two-Wire Serial Interface (TWSI) EEPROM is a 16K bit EEPROM. The interface permits the RTL8411 to read from, and write data to, an external serial EEPROM device.

Values in the internal eFUSE memory or external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8411 will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8411 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the PCI VPD (Vital Product Data). The TWSI EEPROM interface consists of SCL and SDA.

The correct EEPROM (i.e., TWSI) must be used in order to ensure proper LAN function.

Table 18. TWSI EEPROM Interface

EEPROM	Description
SCL	Serial Clock.
SDA	Serial Data I/O.

6.5. Power Management

The RTL8411 is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8411 can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8411 is in power down mode (D1 ~ D3):

- The RX state machine is stopped. The RTL8411 monitors the network for Wake-Up events such as a Magic Packet and Wake-Up Frame in order to wake up the system. When in power down mode, the RTL8411 will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8411.
- Transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held.
- After being restored to D0 state, the RTL8411 transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 FF, then PCI PMC = C3 FF)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 FF, then PCI PMC = 03 7E)

In the above case, if Wake-Up support is desired when main power is off, we suggest that the EEPROM PMC be set to C3 FF (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 7F, then PCI PMC = C3 7F)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 7F, then PCI PMC = 03 7E)

In the above case, if Wake-Up support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 7E.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8411, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8411 adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding Wake-Up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8411, e.g., a broadcast, multicast, or unicast address to the current RTL8411 adapter.
- The received Wake-Up Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8411 is configured to allow direct packet Wake-Up, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8411 supports eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding Wake-Up method (message, beacon, or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8411 may assert the corresponding Wake-Up method (message, beacon, or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wake-Up Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8411 to stop asserting the corresponding Wake-Up method (message, beacon, or LANWAKEB) (if enabled).

When the RTL8411 is in power down mode, e.g., D1~D3, the IO and MEM accesses to the RTL8411 are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.6. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8411's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the TWSI has completed or not.

Write VPD register (write data to the EEPROM):

Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8411, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register (read data from the EEPROM):

Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8411, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note 1: Refer to the PCI 2.3 Specifications for further information.

Note 2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note 3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.

Note 4: The VPD function of the RTL8411 is designed to be able to access the full range of the TWSI.

6.7. Receive-Side Scaling (RSS)

The RTL8411 is compliant with the Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi-CPU platforms.

6.7.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8411 to store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port, and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port, and the destination TCP port.
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address

Hash Bits

Hash bits are used to index the hash result into the indirection table.

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.7.2. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It maintains a network presence for a sleeping higher power host. Protocol offload prevents spurious Wake-Up and further reduces power consumption. It maintains connectivity while hosts are asleep, including receiving requests from other nodes on the network, ignoring packets, generating packets while in the sleep state (e.g., the Ethernet Controller will generate ARP responses if the same MAC and IPv4 address are provided in the configuration data), and intelligently waking up host systems. The RTL8411 supports the ECMA (European Computer Manufacturers Association) specification including proxy configuration and management, IPv4 ARP, IPv6 NDP, and Wake-Up packets. The RTL8411 also supports optional ECMA items such as QoS tagged packets and duplicate address detection.

6.7.3. RSS Operation

After the parameters are set, the RTL8411 will start hash calculation on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8411 uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

6.8. Header Data Split (HDS)

Header Data Split (HDS) was introduced in Microsoft Windows Server 2008. This feature allows NDIS miniport drivers to pass packet information up the networking stack so that the header portion of the packet and the data payload portion of the packet are mapped into two or more Memory Descriptor Lists (MDLs). The headers and the remainder of the payload are located in different areas in virtual memory rather than in one contiguous virtual memory block. This split of the header portion and the data portion of the packets into multiple MDLs increases system performance through intelligent cache management.

6.9. Virtual Machine Queue (VMQ)

Many NICs can support more than one unicast MAC address for a network server. Therefore, the NIC can receive network data frames with a destination MAC address that matches any of the unicast MAC addresses that are set on the NIC hardware, without being in promiscuous mode. Such hardware can allocate a receive queue for each MAC address and route incoming frames with a matching MAC address to the queue. This feature, coupled with the ability to allocate receive buffers for each queue from the memory address space that is assigned to each virtual machine, are the primary capabilities that are required for Virtual Machine Queue (VMQ) support.

A VMQ capable NIC can use DMA to transfer all incoming frames that should be routed to a receive queue to the receive buffers that are allocated for that queue. The miniport driver can indicate all of the frames that are in a receive queue in one receive indication call.

VMQ provides the following features:

- Improves network throughput by distributing processing of network traffic for multiple virtual machines (VMs) among multiple processors.
- Reduces CPU utilization by offloading receive packet filtering to NIC hardware.
- Avoids network data copy by using DMA to transfer data directly to VM memory.

6.10. Energy Efficient Ethernet (EEE)

The RTL8411 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.11. PHY Disable Mode

The RTL8411 can power down the PHY using board-level control signals. Refer to the LAN/PHY Disable Application Note for implementation details.

6.12. LAN Disable Mode

The Ethernet controller can be disabled via LAN disable mode. When a PCI-E reset is de-asserted, the RTL8411 utilizes the GPO signal to disable or enable the Ethernet Controller function. The GPHY does not link and the LAN disappears under this mode. Refer to the LAN/PHY Disable Application Note for details.

6.13. XTAL-Less Wake-On-LAN

The RTL8411 supports board level design with an external 25MHz clock source instead of the 25MHz Crystal.

The external clock source may stop generating 25MHz clock when in suspend mode (S3/S4/S5). To support the Wake-On-LAN function without an external 25MHz clock source, the RTL8411 will automatically change its source clock from the external 25MHz clock to an internal self-oscillating auxiliary clock when it enters suspend mode.

Note 1: The auxiliary clock can establish only a 10Mbps link when in suspend mode and using the internal clock.

Note 2: The auxiliary clock does not support ARP/NS offload and ECMA ProxZzzy when in suspend mode and using the internal clock.

Note 3: Does not support XTAL-less pre-boot.

7. Switching Regulator

The RTL8411 incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.0V output pin (REGOUT) must be connected only to AVDD10, DVDD10, and EVDD10 (do not provide this power source to other devices).

Note: Refer to the separate RTL8411 Layout Guide for details.

7.1. Power Sequence

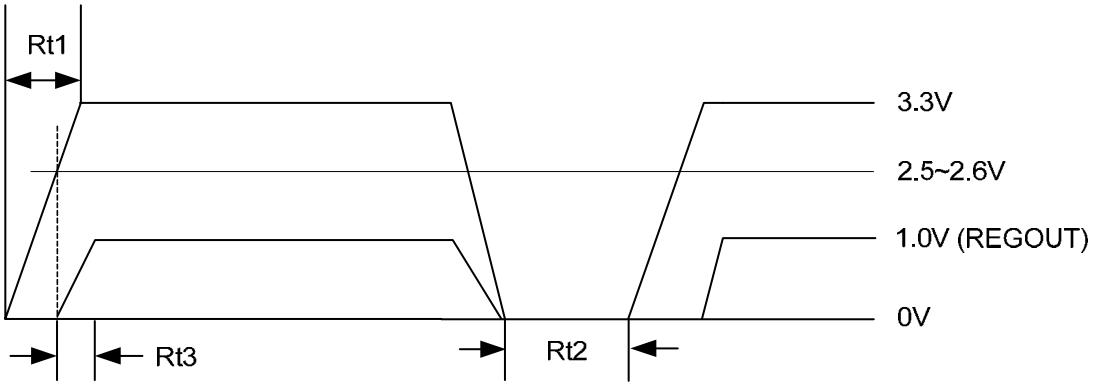


Figure 6. Power Sequence

Table 19. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

7.2. Power Sequence Parameters

The RTL8411 does not support fast 3.3V rising under normal circumstance. The 3.3V rise time must be controlled over 0.5ms.

Rise Time > 0.5ms

No action to take.

Rise Time 0.1ms~0.5ms

If the rise time is between 0.1ms and 0.5ms, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8411 so as to be safely under the system's 3.3V OCP threshold.

For example:

- Assume customer supply power rise time of the RTL8411 is 0.374ms
- The system 3.3V OCP is 9A
- The inrush current of other 3.3V devices is 5.64A

The inrush current to the RTL8411 must be less than 1.12A, otherwise an unanticipated system OCP may be triggered. It can be expressed in the following formula:

Inrush current to the RTL8411 < (System 3.3V OCP - inrush current of other 3.3V devices) / 3

Rise Time < 0.1ms

If the rise time is less than 0.1ms, there is risk of an unanticipated ESD trigger event, which may cause permanent damage to the RTL8411.

If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.0V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

8. LDO Regulator

The RTL8411 incorporates a linear Low-Dropout (LDO) regulator that features high power supply ripple rejection and low output noise. The RTL8411 embedded LDO regulator does not require power inductors on the PCB; only a 1.0V output capacitor between its 1.0V output and analog ground for phase compensation, which saves cost and PCB real estate. Use a X5R low-ESR ceramic capacitor, with a capacitance of at least 1µF, to enhance output voltage stability.

The output capacitors (and bypass capacitors) should be placed as close as possible to the power pins (AVDD10, DVDD10, EVDD10) for adequate filtering.

Note that with regard to voltage conversion efficiency, LDO is inferior to a switching regulator. This balance between cost, size, and efficiency should be taken into consideration when choosing the regulator type.

Note 1: The embedded LDO is designed for RTL8411 internal use only. Do not provide this power source to other devices.

Note 2: Refer to the separate RTL8411 Layout Guide for details.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 20. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33, CARD_3V3, DVDD33	Supply Voltage 3.3V	-0.3	3.6	V
AVDD10, DVDD10, EVDD10	Supply Voltage 1.0V	-0.3	1.2	V
3.3V DC Input 3.3V DC Output	Input Voltage Output Voltage	-0.3	3.6	V
1.0V DC Input 1.0V DC Output	Input Voltage Output Voltage	-0.3	1.2	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 21. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	AVDD33, CARD_3V3, DVDD33	3.14	3.3	3.46	V
	AVDD10, DVDD10, EVDD10	0.95	1.0	1.05	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.3. Crystal Requirements

Table 22. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
Jitter	Broadband Peak-to-Peak Jitter[2]	-	-	200	ps
DL	Drive Level.	-	-	0.3	mW

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

9.4. Oscillator Requirements

Table 23. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[2]	-	-	-	200	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

9.5. Environmental Characteristics

Table 24. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

9.6. DC Characteristics

Table 25. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
AVDD33, CARD_3V3, DVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
AVDD10, DVDD10, EVDD10	1.0V Supply Mean Voltage	-	0.95	1.0	1.05	V
Voh	Minimum High Level Output Voltage	Ioh = -4mA	0.9*VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	-	0.1*VDD33	V
Vih	Minimum High Level Input Voltage	-	2.0	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc33 (See Note 3)	Maximum Operating Supply Current from 3.3V	At 1Gbps with heavy network traffic and with Card Reader R/W operation	-	1400	-	mA
Icc10	Maximum Operating Supply Current from 1.0V	At 1Gbps with heavy network traffic and with Card Reader R/W operation	-	300	-	mA

Note 1: Refer to the latest schematic circuit for correct configuration.

Note 2: All Supply Mean Voltage power noise <±5% of Mean Voltage.

Note 3: When calculating the typical value of Icc33, the maximum current consumption of 800mA for an SD card operating in UHS-104 mode is used. Refer to 'SD Specifications Part 1 Physical Layer Specification', V3.01, Feb. 18, 2010.

9.7. AC Characteristics

9.7.1. Serial EEPROM Interface Timing

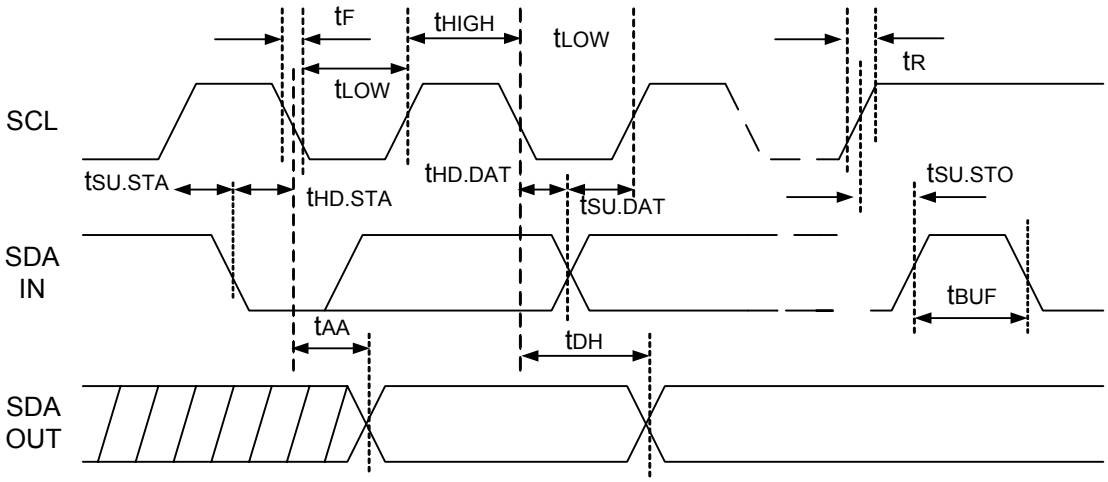


Figure 7. Serial EEPROM Interface Timing-1

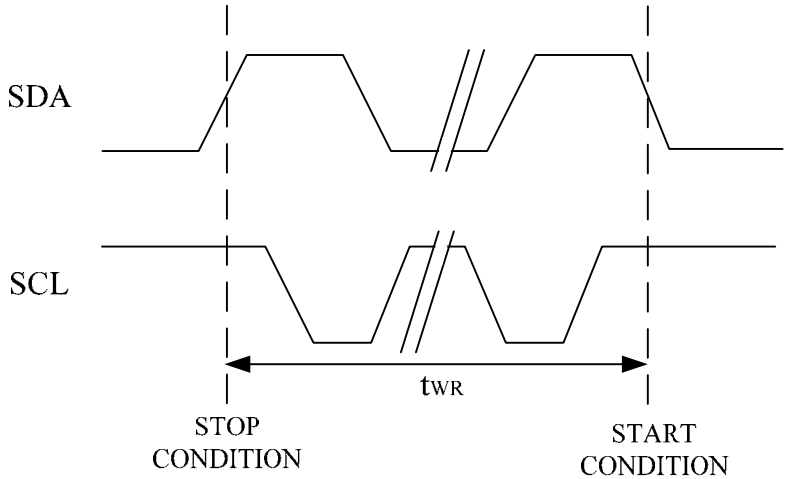


Figure 8. Serial EEPROM Interface Timing-2

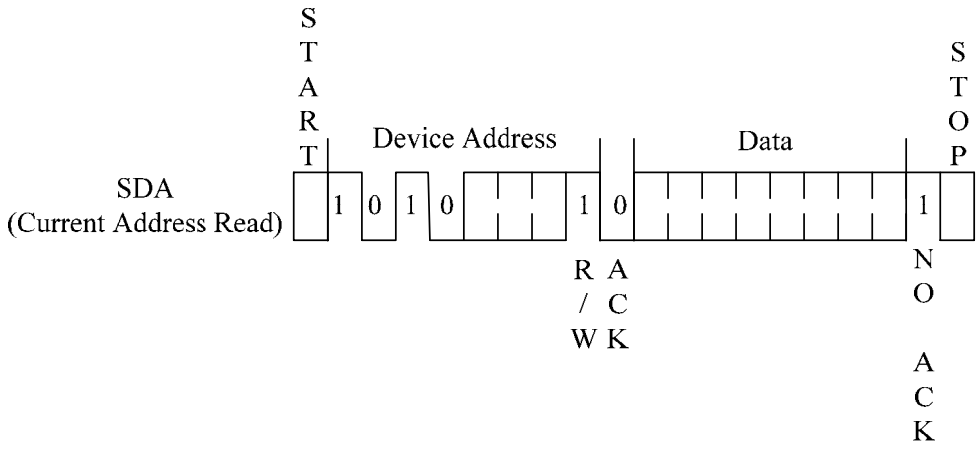


Figure 9. Serial EEPROM Interface Timing-3

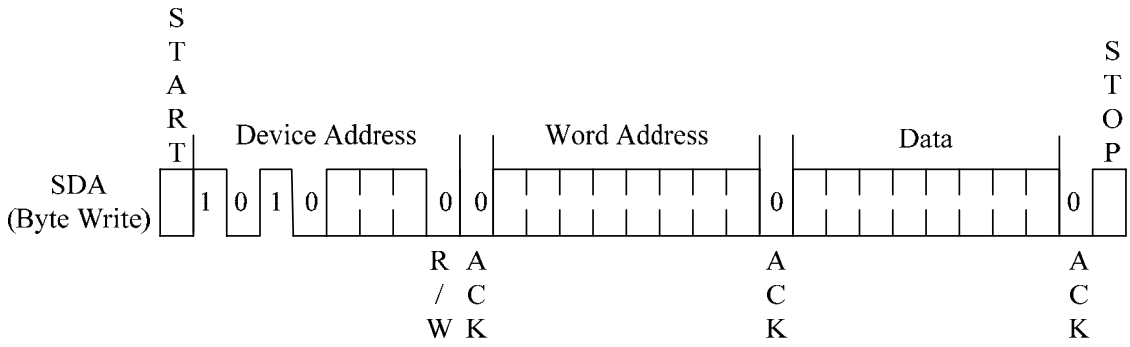


Figure 10. Serial EEPROM Interface Timing-4

Table 26. EEPROM Access Timing Parameters

Symbol	Parameter	1.8V		2.5V/5.0V		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	Clock Pulse Width Low	1.3	-	0.4	-	µs
t_{HIGH}	Clock Pulse Width High	0.6	-	0.4	-	µs
t_{AA}	Clock Low to DO Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus	1.3	-	0.5	-	µs
$t_{HD.STA}$	Start Hold Time	0.6	-	0.25	-	µs
$t_{SU.STA}$	Start Setup Time	0.6	-	0.25	-	µs
$t_{HD.DAT}$	DI Hold Time	0	-	0	-	µs
$t_{SU.DAT}$	DI Setup Time	100	-	100	-	µs
t_R	Input Rise Time	-	0.3	-	0.3	µs
t_F	Input Fall Time	-	300	-	100	µs
$t_{SU.STO}$	Stop Setup Time	0.6	-	0.25	-	µs
t_{DH}	DO Hold Time	50	-	50	-	µs
t_{WR}	Write Cycle Time	-	5	-	5	ms

9.8. PCI Express Bus Parameters

9.8.1. Differential Transmitter Parameters

Table 27. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.05	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications after Leaving an Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note 1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note 2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The +/-300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

9.8.2. Differential Receiver Parameters

Table 28. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.05	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

9.8.3. REFCLK Parameters

Table 29. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Max Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Min Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input Min	100MHz Input Max	Units	Note
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note 1: Measurement taken from single-ended waveform.

Note 2: Measurement taken from differential waveform.

Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 14, page 37.

Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 11, page 36.

Note 5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 11, page 36.

Note 6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 13, page 36.

Note 7: Defined as the maximum instantaneous voltage including overshoot. See Figure 11, page 36.

Note 8: Defined as the minimum instantaneous voltage including undershoot. See Figure 11, page 36.

Note 9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 11, page 36.

Note 10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note 11: System board compliance measurements must use the test load card described in Figure 17 , page 38. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note 12: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range. See Figure 16, page 37.

*Note 13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note 14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 12, page 36.

Note 15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

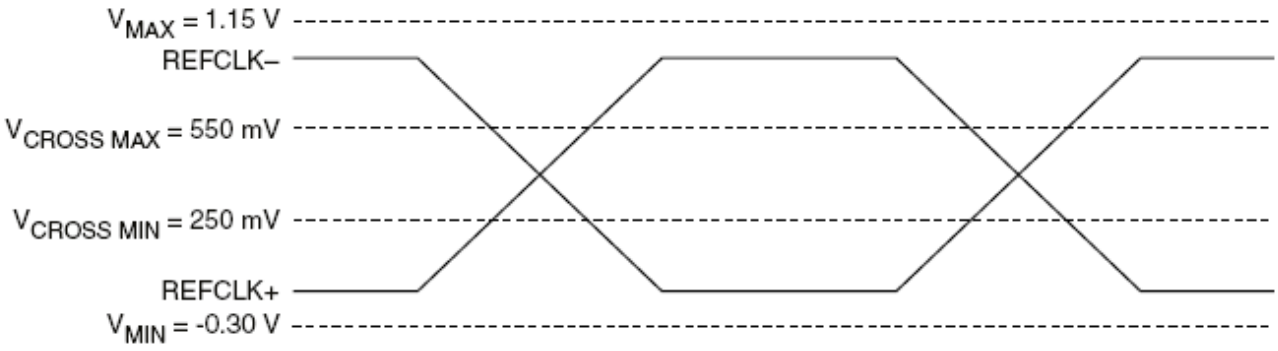


Figure 11. Single-Ended Measurement Points for Absolute Cross Point and Swing

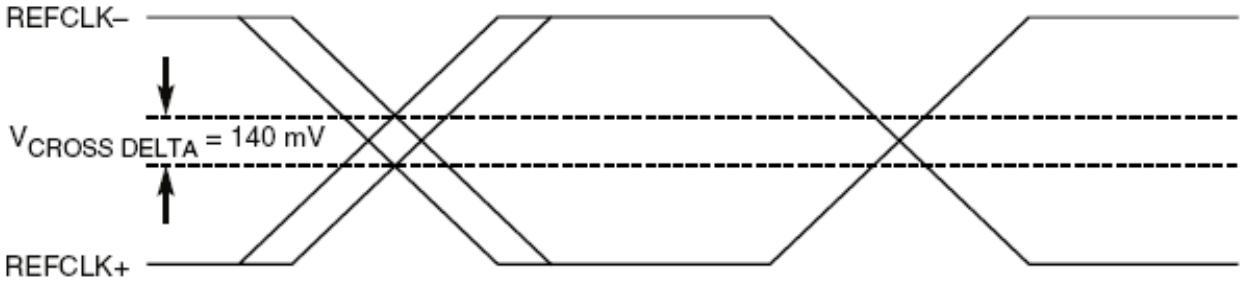


Figure 12. Single-Ended Measurement Points for Delta Cross Point

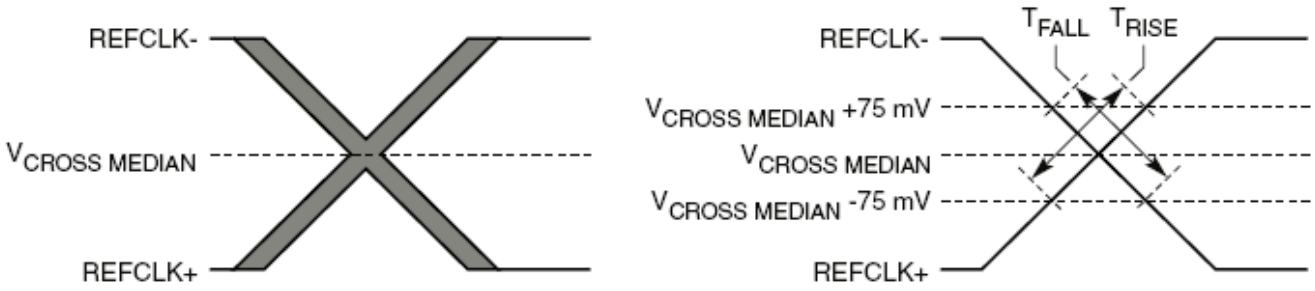


Figure 13. Single-Ended Measurement Points for Rise and Fall Time Matching

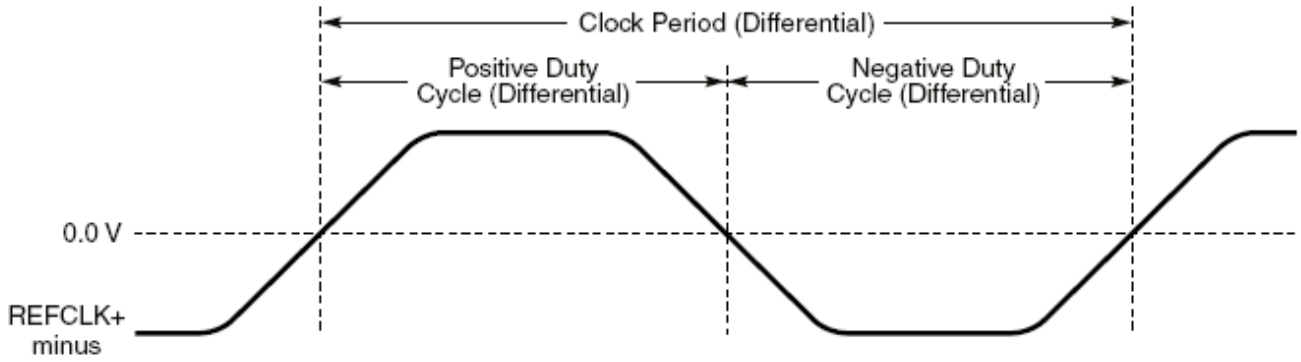


Figure 14. Differential Measurement Points for Duty Cycle and Period

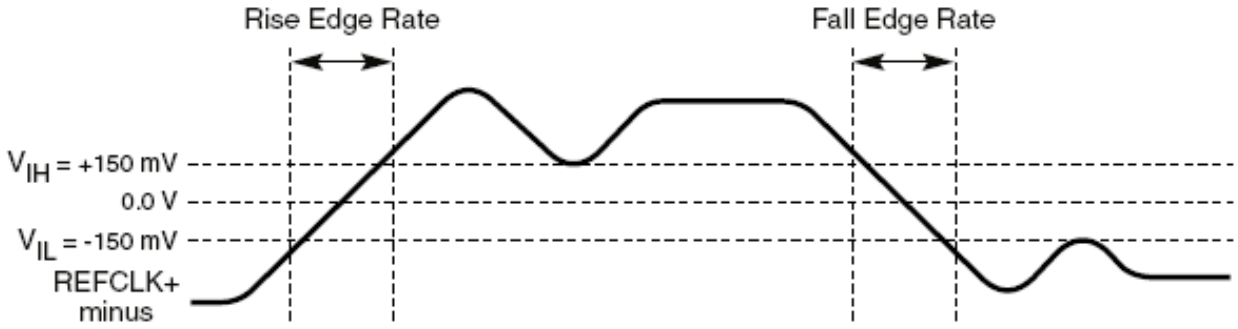


Figure 15. Differential Measurement Points for Rise and Fall Time

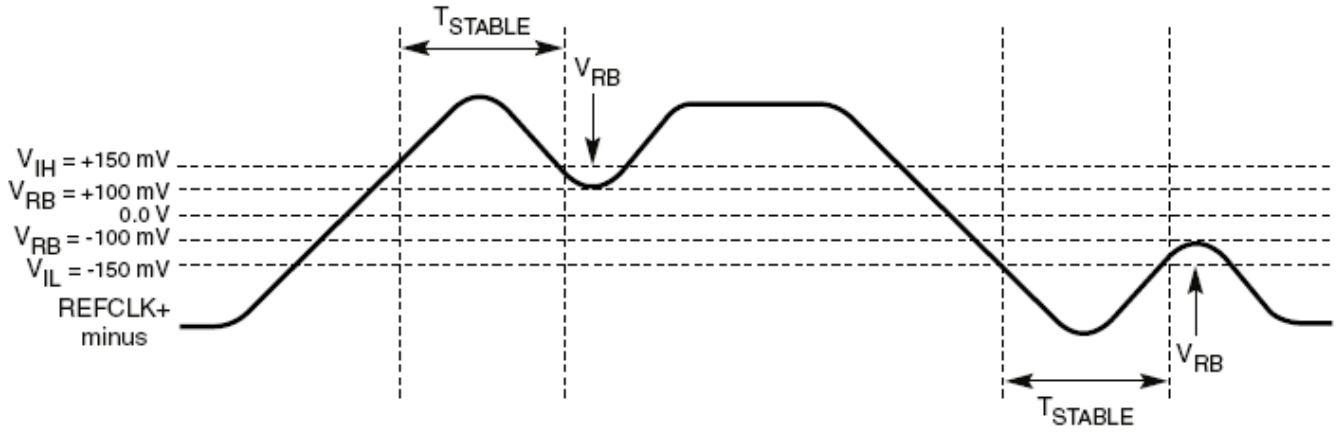


Figure 16. Differential Measurement Points for Ringback

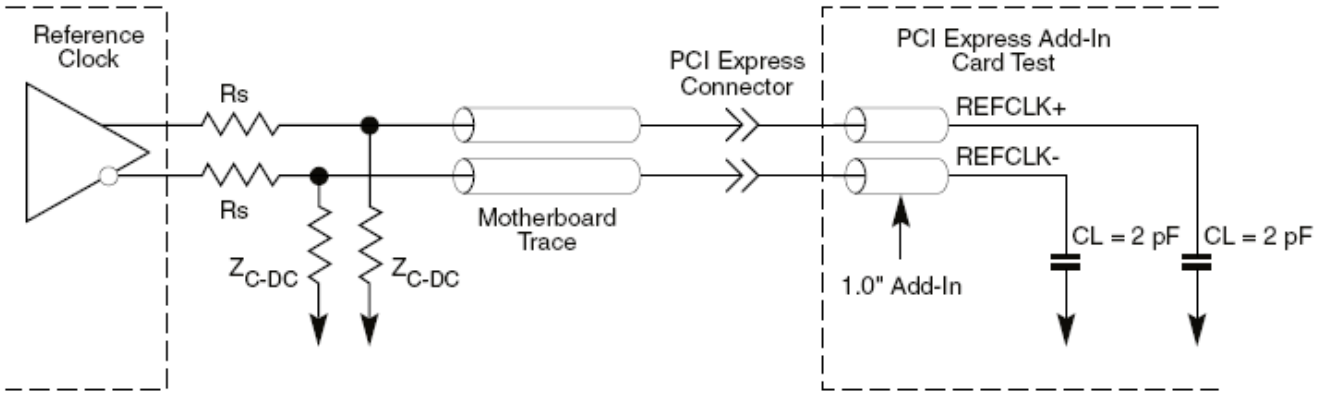


Figure 17. Reference Clock System Measurement Point and Loading

9.8.4. Auxiliary Signal Timing Parameters

Table 30. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{PERSTB-RTD}$	PERSTB Rising Time Duration	10	-	ms
T_{FAIL}*	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PWRON}	3.3Vaux Power On Time (Refer to Section 7.1, Page 25)	-	-	ms

Note 1: T_{FAIL} means 500 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.
Note 2: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

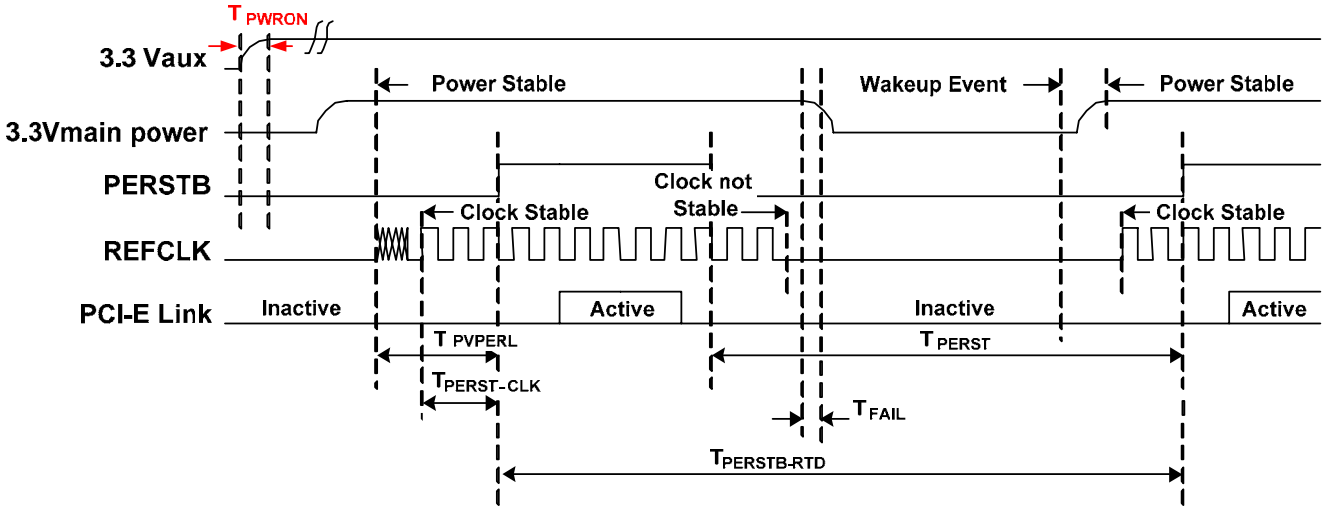
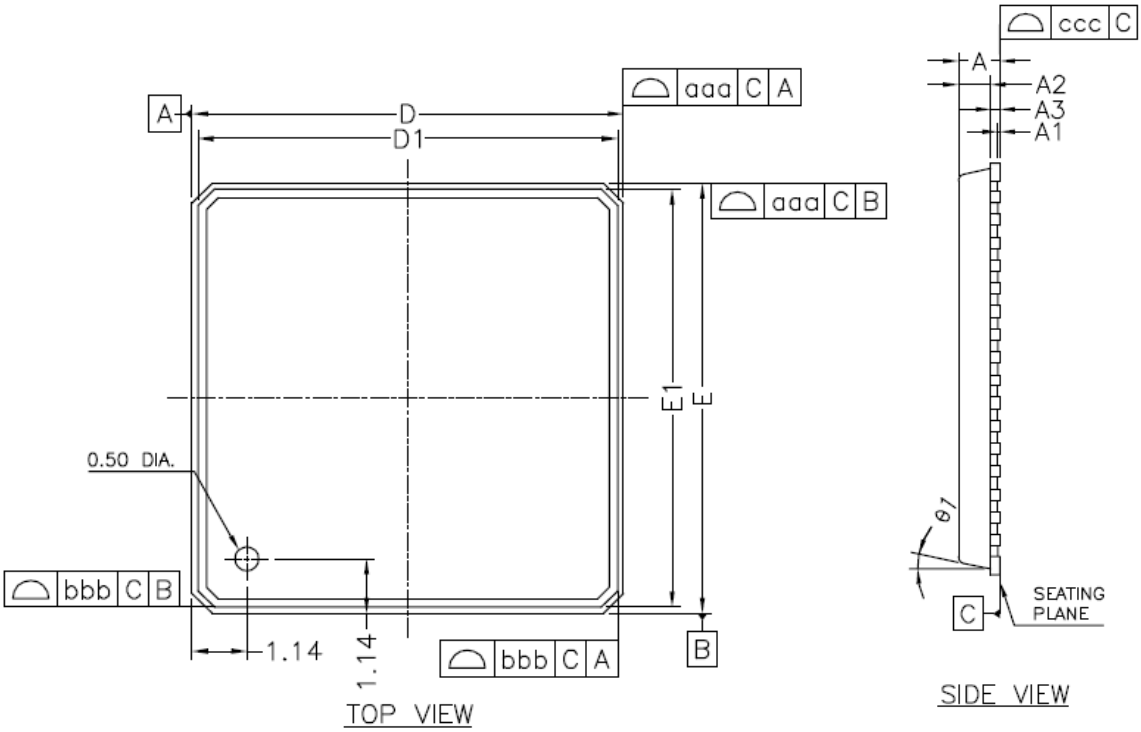
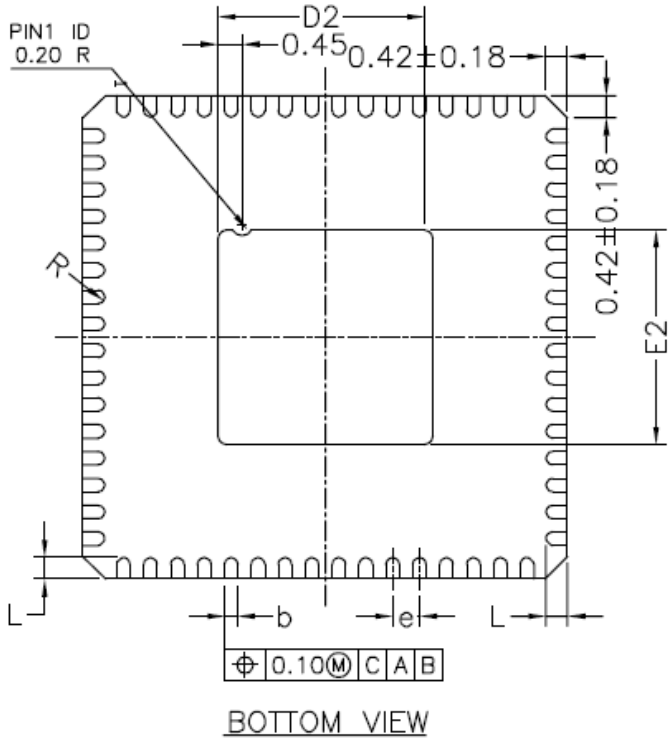


Figure 18. Auxiliary Signal Timing

10. Mechanical Dimensions





10.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.90	-	-	0.035
A_1	0.00	0.01	0.05	0.00	0.0004	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3	0.20 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	9.00 BSC			0.354 BSC		
D_1	8.75 BSC			0.344 BSC		
D_2	3.79	3.99	4.19	0.149	0.157	0.165
E	9.00 BSC			0.354 BSC		
E_1	8.75 BSC			0.344 BSC		
E_2	3.79	3.99	4.19	0.149	0.157	0.165
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 BSC			0.020 BSC		
θ_1	0°	-	12°	0°	-	12°
R	0.10	-	-	0.004	-	-
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Note 1: CONTROLLER DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 31. Ordering Information

Part Number	Package	Status
RTL8411-CG	64-Pin QFN 'Green' Package	MP

Note: See page 5 for package identification information.

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