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RTL8411

INTEGRATED 10/100/1000M ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

EEPROM & eFUSE DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/08/08	First release.
1.1	2011/09/01	Revised Figure 3 EEPROM/eFUSE Data Format, page 3. Revised Table 2 EEPROM & eFUSE Related Ethernet MAC Registers, page 5.

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1. EEPROM Contents

The RTL8411 requires the attachment of an external EEPROM. We support a 2-wire (TWSI) interface to access the EEPROM. The interface permits the RTL8411 to read from, and write data to, the external serial EEPROM device.

Values in the internal eFUSE memory or external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8411 will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8411 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via PCI VPD (Vital Product Data). The 2-wire (TWSI) EEPROM interface consists of SCL and SDA.

Although it is actually addressed by words, the EEPROM contents are listed in Table 1 below by bytes for convenience. After a power-on reset, PCI reset, and software EEPROM auto-load command in the 9346CR, the RTL8411 performs a series of read operations from the EEPROM.

We recommend you obtain Realtek's approval before changing the default settings of the EEPROM.

Table 1. EEPROM Contents

Bytes	Contents	Description
00h	29h	These 2 bytes contain ID code words for the RTL8411.
01h	81h	The RTL8411 will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are '10ECh' and '8168h'.
02h~07h	Ethernet ID	Ethernet ID. After an auto-load command or hardware reset, the RTL8411 loads Ethernet ID to IDR0~IDR5 of I/O registers.
08h-09h	VID	PCI Vendor ID. PCI configuration space offset 00h-01h.
0Ah~0Bh	DID	PCI Device ID. PCI configuration space offset 02h~03h.
0Ch~0Dh	SVID	PCI Subsystem Vendor ID. PCI configuration space offset 2Ch~2Dh.
0Eh~0Fh	SMID	PCI Subsystem ID. PCI configuration space offset 2Eh~2Fh.
10h~17h	PCI Express Serial Number Registers	PCIE Configuration Space Offset 164h~16Bh.
18~19h	Checksum	Checksum of the former data (00h~17h) in EEPROM.
1Ah	PXE_Para	PXE ROM Code Parameter. Reserved. Do not change this field without Realtek approval.
1Bh	RSVD	Reserved
40h~	VPD_Data	VPD Data Field. Offset 40h is the start address of the VPD data. Note: Need to set CONFIG 3 bit6 (VPDSel) to 0.
0Ch~	OTP data	Command to access registers with data. Data fields are always low-byte-first. The range depends on the type of EEPROM IC.

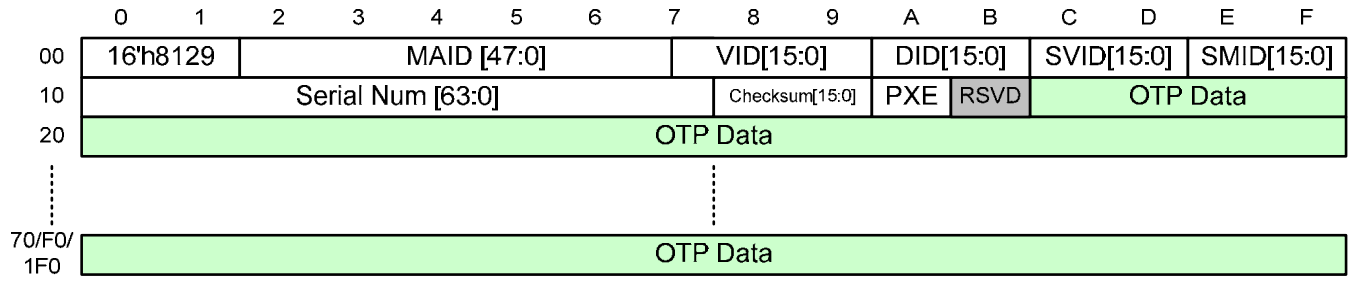

Figure 1. EEPROM Contents

1.1. EEPROM/eFUSE Data Format

Some eFUSE regions are reserved (see Figure 2). We recommend not to modify reserved regions without Realtek approval.

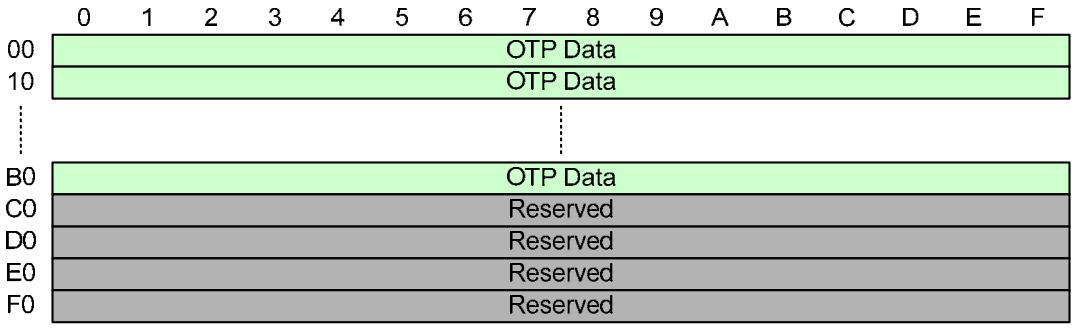

Figure 2. eFUSE Contents

To write commands in EEPROM/eFUSE, follow the format below:

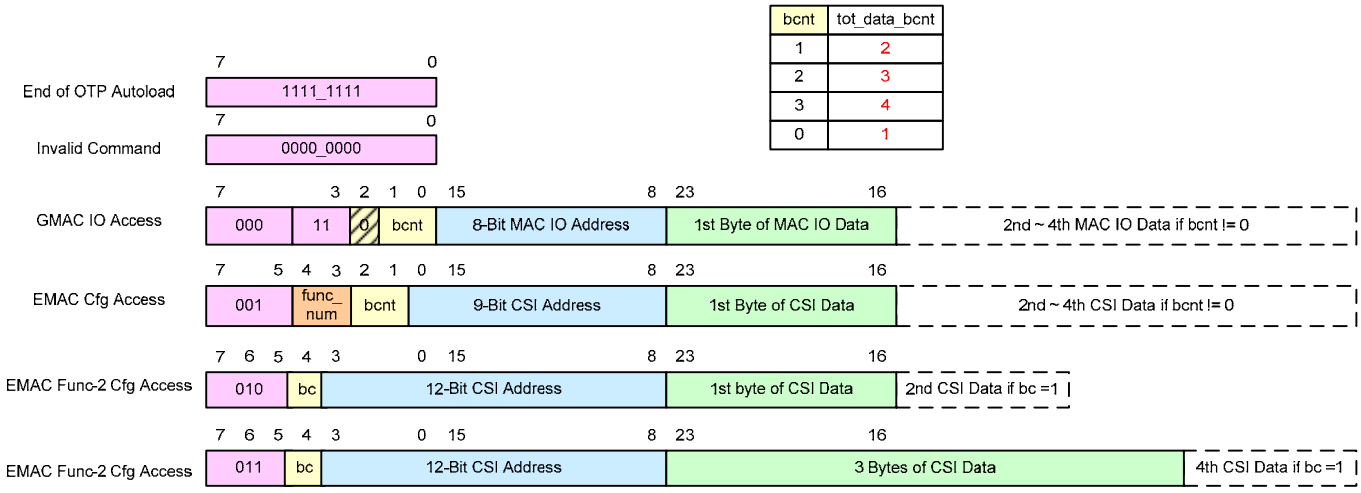

Figure 3. EEPROM/eFUSE Data Format

Note 1: Data fields are always low byte first.

Note 2: The incremental BCNT number of 'GMAC IO access' or 'EMAC cfg access' cannot overpass the DW boundary.

These patterns provide the method to access EMAC and GMAC registers . For example, if we want to fill MAC IO CONFIG 1 (offset 0x52) with value 0xCF, then the data format is 0x (CF 52 18). We first write the lowest byte, 0x18, then 0x52, and 0xCF in EEPROM/eFUSE, thus the value will be auto-loaded to the registers. If we want to write another data command, we continue writing it behind the previous one, as in the pattern below:

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
16'h8129		MAID [47:0]						VID[15:0]		DID[15:0]		SVID[15:0]		SMID[15:0]	
Serial Num [63:0]								Checksum[15:0]		PXE	RSVD	18	52	CF	...

Figure 4. EEPROM/eFUSE Data Example

The patterns are the same whether we write EEPROM or eFUSE, but since eFUSE is One-Time-Programmable, we cannot modify commands in eFUSE, unless we clear them to 0. On the other hand, we can modify commands in EEPROM.

2. PG Tool eFUSE Configuration File Contents

The RTL8411 features embedded configurable 2K-bit eFUSE One-Time-Programmable (OTP) memory. The eFUSE interface permits the RTL8411 to read from, and write data to, an internal eFUSE.

Values in the internal eFUSE allow default fields in PCI configuration space and I/O space to be overridden. Following a power-on reset or software EEPROM/eFUSE auto-load command, the RTL8411 will auto-load values from the eFUSE.

Note: To write commands in EEPROM/eFUSE, follow the format in section 1.1 EEPROM/eFUSE Data Format, page 2.

If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8411 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the eFUSE using 'bit-bang' accesses via the eFUSE Access Register.

3. EEPROM & eFUSE Related Ethernet MAC Registers

Table 2. EEPROM & eFUSE Related Ethernet MAC Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h~05h	IDR0–IDR5	RW	-	-	-	-	-	-	-	-
51h	CONFIG0	R	Bootrom_pgact	P_SPICS	P_SPISCK	P_SPISI	P_SPISO	BS2	BS1	BS0
		W	Bootrom_pgact	P_SPICS	P_SPISCK	P_SPISI	-	-	-	-
52h	CONFIG1	R	-	-	-	Speed_down	MEM MAP	IOMAP	VPD	PMEn
		W	-	-	-	Speed_down	-	-	-	-
53h	CONFIG2	R	-	-	-	Aux_Status	-	led_lp_en	lanwake_dly_en	-
		W	-	-	-	-	-	led_lp_en	lanwake_dly_en	-
54h	CONFIG3	R	-	VPDSel	-	LinkUp	-	Jumbo_en0	-	-
		W	-	VPDSel	-	LinkUp	-	Jumbo_en0	-	-
55h	CONFIG4	R	-	-	-	Isolate_disable_LAN	-	-	-	-
		W	-	-	-	Isolate_disable_LAN	-	-	-	-
56h	CONFIG5	R	-	BWF	MWF	UWF	-	-	LANWake	-
		W	-	BWF	MWF	UWF	-	-	LANWake	-

3.1. CONFIG 0 (Offset 0051h, RW)

Table 3. CONFIG 0 (Offset 0051h, RW)

Bit	Symbol	RW	Description
7	Bootrom_pgact	RW	When set to 1, the SPI flash can be directly accessed via bit 6~3, which now reflects the states of SPICSB, SPISK, SPIDI, and SPIDO pins respectively.
6	P_SPICS	RW	These bits reflect the state of the SPICSB, SPISK, SPIDI and SPIDO pins when bootrom_pgact is set to 1.
5	P_SPISCK	RW	
4	P_SPISI	RW	
3	P_SPISO	R	
2:0	BS2, BS1, BS0	R	Select Boot ROM Size

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	Reserved
1	1	1	Reserved

3.2. CONFIG 1 (Offset 0052h, RW)

Table 4. CONFIG 1 (Offset 0052h, RW)

Bit	Symbol	RW	Description
7:5	-	-	Reserved
4	Speed_down	RW	Speed Down Enable. 0: Link speed will stay at 100Mbps when the isolateb pin is low 1: Link speed changes from 100Mbps to 10Mbps when the isolateb pin is low
3	MEMMAP	R	Memory Mapping: The operational registers are mapped into PCI memory space. Always 1.
2	IOMAP	R	I/O Mapping: The operational registers are mapped into PCI I/O space. Always 1.
1	VPD	R	Vital Product Data: Set to enable Vital Product Data. Always 1.
0	PMEn	R	Power Management Enable. Always 1.

3.3. CONFIG 2 (Offset 0053h, RW)

Table 5. CONFIG 2 (Offset 0053h, RW)

Bit	Symbol	RW	Description
7:5	-	-	Reserved
4	Aux_Status	R	Auxiliary Power Present Status. 1: Aux. Power is present 0: Aux. Power is absent The value of this bit is fixed after each PCI reset.
3	-	-	Reserved
2	led_lp_en	RW	LED Low Power Enable. 1: LEDs are disabled except D0 state 0: LEDs are enabled in all power management states
1	lanwake_dly_en	RW	Lanwakeb Pin Delay Enable. 1: The lanwakeb pin is pulled low after 0.5s when the RTL8411 receives a WOL packet. 0: The lanwakeb pin is pulled low immediately the RTL8411 receives a WOL packet.
0	-	-	Reserved

3.4. CONFIG 3 (Offset 0054h, RW)

Table 6. CONFIG 3 (Offset 0054h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	VPDSel	RW	Vital Product Data Offset Select. 1'b0: VPD address start point = 40h 1'b1: VPD address start point = 00h
5	-	-	Reserved
4	LinkUp	RW	Link Up. This bit is valid when the PMEn bit of the CONFIG1 register is set. The RTL8411, in an adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is re-established.
3	-	-	Reserved
2	Jumbo_En0	RW	Jumbo Enable. 1: This bit sets to 1 when the RTL8411 has jumbo frames to transmit 0: If there are no jumbo frame packets to transmit, this bit sets to 0
1:0	-	-	Reserved

3.5. CONFIG 4 (Offset 0055h, RW)

Table 7. CONFIG 4 (Offset 0055h, RW)

Bit	Symbol	RW	Description
7:5	-	-	Reserved
4	Isolate_disable_LAN	RW	1: Enable (IsolateB is set low to disable LAN) 0: Disable (IsolateB is set low and DOES NOT disable LAN)
3:0	-	-	Reserved

3.6. CONFIG 5 (Offset 0056h, RW)

Table 8. CONFIG 5 (Offset 0056h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	BWF	RW	Broadcast Wakeup Frame. 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. 0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only the DID field = FF FF FF FF FF FF. The power-on default value of this bit is 0.
5	MWF	RW	Multicast Wakeup Frame. 1: Enable Multicast Wakeup Frame with mask bytes of only the DID field, which is a multicast address. 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only the DID field, which is a multicast address. The power-on default value of this bit is 0.
4	UWF	RW	Unicast Wakeup Frame. 1: Enable Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address. 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address. The power-on default value of this bit is 0.
3:2	-	-	Reserved
1	LANWake	RW	LANWake Signal Enable/Disable. 1: Enable LANWake signal 0: Disable LANWake signal
0	-	-	Reserved

4. EEPROM & eFUSE Related Power Management Registers

Table 9. EEPROM & eFUSE Related Power Management Registers

Configuration Space Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

4.1. PCI Configuration Space Table

Table 10. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	IntDisable	0	SERREN
		W	-	-	-	-	-	IntDisable	-	SERREN
06h	Status	R	0	0	0	1	IntSt	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	0	0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	1	1
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	CLS7	CLS6	CLS5	CLS4	CLS3	CLS2	CLS1	CLS0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		RW	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		RW	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		RW	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h~ 17h	Reserved									
18h	MEM 64 BAR	R	MEM7	0	0	0	MEMPF	MEMLOC	MEMLOC	MEMIN
19h		RW	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
1Ah		RW	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
1Bh		RW	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
1Ch		RW	MEM39	MEM38	MEM37	MEM36	MEM35	MEM34	MEM33	MEM32
1Dh		RW	MEM47	MEM46	MEM45	MEM44	MEM43	MEM42	MEM41	MEM40
1Eh		RW	MEM55	MEM54	MEM53	MEM52	MEM51	MEM50	MEM49	MEM48
1Fh		RW	MEM63	MEM62	MEM61	MEM60	MEM59	MEM58	MEM57	MEM56

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h~27h	Reserved									
28h~2Bh	CISPtr	CardBus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		RW	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h~3Bh	Reserved									
3Ch	ILR	RW	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	1	0	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
45h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
46~4Fh	Reserved									
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	1	0	0	0	0
52h	Message Control	R	64-bit Address Capable	Multiple Message Enable			0	0	0	MSI Enable
		W	-	Multiple Message Enable			-	-	0	MSI Enable
53h	Reserved. Always returns 0									
54h~57h	Message Address Low	RW	64-bit Interrupt Message Address Low							
58h~5Bh	Message Address High	RW	64-bit Interrupt Message Address High							
5Ch~5Dh	Message Data	RW	16-bit Message Data							
5E~6Fh	Reserved									
70h	PCIEID	R	0	0	0	1	0	0	0	0
71h	NextPtr	R	1	0	1	0	1	1	0	0
72h~73h	PCIE Cap.	R	0	0	0	0	0	0	1	0
		R	0	0	0	0	0	0	1	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74h~77h	Device Capability Register	R	L0s_acpt_latency[1]	L0s_acpt_latency[0]	Entend_tag_support	0	0	Max_payload_size_support		
		R	Role Base Error rpt	0	0	0	L1_acpt_latency[2]	L1_acpt_latency[1]	L1_acpt_latency[0]	L0s_acpt_latency[2]
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
78h~79h	Device Control Register	RW	Max_payload_size			Relaxed_ordering_en	Unsupport_rqst_rpt_en	Fatal_err_rpt_en	Non_fatal_err_rpt_en	Correct-able_err_rpt_en
		RW	0	Max_read_request_size			No_snoop_en	Auxpwr_PM_en	0	Entend_tag_en
7Ah	Device Status Register	R	0	0	Transaction_pending	AuxPwr_det	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correct-able_err_det
		W	0	0	-	-	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correct-able_err_det
7Bh		R	0	0	0	0	0	0	0	0
7Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
7Dh		R	L1_exit_lat[0]	L0s_exit_lat[2]	L0s_exit_lat[1]	L0s_exit_lat[0]	ASPM_support		0	0
7Eh		R	0	0	0	0	0	Clock_PM	L1_exit_lat[2]	L1_exit_lat[1]0
7Fh		R	0	0	0	0	0	0	0	0
80h	Link Control Register	R	Extended_sync	Common_clock	0	0	RCB	0	ASPM_control	
		W	Extended_sync	Common_clock	0	0	RCB	0	ASPM_control	
81h		R	0	0	0	0	0	0	0	Enable clock_PM
		W	0	0	0	0	0	0	0	Enable clock_PM
82h	Link Status Register	R	0	0	0	1	0	0	0	1
83h		R	0	0	0	Slot_clock_cfg	0	0	0	0
84h	Slot Capability Register	R	Slot power Limit[0]	Hot-Plug Capable	Hot-Plug Surprise	Power Indicator Present	Attn Indicator Present	MRL Sensor Present	Power Control Present	Attn Bottom Present
85h		R	Slot Power Limit scale[0]	Slot Power Limit[7]	Slot Power Limit[6]	Slot Power Limit[5]	Slot Power Limit[4]	Slot Power Limit[3]	Slot Power Limit[2]	Slot Power Limit[1]
86h		R	Physical Slot Number[4]	Physical Slot Number[3]	Physical Slot Number[2]	Physical Slot Number[1]	Physical Slot Number[0]	No Common Complete Support	Electromechanical Interlock Present	Slot Power Limit Scale[1]
87h		R	Physical Slot Number[12]	Physical Slot Number[11]	Physical Slot Number[10]	Physical Slot Number[9]	Physical Slot Number[8]	Physical Slot Number[7]	Physical Slot Number[6]	Physical Slot Number[5]
88h	Slot Control Register	RW	Attn Indicator Control[1]	Attn Indicator Control[0]	Hot-Plug Interrupt Enable	Command Completed Interrupt Enable	Presence Detect Changed Enable	MRL Sensor Changed Enable	Power Fault Detected Enable	Attn Button Pressed Enable
89h		RW	-	-	-	Data Link Layer State Changed Enable	Electromechanical Interlock Control	Power Controller Control	Power Indicator Control[1]	Power Indicator Control[0]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ah	Slot Status Register	R	Electro-mechanical Interlock Status	Presence Detect State	MRL Sensor State	Command Completed	Presence Detect Changed	MRL Sensor Changed	Power Fault Detected	Attn Button Pressed
8Bh		R	Reserved							Data Link Layer State Changed
8Ch~AFh	Reserved									
ACh	MSI-X ID	R	0	0	0	1	0	0	0	1
ADh	NextPtr	R	1	1	0	0	1	1	0	0
AEh		R	MSI-X Table_ Size[7]	MSI-X Table_ Size[6]	MSI-X Table_ Size[5]	MSI-X Table_ Size[4]	MSI-X Table_ Size[3]	MSI-X Table _Size[2]	MSI-X Table _Size[1]	MSI-X Table _Size[0]
AFh		R	MSI-X Enable	Function Mask	Reserved			MSI-X Table _Size[10]	MSI-X Table _Size[9]	MSI-X Table _Size[8]
B0h	MSI-X Table Offset and BIR Register	R	Table Offset[4]	Table Offset[3]	Table Offset[2]	Table Offset[1]	Table Offset[0]	BIR[2]	BIR[1]	BIR[0]
B1h		R	Table Offset[12]	Table Offset[11]	Table Offset[10]	Table Offset[9]	Table Offset[8]	Table Offset[7]	Table Offset[6]	Table Offset[5]
B2h		R	Table Offset[20]	Table Offset[19]	Table Offset[18]	Table Offset[17]	Table Offset[16]	Table Offset[15]	Table Offset[14]	Table Offset[13]
B3h		R	Table Offset[28]	Table Offset[27]	Table Offset[26]	Table Offset[25]	Table Offset[24]	Table Offset[23]	Table Offset[22]	Table Offset[21]
B4h	MSI-X PBA Offset and BIR	R	PBA Table Offset[4]	PBA Table Offset[3]	PBA Table Offset[2]	PBA Table Offset[1]	PBA Table Offset[0]	PBA BIR[2]	PBA BIR[1]	PBA BIR[0]
B5h		R	PBA Table Offset[12]	PBA Table Offset[11]	PBA Table Offset[10]	PBA Table Offset[9]	PBA Table Offset[8]	PBA Table Offset[7]	PBA Table Offset[6]	PBA Table Offset[5]
B6h		R	PBA Table Offset[20]	PBA Table Offset[19]	PBA Table Offset[18]	PBA Table Offset[17]	PBA Table Offset[16]	PBA Table Offset[15]	PBA Table Offset[14]	PBA Table Offset[13]
B7h		R	PBA Table Offset[28]	PBA Table Offset[27]	PBA Table Offset[26]	PBA Table Offset[25]	PBA Table Offset[24]	PBA Table Offset[23]	PBA Table Offset[22]	PBA Table Offset[21]
B8h~CBh	Reserved									
CCh	VPDID	R	0	0	0	0	0	0	1	1
CDh	NextPTR	R	0	0	0	0	0	0	0	0
CEh	Flag VPD Address	RW	VPD ARRD7	VPD ARRD6	VPD ARRD5	VPD ARRD4	VPD ARRD3	VPD ARRD2	VPD ARRD1	VPD ARRD0
CFh		RW	Flag	VPD ARRD14	VPD ARRD13	VPD ARRD12	VPD ARRD11	VPD ARRD10	VPD ARRD9	VPD ARRD8
D0h	VPD Data	RW	VPD Data7	VPD Data6	VPD Data5	VPD Data4	VPD Data3	VPD Data2	VPD Data1	VPD Data0
D1h		RW	VPD Data15	VPD Data14	VPD Data13	VPD Data12	VPD Data11	VPD Data10	VPD Data9	VPD Data8
D2h		RW	VPD Data23	VPD Data22	VPD Data21	VPD Data20	VPD Data19	VPD Data18	VPD Data17	VPD Data16
D3h		RW	VPD Data31	VPD Data30	VPD Data29	VPD Data28	VPD Data27	VPD Data26	VPD Data25	VPD Data24
D4h~FFh	Reserved									

5. PXE Parameters

Table 11. PXE Parameters

Bit	Symbol	RW	Description
7-6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5-4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3	Show Config Message	RW	0: Enable 1: Disable
2	Shift+F10 Menu Entry	RW	0: Enable 1: Disable
1-0	Show Config Time	RW	00: 3 Seconds 01: 5 Seconds 10: 1 Second 11: 0 Seconds

6. Pin Assignments

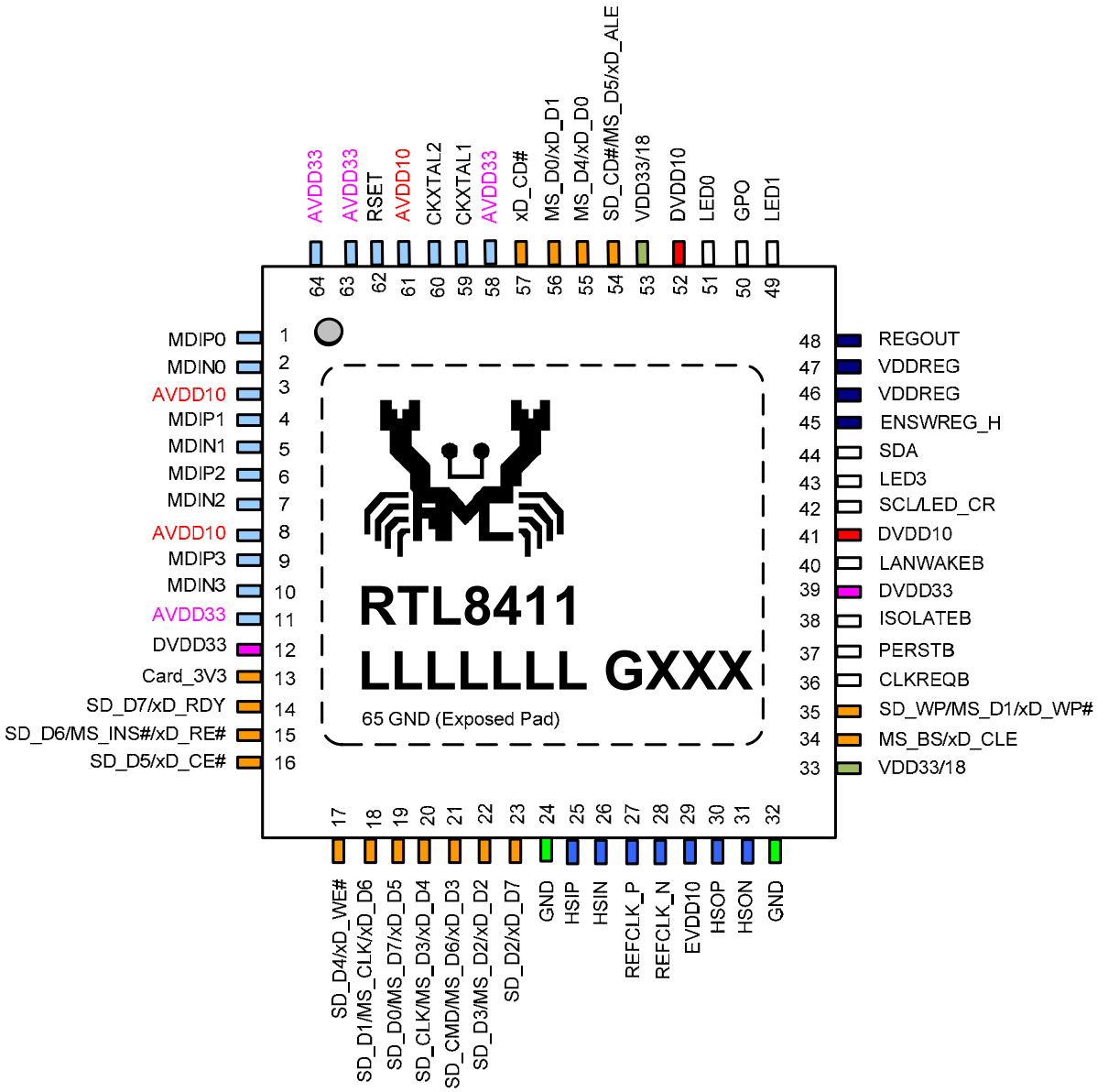

Figure 5. Pin Assignments

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