Electronics Guide for Plastic Logic displays

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Contents

1. Introduction 3
2. Display system – general architecture 4
2.1 Display system-evaluation systems 4
2.2 Host processor choices-general 4
2.3 Display power supply system-general 4
2.4 Display controller-general 5
3. Host processor 6
3.1 Requirements: GPIO, SPI, I^2C, memory 6
3.2 Interfaces to power supply and controller 6
4. Display power supplies 9
4.1 Display power requirements 9
4.2 Choice of PMIC 10
4.3 Configuring the PMIC 10
5. Display controller 13
5.1 I^2C master (where fitted) 13
5.2 Temperature measurement 13
5.3 Display waveforms-general 13
6. Primary power supplies 15
6.1 Voltage range 15
6.2 Batteries 15
6.3 Wall adaptors 15
6.4 PCB layout considerations 15
7. Reference design examples 16

1. Introduction

This document details options available for integration of Plastic Logic's displays into end-user devices

Topics covered include an overview of system requirements, choice of controller, power supply components, and general operation of the display subsystem.

2. Display system – general architecture

The display and its associated electronics system consist of:

1. A host processor to manage the configuration and control of the display subsystem. In the simplest case this may be a microcontroller with storage for a number of pre-prepared images. More complex systems using a system-on-chip based device would allow complex dynamic image creation and manipulation.
2. A power supply that generates the voltages needed for the Plastic Logic display.
3. A display controller, usually an integrated device that converts image data to the correct sequence of control signals and data to drive the display. The display controller may be integrated into the display module itself. Usually such an integrated controller provides direct drive to the display source (data) lines and it generates timing signals to control the display gate (select) lines via a separate gate driver device. The display controller may also optionally control the display power supplies.

2.1 *Display system-evaluation systems*

Plastic Logic offers a range of adaptor circuits to enable connection of different display module types to any of its power supply and host processor options. These are intended to enable system integrators to quickly evaluate different configurations of host processor, power supply system and display module type. Reference circuit designs are available for all adaptor/interface PCBs.

2.2 *Host processor choices-general*

Plastic Logic currently supports and can offer reference hardware and software designs for the following processor devices:

1. Microcontrollers

   A code base targeted at limited-resource single-chip microcontrollers. Currently targeting the TI MSP430 but intended to be portable to a wider range of microcontrollers, *e.g.* PIC and ARM
2. BeagleBone White (support for BeagleBone Black is also planned)

2.3 *Display power supply system-general*

The display power supply system is based around a power management IC (PMIC). The PMIC is used to convert the primary supply *e.g.* 4.2V battery, into the voltages required by the display drivers. Plastic Logic can provide reference hardware designs for two PMICs:

1. Maxim MAX17135
2. Texas Instruments TPS65185

Both PMIC types have hardware control signals for enabling HV generation and use a two-wire serial bus (I^2C) to configure the power-up and power-down sequences and monitor the device status if required.

In some Plastic Logic evaluation systems jumpers are provided in the I^2C bus to enable either the host processor or display controller to act as the I^2C master.

2.4 *Display controller-general*

Plastic Logic's "Epson Platform display modules modules", like S040_T1.1 and S049_T1.1 use the Epson S1D13541 EPD source driver. The controller may be mounted directly to the display (Chip on Plastic – COP) or on a chip-on-film (COF) adaptor together with the display gate driver device.

For both COP and COF types, Plastic Logic's display module terminates in an input connection suitable for a ZIF flip-lock type connector. For COF module types the interface PCB incorporates passive components for supply decoupling, temperature sensing etc. For COP types these components must be fitted as part of the main electronics/power supply PCB.

Plastic Logic's "Driver only Platform display modules", like D107_T3.1 and S047_T2.1 use a separate EPD controller like the Epson S1D13524. The Controller may be mounted to the Processor-PCB.

3. Host processor

3.1 *Requirements: GPIO, SPI, I²C, memory*

The hardware resources required to implement a working display subsystem will depend on exactly which components are chosen and how they are connected together. In the worst case the following is required:

1. An SPI interface to communicate with the Epson display controller (4 wire)
2. An I²C interface to communicate with the PMIC and other peripherals (2 wire)
3. 3 or 4 GPIO's to control/monitor the PMIC power sequencing
4. 1 GPIO for Epson controller management (Reset)
5. 1 GPIO (Interrupt) for interrupt reporting from the Epson controller

The best case is a single SPI interface to communicate with the Epson controller and then use the SPI to I²C bridge within it to provide the I²C interface to the other peripherals. In this case an additional I²C to GPIO converter (not supplied) would be required to control the power supply sequencing – NB although the Epson controller can in principle be used to do this, the required control lines are not currently available on the display connector. Reset would be achieved by a power on reset circuit/chip and interrupts would not be used. Status monitoring would be by polling status registers.

In addition to the hardware resources listed, non-volatile storage is required for the storage of two blobs of binary data which must be passed to the display controller. One file, typically 4KB, contains an Epson firmware with general controller configuration data and must be loaded each time the controller is powered up. The other blob contains display drive configuration data (waveforms) which need to be reloaded as the operating temperature of the display controller changes. Waveform sizes are still being determined but will typically use 32KB or less.

3.2 *Interfaces to power supply and controller*

In this section the host processor is considered to be controlling the display power supplies. In future display modules designs it is intended that the display power supplies will be controllable via the display controller in order to reduce the required GPIO count.

In this section "power supply" refers to the PMIC and the display front-plane COM (VCOM_FP) switch. Please refer to 4.1.5 for details of the COM switch function and operation.

3.2.1 Host processor interface signals

Plastic Logic's displays reference designs use a common pin assignment for connections between the host processor and the display system.

Display system input connector pin number	Signal name	Function
1, 2, 3, 4	VMAIN, VBATT	Primary power supply input
5	HD/C	Not used on displays with S1D13541 controller
6	SCL	I^2C clock (Driven by host or Epson controller)
7	SDA	I^2C data (Driven by host or Epson controller)
8	SPICLK	SPI bus clock
9	SPI_MOSI	SPI bus master out, slave in
10	SPICS	SPI bus chip select
11	SPI_MISO	SPI bus master in, slave out
12	HRDY	Not used on PL displays
13	HIRQ	Interrupt from controller
14	RST#	Reset input to controller
15	VCOM_SW_CLOSE, HVSW_CTRL	VCOM switch control
16	HVEN, PMIC_EN	Display supplies enable
17	HV_POK, PMIC_POK	Power OK return from PMIC
18	PMIC_FLT	PMIC fault detected
19	3V3_EN	Logic supply enable
20	BB_SLEEP	Control line to put PMIC into very low power sleep mode and disable clock circuit
21, 22, 23, 24	GND	Power ground

Table 1: Host processor interface signals

3.2.2 Host to Power Supply

Two communication channels are used:

1. Two-wire serial (I^2C) connection
2. Three individual power supply control and status signals.

Host to power supply I^2C bus

The I^2C bus is used to configure the PMIC power rail switching sequence. Both Maxim and TI PMICs support programmable power sequencing. For all Plastic Logic display modules it is recommended that the sequence defined in the reference software should be used. In some cases incorrect sequencing can lead to display module damage and /or excessive start-up current demand on the primary power supply.

Host to power supply: hardware signals

Four signals are employed:

1. HVEN, PMIC_EN – High Voltage Enable. The host drives this line to logic HIGH to initiate the power up sequence.
2. HV_POK, PMIC_POK – Power OK. The PMIC drives this signal logic HIGH when the display power up sequence has completed successfully.
3. VCOM_SW_CLOSE, HVSW_CTRL. The host drives this signal to logic HIGH to close the display front-plane COM switch.
4. PMIC_FLT. The PMIC drives this to indicate that there is a fault condition within the PMIC which requires host intervention. The two PMICs have a slightly different definition of what constitutes a fault condition.

4. Display power supplies

4.1 *Display power requirements*

In addition to logic level power supplies Plastic Logic display modules require five power supply voltages for the display drivers and front-plane COM supply.

4.1.1 Logic supplies

The display module and PMIC need a 3.3V supply. Plastic Logic's reference designs include a 3.3V low drop out series regulator to provide this supply.

4.1.2 Source driver supplies

VSPOS & VSNEG: +15V and -15V respectively.
The display module source driver supplies are the primary outputs from the PMIC switch-mode converters. The PMIC design ensures that these voltages are equal magnitude *i.e.* VSPOS+VSNEG=0. The value of VSPOS is set by feedback resistors but it is recommended to use the values in the Plastic Logic reference design. It is not possible to set VSNEG independently of VSPOS. The source driver current drawn by small displays is sufficiently low that either PMIC will give adequate output. Large displays may require the Maxim PMIC.

4.1.3 Gate driver supplies

There are two gate driver supplies. The characteristics of Plastic Logic's backplane require that these voltages are not equal.

1. VGPOS: Gate driver supply, usually +25V for small displays and +28V for large displays.
2. VGNEG: Gate driver negative supply. Usually -32V for small displays and -42V for large displays

The current drawn from the gate driver supplies is very small, c. 2mA. In the reference designs the gate voltages are generated from the main outputs using regulated voltage multiplier stages.

4.1.4 Front plane COM supply

VCOM_FP: Display front-plane COM supply. The front-plane COM supply is used to cancel the effect of the display "kickback" voltage. In an ideal display, the front-plane COM voltage would be zero but due to internal feed through of the gate driver output signals this is not the case. In Plastic Logic's backplane VCOM_FP is set to a positive voltage in the range 2 to 12V depending on the exact display design and characteristics. Each display is characterised at the factory and a value of VCOM_FP is measured. It is important that VCOM_FP is set to the factory value otherwise image quality will be degraded with loss of contrast.

It is a requirement that the front-plane COM supply is able to both sink and source current. In Plastic Logic's reference designs an operational amplifier (op-amp) is used. Refer to Section 4.3.2 for more information on the VCOM_FP supply.

4.1.5 Front plane COM switch

The front-plane COM switch is included in the VCOM_FP supply to isolate the display front-plane COM electrode during display power-up and power-down. This prevents unwanted drive to the display medium during display power transitions. The timing of the switch control is discussed in Section 4.3.3.

4.2 *Choice of PMIC*

Plastic Logic has tested and developed circuits for two display power management ICs (PMICs), the Maxim MAX17135 and Texas Instruments' TPS65185.
Each has its own merits and the choice of PMIC is application dependent. Table 2 below shows the primary features that determine the application.

Feature	MAX17135	TPS65185
Package size (mm)	5 x 5	6 x 6
Max output, mA (VSPOS &VSNEG)	200	120
Quiescent power, supplies on, no load	100mW	30mW
Very low power (sleep) mode	Yes (I^2C register)	Yes (hardware pin)
Start up inrush	Approx 1.5A for 5us	Approx 1A for 5us
Non-volatile storage of power sequence timings	Yes (via fuse)	No

Table 2: Comparison of PMIC features

For small displays, the better low-load efficiency favours the TPS65185 although for possible wearable applications the larger package size counts against it. Large displays may require the maximum power output of the Maxim PMIC

4.3 *Configuring the PMIC*

Both Maxim and TI PMICs have I^2C registers that are used to control the sequence in which the power rails are turned on and off. For optimum display performance and minimal power consumption it is important that the display supplies are sequenced correctly. Plastic Logic's reference software defines the optimum power sequence.

4.3.1 Power supply sequencing

The sequence in the Plastic Logic reference software has been optimised for display performance and minimum inrush current to the PMIC. The exact timings of the sequences to turn the power on and off vary with each display type as they depend on the driver chips used and the general display design. The software needs to be aware of which display type is being used in order to use

the correct sequence, which may be typically read back from a display EEPROM, hard-coded in the software driver or defined in a configuration file.

4.3.2 VCOM_FP setting

Each display has a value for VCOM_FP which is measured at the factory. In the Plastic Logic displays reference designs the VCOM_FP supply is an inverting op-amp with its input taken from the PMIC's internal VCOM generator. [Both Maxim and TI PMICs are designed for backplanes with N-channel TFTs and their VCOM outputs are negative. Plastic Logic's backplanes use P-channel TFTs and VCOM_FP needs to be a positive voltage, hence the need for an inverting amplifier.]

There will be gain and offset errors in the VCOM_FP supply and these errors will vary from one instance of the circuit to the next. These errors can be compensated by the VCOM_FP setting procedure. This will make use of factory measurements of the VCOM_FP supply characteristics, essentially some VCOM DAC register values and the corresponding output voltages.

The ideal VCOM_FP voltage also needs to be scaled on a per-board basis with the difference between the gate power supplies VGPOS and VGNEG. This voltage difference is referred to as the VG swing.

Factory calibration of the COM DAC & amplifier chain

This method uses a two-point calibration to determine the gain and offset of the VCOM_FP DAC and amplifier. For reference design hardware the calibration is performed in the PL factory, but the basic principle is described here:

1. Program the VCOM DAC with ¼ full scale
2. Measure the resulting VCOM_FP
3. Program the VCOM DAC with ¾ full scale
4. Measure the resulting VCOM_FP
5. Measure the positive and negative gate power voltages

Use of calibration data by the controller or application

The calibration data is typically stored in an EEPROM on Hummingbird Z6 and Z7. These data may be stored in another persistent memory on an optimised product design to reduce the costs. The method as documented below is implemented by the reference software, which takes as inputs the ideal VCOM_FP voltage in mV and the factory calibration data in order to set the correct VCOM DAC register value.

1. Scale the ideal VCOM_FP voltage by multiplying by VG swing and dividing it by the ideal VG swing (typically 57.089 V) :

VCOM_FP_SCALED = VCOM_FP * (VGPOS – VGNEG) / VG_SWING_IDEAL

2. Calculate the DAC register value based on the factory measurements and the scaled VCOM_FP_SCALED voltage using linear interpolation. For a given pair of DAC register values (x1, x2) and output voltages (y1, y2), the DAC register value is:
   dx = x2 - x1
   dy = y2 - y1
   dac_offset = y1 - (x1 * dy / dx)
   dac_value = (VCOM_FP_SCALED - dac_offset) * dx / dy

4.3.3 COM switch control

The COM switch is under the control of the host processor. The COM switch must be open during display supplies' power up and power down and must only be closed when the display is updating.

5. Display controller

5.1 *I²C master (where fitted)*

The display controller may be configured to act as an I²C master. The controller has an SPI to I²C bridge through which the host processor can access the power supply PMIC's I²C registers and other devices on the I²C bus.

5.2 *Temperature measurement*

For correct operation of the display the display controller must use the correct waveform data for the current environmental temperature. In the S1D13541 controller this involves measuring the temperature, asking the controller to determine if new waveforms are required and, if so, sending the updated waveform data to the controller.

Temperature measurements may be obtained from the display controller, the power supply PMIC or some external component by the host processor as appropriate to the design. In addition the display controller can be configured to automatically sense the temperature either by querying an LM75 compatible temperature sensor over I²C or using its internal temperature sensor.

5.2.1 Temperature from display controller

Some Plastic Logic display modules have negative temperature coefficient (NTC) thermistor-based temperature sensors. The display controller can report temperature by measuring the voltage on its VNTC input. Temperature information may be used to select the optimum display driver waveform.

5.2.2 Temperature from PMIC

Both PMICs have temperature sensing capabilities. The TI device uses an external thermistor; the Maxim device uses an external diode. The Maxim device's temperature register is designed to mimic an LM75 I²C temperature sensor and this is compatible with the display controller's requirement.

5.3 *Display waveforms-general*

"Waveform" is the name given to a table that defines the sequence of drive pulses generated by the display controller source drivers. It determines the sequences of drive-to-black or drive-to-white that are applied to the display medium in order to change any given pixel from one grey level to another. The properties of the display medium are such that the optimum waveform changes with temperature and media batch, in which case there may be several waveform tables associated with the display module. The correct waveforms must be used with a given display

panel. Waveforms should not, generally, be considered interchangeable or generic across displays.

5.3.1 Waveform storage options

The waveform information needs to be readily accessible as it will be necessary to resend the waveform data when the controller determines that the waveform data it currently has in no longer valid for the environmental temperature it is currently operating in. The typical waveform size is still being determined but is likely to exceed the amount of internal storage available in many microcontroller devices. It is likely that external storage will be required for the waveform data.

6. Primary power supplies

6.1 *Voltage range*

Plastic Logic's displays electronics systems are designed to operate with input voltage in the range 3.5 to 5V. It is important that the primary power source has low internal resistance to minimise the effects of voltage drops due to load current. In particular the PMICs draw considerable inrush current, albeit for a short duration. See PCB layout considerations below.

6.2 *Batteries*

Plastic Logic has found that 4.2V Li-polymer batteries are suitable as a power source. Rechargeable mobile phone (5V output) types are also suitable. The Ah rating required is application dependent, but the battery should have an internal resistance of less than 100 mΩ.

Coin cells are not suitable because their internal resistance is too high.

6.3 *Wall adaptors*

Wall adaptors without output voltage of 5V are a suitable power source. For small displays units rated at 1A or more are suitable. Large displays may require units rated at 2A or above.

6.4 *PCB layout considerations*

The remarks concerning inrush current in Section 6.1 are applicable. The trace width for the PMIC switch mode inputs (VMAIN) should be as wide as possible and a ground plane should be used. If the primary power supply is remote from the display system the power wiring should have substantial cross-section.

7. Reference design examples

PL Name	COM DAC	PMIC	Display conn	CPU conn	CPU	Module B	Bracelet	Supports Epson PSU control	Controller support comps.
HB Z6	Internal only	TI	20-way	24-way	MSP 430 via Ruddock	Y	N	N	On flex
HB Z7 Jf	Internal only	TI	30-way	24-way	MSP 430 via Ruddock	N	Y	N	On main board