AN-6076 Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

INTRODUCTION

The purpose of this paper is to demonstrate a systematic approach to design high−performance bootstrap gate drive circuits for high−frequency, high−power, and high−efficiency switching applications using a power MOSFET and IGBT. It should be of interest to power electronics engineers at all levels of experience. In the most of switching applications, efficiency focuses on switching losses that are mainly dependent on switching speed. Therefore, the switching characteristics are very important in most of the high−power switching applications presented in this paper. One of the most widely used methods to supply power to the high−side gate drive circuitry of the high−voltage gate−drive IC is the bootstrap power supply. This bootstrap power supply technique has the advantage of being simple and low cost. However, it has some limitations, on time of duty−cycle is limited by the requirement to refresh the charge in the bootstrap capacitor and serious problems occur when the negative voltage is presented at the source of the switching device. The most popular bootstrap circuit solutions are analyzed; including the effects of parasitic elements, the bootstrap resistor, and capacitor; on the charge of the floating supply application.

HIGH−SPEED GATE−DRIVER CIRCUITRY

Bootstrap Gate−Drive Technique

The focus of this topic is the bootstrap gate−drive circuit requirements of the power MOSFET and IGBT in various switching−mode power−conversion applications. Where input voltage levels prohibit the use of direct−gate drive circuits for high−side N−channel power MOSFET or IGBT, the principle of bootstrap gate−drive technique can be considered. This method is utilized as a gate drive and accompanying bias circuit, both referenced to the source of the main switching device. Both the driver and bias circuit swing between the two input voltage rails together with the source of the device. However, the driver and its floating bias can be implemented by low−voltage circuit elements since the input voltage is never applied across their components. The driver and the ground referenced control signal are linked by a level shift circuit that must tolerate the high−voltage difference and considerable capacitive switching currents between the floating high−side and ground−referenced low−side circuits. The high−voltage gate−drive ICs are differentiated by unique level−shift design. To maintain high efficiency and manageable power dissipation, the level−shifters should not draw any current during the on−time of the main switch. A widely used technique for these applications is called pulsed latch level translators, shown in Figure 1.

Bootstrap Drive Circuit Operation

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the V_S goes below the IC supply voltage V_{DD} or is pulled down to ground (the low-side switch is turned on and the high-side switch is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the V_{DD} power supply, as shown in Figure 2. This is provided by V_{BS} when V_S is pulled to a higher voltage by the high-side switch, the V_{BS} supply floats and the bootstrap diode reverses bias and blocks the rail voltage (the low-side switch is turned off and high-side switch is turned on) from the IC supply voltage, V_{DD}.

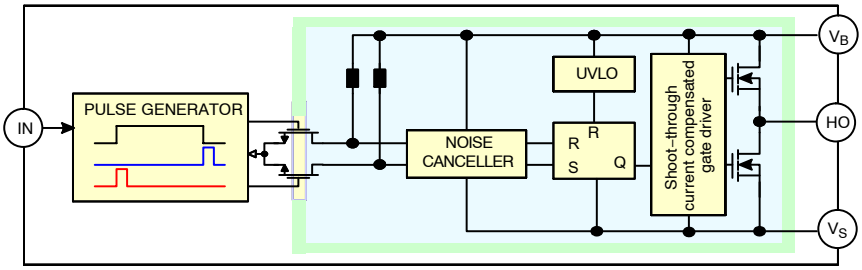


Figure 1. Level−Shifter in High−Side Drive IC

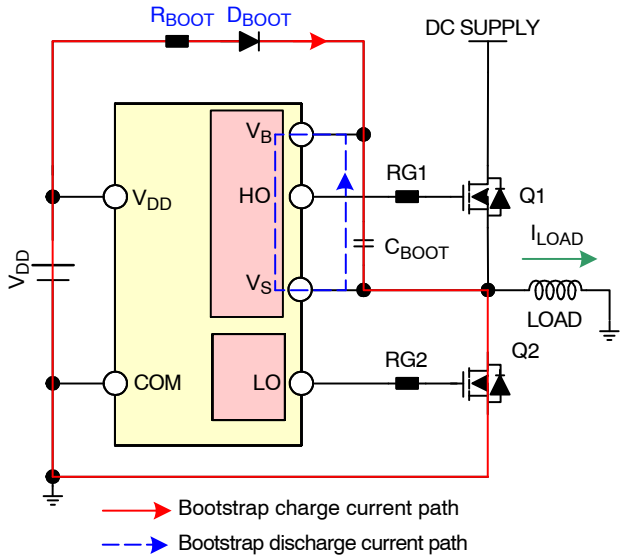


Figure 2. Bootstrap Power Supply Circuit

Drawback of Bootstrap Circuitry

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations.

Duty−cycle and on time is limited by the requirement to refresh the charge in the bootstrap capacitor, C_{BOOT}.

The biggest difficulty with this circuit is that the negative voltage present at the source of the switching device during turn−off causes load current to suddenly flow in the low−side freewheeling diode, as shown in Figure 3.

This negative voltage can be trouble for the gate driver's output stage because it directly affects the source V_S pin of the driver or PWM control IC and might pull some of the internal circuitry significantly below ground, as shown in Figure 4. The other problem caused by the negative voltage transient is the possibility to develop an over−voltage condition across the bootstrap capacitor.

The bootstrap capacitor, C_{BOOT}, is peak charged by the bootstrap diode, D_{BOOT}, from V_{DD} the power source.

Since the V_{DD} power source is referenced to ground, the maximum voltage that can build on the bootstrap capacitor is the sum of V_{DD} and the amplitude of the negative voltage at the source terminal.

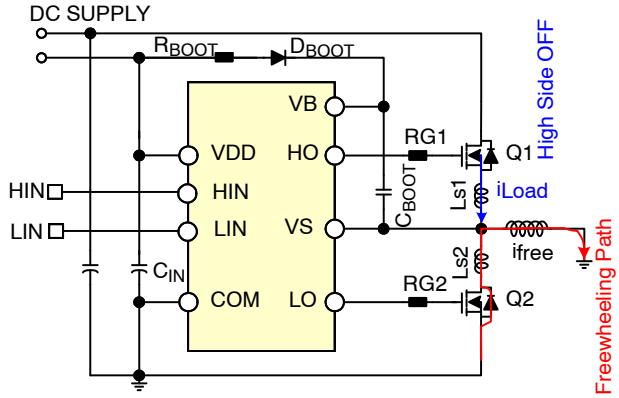


Figure 3. Half−Bridge Application Circuits

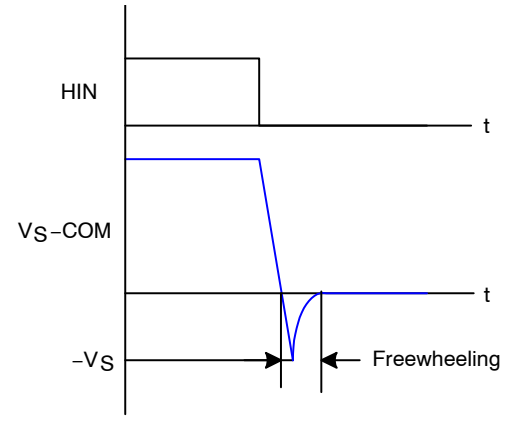


Figure 4. V_S Waveforms During Turn−off

Cause of Negative Voltage on V_S Pin

A well−known event that triggers V_S go below COM (ground) is the forward biasing of the low−side freewheeling diode, as shown in Figure 5.

Major issues may appear during commutation, just before the freewheeling diode starts clamping.

In this case, the inductive parasitic elements, LS1 and LS2, may push V_S below COM, more than as described above or normal steady−state condition.

The amplitude of negative voltage is proportional to the parasitic inductances and the turn−off speed, di/dt, of the switching device; as determined by the gate drive resistor, R_{GATE}, and input capacitance, C_{iss}, of switching device.

It is sum of C_{gs} and C_{gd}, called Miller capacitance.

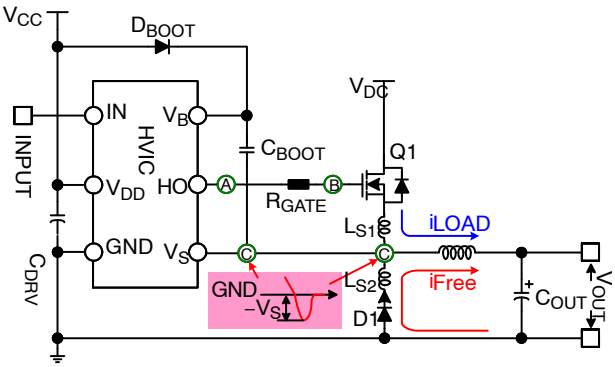


Figure 5. Step−Down Converter Applications

Figure 6 shows the waveforms of the high−side, N−channel MOSFET during turn−off.

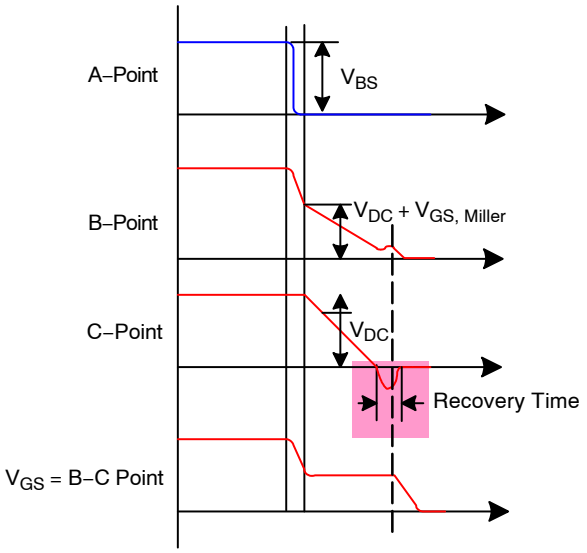


Figure 6. Waveforms During Turn−off

Effects in the Undershoot Spike on V_S Pin

If undershoot exceeds the absolute maximum rating specified in the datasheet, the gate drive IC suffers damage or the high−side output is temporarily unresponsive to input transition as shown in Figure 7 and Figure 8.

Figure 7 shows Latch−up case that the high−side output does not changed by input signal. In this case, short−circuit condition occur on external, main, high−side and low−side switches in half−bridge topology.

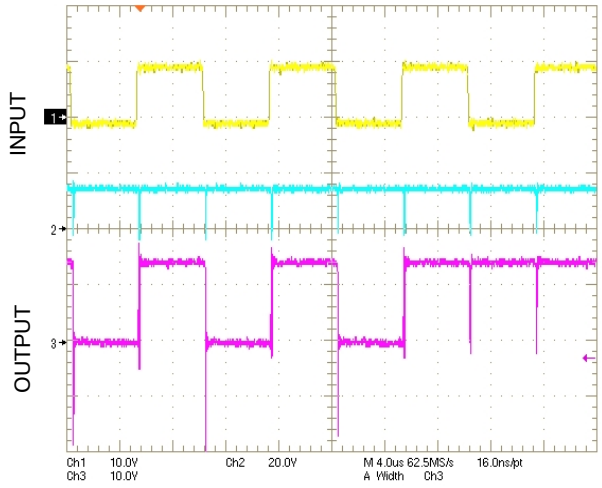


Figure 7. Waveforms in Case of Latch−up

Figure 8 shows Missing case that the high−side output does not responded to input transition. In this case, the level shifter of the high−side gate driver suffers form a lack of the operation voltage headroom. This should be noted, but proves trivial in most applications, as the high−side in not usually required to change state immediately following a switching event.

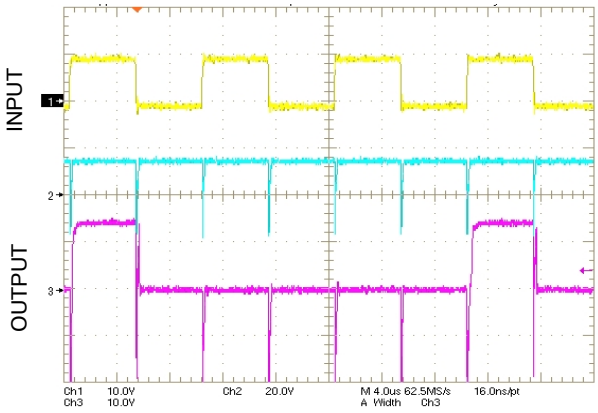


Figure 8. Waveforms in Case of Signal Missing

Consideration of Latch−up Problem

The most integrated high−voltage gate−drive ICs have parasitic diodes, which, in forward or reverse break−down, may cause parasitic SCR latch−up. The ultimate outcome of latch−up often defies prediction and can range from temporary erratic operation to total device failure. The gate−drive IC may also be damaged indirectly by a chain of events following initial overstress. For example, latch−up could conceivably result in both output drivers assuming a HIGH state, causing cross−conduction followed by switch failure and, finally, catastrophic damage to the gate−drive IC. This failure mode should be considered a possible root−cause, if power transistors and/or gate−drive IC are destroyed in the application. The following theoretical extremes can be used to help explain the relationships between excessive V_S undershoot and the resulting latch−up mechanism.

In the first case, an “ideal bootstrap circuit” is used in which V_{DD} is driven from a zero−ohm supply with an ideal diode feed V_B, as shown in Figure 9. When the high current flowing through freewheeling diode, V_S voltage is below ground level by high di/dt. This time, latch−up risk appears since internal parasitic diode, D_{BS} of the gate driver ultimately enters conduction from V_S to V_B, causing the undershoot voltage to sum with V_{DD}, causing the bootstrap capacitor to overcharge, as shown Figure 10.

For example, if V_{DD} = 15 V, then V_S undershoot in excess of 10 V forces the floating supply above 25 V, risking breakdown in diode D_{BS} and subsequent latch−up.

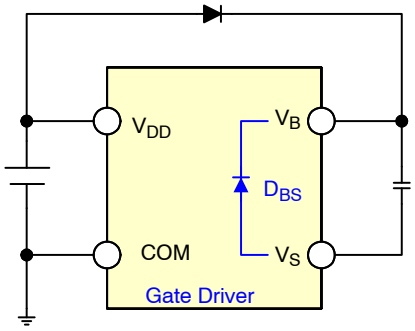


Figure 9. Case 1: Ideal Bootstrap Circuits

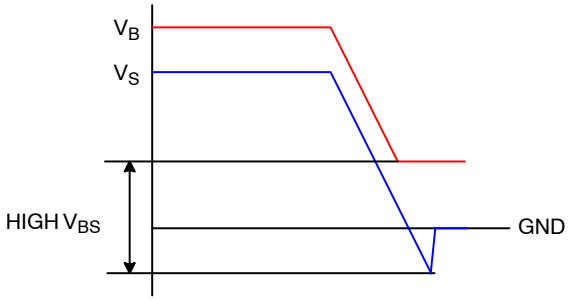


Figure 10. VB and VS Waveforms of Case 1

Suppose that the bootstrap supply is replaced with the ideal floating supply, as shown in Figure 11, such that V_{BS} is fixed under all circumstances. Note that using a low impedance auxiliary supply in place of a bootstrap circuit can approach this situation. This time, latch−up risk appears if V_S undershoot exceeds the V_{BS} maximum specified in datasheet, since parasitic diode D_{BCOM} ultimately enters conduction from COM to V_B, as shown in Figure 12.

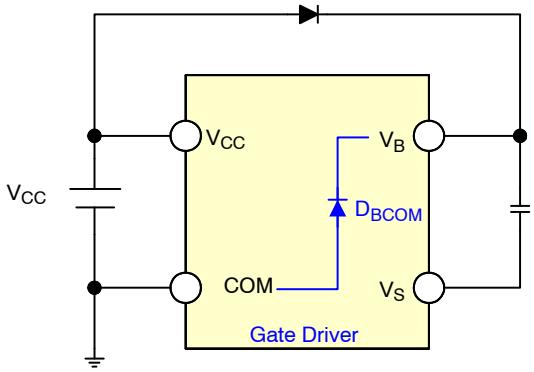


Figure 11. Case 2: Ideal Floating Supply

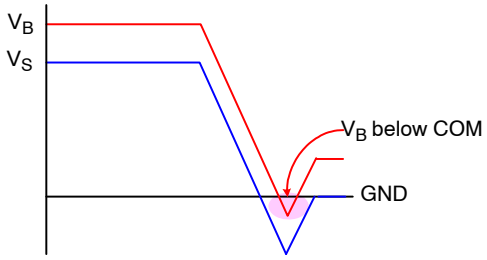


Figure 12. V_B and V_S Waveforms of Case 2

A practical circuit is likely to fall somewhere between these two extremes, resulting in both a small increase of V_{BS} and some V_B droop below V_{DD}, as shown in Figure 13.

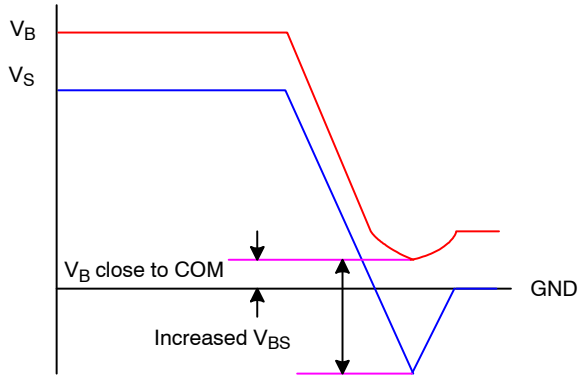


Figure 13. Typical Response of V_B and V_S

Exactly which of the two extremes is prevalent can be checked as follows. If the V_S pins undershoot spike has a time length that is on order of tenths of nanoseconds; the bootstrap capacitor, C_{BOOT}, can become overcharged and the high−side gate−driver circuit has damage by over−voltage stress because it exceeds an absolute maximum voltage (V_{BSMAX}) specified in datasheet. Design to a bootstrap circuit, that does not exceed the absolute maximum rating of high−side gate driver.

Effect of Parasitic Inductances

The amplitude of negative voltage is:

$$V_S - COM = V_{FD1} - L_{S2} \times \frac{dI}{dt} \qquad \text{(eq. 1)}$$

To reduce the slope of current flowing in the parasitic inductances to minimize the derivative terms in Equation 1.

For example, if L/S MOSFET is FCP20N60, the negative voltage spike between V_S and ground is about −21 V in given condition such as 0.2 A/ns dI/dt, 100 nH Parasitic inductance (L_{S2}) and 10 A peak current of freewheeling. Actually, 0.7~0.9 V forward drop (V_{FD1}) at 10 A forward current of body diode in FCP20N60 is negligeable.

DESIGN PROCEDURE OF BOOTSTRAP COMPONENTS

Select the Bootstrap Capacitor

The bootstrap capacitor (C_{BOOT}) is charged every time the low−side driver is on and the output pin is below the supply voltage (V_{DD}) of the gate driver. The bootstrap capacitor is discharged only when the high−side switch is turned on. This bootstrap capacitor is the supply voltage (V_{BS}) for the high circuit section. The first parameter to take into account is the maximum voltage drop that we have to guarantee when the high−side switch is in on state. The maximum allowable voltage drop (V_{BOOT}) depends on the minimum gate drive voltage (for the high−side switch) to maintain. If V_{GSMIN} is the minimum gate−source voltage, the capacitor drop must be:

$$V_{BOOT} = V_{DD} - V_F - V_{GSMIN} \quad \text{(eq. 2)}$$

where:
V_{DD} = Supply voltage of gate driver [V]; and
V_F = Bootstrap diode forward voltage drop [V]

The value of bootstrap capacitor is calculated by:

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} \quad \text{(eq. 3)}$$

where Q_{TOTAL} is the total amount of the charge supplied by the capacitor.

The total charge supplied by the bootstrap capacitor is calculated by equation 4.:

$$Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE}) \times t_{ON} + Q_{LS} \quad \text{(eq. 4)}$$

where:
Q_{GATE} = Total gate charge;
I_{LKGS} = Switch gate−source leakage current;
I_{LKCAP} = Bootstrap capacitor leakage current;
I_{QBS} = Bootstrap circuit quiescent current;
I_{LK} = Bootstrap circuit leakage current;
Q_{LS} = Charge required by the internal level shifter, which is set to 3 nC for all HV gate drivers;
t_{ON} = High−side switch on time; and $I_{LKDIODED}$ = Bootstrap diode leakage current.

The capacitor leakage current is important only if an electrolytic capacitor is used; otherwise, this can be neglected.

For example: Evaluate the bootstrap capacitor value when the external bootstrap diode used.

- Gate Drive IC = FAN7382 (ON Semiconductor)
- Switching Device = FCP20N60 (ON Semiconductor)
- Bootstrap Diode = UF4007
- V_{DD} = 15 V
- Q_{GATE} = 98 nC (Maximum)
- I_{LKGS} = 100 nA (Maximum)
- I_{LKCAP} = 0 (Ceramic Capacitor)
- I_{QBS} = 120 μA (Maximum)
- I_{LK} = 50 μA (Maximum)
- Q_{LS} = 3 nC
- T_{ON} = 25 μs (Duty = 50% at f_s = 20 KHz)
- $I_{LKDIODE}$ = 10 μA

If the maximum allowable voltage drop on the bootstrap capacitor is 1.0 V during the high side switch on state, the minimum capacitor value is calculated by Equation 3.

$$Q_{Total} = (98x10^{-9}) + (100x10^{-9} + 120x10^{-6} + 50x10^{-6} + 10x10^{-6}) \times (25x10^{-6}) + (3x10^{-9}) = 105.5x10^{-9}[C] \quad \text{(eq. 5)}$$

The value of bootstrap capacitor is calculated as follows:

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{105.5x10^{-9}}{1} \cong 106[nF] \quad \text{(eq. 6)}$$

The voltage drop due to the external diode is nearly 0.7 V. Assume the capacitor charging time is equal to the high−side on−time (duty cycle 50%). According to different bootstrap capacitor values, the following equation applies:

$$\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}}$$

$$100\ nF \Rightarrow \Delta V_{BOOT} = 1.06[V]$$
$$150\ nF \Rightarrow \Delta V_{BOOT} = 0.7[V] \quad \text{(eq. 7)}$$
$$220\ nF \Rightarrow \Delta V_{BOOT} = 0.48[V]$$
$$570\ nF \Rightarrow \Delta V_{BOOT} = 0.19[V]$$

Suggested values are within the range of 100 nF ~ 570 nF, but the right value must be selected according to the application in which the device is used. When the capacitor value is too large, the bootstrap charging time slows and the low−side on time might be not long enough to reach the bootstrap voltage.

Select the Bootstrap Resistor

When the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop:

$$V_{RBOOT} = \frac{I_{CHARGE} \times R_{BOOT}}{t_{CHARGE}} \quad \text{(eq. 8)}$$

where:
I_{CHARGE} = Bootstrap capacitor charging current;
R_{BOOT} = Bootstrap resistance; and
t_{CHARGE} = Bootstrap capacitor charging time (the low−side turn−on time).

Do not exceed the ohms (typically 5~10 Ω) that increase the V_{BS} time constant. This voltage drop of bootstrap diode must be taken into account when the maximum allowable voltage drop (V_{BOOT}) is calculated. If this drop is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra−fast recovery diode can be used.

CONSIDERATION OF BOOTSTRAP APPLICATION CIRCUITS

Bootstrap Startup Circuit

The bootstrap circuit is useful in high−voltage gate driver, as shown in Figure 1. However, it has a initial startup and limited charging a bootstrap capacitor problem when the source of the main MOSFET (Q1) and the negative bias node of bootstrap capacitor (C_{BOOT}) are sitting at the output voltage. Bootstrap diode (D_{BOOT}) might be reverse biased at startup and main MOSFET (Q1) has a insufficient turn−off time for the bootstrap capacitor to maintain a required charge, as shown in Figure 1.

In certain applications, like in battery chargers, the output voltage might be present before input power is applied to the converter. Delivering the initial charge to the bootstrap capacitor (C_{BOOT}) might not be possible, depending on the potential difference between the supply voltage (V_{DD}) and output voltage (V_{OUT}) levels. Assuming there is enough voltage differential between input voltage (V_{DC}) and output voltage (V_{OUT}), a circuit comprised of startup resistor (R_{START}), startup diode (D_{START}), and Zener diode (D_Z) can solve the problem, as shown in Figure 14. In this startup circuit, startup diode D_{START} serves as a second bootstrap diode used for charging the bootstrap capacitor (C_{BOOT}) at power up. Bootstrap capacitor (C_{BOOT}) is charged to the Zener diode of D_Z, which is supposed to be higher than the driver's supply voltage (V_{DD}) during normal operation. The charge current of the bootstrap capacitor and the Zener current are limited by the startup resistor. For best efficiency, the value of startup resistor should be selected to limit the current to a low value, since the bootstrap path through the startup diode is permanently in the circuit.

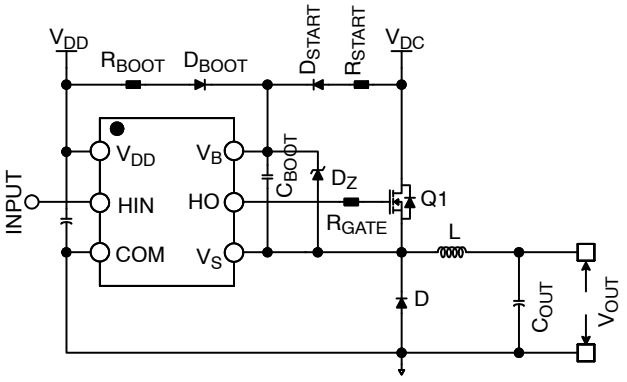


Figure 14. Simple Bootstrap Startup Circuit

Resistor in Series with Bootstrap Diode

In the first option, the bootstrap circuit includes a small resistor, R_{BOOT}, in series with bootstrap diode, as shown in Figure 15. The bootstrap resistor, R_{BOOT}, provides current limit only during a bootstrap charging period which represents when the V_S goes below the IC supply voltage, V_{CC}, or is pulled down to ground (the low−side switch is turned on and the high−side switch is turned off). The bootstrap capacitor, C_{BOOT}, charge through the bootstrap resistor, R_{BOOT}, and diode, D_{BOOT}, from the V_{CC} power supply. The bootstrap diode must have a break−down voltage (BV) larger than V_{DC} and a fast recovery time to minimize the amount charge feedback from the bootstrap capacitor to V_{CC} power supply.

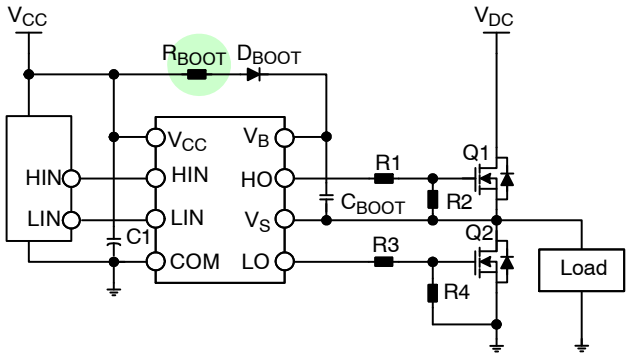


Figure 15. Adding a Series Resistor with DBOOT

This method has the advantage of being simple for limiting the current when the bootstrap capacitor is initially charged, but it has some limitations. Duty−cycle is limited by the requirement to refresh the charge in the bootstrap capacitor, C_{BOOT}, and there are startup problems. Do not exceed the ohms (typically 5~10 Ω) that would increase the V_{BS} time constant. The minimum on−time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time constant. The time constant depends on the values of bootstrap resistance, capacitance, and duty cycle of switching device calculated in following equation:

$$\tau = \frac{R_{BOOT} \times C_{BOOT}}{D} [s] \qquad \text{(eq. 9)}$$

where R_{BOOT} is the bootstrap resistor; C_{BOOT} is the bootstrap capacitor; and D is the duty cycle.

$$\tau = \frac{R_{BOOT} \times C_{BOOT}}{D} = \frac{10x1^{-6}}{0.1} = 100\ [\mu s] \qquad \text{(eq. 10)}$$

Even with a reasonably large bootstrap capacitor and resistor, the time constant may be large. This method can mitigate the problem. Unfortunately, the series resistor does not provide a foolproof solution against an over voltage and it slows down the recharge process of the bootstrap capacitor.

Resistor Between V_S and V_{OUT}

In the second option, the bootstrap circuit includes a small resistor, R_{VS}, between V_S and V_{OUT}, as shown in Figure 16. Suggested values for R_{VS} are in the range of some ohms.

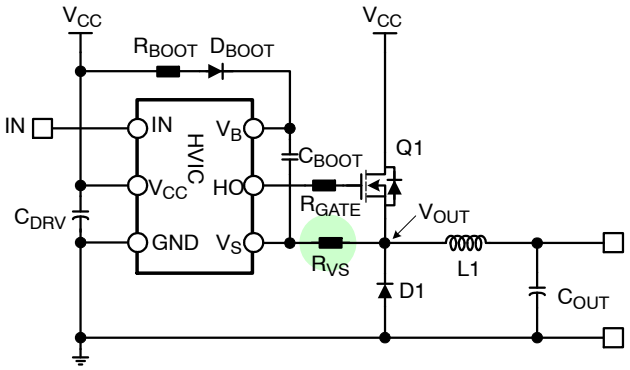


Figure 16. Adding Rvs in Bootstrap Circuit

The R_{VS} works as, not only bootstrap resistor, but also turn−on and turn−off resistors, as shown in Figure 17. The bootstrap resistor, turn−on, and turn−off resistors are calculated by the following equations:

$$R_{BOOT}{}^{*} = R_{BOOT} + R_{VS} \quad \text{(eq. 11)}$$

$$R_{ON}{}^{*} = R_{GATE} + R_{VS} \quad \text{(eq. 12)}$$

$$R_{OFF}{}^{*} = R_{GATE} + R_{VS} \quad \text{(eq. 13)}$$

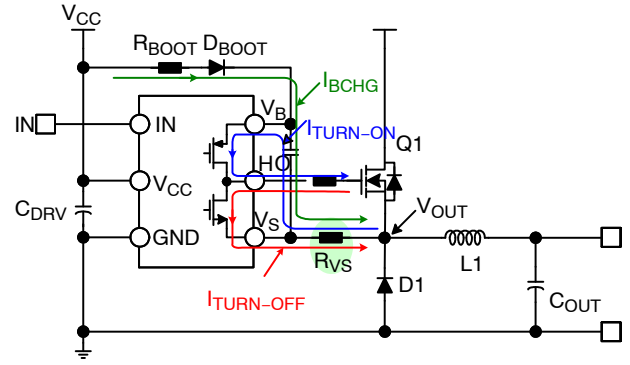


Figure 17. Current Paths of Turn−on and Turn−off

Clamping Diode for V_S and Relocation Gate Resistor

In the third option, the bootstrap relocates a gate resistor between V_S and V_{OUT} and adds a low forward−voltage drop Schottky diode from ground to V_S, as shown in Figure 18. The difference between V_B and V_S should be kept inside the absolute maximum specification in the datasheet and must be satisfied by the following equation:

$$V_B - V_S < V_{BS\_abs\ max} \quad \text{(eq. 14)}$$

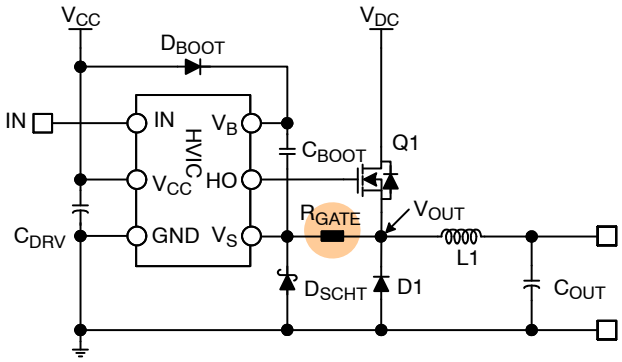


Figure 18. Clamping Structure

Relocated Gate Resistor; Double Purpose

The gate resistor sets the turn−on and turn−off speeds in the MOSFET and provides current limiting for the Schottky diode during the negative voltage transient of the source terminal of the main switch. In additional, the bootstrap capacitor is protected against over voltage by the two diodes connected to the ends of C_{BOOT}. The only potential hazard by this circuit is that the charging current of the bootstrap capacitor must go through gate resistor. The time constant of C_{BOOT} and R_{GATE} slows the recharge process, which might be a limiting factor as the PWM duty cycle.

The fourth options includes relocating a gate resistor between V_S and V_{OUT} and a clamp device should be positioned between ground and V_S, as shown in Figure 19, where a Zener diode and a 600 V diode are placed. The Zener voltage must be sized according to the following rule:

$$V_B - V_S < V_{BS,\ ABSMAX} \quad \text{(eq. 15)}$$

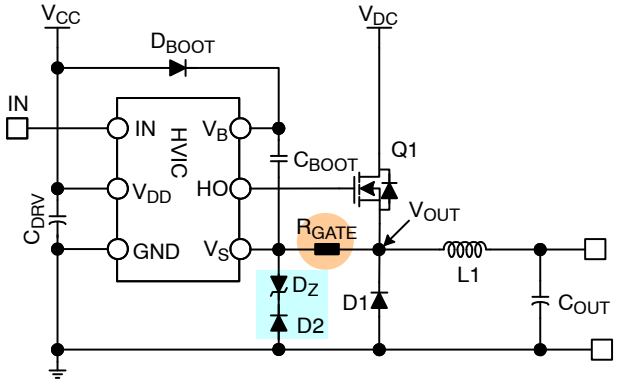


Figure 19. Clamping Structure with Zener Diode

CHOOSE CURRENT CAPABILITY HVIC

The approximate maximum gate charge Q_G that can be switched in the indicated time for each driver current rating is calculated in Table 1:

Table 1. EXAMPLE HVIC CURRENT−DRIVE CAPABILITY

Needed Current Rating	Switching Time ($t_{SW\_ON/OFF}$)	
	100 ns	50 ns
	Maximum Gate Charge ($Q_{G,MAX}$)	
2 A	133 nC	67 nC
4 A	267 nC	133 nC
9 A	600 nC	300 nC

1. For a single 4 A, parallel the two channels of a dual 2 A!

For example, a switching time of 100 ns is:
1 % of the converter switching period at 100 KHz;
3 % of the converter switching period at 300 KHz; etc.

1. Needed gate driver current ratings depend on what gate charge Q_G must be moved in switching time $t_{SW−ON/OFF}$ (because average gate current during switching is I_G):

$$I_{G.AV.SW} = \frac{Q_G}{T_{sw\_on\ /\ off}} \quad \text{(eq. 16)}$$

2. The maximum gate charge, Q_G, is read from the MOSFET datasheet

If the actual gate−drive voltage V_{GS} is different from the test condition in the specifications table, use the V_{GS} vs. Q_G curve instead. Multiply the datasheet value by the number of MOSFETs in parallel.

3. $t_{SW\_ON/OFF}$ is how fast the MOSFET should be switched. If unknown, start with 2% of the switching period t_{SW}:

$$t_{SWON,\ OFF} = 0.02 \times t_{SW} = \frac{0.02}{f_{SW}} \quad \text{(eq. 17)}$$

If channel (V−I) switching loss is dominated by one switching transition (turn−on or turn−off), size the driver for that transition. For clamped inductive switching (the usual case), channel switching loss for each transition is estimated as:

$$E_{SW} = 0.5\ V_{DS} \times I_D \times t_{SW}\ [\text{Joules}] \quad \text{(eq. 18)}$$

where V_{DS} and I_D are maximum values during the switching interval.

4. The approximate current drive capability of gate driver may be calculated like below
   a. Sourcing Current Capability (Turn−on):

$$I_{SOURCE} \geq 1.5 \times \frac{Q_G}{t_{SW,\ ON}} \quad \text{(eq. 19)}$$

   b. Sinking Current Capability (Turn−off)

$$I_{SINK} \geq 1.5 \times \frac{Q_G}{t_{SW,\ OFF}} \quad \text{(eq. 20)}$$

where:
Q_G = MOSFET gate charge at $V_{GS} = V_{DD}$;
$t_{SW\_ON/OFF}$ = MOSFET switch turn−on / turn−off time;
and 1.5 = empirically determined factor (influenced by delay through the driver input stages and parasitic elements).

GATE RESISTOR DESIGN PROCEDURE

The switching speed of the output transistor can be controlled by values of turn−on and turn−off gate resistors controlling the turn−on and turn−off current of gate driver. This section describes basic rules for values of the gate resistors to obtain the desired switching time and speed by introducing the equivalent output resistor of the gate driver. Figure 20 shows the equivalent circuit of gate driver and current flow paths during the turn−on and turn−off, including a gate driver and switching devices.

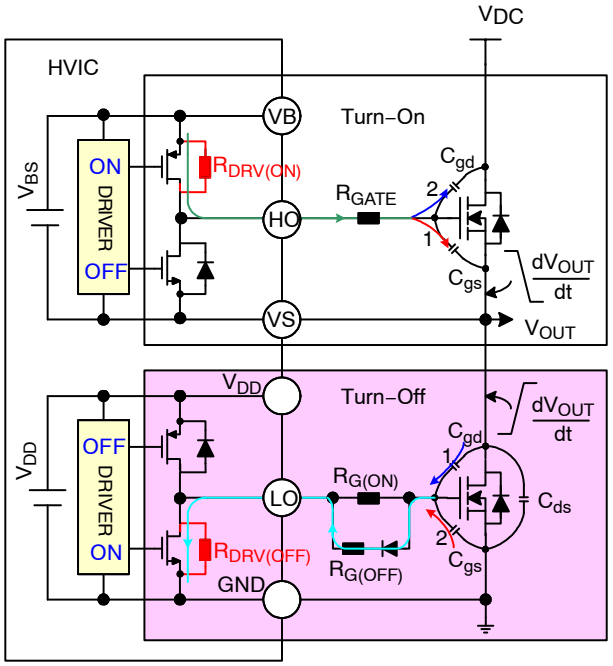


Figure 20. Gate Driver Equivalent Circuit

Figure 21 shows the gate−charge transfer characteristics of switching device during turn−on and turn−off.

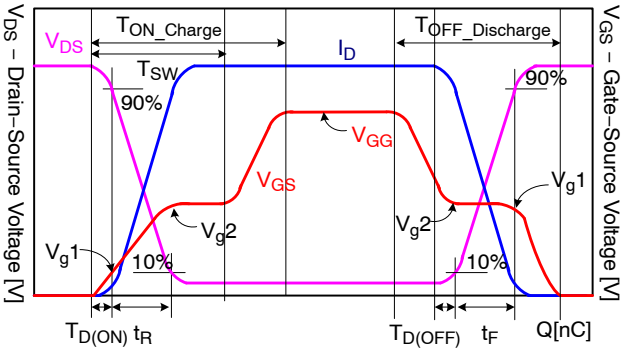


Figure 21. Gate Charge Transfer Characteristics

Sizing the Turn−On Gate Resistor

Turn−on gate resistor, $R_{g(ON)}$, can be chosen to obtain the desired switching time by using switching time, t_{sw}. To determine a value of resistor using the switching time, supply voltage, V_{DD} (or V_{BS}), equivalent on resistance ($R_{DRV(ON)}$) of the gate driver, and switching device parameters (Q_{gs}, Q_{gd}, and $V_{gs(th)}$) are needed.

The switching time is defined as the time spent to reach the end of the plateau voltage (a total Q_{gd} + Q_{gd} has been provided to the MOSFET gate), as shown in Figure 21.

The turn−on gate resistor calculated as follows:

$$I_{g(avr)} = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \quad \text{(eq. 21)}$$

$$R_{TOTAL} = R_{g(ON)} + T_{DRV(ON)} = \frac{V_{DD} + V_{gs}}{Ig(avr)} \quad \text{(eq. 22)}$$

where $R_{g(ON)}$ is the gate on resistance and $R_{DRV(ON)}$ is the driver equivalent on resistance.

Output Voltage Slope

Turn−on gate resistor $R_{g(ON)}$ can be determined by control output slope (dV_{OUT}/dt). While the output voltage has a non−linear behavior, the maximum output slope can be approximated by:

$$\frac{dV_{OUT}}{dt} = \frac{I_{g(avr)}}{C_{gd(off)}} \quad \text{(eq. 23)}$$

Inserting the expression yielding $I_{g(avr)}$ and rearranging:

$$R_{TOTAL} = \frac{V_{DD} - V_{gs(th)}}{C_{gd(off)} \times \frac{dV_{OUT}}{dt}} \quad \text{(eq. 24)}$$

where $C_{gd(off)}$ is the Miller effect capacitor, specified as C_{rss} in the datasheet.

Sizing the Turn−Off Gate Resistor

The worst case in sizing the turn−off resistor is when the drain of the MOSFET in turn−off state is forced to commutate by external events.

In this case, dV/dt of the output node induces a parasitic current through C_{gd} flowing in $R_{G(OFF)}$ and $R_{DRV(OFF)}$, as shown in Figure 22.

The following describes how to size the turn−off resistor when the output dv/dt is caused by the companion MOSFET turning−on, as shown in Figure 22.

For this reason, the off−resistance must be sized according to the application worst case. The following equation relates the MOSFET gate threshold voltage to the drain dv/dt:

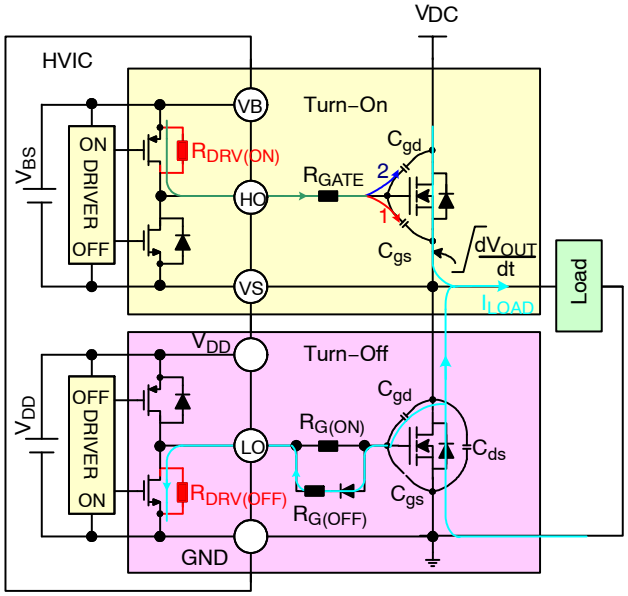


Figure 22. Current Paths: Low−Side Switch Turned Off, High−Side Switch Turned On

$$V_{gs(th)} \geq \left\{(R_{g(OFF)} + R_{DRV(OFF)}) \times i_g\right\} = \left\{(R_{g(OFF)} + R_{(drv)} \times C_{gd}\frac{dV_{out}}{dt}\right\} \quad \text{(eq. 25)}$$

Rearranging the equation yields:

$$R_g(off) \leq \frac{V_{gs(th)}}{C_{gd} \times \frac{dV_{out}}{dt}} - R_{(drv)} \quad \text{(eq. 26)}$$

Design Example

Determine the turn−on and off gate resistors using the ON Semiconductor MOSFET with FCP20N60 and gate driver with FAN7382. The power MOSFET of FCP20N60 parameters are as follows:

$$Q_{gs} = 13.5\ nC,\ Q_{gd} = 36\ nC,\ C_{gd} = 95pF,\ V_{GS(th)} = 5\ V,\ V_{GS(th)MIN} = 3\ V \quad \text{(eq. 27)}$$

Turn−On Gate Resistance

1. If the desired switching time is 500 ns at V_{DD} = 15 V, the average gate charge current is calculated as:

$$I_{g(avr)} = \frac{Q_{gs} + Q_{gd}}{t_{SW}} = \frac{36\ nC + 13.5\ nC}{500}\ ns = 99\ [mA] \quad \text{(eq. 28)}$$

$$R_{Total} = \frac{V_{DD} + V_{gs(th)}}{I_{g(avr)}} = \frac{15 - 5}{99\ mA} = 101\ [\Omega] \quad \text{(eq. 29)}$$

$$R_{DRV(ON)} = \frac{V_{DD}}{I_{SOURCE}} = \frac{15\ V}{350\ mA} = 43\ [\Omega] \quad \text{(eq. 30)}$$

The turn−on resistance value is about 58 Ω.

2. If dV_{out}/dt = 1 V/ns at V_{DD} = 15 V, the total gate resistor is as calculated as:

$$R_{Total} = \frac{V_{DD} - V_{GS(th)}}{C_{gd(off)} \times \frac{dV_{out}}{dt}} = \frac{15 - 5}{95x10^{-12}x10^{9}} \quad \text{(eq. 31)}$$

$$R_{DRV(ON)} = \frac{V_{DD}}{I_{SOURCE}} = \frac{15\ V}{350\ mA} = 43\ [\Omega] \quad \text{(eq. 32)}$$

The turn−on resistance value is about 62 Ω.

Turn−Off Gate Resistance

If dV_{out}/dt=1 V/ns, the turn−off gate resistor is calculated as:

$$R_{DRV(OFF)} = \frac{V_{DD}}{I_{SINK}} = \frac{15\ V}{650\ mA} \approx 23[\Omega] \quad \text{(eq. 33)}$$

$$R_{g(off)} \leq \frac{V_{gs(th)min}}{C_{gd} \times \frac{dV_{out}}{dt}} - R_{(drv)} = \frac{3}{95x10^{-12}x10^{9}} - 23 = 8.6 \quad \text{(eq. 34)}$$

POWER DISSIPATION CONSIDERATIONS

Gate Driver Power Dissipation

The total power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are comprised of the static and dynamic losses related to the switching frequency, output load capacitance on high− and low−side drivers, and supply voltage, V_{DD}.

The static losses are due to the quiescent currents from the voltage supplies V_{DD} and ground in low−side driver and the leakage current in the level shifting stage in high−side driver, which are dependent on the voltage supplied on the V_S pin and proportional to the duty cycle when only the high−side power device is turned on.

The dynamic losses are defined as follows: In the low−side driver, the dynamic losses are due to two different sources. One is due to whenever a load capacitor is charged or discharged through a gate resistor, half of energy that goes into the capacitance is dissipated in the resistor. The losses in the gate drive resistance, internal and external to the gate driver, and the switching loss of the internal CMOS circuitry. Also, the dynamic losses of the high−side driver have two different sources. One is due to the level−shifting circuit and one due to the charging and discharging of the capacitance of the high side. The static losses are neglected here because the total IC power dissipation is mainly dynamic losses of gate drive IC and can be estimated as:

$$P_{DGATE} = 2 \times C_L \times f_s \times V_{DD}^2 \text{ [W]} \qquad \text{(eq. 35)}$$

Figure 23 shows the calculated gate driver power dissipation versus frequency and load capacitance at V_{DD} = 15 V. This plot can be used to approximate the power losses due to thegate driver

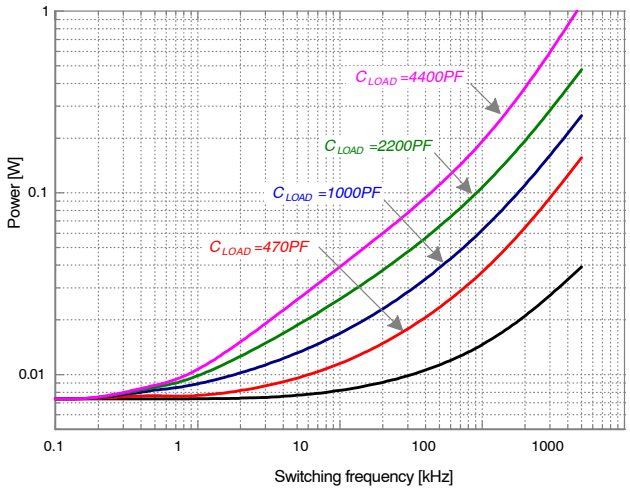


Figure 23. Gate Driver Total Power Dissipation

The bootstrap circuit power dissipation is the sum of the bootstrap diode losses and the bootstrap resistor losses if any exist. The bootstrap diode loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to switching frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor, resulting in more losses.

Higher input voltages (V_{DC}) to the half−bridge result in higher reverse recovery losses. The total IC power dissipation can be estimated by summing the gate driver losses with the bootstrap diode losses, except bootstrap resistor losses.

If the bootstrap diode is within the gate driver, add an external diode in parallel with the internal bootstrap diode because the diode losses can be significant. The external diode must be placed close to the gate driver to reduce parasitic series inductance and significantly lower forward voltage drop.

Package Thermal Resistance

The circuit designer must provide:

- Estimate power dissipation of gate driver package
- The maximum operating junction temperature $T_{J, MAX,OPR}$, e.g., 120 °C for these drivers if derated to 80 % of $T_{J, MAX}$ =150 °C
- Maximum operating lead temperature $T_{L, MAX, OPR}$, approximately equal to the maximum PCB temperature underneath the driver, e.g., 100 °C
- Maximum allowable junction−to−lead thermal resistance is calculated by:

$$\theta_{JL, max} = \frac{T_{J, max} + T_{L, max}}{R_{PKG}} \qquad \text{(eq. 36)}$$

GENERAL GUIDELINES

Printed Circuit Board Layout

The layout for minimized parasitic inductances is as follows:

- Direct tracks between switches with no loops or deviation
- Avoid interconnect links. These can add significant inductance
- Reduce the effect of lead−inductance by lowering package height above the PCB
- Consider co−locating both power switches to reduce track length
- Placement and routing for decoupling capacitor and gate resistors as close as possible to gate drive IC
- The bootstrap diode as close as possible to bootstrap capacitor

Bootstrap Components

The bootstrap resistor (R_{BOOT}) must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM (ground), especially during startup and extremes of frequency and duty cycle.

The bootstrap capacitor (C_{BOOT}) uses a low−ESR capacitor, such as ceramic capacitor. The capacitor from V_{DD} to COM supports both the low−side driver and bootstrap recharge. A value at least ten times higher than the bootstrap capacitor is recommended.

The bootstrap diode must use a lower forward voltage drop and switching time as soon as possible for fast recovery, such as ultra−fast.

Table 2. SUMMARY OF HIGH−SIDE GATE DRIVE CIRCUITRY

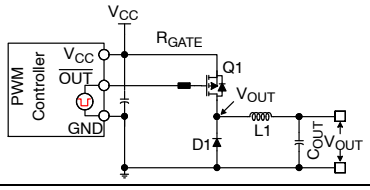
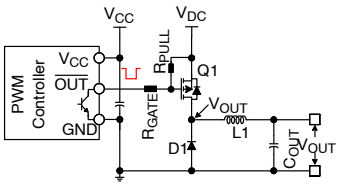
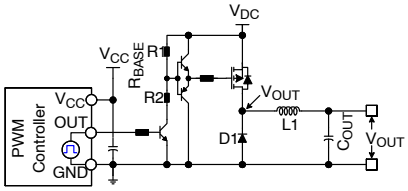
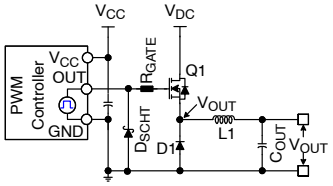
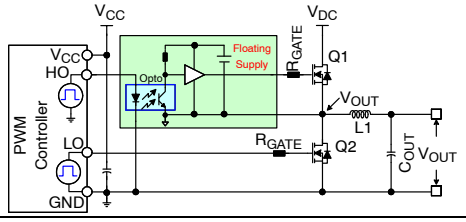
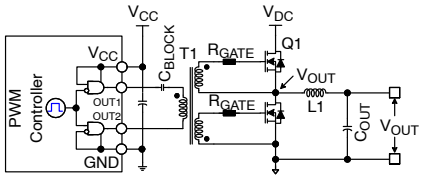
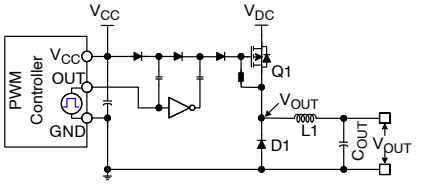
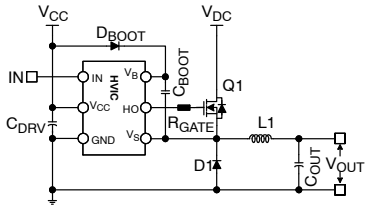
Method	Basic Circuit	Advantages & Limitations
HIGH−SIDE GATE DRIVERS FOR P−CHANNEL		
Direct Drive		Can be implemented if the maximum input voltage is less than the gate−to−source break down voltage of the device
Open Collector		Simple method, but is not suitable for driving MOSFET directly in a high−speed application
Level−Shifted Drive		Suitable for high−speed application and works seamlessly with regular PWM controller
HIGH−SIDE GATE DRIVERS FOR N−CHANNEL		
Direct Drive		Easiest high−side application the MOSFEF and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: $V_{CC} < V_{GS,\ MAX}$ and $V_{DC} < V_{CC} - V_{GS,\ Miller}$
Floating Supply Gate Drive		Cost impact of isolated supply is significant. Opto−coupler tends to be relatively expensive, limited in bandwidth, and noise sensitive

Table 2. SUMMARY OF HIGH−SIDE GATE DRIVE CIRCUITRY (continued)

Method	Basic Circuit	Advantages & Limitations
HIGH−SIDE GATE DRIVERS FOR N−CHANNEL		
Transformer Coupled Drive		Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity
Charge Pump Drive		The turn−on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping
Bootstrap Drive		Simple and inexpensive with limitations; such as, the duty cycle and on−time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties

Consideration Points of Bootstrap Circuit Problem

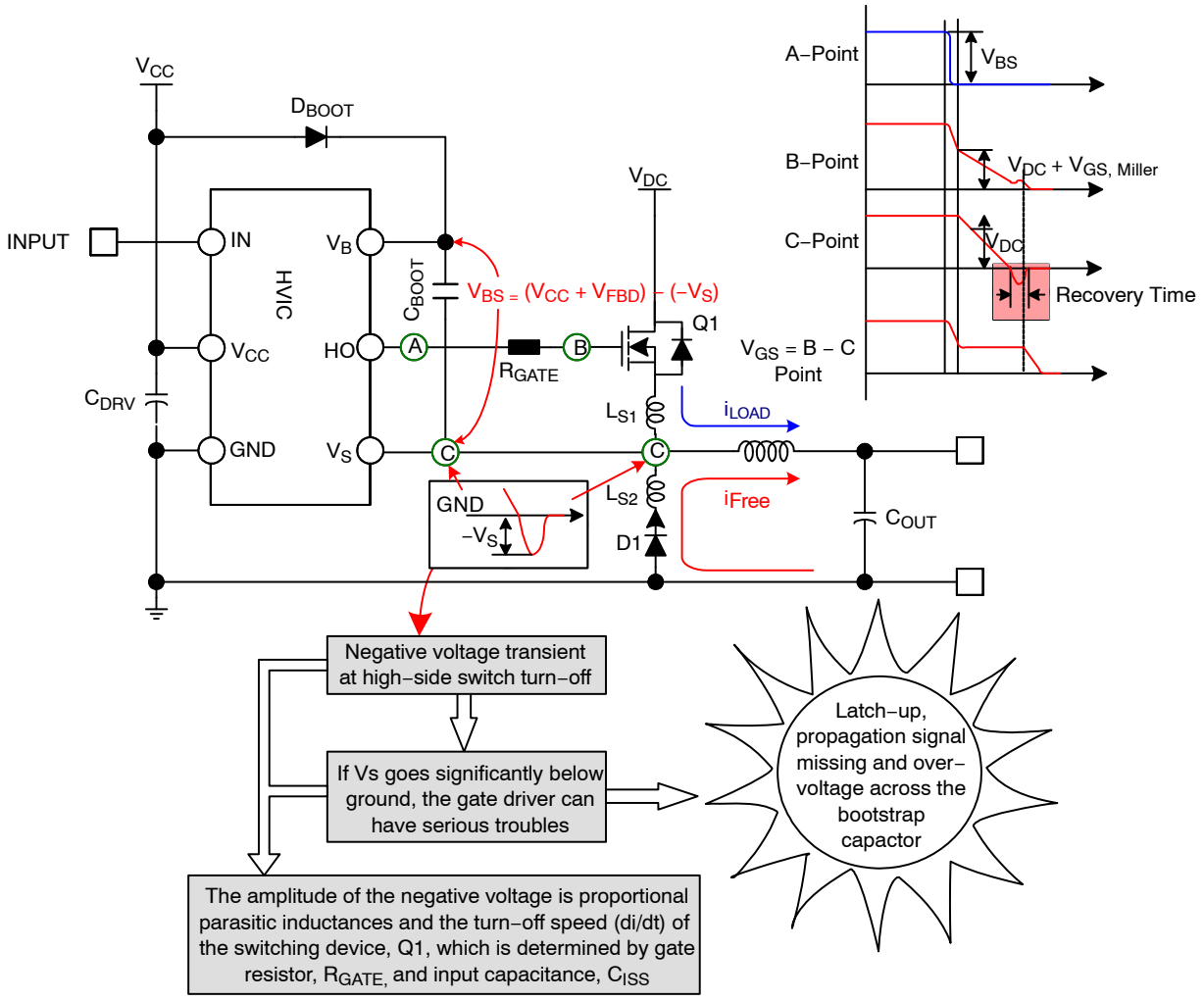


Figure 24.

Remedies of Bootstrap Circuit Problem

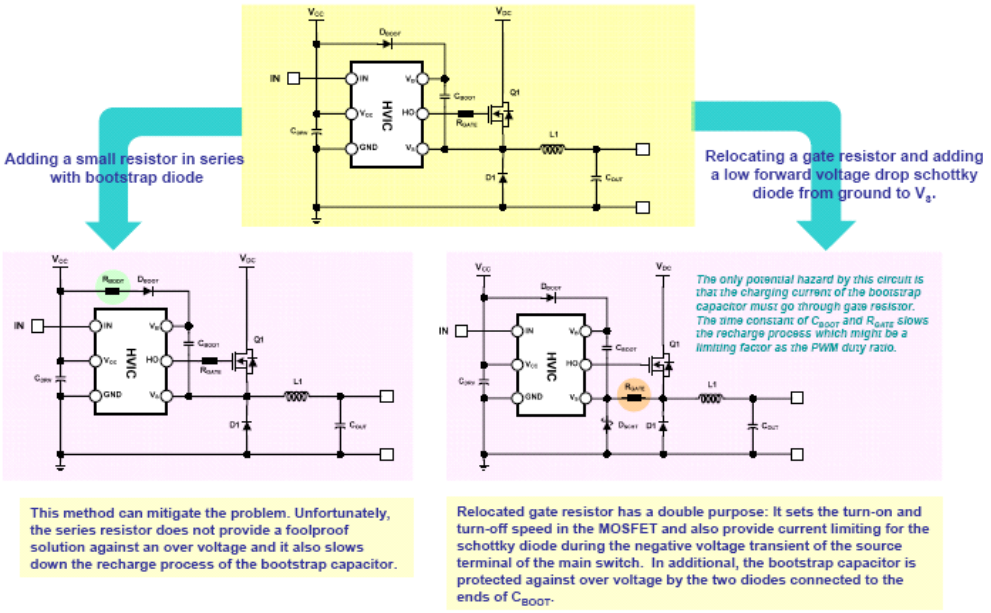


Figure 25.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative