Interface Control Document

SatNOGS COMMS

Version 1.6

Contents

1. Changelog

Version	Date	Changes
1.0	Dec 18, 2023	No Changes
1.1	Dec 29, 2023	No Changes
1.2	Mar 19, 2024	Updates for PCB v0.3.1
1.3	Apr 30, 2024	No Changes
1.4	Nov 05, 2024	No Changes
1.5	Dec 10, 2024	• Merged "Subsystem Interface" section with "Electrical interfaces" • Updated mechanical specifications to include the bottom shield • Updated connector part numbers and pinout, added mating connector parts • Added FPGA SoM documentation • Update Software Interfaces chapter • Added "Environmental Specifications", "Performance Measurements", and "Material List" sections
1.5.1	Dec 10, 2024	Fix static GitLab pipeline
1.5.2	Dec 18, 2024	No changes
1.6		Add more details for RF measurements

1.1 Acronyms

AGC Automatic Gain Control

API Application programming interface

BER Bit Error Rate

BPF Band Pass Filter

CAN Controller Area Network

FPGA Field Programmable Gate Array

GMII Gigabit Media Independent Interface

gRPC gRPC Remote Procedure Calls

HDF5 Hierarchical Data Format

I2C Inter-Integrated Circuit

IC Integrated Circuit

JTAG Joint Test Action Group

LO Local Oscillator

MCU Micro-Controller Unit

PA Power Amplifier

PCB Printed Circuit Board

PDN Power Distribution Network

RF Radio Frequency

RGMII Reduced Gigabit Media-Independent Interface

RSSI Received signal strength indication

SDR Software Defined Radio

SFCG Space Frequency Coordination Group

SMPS Switching Mode Power Supply

SPI Serial Peripheral Interface

TGT Target

UART Universal Asynchronous Receiver Transmitter

UHF Ultra High Frequency

VGA Variable Gain Amplifier

2. Introduction

This Interface Control Document (ICD) defines the interface requirements for integrating SatNOGS COMMS into a CubeSat. In this document, the mechanical interface of the board along with its environmental specifications and materials list are provided. Additionally, the electrical interfaces are described in detail. In particular, the SatNOGS COMMS system included 2 RF interfaces (UHF and S-band), 2 external reference clock interfaces, multiple communication interfaces, and an interface for an FPGA SoM daughter board. For these interfaces, their position on the board along with pinout and other required electrical information are described. Moreover, key performance measurements, such as the power consumption in various operational states, are provided. Finally, the software interfaces of the system are also outlined in this document.

3. Mechanical interface

3.1 Dimensions

PCB dimensions, mounting holes, PC104 connector type and location follow LibreCube [1] standard, with the exception of the height of the bottom EMI shield. The PC104 interface connectors are SAMTEC ESQ-126–39–G-D. A mechanical drawing of the outline and mounting hole locations is shown in Figure 3.1 and the respective one for its side view along with an isometric view is shown in Figure 3.2.

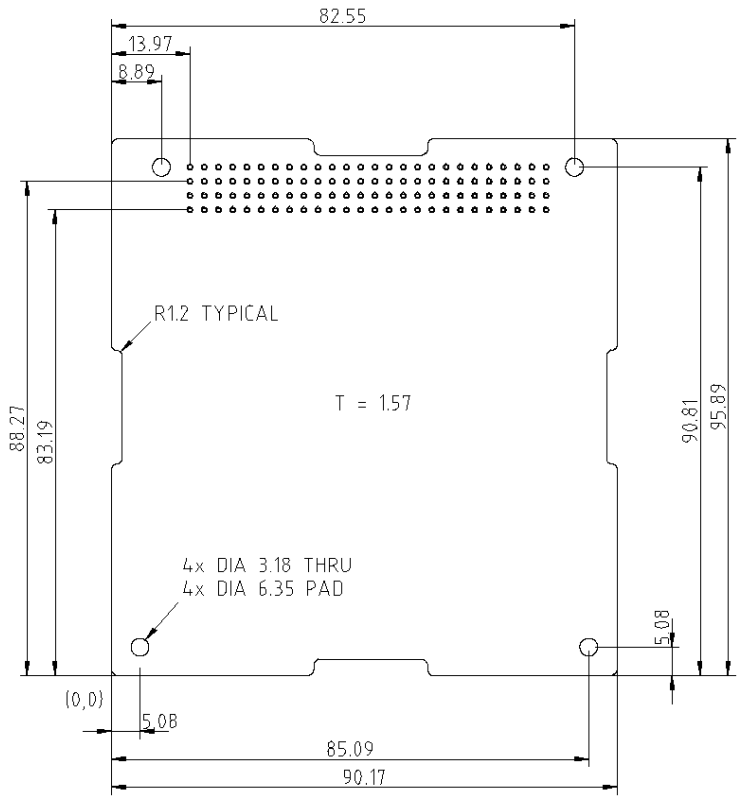

Figure 3.1: LibreCube mechanical drawing (mm)

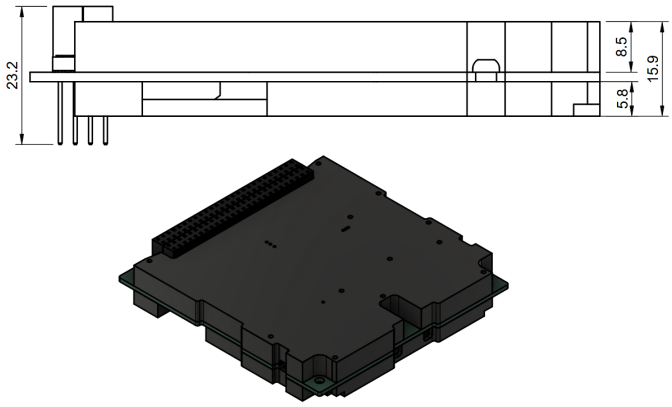

Figure 3.2: Side view dimensions (mm)

3.2 Mass Budget

#	Component	Material	Mass (grams)
1	PCB	FR4 and copper	31.1
2	Passive Components	NA	7.1
3	ICs	NA	16.7
4	Connector	NA	6.0
5	Top Shield	Al 7075	80
6	Bottom Shield	Al 7075	50
7	Screws	A4 Stainless Steel	4.1
		TOTAL	195g ($\pm 10g$)

Table 3.1: Mass Budget Table

4. Electrical Interfaces

4.1 BUS Connector

SatNOGS COMMS connects to a CubeSat bus via a PC–104 connector. The connector type used is the SAMTEC ESQ-126–39–G-D. Regarding pin assignment, it is based on Librecube standard [1]. As far as pin numbering and header naming is concerned, again the Librecube standard is followed and Figure 4.1 contains all necessary information.

For subsystem communication the following interfaces are available on the PC–104 connector:

- Two CAN-FD interfaces backward compatible with CAN-2.0. CAN-FD fulfills interconnect link speed requirements, while subsystems only capable of CAN-2.0 can use SPI for data transfer and CAN-2.0 for control. The CAN transceiver used on SatNOGS COMMS is the TCAN334GDCNT. Additionally, it is possible during the order configuration phase to select whether the 120 Ohm CAN termination resistors will be soldered on SatNOGS COMMS or not. Details about the electrical specifications of the interface can be found in Table 10.3.
- One SPI interface with a maximum link speed of 8Mbps. Details about the electrical specifications of the interface can be found in Table 10.2.
- Two I2C interfaces. Details about the electrical specifications of the interface can be found in Table 10.8.
- Two UART from the MCU. Details about the electrical specifications of the interface can be found in Table 10.7.
- One UART from the FPGA. Details about the electrical specifications of the interface can be found in Table 10.7.

Note that only the CAN interface has been subjected to environmental tests so far.

H2	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46
	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45
H1	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46
	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45

Header	Pin	Name	Description	Nominal Voltage (V)
H1	1	CAN_A_L	CANFD Bus A (Low Signal)	-5 to 5
H1	2	CAN_B_L	CANFD Bus B (Low Signal)	-5 to 5
H1	3	CAN_A_H	CANFD Bus A (High Signal)	-5 to 5
H1	4	CAN_B_H	CANFD Bus B (High Signal)	-5 to 5
H1	5	UART_C_TO_BUS	UART Connected to FPGA-PS	0 to 3.3
H1	6	UART_D_TO_BUS	UART Connected to FPGA-PL	0 to 3.3
H1	7	UART_C_FROM_BUS	UART Connected to FPGA-PS	0 to 3.3
H1	8	UART_D_FROM_BUS	UART Connected to FPGA-PL	0 to 3.3
H1	9	SPI_A_CS	SPI Bus A, Chip Select	0 to 3.3
H1	10	SPI_A_MOSI	SPI Bus A, Controller Out, Peripheral In	0 to 3.3
H1	11	SPI_A_CLK	SPI Bus A, Clock	0 to 3.3
H1	12	SPI_A_MISO	SPI Bus A, Controller In, Peripheral Out	0 to 3.3
H1	13	UART_A_TO_BUS	UART From MCU	0 to 3.3
H1	15	UART_A_FROM_BUS	UART From MCU	0 to 3.3
H1	21	I2C_B_SCL	I2C Bus B, Clock	0 to 3.3
H1	22	UART_B_TO_BUS	UART From MCU	0 to 3.3
H1	23	I2C_B_SDA	I2C Bus B, Data	0 to 3.3
H1	24	UART_B_FROM_BUS	UART From MCU	0 to 3.3
H1	33-34	GND	Ground	0
H1	41	I2C_A_SDA	I2C Bus A, Data	0 to 3.3
H1	43	I2C_A_SCL	I2C Bus A, Clock	0 to 3.3
H2	11	SW2_VBAT	Selectable Input Power	5.5 to 30
H2	12	SW1_VBAT	Selectable Input Power	5.5 to 30
H2	29-30	GND	Ground	0
H2	30-32	GND	Ground	0
H2	45-46	VBAT	Selectable Input Power	5.5 to 30

Figure 4.1: PC104 Pin out

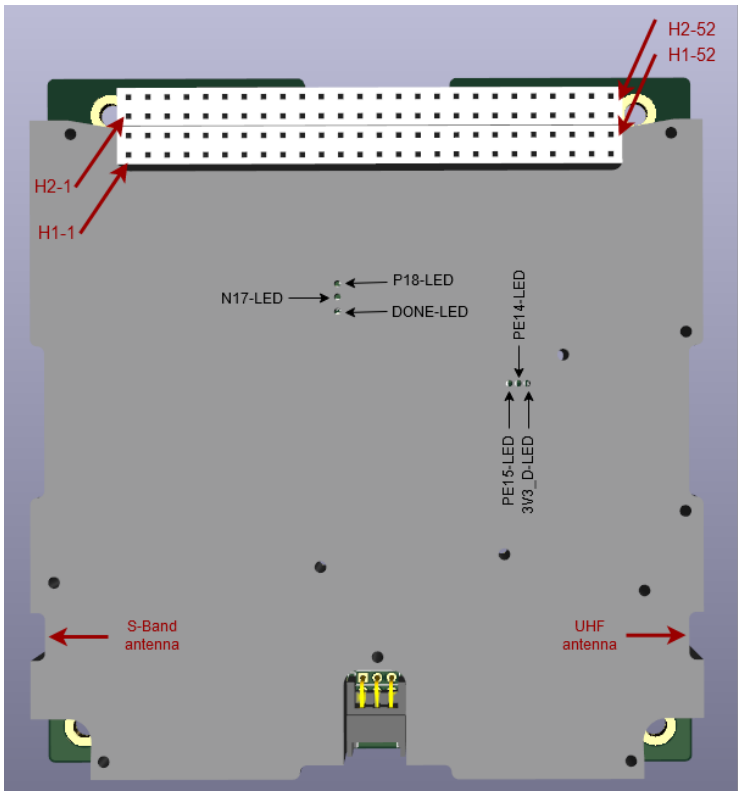

Figure 4.2: PC104, LED and RF connector naming

Regarding the power supply options, one can notice that three options are available. The user can select among those using solder jumpers, which are soldered during the order configuration stage. As mentioned in Figure 4.1, the input voltage range of SatNOGS COMMS is 5.5V to 30V.

4.2 Antenna Deployment Connector

The connector used for the antenna deployment interface along with its mating parts is provide in Table 4.1. The pin assignment is provided in Table 4.2 and the pin numbering is shown in Figure 4.3. The antenna deployment interface exposes two closed loop control endpoints, i.e. two deployment-detection line pairs.

Control signal lines are software configurable as either 3.3V Push-Pull or Open-Drain. Maximum input voltage in Open-Drain configuration is restricted to 5V by an ESD protection diode. Control signal current is limited to 22mA via 220Ω resistor (in the case of a 5V signal).

Detection signal lines are 3.3V compatible and software configured as Pull-Up, Pull-Down or Floating. Pull-Up and Pull-Down resistor value is $40k\Omega \pm 10k\Omega$. Each detection line is protected from over-voltage via a 5V ESD protection diode and a $1k\Omega$ resistor.

Antenna Deployment Connector	
SatNOGS COMMS connector	Harwin G125-MH10605L7P
Mating Connector	Harwin G125–2040696L0
Mating Connector Crimps	Harwin G125-FW20450L94

Table 4.1: Antenna deployment connector and mating parts

Pin	Function
1	GND
2	GND
3	Deploy-B
4	Detect-B
5	Deploy-A
6	Detect-A

Table 4.2: Antenna Deploy connector pin assignment

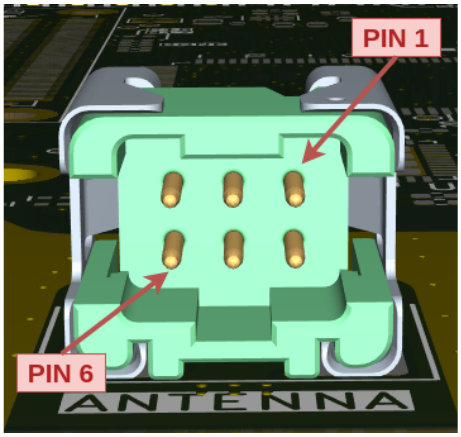

Figure 4.3: Antenna deployment interface pin numbering

4.3 Programming and debuging connectors

The connectors used to program and debug the MCU and the FPGA along with their mating parts are provided in Table 4.3. The supported interface for the FPGA is JTAG, while the MCU also supports SWD. Pin assignment is provided in Table 4.4, and pin 1 position is shown in Figure 4.4. Note that the debug reset pin on the MCU JTAG connector refers to a soft reset induced by the debug interface and not to the NRST pin of the MCU.

Programming and Debugging Connector	
SatNOGS COMMS connector	Molex 53261–1071
Mating Connector	Molex 51021–1000
Mating Connector Crimps	Molex 500588020

Table 4.3: Programming and debugging connector and mating parts

Pin	MCU SWD	MCU JTAG	FPGA JTAG
1	Clock	Clock	Clock
2,4,6	GND	GND	GND
3	SWDIO	JTMS	TMS
5	SWO	JTDO	TDO
7	—	JTDI	TDI
8	NRST	NRST	GND
9	Debug reset	Debug reset	PS POR B
10	3.3V Reference	3.3V Reference	3.3V Reference

Table 4.4: Programming connector pin assignment

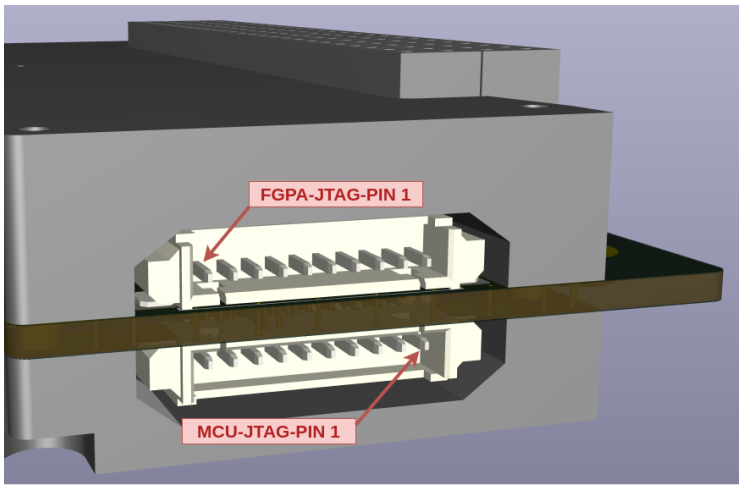

Figure 4.4: Programming connector pin numbering

4.4 RF Connectors

The connector used for the RF communication interfaces along with its mating part are provided in Table 4.5. The position of the UHF and S-Band interface on the board is noted in Figure 4.2.

Communication RF Connectors	
SatNOGS COMMS connector	Molex 73415–0961
Mating Connector	Any MMCX
Mating Connector Crimps	Any MMCX

Table 4.5: Communication RF connectors and mating parts

The connector used for the 26MHz and 1PPS external reference clock interfaces along with its mating part is provided in Table 4.7. The position of the external reference clock interface on the board is noted in Figure 4.5. This figure only shows the cutouts on the EMI shield from which the interface cables exit the system. During assembly, the cables are connected before the EMI shield is placed and secured.

Some additional information on the external reference clock interface, is provided in Table 4.6.

Interface	Voltage Limit	Signal Type	Input Interface
1PPS	0V to 3.3V	Rectanglular pulse	LMK1C1102DQF
26MHz	600mV to 1500mV (peak to peak) AC Coupling	Rectanglular pulse Sine Clipped Sine	TS5A3157DCKR

Table 4.6: External Clock Interfaces

Reference Clock RF Connectors	
SatNOGS COMMS connector	Wurth 66011102111302
Mating Connector	Same as mating crimp
Mating Connector Crimps	AmphenolRF 262111 MMCX Right Angle Crimp Plug RG-316DS RD-316 50 Ohm

Table 4.7: Reference clock RF connectors and mating parts

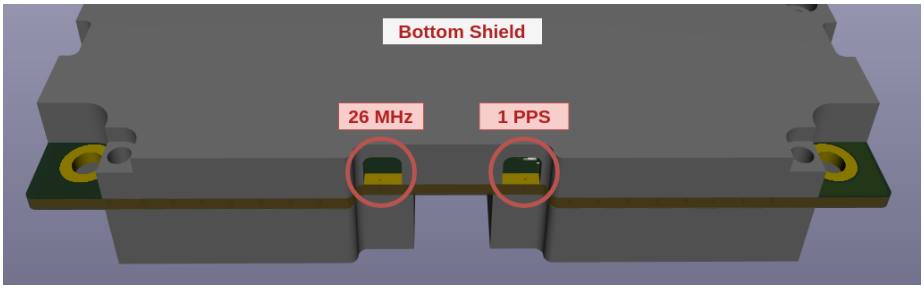

Figure 4.5: External clock reference interface

4.5 RGMII, UART & eMMC Connector

SatNOGS COMMS provides an RGMII interface which is connected to the PS part of the Zync SoC and, internally, it is fed by a GMII to RGMII adapter, which is wired to an IEEE 802.3–2008 [2] compliant gigabit ethernet controller. Up to 100 Mbps throughput on 1.8V operation has been achieved through this interface during testing.

The RGMII interface, a UART interface for debugging the SoM, along with some lines to access the eMMC memory are exposed on the connector listed in Table 4.8. The pinout of said connector is provided in Table 4.9 and the position of pin 1 is shown in Figure 4.6.

RGMII, UART, eMMC Connector	
SatNOGS COMMS connector	Harwin G125-MH12605L3R
Mating Connector	Harwin G125–2042696L0
Mating Connector Crimps	Harwin G125-FW20150F94

Table 4.8: RGMII, UART, eMMC connector and mating parts

Pin	Function
1	PHY_RESET
2	1.8V output
3	RGMII-MDC
4, 7, 8, 22	GND
5	RGMII-MDIO
6	PHY_INT
9	RGMII-TXD0 from SoM
10	RGMII-RXCLK to SoM
11	RGMII-TXD1 from SoM
12	RGMII-RXCTL to SoM
13	RGMII-TXD2 from SoM
14	RGMII-RXD0 to SoM
15	RGMII-TXD3 from SoM
16	RGMII-RXD1 to SoM
17	RGMII-TXCLK from SoM
18	RGMII-RXD2 to SoM
19	RGMII-TXCTL from SoM
20	RGMII-RXD3 to SoM
21	MCU_MMC-D0
23	MCU_MMC-CMD
24	UART-RX to SoM
25	MCU_MMC-CK
26	UART-TX from SoM

Table 4.9: RGMII, UART & eMMC connector pinout

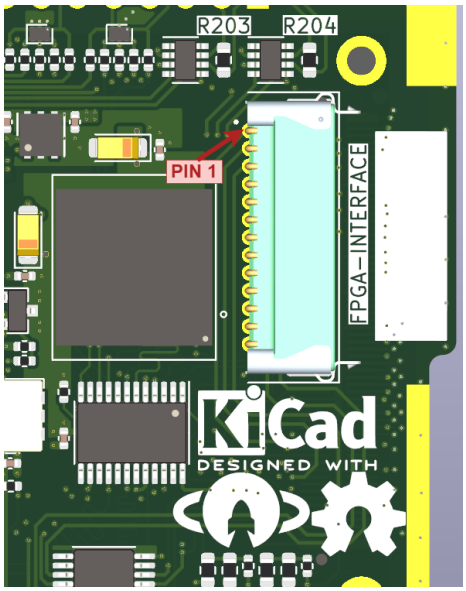

Figure 4.6: RGMII, UART & eMMC connector pin 1

4.6 ESD & Power protections

4.6.1 ESD

Most of the interfaces of SatNOGS COMMS include ESD protection in the form of clamping diodes placed as close as possible to the connectors. In particular, the protected interfaces are:

- MCU and FPGA JTAG
- PC–104 SPI, I2C and UART. Also resistors are included in-series after the diodes and before the components.
- Antenna deployment

Regarding the CAN interface on the PC–104, the selected CAN driver (TCAN334G) incorporates ESD protection.

Regarding the external reference clock 26MHz and 1PPS, the selected multiplexer and clock buffer incorporated ESD protection.

4.6.2 Power protection

The power system of SatNOGS COMMS is paired with an elaborate protection scheme able to protect the downstream components from overvoltage, undervoltage and excessive current draw. All major power rails on the board are automatically reset in the event of excessive current draw or overvoltage, while an MCU signal is required in addition to a proper voltage level for the RF and FPGA power rails to be enabled. For further details on the operation of the power protection system along with an FMEA analysis, please refer to the System Design Document.

5. FPGA SoM

This chapter details the various interfaces related to the FPGA SoM that can be hosted on SatNOGS COMMS. The electrical and mechanical interface characteristics required for a user to employ their own SoM on SatNOGS COMMS are provided.

5.1 RF Functionality

The baseband transceiver functionalities are listed below:

- Modulation: GMSK/GFSK, BPSK, QPSK
- Tx: ECC, CCSDS CC1/2 w/ and w/o RS, Rx: only CCSDS RS
- Framing encapsulation: CCSDS, IEEE 802.15.4
- Data Rates: UHF, up to 50 kbps, S-Band, up to 1 Mbps

In the default SatNOGS COMMS configuration with the Alinx AC7Z020, the SoM provides a 13-bit I/Q data interface with a sampling frequency up to 4MHz through which additional RF functionalities can be implemented.

5.2 Mechanical Interface

The FPGA SoM is mechanically attached to SatNOGS COMMS through nuts, bolts, and threaded spacers. In particular, the following parts are used:

- Nut M2 DIN934
- Bolt M2L8 DIN912
- Female to Female M2 L3, Knurled, Brass, Round Spacer

For the default SoM used in SatNOGS COMMS (the Alinx AC7Z020), the mounting is performed by placing the bold such that the bolt head contacts the bottom side of the board and the nut contacts the top side of the SoM, as shown in Figure 5.1. For the flight configuration, glue is applied to the nut and bolt.

Regarding the relative position of the SoM mounting holes to the mezzanine connectors, a SoM KiCAD footprint has been created as part of the LibreWave project and it can be found in lsf-kicad-lib under the footprint name *LibreWave-SoM*.

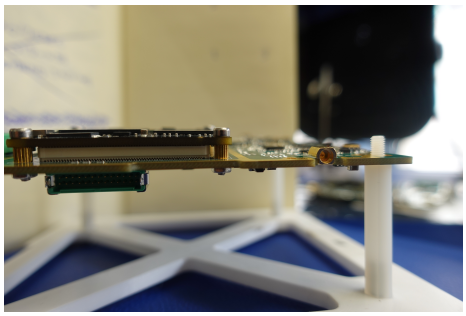

Figure 5.1: AC7Z020 SoM mounting

5.3 Electrical Interface

5.3.1 Mezzanine Connector Pinout

The connector used to interface SatNOGS COMMS with the FPGA SoM along with its mating part are provided in Table 5.1.

The functionalities of the mezzanine connector pins are provided in Table 5.2 and Table 5.3, while the naming of the two headers of the mezzanine connectors are shown in Figure 5.2.

RGMII, UART, eMMC Connector	
SatNOGS COMMS connector	Panasonic AXK6A2337YG
Mating Connector	Panasonic AXK5A2137YG
Mating Connector Crimps	N/A

Table 5.1: FPGA SoM mezzanine connector and mating part

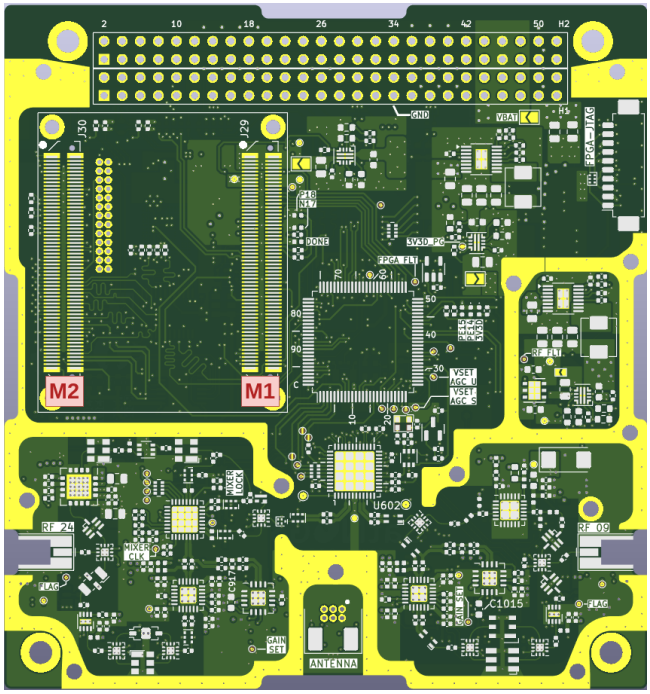

Figure 5.2: Mezzanine connector header numbering

H1		
Header no	**Overall no**	**Functionality**
1, 2, 3, 4, 5, 6, 7, 8	1, 2, 3, 4, 5, 6, 7, 8	5V SoM input
11, 13, 15, 17	11, 13, 15, 17	3.3V SoM input
12, 14, 16, 18	12, 14, 16, 18	2.5V SoM input
9, 10, 19, 20, 29, 30, 39, 40, 49, 50, 59, 60, 69, 70, 79, 80, 89, 90, 99, 100, 109, 110	9, 10, 19, 20, 29, 30, 39, 40, 49, 50, 59, 60, 69, 70, 79, 80, 89, 90, 99, 100, 109, 110	GND
22	22	SPI-SEL
24	24	SPI-MOSI
28	28	SPI-MISO
37	37	1 PPS SoM clock input line 2
41	41	SPI-CLK
52	52	LED_1 output
54	54	LED_2 output
55	55	UART_2 RX to SoM
57	57	UART_2 TX from SoM
72	72	RX_INT (used as a generic IO or to indicate an interrupt due to RF RX)
76	76	IP_RESET (used as a generic IO or to reset the IP cores)
81	81	100 MHz SoM clock input
111	111	JTAG-TCK
113	113	JTAG-TMS
115	115	JTAG-TDO
116	116	PS_POR_B (specific to some Xilinx FPGAs)
117	117	JTAG-TDI
118	118	FPGA_DONE (also drives a LED)

Table 5.2: Mezzanine connector H1 pinout

H2		
Header pin	**Connector pin**	**Functionality**
9, 10, 29, 20, 29, 30, 39, 40, 49, 50, 59, 60, 69, 70, 79, 80, 89, 90, 99, 100, 109, 110,	129, 130, 139, 140, 149, 150, 159, 160, 169, 170, 179, 180, 189, 190, 199, 200, 209, 210, 219, 220, 229, 230	GND
1	121	LVDS-TXDP from SoM
3	123	LVDS-TXDN from SoM
25	145	LVDS-RXDP Sband to SoM
27	147	LVDS-RXDN Sband to SoM
31	151	LVDS-RXDN UHF to SoM
33	153	LVDS-RXDP UHF to SoM
41	161	LVDS-RXCLKN to SoM
43	163	LVDS-RXCLKP to SoM
52	172	LVDS-TXCLKP from SoM
54	174	LVDS-TXCLKN from SoM
61	181	RGMII-RXCLK to SoM
63	183	RGMII-RXCTL to SoM
65	185	RGMII-RXD0 to SoM
66	186	PHY_INT
67	187	RGMII-RXD1 to SoM
71	191	RGMII-RXD2 to SoM
72	192	1 PPS SoM clock input line 1
73	193	RGMII-RXD3 to SoM
74	194	MMC CK
75	195	RGMII-TXCTL from SoM
76	196	MMC D0
77	197	RGMII-TXCLK from SoM
78	198	MMC CMD
81	201	RGMII-TXD3 from SoM
83	203	RGMII-TXD2 from SoM
84	204	MMC D2
85	205	RGMII-TXD1 from SoM
87	207	RGMII-TXD0 from SoM
92	212	MMC D1
94	214	PHY_RESET
96	216	UART_1 TX from SoM
98	218	UART_1 RX to SoM
102	222	RGMII-MDC
112	232	MMC D3
114	234	UART_0 RX to SoM
116	236	UART_0 TX from SoM
118	238	RGMII-MDIO
119, 120	239, 240	Configurable Pull Up/Down

Table 5.3: Mezzanine connector H2 pinout

5.3.2 SoM Power Interfaces

The SoM is powered via a PDN implemented on SatNOGS COMMS. The voltage levels provided by this PDN along with their current limits are listed below:

- 5V power channel: SMPS (LT8610EMSE#PBF), shared with the RF subsystem, protected against overvoltage, undervoltage, and overcurrent events via an e-fuse (TPS259470A). Overvoltage limits range from 5.3 to 5.47V. Undervoltage limits are 4.75V (for a rising edge) and 4.5V (for a falling edge). Additionally, an undevoltage limit of 5.7V has been set for the input of the SMPS. The current limit stands at 0.59 A. Note that the 3.3V and 2.5V power channels draw from the 5V one, so the aforementined current limit cannot be fully exploited by the 5V power channel.
- 3.3V power channel: LDO (LD39100PU33RY), with a current output capability dependent on the ambient temperature. A current capability of 0.48 A is obtained for the case of 80 C ambient temperature.
- 2.5V power channel: LDO (MIC5320-JGYD6), with a current output capacity dependent on the ambient temperature. A current capability of 0.26 A is obtained for the case of 80 C ambient temperature.

6. Software Interfaces

6.1 Space Segment

SatNOGS-COMMS provide a reference firmware[3] based on the Zephyr-RTOS[4]. This firmware covers the majority of the functionality required from a COMMS subsystem. Moreover, the firmware provides extensive functionality to operate as OBC too, if the mission requires it. Special attention has been given on the design of the firmware, so mission specific code can be added, adapting to the user needs. For more information refer to the main firmware documentation available at [5].

In case a mission or user requirements dictate significant firmware modifications or even another RTOS, SatNOGS-COMMS provide the SatNOGS COMMS Control Library[6]. This is an interface library that controls the SatNOGS COMMS transceiver components. It relies on a peripheral abstraction layer, allowing users of the SatNOGS COMMS to build their own firmware with minimal effort.

6.2 Ground Segment

6.2.1 Telemetry API

SatNOGS provides an API for receiving acquired telemetry as well as signal acquisition parameters. For non real-time operation, raw telemetry data is uploaded directly to SatNOGS DB servers by SatNOGS Client, on predefined intervals. This API endpoint accepts HDF5 formatted files which include additional information and metadata of the scheduled SatNOGS Network observation. The telemetry data are then processed and forward to the InfluxDB database of SatNOGS Dashboards in order to be visualized. For real-time operation, SatNOGS Client forwards the telemetry data to a SatNOGS Yamcs server. The SatNOGS Yamcs server receives the data through a data link plugin which provides a gRPC interface for telemetry. In this case, telemetry data is still eventually forwarded to SatNOGS DB via the Yamcs server and a SatNOGS DB API data link plugin.

6.2.2 Telecommand API

SatNOGS provides an API allowing telecommand data transmission. SatNOGS Client gRPC interface is used to receive telecommands. These commands are

sent by the SatNOGS Yamcs server via a gRPC data link plugin. The client then forwards the telecommands to SatNOGS Radio in order to be encoded and transmitted via the SDR.

6.2.3 Telecommand and Telemetry Format

The default firmware of the SatNOGS-COMMS utilizes the CCSDS XTCE[7] to describe the available telecommands and telemetry responses, as well as the internal structure of each frame. Yamcs provides seamless integration with the CCSDS XTCE.

6.2.4 Control Software

For the reference firmware[3] the SatNOGS COMMS project provides a Yamcs-based control software[8]. This Yamcs based control software can be used to telecommand the transceiver from any of the available interfaces (RF, CAN, UART) as well as receive telemetry. This is accomplished using the CCSDS XTCE definition that ships with the reference firmware. The purpose of this software it to act as a starting point, so missions can build easily the entire mission control with minimal effort.

6.3 Health Status Telemetry

6.3.1 Temperature Sensor Positions

To interpret the temperature values received in the health status telemetry, it is required to know the positions of the temperature sensors on the board. There are three sensors used to measure ambient (PCB) temperature, UHF PA temperature, and S-band PA temperature. The positions of the aforementioned sensors are depived in Figure 6.1.

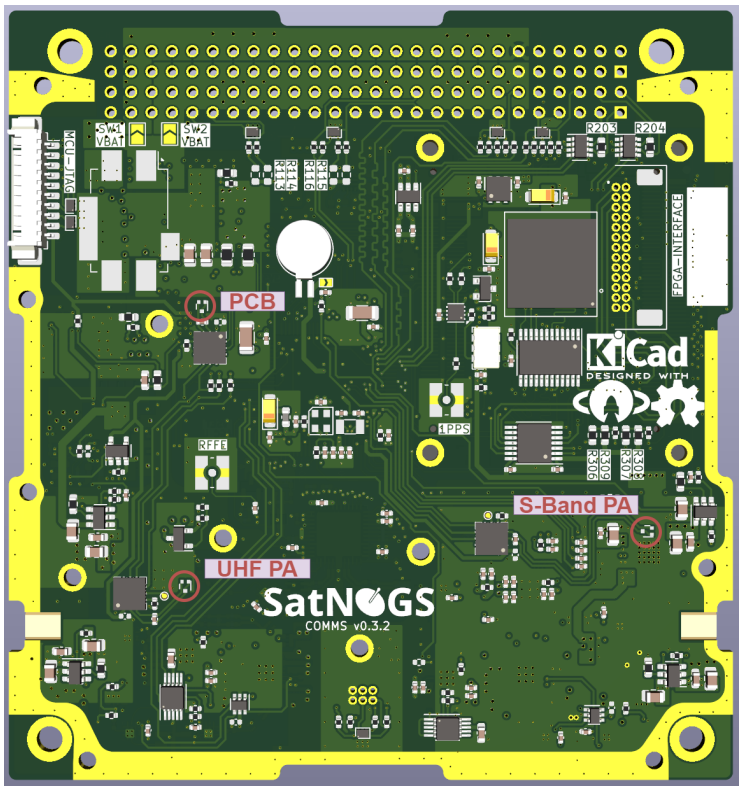

Figure 6.1: Temperature sensor positions

7. Performance Measurements

This chapter includes measurements related to the performance of the system, such as power consumption and RF characteristics.

7.1 Power Measurements

The power consumption of the system has been measured in various operational states. These measurements listed in Table 7.1 below refer to a 12V supply voltage. For a more detailed presentation along with comments on the test conditions refer to this spreadsheet. *Note that the measurements were made in v0.3, but the differences with the most recent version are very minor.*

State no.	Avg Current [mA]	Peak Current [mA]	State Description
State 1	67	NA	MCU peripherals initialized
State 2	57	NA	State 1 + eMMC initialized
State 3	NA	91	State 2 + eMMC write
State 4	NA	91	State 2 + eMMC read
State 5	143	NA	State 2 + FPGA on
State 6	203	NA	State 2 + FPGA running petalinux
State 7	230	NA	State 2 + FPGA stress petalinux
State 8	74	NA	State 1 + RF open
State 9	71	NA	State 8 + init AT86
State 10	370	641	State 9 + full power TX UHF baseband
State 11	247	NA	State 9 + RX UHF
State 12	185	NA	State 9 + RX UHF
State 13	250	NA	State 9 + RX UHF
State 14	NA	NA	State 9 + RX UHF
State 15	467	718	State 9 + fullpower TX S baseband
State 16	303	NA	State 9 + RX S
State 17	267	NA	State 9 + RX S
State 18	305	NA	State 9 + RX S
State 19	245	NA	State 9 + RX S
State 20	574	750	State 15 + FPGA running petalinux
State 21	602	773	State 15 + FPGA stress petalinux

Table 7.1: Current consumption in various operational states

7.2 Inrush current

Inrush current is a brief high current surge drawn when the device is turned ON. It generally occurs due to uncharged capacitors at the input of power supplies. The setup of the inrush current measurement was according to ECSS-E-ST-20–07C Rev.2. The setup consists of a Line Impedance Stabilization Network (LISN), a mechanical switch, a current probe and an oscilloscope for data acquisition. In this case, the current probe was replaced by two voltage probes and a 0.1 Ohm shunt resistor (RS010R1000FE12). To measure the current, the switch is pressed ON to power the device. A 12V battery was used as the power supply.

The inrush current waveform (Figure 7.1), can be characterized by two pulses. The first one, which is the main current draw, and the second one of much smaller amplitude. The small current draw, before the pulse emergence, is associated with the accuracy error of the oscilloscope and slight smoothing applied to the data for better visual representation.

The first current pulse reaches 13A and lasts around 100 μs. Immediately after, it reaches negative values up to -2A. The second pulse reaches around 3A and also lasts around 100 μs. After that, the board stabilizes to the nominal power consumption, when flashed with the particular firmware. It should be noted that the input voltage rise, when pressing the switch, is around 40 us. In case the input voltage has slowly risen to the desired level, the inrush current is much lower, although the number of pulses that occur increases. More details in https://gitlab.com/librespacefoundation/satnogs-comms/satnogs-comms-hardware/-/issues/490.

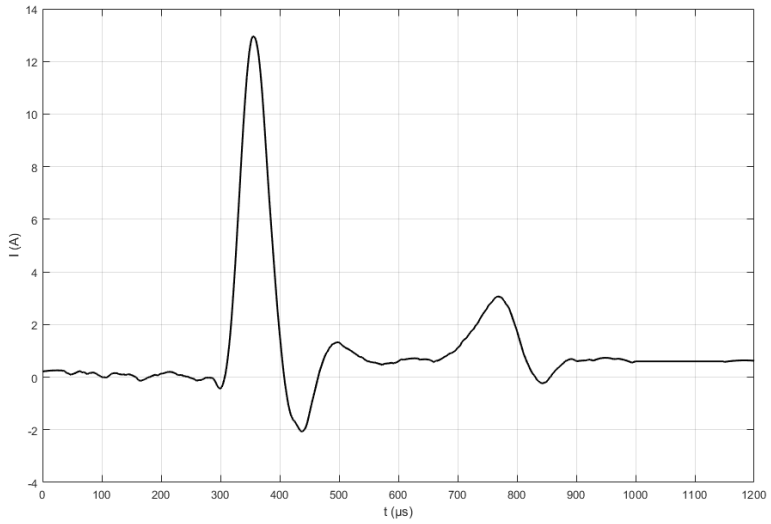

Figure 7.1: Inrush current of SatNOGS COMMS v0.3.2 — PHASMA version when first turned ON

7.3 RF Measurements

7.3.1 UHF Radio-Transmitter

The UHF radio is compliant with the SFCG 21–2R4 recommendations, peak indicated by the marker 2–1 in Figure 7.2 and the markers 2–1, 3–1, 4–1 in Figure 7.3.

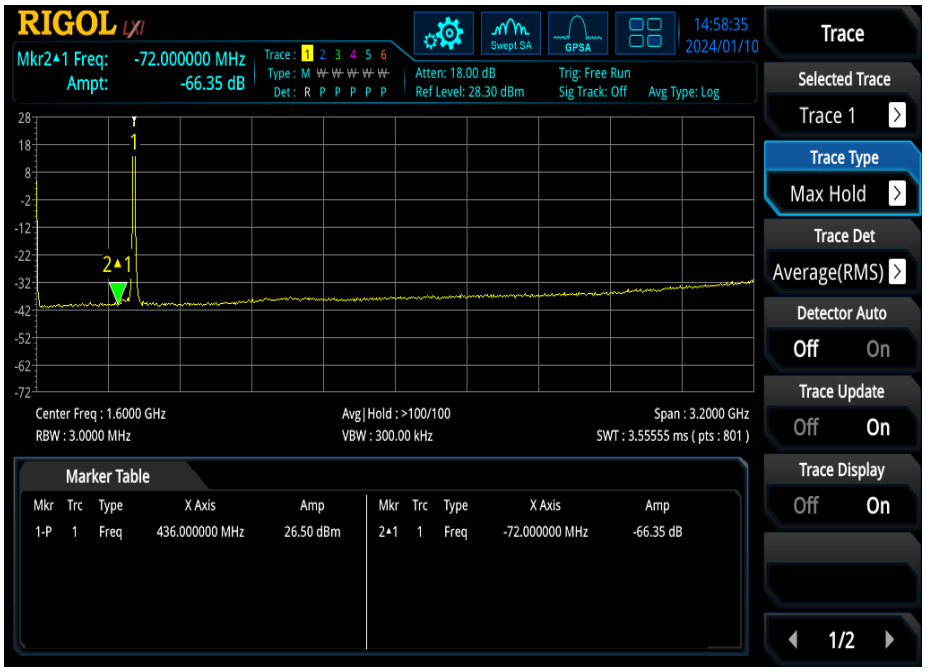

Figure 7.2: UHF spurious emissions, FSK–2, m = 1, TX power = +31 dBm, symbol rate = 50 kHz

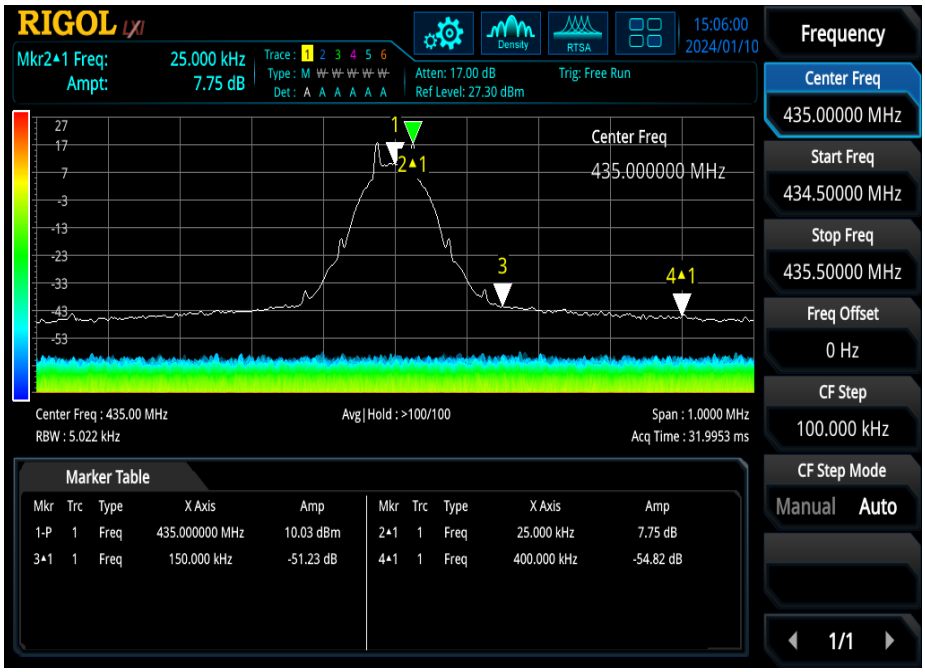

Figure 7.3: UHF spurious emissions, FSK–2, m = 1, TX power = +31 dBm, symbol rate = 50 kHz

The RF output power is not affected by the modulation index (0.5, 1, 1.5, 2) in FSK at 50 ksps. The following diagrams, Figure 7.4 and Figure 7.5, show that the RF output power and the DC power consumption are affected by the operating frequency, 401 and 435MHz. The measurements are done:

- with peak detector and maximum hold as trace type
- the measurement bandwidth (integrated) is 50kHz (FSK-2 at 50ksps) on 200kHz span
- temperature: 25 °C
- Dwell time: 60secs
- the DC power consumption is measured with joulescope and it is the average value of plateau, Figure 7.6

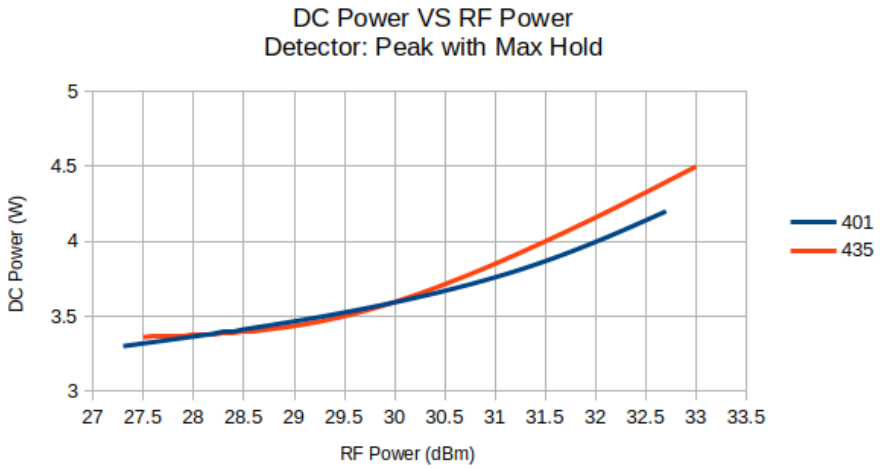

Figure 7.4: DC power vs TX RF power on UHF radio

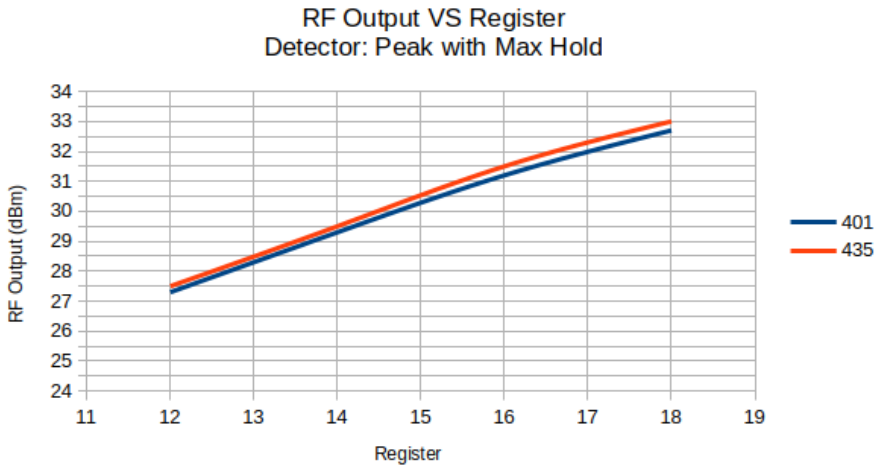

Figure 7.5: TX RF power vs AT86RF215 TX register on UHF radio

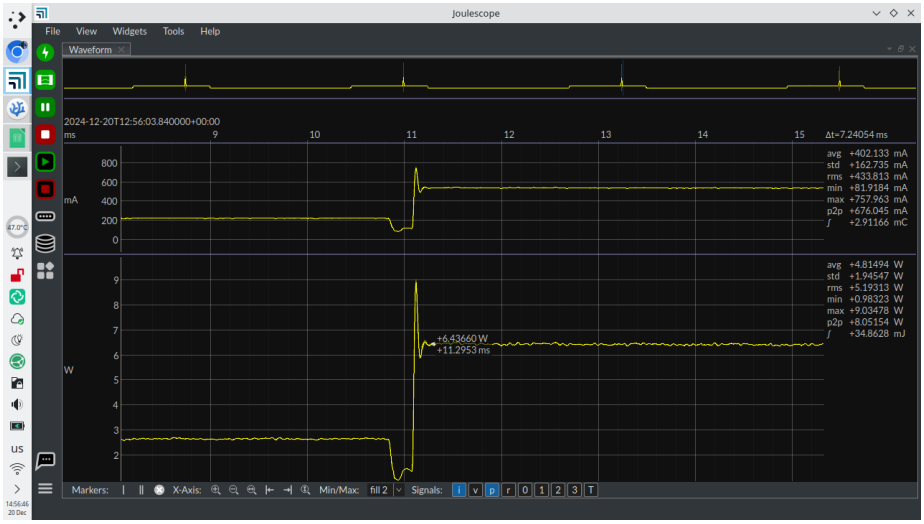

Figure 7.6: DC power consumption plateau measurement (an example)

The frequency step is 100Hz in the range 400MHz to 440MHz as defined by AT86RF215 IC.

7.3.2 UHF Radio-Receiver

The receive RF front end, can operate in two modes:

- AGC is enabled, Figure 7.7.
- AGC is disabled, and VGA is controlled by MCU, Figure 7.8.

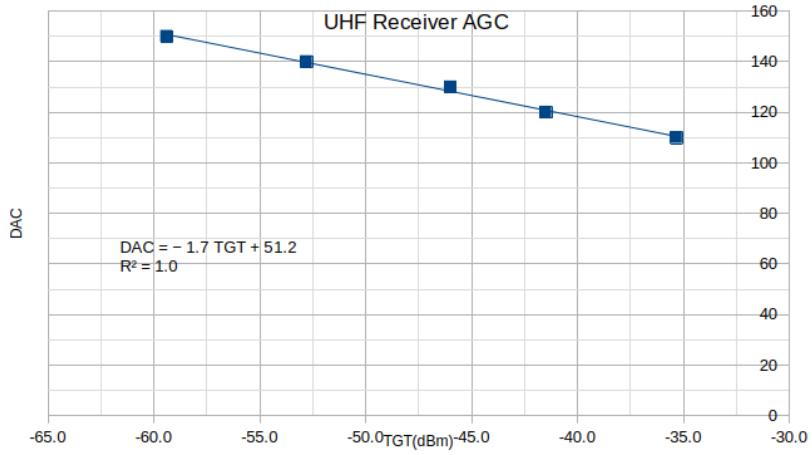

Figure 7.7: UHF AGC-ON, DAC 8-bit

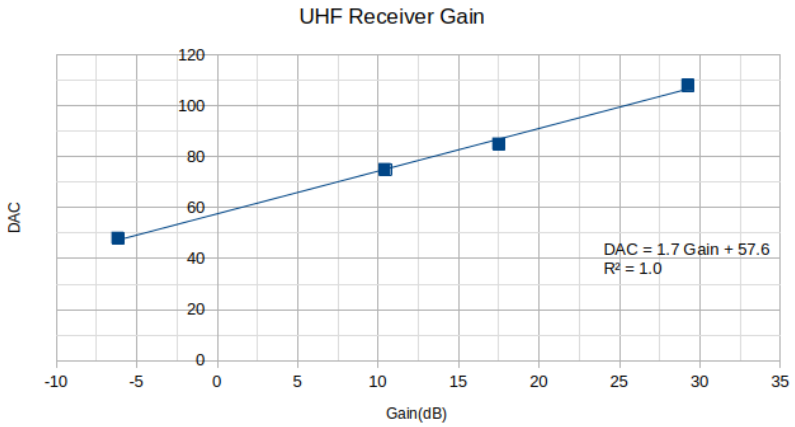

Figure 7.8: UHF AGC-OFF, DAC 8-bit

The suggested mode is AGC ON with TGT level $-55dBm$ to achieve the largest dynamic range of $50dB$. Some critical characteristics:

Noise Figure (dB)	1.8
Maximum input (dBm)	+20

Table 7.2: UHF receiver

The TGT level is measured by using the RSSI of AT86RF215 with tolerance of $\pm 5dB$. The following table, Table 7.3, shows the DC power consumption in different RF input when the AGC in enabled and the output target is set on -52dBm $\pm 5dB$.

RF input (dBm)	RSSI (dBm)	Gain (dB)	DC power (W)
-20	-41	-21	1.69
-30	-51	-21	1.73
-40	-51	-11	1.8
-50	-51	-1	1.88
-60	-51	9	1.98
-70	-51	19	2.1
-80	-51	29	2.25
-90	-53	37	2.5
-100	-61	39	2.5
-110	-70	40	2.5

Table 7.3: RX UHF Radio dynamic range and DC power consumption, AGC ON with TGT -52dBm

The measurements are done:

- with CW RF input signal
- by using the wide BPF

- temperature: 25 °C
- Dwell time: 60secs
- the DC power consumption is measured with joulescope and it is the average value of plateau, Figure 7.6

The frequency step is 100Hz in the range 400MHz to 440MHz as defined by AT86RF215 IC.

Another important aspect is the BER performance of receiver. The following diagram and table, Figure 7.9 and Table 7.4, present the receiver sensitivity in different modulations.

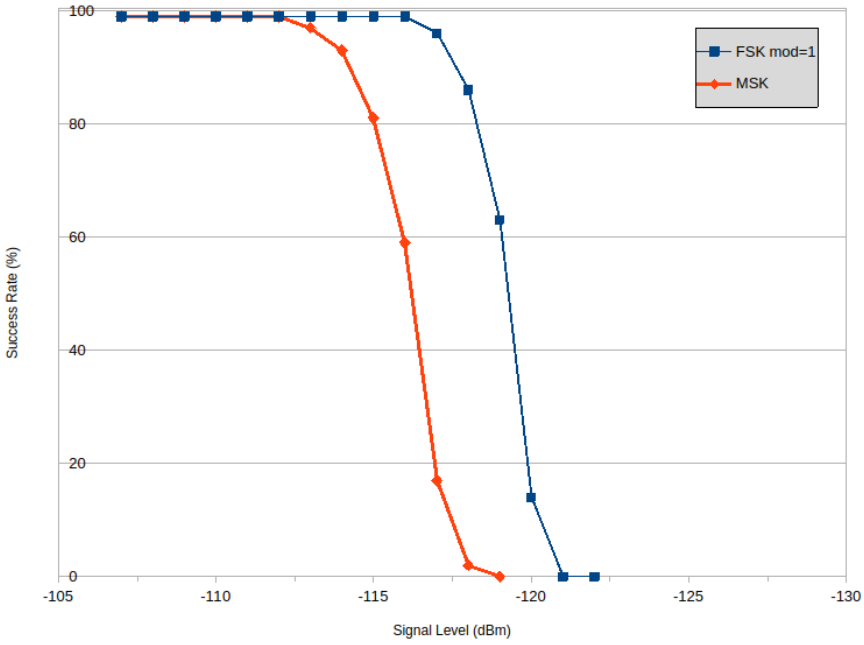

Figure 7.9: UHF Frame success rate for various signal levels

Modulation	Δf (kHz)	Success Rate	Signal Level (dBm)
FSK—2, 50ksps	±10	1099 of 1100	-100
MSK, 50ksps	±10	1100 of 1100	-110

Table 7.4: RX UHF Radio Frequency offset sensitivity

Note:*Better sensitivity is under investigation by the SatNOGS COMMS software team.*

7.3.3 S-Band Radio-Transmitter

The S Band radio is compliant with the SFCG 21–2R4 recommendations, peak indicated by marker 2–1 in Figure 7.10 and markers 2–1, 3–1, 4–1 in Figure 7.11.

Figure 7.10: S Band spurious emissions with FSK–2, m = 0.5, TX power = +33 dBm, 400 kHz symbol rate

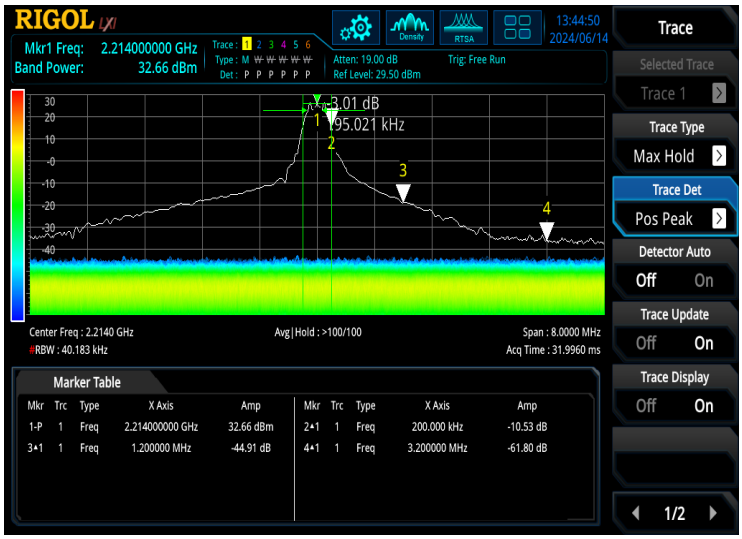

Figure 7.11: S Band spectrum mask for MSK, Input Power = 6.5dBm, symbol rate = 400 kHz

The RF output power is measured only on MSK at 400ksps. The following diagrams, Figure 7.12, Figure 7.13 and Figure 7.14, show that the RF output power and the DC power consumption are affected by the operating frequency, 2200MHz and 2290MHz. The measurements are done:

- with peak detector and maximum hold as trace type
- the measurement bandwidth (integrated) is 400kHz (MSK at 400ksps) on 600kHz span

- temperature: 25 °C
- Dwell time 60 secs
- the DC power consumption is measured with joulescope and it is the average value of plateau, Figure 7.6

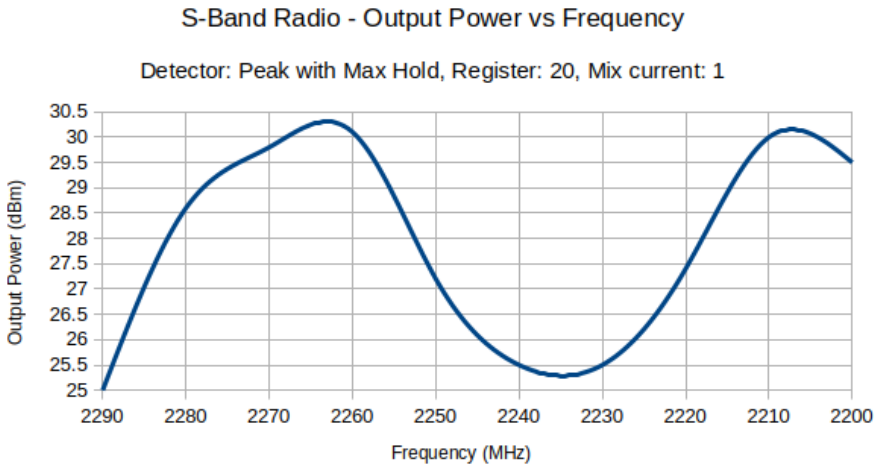

Figure 7.12: TX RF power vs Frequency on S-Band radio

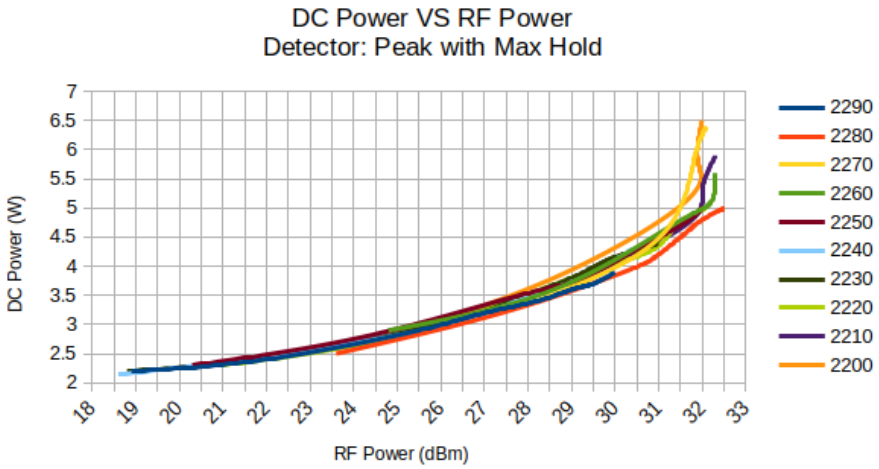

Figure 7.13: DC power vs TX RF power on S-Band radio

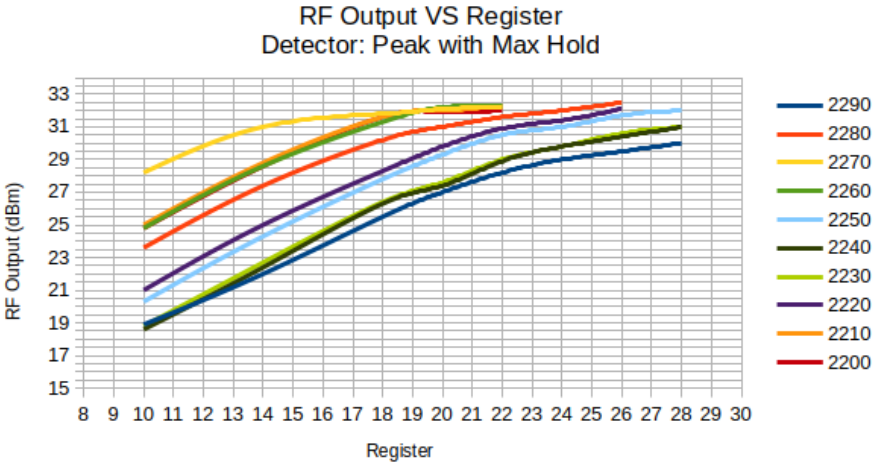

Figure 7.14: TX RF power vs AT86RF215 TX register on S-Band radio

The LO is selected according to the following table Table 7.5. The frequency step is 400Hz in the range 2200MHz to 2290MHz as defined by AT86RF215 IC. **Option:***Fine frequency step is possible after request.*

LO (MHz)	IF (MHz)	RF (MHz)	Image (MHz)
182	2472	2290	2654
182	2462	2280	2644
216	2486	2270	2702
216	2476	2260	2692
216	2466	2250	2682
216	2456	2240	2672
216	2446	2230	2662
216	2436	2220	2652
216	2426	2210	2642
216	2416	2200	2632

Table 7.5: Look-up Table of LO frequencies of Transmitter

The mix current register of the RF mixer is set to 1.

7.3.4 S-Band Radio-Receiver

In the same manner with section subsection 7.3.2 are following the diagrams, Figure 7.15 and Figure 7.16.

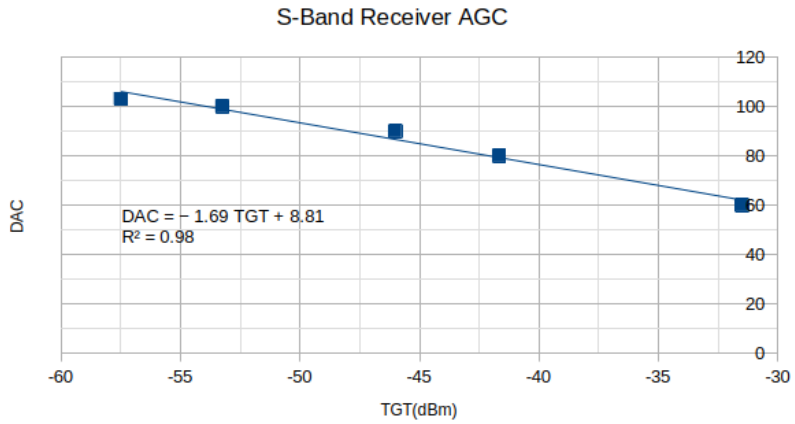

Figure 7.15: S-Band AGC-ON, DAC 8-bit

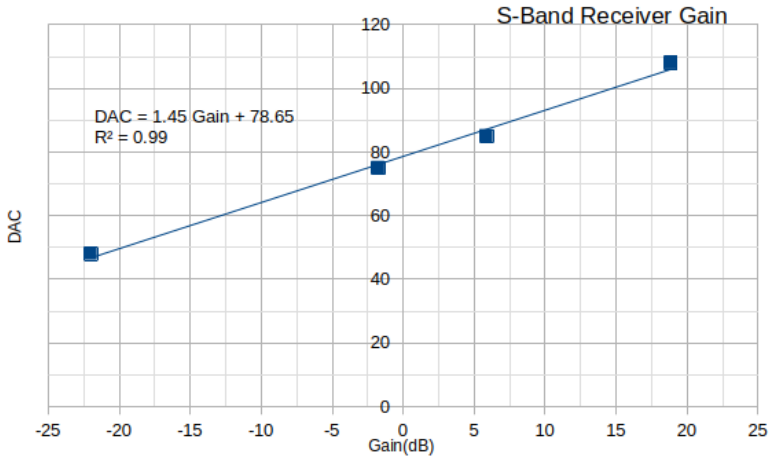

Figure 7.16: S-Band AGC-OFF, DAC 8-bit

The suggested mode is AGC ON with TGT level $-55dBm$ to achieve the largest dynamic range of $40dB$. Some critical characteristics:

Noise Figure (dB)	2.2
Maximum input (dBm)	+27

Table 7.6: S-Band receiver

The TGT level is measured by using the RSSI of AT86RF215 with tolerance of $\pm 5dB$. The following table, Table 7.7, shows the DC power consumption in different RF input when the AGC in enabled and the output target is set on -52dBm $\pm 5dB$.

RF input (dBm)	RSSI (dBm)	Gain (dB)	DC power (W)
-20	-48	-28	2.22
-30	-51	-21	2.27
-40	-51	-11	2.34
-50	-52	-2	2.45
-60	-52	8	2.57
-70	-52	18	2.7
-80	-59	21	2.83
-90	-70	20	2.83
-100	-78	22	2.8
-110	-88	22	2.84

Table 7.7: RX S-Band Radio dynamic range and DC power consumption, AGC ON with TGT -52dBm

The measurements are done:

- with CW RF input signal
- by using the wide BPF
- temperature: 25 °C
- Dwell time: 60secs
- the DC power consumption is measured with joulescope and it is the average value of plateau, Figure 7.6

The LO is selected according to the following table Table 7.8. The frequency step is 400Hz in the range 2025MHz to 2110MHz as defined by AT86RF215 IC. **Option:***Fine frequency step is possible after request.*

Image (MHz)	IF (MHz)	LO (MHz)	RF (MHz)	5th LO (MHz)	6th LO (MHz)	7th LO (MHz)
1635	2415	390	2025	1950	2340	2730
1640	2420	390	2030	1950	2340	2730
1650	2430	390	2040	1950	2340	2730
1660	2440	390	2050	1950	2340	2730
1670	2450	390	2060	1950	2340	2730
1706	2434	364	2070	1820	2184	2548
1716	2444	364	2080	1820	2184	2548
1726	2454	364	2090	1820	2184	2548
1736	2464	364	2100	1820	2184	2548
1746	2474	364	2110	1820	2184	2548

Table 7.8: Look-up Table of LO frequencies of Receiver

The mix current register of the RF mixer is set to 1.

Another important aspect is the BER performance of receiver. The following diagram and table, Figure 7.17 and Table 7.9, present the receiver sensitivity in different modulations.

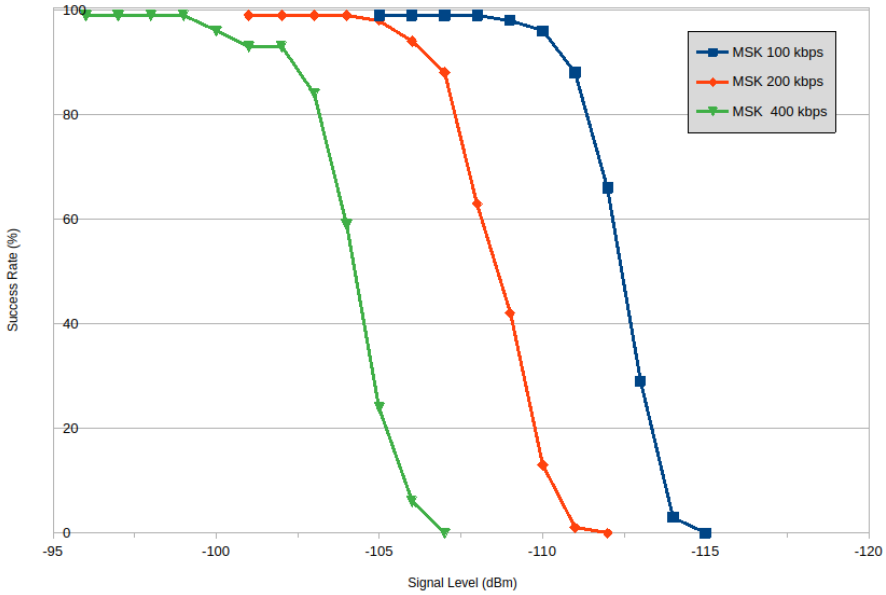

Figure 7.17: S-Band Frame success rate for various signal levels

Modulation	Δf (kHz)	Success Rate	Signal Level (dBm)
MSK, 400ksps	±60	1100 of 1100	-96

Table 7.9: RX S-Band Radio Frequency offset sensitivity

Note:*Better sensitivity is under investigation by the SatNOGS COMMS software team.*

8. Environmental Specifications

This chapter outlines the system specifications related to its operational environment.

8.1 Operational Temperature

Based on the maximum and minimum operational temperatures of its components, the operational temperatures of SatNOGS COMMS range from −20° to 60° C. A component-level analysis is provided here. As one can notice in the analysis, only a few resistors, capacitors, and inductors have been studied as samples, yet the analysis includes all the more complex integrated circuits. Additionally, a report from the most recent TVAC test can be found here.

8.2 Vibration Environment

The report from the most recent vibration test can be found here.

8.3 Electromagnetic Compatibility

8.3.1 Possible EM Emitters

Listed in Table 8.1 are potential EMI emitters on the board. This list mostly serves as a reference in case EMC debugging is required, because if detailed emission characterization is required (for example for a sensitive on—board payload), the emissions spectrum from the EMC test shall be used. Harmonics of the frequencies listed below are also possible to appear.

The report from the most recent EMC test is provided here. Note that this test was conducted on SatNOGS COMMS v0.3.1. The upcoming SatNOGS COMMS v0.3.2 includes an EMI filter on the power input, which aims to alleviate the emissions which violate the limits in the provided test report.

Possible Emitter	Frequency
3.3V SMPS	1.2 MHz
5V SMPS	1.0 MHz
FPGA SoM 1V SMPS	2.5 MHz
FPGA SoM 1.8V SMPS	2.5 MHz
MCU HSE Crystal	32 MHz
MCU LSE Crystal	32.768 kHz
RF Transceiver Crystal	26 MHz
FPGA Crystal	100 MHz
LVDS	64 MHz
RGMII	Depends on selected bus clock frequency
MCU-FPGA SPI	Depends on selected bus clock frequency
MCU-Transceiver SPI	Depends on selected bus clock frequency
Bus SPI	Depends on selected bus clock frequency
Bus UART	Depends on selected data rate
Bus I2C	Depends on selected bus clock frequency
SMBus	Depends on selected bus clock frequency
CAN-FD	Depends on selected data rate
CAN 2.0	Depends on selected data rate

Table 8.1: Possible EMI emitters list

8.3.2 Grounding

The PCB is grounded through the PC-104 connector. So, there are no deliberate structure currents because the system has a single path to the satellite common ground (through the PC-104 connector). This grounding architecture is selected according to the NASA electrical grounding architecture technical handbook[9]. It must, however, be noted that the grounding of the EMI shield is not optimal. Instead of being connected to the satellite's chassis ground (which, in turn, is connected to the common ground), the EMI shield is connected to the SatNOGS COMMS system ground and then to the satellite's ground through the PC-104 connector. This structure results in a larger impedance on the path between the EMI shield and the common ground. Finally, it is noted that the ground of the RG ports is connected to the system ground.

8.4 Radiation Tolerance

Besides the power protection features aiming to increase radiation hardness against single event effects, SatNOGS COMMS employs aluminum shielding to protect its components from total ionizing dose faults. An analysis for a 6-year mission in a LEO orbit is provided in [10].

9. Material List

The list of materials contained in the SatNOGS COMMS system is provided here.

10. Interfaces Data Sheet

INTERFACE DATA SHEET				
	I/F Designation:	**DC Power interface**		
ID	**Source Circuit Specification**		Ver	Iss
-1	Bus voltage	5.5V-30V input range		
-2	Bus current	1.6A max @ 12V Bus voltage		
-3	Response to bus undervoltage	All loads except MCU switch off automatically MCU is deactivated at 3.2V Bus voltage		
-4	Bus voltage (anomaly):	The load shall not be damaged when subjected to any bus voltage in the range 0V to 30V, steady-state or at any rate of change.		

Table 10.1: DC Power Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**SPI interface**		
ID	**Voltage, data rate and timing specification**		Ver	Iss
-1	Data rate	8 Mbps for 3m total bus length between devices		
-2	Voltage range	0V–3.3V		
-3	Voltage tolerance	-0.3V–5.5V		
-4	SPI clock frequency	Slave receiver mode: 100MHz max Slave mode transmitter/full duplex: 31MHz Slave mode transmitter/full duplex: 25MHz		
-5	NSS setup time	Min 2ns		
-6	NSS hold time	Min 1ns		
-7	Data input setup time	Min 2ns		
-8	Data input hold time	Min 1ns		
-9	Data input hold time	1ns		
-10	Data output access time	9ns–27ns		
-11	Data output disable time	Max 5ns		
-12	Data output valid time	Max 16ns		
-13	Data output hold time	Min 9ns		

Table 10.2: SPI Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**CAN interface**		
ID	**CAN Bus characteristics**		Ver	Iss
-1	Bus 1	Compliant with ISO 11898–1[11] (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0 Supports time triggered CAN (TT-FDCAN) specified in ISO 11898–4[12]		
-2	Bus 2	Compliant with ISO 11898–1[11] (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0		
-3	Receiver common mode input voltage	+/-12V		
-4	Bus fault protection	+/-58V		
-5	Max differential voltage between CANH and CANL	+/-45V		
-6	Bus termination	120 Ω at each end of the bus. Split termination is supported		

Table 10.3: CAN Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**Antenna interface**		
ID	**RF characteristics**		Ver	Iss
-1	UHF Impedance	50 Ω		
-2	S-Band impedance	50 Ω		
Deployment control				
-3	Output type	Push-pull or Open-drain		
-4	Output voltage	Push-pull: 3.3V Open-drain: 5V		
-5	Output current	Max 18mA		
Deployment detection				
-6	Input type	Pull-Up, Pull-Down, Floating or Analog		
-7	Input voltage	Nominal 3.3V (reference voltage for analog) Tolerant 5V (only Digital)		
-8	High threshold	2V		
-9	Low threshold	0.8V		
-10	Pull-up/Pull-down resistor	40kΩ±10kΩ		

Table 10.4: Antenna Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**External Clock interface**		
ID	**RF characteristics, Voltage and timing specification**		Ver	Iss
-1	Impedance: 1PPS	50 Ω		
-2	Impedance: RFFE-26MHz	50 Ω		
-3	Voltage Level: 1PPS	0V and 3.3V		
-4	Voltage Level: RFFE-26MHz	peak-to-peak amplitude: 600mV to 1600mV		
-5	Signal Type: 1PPS	Pulse		
-6	Signal Type: RFFE-26MHz	Pulse or Clipped Sine		

Table 10.5: External Clock, 1PPS and 26MHz characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**RGMII**		
ID	**RGMII characteristics**		Ver	Iss
-1	Signal characteristics	Gigabit Ethernet Controller compliant with IEEE 802.3–2008 standard [2]		
-2	Data rate	10/100/1000 Mbps		
-3	Voltage range	0V 1.8V		

Table 10.6: RGMII Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**UART**		
ID	**UART characteristics**		Ver	Iss
-1	Type	Asynchronous		
-2	Data rate	User defined		
-3	Voltage range	0V to 3.3V		

Table 10.7: UART Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**I2C**		
ID	**I2C characteristics**		Ver	Iss
-1	Type	Bidirectional		
-2	Data rate	0.1/0.4/1.0 Mbps		
-3	Voltage range	0V to 3.3V		

Table 10.8: I2C Interface characteristics

References

[1] LibreCube. LibreCube project.

[2] IEEE. Ieee standard for information technology–telecommunications and information exchange between systems–local and metropolitan area networks–specific requirements part 3: Carrier sense multiple access with collision detection (csma/cd) access method and physical layer specifications, 2008.

[3] Libre Space Foundation. SatNOGS COMMS Firmware.

[4] Zephyr RTOS, 2024.

[5] Libre Space Foundation. SatNOGS COMMS Software Documentation.

[6] Libre Space Foundation. SatNOGS COMMS Control Library.

[7] CCSDS. *CCSDS Recommended Standard for XML Telemetric and Command Exchange, CCSDS 660.0-B-2*. 2020.

[8] Libre Space Foundation. SatNOGS COMMS YAMCS Control Software.

[9] NASA. ELECTRICAL GROUNDING ARCHITECTURE FOR UNMANNED SPACECRAFT, 1998.

[10] SatNOGS COMMS radiation shield analysis.

[11] ISO/TC 22/SC 31. Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling, 2015.

[12] ISO/TC 22/SC 31. Road vehicles — Controller area network (CAN) — Part 4: Time-triggered communication, 2004.

