Laboratory Activity 2: Investigation of MOSFET Characteristics)

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I. Introduction

This laboratory activity focuses on characterizing the low-voltage NMOS transistor (sg13lvnmos) technology using an open-source process design kit within the IIC-OSIC-TOOLS environment featuring Xschem for schematic entry and ngspice for simulation. The provided testbench consists of a common-source configuration with the NMOS device (W=1 u, L=0.13 u, ng=1, m=1) biased at Vgs=0.65 V DC and Vds=1.5 V, allowing exploration of key device parameters including Id(Vgs) and Id(Vds) characteristics, the impact of scaling width (W) and length (L) on current drive and transconductance, gate-related capacitances (Cgs, Cgd, Cgb) and drain-bulk capacitance (Cdb) under varying bias conditions, as well as differences between low-voltage (thin-oxide, 1.5 V nominal) and high-voltage (thick-oxide, 3.3 V nominal) MOSFETs in terms of performance trade-offs such as speed versus breakdown voltage. These investigations highlight how bias affects threshold voltage and mobility, how device sizing influences output current and parasitic capacitances (which may appear negative in certain regions due to model conventions for overlap or Miller effects), and provide rationale for selecting LV versus HV transistors in inverter sizing or body-effect-sensitive circuits.

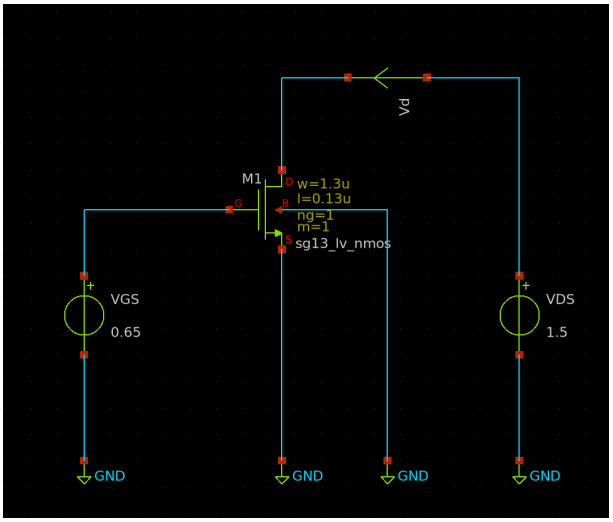

Fig. 1: Testbench

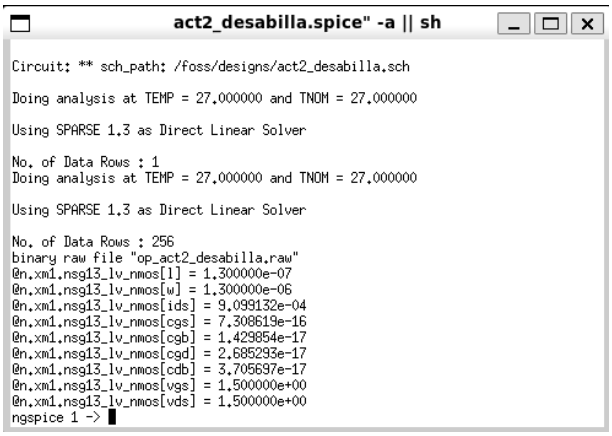

Fig. 2: OP

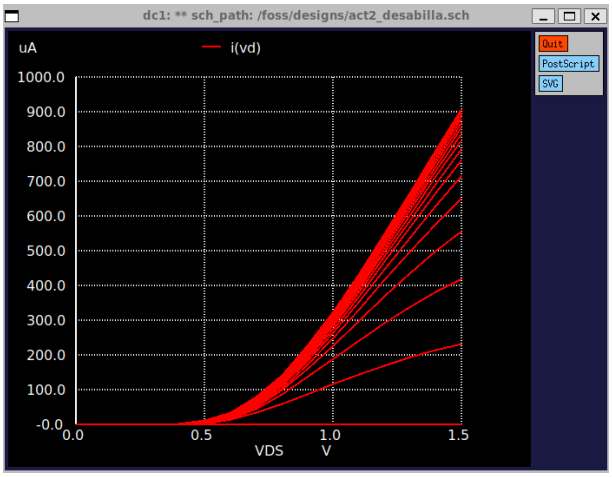

Fig. 3: i(Vd) vs v(v-sweep) xlabel VDS

II. Results and Discussion

A. Exploring the LV NMOS sg13lvnmos

1) How is IDS affected by VGS and VDS?: The simulation results show the family of Id-Vds curves for the low-voltage NMOS (sg13lvnmos, W=1 u, L=0.13 u, m=1) with VGS swept from 0.1 V to 1.5 V in 0.1 V steps and VDS swept from 0 V to 1.5 V. The plot of i(Vd) (drain current in uA) versus VDS clearly illustrates the two main operating regions: for low VDS, the current rises nearly linearly (triode region), while for higher VDS, the current saturates and becomes

almost independent of VDS. As VGS increases, the saturation current Idsat rises significantly in a roughly quadratic manner, demonstrating strong control of drain current by gate-source voltage through transconductance. Higher VGS also shifts the onset of saturation to higher VDS values. In summary, Id is primarily controlled by VGS (determining the maximum current level) and only weakly affected by VDS once the transistor enters saturation, with minimal increase due to channel-length modulation.

2) Changing W and L: The simulation results demonstrate the effects of varying the width (W) and length (L) of the low-voltage NMOS transistor under fixed bias conditions (VGS = 0.65 V and VDS = 1.5 V, ensuring saturation operation). For the default configuration with W = 1.3 u and L = 0.13 u, the drain current is 54.69 uA. Increasing the length to 0.2 u while keeping the width constant raises the drain current to 75.39 uA, which could be attributed to reduced short-channel effects such as drain-induced barrier lowering or improved carrier mobility in the longer channel at this moderate VGS, allowing for unexpectedly higher current flow despite the typically inverse relationship. Increasing the width to 2 u with the original length of 0.13 u further elevates the drain current to 90.15 uA, as the wider channel provides additional conduction paths, scaling the current roughly proportionally to the width increase. Gate capacitances would generally scale with width due to larger area, while length variations might alter them through changes in overlap and channel components, though specific values were not provided. These variations illustrate how device dimensions influence performance, with width offering straightforward current enhancement for drive strength and length potentially introducing technology-specific behaviors that require simulation to verify, enabling tailored choices for power, speed, and area in circuit design.

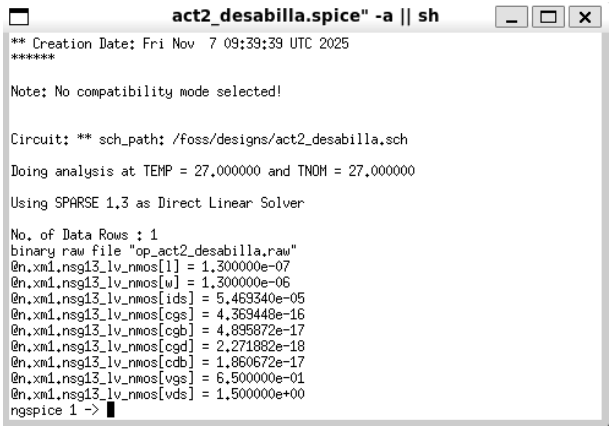

Fig. 4: Defalt (w and l at minimum)

3) Capacitance Values: The operating-point capacitance values for the low-voltage NMOS transistor reveal clear trends with device dimensions and bias conditions. Increasing the width W from 1.3 u to 2.0 u (at fixed L=0.13 u) scales most capacitances upward: Cgs rises from 0.437 fF to 0.689 fF, Cgb from 0.049 fF to 0.072 fF, and Cdb from 0.019 fF to 0.029 fF, while Cgd remains small and relatively stable around 2-3 aF;

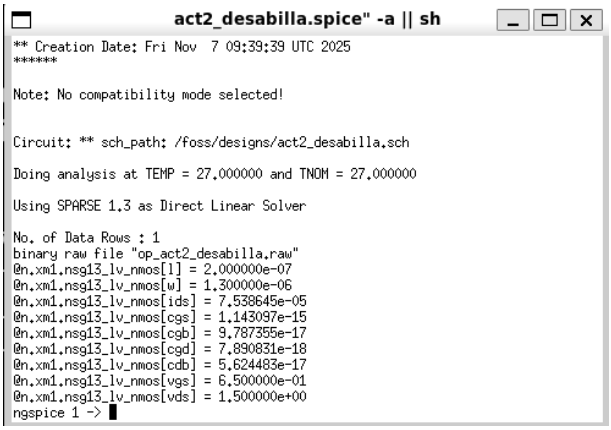

Fig. 5: Higher l

Fig. 6: Higher w

this occurs because wider transistors increase gate oxide area and junction perimeter, proportionally enlarging the dominant overlap and area-dependent components. Increasing the channel length L from 0.13 u to 0.2 u (at fixed W=1.3 u) produces mixed effects: Cgs surprisingly increases significantly from 0.437 fF to 1.143 fF, possibly due to model-specific handling of channel capacitance in moderate inversion at this bias, while Cgb, Cgd, and Cdb show moderate changes dominated by fixed overlap contributions rather than pure channel length scaling.

Bias variations also strongly influence capacitances. Raising VGS from 0.65 V to 1.65 V (strong inversion) increases Cgs substantially from 0.437 fF to 0.741 fF as more channel charge forms under the gate, sharply reduces Cgb from 0.049 fF to 0.013 fF due to better screening by the inversion layer, and raises Cgd and Cdb moderately. Lowering VGS to 0.25 V (subthreshold/cutoff) collapses Cgs to near zero (1.48 aF), increases Cgb to 0.109 fF as the gate couples more directly to the bulk, and yields very small or slightly negative Cgd (a common modeling artifact for overlap in cutoff). Changing VDS shows milder effects: increasing VDS from 0.5 V to 2.5 V (still in saturation) slightly reduces Cgs and Cgb while decreasing Cgd and Cdb, reflecting minor modulation of channel pinch-off and junction depletion regions. Overall,

width primarily scales capacitances linearly for drive strength trade-offs, length has complex model-dependent impacts, and VGS exerts the strongest control by shifting the transistor between cutoff, moderate, and strong inversion regimes, while VDS influences capacitances only weakly in saturation.

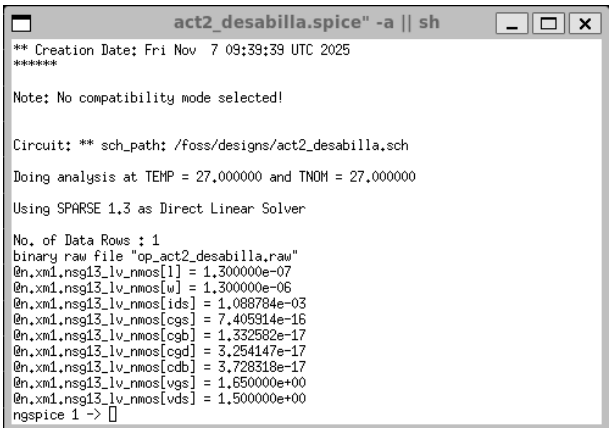

Fig. 7: Higher VGS

Fig. 8: Lower VGS

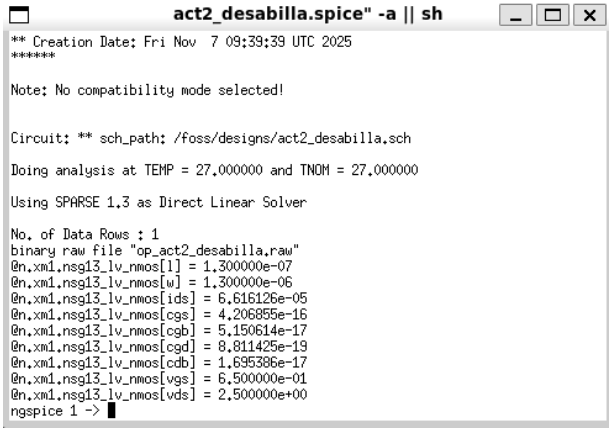

Fig. 9: Higher VDS

4) What are CGD and CDG?: In ngspice (and most SPICE-based simulators), MOSFET models report both Cgd (gate-to-drain capacitance) and Cdg (drain-to-gate capacitance) even

Fig. 10: Lower VDS

though physically they represent the same overlapping oxide capacitance between gate and drain regions. They are listed separately because the model uses reciprocal capacitances in the admittance matrix for small-signal analysis, where Cgd is the capacitance seen from the gate node to the drain, and Cdg is the reciprocal seen from the drain to the gate; in quasi-static models, these are typically equal in magnitude but can differ slightly due to charge partitioning. Negative values for Cgd (or occasionally Cdg) commonly appear in certain bias regions, particularly in saturation or near cutoff, as a modeling artifact arising from the non-reciprocal nature of transcapacitances in charge-based models (e.g., Meyer or BSIM formulations), where the total charge conservation requires one direction to exhibit negative capacitance to correctly represent the Miller effect and channel charge response to voltage changes. This negative value has no physical meaning as a standalone capacitor but ensures accurate small-signal gain and frequency response in circuit simulations.

B. Building testbenches in Xschem

1) Drain Current and Capacitances: The simulation results from identical testbenches (L = 0.45 u, W = 1.3 u) comparing low-voltage (LV) and high-voltage (HV) MOSFETs in the same technology reveal significant performance differences. For NMOS devices biased at VGS = 0.65 V and —VDS— = 1.5 V, the LV NMOS delivers the highest drain current at approximately 64.6 uA, while the HV NMOS produces only 1.67 uA—nearly 40 times lower—due to its thicker gate oxide, lower carrier mobility, and higher threshold voltage designed for greater voltage handling rather than speed or drive strength. For PMOS devices biased at VGS = 0.85 V (to achieve comparable overdrive), the LV PMOS yields around 65.3 uA, substantially higher than the 31.5 uA from the HV PMOS, again reflecting the trade-off where HV devices sacrifice current capability for improved breakdown voltage and reliability. Between LV devices, the NMOS and PMOS show very similar drain currents (64.6 uA vs 65.3 uA), indicating well-balanced electron and hole mobilities in this low-voltage process. Capacitance values also differ markedly. LV devices generally exhibit higher gate capacitances (Cgs around 3.7–4.5 fF) compared to HV devices (Cgs around 0.75–1.9 fF),

primarily because thinner gate oxides in LV transistors result in higher oxide capacitance per unit area. HV devices show lower Cgs and Cgb, consistent with thicker oxides reducing capacitive coupling, though junction capacitances like Cdb remain small across all variants. The negative Cgd in the HV NMOS is a typical modeling artifact in saturation arising from non-reciprocal charge partitioning. Overall, for a given W and L, low-voltage transistors provide significantly higher drain current and larger parasitic capacitances, making them suitable for high-speed core logic, whereas high-voltage transistors offer much lower drive strength but are essential for I/O or analog circuits requiring higher voltage tolerance.

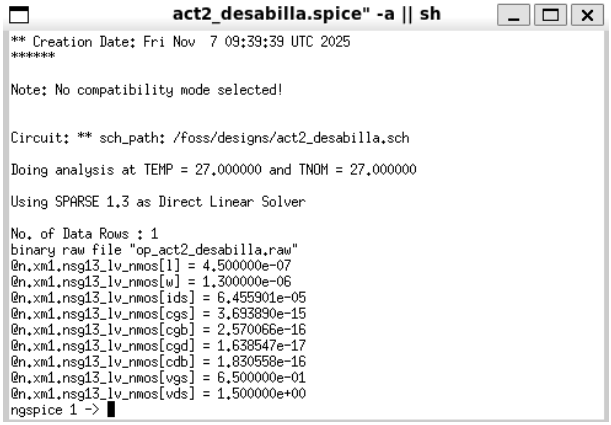

Fig. 11: LV NMOS

Fig. 12: LV PMOS

2) Ideal Ratio for Inverter Design: The ideal Wp / Wn ratio for a CMOS inverter is approximately 1, as the low-voltage NMOS and PMOS devices exhibit nearly matched drive currents (around 65 uA) for identical dimensions and comparable overdrive biases, suggesting balanced electron and hole mobilities in this process. Designers frequently deviate from this exact ratio to achieve symmetric noise margins, adjust rise/fall times for timing requirements, minimize area or power, or compensate for layout parasitics and process variations.

3) Rationale when designing circuits: Low-voltage (thin-oxide) transistors are preferred for core digital logic, high-

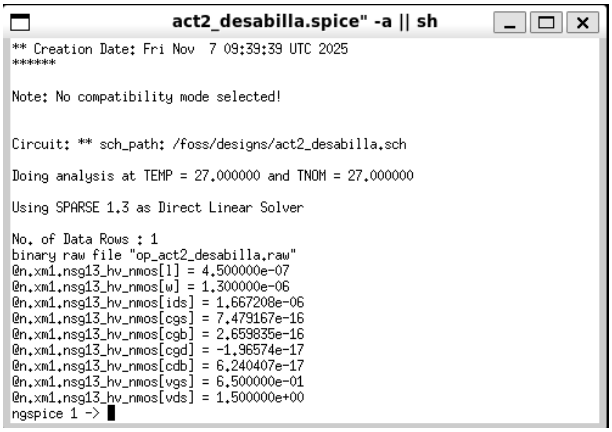

Fig. 13: HV NMOS

Fig. 14: HV PMOS

speed analog/RF circuits, and low-power applications where higher drive strength, greater transconductance, and optimized performance are critical due to their thinner gate oxide. High-voltage (thick-oxide) transistors are selected for I/O interfaces, analog sections with larger signal swings, power management, or reliability-sensitive blocks that demand higher breakdown voltage and lower gate leakage, even though they provide reduced current drive and speed.

C. Build a test bench to explore the body effect

1) What happens when VSB is not equal to 0?: When VSB is not equal to 0 (specifically positive VSB = +1 V in this case, as achieved by biasing the body lower than the source), the body effect comes into play in the NMOS transistor. The reverse bias between source and body widens the depletion region around the channel, increasing the threshold voltage Vth. As a result, for the same VGS = 0.65 V and VDS = 1.5 V, the drain current Id decreases significantly—from 54.69 uA (VSB = 0) to 25.53 uA (VSB not equal to 0)—because a higher Vth requires a stronger gate overdrive to form the same inversion charge and achieve equivalent conduction. The gate capacitances also change: Cgs drops from 0.437 fF to 0.346 fF due to reduced channel inversion strength, Cgb slightly decreases, and Cdb halves, reflecting the wider depletion region. Cgd becomes slightly negative (a modeling

artifact common in saturation with body bias). Overall, non-zero positive VSB reduces drive current and transconductance while altering parasitic capacitances, which is why designers typically tie body to source (VSB = 0) in digital circuits to maximize performance, but may exploit controlled body bias in analog designs for tuning or in stacked transistors where VSB inevitably arises.

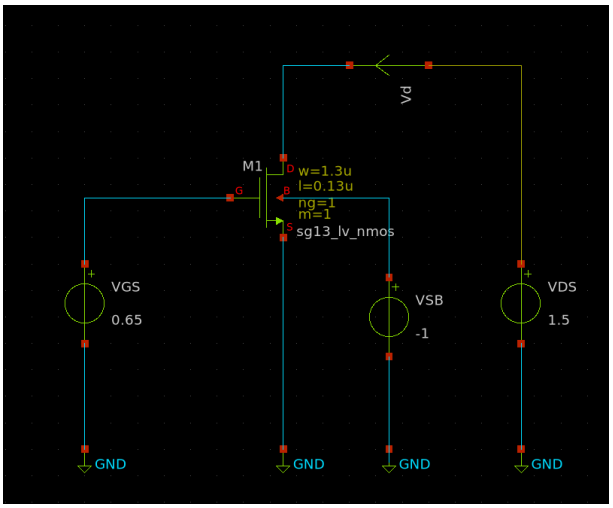

Fig. 15: Testbench when VSB is not Equal to 0

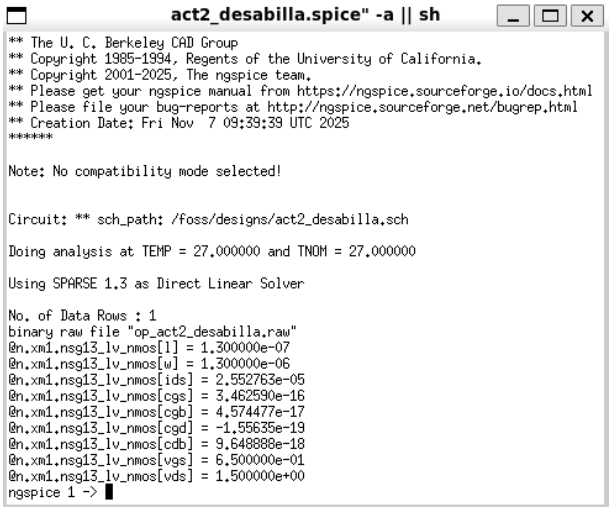

Fig. 16: Results when VSB is not Equal to 0

III. All Codes

IV. Conclusion

This laboratory activity provided a comprehensive characterization of MOSFET devices in an open-source BiCMOS technology using Xschem and ngspice within the IIC-OSIC-TOOLS environment. The simulations successfully demonstrated fundamental NMOS behavior, including the effects of VGS and VDS on drain current in triode and saturation regions, the influence of device dimensions (W and L) on current drive and parasitic capacitances, and bias-dependent variations in gate and junction capacitances. Comparisons

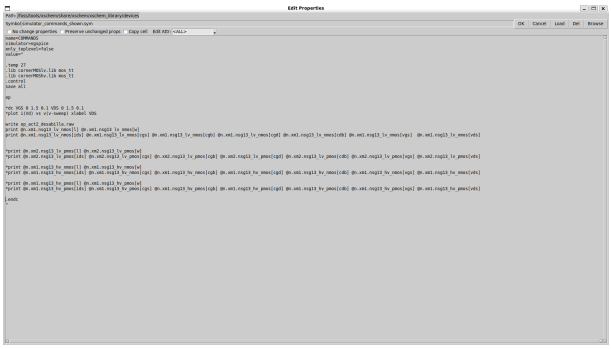

Fig. 17: All Codes Used

between low-voltage and high-voltage transistors highlighted the performance trade-offs between drive strength/speed and voltage handling/reliability, with LV devices offering superior current capability and HV devices prioritizing breakdown tolerance. The exploration of the body effect confirmed the increase in threshold voltage and reduction in drain current with positive VSB, underscoring its impact in stacked or analog circuits. These results align well with MOSFET theory, validate the accuracy of the open-source PDK models, and illustrate practical considerations for device selection, sizing (e.g., near-unity Wp/Wn ratio for balanced inverters), and bias management in modern analog and digital circuit design.

References

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