VladimirZelenkovskii

Hardware Engineering Intern

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StackOverFlow
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English
LSI London, UK
Advanced Certificate 2012

Education

2013 - 2017 **Lomonosov Moscow State University** — Bachelor's degree
Faculty of Computational Mathematics and Cybernetics
Chair of High Performance Computing, Parallel Computations and Quantum Informatics

Programming Experience

3 years	**C++**	STL / Boost / template-based & virtual hierarchy / OOP design patterns / serialization
4 years	**C**	searching / sorting / structuring / process management / system calls / POSIX / signals
3 years	**Assembler**	disassembling / cache misses / optimization / efficient trees & lists & stacks
2 years	**Python**	Cython / numerical calculations / machine learning / data mining / OS & web
2 year	**Parallel Computations**	CUDA / multi-GPU / Intel TBB / MPI / OpenMP / METIS
4 years	**Linux**	kernel calls / pthreads / bash scripts / file descriptors
2 years	**Task Debugging & Profiling**	GDB / code instrumentation
2 years	**Databases**	postgreSQL / MongoDB / first-order predicate logic
version-ctl	**P4 / SVN / Git**	

Electronic Engineering Experience

Sept' 15 - Current Time

Cadence Design Systems — Development Intern

Working on industry's fastest, most accurate Extraction product (C / C++ / Python). Finished a big variety of circuit debugging cycles for TSMC / Texas Instruments foundries, made contributions in physical extraction for IC modules, implemented network devices' recognition in symmetrical system-on-chip designs.

★★★★☆ **Manufacturing** — monocrystal substrate / cutting / grinding / schematic / layout
Familiar with the design process from schematic and layout to circuit design tools and production equipment.
1 year experience in digital logic design: Verilog / VHDL / SystemC

★★★★☆ **Synthesis** — photolithography / photoresist / tech mask / reticles / oxidation / etching
1 year experience in circuits debugging and contributing Schematics / GDS / SPEF / SPICE / DRC & LVC layouts.

★★★★★ **Verification & Extraction** — signal delay & noise, IR drops
Working on a Monte-Carlo Field Solver in a highly competitive industry environment. Performing extraction on each IC xtor / cell levels.

July - August 2015

Intel Corporation — Summer Internship

Headed rapid development and productionisation of multithreading composability of Intel Xeon Phi co-processors for adaptive workload balancing support. Successfully achieved common performance speedup. All developments have become part of the Intel co-processors' internals, released **24 Nov 2015**.