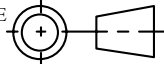
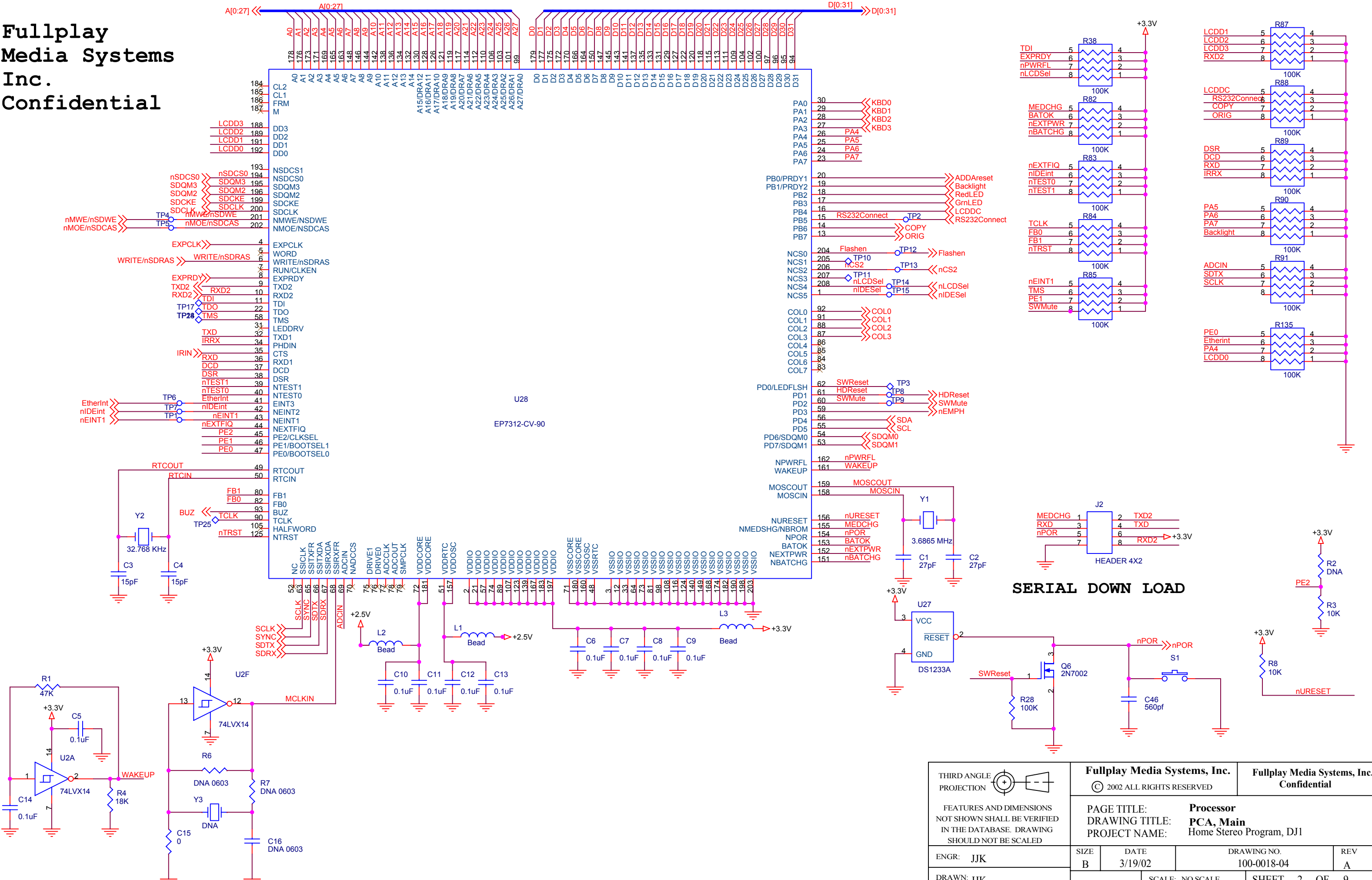


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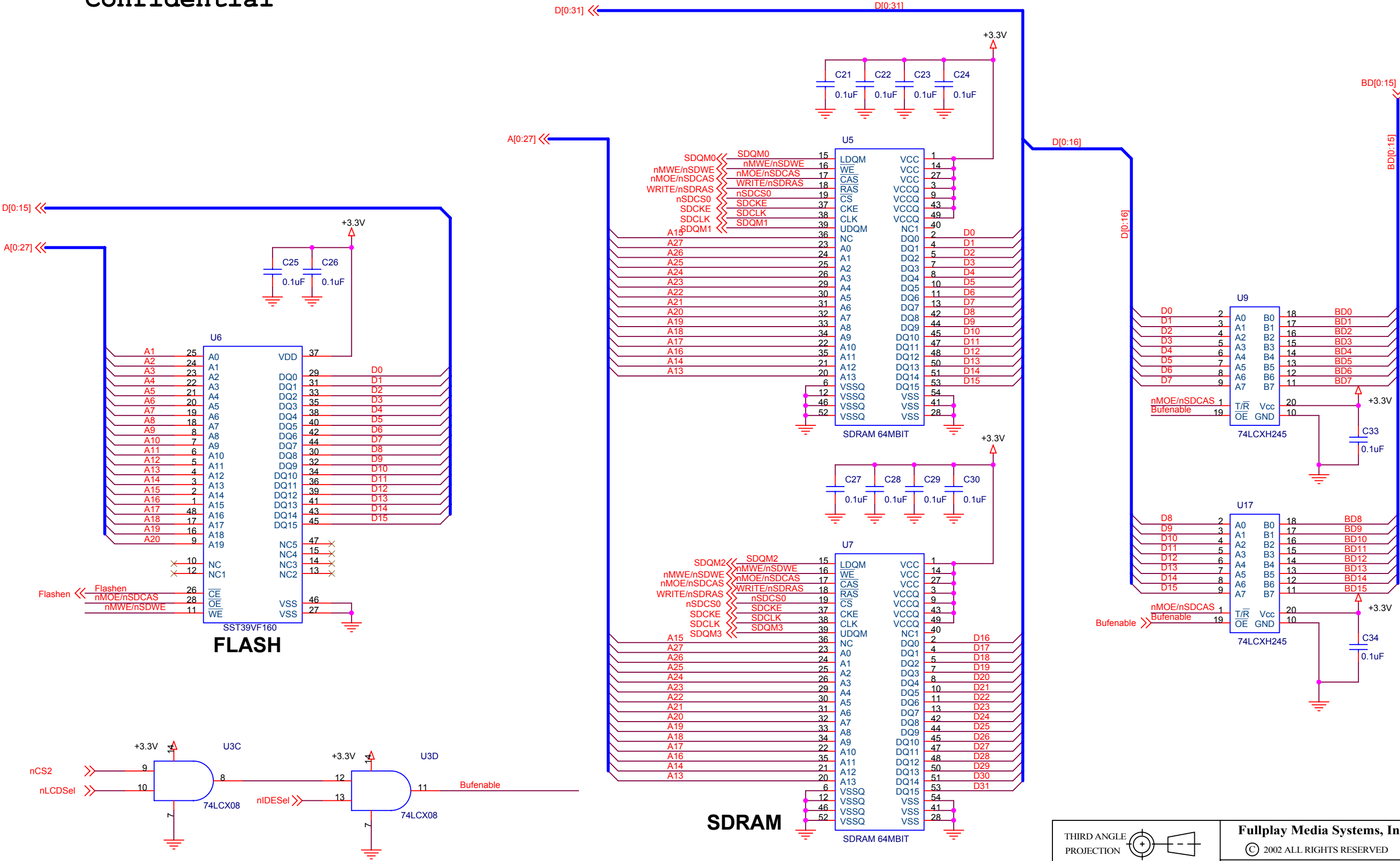
REVISION:	X1		
CHECKED BY:			
APPROVED BY:			
X1	PRE RELEASE JJK		
X2	ADDED AUDIO AMP CIRCUIT AND XILINX CPLD JJK		
X3	Added C127 and C132 Changed Filter caps on 42L50 to Analog Ground. 7/25/02 JJK		
X4	Fixed the symbols for QQ3,Q4,Q5,Q6 Source and Drain were swapped. 8/02/02 JJK		
X5	Moved RS232Connect from PD3 (u23 Pin 59) to PB5 (u23 Pin 15) Net at PB5 was named ACLKCSel. Added GNDTP 1-10. Renamed NET PB2 to RedLED renamed NET PB3 to GrnLED. 8/08/02 JJK Added C133 470pF NPO 0603.		
X6	Created the NET +12VF, moved L6 to +12VF	8/12/02	JJK
X7	Changed C46 from 0.1uf to 560pF	8/15/02	JJK
X8	Changed S1 to PN 960005	8/16/02	JJK
A	Proto Release Changed U9, U17, U14, U16,U24 to 74LCXH245; DNA'd R7, Y3, R6, C16; Relplaced C15 with 0 Ohm, Replaced R79, R80, R60, R67, R128, R134 with 562 Ohm 0603.  Renamed net nEthernetSel to nCS2 from U28 to U15 and U21 Created nets nMOEslow and nMWESlow, Re routed nEthernetSel going from U15 and U21 to U19 Moved U19 onto nets nMOEslow and nMWESlow.  Changed U22 CS8405 to hardware mode (changed the symbol, moved pin 1 from SDA to a new net called ORIG moved pin 2 from ground to +5V moved pin 3 from gnd to a new net called nEMPH, connected pins 10,11,16,17,18, to gnd, moved pin 19 from nEINT1 to gnd,moved pin 20 from R73 to +5V, moved pin 23 from +3.3V to +5V, move pin 24 from gnd to +5V, and moved pin 28 from SCL to a new net called ORIG.) Connected U28 pin 14 (PB6) to net COPY Connected U28 pin 13 (PB7) to net ORIG, Connected U28 pin 59 (PD3) to net nEMPH. Replaced C127 and C132 with 2200pF, replaced C37 with 10uF Tant. Disconnected U33 and U35 pin 1 from the Audio Removed C78,C79,C83,C84. Replaced R75 and R76 with 5.76K 5% 9/24/02 JJK		

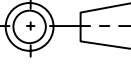
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DRAWN: JJK		SCALE: NO SCALE	SHEET 1 OF 9	

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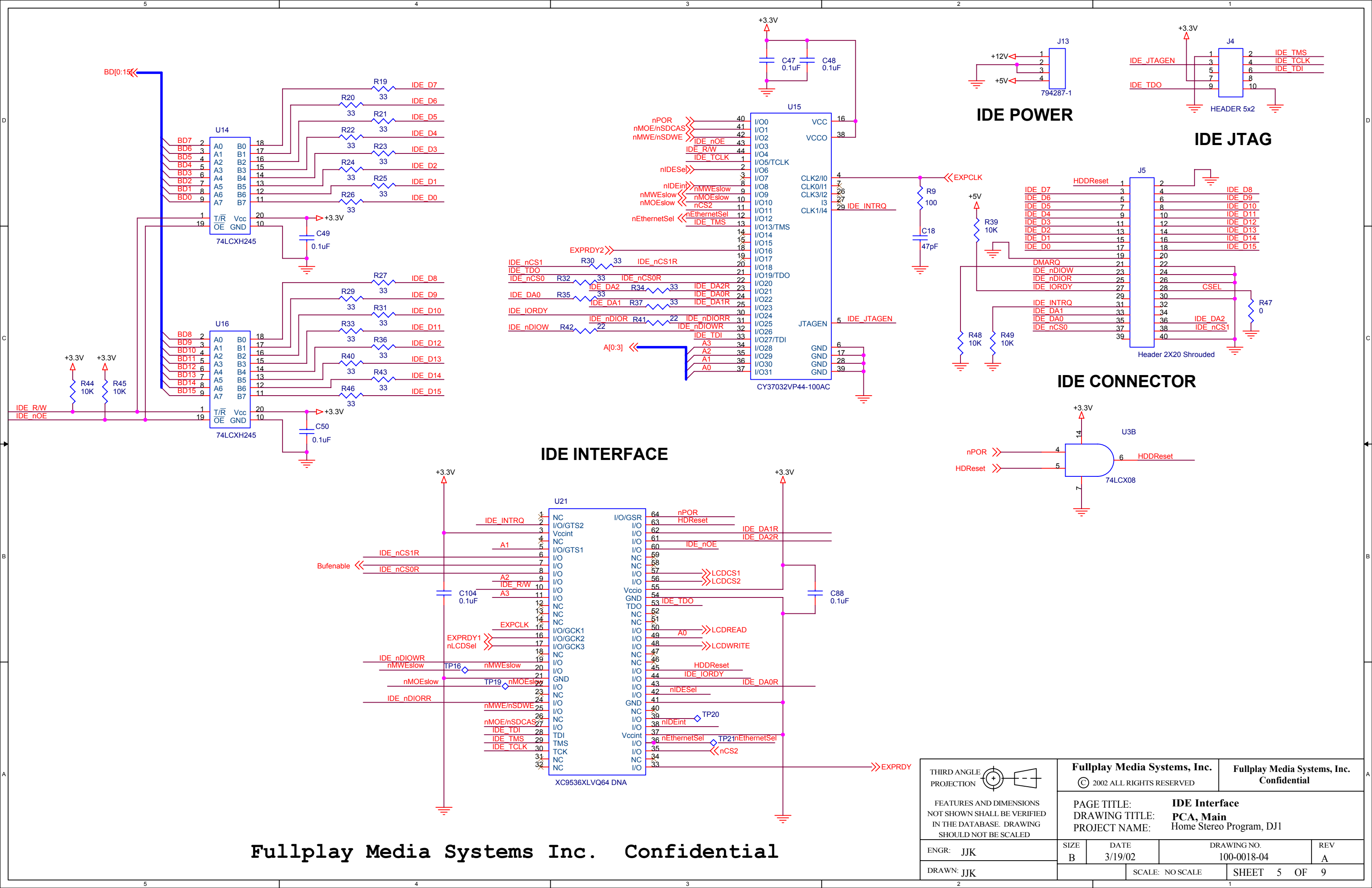
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		SHEET 3 OF 9		



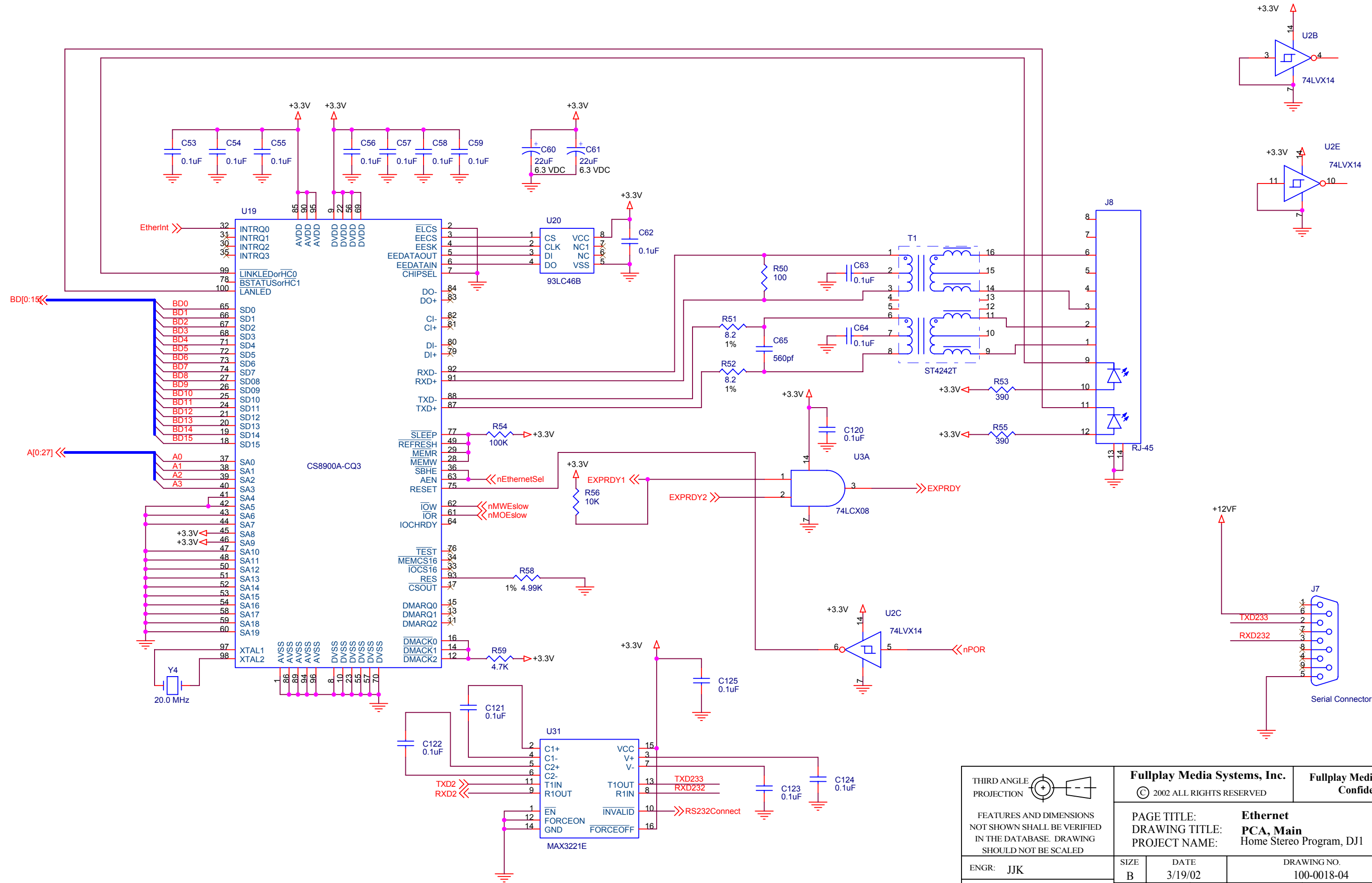
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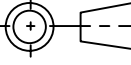


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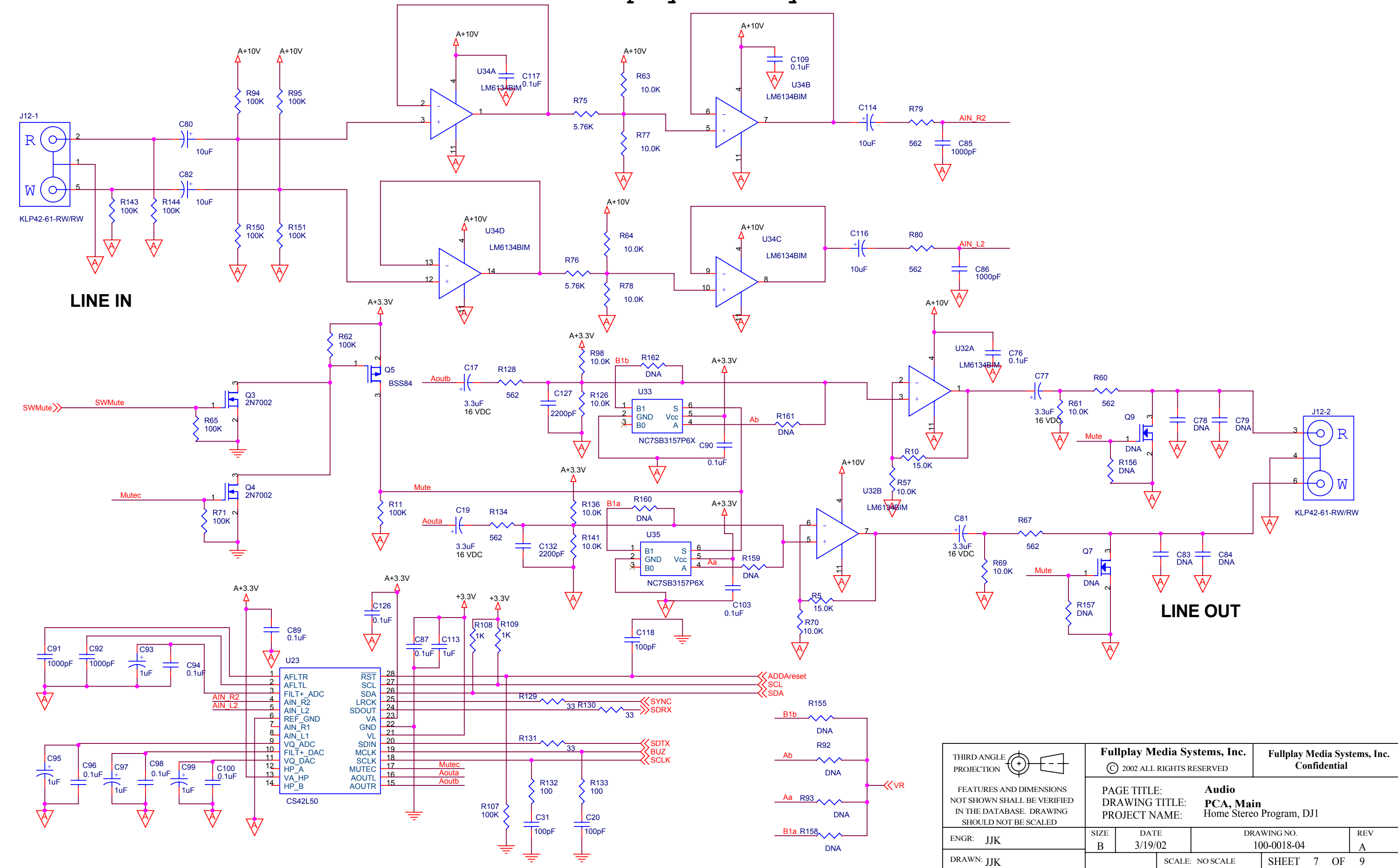


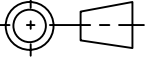
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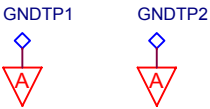
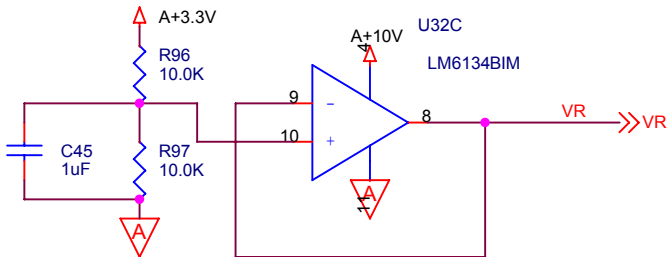
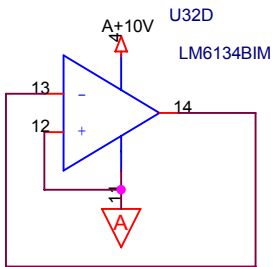
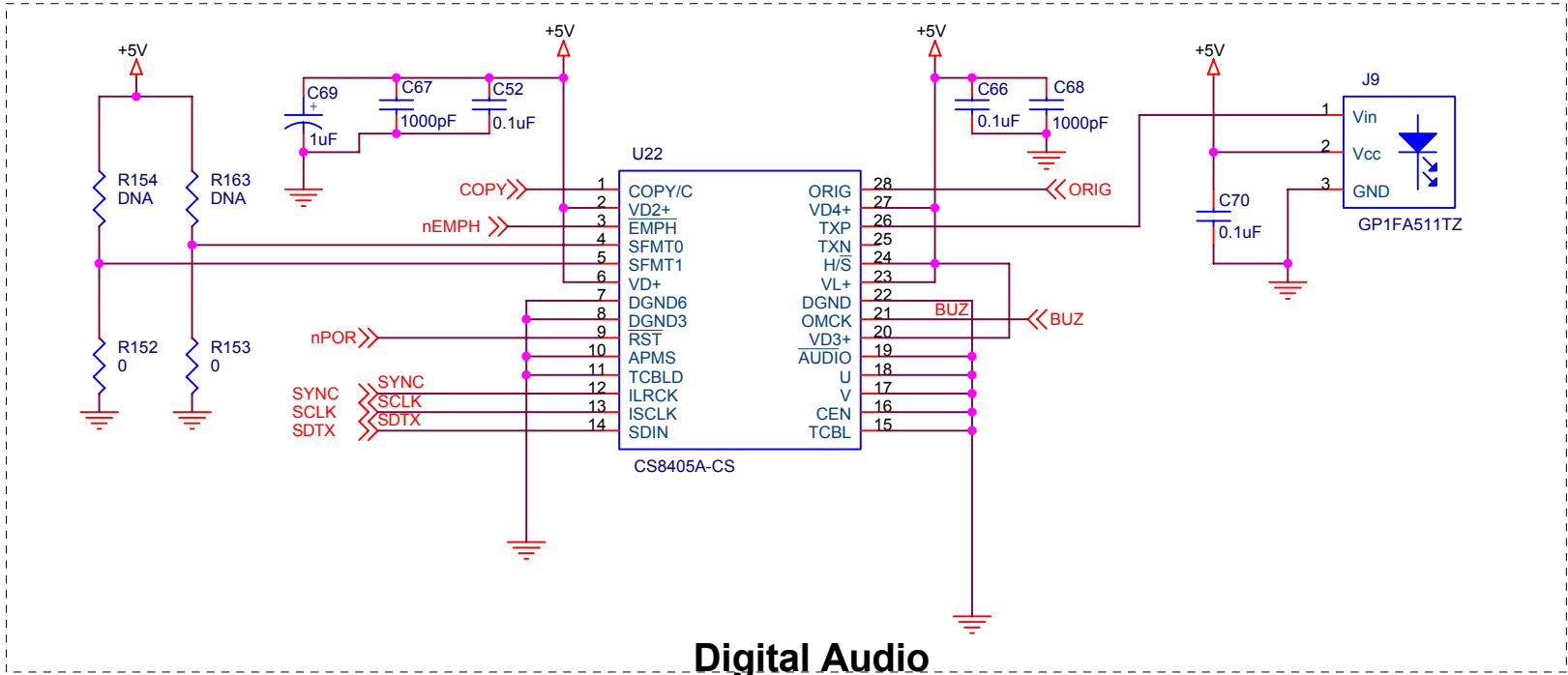
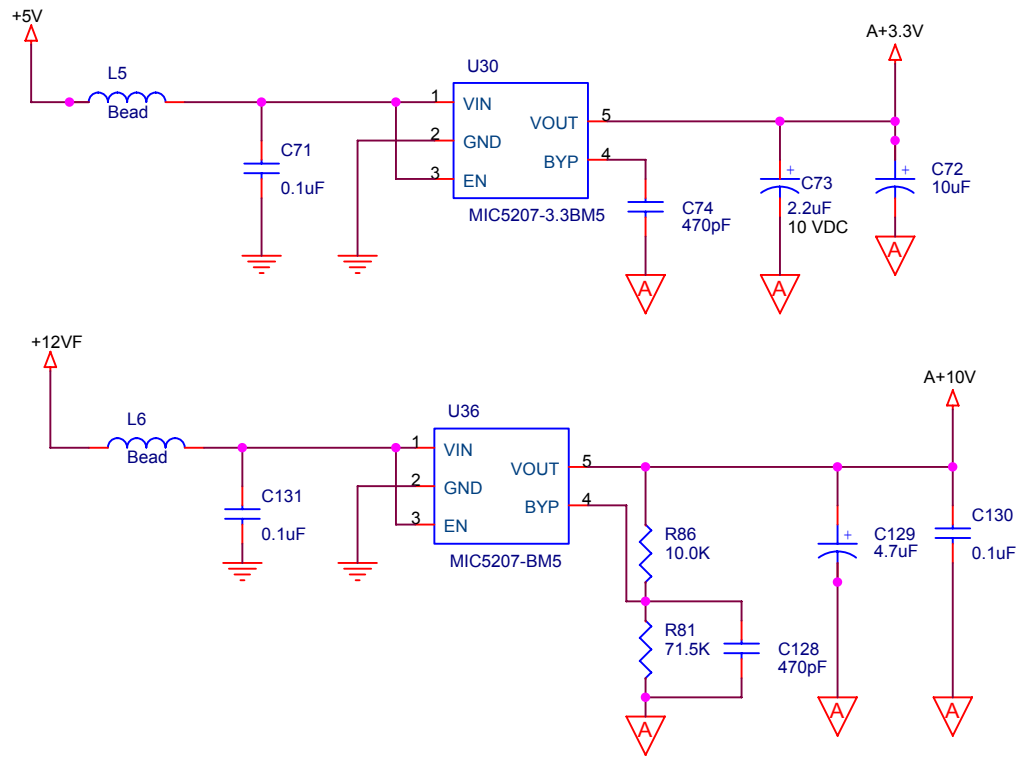


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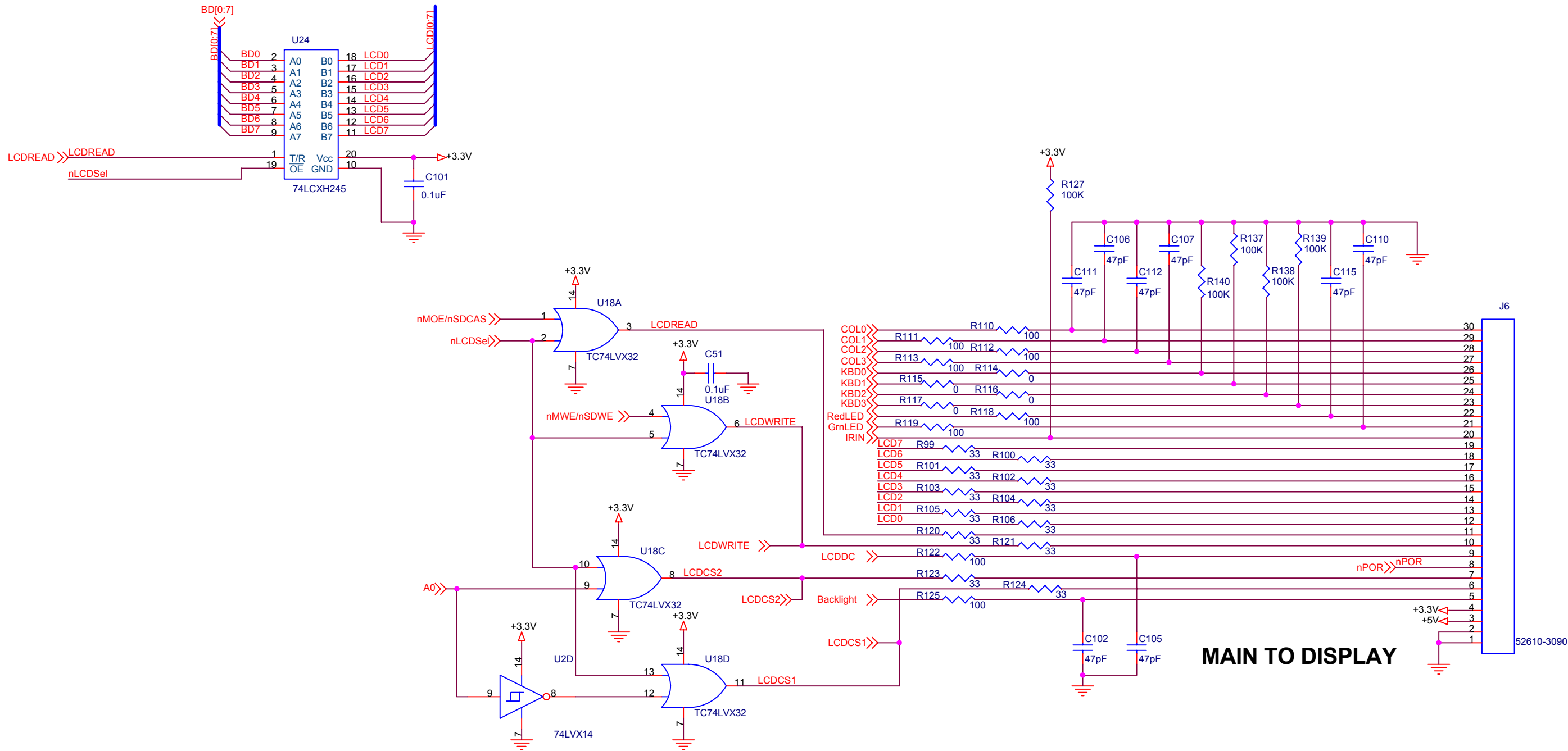
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