CDB53L32A

Evaluation Board for CS53L32A

Features

- Demonstrates recommended layout and grounding arrangements
- CS8404A generates AES/EBU, S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system
- Patch Area

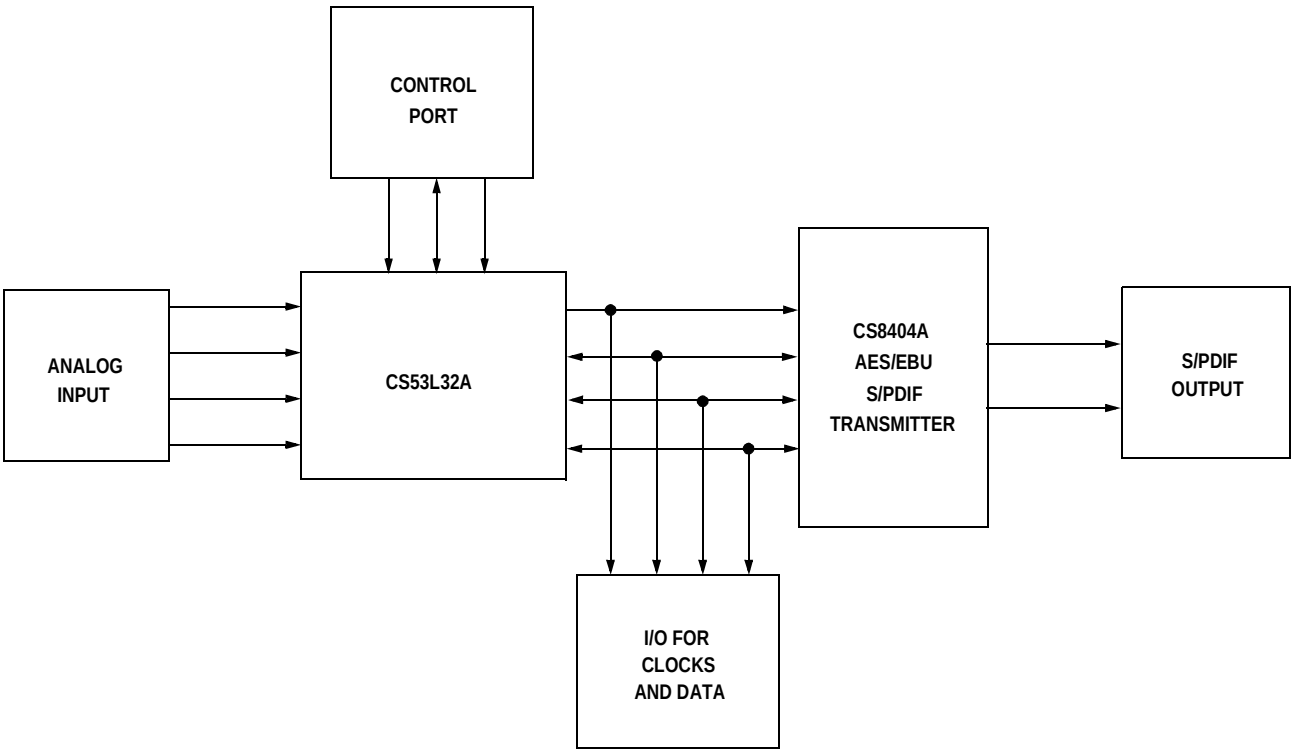
Description

The CDB53L32A evaluation board is an excellent means for quickly evaluating the CS53L32A 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, a PC for controlling the CS53L32A (in control port mode) and a power supply.

Also included is a CS8404A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB53L32A Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

Copyright © Cirrus Logic, Inc. 2000
(All Rights Reserved)

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

I^2C is a registered trademark of Philips Semiconductors.
SPI is a registered trademark of International Business Machines Corporation.

Preliminary product information describes products which are in production, but for which full characterization data is not yet available. Advance product information describes products which are in development and subject to development changes. Cirrus Logic, Inc. has made best efforts to ensure that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). No responsibility is assumed by Cirrus Logic, Inc. for the use of this information, nor for infringements of patents or other rights of third parties. This document is the property of Cirrus Logic, Inc. and implies no license under patents, copyrights, trademarks, or trade secrets. No part of this publication may be copied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means (electronic, mechanical, photographic, or otherwise) without the prior written consent of Cirrus Logic, Inc. Items from any Cirrus Logic website or disk may be printed for use by the user. However, no part of the printout or electronic files may be copied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means (electronic, mechanical, photographic, or otherwise) without the prior written consent of Cirrus Logic, Inc.Furthermore, no part of this publication may be used as a basis for manufacture or sale of any items without the prior written consent of Cirrus Logic, Inc. The names of products of Cirrus Logic, Inc. or other vendors and suppliers appearing in this document may be trademarks or service marks of their respective owners which may be registered in some jurisdictions. A list of Cirrus Logic, Inc. trademarks and service marks can be found at http://www.cirrus.com.

1. CDB53L32A SYSTEM OVERVIEW

The CDB53L32A evaluation board is an excellent means of quickly evaluating the CS53L32A. The CS8404A digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB53L32A schematic has been partitioned into 10 schematics shown in Figures 2 through 11. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS53L32A ANALOG TO DIGITAL CONVERTER

A description of the CS53L32A is included in the CS53L32A datasheet.

3. CS8404A DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8404A Digital Audio Transmitter, Figure 8. The outputs of the CS8404A are RS422 compatible differential line drivers. The operation of the CS8404A and a discussion of the digital audio interface are included in the CS8404A datasheet.

Note: The CS8404 can not be the master clock source for the board

4. CS8404A DATA FORMAT

The CS8404A data format can be set with headers M0, M1, and M2 as described in the CS8404A datasheet. The format selected must be compatible with the data format of the CS53L32A, as shown in the CS53L32A datasheet. Please note that the CS8404A does not support all the possible modes of the CS53L32A.

5. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, HDR8. The schematic for the clock/data input/output is shown in Figure 7.

The CDB53L32A allows some flexibility as to the generation of MCLK. When in slave mode you may internally generate MCLK on board and receive SLCK and LRCK by setting HDR 9, 10, and 11 to 'EXT'. Generating MCLK internally on the CDB53L32A while in slave mode improves performance due to jitter effects which can occur from long cable lengths used to transmit MCLK to the CDB53L32A. If you wish to provide MCLK externally set HDR 9 and 10 to 'INT' and HDR 11 to 'EXT'

In Master mode if you wish to provide MCLK externally via HDR8 set HDR 9 and 10 to 'EXT' and HDR 11 to 'INT'.

6. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (GND, +5 V, VA, VL), see Figure 11. The +5 V input supplies power to the +5 V digital circuitry (VDD) and the amplifiers (VAA), while the two +1.8/+3.3 V inputs supply power to the VA and VL pins of the CS53L32A and to the level shifter circuits.

WARNING: Please refer to Table 1 for allowable voltages levels.

7. GROUNDING AND POWER SUPPLY DECOUPLING

The CS53L32A requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 details the power distribution used on this board. The decoupling capacitors are located as close to the CS53L32A as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

8. CONTROL PORT SOFTWARE

The CDB53L32A is shipped with Windows based software for interfacing with the CS53L32A control port via the DB25 connector, J2. The software can be used to communicate with the CS53L32A in either SPI® or Two Wire mode; however, in SPI mode the CS53L32A registers are write-only.

Note: The Two Wire control port mode is compatible with the I^2C® protocol.

9. CDB53L32A PERFORMANCE PLOTS

The CDB53L32A performance plots, shown if figures 12 through 16, were generated using the Audio Precision System Two Cascade. All tests were performed at a sampling rate of 48 kHz and with VA and VL as indicated, and the +5 V post at 5 V.

10. CDB53L32A A.0 ERRATA

- A 47.5 kohm resistor has been added on the bottom side of the board between the testpoint labled SDATA and the center stake of HDR6. This resistor satisfies the stand-alone pullup/pulldown requirement on SDOUT to choose between master/slave operation of the CS53L23A
- Pin 15, CBL, on the CS8404 is now floating, instead of being connected to ground. CBL is the channel status block output for the CS8404 and should have been floating in the original schematic.
- Pin 4 on U5 was disconnected in order to resolve bus contention issues on the SCLK line. Because of this modification the CS8404 can no longer act as Master for the CS53L32A. In order to test the CS53L32A in slave mode, provide external clocks to HDR8 (see Table 2 for info on how to set jumpers).

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	Input	+ 5 Volt power
VA	Input	+ 1.8 to + 3.3 Volt power for the CS53L32A
VL	Input	+ 1.8 to +3.3 Volt power for the CS53L32A
GND	Input	Ground connection from power supply
AIN_L1	Input	Analog input 1 left channel
AIN_R1	Input	Analog input 1 right channel
AIN_L2	Input	Analog input 2 left channel
AIN_R2	Input	Analog input 2 right channel
Parallel Port	Input/Output	Parallel connection to PC for SPI / Two Wire control port signals
HDR8	Input/Output	I/O for master, serial, left/right clocks and serial data
HDR7	Input/Output	I/O for SPI / Two Wire control port signals
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
SW1	Reset	HI	Resets the CDB53L32A Rev A
HDR1	CS8404A Mode Select M0	HI *LOW	See CS8404A datasheet for details
HDR2	CS8404A Mode Select M1	HI *LOW	See CS8404A datasheet for details
HDR3	CS8404A Mode Select M2	*HI LOW	See CS8404A datasheet for details
HDR4	CS8404A clock master/slave select	*S	Must be set to 'Slave' for proper operation
HDR5	MCLK Divider	x1 *÷2 ÷4	MCLK goes directly into CS8404 (Fs = 96 kHz) MCLK is divided by two prior to CS8404 (Fs = 48 kHz) MCLK is divided by four prior to CS8404 (Fs = 24 kHz)
HDR6	CS53L32A Master/Slave Select	*M S	CS53L32A in Master mode CS53L32A in Slave mode
HDR9/HDR10	Master Clock Source Select	*INT EXT	Master clock from on-board oscillator Master clock externally supplied via HDR8
HDR11	LRCK/SCLK Source Select	*INT EXT	LRCK/SCLK is output on HDR8 LRCK/SCLK is input on HDR8
HDR12	Control Port Enable	Disable *Enable	Enable/Disable the control port
HDR13	AD0/CS/DIV	*HI LOW	See CS53L32A datasheet for details
HDR14	SDA/CDIN/DIF	*HI LOW	See CS53L32A datasheet for details
HDR15	SCL/CCLK/CHSEL	*HI LOW	See CS53L32A datasheet for details

Notes: *denotes default factory settings

Table 2. CDB53L32A Jumper and Switch Settings

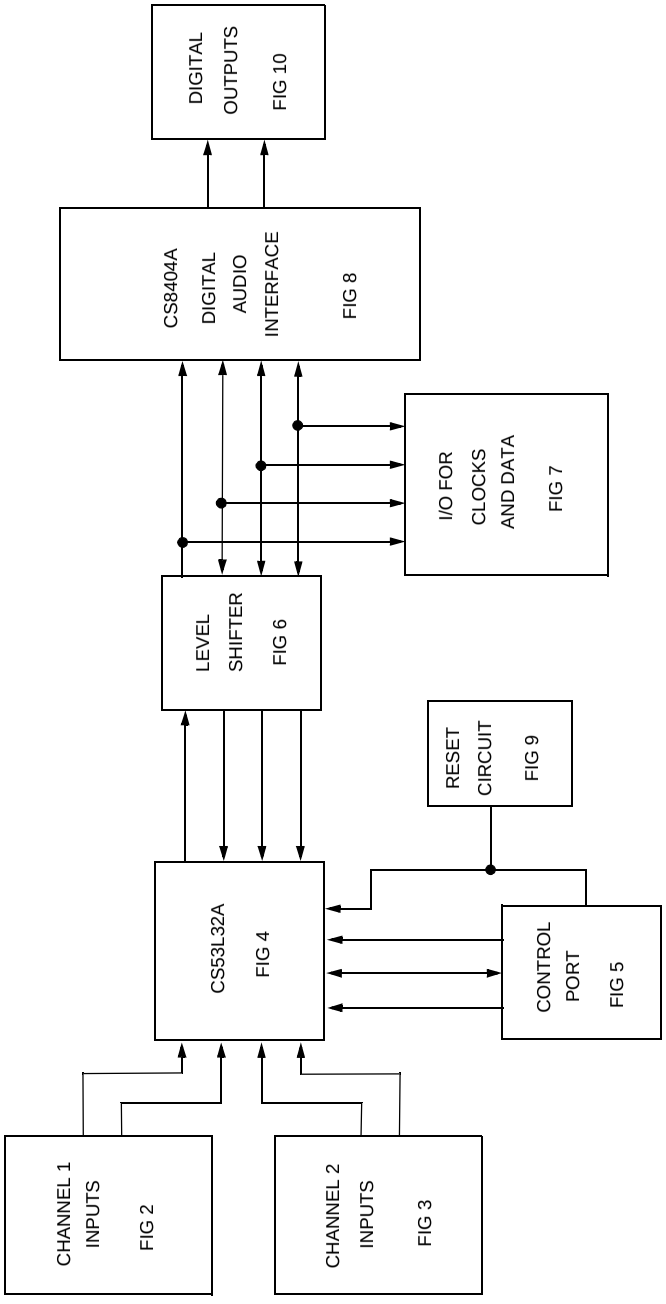


Figure 1. System Block Diagram and Signal Flow

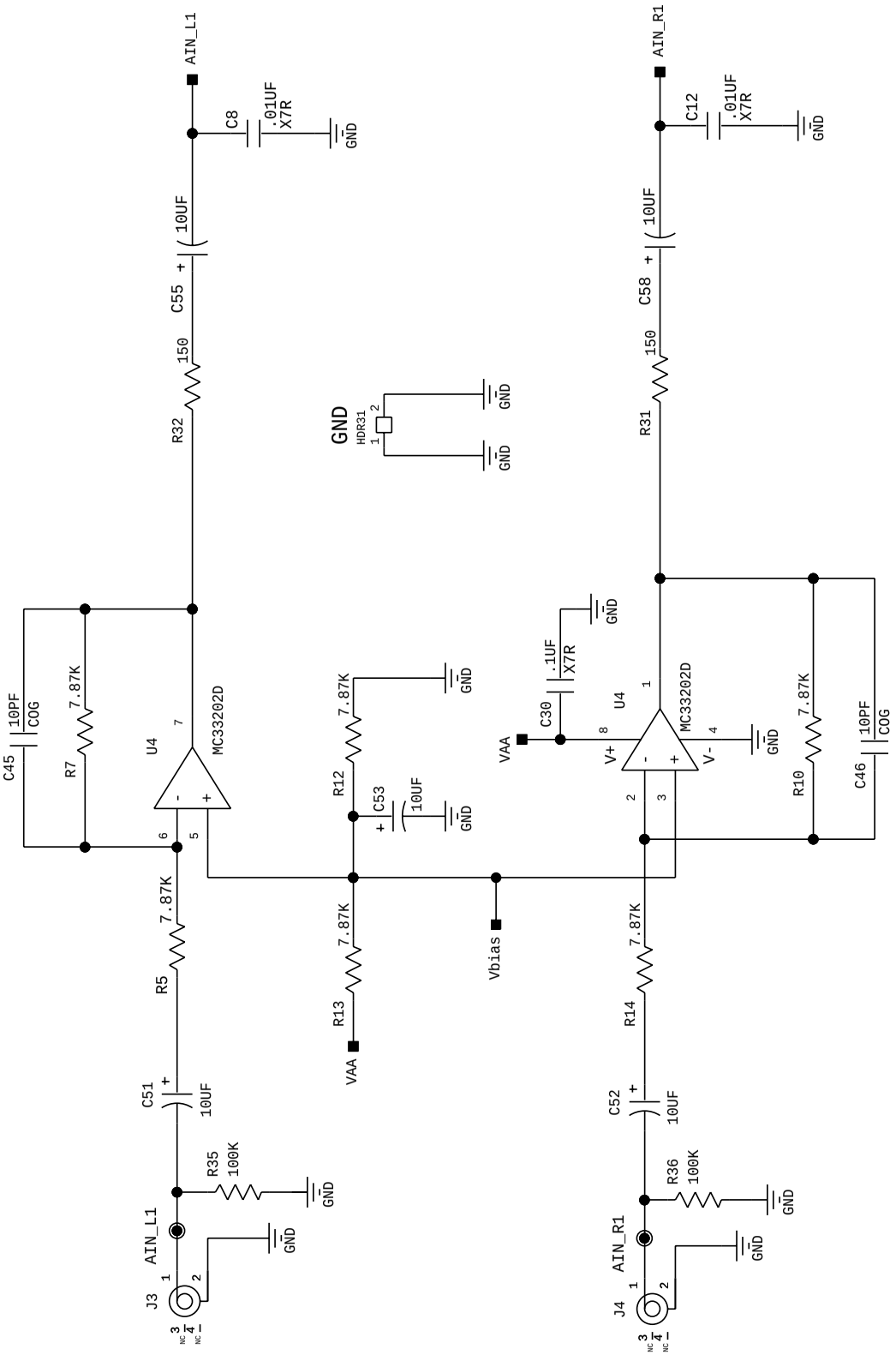


Figure 2. Channel 1 Analog Input

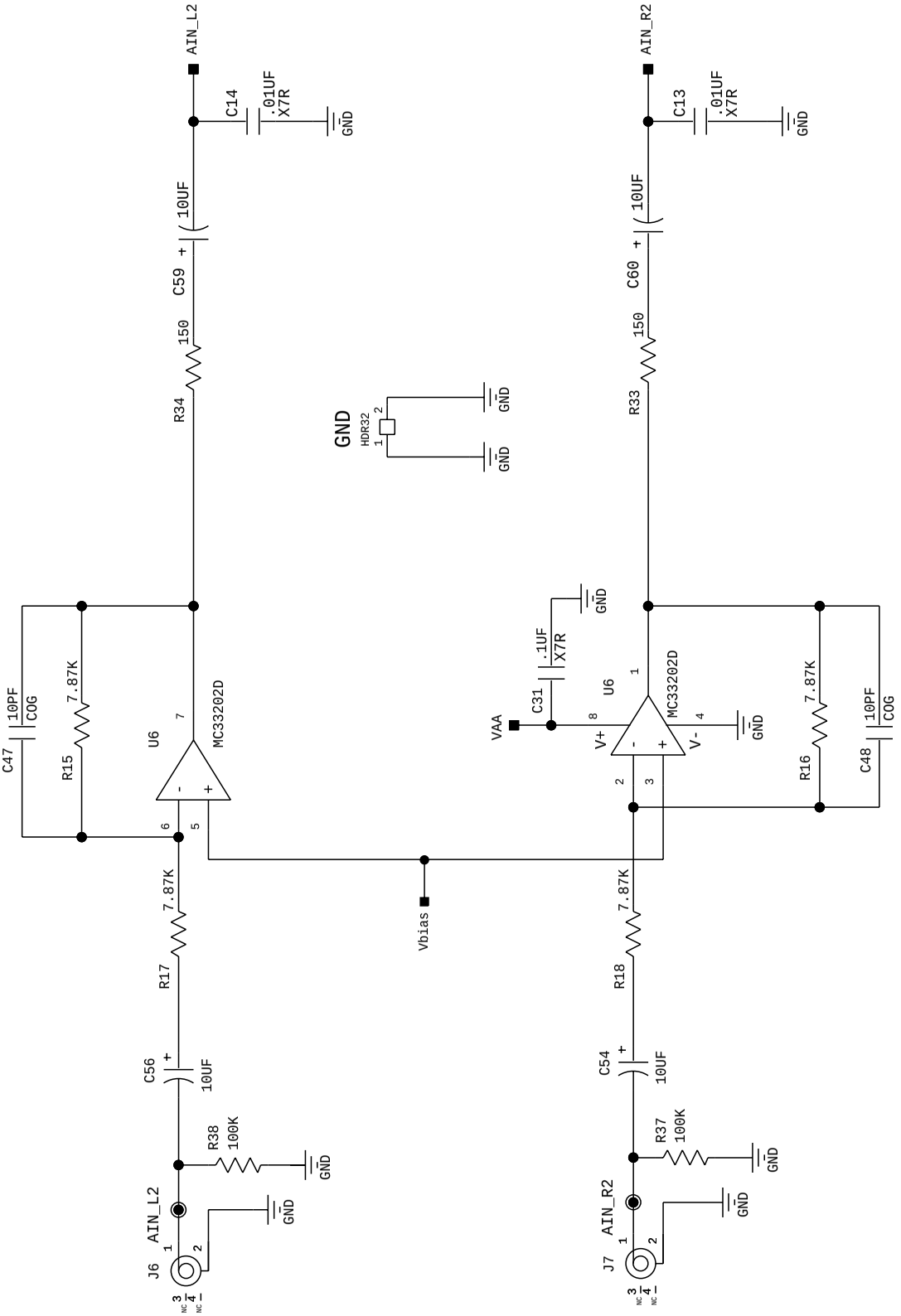


Figure 3. Channel 2 Analog Input

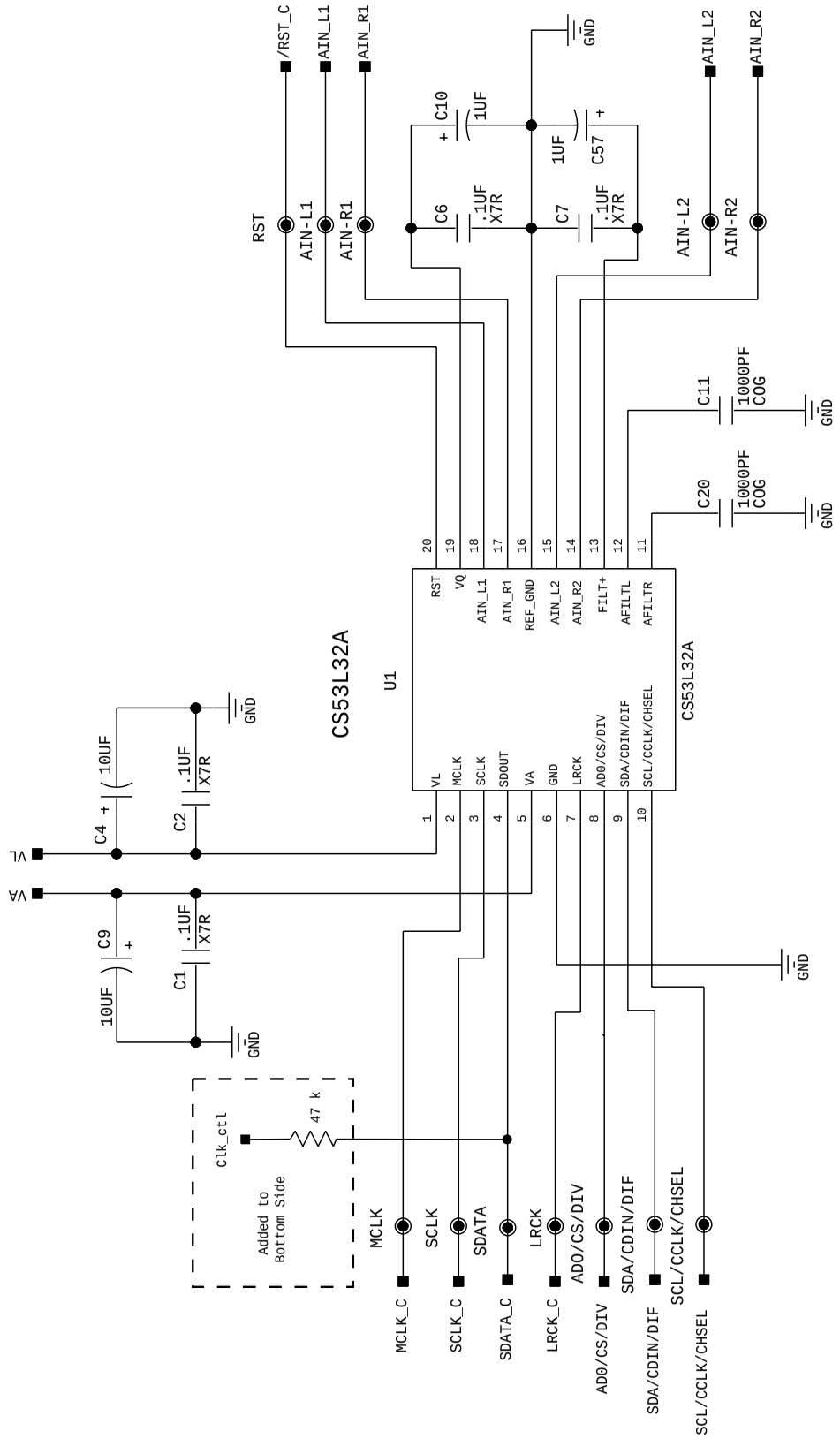


Figure 4. CS53L32A

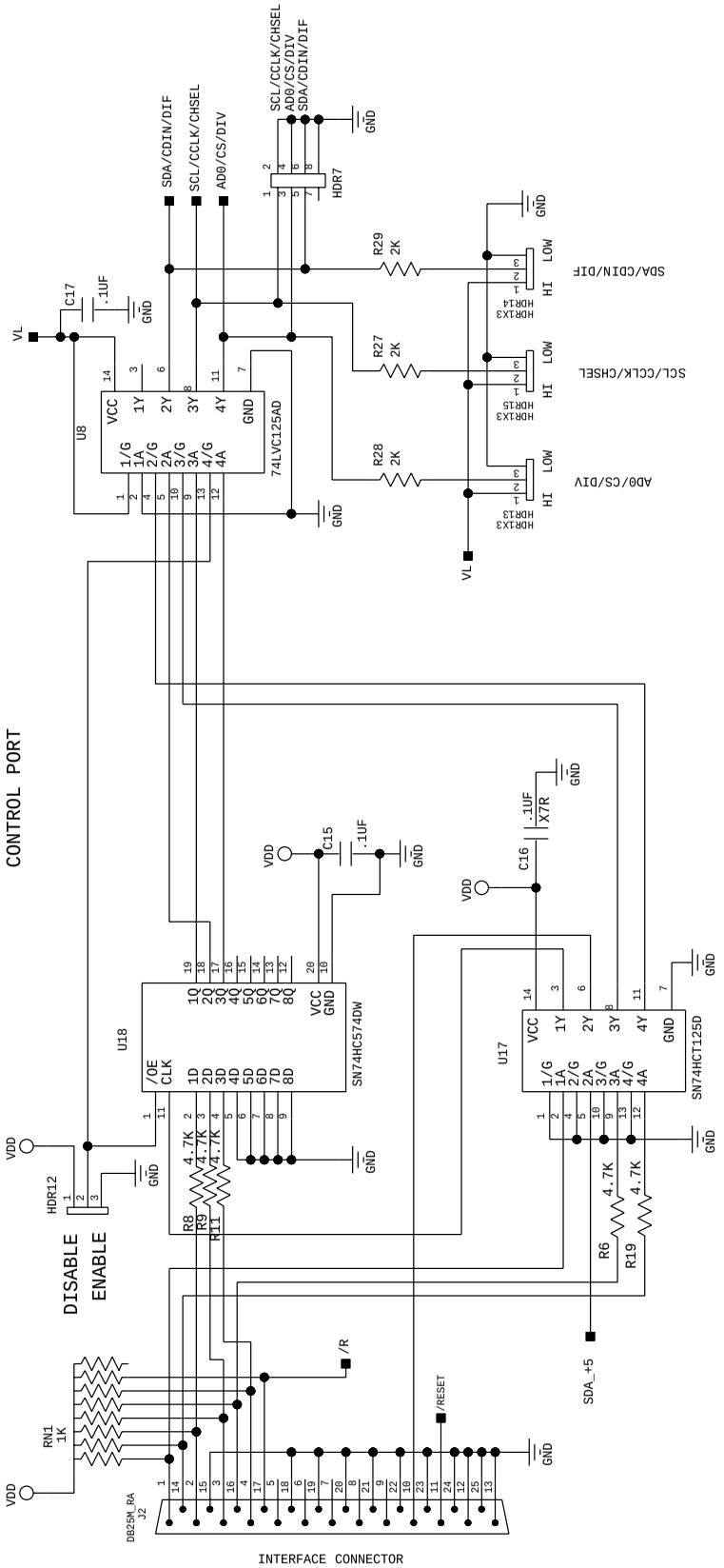


Figure 5. Control Port Interface

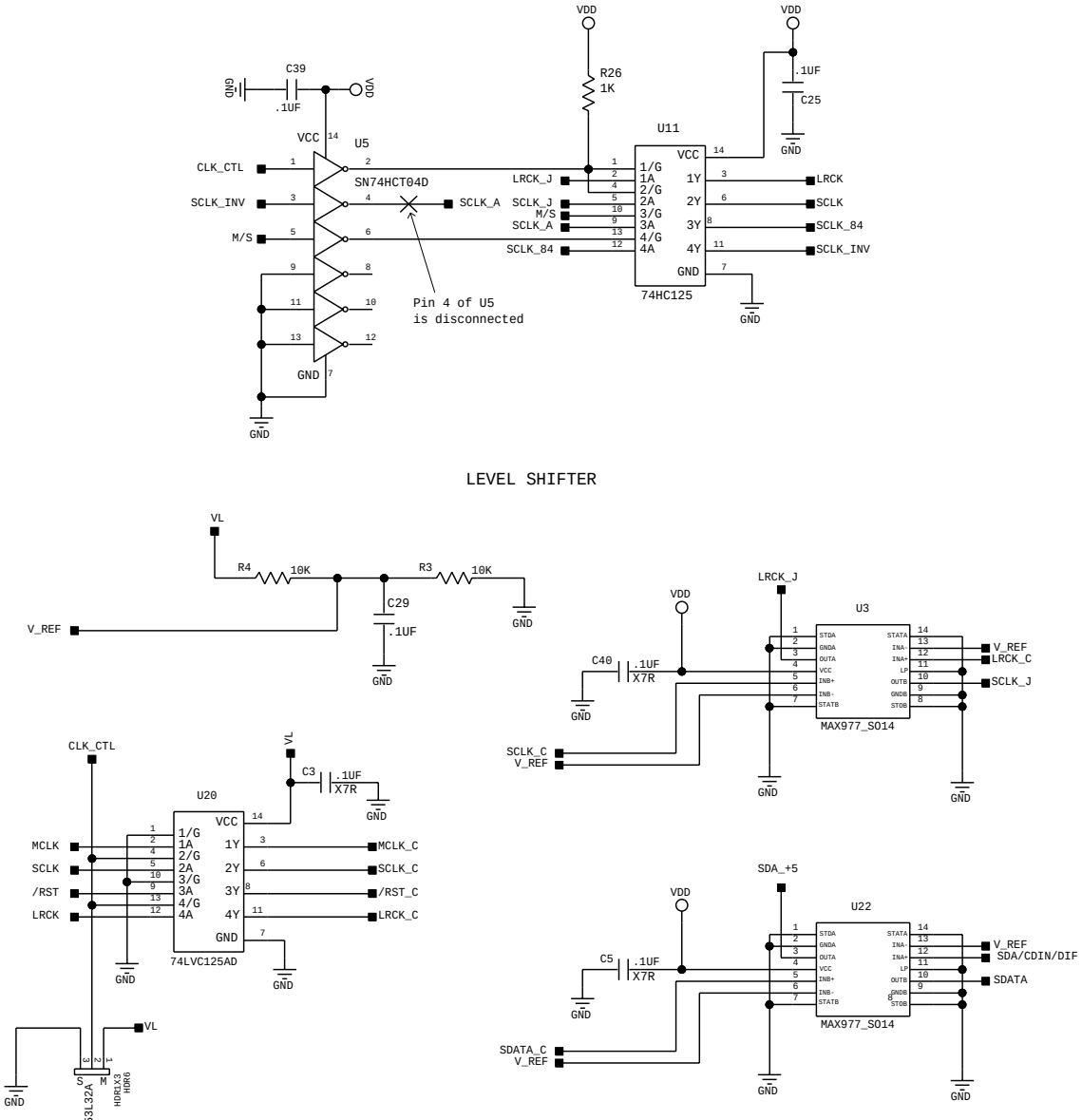


Figure 6. Level Shift

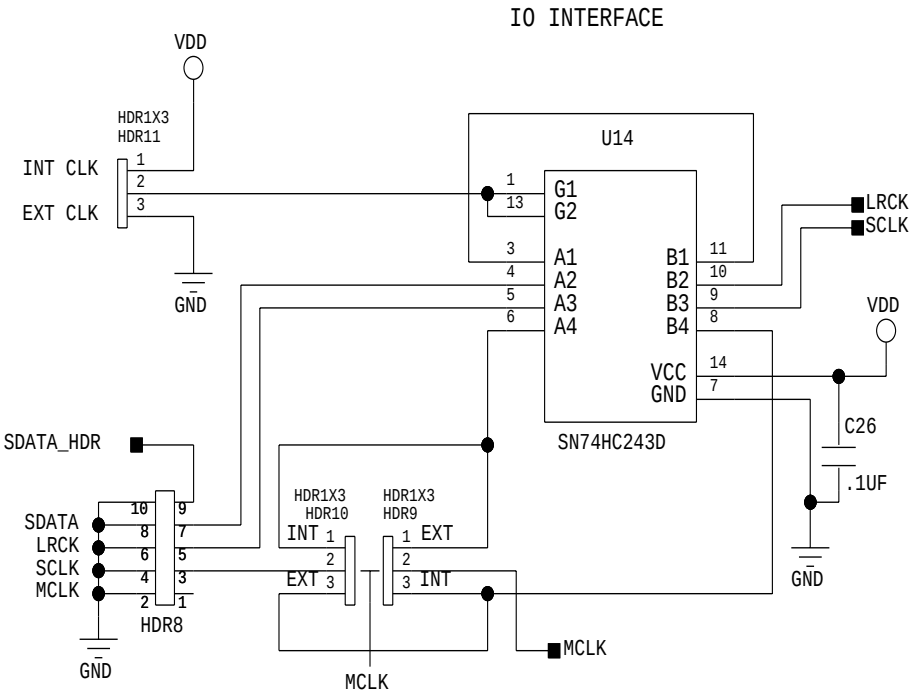


Figure 7. I/O for Clocks and Data

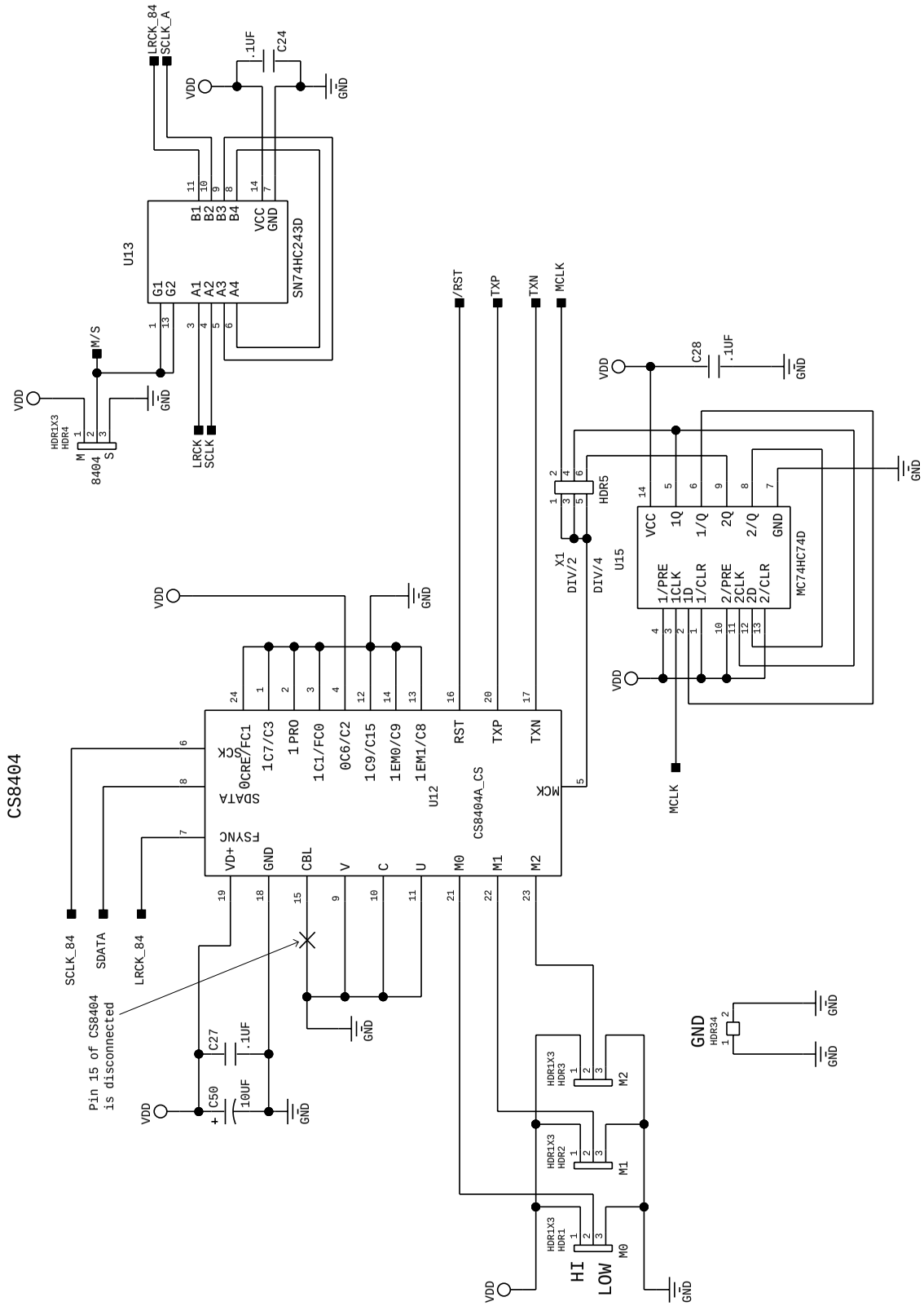


Figure 8. CS8404A Digital Audio Interface

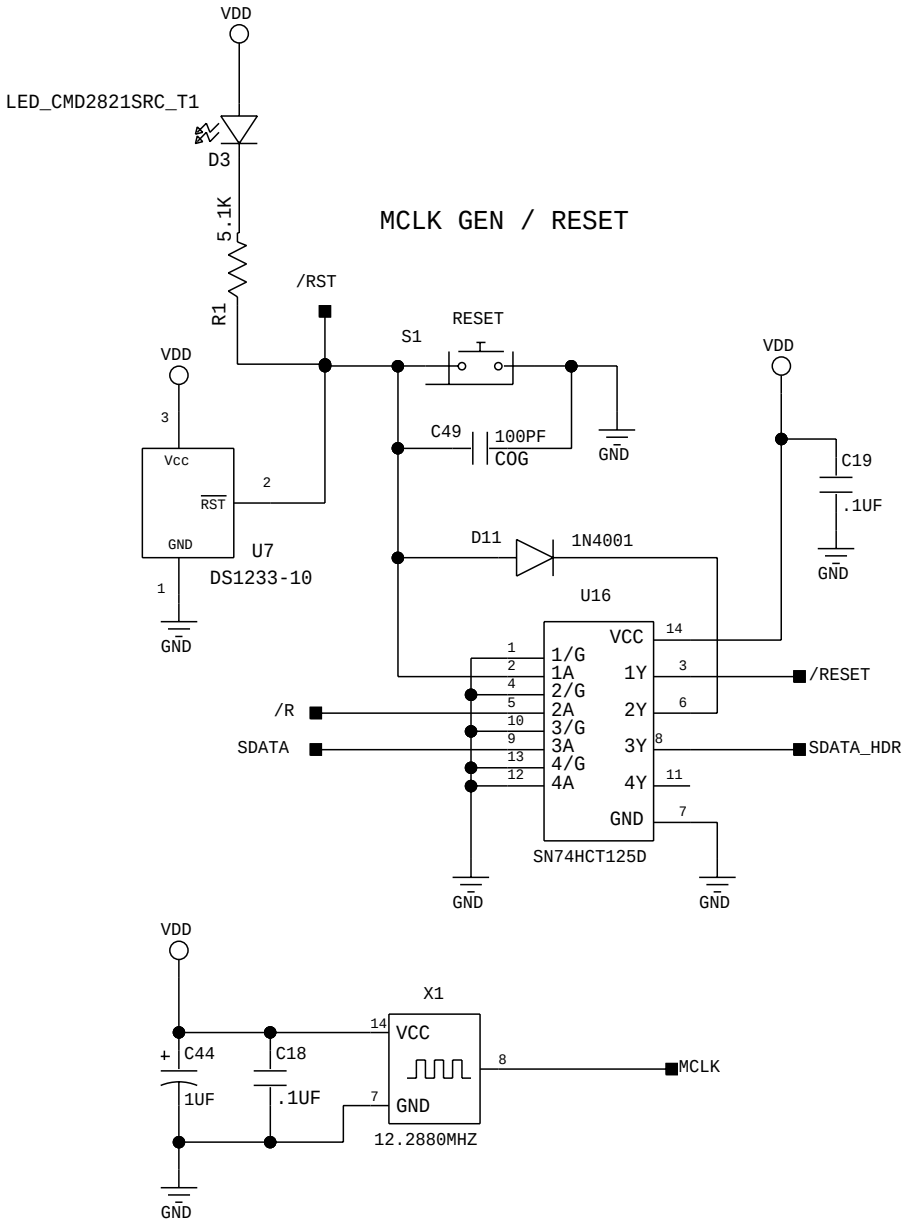


Figure 9. Reset Circuit and Clock Generation

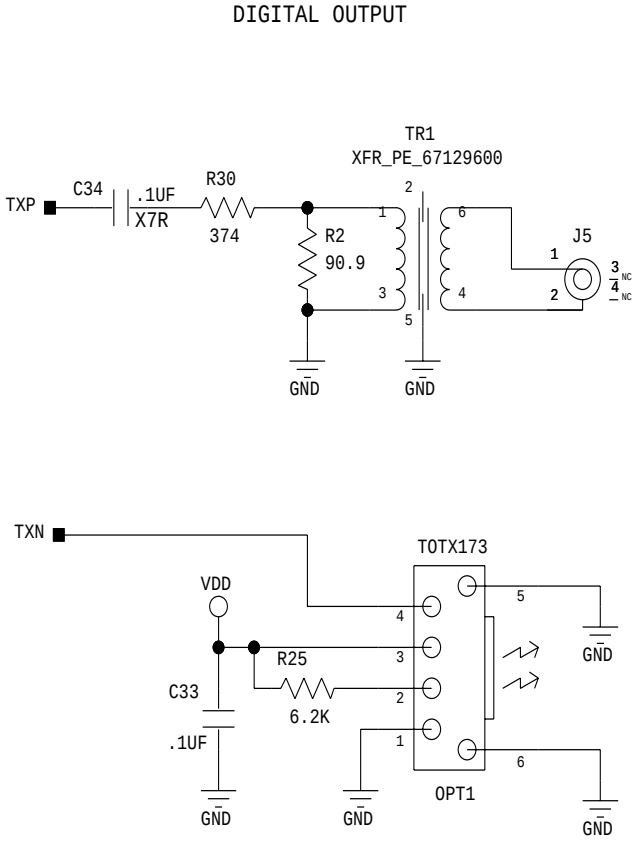


Figure 10. Digital Audio Outputs

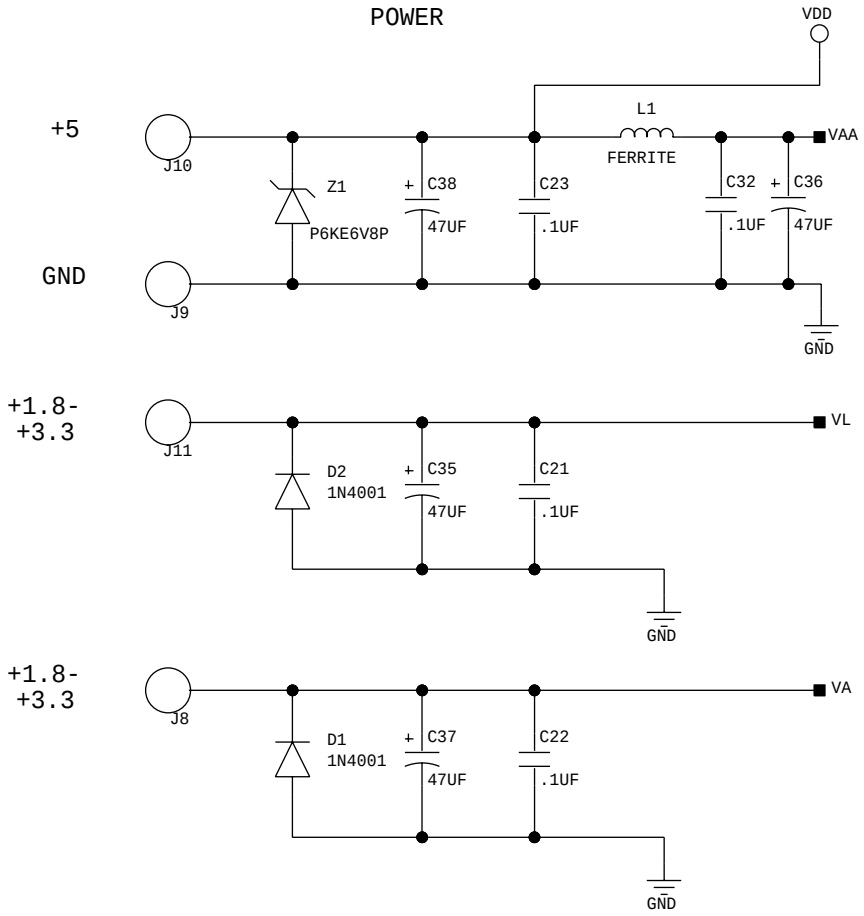


Figure 11. Power Supply

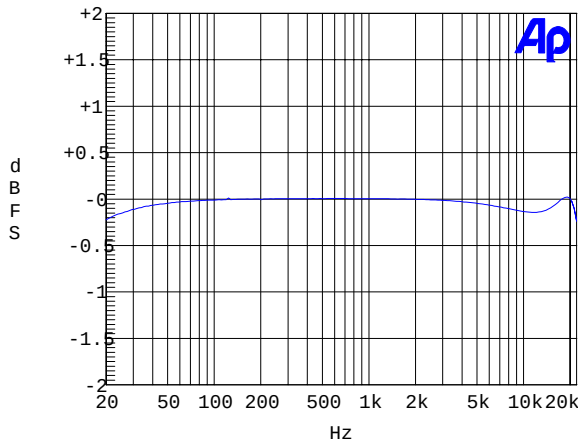


Figure 12. Frequency Response at 1.8 V

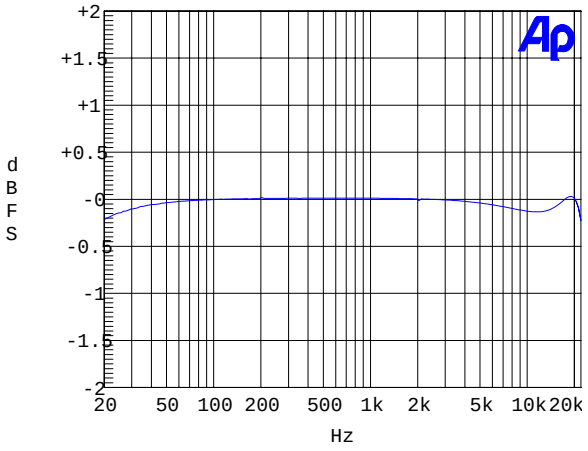


Figure 13. Frequency Response at 3.0 V

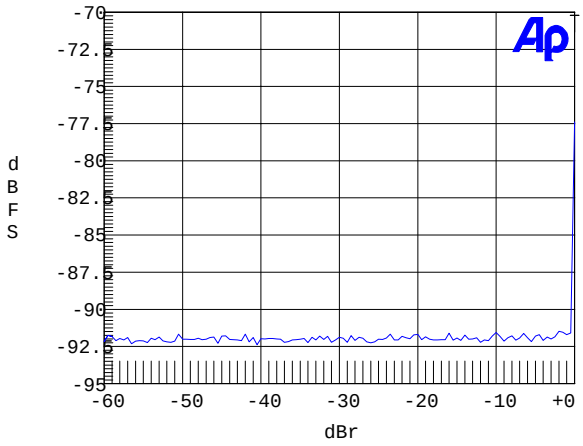


Figure 14. THD+N versus Amplitude at 1.8 V

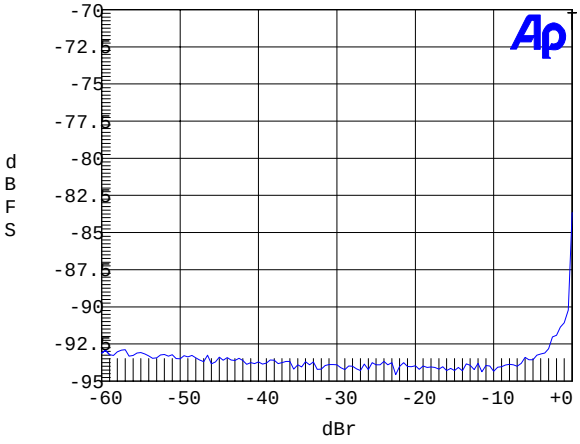


Figure 15. THD+N versus Amplitude at 3.0 V

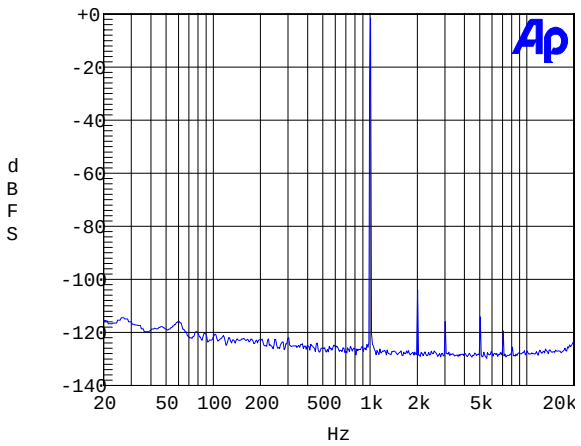


Figure 16. FFT of 1 kHz Sine Wave at -1 dBFS and 1.8 V

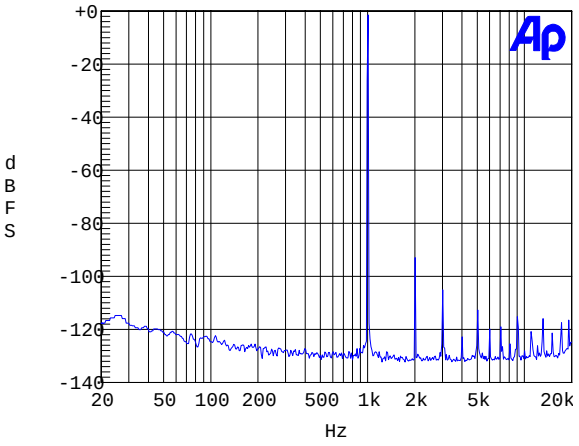


Figure 17. FFT of 1 kHz Sine Wave at -1 dBFS and 3.0 V

CS53L32 Customer Demonstration Board
CDB53L32A_A.0
CRYSTAL SEMICONDUCTOR

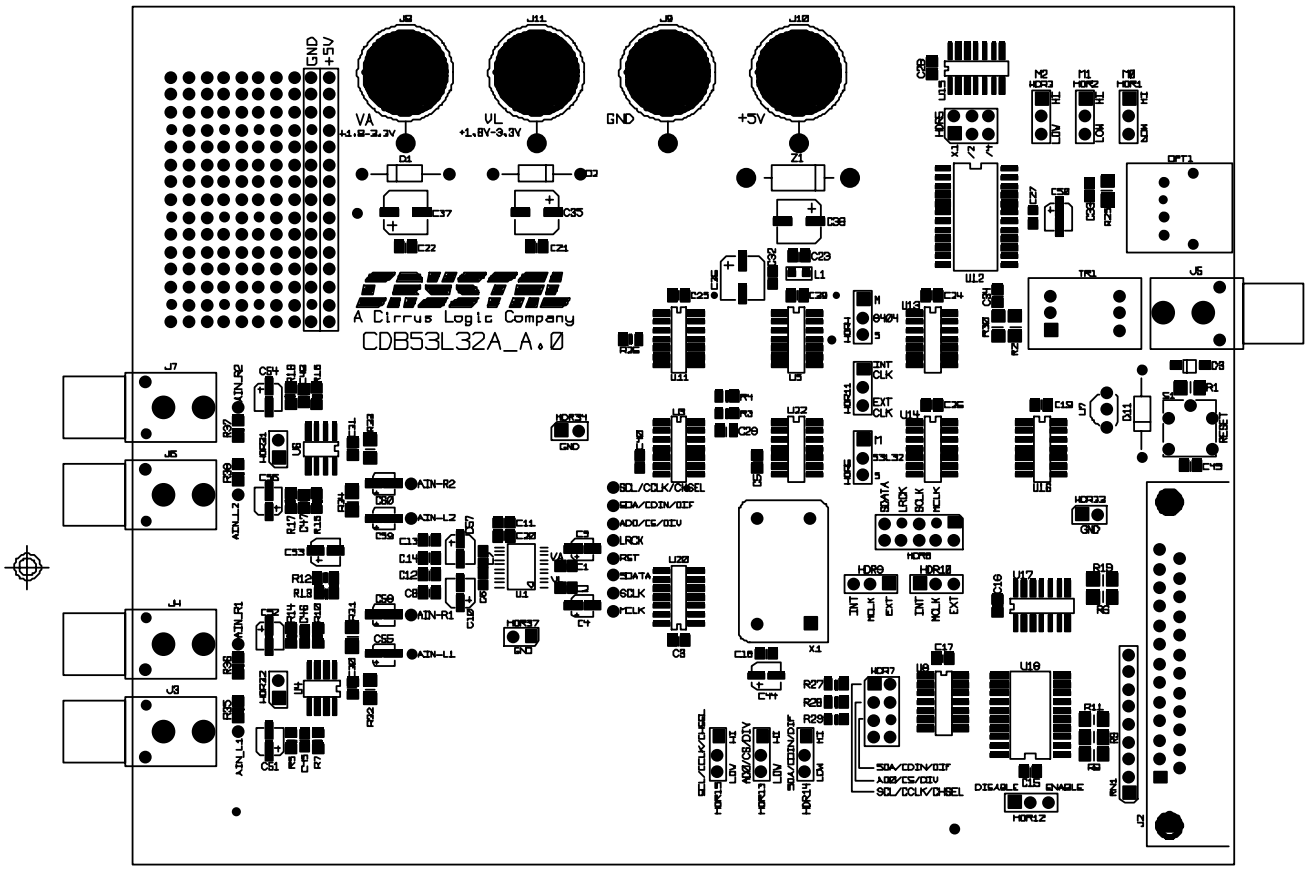


Figure 18. Silkscreen Top

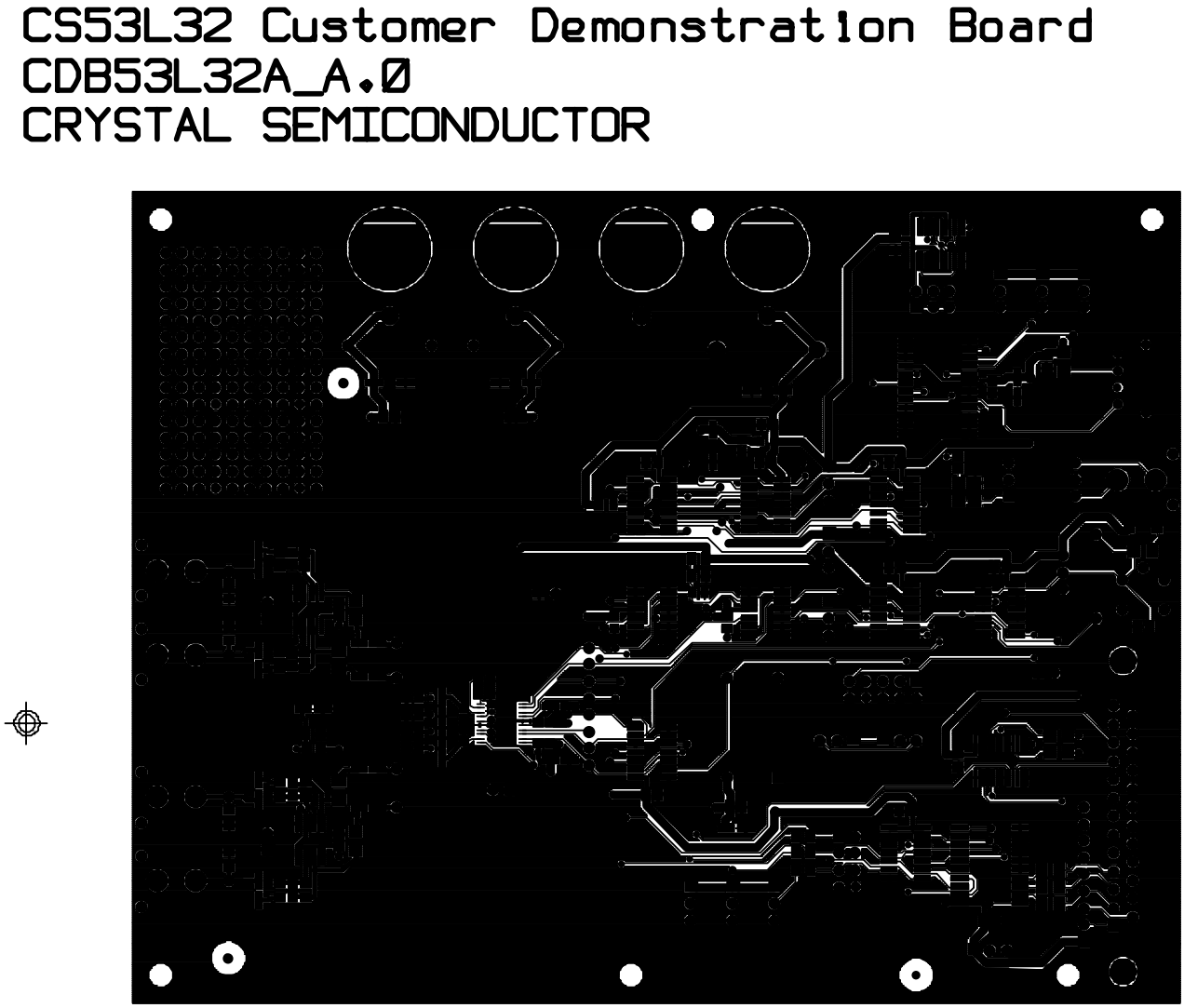


Figure 19. Top Side

CS53L32 Customer Demonstration Board
CDB53L32A_A.0
CRYSTAL SEMICONDUCTOR

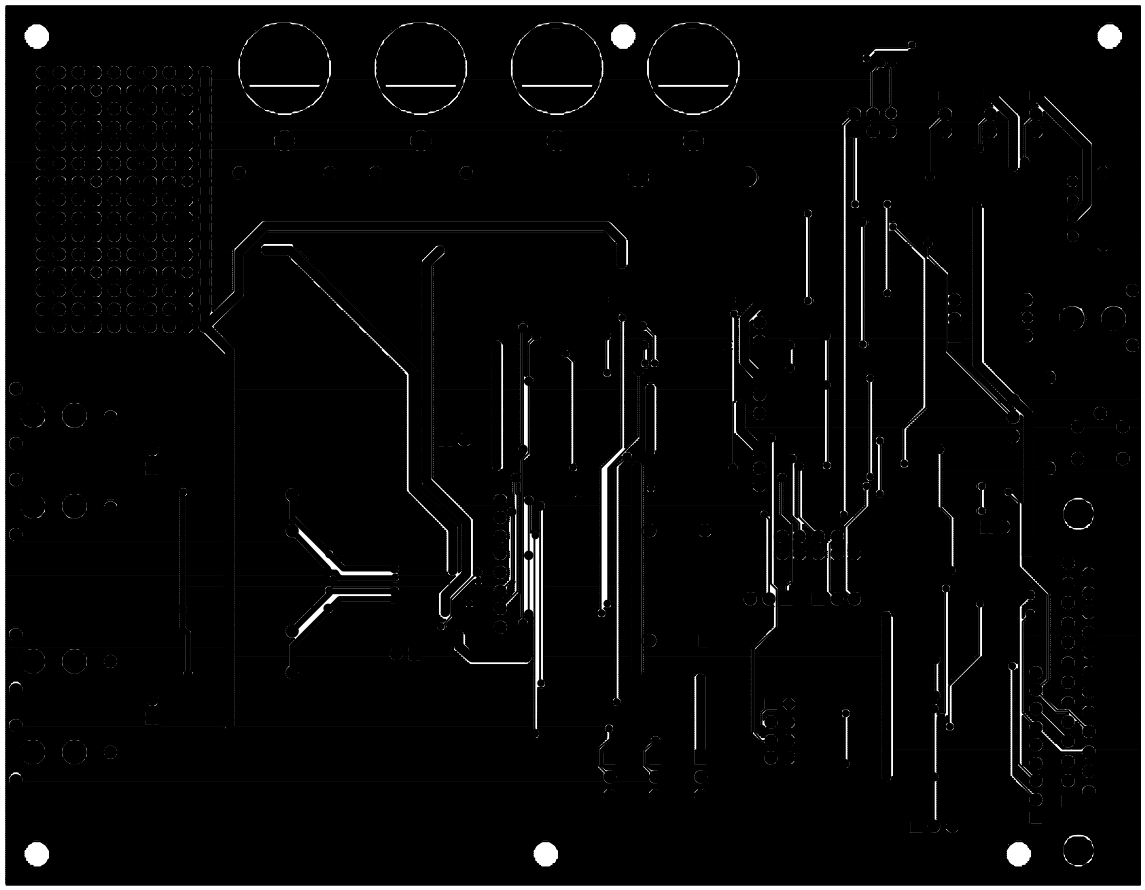


Figure 20. Bottom Side

• Notes •


SMART
Analog
™