AN180

# Application Note

# USING A PLL TO GENERATE CLOCKS FOR DIGITAL AUDIO

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## 1. INTRODUCTION

This application note describes how to use a low-cost PLL (Phase Lock Loop) circuit to generate sample frequencies required for high quality digital audio for use with MP3.

## 2. BACKGROUND

Cirrus Logic EPD-7209/12/7312 ARM®-based microcontrollers are capable of decoding MP3 digital audio in real time. The decoded bit stream is sent to a Crystal CS43L41 DAC using a high-speed Digital Audio Interface (DAI). The DAC requires an MCLK clock signal that is 256 times the desired sample rate. A typical sample rate for MP3 digital audio is 44.1 kHz, but other frequencies are used as well, including 8-, 16-, 22.05-, 24-, 32-, and 48 kHz. A PLL clocking scheme is capable of producing these clocks with little or no error.

Although it is possible to use the DSP capabilities of the ARM processor to do software sample rate conversion (SRC), a hardware approach is much simpler and reduces the number of MIPS (and thereby the power consumption) required of the processor. (Software SRC is supported by Cirrus Logic's MP3 player software.)

A brute-force (and potentially more expensive) method of providing multiple clocks is to switch between separate crystal oscillators. A better choice is to take advantage of PLL technology to synthesize the desired frequencies using one crystal source.

A PLL can be used to multiply a reference frequency by placing a divider circuit in the feedback loop from the VCO (voltage controlled oscillator) output to the phase comparator input as shown in Figure 1. If the divider circuit is programmable, then multiple frequency outputs are generated.

## 3. CIRCUIT DESCRIPTION

Refer to Figure 2 while reading this section.

The circuit is based upon the Integrated Circuit Systems ICS548-02, a low-cost, low-jitter, high-performance clock synthesizer designed to produce audio sampling rates for MP3 and other digital audio systems. Using analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 14.7456 MHz or 3.6864 MHz crystal input to produce 256x all of the popular audio sampling frequencies. With a separate 3.6864 MHz input, the chip provides a clock output, allowing it to drive the MCLK input on the CS43L41 directly.

Alternatively, the MOSCOUT oscillator drive output of the EP7209/12/7312 can provide the clock to the ICS548-02. This approach may be the preferred method to use since the EP7209/12/7312 manages the power consumption by going into a Standby mode when not in use. This mode effectively disables the 3.6864 MHz oscillator that reduces overall system power consumption. Using the external 14.7456 MHz oscillator, the PLL will generate MCLK for all sampling frequencies except 8 KHz.

The ISC548-02 uses 4 digital inputs to select the frequency (S0, S1, S2, and S3). The control inputs can be connected directly to four GPIO output pins of the EP72xx and adjusted under software control. Table 1 lists the frequencies generated by the ICS548-02 PLL circuit as a function of the four input select pins. Notice that S3 is always a one. This pin could be wired to $V_{dd}$ freeing up an extra 72xx/7312 GPIO pin.

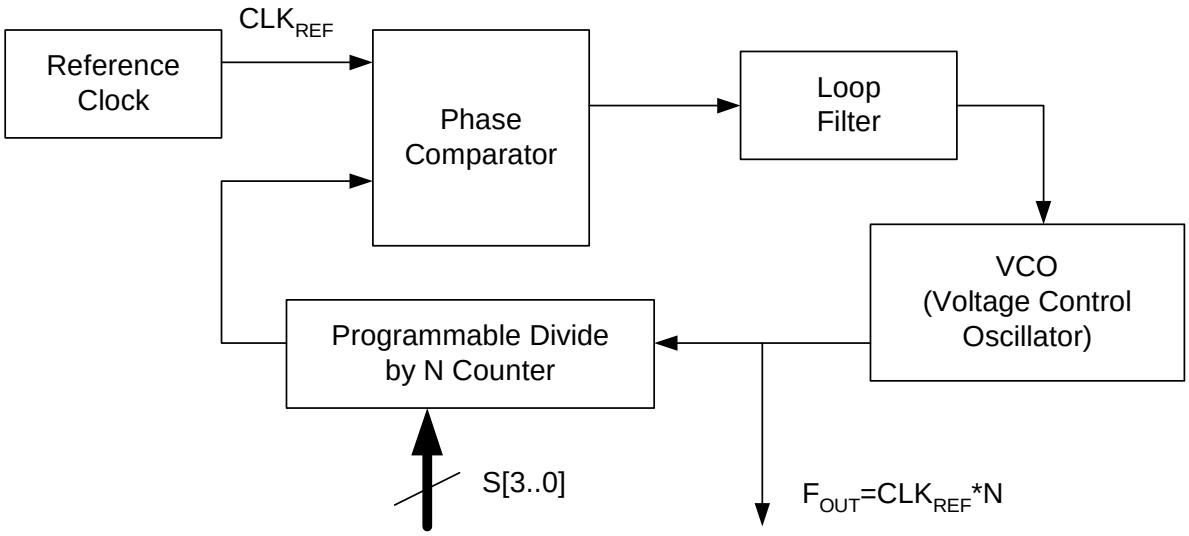


**Figure 1. Typical PLL Circuit**

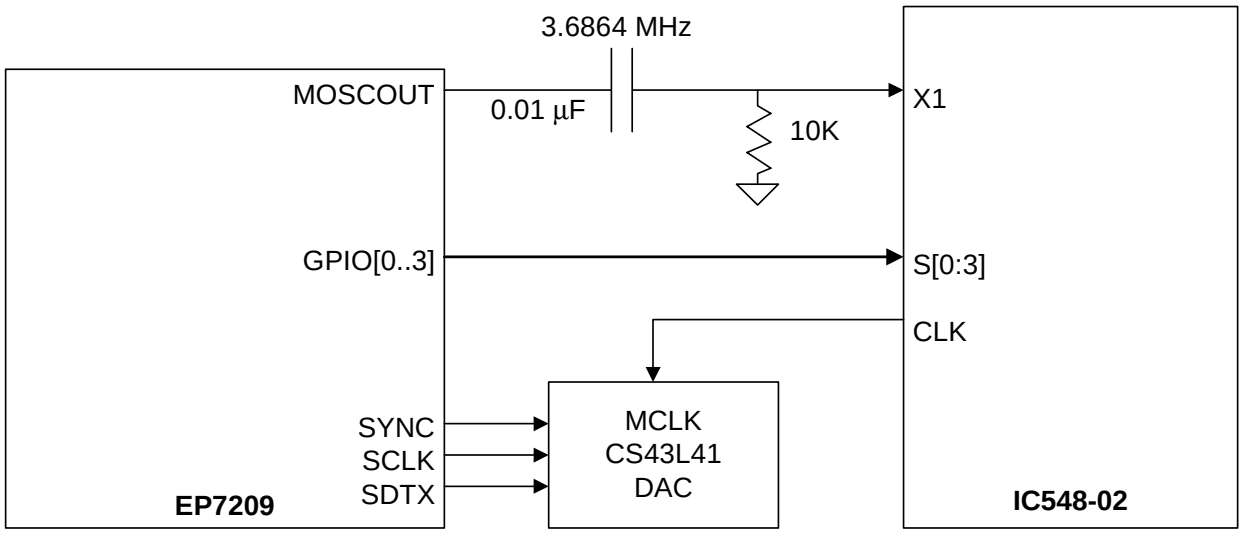


**Figure 2. EP7209/12/7312 ICS548-02 Interface**

| Desired Sampling Rate (Kilo-Hertz) | Output Clock 256 x SR (Mega-Hertz) | Frequency Select Pins | | | |
|---|---|---|---|---|---|
| | | S3 | S2 | S1 | S0 |
| 8 | 2.048 | 1 | 1 | 1 | 1 |
| 16 | 4.096 | 1 | 0 | 0 | 0 |
| 22.05 | 5.6448 | 1 | 0 | 0 | 1 |
| 24 | 6.144 | 1 | 0 | 1 | 0 |
| 32 | 8.192 | 1 | 1 | 0 | 0 |
| 44.1 | 11.2896 | 1 | 1 | 0 | 1 |
| 48 | 12.288 | 1 | 1 | 1 | 0 |

**Table 1. List of Audio Sample Rates and Corresponding Frequency Select Bits**

**NOTE:** Actual values are 256 times the desired sample rate. Reference clock for this table is 3.6864 MHz.


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