Maverick™ from CIRRUS LOGIC

EP7312

FEATURES

- **ARM720T processor**
  - — ARM7TDMI CPU
  - — 8 Kbytes of four-way set-associative cache
  - — MMU with 64-entry TLB (translation look-aside buffer)
  - — Write Buffer
  - — Thumb code support enabled
- **Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz at 2.5 V**
- **MaverickKey™ IDs**
  - — 32-bit unique SDMI ID
  - — 128-bit random ID
- **Ultra low power**
  - — Designed for applications that require long battery life while using standard AA/AAA batteries or rechargeable cells
  - — Typical power numbers
    - 90 mW at 74 MHz in the Operating State
    - 30 mW at 18 MHz in the Operating State
    - 10 mW in the Idle State (clock to the CPU stopped, everything else running)
    - <1 mW in the Standby State (real-time clock "on," everything else stopped)

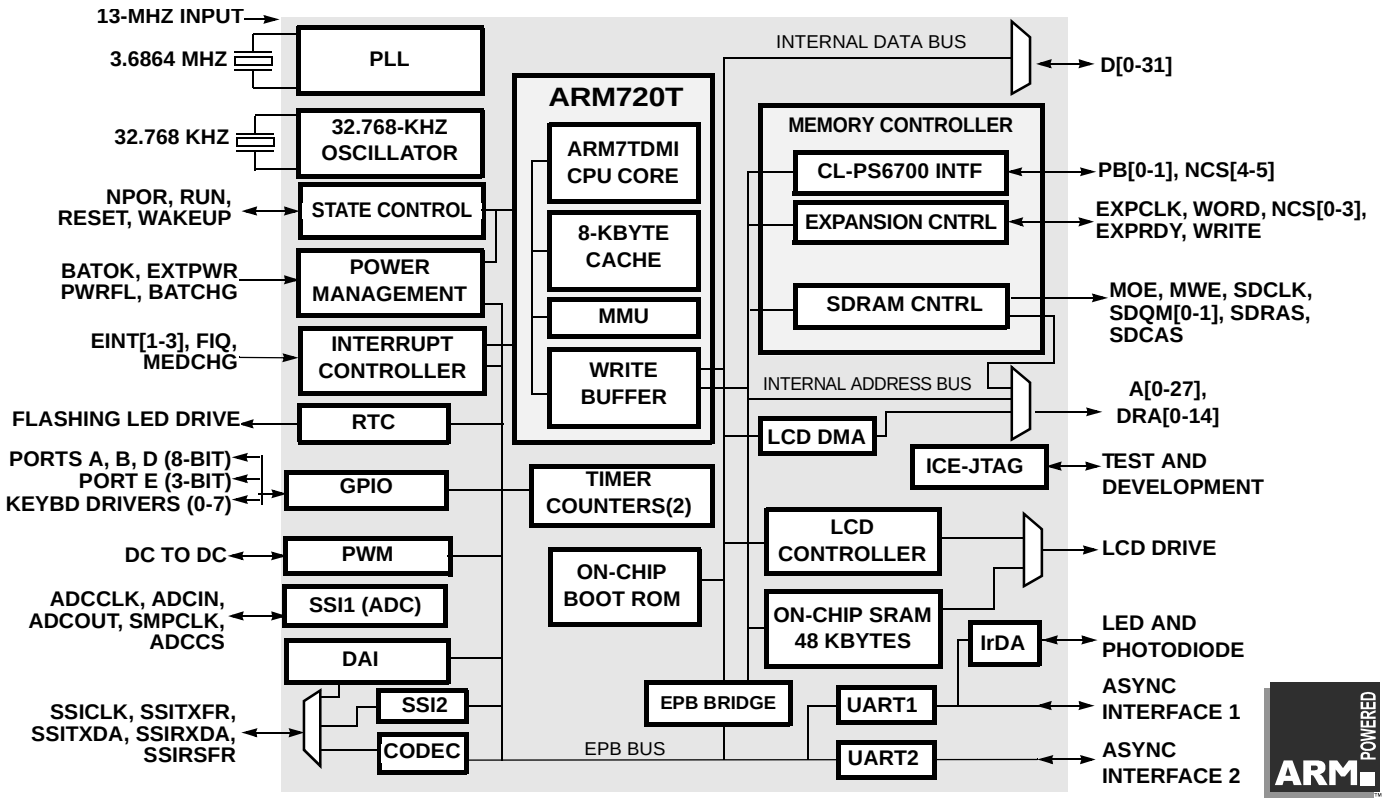
High-Performance, Low-Power System on Chip with SDRAM and Improved Digital Audio Interface

OVERVIEW

The Maverick™ EP7312 is designed for ultra-low-power applications such as PDAs, two-way pagers, smart cellular phones or any hand-held device that features the added capability of digital audio decompression. The core-logic functionality of the device is built around an ARM720T processor with 8 Kbytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for support of sophisticated operating systems like Microsoft® Windows CE.

The EP7312 also includes a 32-bit real-time clock and comparator. *(Continued on Page 3)*

BLOCK DIAGRAM



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FEATURES (cont.)

- **Advanced audio decoder / decompression capability**
  - — Allows for support of multiple audio decompression algorithms
  - — Supports MPEG 1, 2, and 2.5 layer 3 audio decoding, including ISO compliant MPEG 1 and 2 layer 3 support for all standard sample rates and bit rates
  - — Supports bit streams with adaptive bit rates
  - — Improved DAI (Digital Audio Interface) providing glue-less interface to low-power DACs, ADCs, and CODECs
- **SDRAM controller**
  - — Supports four internal memory banks totaling 256 Mbits in size
  - — SDRAM memory interface is programmable from 4 to 32 bits wide.
- **LCD controller**
  - — Interfaces directly to a single-scan panel monochrome or color STN LCD
  - — Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
  - — Video frame buffer size programmable up to 128 kbytes
  - — Bits per pixel of 1, 2, or 4 bits
- **Memory controller**
  - — Decodes up to 6 separate memory segments of up to 256 Mbytes each
  - — Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
  - — Programmable access time for conventional ROM / SRAM / FLASH memory
  - — Supports Removable FLASH card interface
  - — Enables connection to removable FLASH card for addition of expansion FLASH memory modules
- **48 kbytes (0x9600) of on-chip SRAM for fast program execution and / or as a frame buffer**
- **Synchronous serial interface**
  - — ADC (SSI) Interface: Master mode only; SPI® and Microwire1®-compatible (128 kbits/s operation)
- **On-chip ROM; for manufacturing support**
- **27-bits of general-purpose I/O**
  - — Three 8-bit and one 3-bit GPIO port
  - — Supports scanning keyboard matrix
- **Two UARTs (16550 type)**
  - — Supports bit rates up to 115.2 kbits/s
  - — Contains two 16-byte FIFOs for TX and RX
  - — UART1 supports modem control signals
- **SIR (up to 115.2 kbits/s infrared encoder / decoder**
  - — IrDA (Infrared Data Association) SIR protocol encoder / decoder
- **DC-to-DC converter interface (PWM)**
  - — Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a DC to DC converter
- **Two timer counters**
- **Available in 208-pin LQFP or 256-ball PBGA packages**
- **Evaluation kit available with BOM, schematics, sample code, and design database**
- **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**
- **Dedicated LED flasher pin from the RTC**
- **Full JTAG boundary scan and Embedded ICE® support**
- **Commercial and industrial operating temperature range versions**
- **The EP7312 is optimized for low power dissipation and is fabricated on a fully static 0.25 micron CMOS process.**

Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/sales.cfm

OVERVIEW (cont.)

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.

Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.

Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM / SRAM / FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with eight chip selects decoding six 256 Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb® instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

The second is the programmable 4- or 32-bit-wide SDRAM interface that allows direct connection of up to four internal banks of SDRAM, totaling 256 Mbits. To assure the lowest possible power consumption, the EP7312 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State.

A DMA address generator is also provided that fetches video display data for the LCD controller from main SDRAM memory. The display frame buffer start address is programmable. In addition, the built-in LCD controller can utilize external or internal SRAM for memory, thus eliminating the need for SDRAMs.

Digital Audio Capability

The EP7312 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7312.

Serial Interfaces

The EP7312 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbits/s. An IrDA SIR protocol encoder / decoder can be optionally switched into the RX / TX signals to / from one of the UARTs to enable these signals to drive an infrared communication interface directly.

Improved Digital Audio Interface (DAI)

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal® CS43L41 / 42 / 43 low-power audio DACs and the Crystal® CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

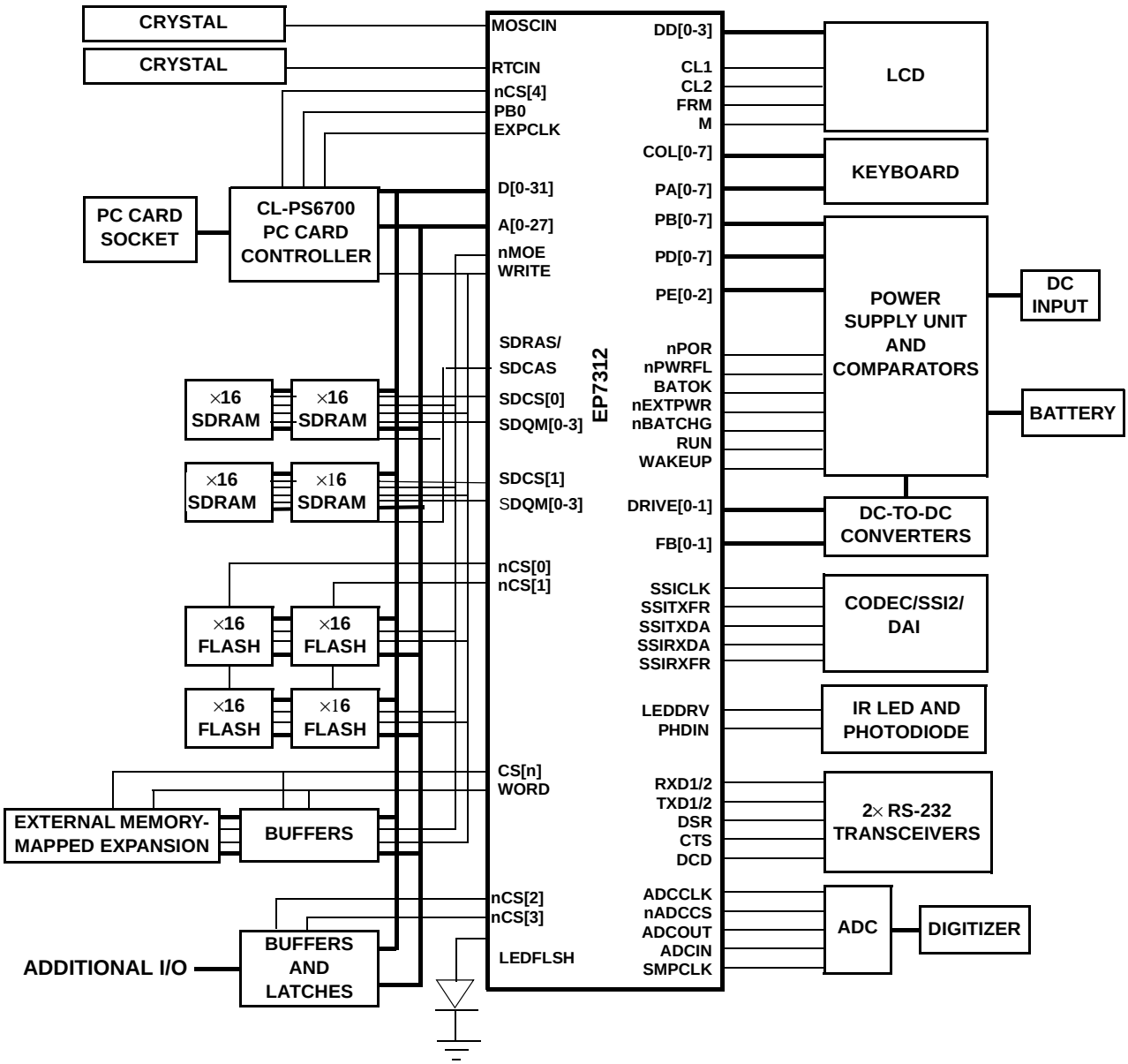
Packaging

The EP7312 is available in a 208-pin LQFP package and a 256-ball PBGA package.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

OVERVIEW *(cont.)*



NOTE: A system can only use one of the following peripheral interfaces at any given time: SSI2, CODEC, or DAI.

Figure 1. A Maximum EP7312 Based System

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LIST OF TABLES

1. CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

1.1. Acronyms and Abbreviations

Table 1 lists abbreviations and acronyms used in this data sheet.

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CMOS	complementary metal oxide semi-conductor
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request

Table 1. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PIA	peripheral interface adapter
PLL	phase locked loop
PSU	power supply unit
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Table 1. Acronyms and Abbreviations *(cont.)*

1.2. Units of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbits/s	kilobits per second
kbyte	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbits/s	megabits (1,048,576 bits) per second
Mbyte	megabyte (1,048,576 bytes)
Mbyte/s	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

Table 2. Unit of Measurement

1.3. General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase “h” appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, ‘11’ designates a binary number). Numbers not indicated by an “h”, 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a hyphen (-) (for example, CODR[0-7]), and are described in the *EP7312 User’s Manual*, The use of “tbd” indicates values that are “to be determined,” “n/a” designates “not available,” and “n/c” indicates a pin that is a “no connect.”

1.4. Pin Description Conventions

Abbreviations used for signal directions are listed in Table 3.

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output

Table 3. Pin Description Conventions

2. ELECTRICAL SPECIFICATIONS

2.1. Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Table 4. Absolute Maximum Ratings

2.2. Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3V - 3.6V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

Table 5. Recommended Operating Conditions

2.3. DC Characteristics

All characteristics are specified at V_{DD} = 2.5 volts and V_{SS} = 0 volts over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures relate to typical conditions at 2.5 V, 18.432 MHz operation with the PLL switched “on.”

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	1.7		V_{DD} + 0.3	V	V_{DD} = 2.5 V
VIL	CMOS input low voltage	-0.3		0.8	V	V_{DD} = 2.5 V
VT+	Schmitt trigger positive going threshold	1.6 (Typ)		2.0	V	
VT-	Schmitt trigger negative going threshold	0.8		1.2 (Typ)	V	
Vhst	Schmitt trigger hysteresis	0.1		0.4	V	VIL to VIH
VOH	CMOS output high voltage Output drive 1 Output drive 2	V_{DD} – 0.2 2.5 2.5			V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage Output drive 1 Output drive 2			0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current[1]			1.0	µA	VIN = V_{DD} or GND
IOZ	Output three-state leakage current[2] [3]	25		100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8		10.0	pF	

Table 6. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8		10.0	pF	
CI/O	Transceiver capacitance	8		10.0	pF	
$IDD_{startup}$	Startup current consumption			15.0	µA	Initial 100 ms from power up, Cache disabled, 32 kHz oscillator not stable, POR signal at VIL, all other I/O static, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{standby}$	Standby current consumption Core, Osc, RTC @2.5V I/O @ 2.5V Core, Osc, RTC @2.5V I/O @ 3.3V		De-Rating Curves to be added	De-Rating Curves to be added	µA	Just 32 kHz oscillator running, Cache disabled, all other I/O static, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle}	Idle current consumption **At 13 MHz** Core, Osc, RTC @2.5V I/O @ 2.5V Core, Osc, RTC @2.5V I/O @ 3.3V **At 18 MHz** Core, Osc, RTC @2.5V I/O @ 2.5V Core, Osc, RTC @2.5V I/O @ 3.3V **At 36 MHz** Core, Osc, RTC @2.5V I/O @ 2.5V Core, Osc, RTC @2.5V I/O @ 3.3		 TBD TBD TBD TBD TBD TBD TBD TBD TBD TBD TBD TBD	 4.2 6.0 12.0	mA	Both oscillators running, CPU static, Cache disabled, LCD refresh active, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V

Table 6. DC Characteristics *(cont.)*

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$IDD_{operatin}$	Operating current consumption				mA	All system active, running typical program, cache disabled, and LCD inactive
	At 13 MHz			14		
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 2.5V		TBD			
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 3.3V		TBD			
	At 18 MHz			30		
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 2.5V		TBD			
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 3.3V		TBD			
	At 36 MHz			40		
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 2.5V		TBD			
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 3.3V		TBD			
	At 49 MHz			50		
			TBD			
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 2.5V					
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 3.3V		TBD			
	At 74 MHz			68		
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 2.5V		TBD			
	Core, Osc, RTC @2.5V		TBD			
	I/O @ 3.3V		TBD			

Table 6. DC Characteristics *(cont.)*

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{DDstandby}$	Standby supply voltage	TBD			V	Minimum standby voltage for state retention and RTC operation only

Table 6. DC Characteristics *(cont.)*

1 The leakage value given assumes that the pin is configured as an input pin but is not currently being driven. An input pin not driven will have a maximum leakage of 1 µA. When the pin is driven, there will be no leakage.

2 Assumes buffer has no pull-up or pull-down resistors.

3 The leakage value given assumes that the pin is configured as an output pin but is not currently being driven. An output pin not driven will have leakage between 25 µA and 100 µA. When the pin is driven, there will be no leakage. Note that this applies to all output pins and all I/O pins configured as outputs.

Notes:
1) All power dissipation values can be derived from taking the particular IDD current and multiplying by 2.5 V.
2) The RTC of the EP7312 should be brought up at room temperature. This is required because the RTC OSC will NOT function properly if it is brought up at –40°C. Once operational, it will continue to operate down to –20°C extended and 0°C commercial.
3) A typical design will provide 3.3 V to the I/O supply (i.e., $V_{DD}IO$), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V DRAMs).
4) Pull-up current = 50 µA typical at V_{DD} = 3.3 volts.

2.4. AC Characteristics

All characteristics are specified at V_{DD} = 2.3 to 2.7 volts and V_{SS} = 0 volts over an operating temperature of 0°C to +70°C. Those characteristics marked with a # will be significantly different for 13 MHz mode because the EXPCLK is provided as an input rather than generated internally. These timings are estimated at present. The timing values are referenced to 1/2 V_{DD}.

Symbol	Parameter	13 MHz		18/36 MHz		Units
		Min	Max	Min	Max	
t1	Falling CS to data bus Hi-Z	0	35	0	25	ns
t2	Address change to valid write data	0	45	0	35	ns
t3	DATA in to falling EXPCLK setup time	0 #	—	18	—	ns
t4	DATA in to falling EXPCLK hold time	10 #	—	0	—	ns
t5	EXPRDY to falling EXPCLK setup time	0 #	—	18	—	ns
t6	Falling EXPCLK to EXPRDY hold time	10 #	50	0	50	ns
t7	Rising nMWE to data invalid hold time	10	—	5	—	ns
t8	Sequential data valid to falling nMWE setup time	–10	10	–10	10	ns
t9	Row address to falling nSDRAS setup time	TBD	-	TBD	-	ns
t10	Falling nSDRAS to row address hold time	TBD	-	TBD	-	ns
t11	Column address to falling nSDCAS setup time	TBD	-	TBD	-	ns
t12	Falling nSDCAS to column address hold time	TBD	-	TBD	-	ns
t13	Write data valid to falling nSDCAS setup time	TBD	-	TBD	-	ns
t14	Write data valid from falling nSDCAS hold time	TBD	-	TBD	-	ns
t15	LCD CL2 low time	80	3,475	80	3,475	ns
t16	LCD CL2 high time	80	3,475	80	3,475	ns
t17	LCD falling CL[2] to rising CL[1] delay	0	25	0	25	ns
t18	LCD falling CL[1] to rising CL[2]	80	3,475	80	3,475	ns
t19	LCD CL[1] high time	80	3,475	80	3,475	ns
t20	LCD falling CL[1] to falling CL[2]	200	6,950	200	6,950	ns
t21	LCD falling CL[1] to FRM toggle	300	10,425	300	10,425	ns
t22	LCD falling CL[1] to M toggle	–10	20	–10	20	ns
t23	LCD rising CL[2] to display data change	–10	20	–10	20	ns
t24	Falling EXPCLK to address valid	—	33 #	—	5	ns

Table 7. AC Timing Characteristics

Symbol	Parameter	13 MHz		18/36 MHz		Units
		Min	Max	Min	Max	
t25	Data valid to falling nMWE for non sequential access only	5	—	5	—	ns
t31	SSICLK period (slave mode)	0	512	0	512	kHz
t32	SSICLK high	925	1025	925	1025	ns
t33	SSICLK low	925	1025	925	1025	ns
t34	SSICLK rise / fall time		7		7	ns
t35	SSICLK rising to RX and / or TX frame sync		528		528	ns
t36	SSICLK rising edge to frame sync low		448		448	ns
t37	SSICLK rising edge to TX data valid		80		80	ns
t38	SSIRXDA data set-up time	30		30		ns
t39	SSIRXDA data hold time	40		40		ns
t40	SSITXFR and / or SSIRXFR period	750		750		ns
t_{nCSRD}	Negative strobe (nCS[0-5]) zero wait state read access time	TBD		TBD		TBD
t_{nCSWR}	Negative strobe (nCS[0-5]) zero wait state write access time	TBD		TBD		TBD
t_{EXBST}	Sequential expansion burst mode read access time	TBD		TBD		TBD
t_{RC}	SDRAM cycle time	TBD	-	TBD	-	TBD
t_{RAC}	Access time from SDRAS	TBD	-	TBD	-	TBD
t_{RP}	SDRAS precharge time	TBD	-	TBD	-	TBD
t_{CAS}	SDCAS pulse width	TBD	-	TBD	-	TBD
t_{CP}	SDCAS precharge in page mode	TBD	-	TBD	-	TBD
t_{PC}	Page mode cycle time	TBD	-	TBD	-	TBD
t_{CSR}	SDCAS set-up time for auto refresh	TBD	-	TBD	-	TBD
t_{RAS}	SDRAS pulse width	TBD	-	TBD	-	TBD

Table 7. AC Timing Characteristics *(cont.)*

Notes: All SDRAM 36 MHz timings are for SDRAM operation. The values for 36 MHz include 1 wait state, and the 18 MHz values have 0 wait states.

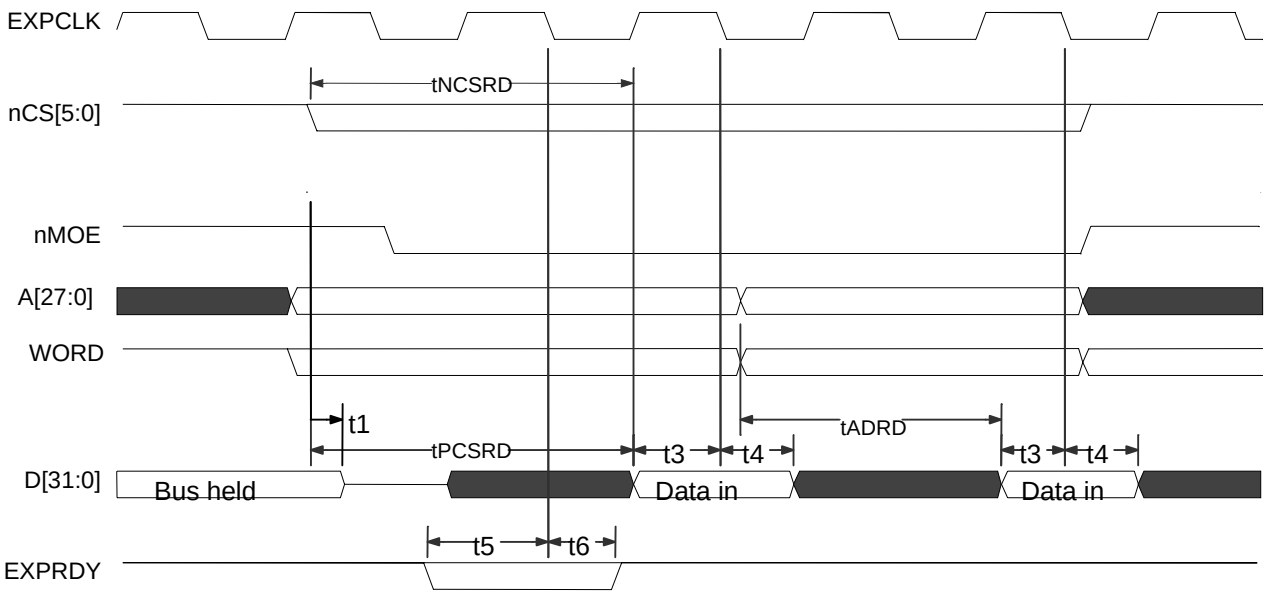

Figure 2. Consecutive Memory Read Cycles with Minimum Wait States

Notes:

1) tnCSRD = 50 ns at 36.864 MHz
   70 ns at 18.432 MHz
   120 ns at 13.0 MHz

   Maximum values for minimum wait states. This time can be extended by integer multiples of the clock period (27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2) Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.

3) tnCSRD = tADRD = tPCSRD

4) When the EP7312 device implements consecutive reads(e.g., use of the LDM instruction), regardless of the state of the SQAEN bit, the signals nMOE and nCSx will always remain low through the entire multi-read access. They will not toggle in-between each different address access. In order to have these signals toggle, single access read instructions (e.g., LDR) must be used.

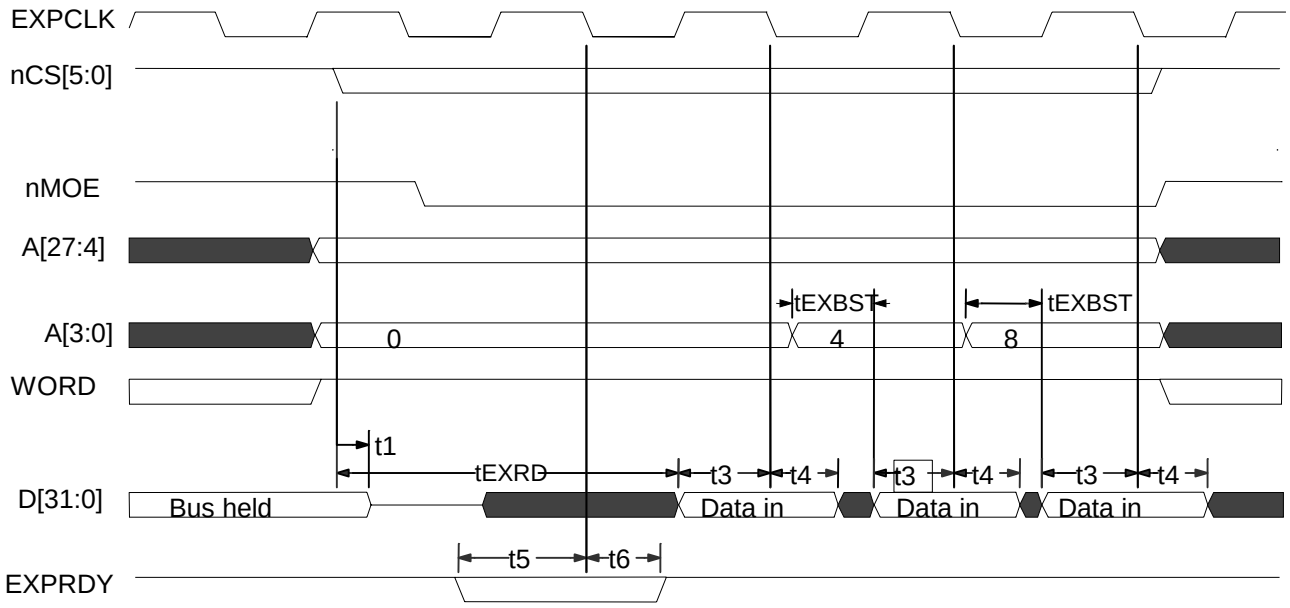

Figure 3. Sequential Page Mode Read Cycles with Minimum Wait States

Notes: 1) tEXBST = 35 ns at 36.864 MHz
35 ns at 18.432 MHz
55 ns at 13.0 MHz
(Value for 36.864 MHz assumes 1 wait state.)

Maximum values for minimum wait states. This time can be extended by integer multiples of the clock period (27 nsec at 36 MHz, 54 nsec at 18.432 MHz and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

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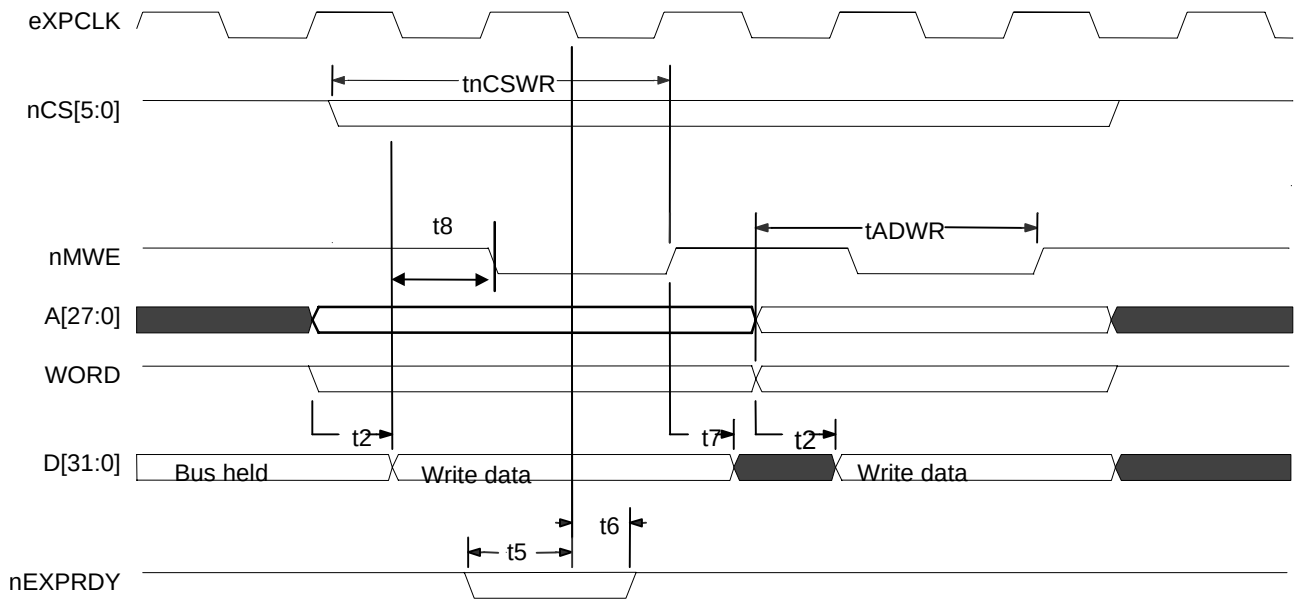


Figure 4. Consecutive Memory Write Cycles with Minimum Wait States

Notes: 1) tnCSWR = 35 nsec at 36.864 MHz
70 ns at 18.432 MHz
120 ns at 13.0 MHz

Maximum values for minimum wait states. This time can be extended by integer multiples of the clock period (27 nsec at 36 MHz, 54 nsec at 18.432 MHz, and 77 nsec at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2) Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.

3) Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

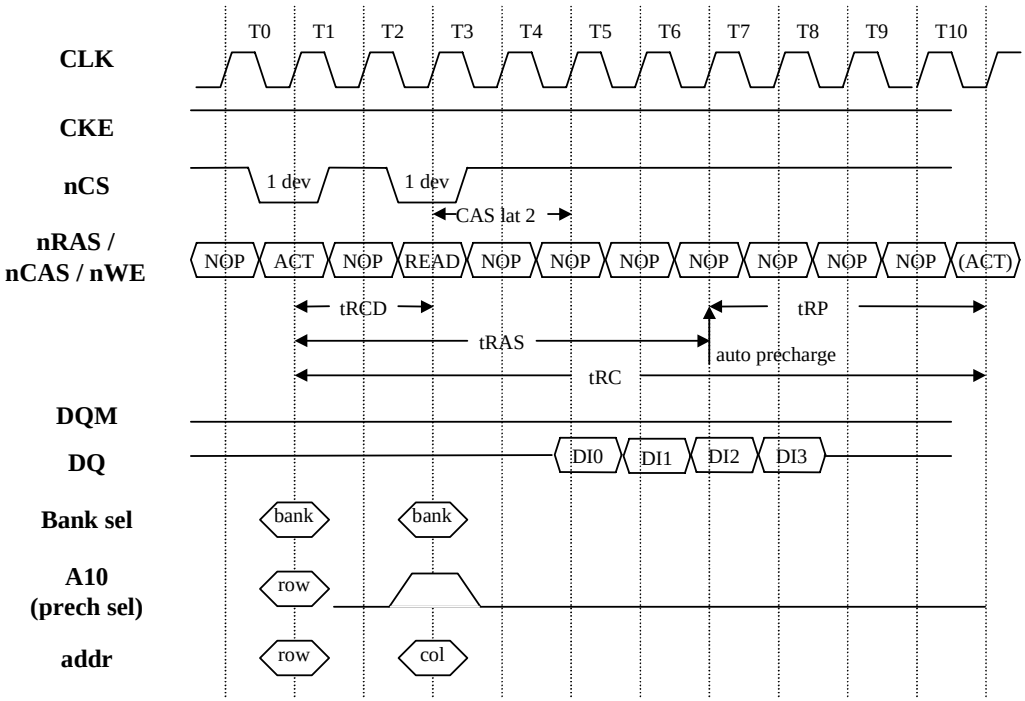


Figure 5. SDRAM Read Cycles SDCAS Latency = 2

Notes:
1. tRCD (delay time ACT to READ/WRITE command) = 30 ns or 2 cycles at 36 MHz.
2. tRP (PRE to ACT command period) = 30 ns or 2 cycles at 36 MHz.
3. tRAS (ACT to PRE command period) = 60 ns or 3 cycles at 36 MHz.
4. tRC (ACT to REF/ACT command period [operation]) = 90 ns or 4 cycles at 36 MHz.
5. For SDCAS latency 3, there will be an extra cycle between T4 and T5.

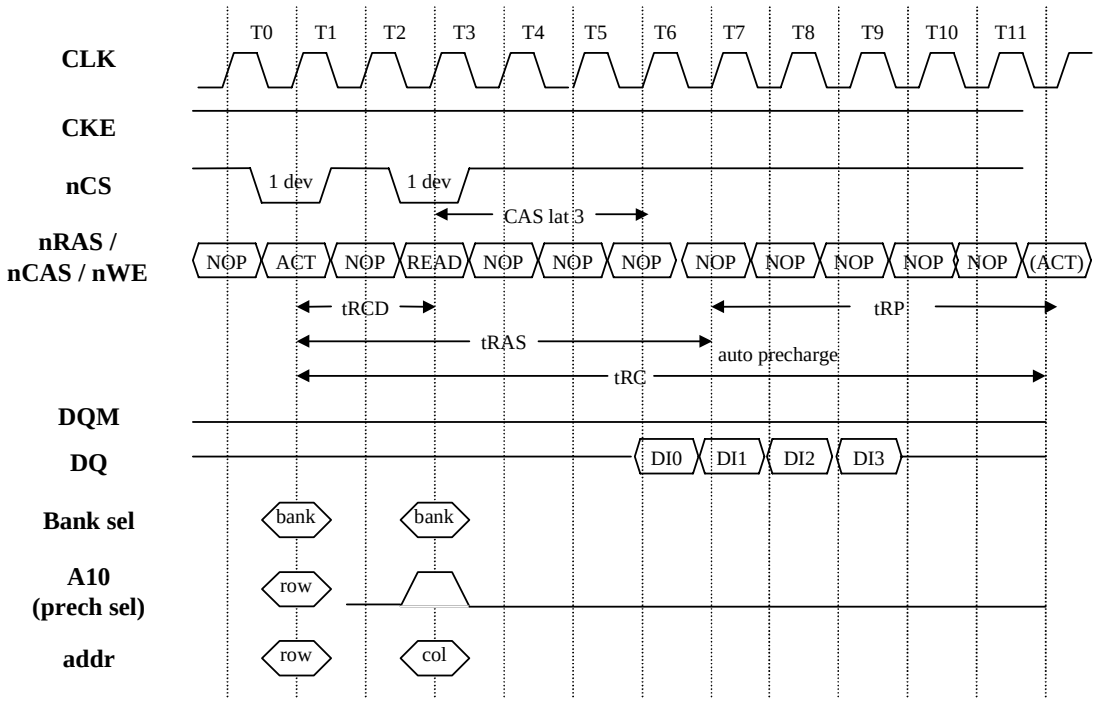


Figure 6. SDRAM Read Cycles SDCAS Latency = 3

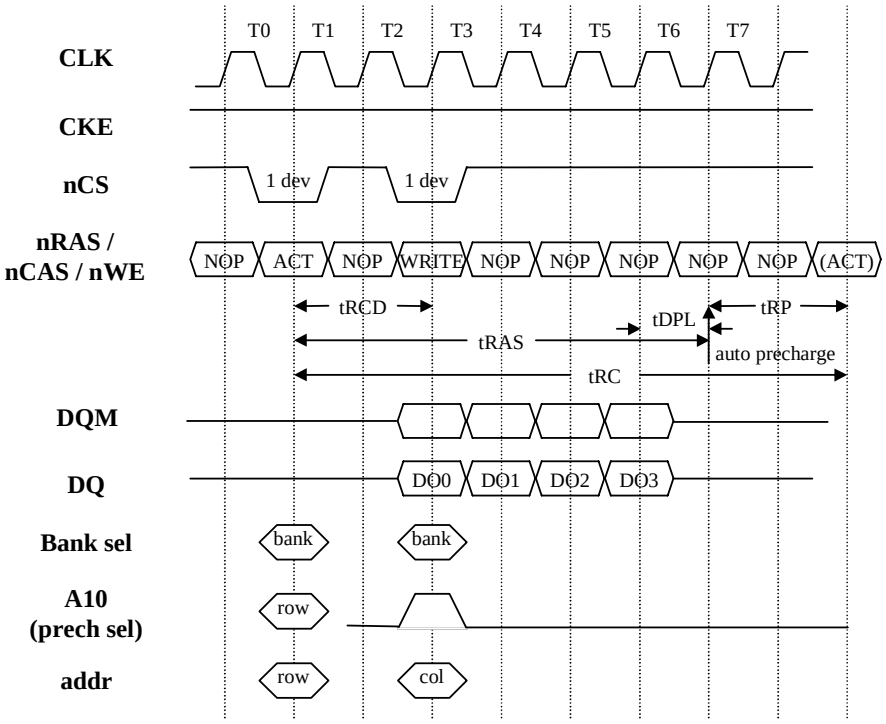


Figure 7. SDRAM Write Cycles

Note: tDPL (data in to PRE command period command) = 10 ns or 1 cycle at 36 MHz.

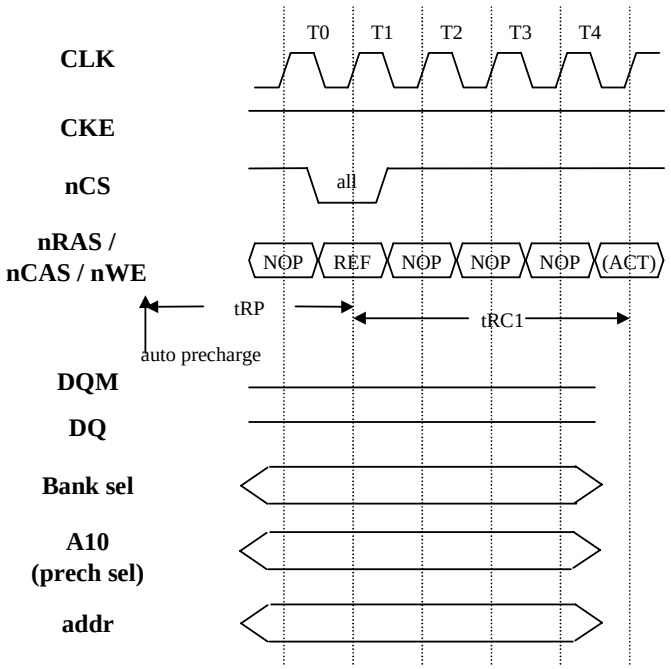


Figure 8. SDRAM Refresh Cycles

Note: tRC1 (REF to REF/ACT command period [refresh]) = 90 ns or 4 cycles at 36 MHz.

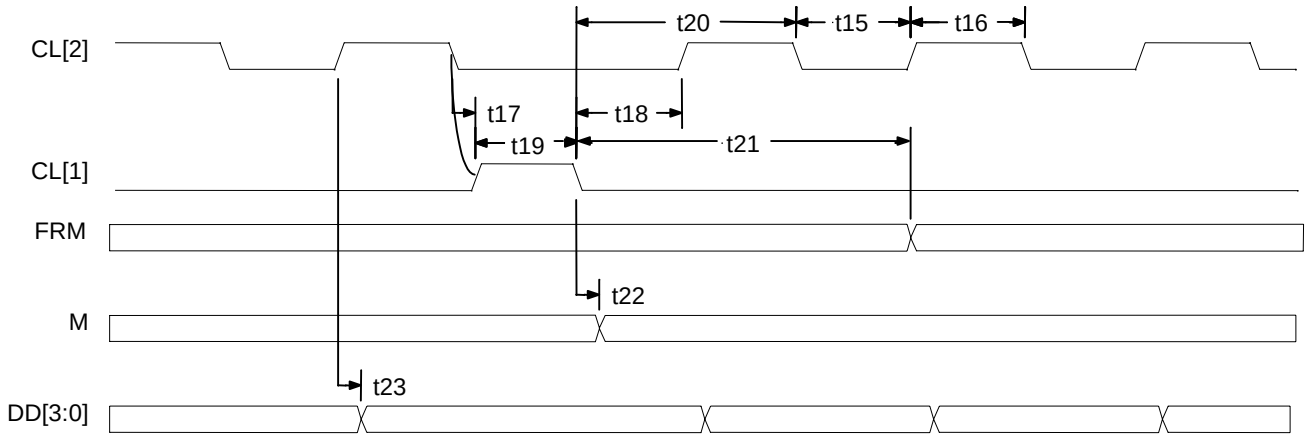


Figure 9. LCD Controller Timings

Notes:
1) The figure shows the end of a line.
2) If FRM is high during the CL[1] pulse, this marks the first line in the display.
3) CL[2] low time is doubled during the CL[1] high pulse.

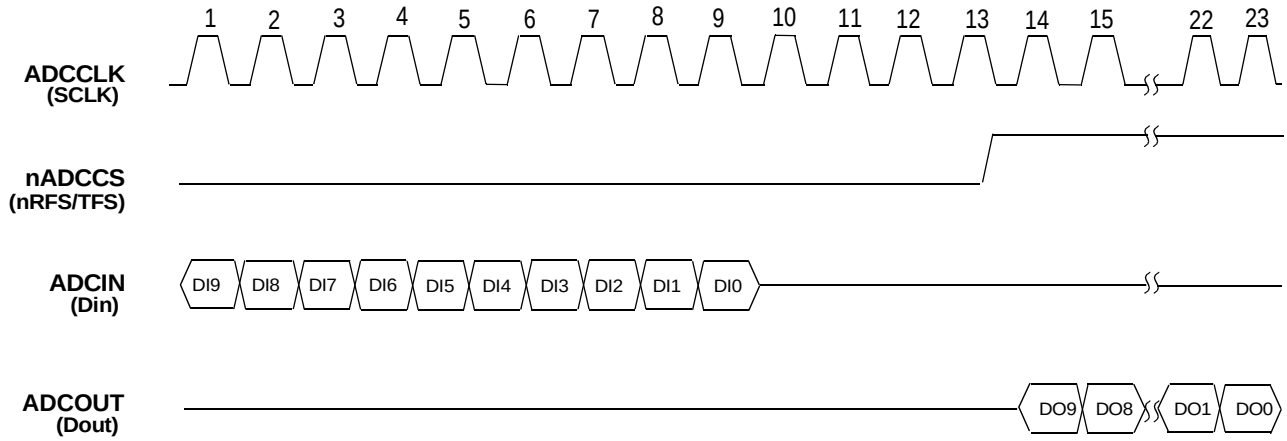


Figure 10. SSI1 Interface for AD7811/2

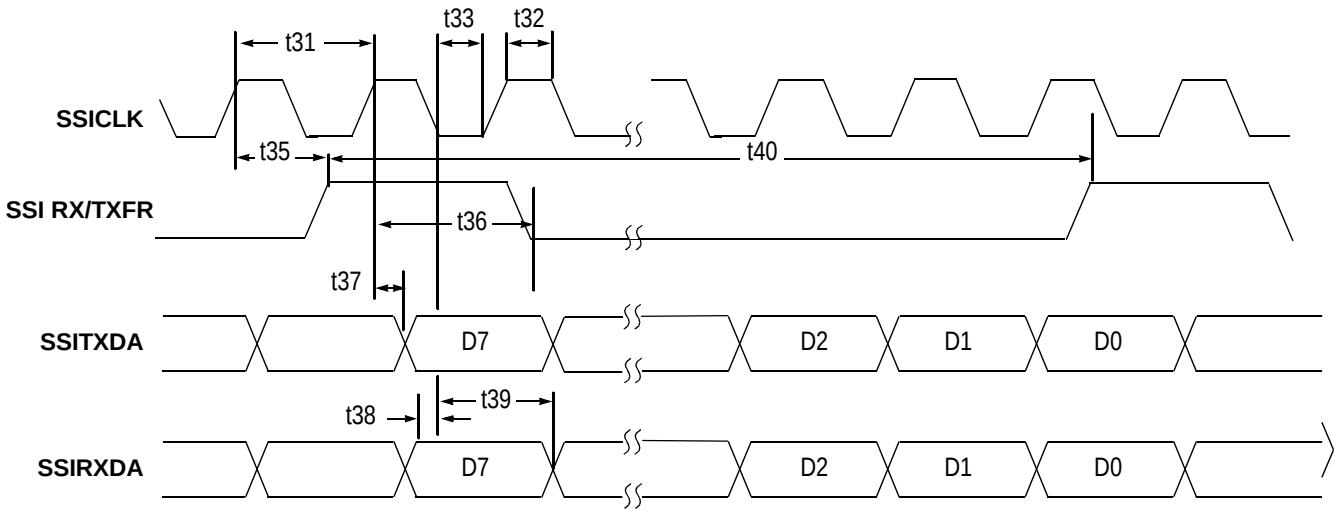


Figure 11. SSI2 Interface Timings

3. 208-PIN LQFP PACKAGE CHARACTERISTICS

3.1. 208-Pin LQFP Pin Diagram

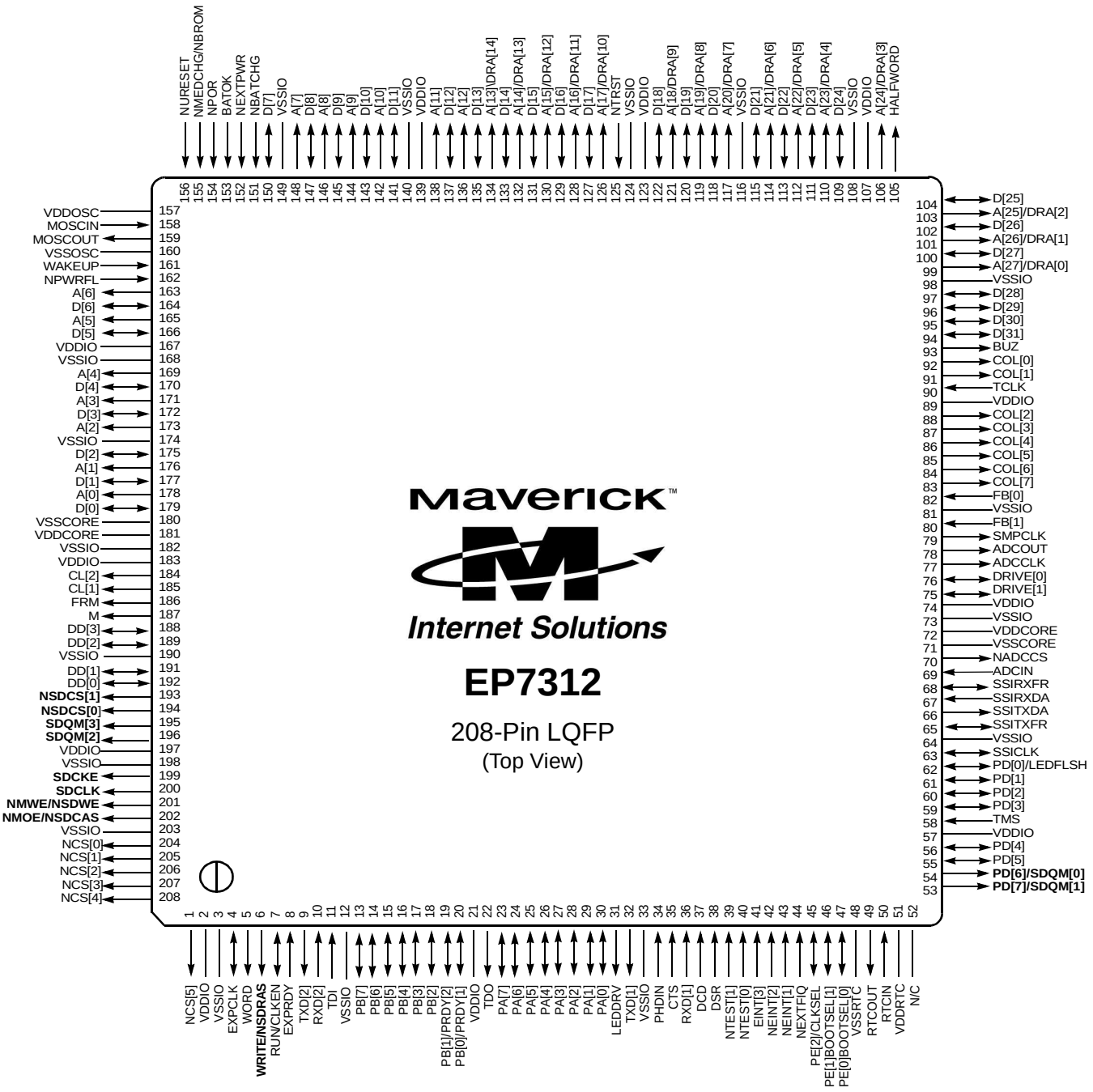


Figure 12. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Notes: 1. N/C should not be grounded but left as no connects.

2. Pin differences between the EP7212 and the EP7312 are bolded.

3.2. 208-Pin LQFP Package Specifications

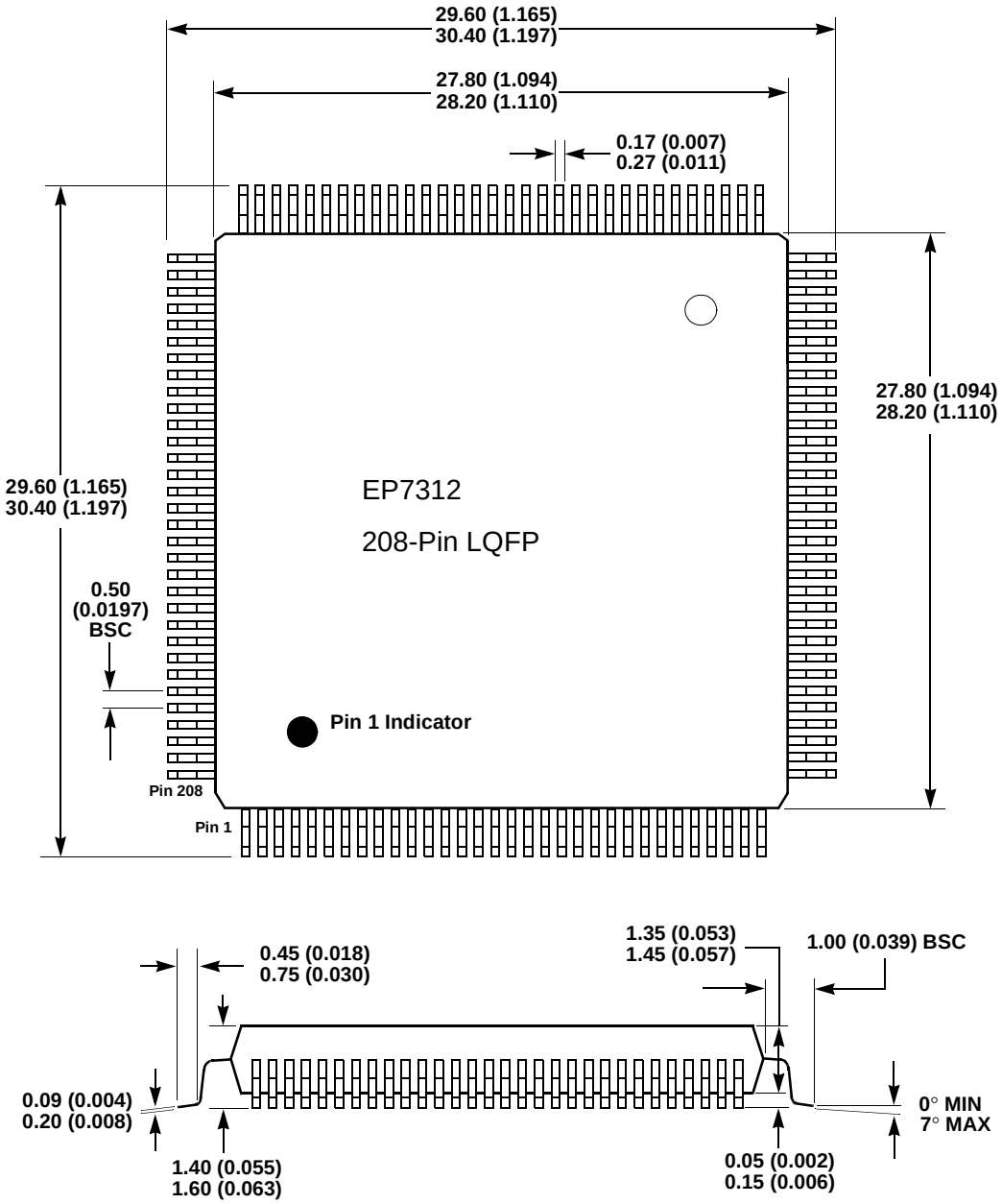


Figure 13. 208-Pin LQFP Package Outline Drawing

Notes:
1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 12. For pin descriptions see the *EP7312 User's Manual*.

3.3. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Type	Strength	Reset State
1	nCS[5]	Out	1	High
2	VDDIO	Pad Pwr		
3	VSSIO	Pad Gnd		
4	EXPCLK	I/O	1	
5	WORD	Out	1	Low
6	WRITE/ nSDRAS	Out	1	Low
7	RUN/CLKEN	O	1	Low
8	EXPRDY	In	1	
9	TXD[2]	Out	1	High
10	RXD[2]	In		
11	TDI	In	with p/u*	
12	VSSIO	Pad Gnd		
13	PB[7]	I/O	1	Input
14	PB[6]	I/O	1	Input
15	PB[5]	I/O	1	Input
16	PB[4]	I/O	1	Input
17	PB[3]	I/O	1	Input
18	PB[2]	I/O	1	Input
19	PB[1]/ PRDY2	I/O	1	Input
20	PB[0]/ PRDY1	I/O	1	Input
21	VDDIO	Pad Pwr		
22	TDO	Out	1	Three state
23	PA[7]	I/O	1	Input
24	PA[6]	I/O	1	Input
25	PA[5]	I/O	1	Input
26	PA[4]	I/O	1	Input
27	PA[3]	I/O	1	Input
28	PA[2]	I/O	1	Input
29	PA[1]	I/O	1	Input
30	PA[0]	I/O	1	Input
31	LEDDRV	Out	1	Low
32	TXD[1]	Out	1	High
33	VSSIO	Pad Gnd	1	High
34	PHDIN	In		
35	CTS	In		
36	RXD[1]	In		
37	DCD	In		
38	DSR	In		
39	nTEST[1]	In	With p/u*	
40	nTEST[0]	In	With p/u*	
41	EINT[3]	In		
42	nEINT[2]	In		
43	nEINT[1]	In		
44	nEXTFIQ	In		
45	PE[2]/ CLKSEL	I/O	1	Input
46	PE[1]/ BOOTSEL[1]	I/O	1	Input
47	PE[0]/ BOOTSEL[0]	I/O	1	Input
48	VSSRTC	RTC Gnd		
49	RTCOUT	Out		
50	RTCIN	In		
51	VDDRTC	RTC power		
52	N/C			
53	PD[7]/ SDQM[1]	I/O	1	Low
54	PD[6]/ SDQM[0]	I/O	1	Low
55	PD[5]	I/O	1	Low
56	PD[4]	I/O	1	Low
57	VDDIO	Pad Pwr		
58	TMS	In	with p/u*	
59	PD[3]	I/O	1	Low
60	PD[2]	I/O	1	Low
61	PD[1]	I/O	1	Low
62	PD[0]/ LEDFLSH	I/O	1	Low
63	SSICLK	I/O	1	Input
64	VSSIO	Pad Gnd		
65	SSITXFR	I/O	1	Low
66	SSITXDA	Out	1	Low
67	SSIRXDA	In		
68	SSIRXFR	I/O		Input
69	ADCIN	In		
70	nADCCS	Out	1	High

Table 8. 208-Pin LQFP Numeric Pin Listing

Table 8. 208-Pin LQFP Numeric Pin Listing *(cont.)*

Pin No.	Signal	Type	Strength	Reset State
71	VSSCORE	Core Gnd		
72	VDDCORE	Core Pwr		
73	VSSIO	Pad Gnd		
74	VDDIO	Pad Pwr		
75	DRIVE[1]	I/O	2	High / Low
76	DRIVE[0]	I/O	2	High / Low
77	ADCCLK	Out	1	Low
78	ADCOUT	Out	1	Low
79	SMPCLK	Out	1	Low
80	FB[1]	In		
81	VSSIO	Pad Gnd		
82	FB[0]	In		
83	COL[7]	Out	1	High
84	COL[6]	Out	1	High
85	COL[5]	Out	1	High
86	COL[4]	Out	1	High
87	COL[3]	Out	1	High
88	COL[2]	Out	1	High
89	VDDIO	Pad Pwr		
90	TCLK	In		
91	COL[1]	Out	1	High
92	COL[0]	Out	1	High
93	BUZ	Out	1	Low
94	D[31]	I/O	1	Low
95	D[30]	I/O	1	Low
96	D[29]	I/O	1	Low
97	D[28]	I/O	1	Low
98	VSSIO	Pad Gnd		
99	A[27]/DRA[0]	Out	2	Low
100	D[27]	I/O	1	Low
101	A[26]/DRA[1]	Out	2	Low
102	D[26]	I/O	1	Low
103	A[25]/DRA[2]	Out	2	Low
104	D[25]	I/O	1	Low
105	HALFWORD	Out	1	Low
106	A[24]/DRA[3]	Out	1	Low
107	VDDIO	Pad Pwr		—
108	VSSIO	Pad Gnd		—

Table 8. 208-Pin LQFP Numeric Pin Listing *(cont.)*

Pin No.	Signal	Type	Strength	Reset State
109	D[24]	I/O	1	Low
110	A[23]/DRA[4]	Out	1	Low
111	D[23]	I/O	1	Low
112	A[22]/DRA[5]	Out	1	Low
113	D[22]	I/O	1	Low
114	A[21]/DRA[6]	Out	1	Low
115	D[21]	I/O	1	Low
116	VSSIO	Pad Gnd		
117	A[20]/DRA[7]	Out	1	Low
118	D[20]	I/O	1	Low
119	A[19]/DRA[8]	Out	1	Low
120	D[19]	I/O	1	Low
121	A[18]/DRA[9]	Out	1	Low
122	D[18]	I/O	1	Low
123	VDDIO	Pad Pwr		
124	VSSIO	Pad Gnd		
125	nTRST	In		
126	A[17]/ DRA[10]	Out	1	Low
127	D[17]	I/O	1	Low
128	A[16]/ DRA[11]	Out	1	Low
129	D[16]	I/O	1	Low
130	A[15]/ DRA[12]	Out	1	Low
131	D[15]	I/O	1	Low
132	A[14]/ DRA[13]	Out	1	Low
133	D[14]	I/O	1	Low
134	A[13]/ DRA[14]	Out	1	Low
135	D[13]	I/O	1	Low
136	A[12]	Out	1	Low
137	D[12]	I/O	1	Low
138	A[11]	Out	1	Low
139	VDDIO	Pad Pwr		
140	VSSIO	Pad Gnd		
141	D[11]	I/O	1	Low
142	A[10]	Out	1	Low
143	D[10]	I/O	1	Low
144	A[9]	Out	1	Low
145	D[9]	I/O	1	Low
146	A[8]	Out	1	Low
147	D[8]	I/O	1	Low
148	A[7]	Out	1	Low

Table 8. 208-Pin LQFP Numeric Pin Listing *(cont.)*

Pin No.	Signal	Type	Strength	Reset State
149	VSSIO	Pad Gnd		
150	D[7]	I/O	1	Low
151	nBATCHG	In		
152	nEXTPWR	In		
153	BATOK	In		
154	nPOR	In	Schmitt	
155	nMEDCHG/ nBROM	In		
156	nURESET	In	Schmitt	
157	VDDOSC	Osc Pwr		
158	MOSCIN	Osc		
159	MOSCOUT	Osc		
160	VSSOSC	Osc Gnd		
161	WAKEUP	In	Schmitt	
162	nPWRFL	In		
163	A[6]	Out	1	Low
164	D[6]	I/O	1	Low
165	A[5]	Out	1	Low
166	D[5]	I/O	1	Low
167	VDDIO	Pad Pwr		
168	VSSIO	Pad Gnd		
169	A[4]	Out	1	Low
170	D[4]	I/O	1	Low
171	A[3]	Out	2	Low
172	D[3]	I/O	1	Low
173	A[2]	Out	2	Low
174	VSSIO	Pad Gnd		
175	D[2]	I/O	1	Low
176	A[1]	Out	2	Low
177	D[1]	I/O	1	Low
178	A[0]	Out	2	Low
179	D[0]	I/O	1	Low
180	VSS CORE	Core Gnd		
181	VDD CORE	Core Pwr		
182	VSSIO	Pad Gnd		
183	VDDIO	Pad Pwr		
184	CL[2]	Out	1	Low
185	CL[1]	Out	1	Low
186	FRM	Out	1	Low
187	M	Out	1	Low

Table 8. 208-Pin LQFP Numeric Pin Listing *(cont.)*

Pin No.	Signal	Type	Strength	Reset State
188	DD[3]	I/O	1	Low
189	DD[2]	I/O	1	Low
190	VSSIO	Pad Gnd		
191	DD[1]	I/O	1	Low
192	DD[0]	I/O	1	Low
193	nSDCS[1]	Out	1	High
194	nSDCS[0]	Out	1	High
195	SDQM[3]	I/O	2	Low
196	SDQM[2]	I/O	2	Low
197	VDDIO	Pad Pwr		
198	VSSIO	Pad Gnd		
199	SDCKE	I/O	2	Low
200	SDCLK	I/O	2	Low
201	nMWE/nSDWE	Out	1	High
202	nMOE/ nSD-CAS	Out	1	High
203	VSSIO	Pad Gnd		
204	nCS[0]	Out	1	High
205	nCS[1]	Out	1	High
206	nCS[2]	Out	1	High
207	nCS[3]	Out	1	High
208	nCS[4]	Out	1	High

Note: ‘With p/u’ means with internal pull-up on the pin.

Table 8. 208-Pin LQFP Numeric Pin Listing *(cont.)*

3.4. JTAG Boundary Scan Signal Ordering for 208-Pin LQFP

Pin No.	Signal	Type	Position
1	NCS[5]	Out	1
4	EXPCLK	I/O	3
5	WORD	Out	6
6	WRITE	Out	8
7	RUN/CLKEN	O	10
8	EXPRDY	I	13
9	TXD2	Out	14
10	RXD2	In	16
13	PB[7]	I/O	17
14	PB[6]	I/O	20
15	PB[5]	I/O	23
16	PB[4]	I/O	26
17	PB[3]	I/O	29
18	PB[2]	I/O	32
19	PB[1]/PRDY2	I/O	35
20	PB[0]/PRDY1	I/O	38
23	PA[7]	I/O	41
24	PA[6]	I/O	44
25	PA[5]	I/O	47
26	PA[4]	I/O	50
27	PA[3]	I/O	53
28	PA[2]	I/O	56
29	PA[1]	I/O	59
30	PA[0]	I/O	62
31	LEDDRV	Out	65
32	TXD1	Out	67
34	PHDIN	In	69
35	CTS	In	70
36	RXD1	In	71
37	DCD	In	72
38	DSR	In	73
39	NTEST1	In	74
40	NTEST0	In	75
41	EINT3	In	76
42	NEINT2	In	77
43	NEINT1	In	78
44	NEXTFIQ	In	79
45	PE[2]/CLKSEL	I/O	80
46	PE[1]/BOOTSEL1	I/O	83
47	PE[0]/BOOTSEL0	I/O	86

Table 9. JTAG Boundary Scan Signal Ordering for 208-Pin LQFP Package

Pin No.	Signal	Type	Position
53	PD[7]	I/O	89
54	PD[6]	I/O	92
55	PD[5]	I/O	95
56	PD[4]	I/O	98
59	PD[3]	I/O	101
60	PD[2]	I/O	104
61	PD[1]	I/O	107
62	PD[0]/LEDFLSH	O	110
68	SSIRXFR	I/O	122
69	ADCIN	In	125
70	NADCCS	Out	126
75	DRIVE1	I/O	128
76	DRIVE0	I/O	131
77	ADCCLK	Out	134
78	ADCOUT	Out	136
79	SMPCLK	Out	138
80	FB1	In	140
82	FB0	In	141
83	COL7	Out	142
84	COL6	Out	144
85	COL5	Out	146
86	COL4	Out	148
87	COL3	Out	150
88	COL2	Out	152
91	COL1	Out	154
92	COL0	Out	156
93	BUZ	Out	158
94	D[31]	I/O	160
95	D[30]	I/O	163
96	D[29]	I/O	166
97	D[28]	I/O	169
99	A[27]/DRA[0]	Out	172
100	D[27]	I/O	174
101	A[26]/DRA[1]	Out	177
102	D[26]	I/O	179
103	A[25]/DRA[2]	Out	182
104	D[25]	I/O	184
105	HALFWORD	Out	187
106	A[24]/DRA[3]	Out	189
109	D[24]	I/O	191
110	A[23]/DRA[4]	Out	194
111	D[23]	I/O	196
112	A[22]/DRA[5]	Out	199
113	D[22]	I/O	201

Table 9. JTAG Boundary Scan Signal Ordering for 208-Pin LQFP Package *(cont.)*

Pin No.	Signal	Type	Position
114	A[21]/DRA[6]	Out	204
115	D[21]	I/O	206
117	A[20]/DRA[7]	Out	209
118	D[20]	I/O	211
119	A[19]/DRA[8]	Out	214
120	D[19]	I/O	216
121	A[18]/DRA[9]	Out	219
122	D[18]	I/O	221
126	A[17]/DRA[10]	Out	224
127	D[17]	I/O	226
128	A[16]/DRA[11]	Out	229
129	D[16]	I/O	231
130	A[15]/DRA[12]	Out	234
131	D[15]	I/O	236
132	A[14]	Out	239
133	D[14]	I/O	241
134	A[13]	Out	244
135	D[13]	I/O	246
136	A[12]	Out	249
137	D[12]	I/O	251
138	A[11]	Out	254
141	D[11]	I/O	256
142	A[10]	Out	259
143	D[10]	I/O	261
144	A[9]	Out	264
145	D[9]	I/O	266
146	A[8]	Out	269
147	D[8]	I/O	271
148	A[7]	Out	274
150	D[7]	I/O	276
151	NBATCHG	In	279
152	NEXTPWR	In	280
153	BATOK	In	281
154	NPOR	In	282
155	NMEDCHG/BROM	In	283
156	NURESET	In	284
161	WAKEUP	In	285
162	NPWRFL	In	286
163	A[6]	Out	287
164	D[6]	I/O	289
165	A[5]	Out	292
166	D[5]	I/O	294
169	A[4]	Out	297
170	D[4]	I/O	299

Table 9. JTAG Boundary Scan Signal Ordering for 208-Pin LQFP Package *(cont.)*

Pin No.	Signal	Type	Position
171	A[3]	Out	302
172	D[3]	I/O	304
173	A[2]	Out	307
175	D[2]	I/O	309
176	A[1]	Out	312
177	D[1]	I/O	314
178	A[0]	Out	317
179	D[0]	I/O	319
184	CL2	Out	322
185	CL1	Out	324
186	FRM	Out	326
187	M	Out	328
188	DD[3]	I/O	330
189	DD[2]	I/O	333
191	DD[1]	I/O	336
192	DD[0]	I/O	339
193	nSDRAS[1]	Out	342
194	nSDRAS[0]	Out	344
195	nSDCAS[3]	I/O	346
196	nSDCAS[2]	I/O	349
199	nSDCAS[1]	I/O	352
200	nSDCAS[0]	I/O	355
201	NMWE	Out	358
202	NMOE	Out	360
204	NCS[0]	Out	362
205	NCS[1]	Out	364
206	NCS[2]	Out	366
207	NCS[3]	Out	368
208	NCS[4]	Out	370

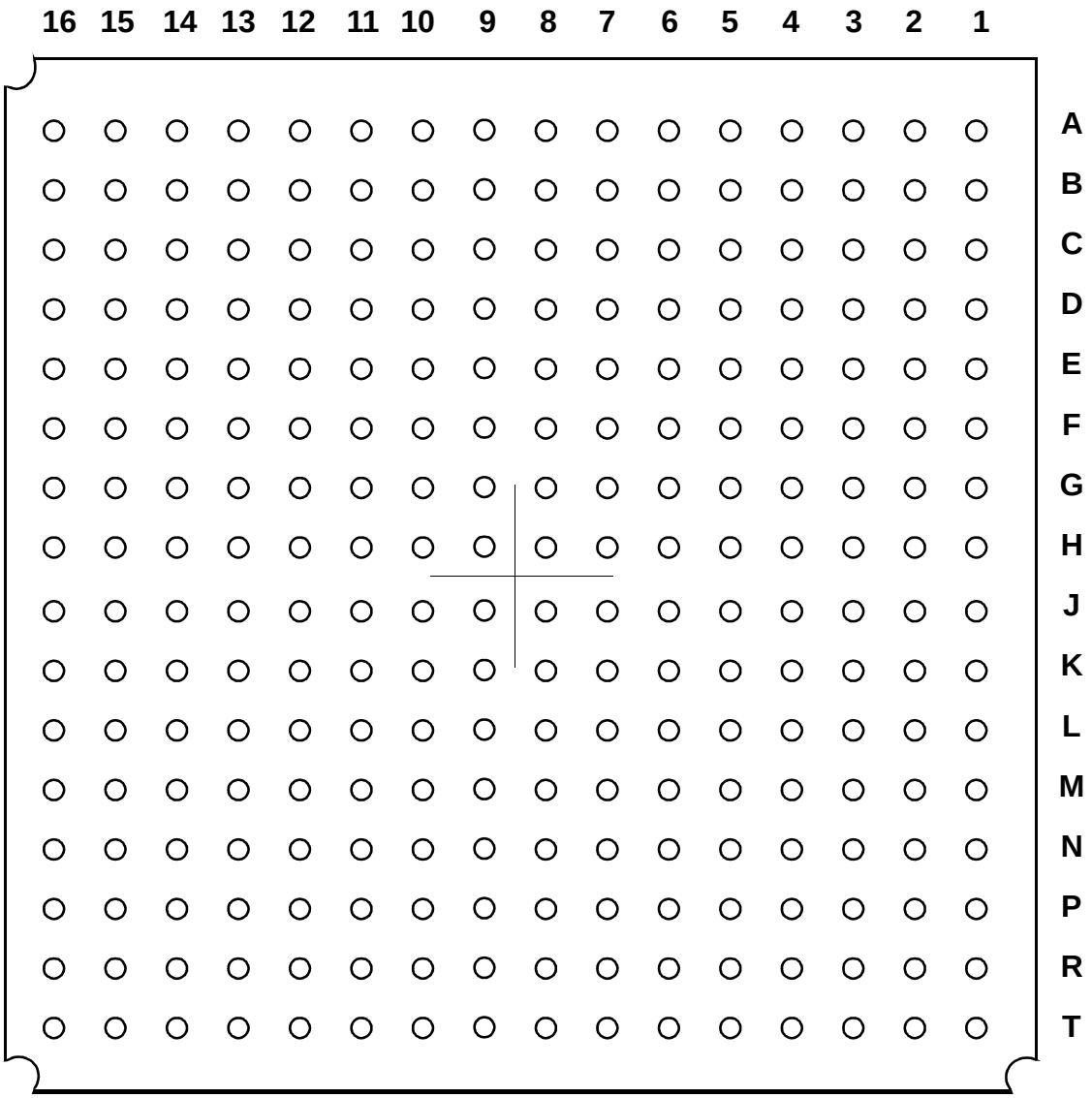
Table 9. JTAG Boundary Scan Signal Ordering for 208-Pin LQFP Package *(cont.)*

Notes:

1) See *EP7312 Users' Manual* for pin naming / functionality.
2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

4. 256-PIN PBGA PACKAGE CHARACTERISTICS

4.1. 256-PIN PBGA PIN DIAGRAM

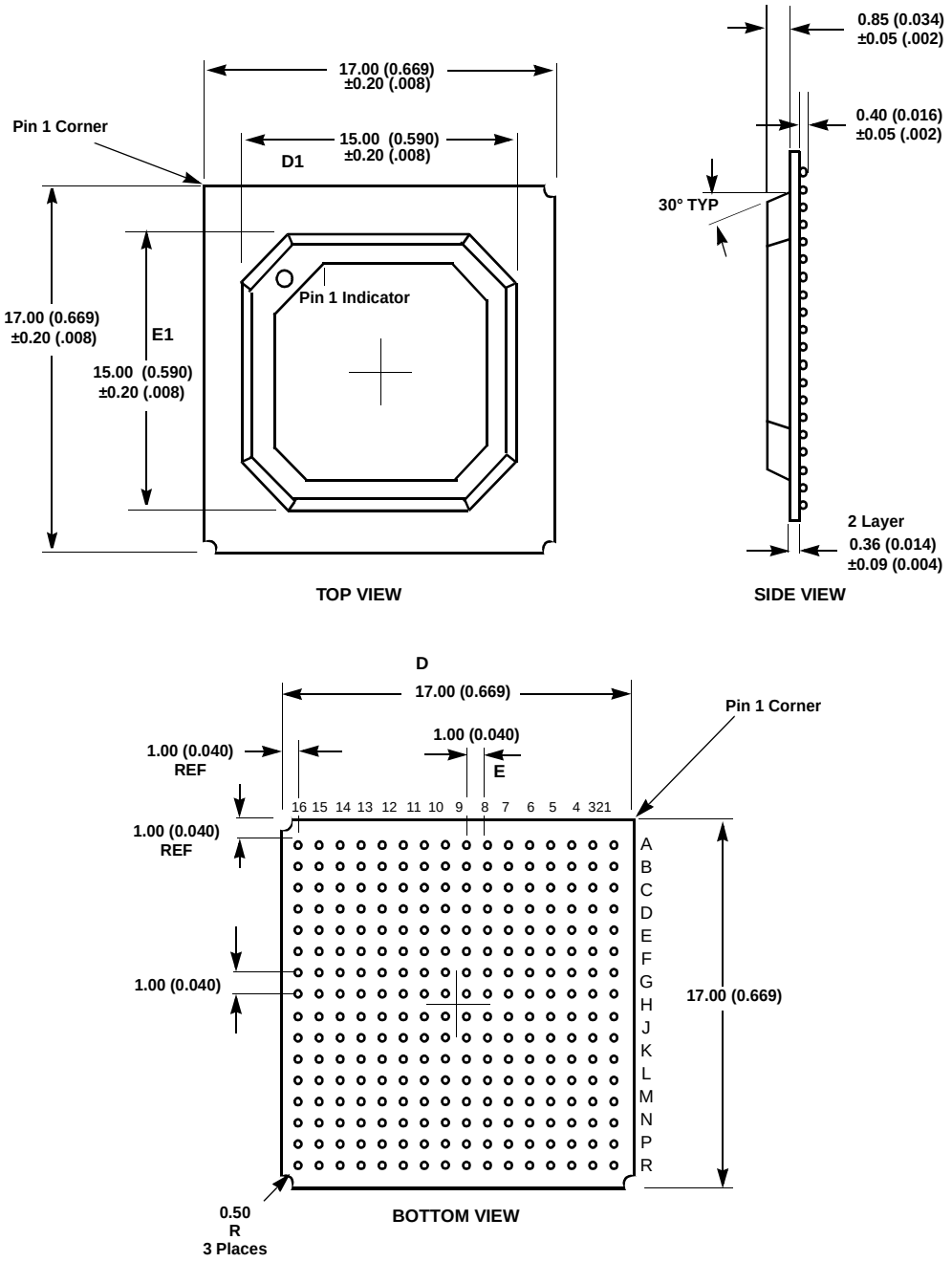


256-Ball PBGA
(Bottom View)

Figure 13. 256-Ball Pin Diagram

Note: For package specifications, please see Figure 14.

4.2. EP7312 256-Ball PBGA (17 × 17 × 1.61-mm Body) Dimensions



JEDEC #: MO-151

Ball Diameter: 0.50 mm ± 0.10 mm

Figure 14. 256-Ball PBGA Package Drawing

Notes:
1. For pin locations, please see Figure 13**.** For pin descriptions, See the *EP7312 User's Manual.*
2. Dimensions are in millimeters (inches), and controlling dimension is millimeter.
3. Before beginning any new EP7312 design, contact Cirrus Logic for the latest package information.

4.3. 256-Ball PBGA Ball Listing

Ball Location	Name	Type
A1	VDDIO	Pad power
A2	nCS[4]	O
A3	nCS[1]	O
A4	SDCLK	O
A5	nSDQM3	O
A6	DD[1]	O
A7	M	O
A8	VDDIO	Pad power
A9	D[0]	I/O
A10	D[2]	I/O
A11	A[3]	O
A12	VDDIO	Pad power
A13	A[6]	O
A14	MOSCOUT	O
A15	VDDOSC	Oscillator power
A16	VSSIO	Pad ground
B1	nCS[5]	O
B2	VDDIO	Pad power
B3	nCS[3]	O
B4	nMOE/nSDCAS	O
B5	VDDIO	Pad power
B6	nSDCS[1]	O
B7	DD[2]	O
B8	CL[1]	O
B9	VDDCORE	Core power
B10	D[1]	I/O
B11	A[2]	O
B12	A[4]	O
B13	A[5]	O
B14	WAKEUP	I
B15	VDDIO	Pad power
B16	nURESET	I
C1	VDDIO	Pad power
C2	EXPCLK	I
C3	VSSIO	Pad ground
C4	VDDIO	Pad power
C5	VSSIO	Pad ground
C6	VSSIO	Pad ground
C7	VSSIO	Pad ground
C8	VDDIO	Pad power
C9	VSSIO	Pad ground
C10	VSSIO	Pad ground
C11	VSSIO	Pad ground

Table 10. 256-Ball PBGA Ball Listing

Ball Location	Name	Type
C12	VDDIO	Pad power
C13	VSSIO	Pad ground
C14	VSSIO	Pad ground
C15	nPOR	I
C16	nEXTPWR	I
D1	WRITE/nSDRAS	O
D2	EXPRDY	I
D3	VSSIO	Pad ground
D4	VDDIO	Pad power
D5	nCS[2]	O
D6	nMWE/nSDWE	O
D7	nSDCS[0]	O
D8	CL[2]	O
D9	VSSRTC	Core ground
D10	D[4]	I/O
D11	nPWRFL	I
D12	MOSCIN	I
D13	VDDIO	Pad power
D14	VSSIO	Pad ground
D15	D[7]	I/O
D16	D[8]	I/O
E1	RXD[2]	I
E2	PB[7]	I
E3	TDI	I
E4	WORD	O
E5	VSSIO	Pad ground
E6	nCS[0]	O
E7	SDQM[2]	O
E8	FRM	O
E9	A[0]	O
E10	D[5]	I/O
E11	VSSOSC	Oscillator ground
E12	VSSIO	Pad ground
E13	nMED-CHG/nBROM	I
E14	VDDIO	Pad power
E15	D[9]	I/O
E16	D[10]	I/O
F1	PB[5]	I
F2	PB[3]	I
F3	VSSIO	Pad ground
F4	TXD[2]	O
F5	RUN/CLKEN	O
F6	VSSIO	Pad ground

Table 10. 256-Ball PBGA Ball Listing *(cont.)*

Ball Location	Name	Type
F7	SDCKE	O
F8	DD[3]	O
F9	A[1]	O
F10	D[6]	I/O
F11	VSSRTC	RTC ground
F12	BATOK	I
F13	nBATCHG	I
F14	VSSIO	Pad ground
F15	D[11]	I/O
F16	VDDIO	Pad power
G1	PB[1]/PRDY[2]	I
G2	VDDIO	Pad power
G3	TDO	O
G4	PB[4]	I
G5	PB[6]	I
G6	VSSRTC	Core ground
G7	VSSRTC	RTC ground
G8	DD[0]	O
G9	D[3]	I/O
G10	VSSRTC	RTC ground
G11	A[7]	O
G12	A[8]	O
G13	A[9]	O
G14	VSSIO	Pad ground
G15	D[12]	I/O
G16	D[13]	I/O
H1	PA[7]	I
H2	PA[5]	I
H3	VSSIO	Pad ground
H4	PA[4]	I
H5	PA[6]	I
H6	PB[0]/PRDY[1]	I
H7	PB[2]	I
H8	VSSRTC	RTC ground
H9	VSSRTC	RTC ground
H10	A[10]	O
H11	A[11]	O
H12	A[12]	O
H13	A[13]/DRA[14]	O
H14	VSSIO	Pad ground
H15	D[14]	I/O
H16	D[15]	I/O
J1	PA[3]	I
J2	PA[1]	I
J3	VSSIO	Pad ground

Table 10. 256-Ball PBGA Ball Listing *(cont.)*

Ball Location	Name	Type
J4	PA[2]	I
J5	PA[0]	I
J6	TXD[1]	O
J7	CTS	I
J8	VSSRTC	RTC ground
J9	VSSRTC	RTC ground
J10	A[17]/DRA[10]	O
J11	A[16]/DRA[11]	O
J12	A[15]/DRA[12]	O
J13	A[14]/DRA[13]	O
J14	nTRST	I
J15	D[16]	I/O
J16	D[17]	I/O
K1	LEDDRV	O
K2	PHDIN	I
K3	VSSIO	Pad ground
K4	DCD	I
K5	nTEST[1]	I
K6	EINT[3]	I
K7	VSSRTC	RTC ground
K8	ADCIN	I
K9	COL[4]	O
K10	TCLK	I
K11	D[20]	I/O
K12	D[19]	I/O
K13	D[18]	I/O
K14	VSSIO	Pad ground
K15	VDDIO	Pad power
K16	VDDIO	Pad power
L1	RXD[1]	I
L2	DSR	I
L3	VDDIO	Pad power
L4	nEINT[1]	I
L5	PE[2]/CLKSEL	I
L6	VSSRTC	RTC ground
L7	PD[0]/LEDFLSH	I/O
L8	VSSRTC	Core ground
L9	COL[6]	O
L10	D[31]	I/O
L11	VSSRTC	RTC ground
L12	A[22]/DRA[5]	O
L13	A[21]/DRA[6]	O
L14	VSSIO	Pad ground
L15	A[18]/DRA[9]	O
L16	A[19]/DRA[8]	O

Table 10. 256-Ball PBGA Ball Listing *(cont.)*

Ball Location	Name	Type
M1	nTEST[0]	I
M2	nEINT[2]	I
M3	VDDIO	Pad power
M4	PE[0]/BOOT-SEL[0]	I
M5	TMS	I
M6	VDDIO	Pad power
M7	SSITXFR	I/O
M8	DRIVE[1]	I/O
M9	FB[0]	I
M10	COL[0]	O
M11	D[27]	I/O
M12	VSSIO	Pad ground
M13	A[23]/DRA[4]	O
M14	VDDIO	Pad power
M15	A[20]/DRA[7]	O
M16	D[21]	I/O
N1	nEXTFIQ	I
N2	PE[1]/BOOT-SEL[1]	I
N3	VSSIO	Pad ground
N4	VDDIO	Pad power
N5	PD[5]	I/O
N6	PD[2]	I/O
N7	SSIRXDA	I/O
N8	ADCCLK	O
N9	SMPCLK	O
N10	COL[2]	O
N11	D[29]	I/O
N12	D[26]	I/O
N13	HALFWORD	O
N14	VSSIO	Pad ground
N15	D[22]	I/O
N16	D[23]	I/O
P1	VSSRTC	RTC ground
P2	RTCOUT	O
P3	VSSIO	Pad ground
P4	VSSIO	Pad ground
P5	VDDIO	Pad power
P6	VSSIO	Pad ground
P7	VSSIO	Pad ground
P8	VDDIO	Pad power
P9	VSSIO	Pad ground
P10	VDDIO	Pad power
P11	VSSIO	Pad ground

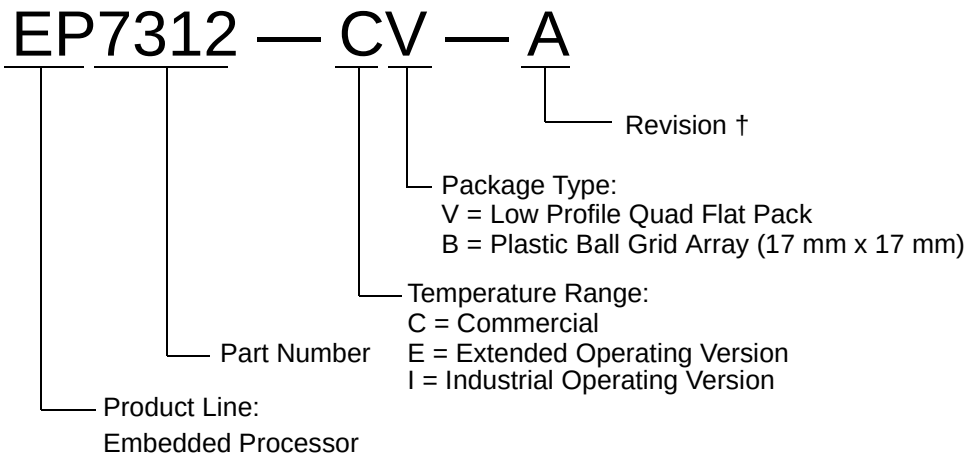
Table 10. 256-Ball PBGA Ball Listing *(cont.)*

Ball Location	Name	Type
P12	VSSIO	Pad ground
P13	VDDIO	Pad power
P14	VSSIO	Pad ground
P15	D[24]	I/O
P16	VDDIO	Pad power
R1	RTCIN	I/O
R2	VDDIO	Pad power
R3	PD[4]	I/O
R4	PD[1]	I/O
R5	SSITXDA	O
R6	nADCCS	O
R7	VDDIO	Pad power
R8	ADCOUT	O
R9	COL[7]	O
R10	COL[3]	O
R11	COL[1]	O
R12	D[30]	I/O
R13	A[27]/DRA[0]	O
R14	A[25]/DRA[2]	O
R15	VDDIO	Pad power
R16	A[24]/DRA[3]	O
T1	VDDRTC	RTC power
T2	PD[7]/SDQM[1]	I/O
T3	PD[6]/SDQM[0]	I/O
T4	PD[3]	I/O
T5	SSICLK	I/O
T6	SSIRXFR	–
T7	VDDCORE	Core power
T8	DRIVE[0]	I/O
T9	FB[1]	I
T10	COL[5]	O
T11	VDDIO	Pad power
T12	BUZ	O
T13	D[28]	I/O
T14	A[26]/DRA[1]	O
T15	D[25]	I/O
T16	VSSIO	Pad ground

Table 10. 256-Ball PBGA Ball Listing *(cont.)*

5. ORDERING INFORMATION

The order number for the device is:



Note: † Contact Cirrus Logic for up-to-date information on revisions. Go to the Cirrus Logic Internet site at http://cirrus.com/corporate/contacts to find contact information for your local sales representative.

6. INDEX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