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A Flexible Design Platform for Si/SiGe Exchange-Only Qubits with Low Disorder

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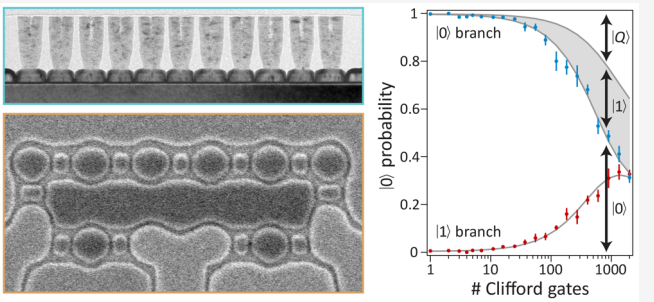
ABSTRACT: Spin-based silicon quantum dots are an attractive qubit technology for quantum information processing with respect to coherence time, control, and engineering. Here we present an exchange-only Si qubit device platform that combines the throughput of CMOS-like wafer processing with the versatility of direct-write lithography. The technology, which we coin "SLEDGE", features dot-shaped gates that are patterned simultaneously on one topographical plane and subsequently connected by vias to interconnect metal lines. The process design enables nontrivial layouts as well as flexibility in gate dimensions, material selection, and additional device features such as for rf qubit control. We show that the SLEDGE process has reduced electrostatic disorder with respect to traditional overlapping gate devices with lift-off metallization, and we present spin coherent exchange oscillations and single qubit blind randomized benchmarking data.



KEYWORDS: *quantum dots, qubits, exchange-only, silicon, silicon germanium*

Gated silicon quantum dots are of widespread interest as physical qubits for quantum information processing due to favorable coherence times,[1,2] a variety of control techniques,[3−5] and the prospect of leveraging well-established Si CMOS engineering for density, scale, and yield. However, much of the Si qubit work to date has been demonstrated using gates defined by lift-off metallization techniques,[6,7] which suffer from poor wafer-level process control and which have not been used in Si integrated circuit foundries in several decades.[8] There have been examples of Si quantum dots fabricated in CMOS facilities with industry-standard processes,[9−12] some of which have exhibited coherent control of single electron spins. However, single-spin qubits are known to be susceptible to decoherence from global magnetic fields, among several disadvantages.[13] In this work, we present a device fabrication process termed SLEDGE (single-layer etch-defined gate electrodes) for Si/SiGe heterostructure exchange-only spin qubits. The SLEDGE platform uses processes designed for typical CMOS wafer fabrication, but it has inherent design flexibility for highly customizable device layouts. We show that the SLEDGE process has reduced electrostatic disorder with respect to lift-off technologies, and we show representative coherent exchange oscillations and single-qubit blind randomized benchmarking data to extract quantum gate performance.[5]

The SLEDGE technology is designed for heterostructure quantum dots, wherein semiconductor epitaxial boundaries and gate-defined electric fields confine and, in the latter case, manipulate individual electrons. A SLEDGE device, as shown in Figure 1A, consists of (1) a gate layer, in which all gates are patterned simultaneously on the same plane (i.e., uniplanar); and (2) back-end-of-line (BEOL) interconnect layers, in which vertical vias directly contact active gates and then spans ("M1") connect vias to macroscopic routing 10−50 μm away (not shown). The gate-level design (Figure 1B) is similar to recent work on Si quantum dot devices.[7,14] Plunger (P) and exchange (X) gates for accumulating and exchange-coupling electron spins are arranged collinearly and are offset from measure dot (M) gates used for charge sensing and readout of spin-to-charge conversion. Electrons are supplied by bath (B) gates via tunnel gates (T and Z) to P- and M-gates, respectively. Electron baths are supplied from source/drain Ohmics via supply gates (SG, see Figure 2A lower right),

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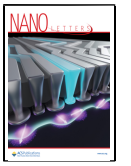

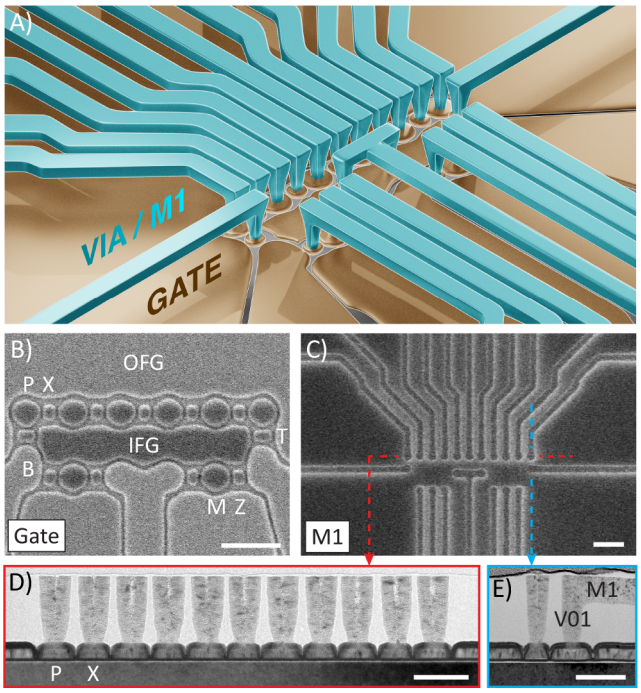

Figure 1. (A) Illustrated render of SLEDGE device. Gate level in tan and BEOL levels in aqua. (B) Top-down SEM image after gate etch with gaps evident between gates. Labels are as described in text. (C) Top-down SEM image after M1 CMP of dual damascene BEOL. Spans connect each via to bond-level routing (not shown). Scale bars in panels B and C are 200 nm. (D) Cross-section TEM image through P-gate row, as illustrated by red dashed line in panel C, showing BEOL vias contacting uniplanar gates. (E) Cross-section TEM image through right-most P−T-gates, as illustrated by blue dashed line in panel C, showing M1 trench in ILD connecting to P-gate via. Scale bars in (D) and (E) are 100 nm. Panel A courtesy of HRL Laboratories, LLC (graphic by John B. Carpenter). Copyright 2021.

which control Ohmic−bath contact resistance independent of B-gate voltage.[15] There are two field gates used for depleting carriers around the active gates: the inner field gate (IFG) for the region between P- and M-gates and the outer field gate (OFG) for the periphery. SLEDGE devices are nominally designed for triple-dot exchange-only qubit operation,[16] but could be used for a variety of encodings. Moreover, the process flow should be applicable to SiMOS devices,[17] assuming appropriate design adjustments are made to account for enhanced gate capacitance.

The uniplanar gate arrangement is a key feature of SLEDGE and is unlike conventional academic-style quantum dot qubit devices that have been demonstrated to date, in which exchange gates (sometimes referred to as barrier gates) are on a separate dielectric plane and may overlap laterally with plunger gates.[18] From a qubit operation perspective, exchange gates on the same topographical plane as plunger gates experience less electric field screening than those on a separate plane and therefore require smaller voltage throws to modulate exchange energy for qubit rotations (see the Supporting Information). The absence of an additional dielectric layer between exchange gates and quantum well may also reduce charge noise.[19] In addition to the uniplanar gate design, the quantum dot gates are notably dot-shaped (∼zero-dimensional), as opposed to conventional extended line-shaped gates (∼one-dimensional). The major drawback of using one-dimensional gate lines to define a zero-dimensional quantum dot is that device designs are essentially topologically limited to ring-like (i.e., two-row) geometries, whereas SLEDGE designs can be extended to highly customizable gate arrangements with additional BEOL levels as needed (see the Supporting Information).

The process flow to fabricate SLEDGE devices on Si/SiGe quantum well heterostructures is outlined in Figure 2A. The heterostructure ("epi wafer") consists of a tensile-strained Si quantum well epitaxially grown on a strain-relaxed $Si_{1-x}Ge_x$ (x = 0.25−0.35) buffer, followed by a SiGe capping layer of the same stoichiometry as the buffer. The beginning of the process flow includes optical lithography steps to pattern degenerately doped phosphorus-implanted Ohmics (NWELL) and argon-implanted electrically inactive regions (ISO). After defining implant regions, the gate dielectric (bilayer Al_2O_3/HfO_2) and gate metal (TiN) stack are blanket deposited, and gates are patterned in two steps. First, an optically defined coarse etch removes gate metal from a majority of the wafer, leaving a block of gate metal for each device from which all active gates will be subtractively patterned. Second, positive tone e-beam lithography is used to write gaps between gates, and a F-based dry-etch of gaps defines gates, as seen in the top-down SEM image of Figure 1B. The process flow then enters the BEOL

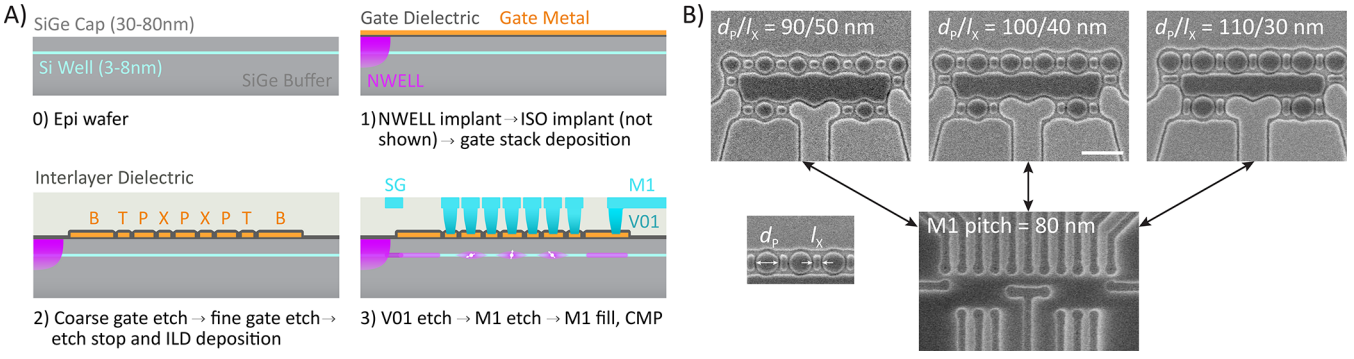

Figure 2. (A) Depiction of SLEDGE process flow, not to scale. Cross-section is an illustrative piecewise cut from an Ohmic, through bath gates, up T-gates, and across a triple-dot P-gate row. Steps are as described in text. "SG" in lower right panel is supply gate patterned at M1. (B) Top-down SEM images of three different devices patterned on the same wafer, each with varying P- and X-gate dimensions. The P-gate diameter (d_P) and X-gate length (l_X) parameters are defined in the lower left image with 10 nm gaps between gates. Because each device has the same P−P pitch and M−P distance, all use the same M1-level pattern as shown in the lower SEM image. All images are at the same scale, with 200 nm scale bar in center top image. Panel A courtesy of HRL Laboratories, LLC (graphic by John B. Carpenter). Copyright 2021.

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phase, wherein gates are contacted by vias (V01, connects M0 (gate) to M1) through an interlayer dielectric material (ILD, SiO_2), and spans (M1) connect vias to macroscopic routing at the bond pad level. A top-down SEM image after M1 patterning is shown in Figure 1C.

The gate stack consisting of bilayer Al_2O_3/HfO_2 gate dielectric and TiN gate metal optimizes process integration and device operation considerations. Experimentally, we have found that the bilayer gate dielectric combines a low defect density SiGe-Al_2O_3 interface with a high-k and etch-resistant HfO_2 layer, consistent with recent interface studies.[20] Each layer by itself does not have all three benefits. TiN gate metal is used because it has favorable etch selectivity to HfO_2 and because it has a London penetration depth potentially several orders of magnitude larger than that of Al previously used in lift-off gate devices.[21] This is expected to drastically reduce Meissner-induced paramagnetic gradients at low applied magnetic field.

The SLEDGE gate process is compatible with a variety of BEOL integration schemes due to its topographically flat design. Panels D and E of Figure 1 show cross-sectional TEM images along horizontal and vertical cuts from a TiN dual damascene process. (We have also demonstrated a subtractive BEOL process flow, as discussed in the Supporting Information.) Here, vias are patterned by e-beam lithography and etched into the ILD, stopping selectively on a HfO_2 etch stop dielectric layer deposited on top of the gates prior to ILD deposition. M1 spans are then patterned by e-beam lithography, and trenches are etched into the ILD. Following e-beam resist strip, a blanket etch completes the via etch down to gates through the etch stop layer. We fill V01 and M1 with an atomic layer deposition (ALD) TiN process, followed by chemical−mechanical polishing (CMP) to remove excess TiN and isolate M1 spans (Figure 1C). M1 is subsequently contacted by an optically defined metallization step to create wide (1−3 μm) routing lines and bond pads for wire-bonding to a chip carrier.

Using direct-write e-beam lithography with separate gate and BEOL contact layers allows for within-wafer flexibility in device design. In one reticle (∼10 mm × 10 mm), of which many are patterned across each wafer, we can fabricate devices with varying parameters to explore a broad design space including, but not limited to, gate pitch, P−M separation, relative P/X ratio, and M1 width. The gate, V01, and M1-level designs can be easily and independently modified in layout. Using appropriate proximity effect correction,[22] new designs are fractured and patterned in e-beam lithography without needing substantial development, if any, to optimize exposure or develop conditions. As an example, we show in Figure 2B SEM images of three different devices patterned in one reticle with varying P/X dimensions but fixed pitch and fixed V01/M1-level design. The P-gate diameter (d_P) and X-gate length (l_X) are varied from 90/50 nm to 110/30 nm, but the BEOL dimensions are unchanged between devices. This allows for examining relative P- and X-gate capacitances without confounding effects from differences in contact layers. The device design flexibility is additionally independent of the substrate heterostructure design, wherein Si well and SiGe cap can be modified in the epitaxial growth stage prior to fabrication. The ability to explore a broad parameter space is crucial for converging on the optimal device design for spin-based quantum information processing.

Flexibility of the SLEDGE process extends beyond gate-level device design. BEOL materials can be chosen separately from gate metal provided a sufficient Ohmic contact can be engineered. For example, a subtractive BEOL process can be used if sputtered metals (e.g., Nb or Pt) are desired, while dual damascene is conducive to materials deposited by chemical vapor deposition or ALD (e.g., W or TiN). Moreover, the BEOL span fanout can be readily designed to allow space for additional active features in arbitrary locations around the device, such as a micromagnet or a superconducting resonator,[4,23] again independent of the gate-level design. A schematic of additional post-BEOL device features as well as a discussion of BEOL scaling limitations can be found in the Supporting Information.

The requirements for e-beam overlay between V01-gate and M1-V01 layers are approximately 5−15 nm, set by gate pitch and minimum gate dimension. While nontrivial, we readily achieve the alignment requirements within-wafer and across lots with a noncustomized, commercially available Raith EBPG5200 e-beam writer. In the Supporting Information, we show that the mean misalignment magnitude across four representative lots (with four wafers per lot) is $\lesssim$5 nm for both V01-gate and M1-V01 levels. We use the tool with four 3-in. wafers (i.e., one lot) mounted onto a 200 mm wafer holder, and therefore the overlay we achieve represents a 200 mm wafer capability for e-beam lithography. We show also that the mean P-gate critical dimension (CD) in lithography varies <7% between the same four lots. Overall, this demonstrates that e-beam lithography is well-capable of wafer-level Si qubit fabrication. Note that although e-beam lithography is conventionally slower than optical lithography, the overall process time for the three SLEDGE e-beam levels (gate, V01, M1) is still a relatively small fraction (∼10%) of the overall process flow. This fraction is expected to remain approximately constant for different device designs.

In addition to device design flexibility, the SLEDGE process flow enables aggressive SiGe surface cleaning prior to gate dielectric deposition. With overlapping gate technologies,[7,24] the screening gate (also known as confinement gate) and underlying gate dielectric, which are commonly Al-based, preclude most wet surface cleans prior to plunger gate dielectric deposition. Similar restrictions exist for exchange gate dielectric deposition. This can lead to substantial interface defect densities and associated electrostatic non-uniformity. Pd gates are more etch-resistant than Al[25] but still may be roughened or delaminated in common HCl- or piranha-based (H_2SO_4:H_2O_2:H_2O) cleaning chemistries. In the SLEDGE process with simultaneously patterned uniplanar gates, there is only one dielectric layer for all gates, and the semiconductor surface is free of metal and dielectric materials prior to dielectric deposition. Therefore, wet etchants for trace metal, oxide, and carbon contamination, such as SC1 (NH_4OH:H_2O_2:H_2O), SC2 (HCl:H_2O_2:H_2O), HF, and piranha, can be used given ratios are chosen to have reasonable selectivity to SiGe.

The improvement in electrostatic uniformity with appropriate surface cleaning can be demonstrated from characteristics of gated Hall bars (HB) fabricated on-wafer alongside quantum dot devices. On our device wafers, gates for HBs (∼400 μm × 20 μm) are fabricated as process control monitors at each planar metallization step (e.g., gate, M1, bond), and Hall parameters are measured to characterize the epitaxial material and device dielectric layers. Such HBs serve

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to quickly quantify intra- and interwafer gate/semiconductor uniformity due to relative ease of fabrication and measurement interpretation. We use low carrier density HB properties to quantify potential disorder,[26] which influences charge manipulation at the dot level. In two-dimensional electron systems, potential disorder on relevant length scales can be characterized by the density at which there is a crossover from metallic to insulating behavior. The crossover density has various potential mechanisms, for example strong localization or that of classical percolation theory, both of which have several measurement methods.[27] In our Hall measurements, we characterize disorder instead using the sheet density at which the Hall mobility extrapolates to 0 in a linear mobility−density plot, which we denote as n_{min}. To extract n_{min}, we perform a line fit using only data in the low-density regime ($n \leqslant 4 \times 10^{10}$ cm^{-2}). While not necessarily physical (negative values are possible),[28] the advantage of n_{min} is that extrapolation is relatively straightforward, in contrast to the percolation density or metal−insulator transition density. The latter may involve temperature sweeps and/or fitting many data points to some functional form, which can be difficult for imperfect gate or epitaxial structures. In addition, we have found in our HBs that n_{min} typically scales similarly as the percolation and metal−insulator transition densities.

In Figure 3A, we plot n_{min} distributions for lift-off plunger gates (from our overlapping gate technology prior to SLEDGE), SLEDGE gates with unoptimized surface cleaning, and SLEDGE gates with optimized surface cleaning. For all categories, only data from wafers with 60 nm SiGe cap thickness are plotted, to control for gate capacitance. Our prior overlapping gate technology uses a similar bilayer Al_2O_3/HfO_2 dielectric stack as in SLEDGE, and the devices are similar to those reported elsewhere.[7,29] From lift-off gates to unoptimized SLEDGE gates, mean n_{min} is reduced from 4.5×10^{10} to 2.6×10^{10} cm^{-2}. There is a further reduction in mean n_{min} with optimized SLEDGE gates to 1.4×10^{10} cm^{-2}. The means are statistically different with >99% confidence. The data imply a reduction in disorder by switching from overlapping or multiplanar gates, which have several dielectric depositions before gate patterning and limited pregate clean options, to uniplanar gates, which allow for more aggressive predeposition wet cleans.

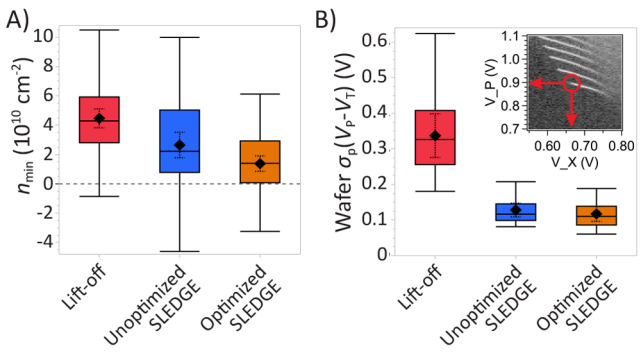

Figure 3. (A) Gated Hall bar measurements of n_{min} for various gate types. Quartile box plots, means (diamonds), and 99% confidence intervals (dashed whiskers) are shown. Mean n_{min} exhibits a statistically significant decrease from lift-off gates to unoptimized SLEDGE gates to optimized SLEDGE gates. (B) Per-wafer pooled standard deviations of P- and X-/T-gate voltage differences at first electron loading line in single dot charge stability diagram (inset), measured at 1.6 K. Quartile box plots, means, and 99% confidence intervals are shown. There is a statistically significant decrease in mean from lift-off gates to SLEDGE gates, unoptimized or optimized.

We can further quantify potential disorder at the device level by analyzing single-dot charge stability diagrams across wafers. One metric is to use the differential voltage between P- and neighboring T- or X-gates ($V_P - V_T$) at the first electron loading line, as shown in the inset of Figure 3B. We have found that the differential voltage scales exponentially with SiGe cap thickness as expected from solving Laplace's equation for a pinned surface gate potential model.[30] This indicates that (1) across devices, the quantum well is tuned to approximately the same potential at the one-electron loading line and (2) variations in the voltage difference to load one electron are due to potential disorder. Note that the data acquisition time scale has minimal effect on V_T because of the exponential dependence of electron tunneling rate on barrier voltage.[31] For each wafer, we find the standard deviation (pooled by device) of all ($V_P - V_T$) differential biases from the wafer, which we use as a metric for disorder. In Figure 3B, we plot distributions of the pooled standard deviations (σ_p) for lift-off gates, SLEDGE gates with unoptimized preclean, and SLEDGE gates with optimized preclean. As with Figure 3A, only 60 nm SiGe cap wafers are compared to control for gate capacitance. We observe a statistically significant reduction (>99% confidence) in mean σ_p from lift-off gates to unoptimized SLEDGE gates of 0.34 to 0.13 V. The mean for optimized SLEDGE gates is 0.12 V, but it is not statistically different from that of unoptimized SLEDGE gates at the same confidence level, perhaps because of residual disorder in the gate stack itself. The reduction in σ_p indicates that, on a SLEDGE wafer, the voltage difference $V_P - V_T$, and therefore the electrostatic potential landscape, is more consistent across devices than on a lift-off gate wafer. Moreover, the mean SLEDGE σ_p values compare favorably to corresponding addition voltages (~40 mV; see Figure 3B inset). While the HB and charge stability diagram data both show a clear reduction in wafer-level disorder with SLEDGE devices, the effect is likely larger for quantum dots because they are more susceptible to local disorder than large-area HBs.

Beyond the advantages in device design flexibility and disorder with the SLEDGE process, the technology also readily produces qubit devices capable of spin coherent operations. A representative set of charge stability diagrams from a six-dot SLEDGE device recorded at 1.6 K is shown in Figure 4A, with one diagram for each adjacent plunger gate pair. Each diagram exhibits the canonical double-dot honeycomb pattern with cells merging at higher electron occupancy due to tunnel barrier lowering.[31] Loading voltages for the most relevant (0,1), (1,0), and (1,1) charge configurations are all ≤1 V, and with the exception of the outer dots, which experience enhanced cross-capacitance from the OFG, all loading voltages are similar to each other. This is a critical feature for proposed multiplexed cryogenic control.[32]

Representative plots from each X-gate showing exchange (J) fringes as a function of neighboring P−P detuning (Δ, ordinate) and exchange gate voltage (V_X, abscissa) are shown in Figure 4B. In these so-called "fingerprint" plots,[29] which were measured at dilution refrigerator (DF) temperatures from the same device as in Figure 4A, the exchange frequency between interdot electrons increases with both tunnel coupling (controlled by V_X) and Δ. Fingerprint plots are used to determine the symmetric axis (vector in $\Delta - V_X$ voltage space

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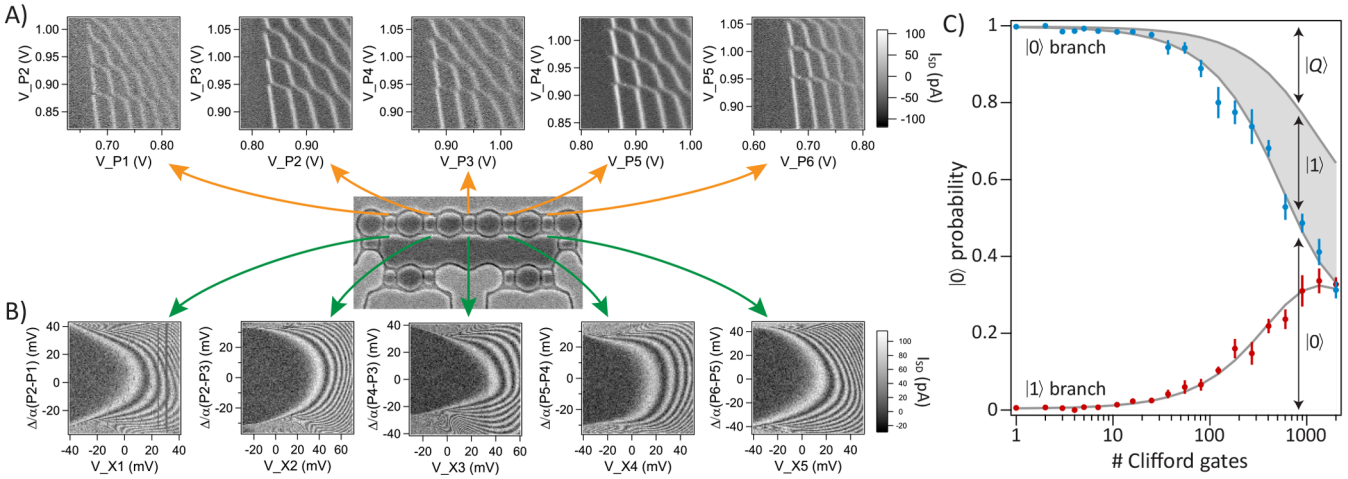

Figure 4. (A) Charge stability diagrams measured at 1.6 K from each double-dot pair of a representative six-dot SLEDGE device. (B) Exchange oscillation fringes measured in a DF (nominally at 50 mK) for each double-dot pair as a function of corresponding P−P detuning and X-gate voltage ("fingerprint" plots). Fingerprints were measured from the same device as in panel A. (C) Single-qubit blind randomized benchmarking from a SLEDGE device. The $|0\rangle$ branch (blue points) and $|1\rangle$ branch (red points) are used to extract per-Clifford error and leakage rates. The arrows show estimated populations in states $|0\rangle$, $|1\rangle$ (shaded region) and leaked states $|Q\rangle$.

where $\frac{dJ}{d\Delta} \sim 0$) for reduced sensitivity to charge noise, and they indicate that a given double-dot pair exhibits spin coherent exchange oscillations. Furthermore, single-qubit blind randomized benchmarking (RB) data from an exchange-only encoded three-dot SLEDGE device is shown in Figure 4C. In the blind RB sequence, the qubit is initialized in the spin singlet ($|0\rangle$), a sequence of N gates randomly selected from the Clifford group is applied, and a recovery Clifford returns the qubit ideally to the spin singlet or spin triplet ($|1\rangle$).[5] The sum and difference of the $|0\rangle$ and $|1\rangle$ return probabilities as a function of N can be fit to exponential forms to extract per-Clifford error and leakage rates. For this particular device, we find per-Clifford error from the right-most triple dot of 0.12 ± 0.01% and leakage of 0.035 ± 0.011%. Other operable triple dots in the device displayed similar RB error, and mechanisms of error variability are expected to be discussed in future work. The SLEDGE qubit fidelity measured here is slightly improved with respect to our previous demonstration with lift-off gate devices.[5] In both cases, errors are consistent with process-independent limitations from nuclear spin hyperfine dephasing and unintentional voltage pulse overlap control errors.

In conclusion, we have demonstrated a flexible fabrication process for Si/SiGe exchange-only qubits wherein uniplanar dot-shaped gates and routing are defined on separate planes and are contacted with interconnect vias. The separation, in combination with electron-beam lithography, enables high customizability in materials and device designs, particularly toward nonconventional layouts. SLEDGE qubit devices have low electrostatic disorder compared to overlapping gate devices fabricated with lift-off metallization processes. Future work includes improved rf engineering of M1 and optical layer routing, as well as integration of micromagnets and superconducting resonators.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c03026.

Figures and discussion of SLEDGE design extensions, SLEDGE exchange energy, e-beam lithography repeatability, SLEDGE M-to-P tunability, and subtractive BEOL and parasitic metal dots (PDF)

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Notes

The authors declare no competing financial interest.

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