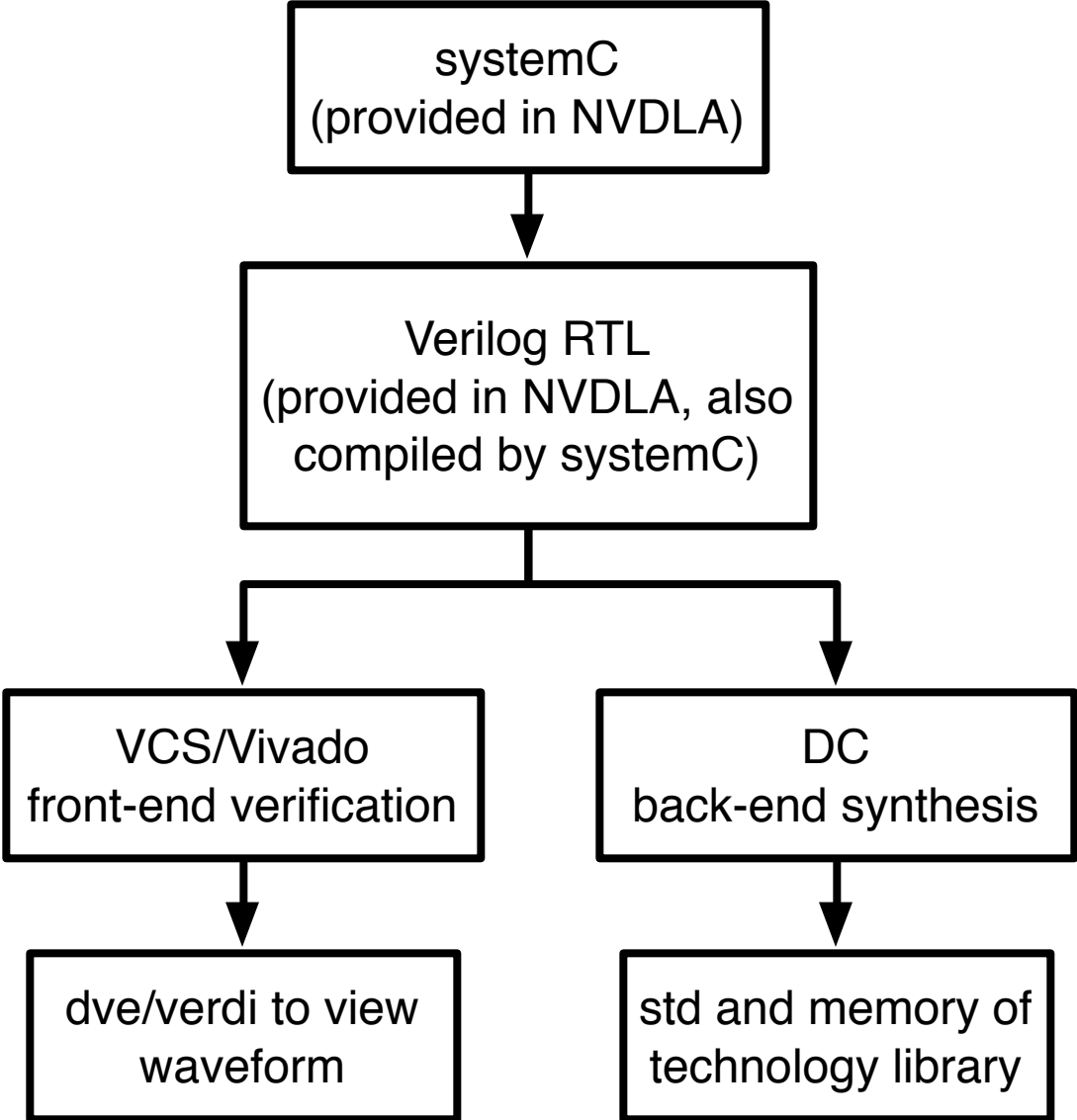


systemC
(provided in NVDLA)



```
graph TD; A["systemC  
(provided in NVDLA)"] --> B["Verilog RTL  
(provided in NVDLA, also  
compiled by systemC)"]; B --> C["VCS/Vivado  
front-end verification"]; B --> D["DC  
back-end synthesis"]; C --> E["dve/verdi to view  
waveform"]; D --> F["std and memory of  
technology library"];
```

The diagram is a flowchart showing the compilation and verification process for NVDLA. It starts with a box for 'systemC (provided in NVDLA)', which points down to a box for 'Verilog RTL (provided in NVDLA, also compiled by systemC)'. From this central box, the flow splits into two parallel paths. The left path goes through 'VCS/Vivado front-end verification' to 'dve/verdi to view waveform'. The right path goes through 'DC back-end synthesis' to 'std and memory of technology library'. All boxes are rectangular with black borders and black text, connected by black arrows.

Verilog RTL
(provided in NVDLA, also
compiled by systemC)

VCS/Vivado
front-end verification

dve/verdi to view
waveform

DC
back-end synthesis

std and memory of
technology library