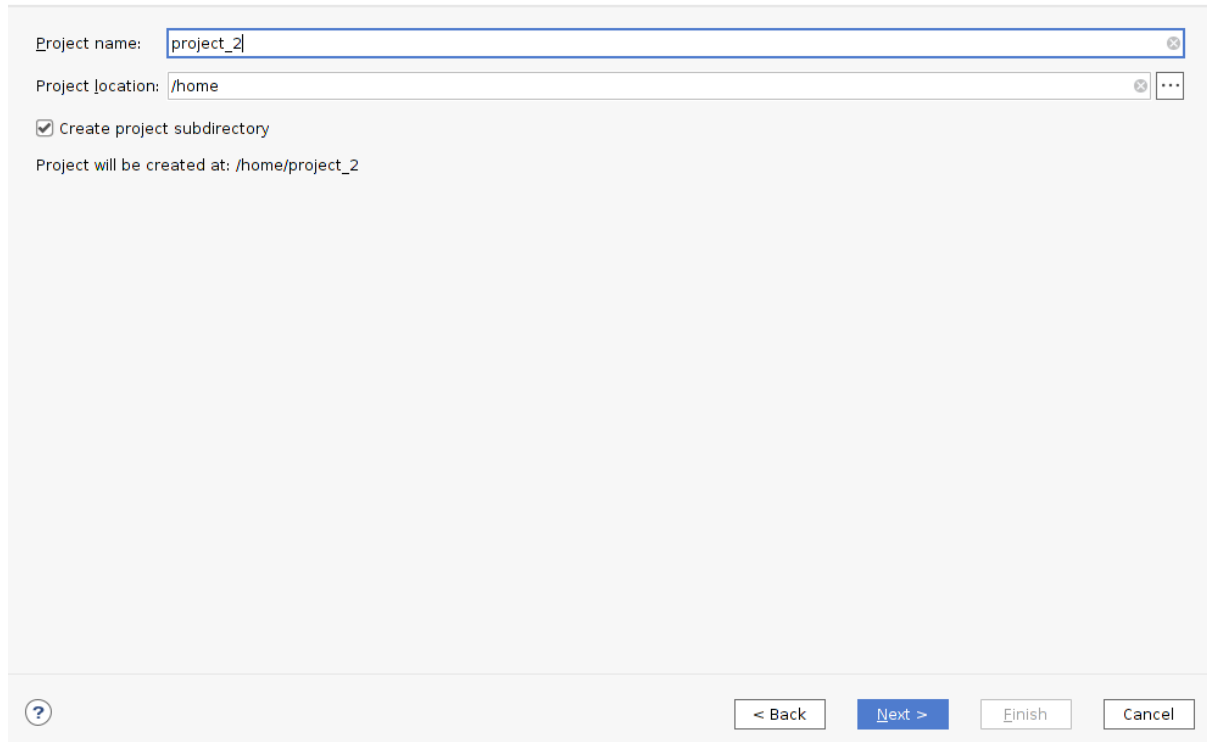


# Creating Project in Xilinx

1. In the Vivado launcher, create a new project **outside of your github folder**, select "RTL project".

## Project Name

Enter a name for your project and specify a directory where the project data files will be stored.



The screenshot shows the 'Project Name' dialog box in Vivado. It has a light gray background. At the top, there's a title bar with a question mark icon on the left and a close button on the right. Below the title bar, the text 'Project Name' is followed by the instruction 'Enter a name for your project and specify a directory where the project data files will be stored.' There are two input fields: 'Project name:' with the text 'project\_2' and 'Project location:' with the text '/home'. The 'Project location' field has a browse button (three dots) to its right. Below these fields, there is a checkbox labeled 'Create project subdirectory' which is checked. Underneath the checkbox, it says 'Project will be created at: /home/project\_2'. At the bottom of the dialog, there are four buttons: '< Back' (disabled), 'Next >' (active/highlighted in blue), 'Finish' (disabled), and 'Cancel' (disabled). A small question mark icon is also present in the bottom left corner of the dialog area.

Project name: project\_2

Project location: /home

☒ Create project subdirectory

Project will be created at: /home/project\_2

< Back Next > Finish Cancel

New Project

Project Type

Specify the type of project to create.

☒RTL Project

You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform

☐ Post-synthesis Project

You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ I/O Planning Project

Do not specify design sources. You will be able to view part/package resources.

☐ Imported Project

Create a Vivado project from a Synplify, XST or ISE Project File.

☐ Example Project

Create a new Vivado project from a predefined template.

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< Back

Next >

Finish

Cancel

2. Add all ".v" files in the "lab2/src/" folder as "design sources", add all ".v" files in the "lab2/sim/" folder as "simulation sources", and add the ".xdc" file in the "lab2/src/" folder as "constraints".

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

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	Index	Name	Library	HDL Source For	Location
	1	adder_tester.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	2	behavioral_adder.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	3	counter.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	4	full_adder.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	5	structural_adder.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	6	z1top.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/src
	7	adder_testbench.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/sim
	8	counter_testbench.v	xil_defaultlib	Synthesis & Simulation	/home/yourifpga_labs_sp22/lab2/sim

Add Files

Add Directories

Create File

☐ Scan and add RTL include files into project
 ☐ Copy sources into project
 ☒ Add sources from subdirectories

Target language: Verilog

Simulator language: Mixed

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< Back

Next >

Finish

Cancel

New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

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Constraint File	Location
z1top.xdc	/home/yourifpga_labs_sp22/lab2/src

Add Files

Create File

☐ Copy constraints files into project

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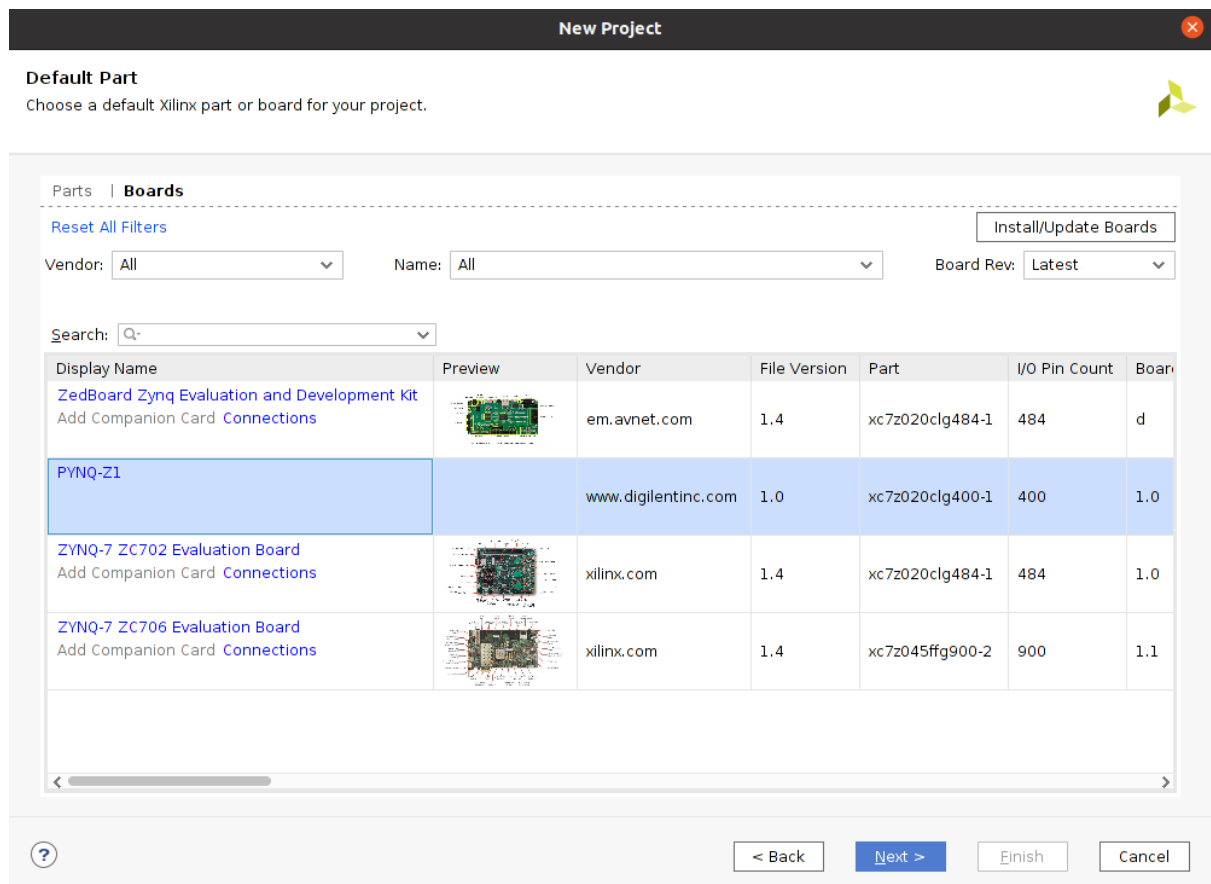
< Back

Next >

Finish

Cancel

3. Select the pynq-z1 board. **Make sure you have Pynq-z1 board support.**



4. If you don't have pynq-z1 board support, you could download:  
[https://github.com/cathalmccabe/pynq-z1\\_board\\_files](https://github.com/cathalmccabe/pynq-z1_board_files) , then you can paste this pynq\_z1 folder to /tools/Xilinx/Vivado/2020.2/data/boards/board\_files

```
youri@youri-400TDA-4005DA: /tools/Xilinx/Vivado/2020.2/data/boards/board_files$ ls  
lls1mx274-mip1  pynq-z1  xc7z02  xc7z06  zed
```

<https://s3-us-west-2.amazonaws.com/secure.notion-static.com/c3ab40c1-b4f4-420d-a95e-b072dc3404fb/Untitled.zip>

5. run `export PATH=/opt/xilinx/Vivado/2019.1/bin:$PATH`

- Reference

[https://github.com/EECS150/fpga\\_labs\\_sp22/blob/master/lab1/spec/spec.md](https://github.com/EECS150/fpga_labs_sp22/blob/master/lab1/spec/spec.md)