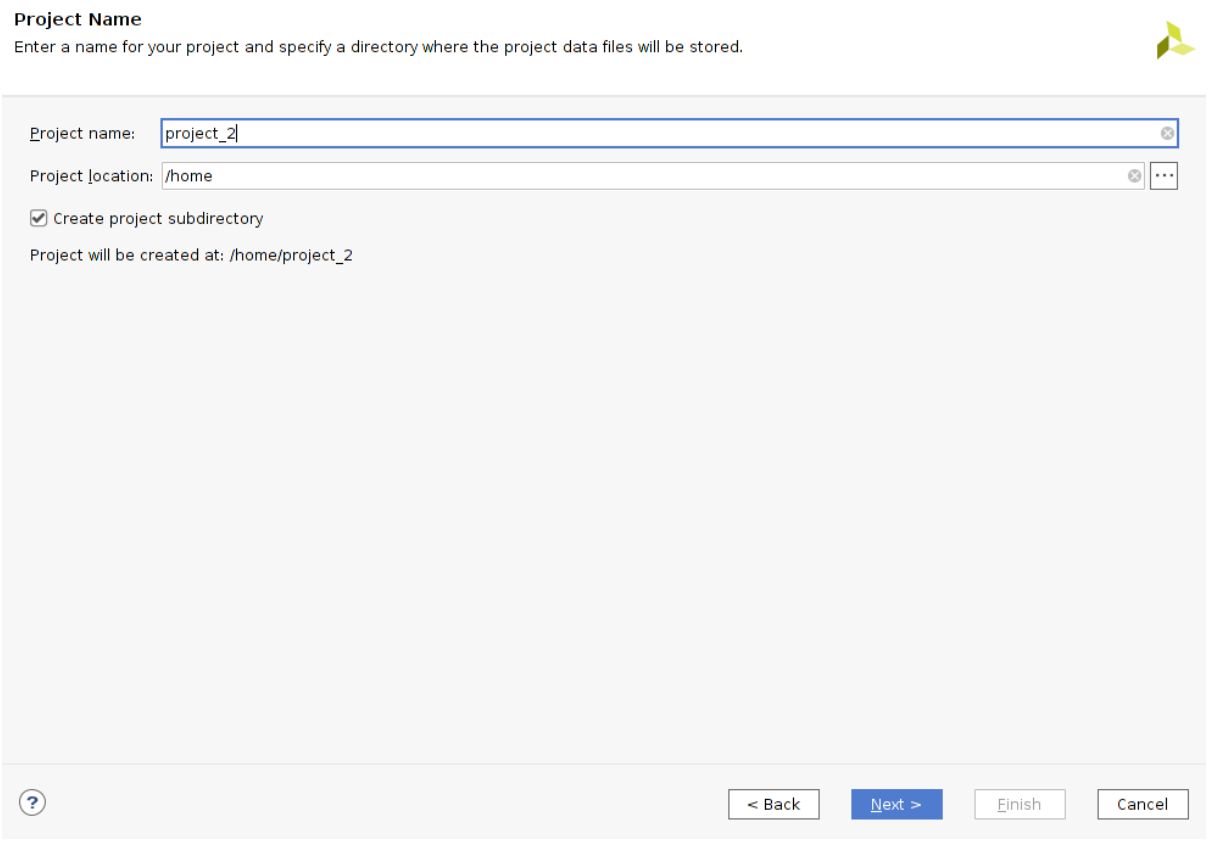
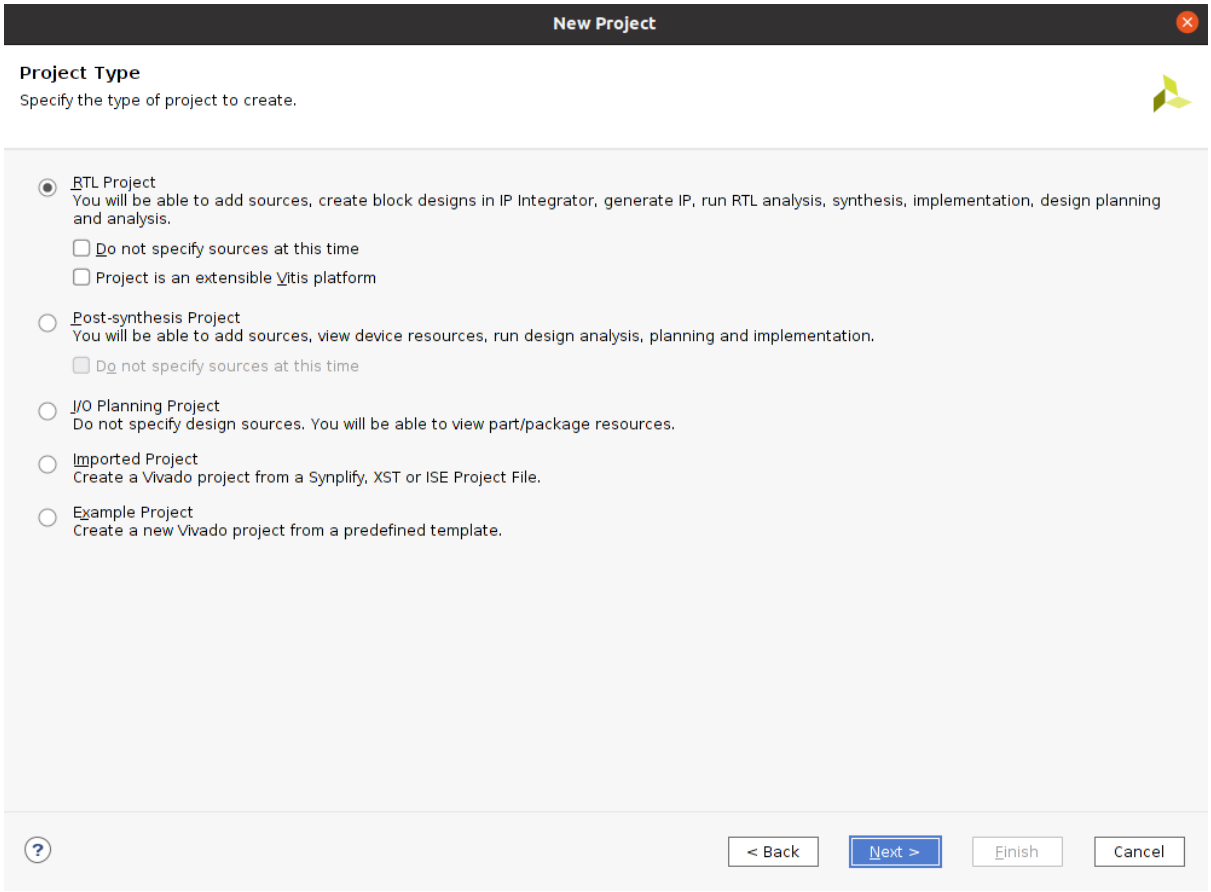
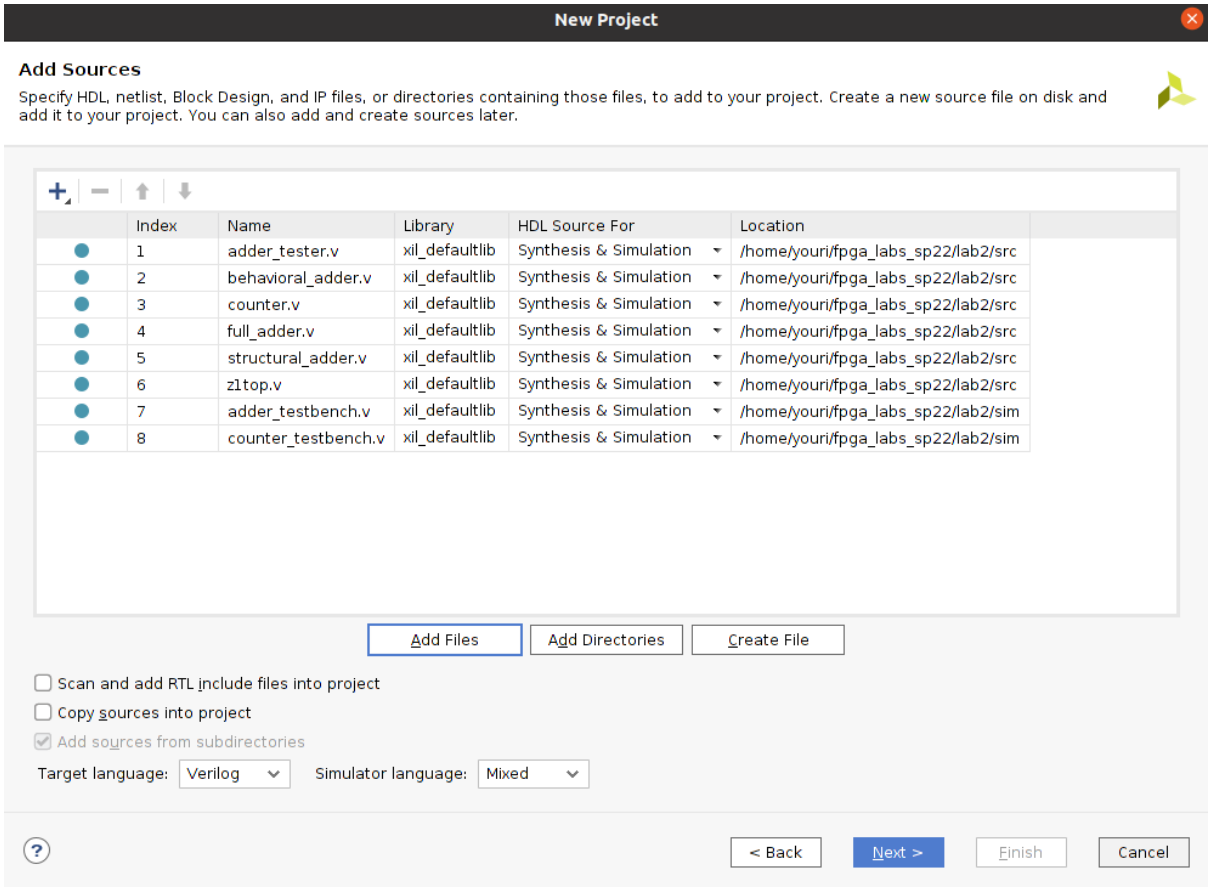
Creating Project in Xilinx

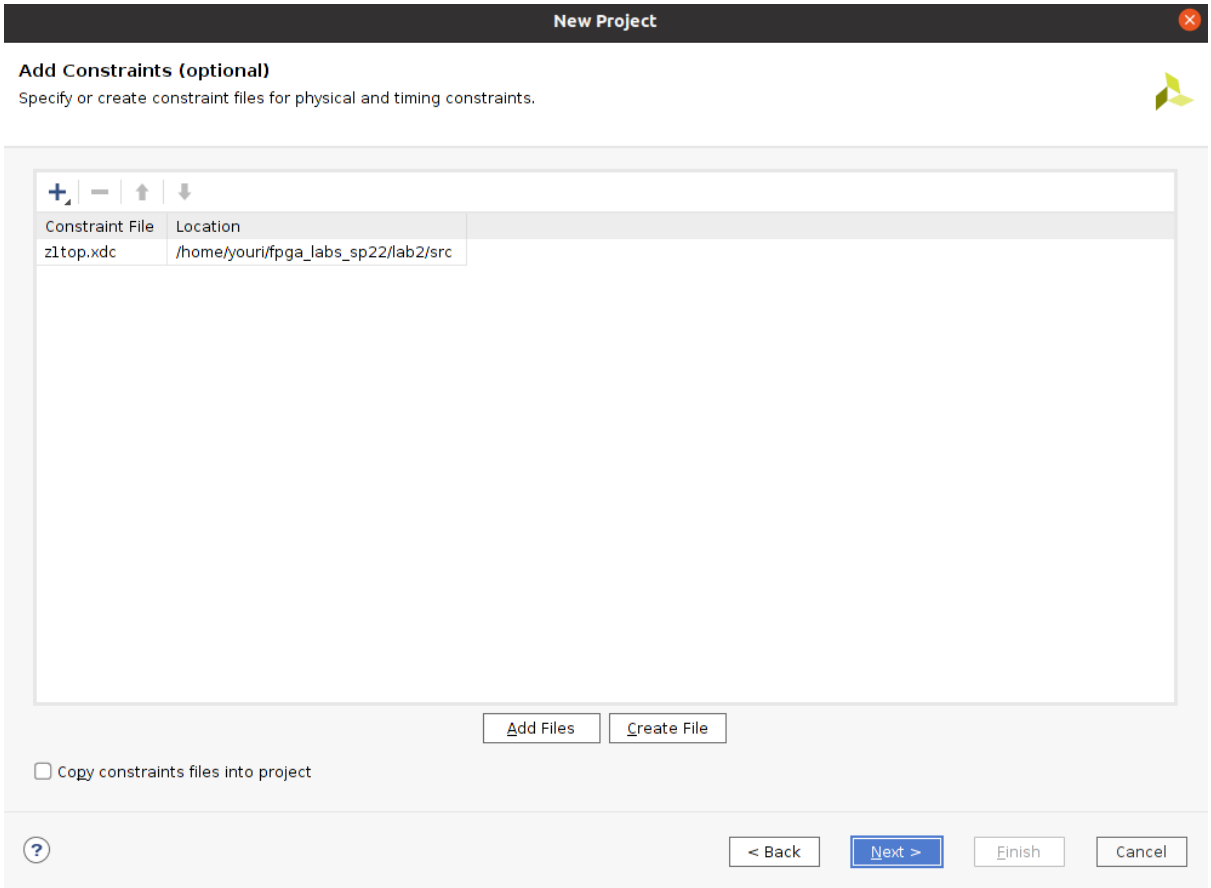
1. In the Vivado launcher, create a new project **outside of your github folder**, select "RTL project".



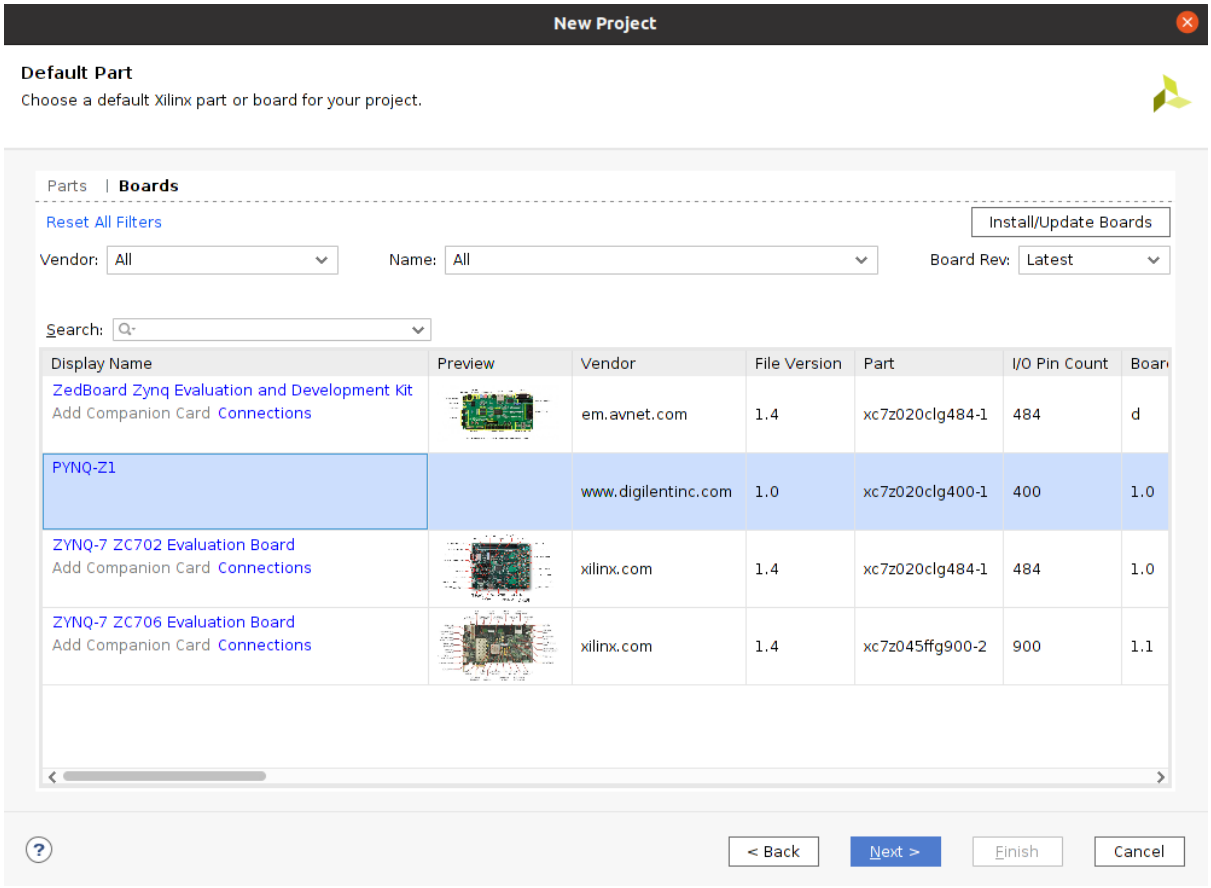


2. Add all ".v" files in the "lab2/src/" folder as "design sources", add all ".v" files in the "lab2/sim/" folder as "simulation sources", and add the ".xdc" file in the "lab2/src/" folder as "constraints".


New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1 adder_tester.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
2 behavioral_adder.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
3 counter.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
4 full_adder.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
5 structural_adder.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
6 z1top.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/src
7 adder_testbench.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/sim
8 counter_testbench.v xil_defaultlib Synthesis & Simulation /home/youri/fpga_labs_sp22/lab2/sim
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: Verilog
Simulator language: Mixed
< Back
Next >
Finish
Cancel


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Constraint File
Location
z1top.xdc /home/youri/fpga_labs_sp22/lab2/src
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

3. Select the pynq-z1 board. **Make sure you have Pynq-z1 board support.**



4. If you don't have pynq-z1 board support, you could download: https://github.com/cathalmccabe/pynq-z1_board_files , then you can paste this pynq_z1 folder to /tools/Xilinx/Vivado/2020.2/data/boards/board_files

https://s3-us-west-2.amazonaws.com/secure.notion-static.com/c3ab40c1-b4f4-420d-a95e-b072dc3404fb/Untitled.zip

5. run `export PATH=/opt/xilinx/Vivado/2019.1/bin:$PATH`

- Reference

  https://github.com/EECS150/fpga_labs_sp22/blob/master/lab1/spec/spec.md