P-N Junction

Diodes [2 Hours]

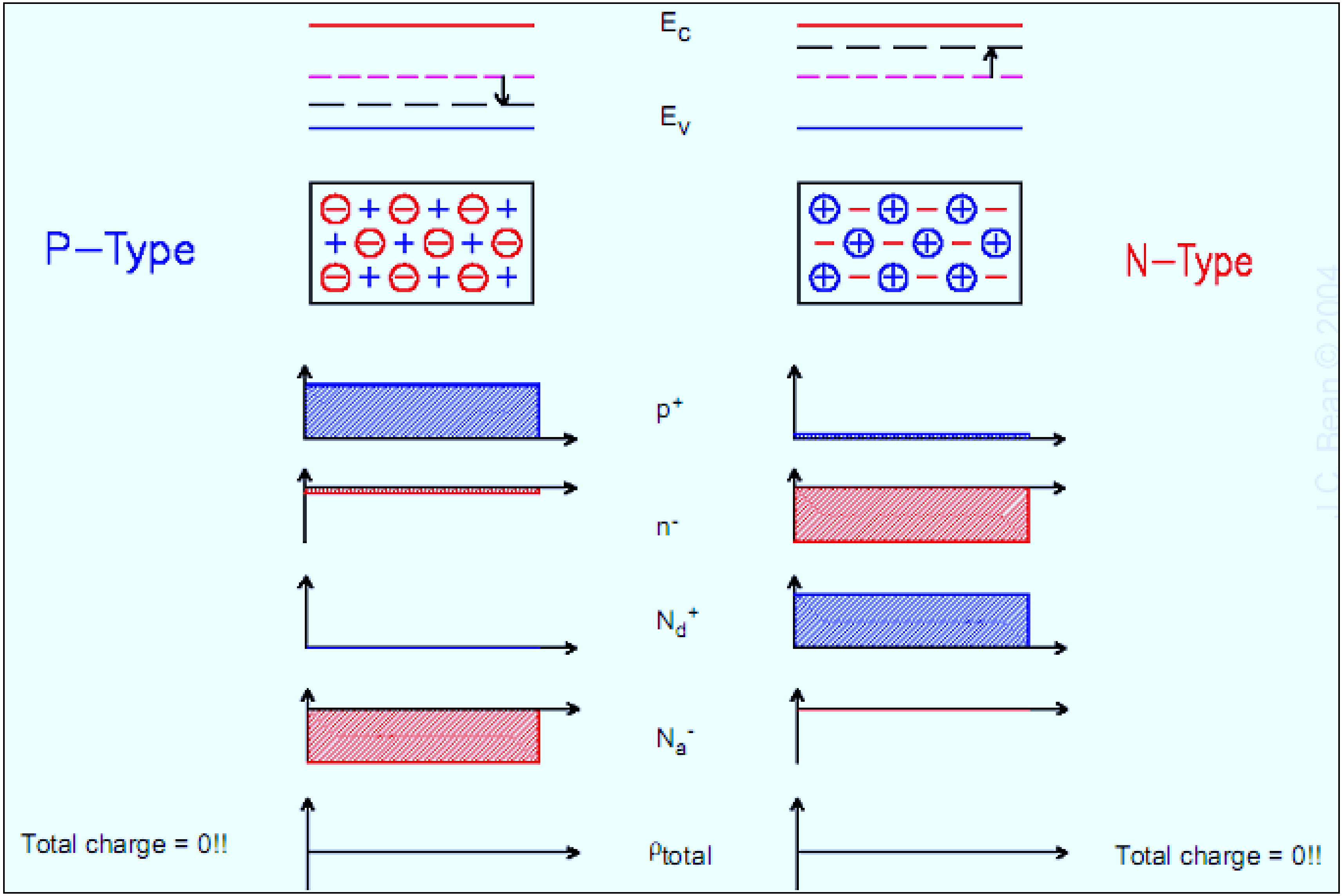
2.1. Construction

2.2. Unbiased diode; Depletion layer and Barrier potential; junction capacitance (expression only)

2.3. Principle of operation with forward biasing and reverse biasing

2.4. Characteristics

2.5 Diode's three models/equivalent circuits



E_c
E_v
P–Type
N–Type
p^+
n^-
N_d^+
N_a^-
ρ_{total}
Total charge = 0!!
Total charge = 0!!
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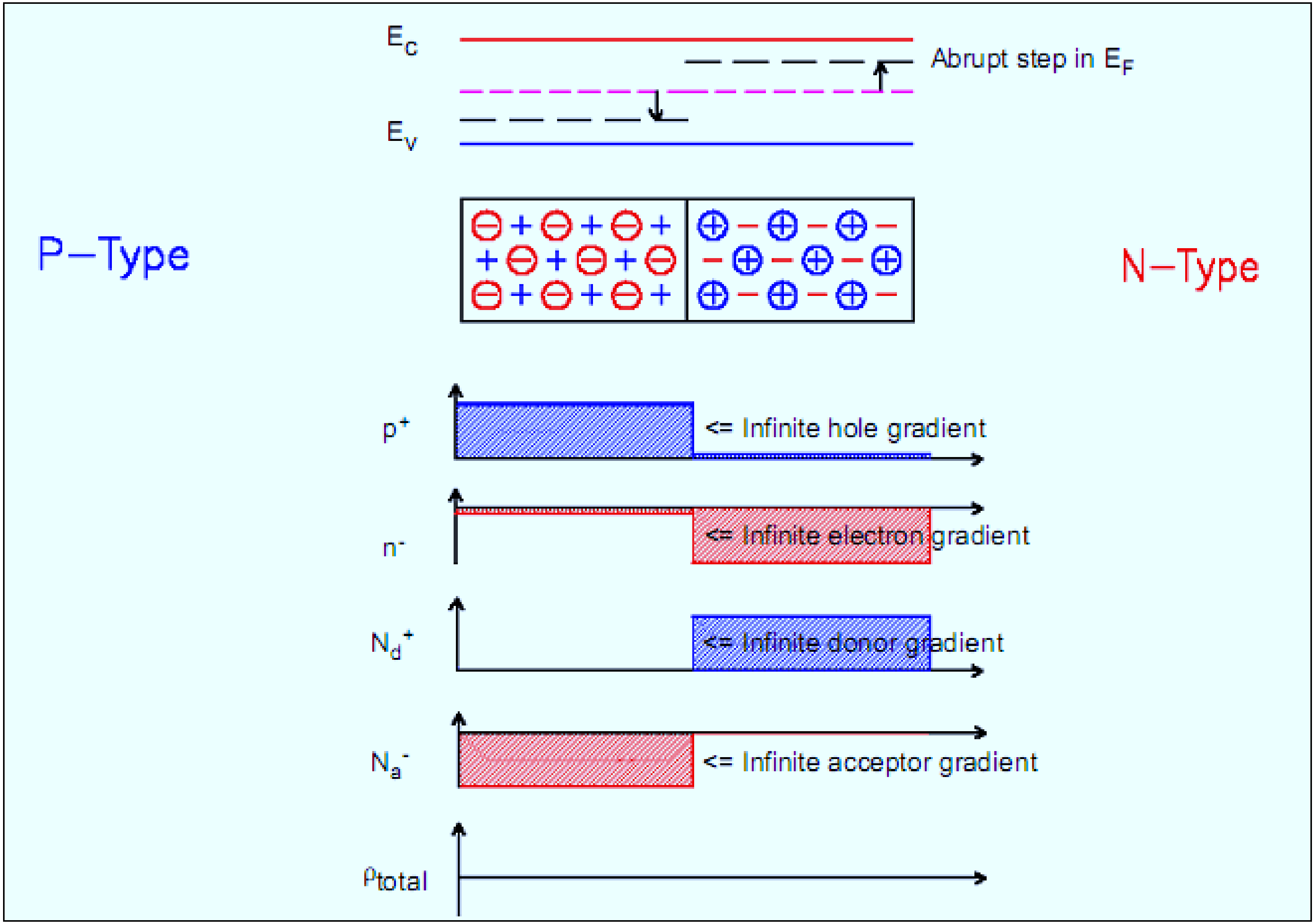
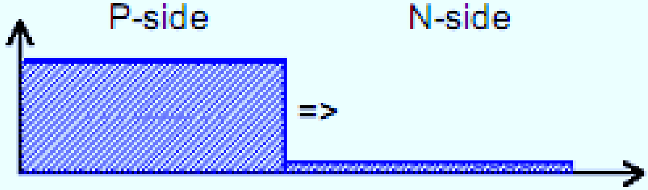
P-N Junction ***without*** Bias



P-N Junction ***without*** Bias

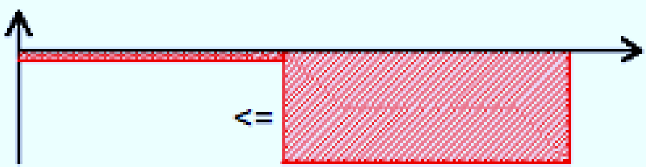
Hole gradient:



$$J_{diffusion\_p} = -q \cdot D_p \cdot \frac{d}{dx} p$$ => huge hole diffusion to right!

Holes entering N-type side find MANY electrons to recombine with

Electron gradient:

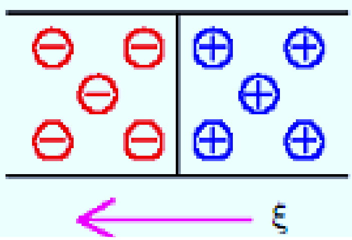


$$J_{diffusion\_n} = q \cdot D_n \cdot \frac{d}{dx} n$$ => huge electron diffusion to left!!

Electrons entering P-type side find MANY holes to recombine with

However: Holes leave behind negative acceptor ions! Electrons leave behind positive donor ions!

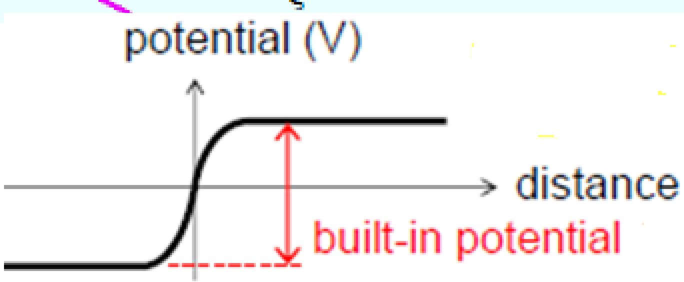
P-side w/o holes



N-side w/o electrons

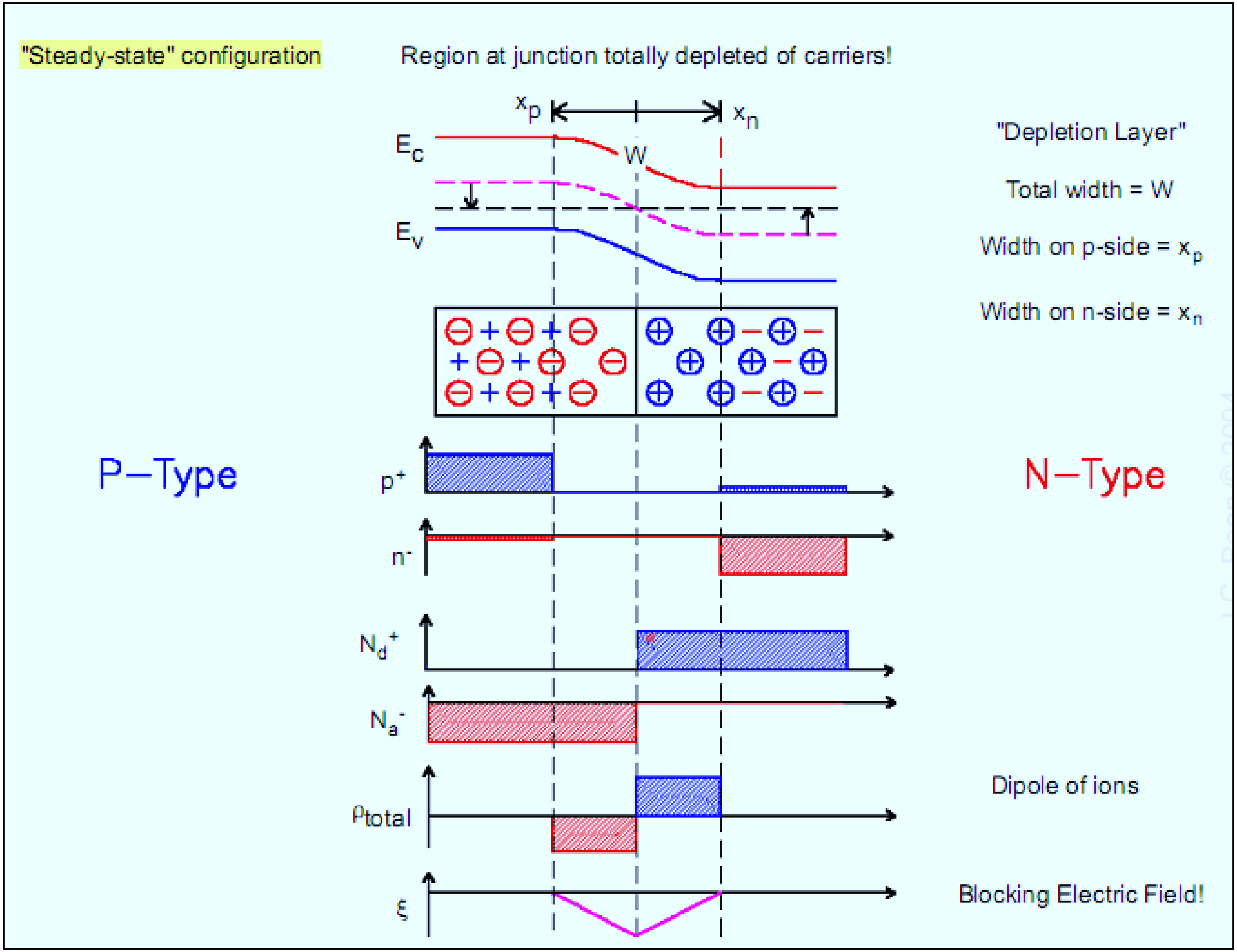
Dipole of ions builds up electric field

Eventually stops further carrier crossing



$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right)$$

P-N Junction *without* Bias



P-N Junction *without* Bias

$$W = \sqrt{\frac{2\varepsilon \cdot V_{bi}}{q} \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \quad = \text{Total "Depletion Width"}$$

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_a \cdot N_d}{n_i^{2}}\right)$$

Depletion width almost totally determined by more lightly doped side:

$N_a << N_d$:

$$W = \sqrt{\frac{2\varepsilon \cdot V_{bi}}{q} \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = \sqrt{\frac{2\varepsilon \cdot V_{bi}}{q} \cdot \frac{1}{N_a}}$$

$N_a >> N_d$:

$$W = \sqrt{\frac{2\varepsilon \cdot V_{bi}}{q} \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = \sqrt{\frac{2\varepsilon \cdot V_{bi}}{q} \cdot \frac{1}{N_d}}$$

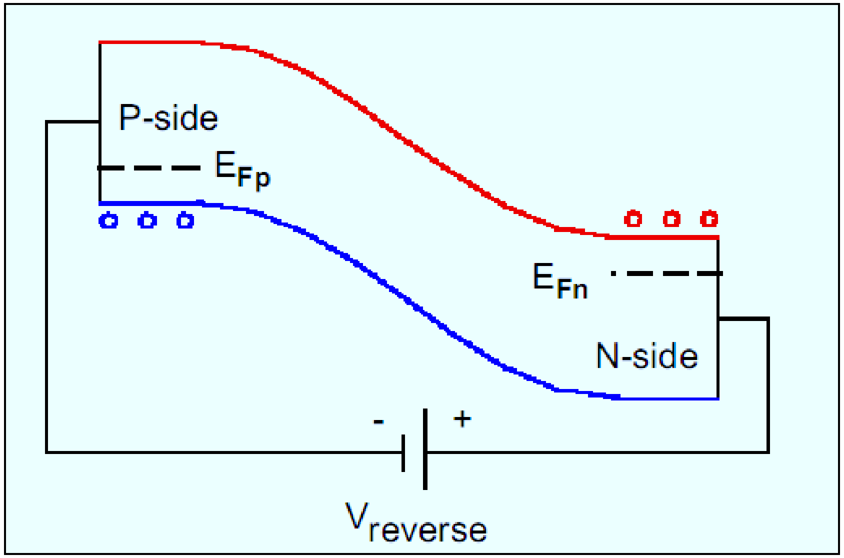
$$W = \sqrt{\frac{2 \cdot \varepsilon \cdot V_{bi}}{q} \cdot \frac{1}{\text{Doping\_on\_lighter\_side}}}$$

P-N Junction *with* Bias

1) Apply "Reverse Voltage" **Reversed in the sense: + Applied to N-side**
- Applied to P-side

Remember that Voltage = Potential Energy per positive charge = opposite of our electron bands

So positive voltage pulls DOWN electron energy



$$W = \sqrt{\frac{2\varepsilon \cdot (V_{bi} + V_{reverse})}{q} \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = \text{Total "Depletion Width"}$$

P-N Junction *with* Bias

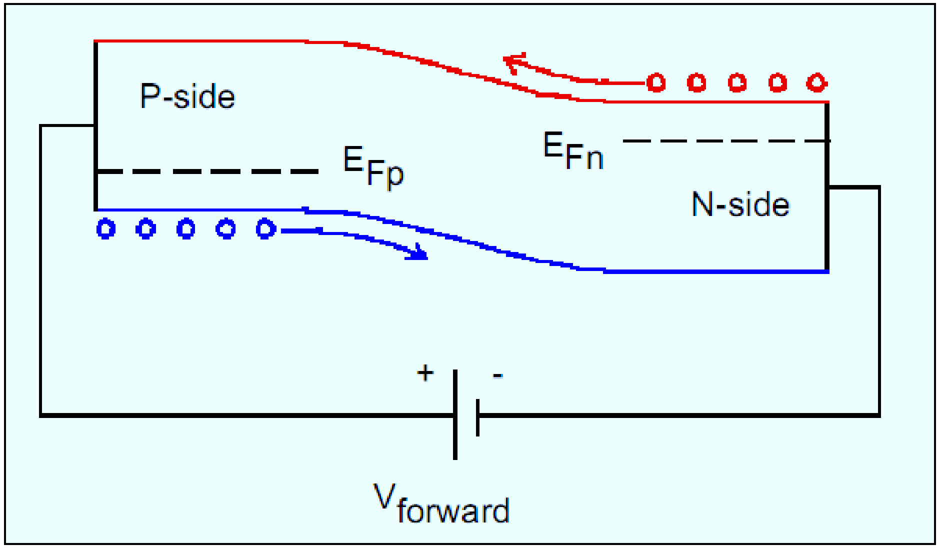
2) Apply Forward Voltage: **Forward in the sense:** **+ Applied to P-side**
- Applied to N-side

Effect is opposite of that described above:

$V_{forward}$ subtracts for built-in barrier V_{bi}

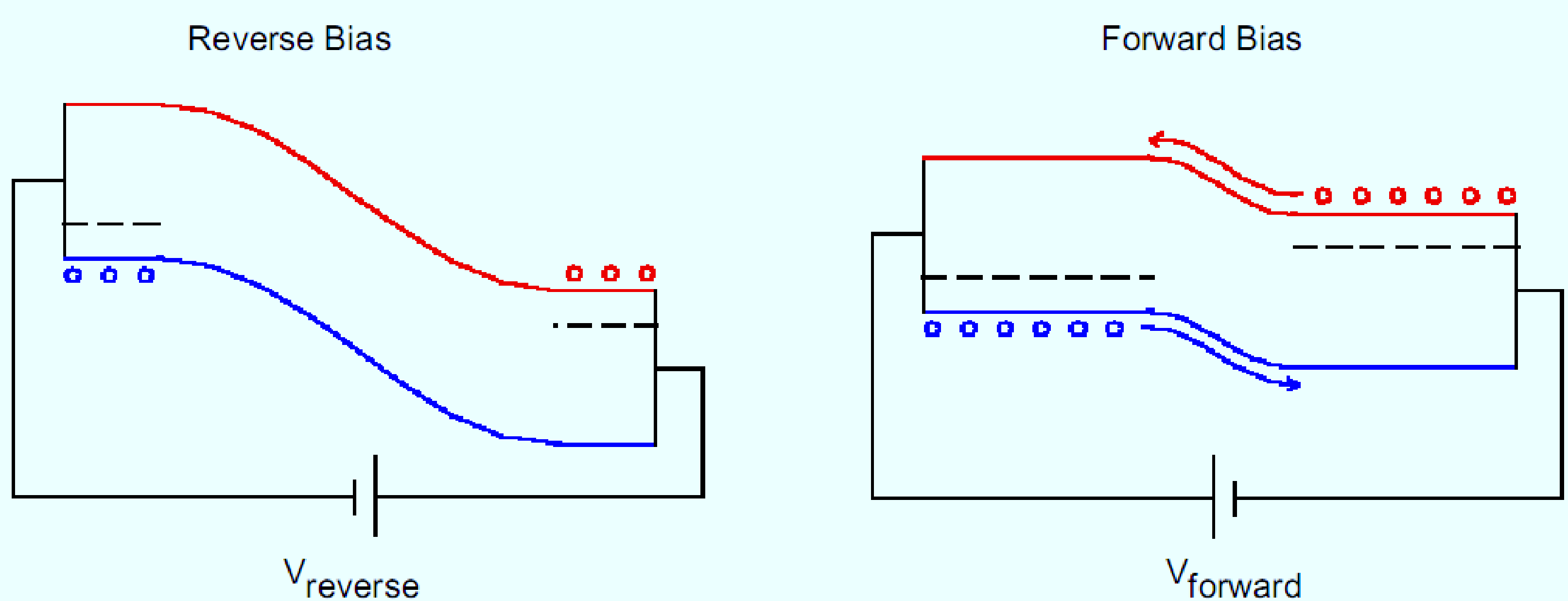
Enhances chance of additional carriers crossing junction

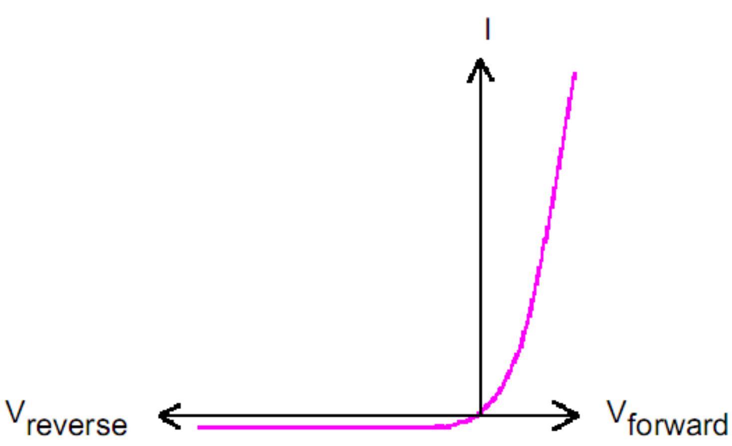
Possibility of steady-state current flow



P-N Junction *with* Bias

We have just defined the two states of a semiconductor DIODE:



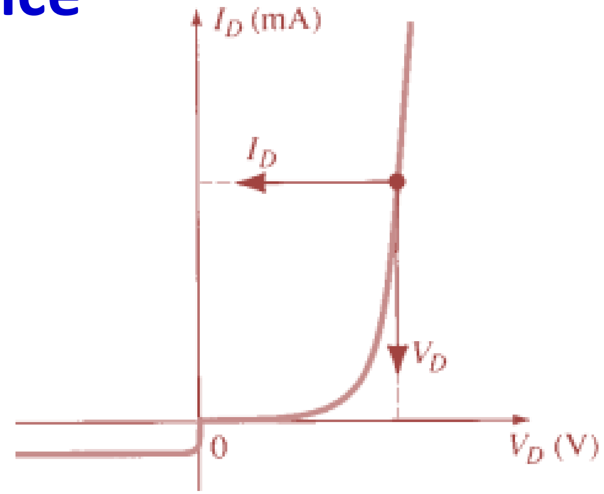


$$I = I_o[e^{qV/kT}\text{-}1]$$

Resistance Levels

Static Resistance

$$R_D = \frac{V_D}{I_D}$$

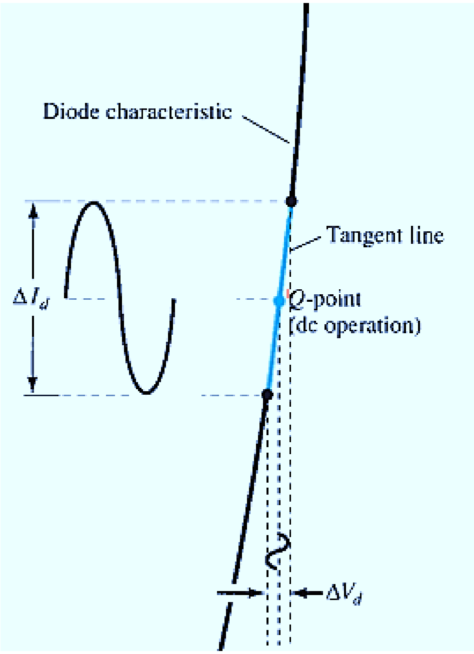


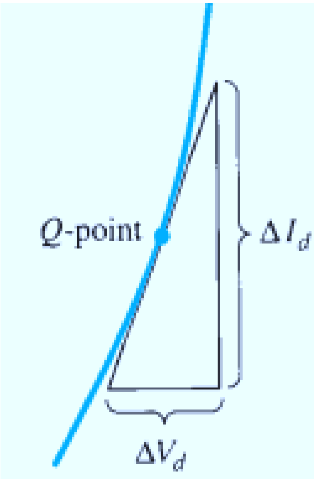
Dynamic Resistance

If a sinusoidal rather than a dc input is applied, then the varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage.

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

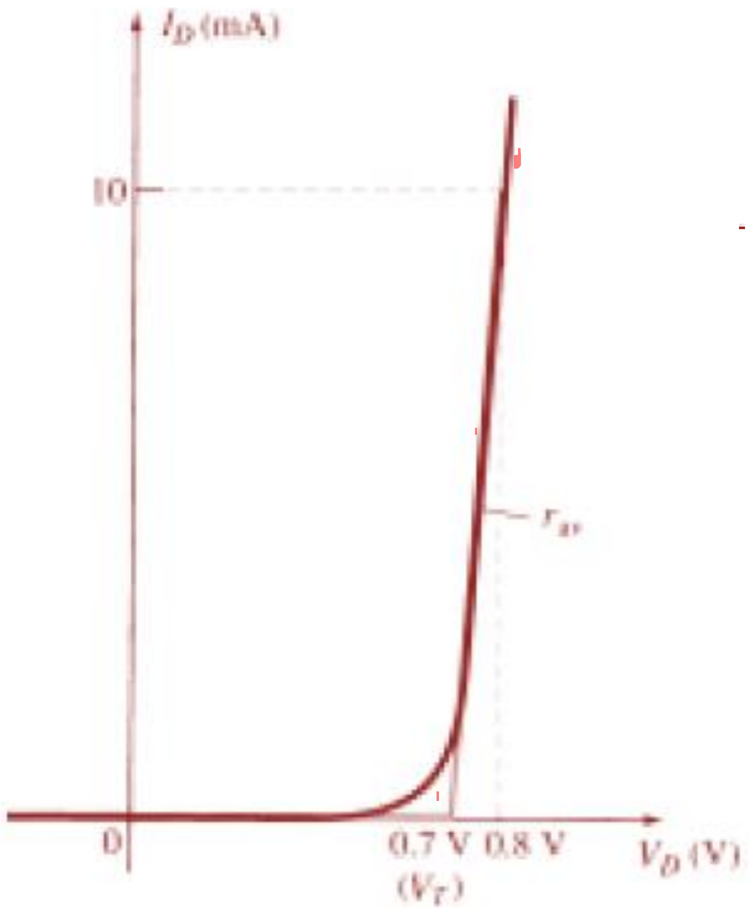
$$r_d = \frac{26\ \text{mV}}{I_D}$$

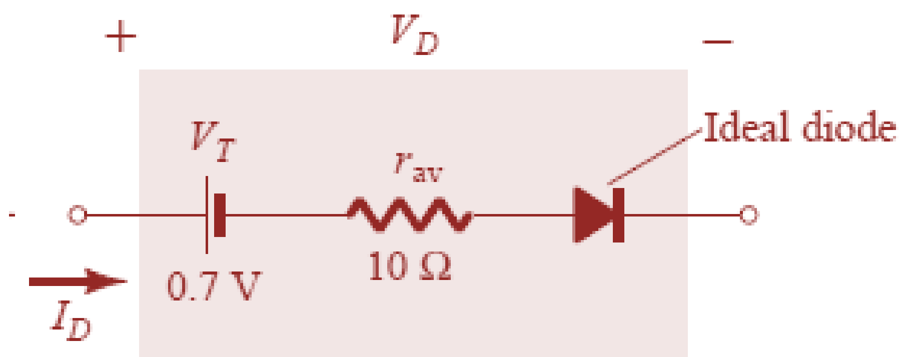




Diode Equivalent Circuits

Piece Wise Linear Model



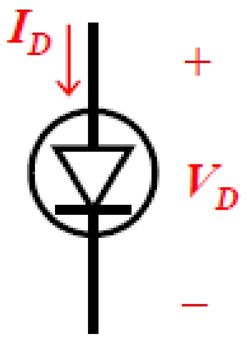


Diode Equivalent Circuits

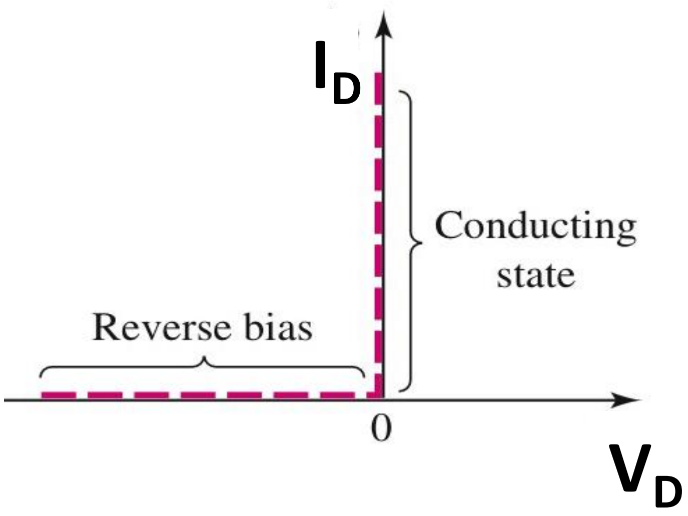
Simplified Equivalent Circuit

Diode Equivalent Circuits

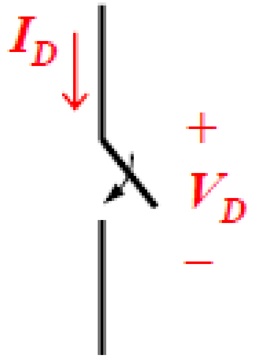
Ideal Diode



Circuit Symbol



I-V Characteristic



Switch Model

$I_D > 0$, $V_D = 0$

$I_D = 0$, $V_D < 0$

Diode behaves like a switch.
It is closed in forward bias and open in reverse bias

Capacitances

Basically, there are two types of capacitance associated with a p-n junction

I. Junction capacitance: Due to the dipole in the transition region. Also called transition region capacitance or depletion layer capacitance. It dominates under reverse bias conditions.

$$C_j = \frac{\varepsilon \cdot A}{\sqrt{\frac{2 \cdot \varepsilon \cdot \left(V_{bi} - V_{applied}\right)}{q} \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)}}$$

II Charge storage capacitance: Arises from the voltage lagging behind the current due to charge storage effects. Also referred to as diffusion capacitance. It is dominant when the junction is forward biased

1. The intrinsic carrier concentration of silicon sample at 300K is 1.5 x $10^{16}/m^3$. If after doping the number of majority carriers is 5 x $10^{20}/m^3$, find the minority carrier density.

$$n_i^2 = np \text{ (Law of mass action)}$$

$$p = \frac{n_i^2}{n} = 4.5\ x\ 10^{11}/m^3$$

2. An N-type Si bar 0.1 cm long and 100 μm^2 in cross-sectional area has a majority carrier concentration of 5 x 10^{20} m^{-3} and the carrier mobility is 0.13 m^2/V s at 300K.Find the resistance of the Si bar.

Here Si bar is N type, so

$$\sigma_n = qn\mu_n$$

$$\rho_n = \frac{1}{\sigma_n}$$

$$R = \frac{\rho_n l}{A} = 0.96\ x\ 10^6 ohm$$

3. Consider a Si P-N junction diode at room temperature having the following parameters

Doping of the N-side = 1×10^{17} /cm^3

Depletion width on the N-side = 0.1 μm

Depletion width on the p-side = 1.0 μm

Intrinsic carrier concentration = 1.4×10^{10}/cm^3

Thermal voltage (kT/q) = 26mV

Find the build-in-potential

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right)$$

$W_P N_A = W_N N_D$

$N_A = W_N N_D / W_P = 1 \times 10^{22}$ /cm^3

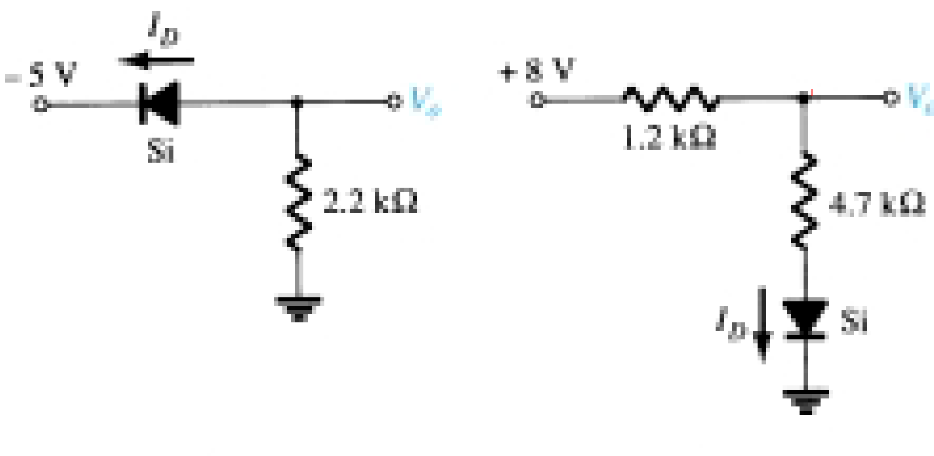
$V_{bi} = 0.76$ V

4. The current flowing through a P-N junction diode is 60 mA for a forward bias of 0.9V at 300K. Find static resistance and dynamic resistance.

$R_D = V_D / I_D$

$r_d = 26\text{mV} / I_D$

5. Determine *Vo* and *ID* for the networks of the following Fig.



(a) (b)

(a) V_0= 0.7V-5V= -4.3V

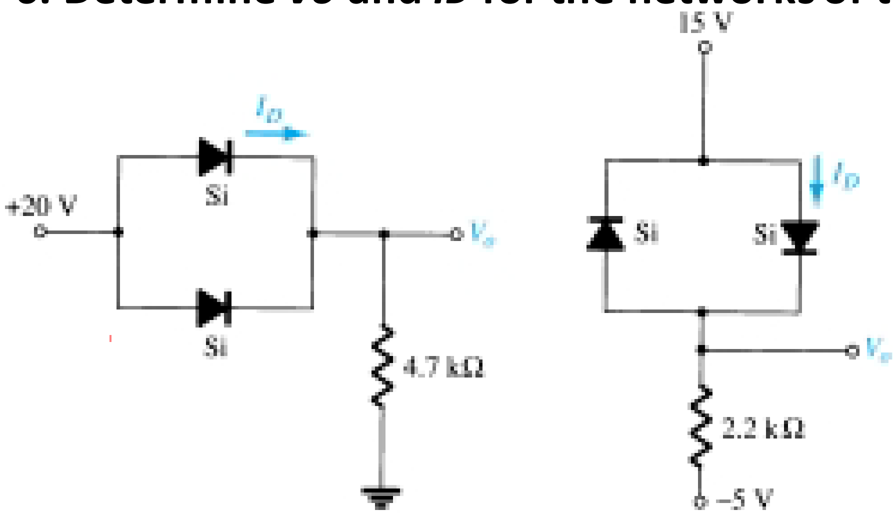
$$I_D = \frac{0-(-4.3)}{2.2\ x\ 10^3} = 1.955 \text{ mA}$$

(b) $$I_D = \frac{8-0.7}{(1.2+4.7)x\,10^3} = 1.24\text{mA}$$

$$V_0 = 1.24mA\ x\ 4.7kohm + 0.7V$$

= 6.53V

6. Determine *Vo* and *ID* for the networks of the following Fig.



(a) (b)

(a) $$I_{Total} = \frac{20-0.7}{4.7\ x\ 10^3} = 4.106 \text{ mA}$$

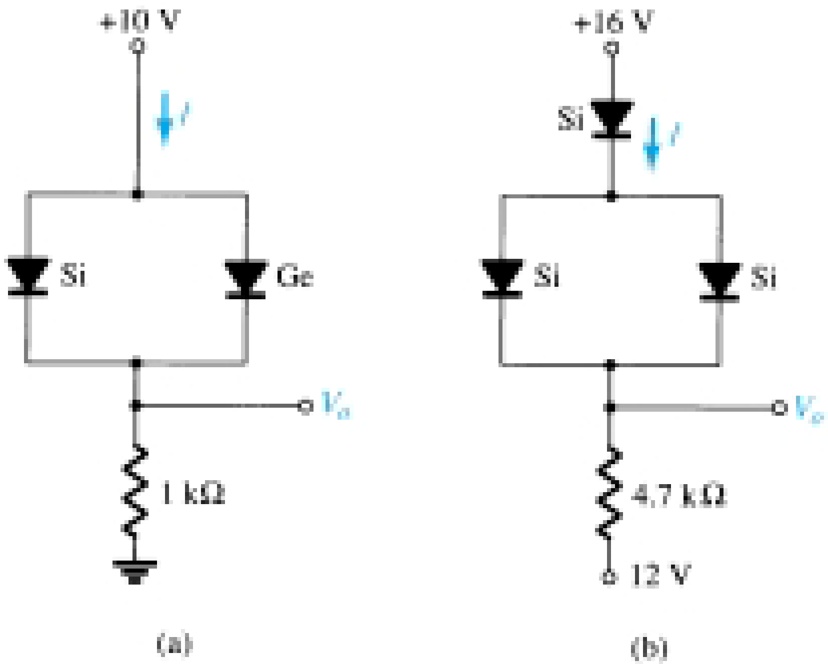
$$I_D = \frac{I_{Total}}{2} = 2.05 \text{ mA}$$

$$V_0 = 20 - 0.7 = 19.3\text{V}$$

(b) $$I_D = \frac{15+5-0.7}{2.2\ x\ 10^3} = 8.77 \text{ mA}$$

$$V_0 = 15 - 0.7 = 14.3\text{V}$$

7. Determine *Vo* and *I* for the networks of the following Fig.



(a) $I = \frac{10-0.3}{1\ x\ 10^3} = 9.7\text{mA}$

V_0= 10-0.3V = 9.7V

(b) $I = \frac{16-0.7-0.7-12}{4.7\ x\ 10^3} = 0.553\text{mA}$

V_0= (0.553mA x 4.7kohm)+12V
= 14.6V

8. Consider an abrupt p-n junction. If the junction capacitance is 1pF for applied reverse bias of 1V, what is the value of junction capacitance for reverse bias of 4V?

$$C_j \propto 1/\sqrt{V_R} \qquad \frac{C_{j1}}{C_{j2}} = \sqrt{\frac{V_{R2}}{V_{R1}}} = \sqrt{\frac{4}{1}} = 2$$

C_{j2} = 0.5pF