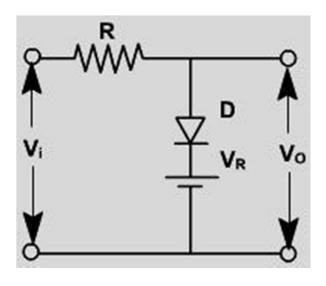
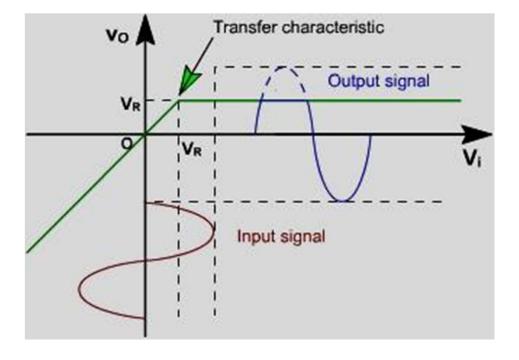
# Clipper

Clipping circuits are used to select that portion of the input wave which lies above or below some reference level. Some of the clipper circuits are discussed here. The transfer characteristic ( $v_o$  vs  $v_i$ ) and the output voltage waveform for a given input voltage are also discussed.

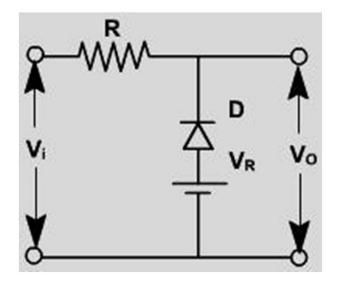
#### **Clipper Circuit 1**



- > If  $v_i$  <  $V_R$ , diode is reversed biased and does not conduct. Therefore,  $v_o = v_i$
- $\rightarrow$  if  $v_i > V_R$ , diode is forward biased and thus,  $v_o = V_R$ .

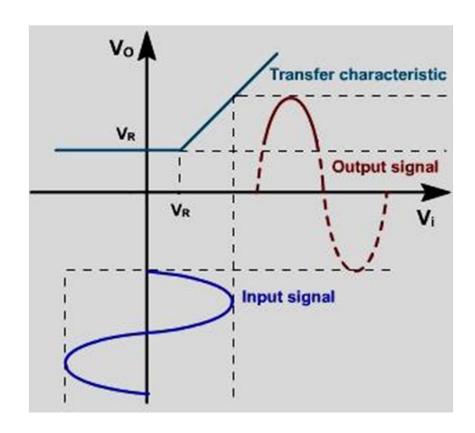


#### **Clipper Circuit 2**

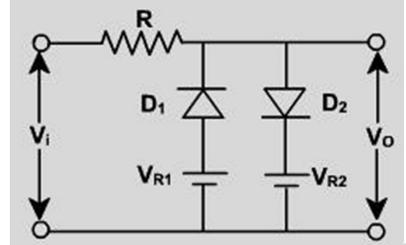


- $\triangleright$  If  $v_i > V_R$ , diode is reverse biased.
  - $v_o = v_i$
- $\triangleright$  If  $v_i < V_R$ , diode is forward biased.

$$v_o = V_R$$



### Clipper Circuit 3 To clip the input signal between two independent levels ( $V_{R1} < V_{R2}$ )

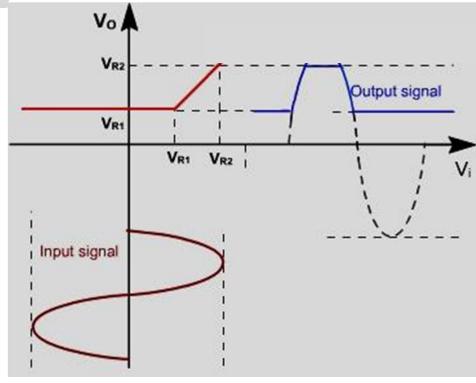


## When

(i) 
$$v_i \le V_{R1}, v_o = V_{R1}$$

(ii) 
$$V_i \ge V_{R2}$$
,  $V_o = V_{R2}$ 

(iii) 
$$V_{R1} < v_i < V_{R2}$$
  $v_o = v_i$ 

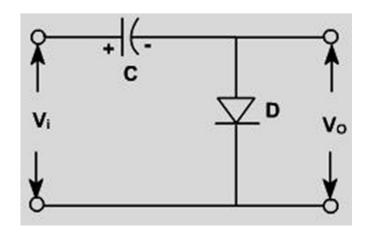


# **Clamper**

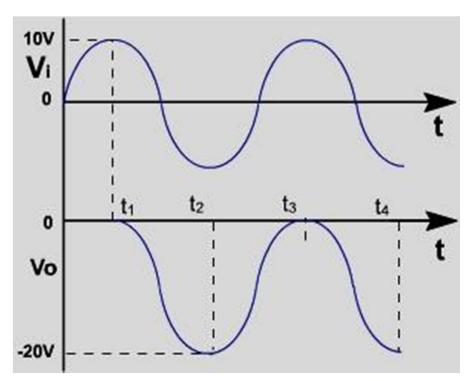
- The clamping network is one that will "clamp" a signal to a different dc level.
- The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift.
- The magnitude of R and C must be chosen such that the time constant  $\tau$  = RC is large enough (generally 5 times) to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting.

Clamper
Positive clamper
Negative clamper

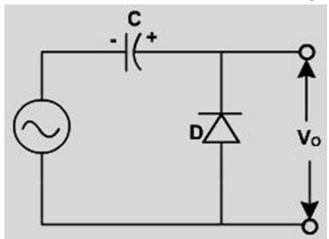
#### **Negative Diode Clamper:**



- ☐ Let the input signal swings form +10 V to -10 V.
- ☐ During first positive half cycle as Vi rises from 0 to 10 V, the diode conducts.
- Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to  $t_1$ .
- ☐ The capacitor charges during this period to 10 V, with the polarity shown.
- $\Box$  V<sub>i</sub> starts to drop which means the anode of D is negative relative to cathode, (V<sub>D</sub> = v<sub>i</sub> v<sub>c</sub>) thus reverse biasing the diode and preventing the capacitor from discharging.
- ☐ Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit,
- ☐ Therefore the equivalent circuit becomes an input supply in series with -10 V dc voltage
- ☐ The resultant output voltage is the sum of instantaneous input voltage and dc voltage (-10 V).



### **Positive Diode Clamper:**



- ☐ Let the input signal swings form +10 V to -10 V.
- ☐ During first negative half cycle as V<sub>i</sub> rises from 0 to -10 V, the diode conducts.
- Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to  $t_1$ .
- ☐ The capacitor charges during this period to 10 V, with the polarity shown.
- After that  $V_i$  starts to drop which means the anode of D is negative relative to cathode,  $(V_D = v_i v_c)$  thus reverse biasing the diode and preventing the capacitor from discharging.
- ☐ Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit, therefore the equivalent circuit becomes an input supply in series with +10 V dc voltage and
- ☐ The resultant output voltage is the sum of instantaneous input voltage and dc voltage (+10 V).

