

Basic Electronics
ECC 01

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Band Structure

The band structure of a solid describes ranges of energy that an electron is "forbidden" or "allowed to have". There are many bands, but most are completely filled or empty.

The two at the boundary between filled and empty determine the behaviours of insulators, metals and semiconductors.

Silicon and Germanium are the most familiar and extensively used semiconductors.

Energy Bands in Solids

An energy band is a set of close lying energy levels, which are nearly continuous.

Valence band the energy band corresponding to the valence electrons is called the valence band.

After applying sufficient energy to the electrons in the valence band, they become free electrons and contribute to the electrical conductivity of the material. This energy band is defined as the conduction band.

Except in good conductors, there is a gap between the valence band and the conduction band. This gap is called the forbidden energy gap.

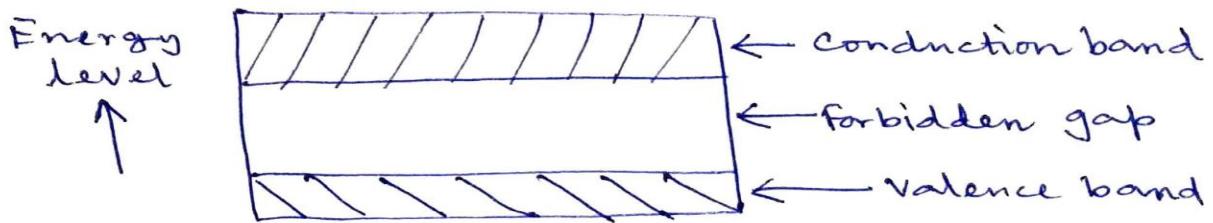


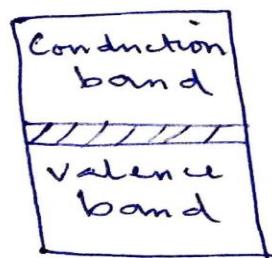
figure: Conduction and Valence bands

Conductors, Semiconductors and Insulators

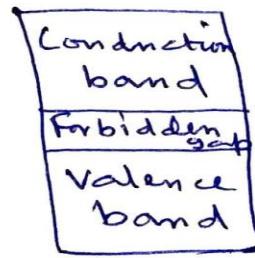
A metallic conductor has a large number of free electrons. In case of Conductors, the Conduction and Valence bands overlap and the forbidden gap is zero.

In Case of semiconductors, the Conduction band and the Valence band are partially filled. There is a small energy gap between the Conduction and Valence bands.

In Case of insulators, the Conduction band is empty and the Valence band is completely filled. The energy gap between the Conduction band and the Valence band is very large.



(a)
conductor



(b)
Semiconductor



(c)
Insulator

Figure: Energy bands in Solids

Table:- Energy gap of a few materials

Material	Forbidden gap
Conductor-metals	Zero
Insulator - diamond	7 ev
Semiconductors	
— Silicon	1.1 ev
— Germanium	0.72 ev
— Gallium arsenide	1.34 ev

Intrinsic Semiconductors

Semiconductor like germanium or silicon in pure form is called an intrinsic semiconductor.

Extrinsic Semiconductors

An intrinsic semiconductor is converted to an extrinsic semiconductor by adding very small quantities of either pentavalent atoms or trivalent atoms. The element added is called impurity. The process of adding the impurity is called doping.

This leads to the possibility of two types of Semiconductors.

a) n-type Semiconductors:- Here the majority charge carriers ~~and~~ are free electrons.

b) p-type Semiconductors:- Here the majority charge carriers are holes.

Free Electron theory and Fermilevel

The free electron theory explains satisfactorily most metallic properties.

Enrico Fermi, using Fermi-Dirac statistics showed that the probability of a particular energy state being occupied by electrons is given by a factor called the Fermi factor as

$$f(E) = \frac{1}{e^{(E-E_0)/kT} + 1}$$

E = Energy of an electron in the allowed energy state

E_0 = Fermi energy

Fermi energy is indicated as "Fermi level" in the energy band diagram.

For $E < E_0$, the exponential term is negative.

As $T \rightarrow 0$, the exponential term approaches zero.

$$f(E) = 1$$

For $E > E_0$, the exponential term is positive.

As $T \rightarrow 0$, the exponential term approaches infinity.

$$f(E) = 0$$

Fermi level in intrinsic Semiconductors

$$E_0 = \left(\frac{E_c + E_v}{2} \right)$$

$$E_g = 2(E_0 - E_v)$$

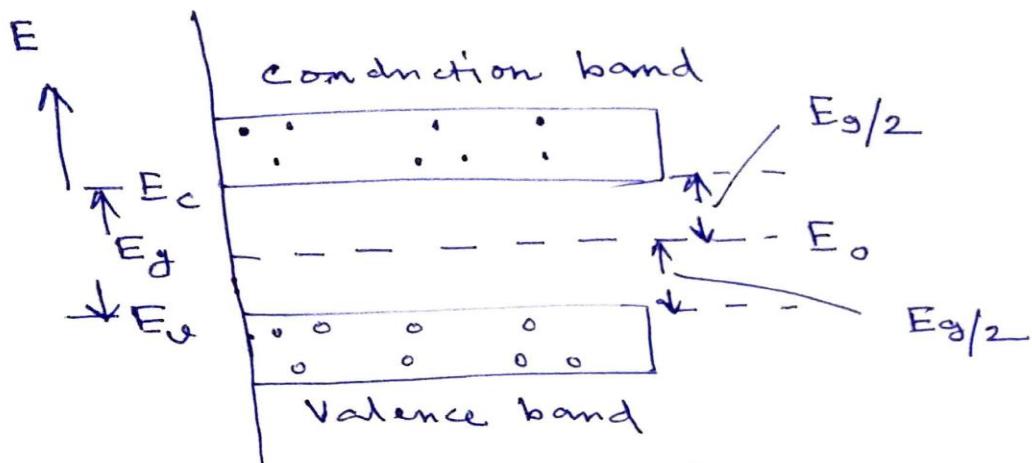


Figure: Fermilevel in intrinsic Semicond

Fermi Level in n-type semiconductor

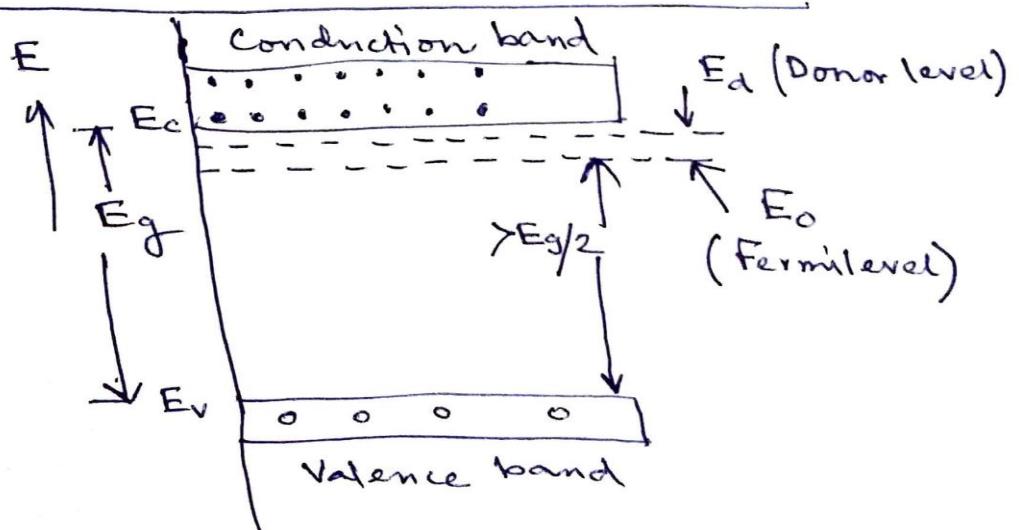


Figure: Fermilevel in n-type Semiconductors

p-type Semiconductor

The fermilevel shifts towards conduction band due to n-type impurity and shifts towards valence band due to p-type impurity.

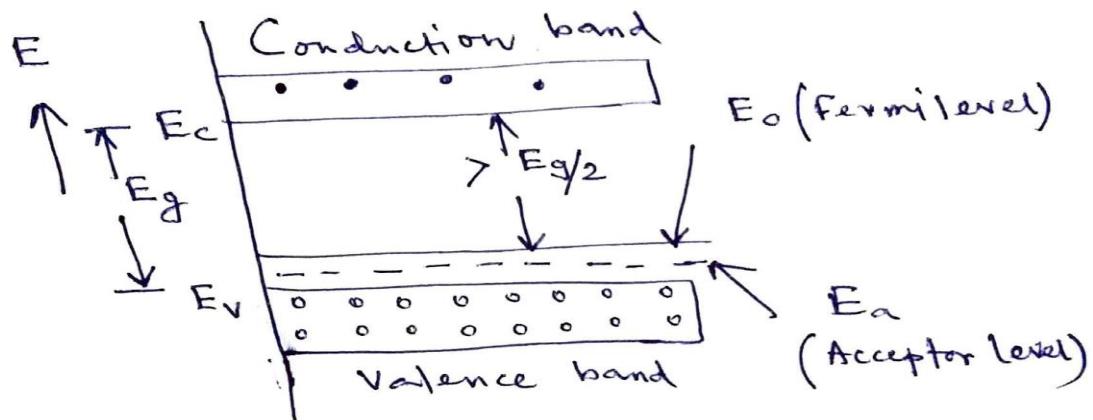


Figure: Fermilevel in p-type semiconductors

Electrical Conductivity of Semiconductors

The current components due to the drift of free electrons and holes add up because of the opposite polarity of the charge carriers.

The total current due to the electric field is called the drift Current. Drift current depends on the ability of the charge carriers to move. A measure of this ability to move is called drift mobility and designated

by μ .

$$\mu = v/E$$

v = drift velocity
 E = Electric field.

$$\begin{aligned}
 \text{The unit of } M &= \frac{V}{E} \\
 &= \frac{\text{meter second}^{-1}}{\text{volt meters}^{-1}} \\
 &= \frac{\text{meter}^2}{\text{volt second}}
 \end{aligned}$$

Current density

$$J = \frac{I}{A}$$

The Current density in a Semiconductor

$$\begin{aligned}
 J &= J_n + J_p \\
 &= ne \mu_n E + pe \mu_p E
 \end{aligned}$$

In an intrinsic semiconductor

$$n = p = n_i \text{ (intrinsic carrier concentration)}$$

$$\therefore J = n_i e (\mu_n + \mu_p) E$$

In terms of drift velocities

$$J = n_i e (v_n + v_p)$$

For an extrinsic semiconductor

$$np = n_i^2$$

Conductivity

$$\begin{aligned}
 \sigma &= \frac{1}{\rho} \\
 \rho &= \frac{RA}{l} \quad [\because R = \rho \frac{l}{A}]
 \end{aligned}$$

ρ = resistivity of the material
in Ωm

l = length of the semiconductor bar

$$A = bh \quad [b = \text{breadth}, h = \text{height}]$$

$$\sigma = \frac{1}{\rho} = n \mu_n e + p \mu_p e$$

Problem A potential difference of 10V is applied across the ends of pure bar of silicon of cross-sectional area $0.4 \times 10^{-3} \text{ m}^2$ and length $0.6 \times 10^{-2} \text{ m}$. The intrinsic carrier concentration is $1.5 \times 10^{16} \text{ electrons/m}^3$. Assuming $\mu_n = 0.14 \text{ m}^2/\text{Vs}$, $\mu_p = 0.05 \text{ m}^2/\text{Vs}$, $e = 1.6 \times 10^{-19} \text{ coulomb}$.

$$\mu_p = 0.05 \text{ m}^2/\text{Vs}$$

calculate

- i) electric field in the specimen
- ii) drift velocities of electrons and holes
- iii) total current density
- iv) total current
- v) conductivity
- vi) resistivity
- vii) and
- viii) bulk resistance of the bar.

Problem If the bar of silicon of the last problem is doped with a p-type impurity to have a hole concentration of 8.5×10^{21} holes/m³, calculate

- i) electron concentration in the extrinsic semiconductor
- ii) new current density
- iii) Conductivity for the extrinsic Semiconductor bar

Effect of temperature on Semiconductor

A semiconductor is an insulator at 0K. As temperature is increased, conductivity increases. With temperature, the resistance decreases. Thus, it is called that semiconductors have negative temperature co-efficient of resistance.

Dependence of n_i on Temperature

$$n_i^2 = A_0 T^3 e^{-E_{go}/kT}$$

A_0 = constant, the value depends on the type of Semiconductor

T = Temperature in K

E_{go} = forbidden energy gap

= 0.785 eV for Ge at 0K
= 1.21 eV for Si at 0K

K = Boltzmann constant
 $= 8.62 \times 10^{-5}$ eV/K

9

$$\text{Thus } A_0 = \frac{n_i^2 \cdot e^{Eg_0/kT}}{T^3}$$

Mass - Action Law

Mathematically $n_p = n_i^2$

n_i = intrinsic Carrier Concentration

n = electron Concentration

p = hole Concentration

why Si is preferred over Ge

i) Si devices can operate upto 150°C

whereas for Ge it is 100°C .

ii) Si is more readily available than Ge.

iii) Extremely pure Ge is more costly than extremely pure Si.

iv) Si devices can support more higher voltage than Ge.

v) Si shows better performance than Ge.

Advantages of semiconductor devices over Vacuum tubes

i) Semiconductor devices consume much less power than vacuum devices

ii) Semiconductor devices occupy smaller area and are lighter

iii) Semiconductor devices offer more reliability and life time

iv) Semiconductor devices are faster.

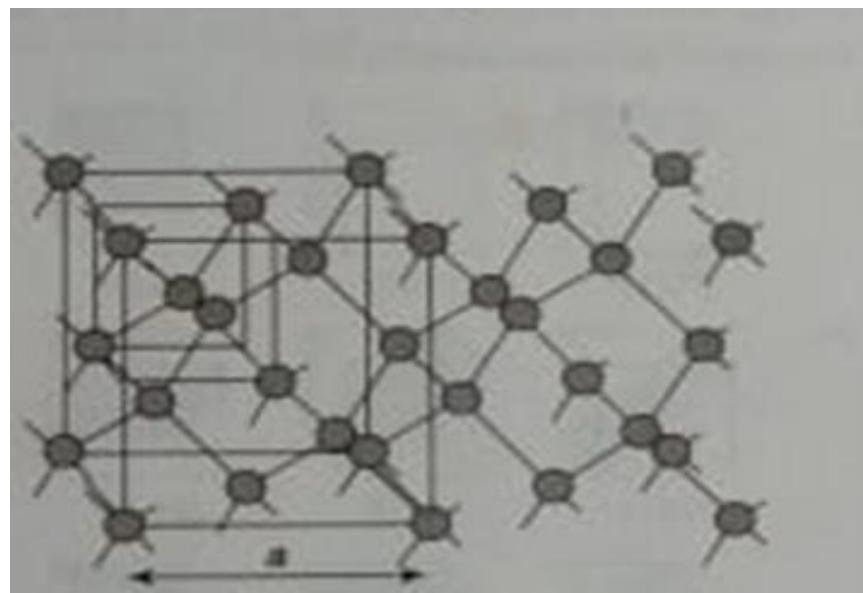
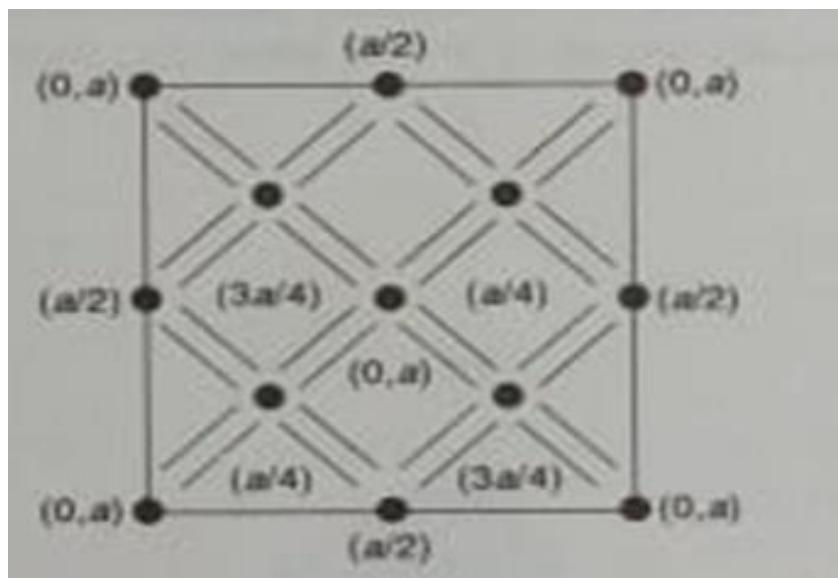


Figure.(a) The diamond lattice of Silicon and Germanium



**Figure.(b) The dc structure showing position of 18 atoms
on the plan view of the lattice structure**

Problem A conductor has free electron density of $4.5 \times 10^{24}/m^3$. When a voltage is applied, a constant drift velocity of $4.5 \times 10^{-2} m/s$ is attained by electrons. Find current flowing through the material when its cross-sectional area is 1 cm^2 .

Problem What is the hole concentration of an Si crystal having donor concentration of $2.4 \times 10^{24}/m^3$, when intrinsic carrier concentration is $1.6 \times 10^{18}/m^3$? Find ratio of electron and hole concentration.

P-N Junction

A junction between n and p-type materials in a specimen called the p-n junction.

The figure shows the p-n junction. It is a single crystal of germanium or silicon with its one half doped with n-type impurity and the other half doped with p-type impurity.

On the p-side, the majority charge carriers are holes whereas the majority charge carriers are free electrons for n-side.

Unbiased p-n junction

A barrier potential is created at the junction with negative polarity on the p-side and a positive polarity on the n-side.

The typical barrier potential for a Ge p-n junction is about 0.3V and 0.7V for a Si junction at room temperature. The barrier potential is represented by V_B .

The movement of charge carriers across the junction leaves a layer on either side, which is depleted of mobile charge carriers. This region is called depletion region.

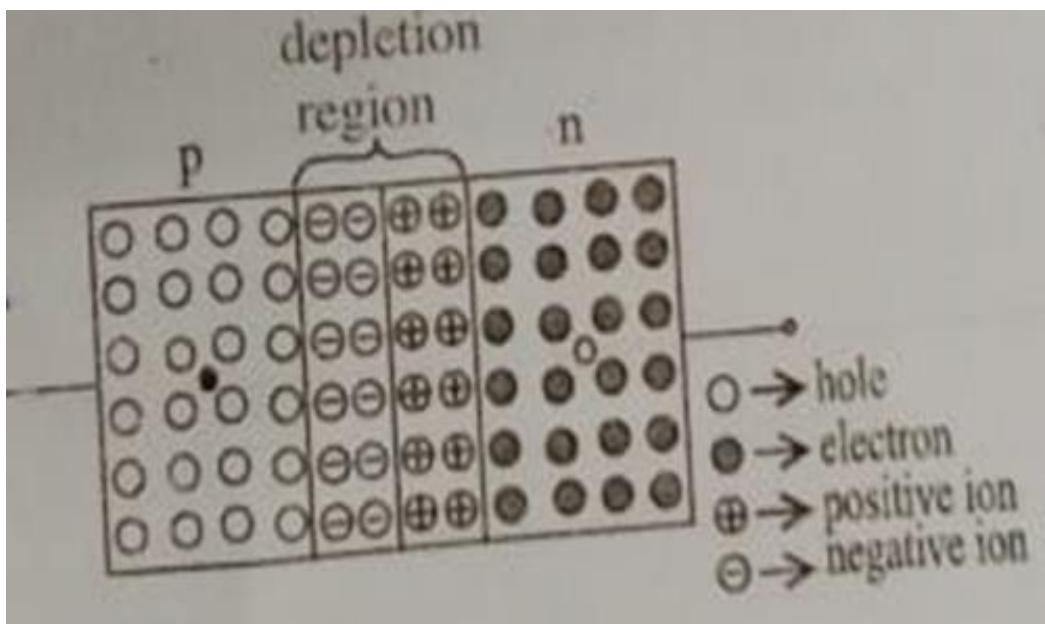


Figure. pn junction

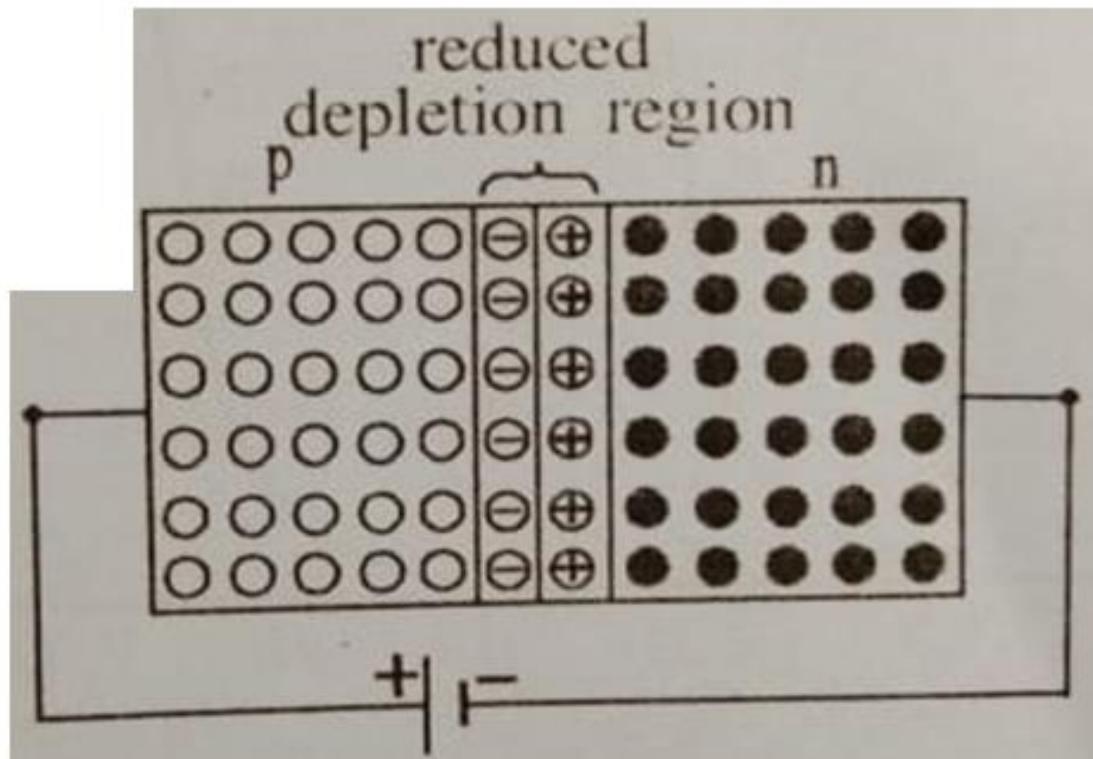


Figure. pn junction under forward bias

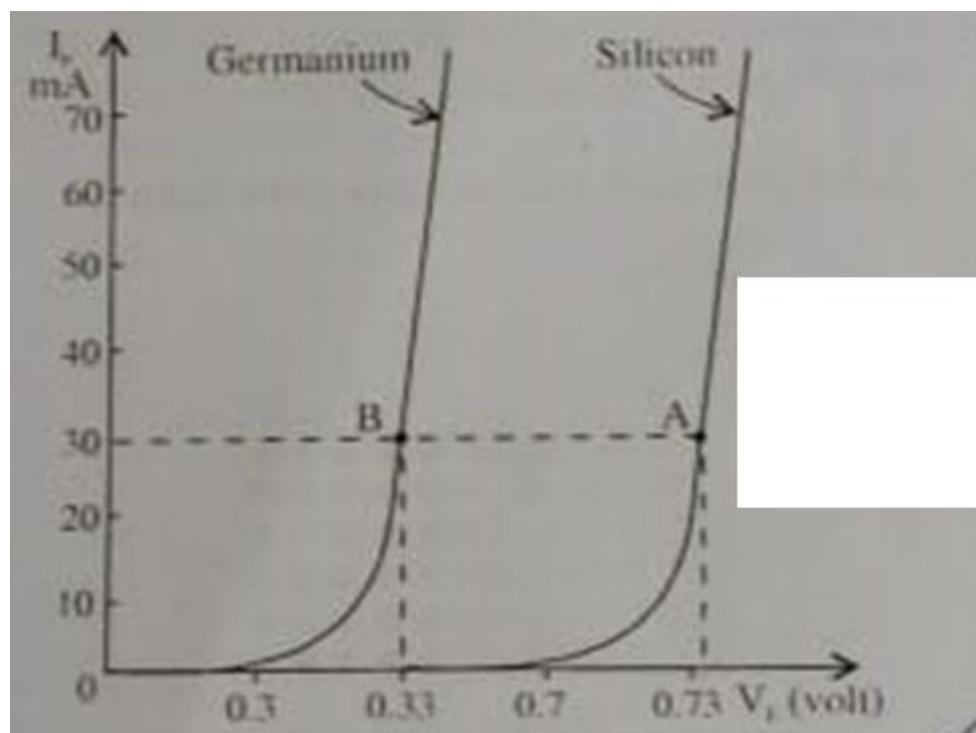


Figure. Forward bias characteristics for germanium and silicon diodes

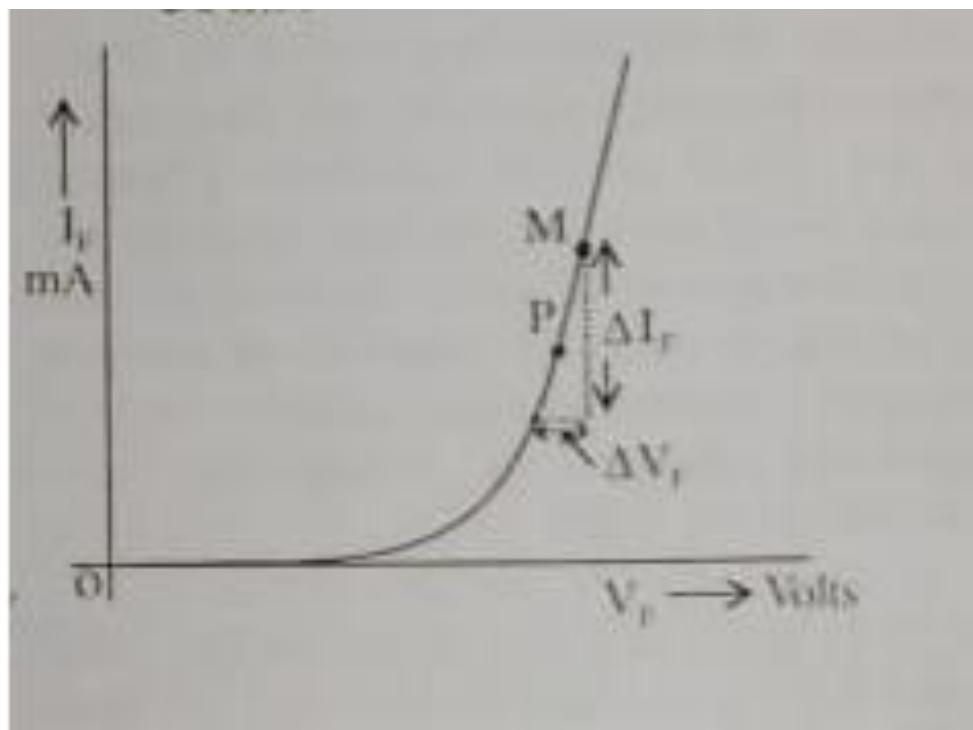


Figure. Forward characteristics to determine dynamic resistance

Flow of charge carriers across the junction

Electric field produced by the barrier potential at the junction opposes the flow of electrons from the n-side and the flow of holes from the p-side. The barrier potential assists the flow of minority carriers across the junction.

Forward biased pn junction

A majority carrier current flows and the junction is said to be forward biased.

Here, the external bias voltage is applied with the positive polarity on the p-side and negative on the n-side.

Static resistance (R_F)

From point A on figure

$$R_F \text{ for Silicon} = \frac{0.7V}{30mA} = 23.3\Omega$$

At point B

$$R_F \text{ for Germanium} = \frac{0.3V}{30mA} = 10\Omega$$

Dynamic resistance is measured as the reciprocal of the slope of the forward characteristic beyond the knee.

$$\text{We get } r_F = \frac{\Delta V_F}{\Delta I_F}$$

Due to the very small value of forward resistance of a diode, a pn junction diode can be considered as a closed switch under forward bias.

Reverse biased pn junction

A pn junction with n side connected to the positive and the p-side to the negative of a battery is said to be reverse biased.

Although there is no majority carrier current under reverse bias, there is a very small current due to the minority carriers crossing the junction. This is usually called Reverse Saturation Current, I_0 .

The dynamic reverse resistance

$$r_d = \frac{\Delta V_R}{\Delta I_R}$$

Since $\Delta I_R \rightarrow 0, r_d \rightarrow \infty$

Hence a reverse biased pn junction has very large resistance and hence it can be considered as an open switch under reverse bias.

Reverse breakdown in a diode

When the reverse voltage is gradually increased, the current is found to abruptly shoot up at a certain applied voltage, called reverse breakdown voltage.

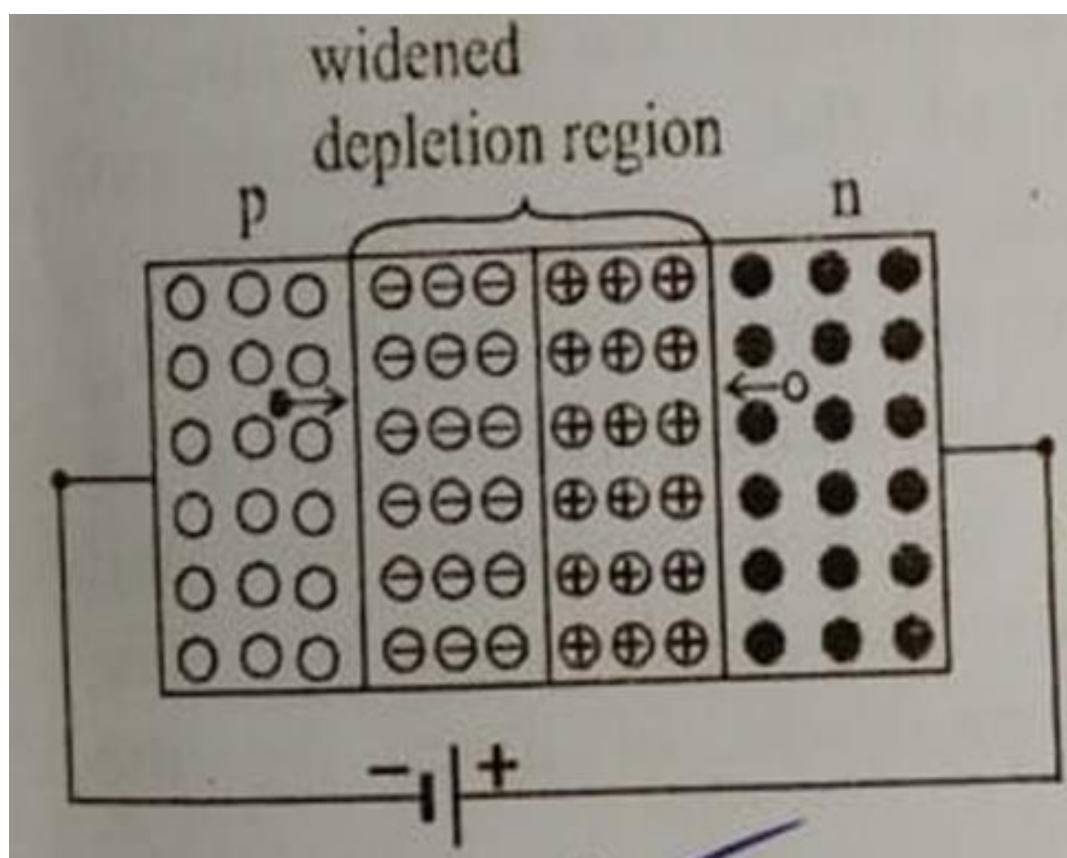


Figure. pn junction under reverse bias

Two types of breakdown mechanisms:

i) Avalanche breakdown
and

ii) Zener breakdown

The voltage at which the Zener breakdown occurs is called the Zener breakdown voltage, V_Z .

V-I characteristics of p-n diode
and diode equation

$$I = I_0 \left(\frac{e^{qV}}{e^{\eta kT}} - 1 \right)$$

where, I_0 = reverse saturation current

$$q = 1.6 \times 10^{-19} \text{ Coulomb}$$

V = applied voltage across the junction

$$k = \text{Boltzmann constant} \\ = 1.38 \times 10^{-23} \text{ J/K}$$

T = Temp. in Kelvin

$$\eta = \text{a constant} \\ = 1 \text{ for Ge} \\ = 2 \text{ for Si}$$

Consider the diode equation

$$I = I_0 \left(e^{qV/kT} - 1 \right)$$

Under forward bias,

V is +ve and

$$I = I_0 e^{qV/kT}$$

The current increases exponentially.

Under reverse bias, V is $-Ve$

$$\therefore I_o \left(e^{\frac{q(-V)}{kT}} - 1 \right) \approx -I_o$$

Problem: Reverse saturation current for a Ge diode at $27^\circ C$ is 10 mA . Calculate the current through it when the applied voltage across it is i) 0.3 V and ii) -6 V

Problem: A germanium diode for which the reverse saturation current is 5 mA has a forward current of 1 A at $27^\circ C$. Calculate the forward voltage drop across it.

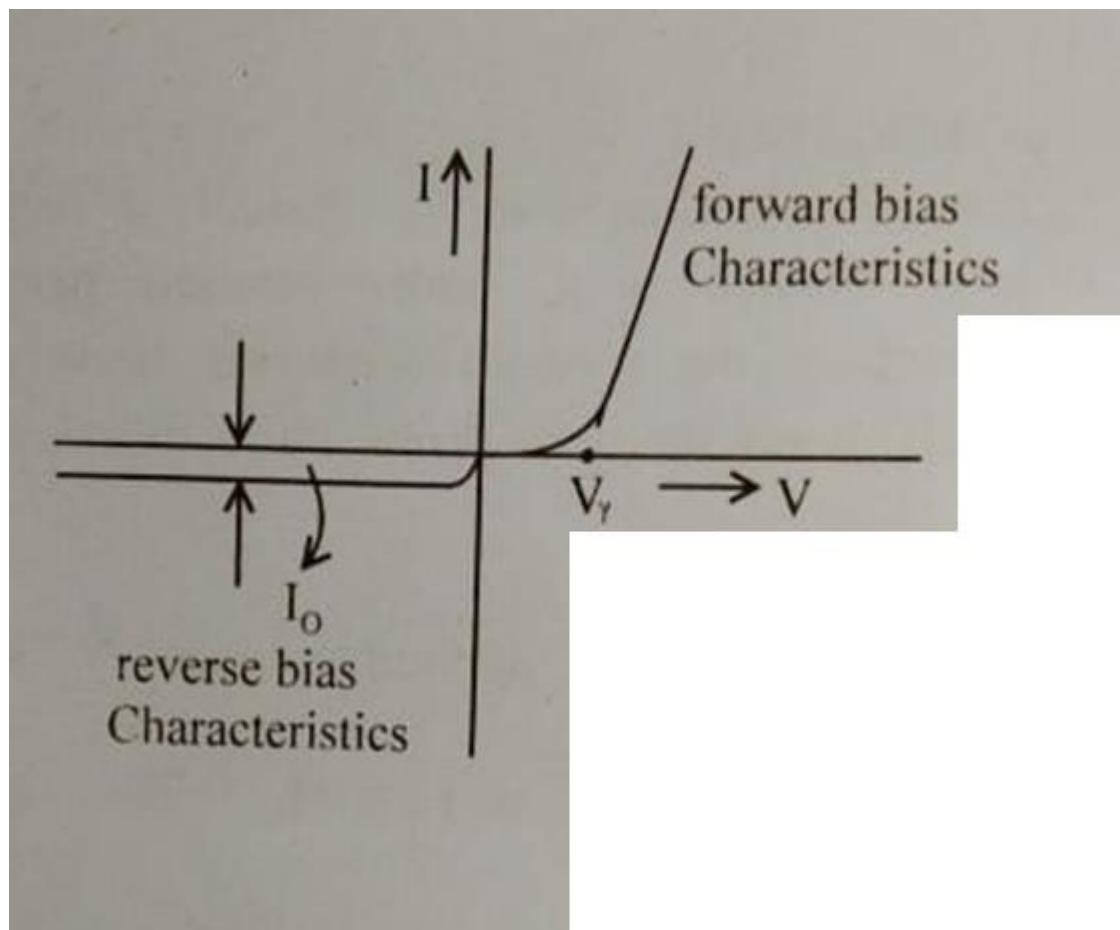


Figure. V-I characteristics of a pn diode

Zener diode

It is designed to operate in reverse breakdown region.

Zener and avalanche breakdown

Here a sudden of current results, called Zener breakdown.

V-I characteristics of a Zener diode

In a Zener diode, when the applied voltage exceeds the reverse breakdown voltage, the Zener maintains a constant voltage.

Zener diode as a voltage regulator

Zener diode is used as a voltage regulator. A good voltage regulator is a device which supplies current to a load at constant voltage independent of the variations in its input voltage and the load.

$$I_Z(\text{max}) = \frac{P_V}{V_Z}$$

I_Z = maximum permissible current in the circuit

P_V = Power rating of the Zener

V_Z = Zener breakdown voltage.

i) $V_i < V_Z$; the output follows the input.

ii) $V_i > V_Z$; the output = V_Z

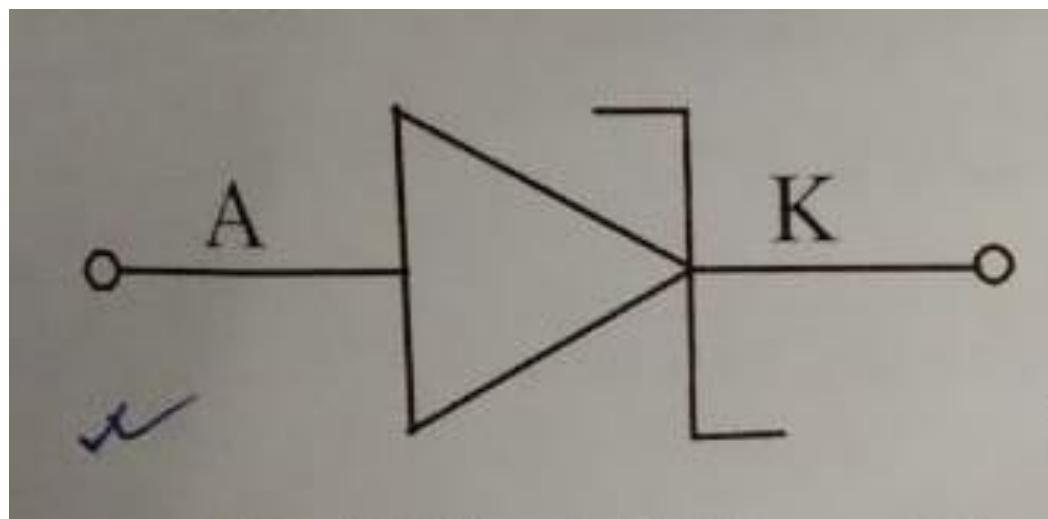


Figure. Symbol of Zener diode

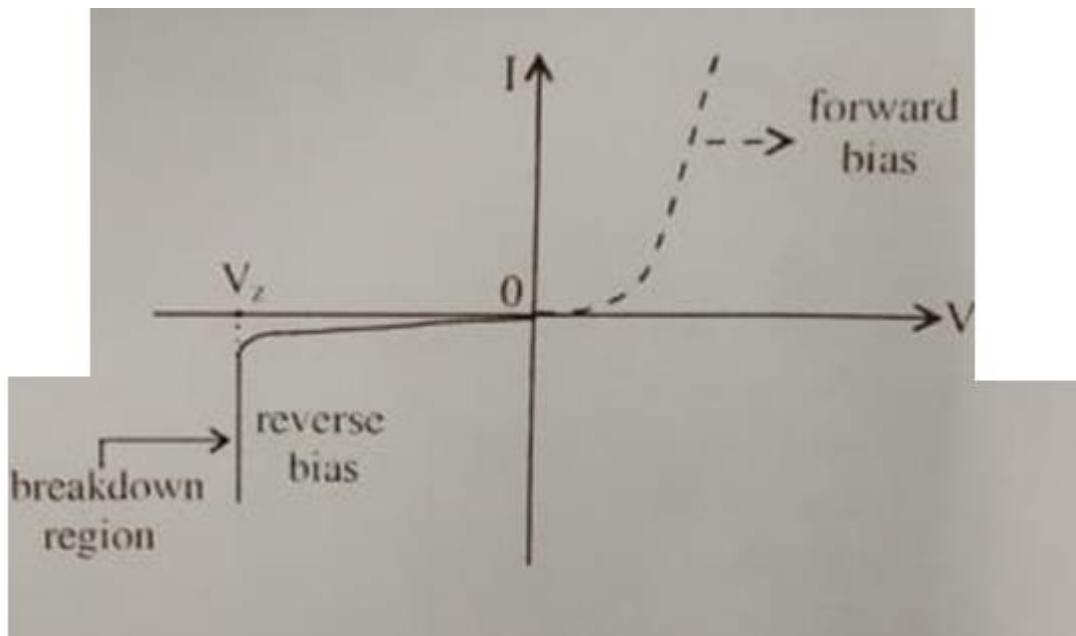


Figure. Zener diode characteristics

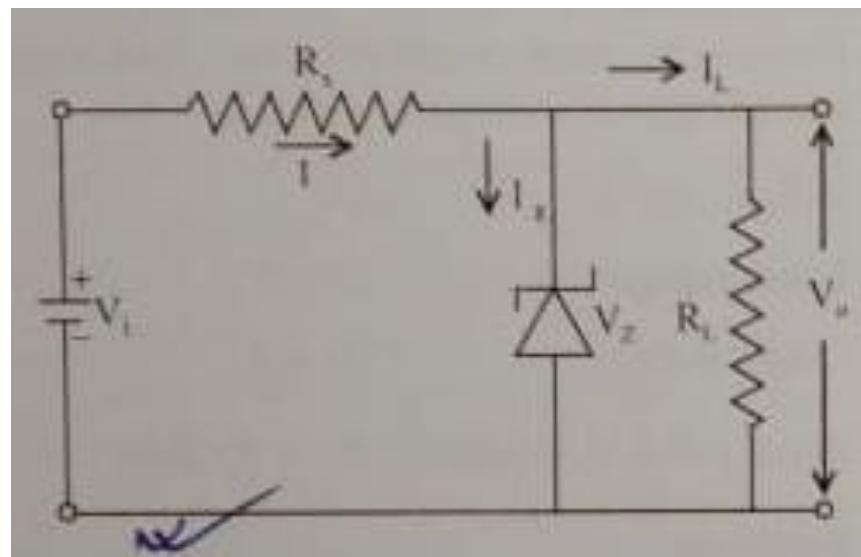


Figure. Zener regulator

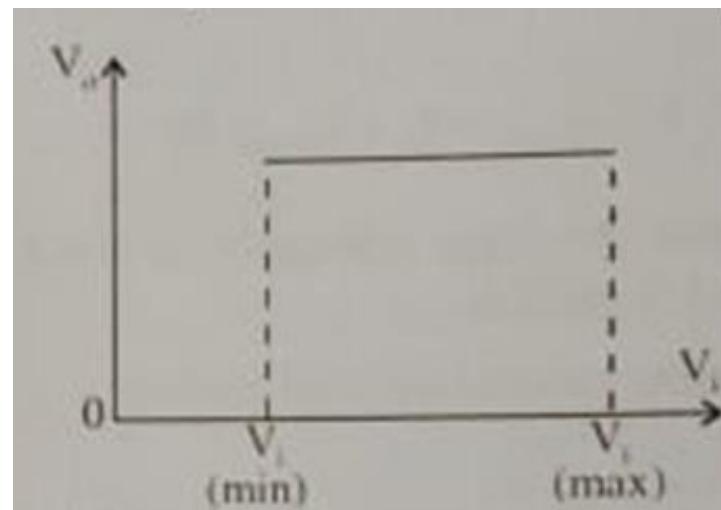


Figure. Line regulation

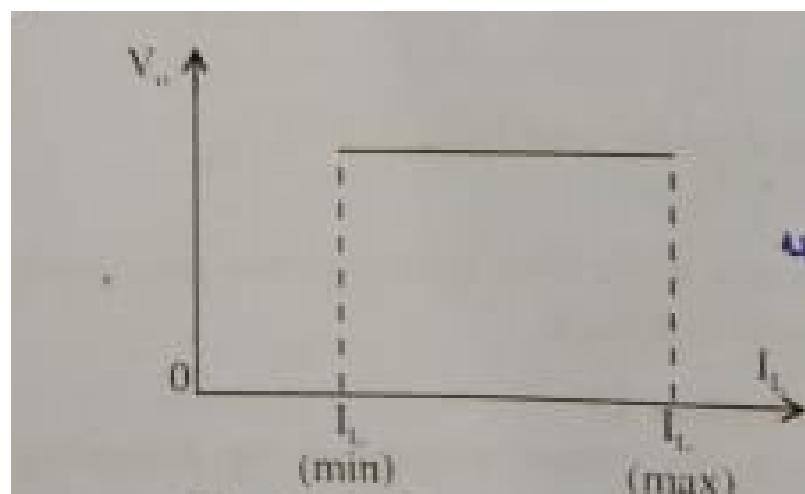


Figure. Load regulation

For a fixed load, if there is a change in the input voltage, the output voltage remains constant for a specified range of input voltage. This is called line regulation.

But for a fixed input voltage, if the load current is varied within specified limits, the output voltage still remains constant. This is called load regulation.

Problem: Design the Zener Regulator for following specifications:

$$\text{Output voltage} = 5V$$

$$\text{Load current} = 10 \text{ mA}$$

$$\text{Zener Wattage} = 400 \text{ mW}$$

$$\text{Input voltage} = 10V \pm 2V$$

Problem: Design a Zener Regulator for following specifications.

$$\text{Output voltage} = 5V$$

$$\text{Input voltage} = 12 \pm 3V$$

$$\text{Load current} = 20 \text{ mA}$$

$$\text{Zener power}$$

$$\text{dissipation} = 500 \text{ mW}$$

$$\text{Zener voltage} = 5V$$

Rectifiers

A circuit which converts ac to dc voltages, is called a rectifier.

The unidirectional Conducting property of a diode is used in rectification.

Half-Wave rectifier

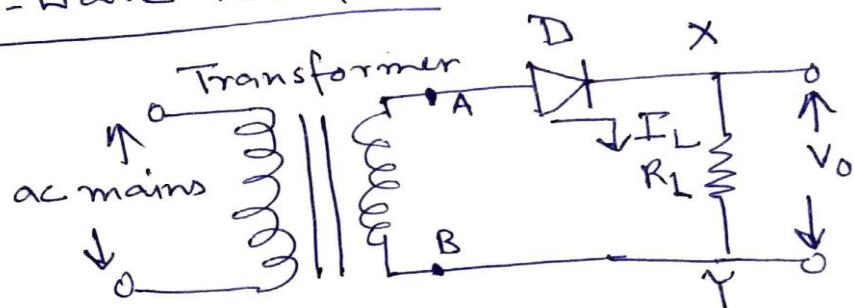


Figure: Half-wave rectifier

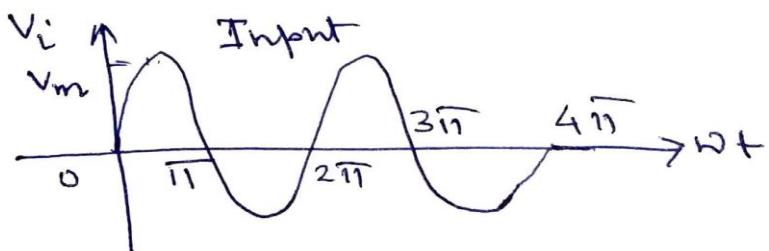


Figure: ac input voltage Waveform

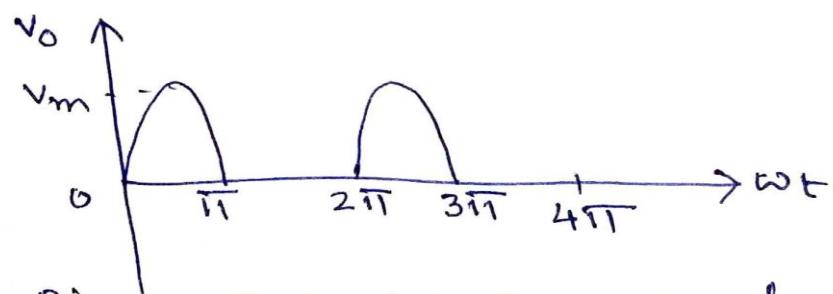


Figure: Output voltage Waveform

During the positive half cycle of the input, diode D is forward biased and conducts. The direction of the current I_L is from X to Y.

During the negative half cycle, the diode D is reverse biased and does not conduct. The entire input voltage appears across the diode. The diode selected should have reverse breakdown voltage much greater than the peak value of the input voltage. If the peak value of the input voltage is V_m , during the negative half cycle, the maximum voltage across the diode is V_m .

The maximum negative voltage appearing across the diode when it is not conducting is called peak inverse voltage, PIV.

The input voltage

$$v_i = V_m \sin \omega t$$

$$i_L = \frac{v_i}{R}$$

$$= \frac{V_m \sin \omega t}{R}$$

$$= I_m \sin \omega t$$

$$\text{and } i_L = I_m \sin \omega t \text{ for } 0 \leq \omega t \leq \pi$$

$$i_L = 0 \text{ for } \pi \leq \omega t \leq 2\pi$$

The dc current in a waveform is nothing but the average value of the output waveform.

$$\begin{aligned} I_{dc} &= \frac{1}{2\pi} \int i_L d(\omega t) \\ &= \frac{1}{2\pi} \int I_m \sin \omega t d(\omega t) \\ &= \frac{I_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} \end{aligned}$$

$$\therefore I_{dc} = \frac{I_m}{\pi}$$

V_{dc} = dc voltage across the load

$$\begin{aligned} &= I_{dc} R_L \\ &= \frac{I_m}{\pi} R_L \\ \therefore V_{dc} &= \frac{V_m}{\pi} \end{aligned}$$

The rms value of the output current is I_{rms} .

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_L^2 d(\omega t)}$$

Since $i_L = I_m \sin \omega t$ in the interval $0 \leq \omega t \leq \pi$

and $i_L = 0$ in the interval $\pi \leq \omega t \leq 2\pi$

$$\text{Thus } I_{rms} = \frac{I_m}{2}$$

$$\text{and } V_{rms} = \frac{V_m}{2}$$

I_{rms} indicated corresponds to the total current which consists of a dc with an ac component superimposed on it.

The rms value of ac fluctuations called the ripples be I'_{rms} .

$$\text{So } I_{rms}^2 = I_{dc}^2 + I'^2_{rms}$$

$$\text{or } I'^2_{rms} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

The output of a rectifier contains ripple. The ripple factor of a rectifier is a measure of the smoothness of the dc output of a rectifier and is given by

$$\text{or } \gamma = \frac{\text{rms value of ripple component}}{\text{dc component}}$$

$$\begin{aligned} \text{or } \gamma &= \frac{I'^2_{rms}}{I_{dc}} \\ &= \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}} \\ &= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \end{aligned}$$

$$\text{Here, } I_{rms} = \frac{I_m}{2}$$

$$\text{and } I_{dc} = \frac{I_m}{\pi}$$

$$\therefore \gamma = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$= 1.21$$

which is high. Thus a half wave rectifier is a poor rectifier

Efficiency

It is another measure of the effectiveness of a rectifier.

It is defined as

$$\eta = \frac{\text{Output dc power delivered to load}}{\text{Input ac power from the Secondary of transformer}}$$

$$= \frac{P_{dc}}{P_{ac}}$$

$$= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times (R_f + R_L)}$$

R_L = Load resistance

R_f = Diode forward resistance

$$\therefore \eta = \frac{\left(\frac{I_m}{\pi}\right)^2 \times R_L}{\left(\frac{I_m}{2}\right)^2 \times (R_L + R_f)}$$

$$= \frac{0.406}{1 + \frac{R_f}{R_L}}$$

With $R_f \ll R_L$, $\eta = 0.406$

Meaning :- only 40.6% of the ac input power is converted to dc in a half wave rectifier

Disadvantages :-

1) The ripple factor $\gamma = 1.21$ is very large

2) The efficiency $\eta = 40.6\%$ is very small.

Full-wave rectifier

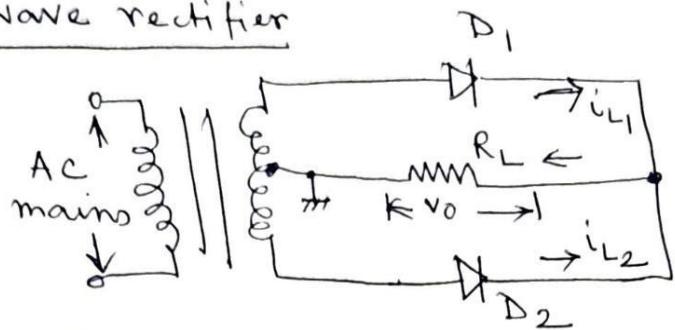


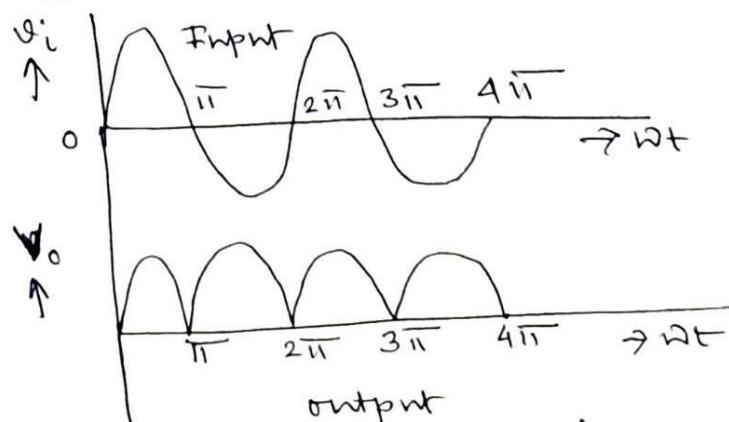
Figure: Full-Wave rectifier

It uses two diodes D_1 and D_2 . The transformer secondary winding has a tapping in the centre. The load resistance R_L is connected between the centre tap and the junction of the cathodes of the two diodes.

During the +ve half cycle of the input, D_1 conducts, D_2 does not conduct.

During the -ve half cycle, D_1 does not conduct, D_2 conducts.

Thus the diodes D_1 and D_2 conduct on alternate half cycles passing the current through the load in the same direction.



Both halves of the input waveform are available at the output as shown in figure above. Hence this circuit is called a full wave rectifier.

$$i_{L_1} = I_m \sin \omega t \text{ for } 0 \leq \omega t \leq \pi$$

$$i_{L_2} = I_m \sin \omega t \text{ for } \pi \leq \omega t \leq 2\pi$$

Thus average value of the current

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i_L d(\omega t)$$

The load current $i_L = i_{L_1} + i_{L_2}$

$$\begin{aligned} \therefore I_{dc} &= \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t d(\omega t) \\ &= \frac{I_m}{\pi} \left[-\cos \omega t \right]_0^{\pi} \\ &= \frac{2 I_m}{\pi} \end{aligned}$$

The output dc voltage across the load $V_{dc} = I_{dc} \cdot R_L$

$$= \frac{2 I_m}{\pi} \times R_L$$

$$= \frac{2 V_m}{\pi}$$

$$I_{rms} = \sqrt{\frac{1}{\pi} \int_0^{\pi} i_L^2 d(\omega t)}$$

$$\text{We get finally } I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\text{and } V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\text{Hence ripple factor } \delta = \sqrt{\left(\frac{I_{rms}}{I_{dc}} \right)^2 - 1}$$

$$= \sqrt{\left(\frac{(I_m/\sqrt{2})}{(2 I_m/\pi)} \right)^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.482$$

which is lower as compared to a half wave rectifier.
Therefore, full wave rectifier is a good rectifier.

Efficiency

As before,

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times (R_L + R_f)}$$

Substituting all the values

$$\eta = \frac{0.812}{1 + R_f/R_L}$$

If R_f is negligible, $\eta = 0.812$.

Thus, the maximum efficiency obtainable for a full wave rectifier is 81.2%.

Advantages

- 1) The dc output is twice that of half-wave rectifier
- 2) δ is very low
- 3) η is twice that of half wave rectifier

Ap

Disadvantages

- 1) Requirement of centre tapped transformer makes it expensive
- 2) PIV is twice that of half wave rectifier.

Problem In a half wave rectifier the secondary voltage of the transformer is 80V. If the value of load resistance used is 20Ω , calculate i) dc voltage across the resistor, ii) the PIV and iii) the dc current, iv) power delivered to load and v) efficiency.

Problem In a centre tapped full-wave rectifier the step down transformer has a turns ratio of primary to secondary as $10:1$. If primary voltage is 230V, calculate
i) dc output voltage
ii) PIV and
iii) Rectification efficiency for a load resistance of 100Ω assuming ideal diodes.

Bridge Rectifier

Full-Wave rectification is also achieved with the aid of a bridge circuit employing four diodes as shown in figure below:

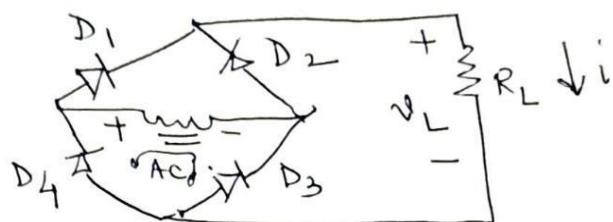


Figure: Bridge rectifier circuit

In the circuit, only two diodes in the opposite arms of the bridge conduct simultaneously while the other two diodes remain off.

V_L is unidirectional with the polarity as marked in the figure.

Peak Inverse Voltage

The PIV is the maximum reverse voltage to which the diode is subjected when it is non conducting.

To avoid a possible damage, the diode must not be subjected to a PIV not exceeding its rated value.

In a half wave rectifier, the PIV is the maximum voltage appearing across the transformer secondary.

In a full-wave rectifier, the PIV for each diode is found to be twice the maximum voltage between the centre tap and either end of the transformer secondary. In a bridge circuit, the PIV is the maximum voltage of the transformer secondary.

Comparison between a full-wave and a bridge rectifier

(A) Advantages of the bridge rectifier

- i> A transformer without a centre tap can be used.
- ii> A bridge circuit requires a smaller transformer than that needed by a full-wave rectifier giving the same dc output voltage.
- iii> PIV rating of a diode in a bridge rectifier is half that for a full-wave rectifier circuit yielding the same dc output voltage. The bridge circuit is therefore suitable for high voltage applications.

(B) Disadvantages of the bridge rectifier

- i> It uses four diodes whereas a full-wave rectifier uses two.
- ii> Bridge circuit is not efficient for low voltages.

Problem: A bridge rectifier feeds a load resistance of $2500\ \Omega$ from a 100V (rms) supply. Each diode of the rectifier has a forward resistance of $50\ \Omega$. Calculate
i) the dc load voltage
ii) the ripple voltage at the output.

Problem: In a bridge rectifier if the diodes are ideal, determine
a) dc output voltage
b) PIV and
c) output dc current for $R_L = 100\ \Omega$
and the step down transformer has turns ratio of 10:1. The mains voltage at the input is 230V at 50 Hz.

Filter circuit

The output of a rectifier is not a pure dc but a pulsating dc.

That is, the output consists of dc component and ac ripples.

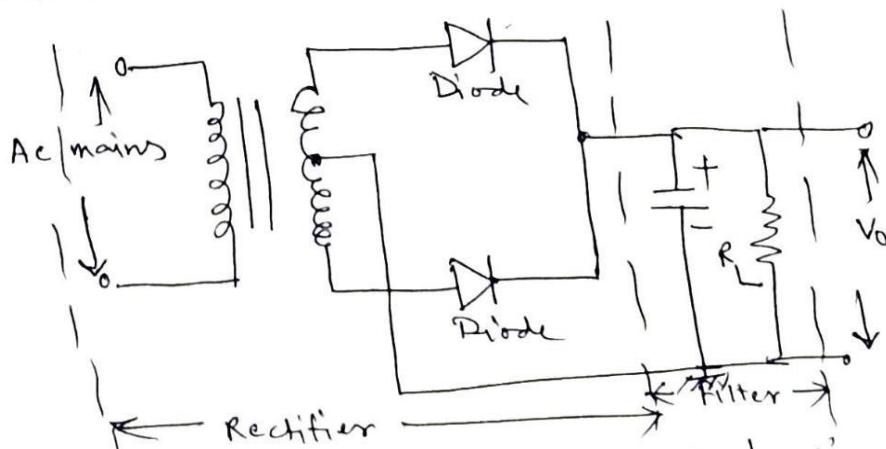
These ac ripples are to be minimized to make smooth dc.

The process of removing or minimizing the ripples in the output is called filtering. The circuit is

called a filter.

Shunt Capacitor filter

The simplest among several types of filter circuits is a capacitor filter. A high value of capacitor is connected across the load.



The capacitor offers a path of low reactance ($1/wC$) to the ac components.

Thus all the ac components are bypassed through the capacitor. Only the dc component flows through the load R_L .

Ripple equation for shunt capacitor filter

The ripple factor for a full-wave rectifier with capacitor filter is

$$\delta = \frac{1}{4\sqrt{3} + R_L C}$$

f = frequency of the ac input

R_L = Load resistance

C = filter capacitance

Hence, by using larger value of C we can reduce the ripple factor.

Problem:- In a half wave rectifier fed from 230V, 50 Hz mains, it is desired to have a ripple factor of 0.005. Estimate the value of capacitor needed if the load current $I_L = 0.5\text{ A}$.

Problem:- A full-wave rectifier is operated from a 50 Hz mains line and has a filter capacitor connected across its output. Calculate the value of capacitance required for a load of 200Ω such that the ripple at the output is $\leq 4\%$.

TRANSISTOR

A transistor is a solid state version of a vacuum tube triode. It consists of a single crystal semiconductor (e.g. germanium or silicon) in which a p-type thin layer is sandwiched between two n-type layers. The resulting structure is an n-p-n transistor.

A transistor may also contain an n-type layer between two p-type layers, the resulting structure is a p-n-p transistor.

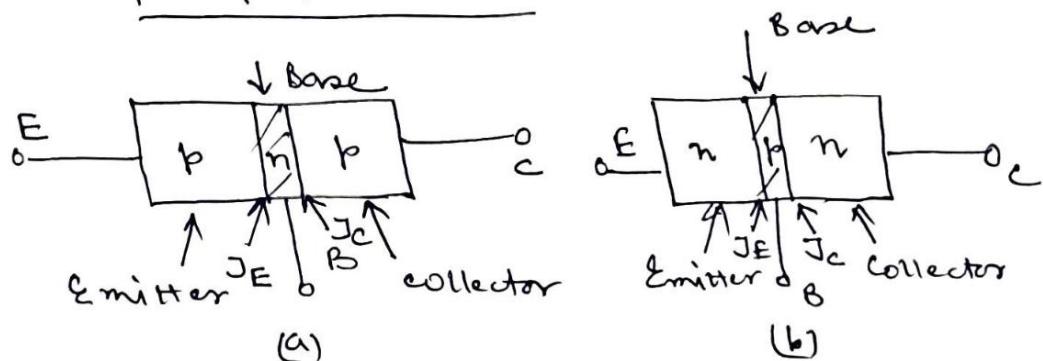


Figure: Bipolar junction transistors
(a) p-n-p (b) n-p-n

$J_E \rightarrow$ Emitter base junction
(emitter junction)

$J_C \rightarrow$ Collector - base junction
(Collector junction)

Since both the majority and the minority carriers are involved in junction transistors, these devices are termed bipolar junction transistors (BJT), bipolar transistors or bipolar devices.

In the normal transistor operation

- the emitter-base junction is forward biased and
- the collector-base junction is reverse biased.

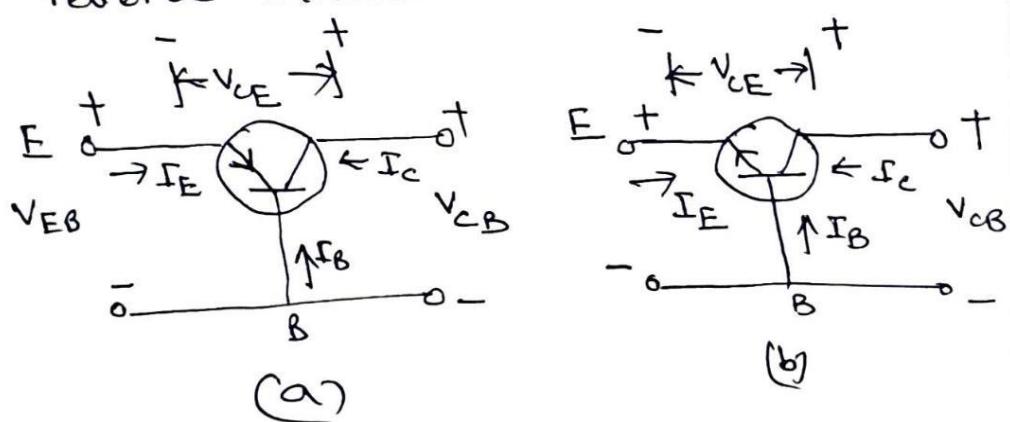


Figure: Circuit symbols with reference current directions and voltage polarities for (a) a p-n-p and (b) an n-p-n transistor

Table: Signs of currents and voltages
for normal transistor operation

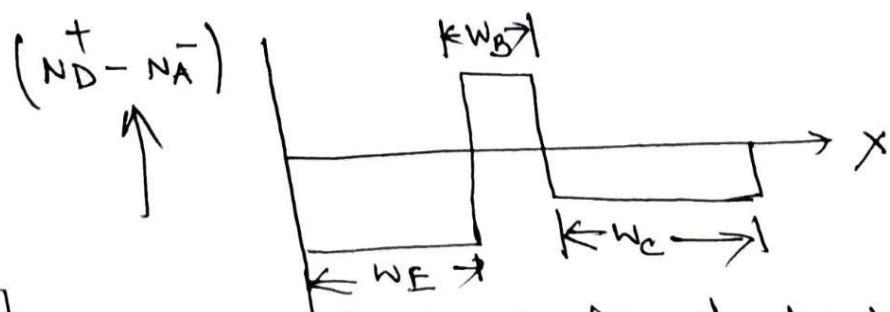
transistor type	I_E	I_B	I_C	V_{EB}	V_{CB}	V_{CE}
p-n-p	+	-	-	+	-	-
n-p-n	-	+	+	-	+	+

Transistor Manufacturing Techniques

- i) Growth technique
- ii) Alloy or fused technique
- iii) Diffusion technique
and
- iv) Epitaxial technique

The doping of the emitter
section > Collector section.

The base region is
oppositely doped at a level intermediate
between the emitter and the collector.



43

figure: Doping profile of a p-n-p transistor.

N_D^+ → Concentrations of ionized donor

N_A^- → concentrations of ionized acceptors.

x → the distance through the transistor from the emitter end.

w_B → width of the base
(typically few micrometers)

w_E → width of the emitter

w_C → width of the collector

(few millimeters or less)

Transistor Amplifier

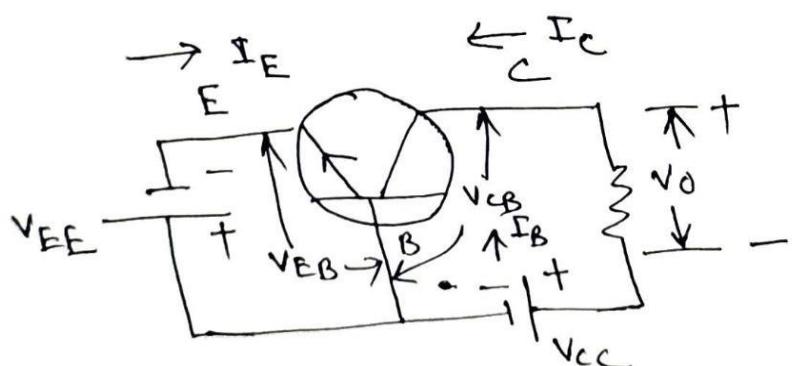


Figure: An n-p-n transistor with bias voltages and a load resistance

$$\Delta V_O = -R_L \Delta I_C \dots \text{ (1)}$$

ΔV_O = voltage drop across the load resistance

$$\Delta V_i = r_e \Delta I_E \quad \dots (2)$$

ΔV_i = Input voltage

r_e = dynamic resistance of the emitter junction

$$\text{Voltage gain } A_v = \frac{\Delta V_o}{\Delta V_i}$$

$$= - \frac{R_L \Delta I_C}{r_e \Delta I_E} \quad \dots (3)$$

A_I = Current gain of the transistor

$$= - \frac{\Delta I_C}{\Delta I_E}$$

The signs of I_C and I_E being opposite, A_I is positive.

Thus A_v is positive

i) A_I is slightly less than unity

ii) R_L can be much larger than r_e

iii) A_v is much larger than unity giving a voltage amplification.

As an example

$$\text{If } A_I = - \left(\frac{\Delta I_C}{\Delta I_E} \right) = 0.98$$

$$R_L = 3000 \Omega$$

$$r_e = 30 \Omega$$

Equation (3) gives $A_v = 98$.

$$\begin{aligned}
 \text{Power gain } A_p &= \frac{\text{output power}}{\text{input power}} \\
 &= \left\{ \frac{\Delta I_C}{\Delta I_E} \right\}^2 \frac{R_L}{r_e} \\
 &= A_I A_V \quad \dots (4)
 \end{aligned}$$

Modes of Transistor operation

- i) Common-base (CB) mode
- ii) Common-emitter (CE) mode
- iii) Common-collector (CC) mode

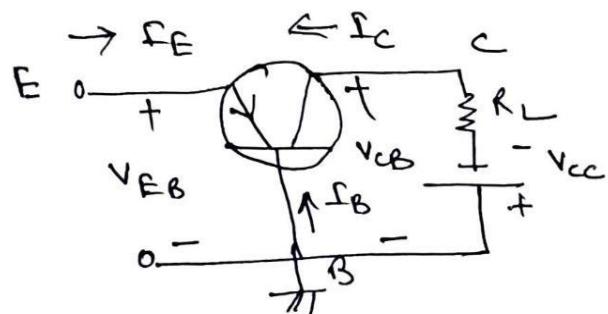


Figure: P-n-p transistor (CB Configuration)

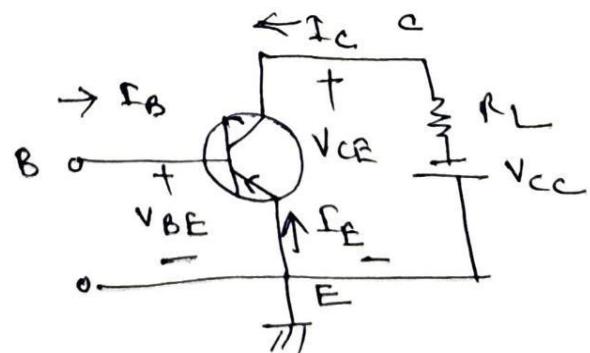


Figure: P-n-p transistor
(CE Configuration)

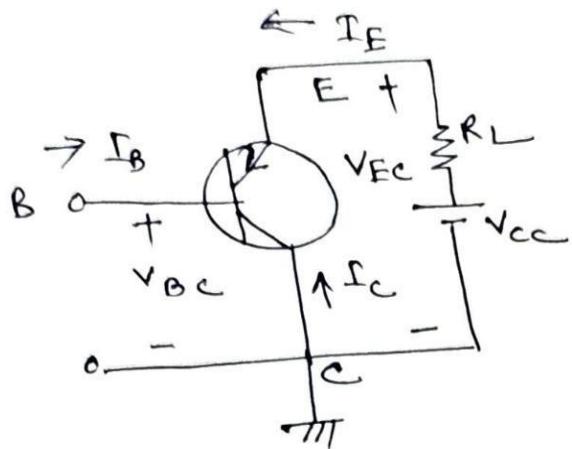


Figure: p-n-p transistor (cc Configuration)

Static characteristics of a Transistor

It gives the graphical forms of relationships among the different Current and voltage variables of the transistor.

Two sets of characteristic curves are ~~are~~

i) Input characteristics
and

ii) Output characteristics

The input characteristics refers to the plot of the input current vs. the input voltage with the output voltage as a parameter

The output characteristics →

plot of the output current vs. the output voltage with the input current as a parameter

i) C-B. characteristics

(a) Input characteristics

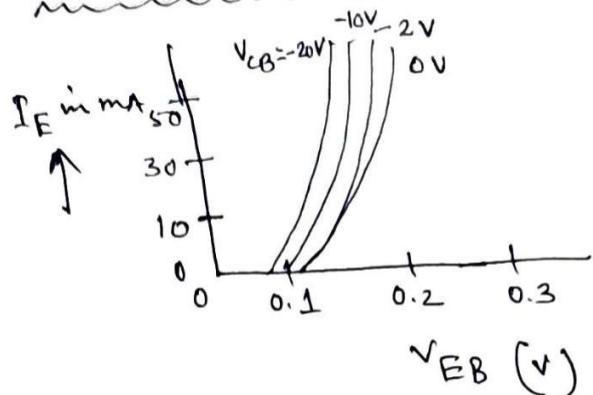


Figure: CB input characteristics
of a typical p-n-p transistor

The change of the effective base width by the collector voltage is termed the "Early effect".

Below a certain voltage V_T , called the cut in, off set or threshold voltage of the transistor, the emitter current is very small. Usually, $V_T = 0.1 \text{ V}$ for Ge transistors and $V_T = 0.5 \text{ V}$ for Si transistors.

(b)

output characteristics

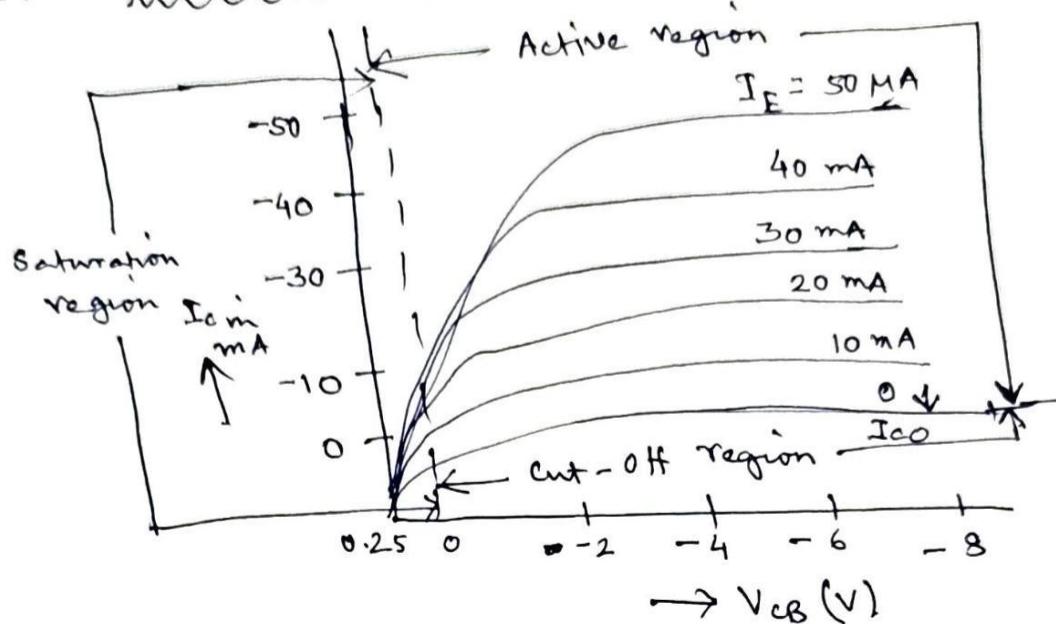


figure: CB output characteristics
of a typical p-n-p transistor

The output characteristics can be divided into three distinct regions

i) Active region:- The normal operating region of a transistor used as an amplifier. Here, the emitter junction is forward biased and the collector junction is reverse biased.

ii) Saturation region:- Here both the emitter and the collector junctions are forward biased.

iii) Cut-off region:- Here, both the emitter and the collector junctions are reverse biased.

(ii) C. E. characteristics

(a) Input characteristics

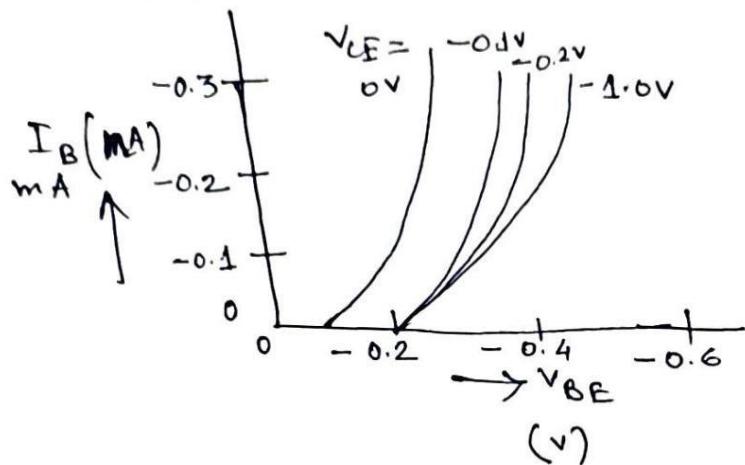


Figure: CE input characteristics
for a typical p-n-p transistor

(b) Output characteristics

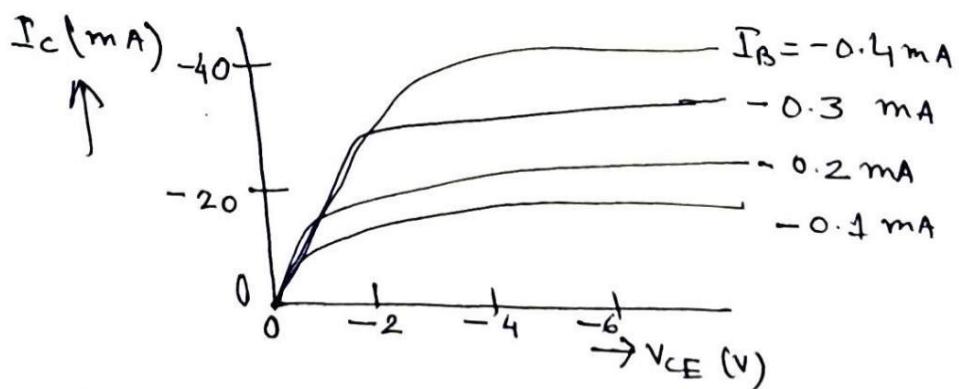


Figure: CE output characteristics
of a typical p-n-p transistor

Expressions for currents

When the emitter is forward biased

$$I_C = I_{C0} - \alpha I_E$$

$$\text{or } \alpha = -\frac{I_C - I_{C0}}{I_E}$$

$\alpha \rightarrow$ dc current gain of a C.B. transistor

Since I_C and I_E have opposite signs for a given transistor, α is always positive. α lies between 0.95 and 0.995.

Since $I_{C0} \ll I_C$,

$$\alpha = -\frac{I_C}{I_E}$$

$$\alpha' = -\frac{\Delta I_C}{\Delta I_E} / V_{CB} = \text{constant}$$

α' = Small signal short circuit current transfer ratio (or gain) of a transistor in the C.B. mode

For a good transistor $\alpha' = \alpha$

$$\beta = \frac{I_C}{I_B}$$

(or h_{FE}) = maximum current gain of a transistor operated in the C.E. mode

Commercial transistors have values of h_{FE} in the range from 20 to 200.

$$\beta' \text{ (or } h_{FE}) = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{constant}}$$

= Small signal short circuit current gain

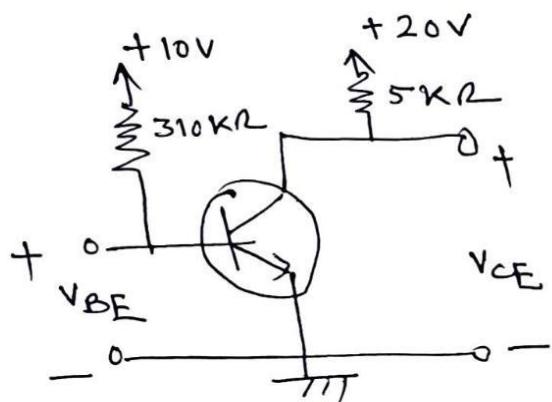
Usually β' differs from β by less than 20%.

$$\text{We have, } \beta' = \frac{d}{1-d}$$

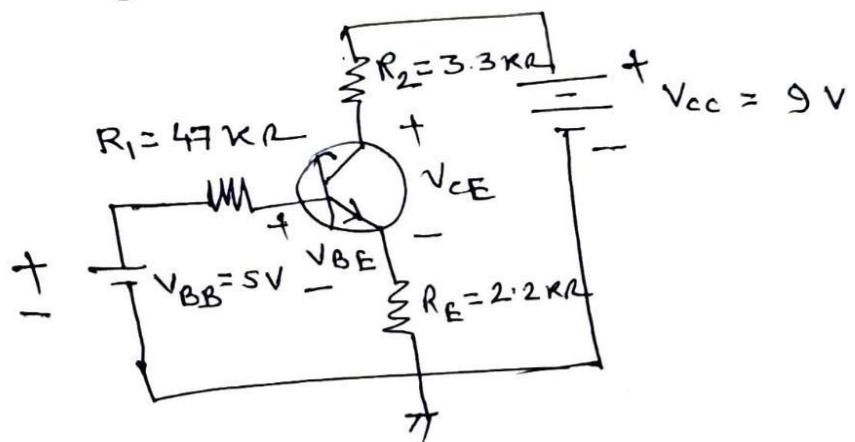
Problem A transistor having $d=0.99$ is used in C.B. amplifier. If the load resistance is $4.5 \text{ k}\Omega$ and the dynamic resistance of the emitter junction is 50Ω , find the voltage gain and power gain.

Problem: An n-p-n transistor with $d=0.98$ is operated in the C.B. configuration. If the emitter current is 3 mA and the reverse saturation current is $I_{CO} = 10 \text{ }\mu\text{A}$, what are the base current and the collector current?

Problem A transistor operating in the CE mode (figure below) draws a constant base current of 30 mA. The collector current is found to change from 3.5 mA to 3.7 mA when the collector-emitter voltage changes from 7.5 V to 12.5 V. Calculate the output resistance and β at $V_{CE} = 12.5$ V. What is the value of α ? Calculate V_{CE} if $\beta = 125$ assuming $V_{BE} = 0.6$ V



Problem:- Refer to the circuit of figure below. At saturation V_{BE} and V_{CE} are $V_{BE, Sat} = 0.85\text{V}$ and $V_{CE, Sat} = 0.22\text{V}$. If $h_{FE} = 110$, is the transistor operating in the saturation region?



Transistor biasing

The purpose of dc biasing of a transistor is to obtain a certain dc collector current at a certain dc collector voltage. These values of current and voltage are expressed by terms operating point (quiescent point or Q-point).

To obtain the operating point, we make use of some circuits and these circuits are called biasing circuits.

Load line and operating point

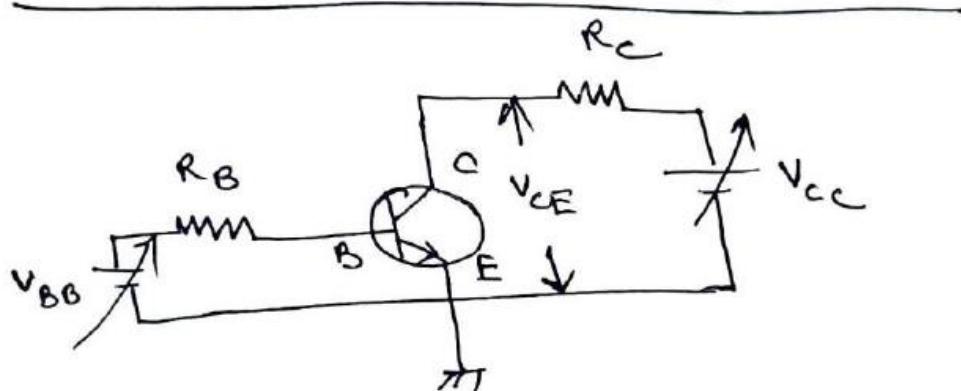


Figure: Transistor in CE Configuration

I_C = Collector Current

V_{CE} = Collector to emitter voltage

R_B and R_C = resistances connected to base and collector respectively

V_{BB} and V_{CC} = bias voltages

Applying KVL

$$V_{CE} = V_{CC} - I_C R_C$$

$$\therefore I_C = \frac{V_{CC}}{R_C} - \left(\frac{1}{R_C} \right) V_{CE}$$

on the x-axis, $I_C = 0$

$$\therefore V_{CE} = V_{CC}$$

$$\text{Thus } A = (V_{CC}, 0)$$

This represents the maximum collector emitter voltage.

At point B, $V_{CE} = 0$

$$\therefore I_C = \left(\frac{V_{CC}}{R_C} \right)$$

$$\text{Thus } B = \left(0, \frac{V_{CC}}{R_C} \right)$$

This represents the maximum collector current that can be obtained for a given load R_C .

Load line the line joining the two points A and B drawn on the output characteristics.

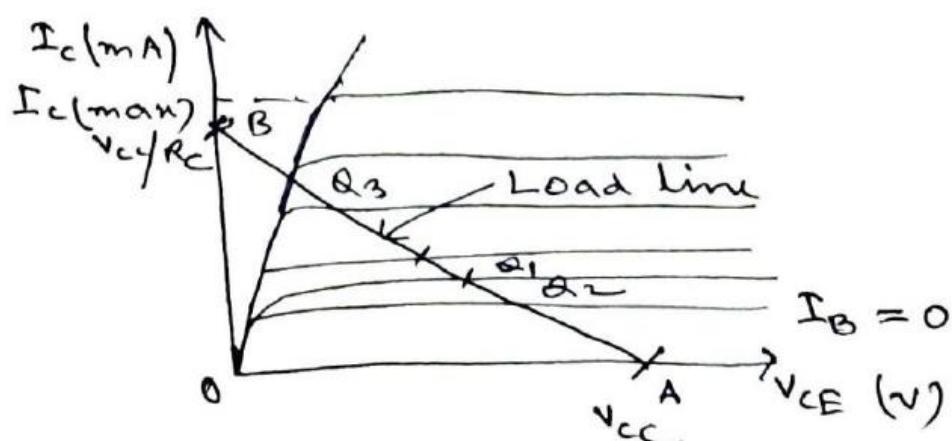


Figure: Load line and operating point

Operating point / Quiescent point

Any point along the load line specifies a collector current and the corresponding collector-emitter voltage and hence it is called an operating point or quiescent point.

i) operating point close to the cut-off ~~saturation~~ region :-

A portion of the negative half cycle of the output voltage is clipped, resulting in distortion.

ii) operating point at the middle of the load line :-

The output is reproduced without distortion.

iii) operating point close to the saturation region :-

Gives clipping at +ve peaks.

Reasons for shift of the operating point

i) Transistor parameters are temperature dependent

ii) Parameters (such as β) change from unit to unit.

Requirement of biasing circuit

- i) Establish the operating point in the centre of active region of the characteristic curve
- ii) Stabilize the collector current against temperature variations
- iii) Make the operating point independent of the transistor used i.e., replacement by the same type is possible.

Stability Factor

$$S = \frac{\Delta I_C}{\Delta I_{C_0}} \dots \dots (1)$$

(β and V_{BE} constant)

S should be as small as possible.
The lowest value of S is one.

$$S_\beta = \frac{\Delta I_C}{\Delta \beta} \dots \dots (2)$$

(I_{C_0} and V_{BE} constant)

$$S_V = \frac{\Delta I_C}{\Delta V_{BE}} \dots \dots (3)$$

(I_{C_0} and β constant)

$$I_C = (1 + \beta) I_{C_0} + \beta I_B \dots \dots (4)$$

Differentiating eqn(4) w.r.t I_C and assuming β to be constant with I_C

$$I = (1+\beta) \frac{d I_C}{d I_C} + \beta \frac{d I_B}{d I_C}$$

$$\Rightarrow S = \frac{\beta + 1}{1 - \beta \frac{d I_B}{d I_C}} \quad \dots (5)$$

$\frac{d I_B}{d I_C}$ depends upon the type of biasing arrangement.

For any fixed bias circuit $\frac{d I_B}{d I_C} = 0$

$$\Rightarrow S = \beta + 1 \quad \dots (6)$$

$$\text{If } \beta = 40, S = 41$$

Thus fixed bias operation is extremely undesirable from the consideration of operating point stability.

Expression for "S_B"

Differentiating eqn(4) w.r.t I_C and considering I_{C0} to be constant

$$I = I_{C0} \frac{d\beta}{d I_C} + \beta \frac{d I_B}{d I_C} + I_B \frac{d\beta}{d I_C}$$

$$\text{or } \frac{d\beta}{d I_C} [I_{C0} + I_B] = 1 - \beta \frac{d I_B}{d I_C}$$

$$\text{Thus } S_B = \frac{d I_C}{d\beta} = \frac{I_{C0} + I_B}{1 - \beta \frac{d I_B}{d I_C}} \quad \dots (7)$$

For fixed bias $\frac{dI_B}{dI_C} = 0$

$$\Rightarrow S_P = I_{C0} + I_B \quad \dots (8)$$

Collector to base bias

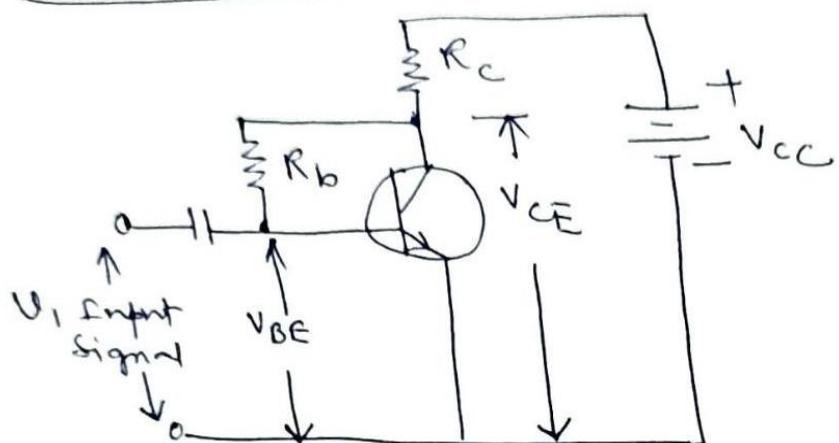


Figure: CE n-p-n amplifier with collector to base bias

Applying KVL to the above circuit

$$V_{CC} = R_C (I_B + I_C) + I_B R_b + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_b} \quad \dots (9)$$

Voltage V_{BE} is almost independent of I_C .

Hence differentiating eqn.(9) w.r.t I_C

$$\frac{dI_B}{dI_C} = - \frac{R_C}{R_C + R_b} \quad \dots (10)$$

Substituting this value of $\frac{dI_B}{dI_C}$ into eqn.(5)

$$S = \frac{\beta + 1}{1 + \beta \frac{R_C}{R_C + R_b}} \quad \dots (11)$$

Eqn (11) shows that the stability factor here is smaller than $(\beta + 1)$.

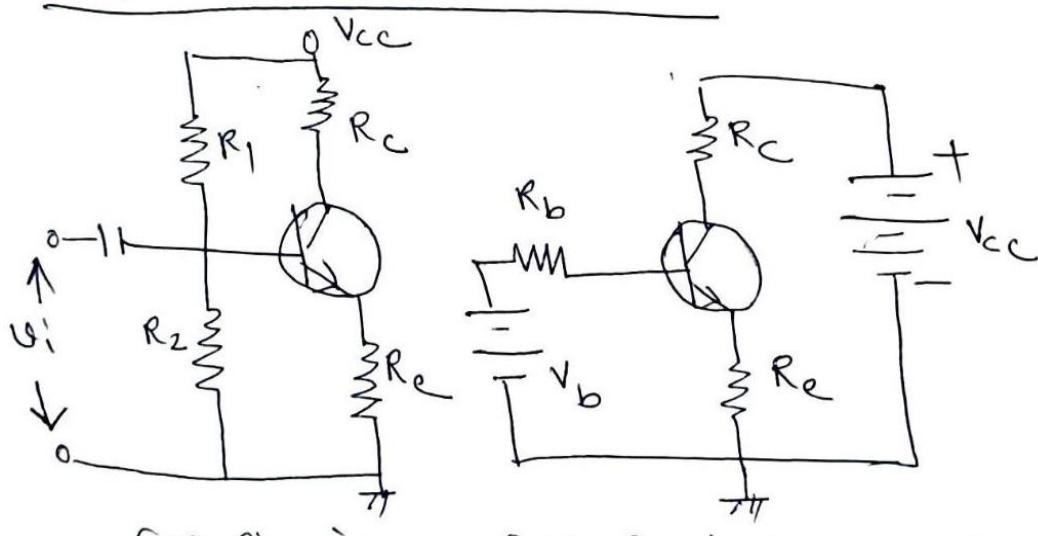
Thus, improvement in the operating point stability results.

We also get

$$S_\beta = \frac{I_{CO} + I_B}{1 + \beta \frac{R_C}{R_C + R_B}} \quad \text{--- (12)}$$

Eqn (12) shows that S_β for this case is much improved over the fixed bias circuit.

Self bias or Emitter bias



(a) Circuit

(b) Equivalent circuit

Figure: CE amplifier with self bias

In case where dc resistance is low (even zero), use of self bias or emitter bias provides good stabilization

Applying Thvenin's theorem to the left in Fig(a), fig(b) is obtained

$$\therefore R_b = \frac{R_1 R_2}{R_1 + R_2}$$

$$\text{and } V_b = \frac{V_{cc} R_2}{R_1 + R_2}$$

$R_b \rightarrow$ the resistance we find looking back from the base terminal.

Application of KVL to the base-emitter circuit gives

$$V_b = I_B R_b + V_{BE} + (I_B + I_C) R_e$$

Differentiating w.r.t I_C

(V_{BE} is almost constant and is independent of I_C)

$$0 = \frac{d I_B}{d I_C} R_b + R_e \left(1 + \frac{d I_B}{d I_C} \right)$$

$$\text{or, } \frac{d I_B}{d I_C} = - \frac{R_e}{R_e + R_b}$$

$$\text{Thus } S = \frac{\beta + 1}{1 + \beta \frac{R_e}{R_e + R_b}}$$

$$\text{As } \beta = \frac{\alpha}{1-\alpha}$$

$$S = \frac{1 + \frac{R_e}{R_b}}{(1-\alpha) + \frac{R_e}{R_b}}$$

For $\frac{R_b}{R_e} \ll 1$

S is unity.

S increases with $\frac{R_b}{R_L}$

and $(\beta + 1)$ for $\frac{R_b}{R_e} \rightarrow \infty$

Problem: A silicon transistor having $\beta = 52$, $V_{BE} = 0.6$ V, $V_{CC} = 24$ Volts and $R_C = 5 k\Omega$ is used in the self bias circuit. The operating point is required to be established at $V_{CE} = 12$ Volts and $I_C = 2$ mA and with stability factor not exceeding 4. Find suitable values of R_E , R_1 and R_2 .

Problem: In the CE amplifier of self bias circuit, $R_1 = 100 k\Omega$, $R_2 = 10 k\Omega$, $R_E = 1 k\Omega$ and $\alpha = 0.98$.

According to manufacturer's data collector reverse saturation current I_{CO} varies from 5 μ A to 25 mA over the working temperature range. Find the variation in collector current I_C when

and 'ii' amplifier is unstabilized and 'ii' stabilizing resistor R_E is used

Problem: In the C.E. Self bias circuit, $f_E = 1 \text{ mA}$, $R_E = 1000\Omega$ and $\alpha = 0.98$. Find out the values of R_1 and R_2 such that the stability factor "S" does not exceed 5. Assume $V_{CC} = 5 \text{ Volts}$, $V_{BE} = 0$

Problem: A Ge transistor having $\beta = 50$ is used in the self bias circuit. If the quiescent operating point is to be $V_{CE} = 6 \text{ V}$ and $I_C = 4 \text{ mA}$, find the values of R_1 , R_2 and R_F when the stability factor is 12. Assume $V_{BE} = 0.2 \text{ V}$, $V_{CC} = 12 \text{ V}$, $R_C = 1 \text{ k}\Omega$.

LCD (Liquid Crystal Display)

It is combination of two states of matter, the solid and the liquid. It uses a Liquid Crystal to produce a visible image.

- * LCDs are Super thin technology display screen.
- * Are generally used in laptop computer screen, TVs, cell phones, portable video games etc.

Advantages of LCD

- * Consumes less power compared to CRT and LED.
- * Consists of some microwatts for display in comparison with some milliwatts for LEDs.
- * These are of low cost and provide excellent contrast.
- * These are thinner and lighter compared to CRT and LED.

Disadvantages of LCD

- * Requires additional light sources.
- * Range of temperature is limited for operation.
- * Less reliability.
- * Speed is very low.
- * Needs an AC drive.

LED (Light Emitting Diode)

- * The LED comes under active semiconductor electronic components.
 - * quite comparable to the normal general purpose diode with the only big difference being its capability to emit light in different colours.
 - * The working principle is based on the quantum theory.
 - * The energy of the photon
- $E_g = h \cdot f$
- h = Plank's Constant
- $f = c/\lambda$
- c = Velocity of light
- λ = wavelength of electromagnetic radiation.
- Thus $E_g = \frac{hc}{\lambda}$

Advantages of LED

- * Cost is less
- * Power consumption can be controlled
- * Energy efficient and long life time

Disadvantages

- * slight excess of voltage / Current can damage the device
- * more expensive on an initial capital cost basis
- * Can shift colour due to age and temperature

Applications

- * Used as bulbs in home and industries, motorcycles and cars, mobile phone display, traffic light signals.