

## Single stage Amplifier

⇒ An amplifier is a circuit, which enhances the voltage, Current or power level of an input signal.

Amplifiers are classified as

1) Small signal amplifiers / voltage amplifiers

2) Large signal amplifiers / power amplifiers.

⇒ Based on the choice of the operating point on the load line, power amplifiers are again classified as

Class A, Class B, Class AB and Class C amplifiers.

## CE Amplifier

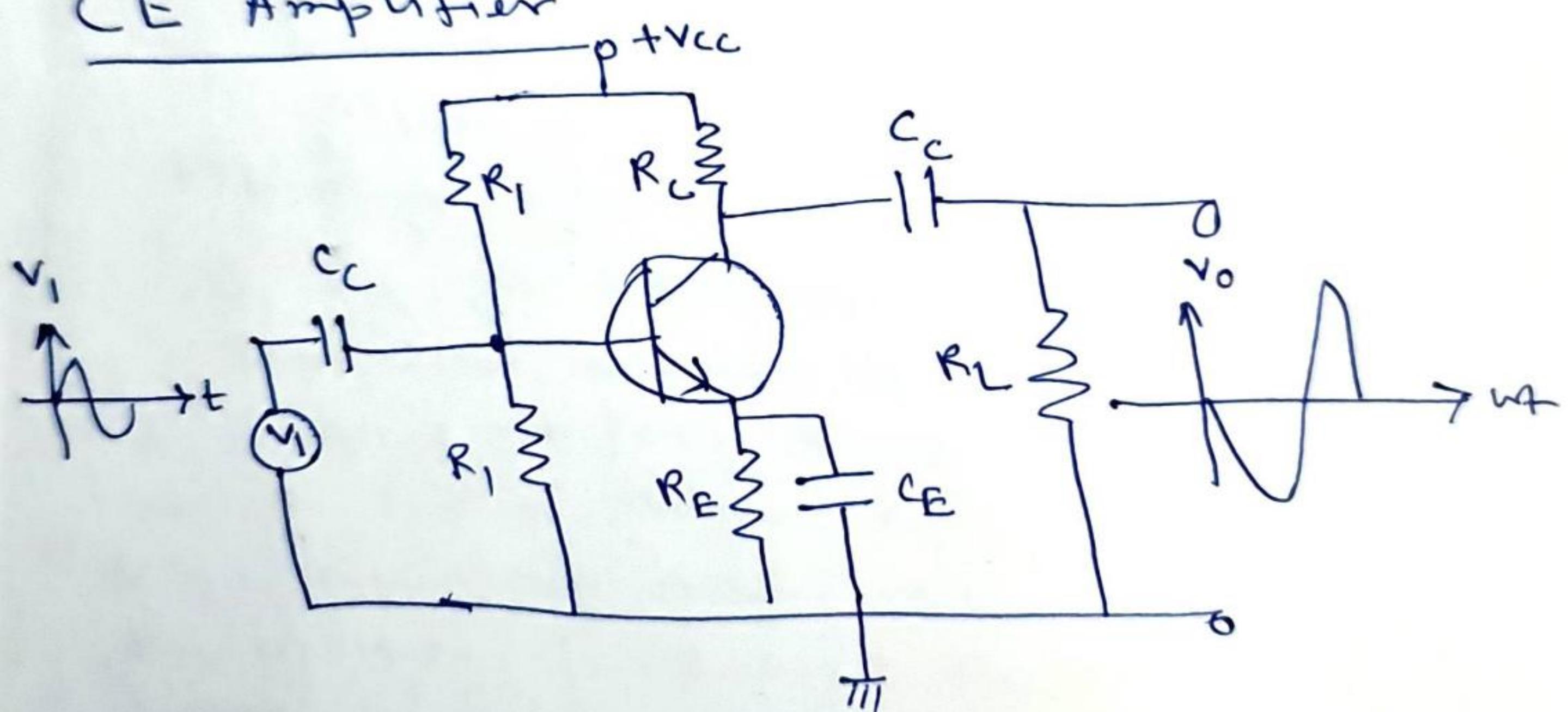


Figure: Common Emitter Amplifier

$R_1$  &  $R_2 \Rightarrow$  Act as a voltage divider

Supply Voltage  $\Rightarrow V_{cc}$  divides among the two resistors

$\Rightarrow$  Voltage across  $R_2$  forward biases the EB junction

$\Rightarrow$  Voltage across  $R_1$  reverse biases the CB junction

$\Rightarrow$  Hence the device is made to work in active region.

$C_c \Rightarrow$  Coupling Capacitor

$\Rightarrow$  Prevents DC voltages from the transistor reaching the source

$\Rightarrow$  Allows only AC signal from the input (source) to reach the base of the transistor.

Thus, it prevents the change in operating point.

$\Rightarrow C_E$  is called emitter bypass capacitor because it prevents the AC signal to pass through  $R_E$  otherwise the AC signal through  $R_E$  gets fed back to the input and alters the output. Thus the presence of  $C_E$  across  $R_E$  makes the emitter to be at ground for AC signals.

## Class - A operation

In Class A amplifier, the output current flows through the load for the entire  $360^\circ$  of the input cycle. The operating point is in the middle of the load line as shown in figure

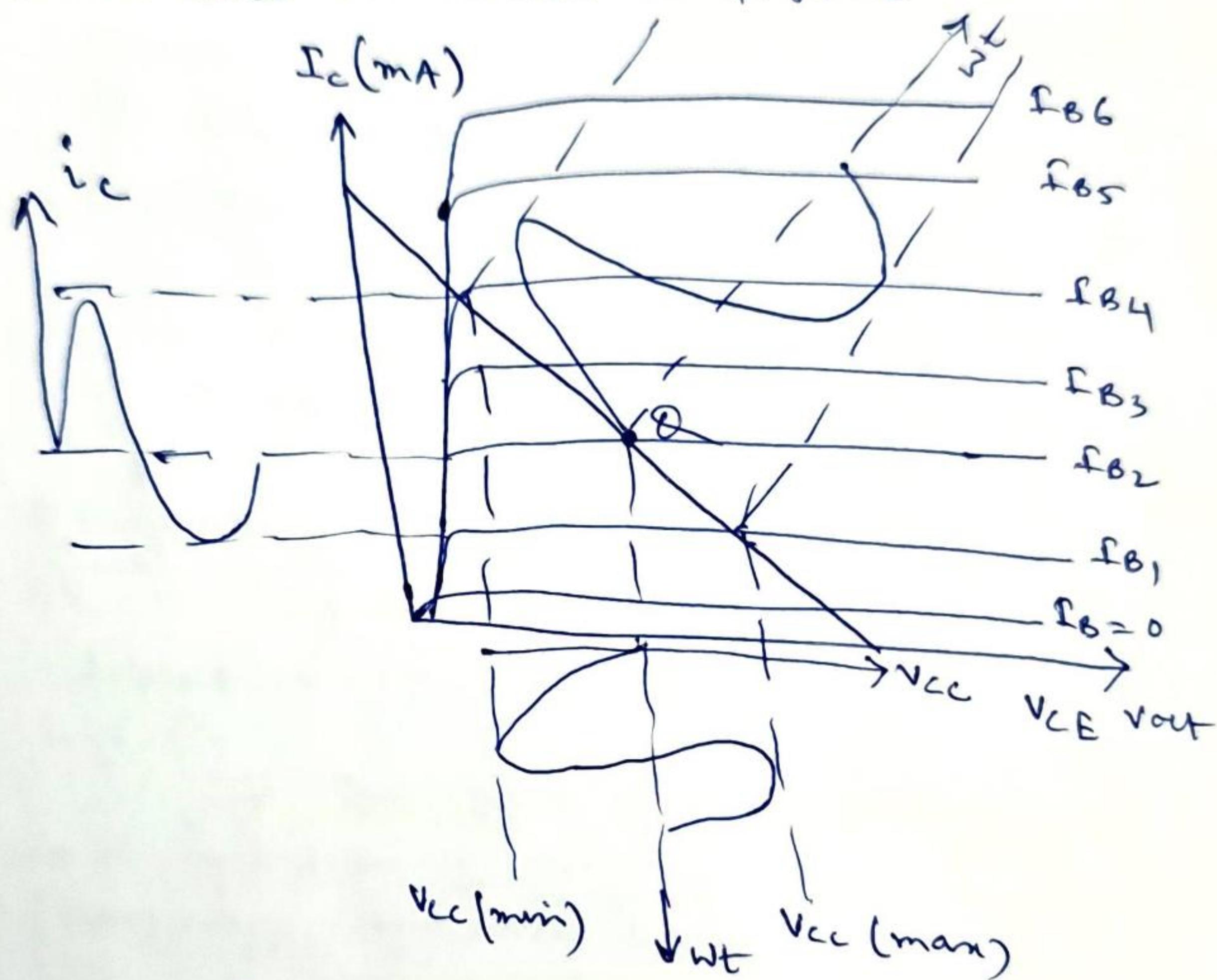


Figure: class A operation

$$A_v = \frac{v_o}{v_i} = \frac{v_{ce}(\text{max}) - v_{ce}(\text{min})}{v_i(\text{max}) - v_i(\text{min})}$$

$$A_i = \frac{i_o}{i_i} = \frac{i_c(\text{max}) - i_c(\text{min})}{i_b(\text{max}) - i_b(\text{min})}$$

$$A_p = \frac{P_o}{P_i}$$

$$= \frac{U_o \cdot I_o}{V_i \cdot I_i}$$

$$= A_v \cdot A_i$$

In a CF amplifier,  $i_c \gg i_b$

Hence  $A_i \gg 1$

$\Rightarrow$  Also output AC voltage is greater than the input AC voltage

$\therefore A_v \gg 1$

$\Rightarrow$  Since  $A_p = A_v \cdot A_i$

$\Rightarrow A_p \gg 1$ .

### Frequency response

$\Rightarrow$  Gain of the amplifier is dependent on the frequency of the input signal.

$\Rightarrow$  The plot of the voltage gain as a function of the frequency is called the frequency response curve.

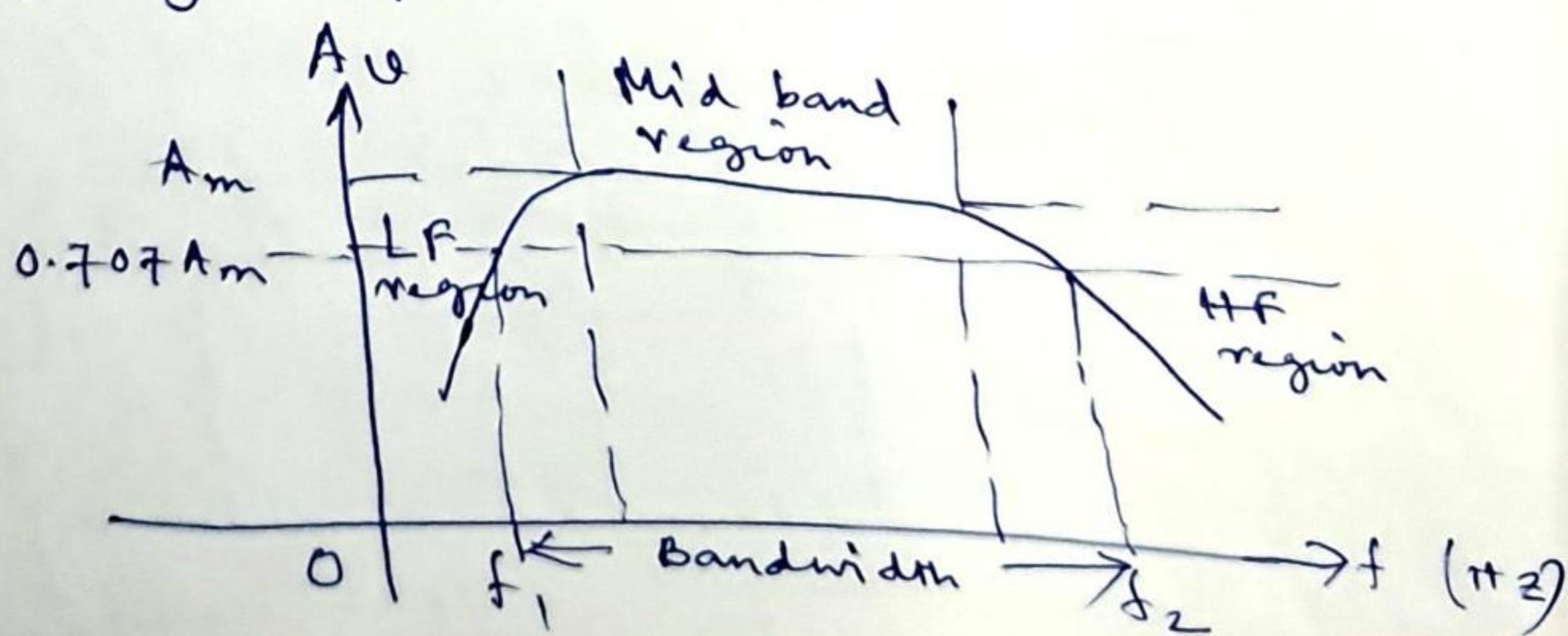


Figure: Frequency response curve

$$\text{Bandwidth} = (f_2 - f_1) \text{ Hz}$$

## Feedback Amplifier

The process of injecting a fraction of output energy of some device and back to the input is known as feedback.

The network used to derive a portion of the output voltage or current is called feedback network.

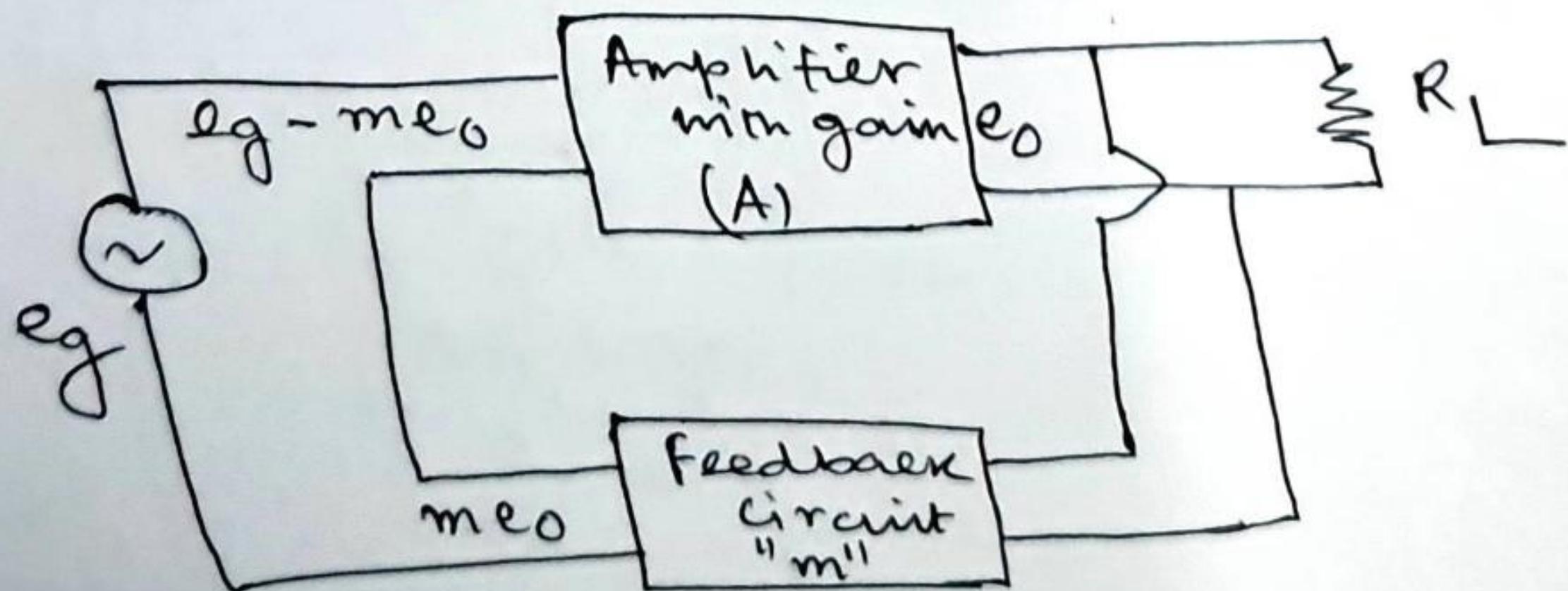
Feedback

- Positive feedback
- Negative feedback

+ve feedback  $\Rightarrow$  Feedback signal is in phase with the input signal

-ve feedback  $\Rightarrow$  Feedback signal is out of phase with the input signal

## Gain of negative feedback amplifier



$$A(\text{eg} - \text{meo}) = e_0$$

$$\therefore A_{\text{eg}} - A_{\text{meo}} = e_0$$

$$\Rightarrow e_0(1 + A_m) = A_{\text{eg}}$$

$$\Rightarrow \frac{e_0}{\text{eg}} = \frac{A}{1 + A_m}$$

$$\therefore A_{\text{fb}} = \frac{A}{1 + A_m}$$

For +ve feedback

$$A_{\text{pf}} = \frac{A}{1 - A_m}$$

Problem: The overall gain of a multistage amplifier is 140. When negative feedback is applied, the gain is reduced to 17.5. Find the fraction of the output that is fed back to the input.

Advantages of negative feedback

i) Gain stability:

$$A_{\text{fb}} = \frac{A}{1 + A_m}$$

$$A_m \gg 1;$$

$$A_{\text{fb}} = \frac{A}{A_m}$$

$$= \frac{1}{m}$$

Thus the gain of the amplifier is extremely stable.

ii) Reduces non linear distortion

$$D_{fb} = \frac{D}{1 + A_m}$$

iii) Improves frequency response

Voltage gain of the amplifier  
is independent of signal frequency.

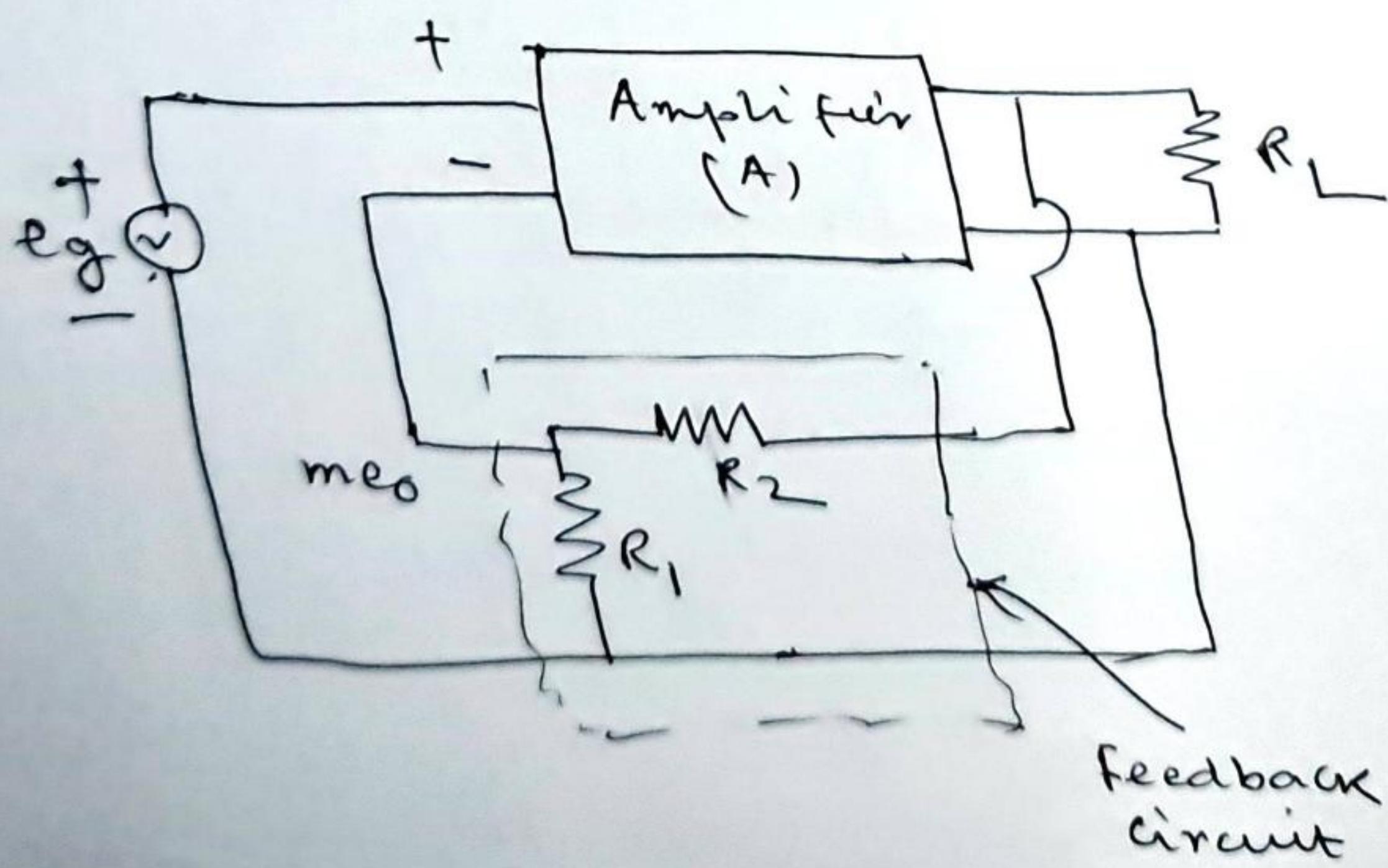
iv) Increases input impedance

$$Z_{in}' = Z_{in} (1 + A_m)$$

v) Decreases output impedance

$$Z_{out}' = \frac{Z_{out}}{1 + A_m}$$

Feedback circuit

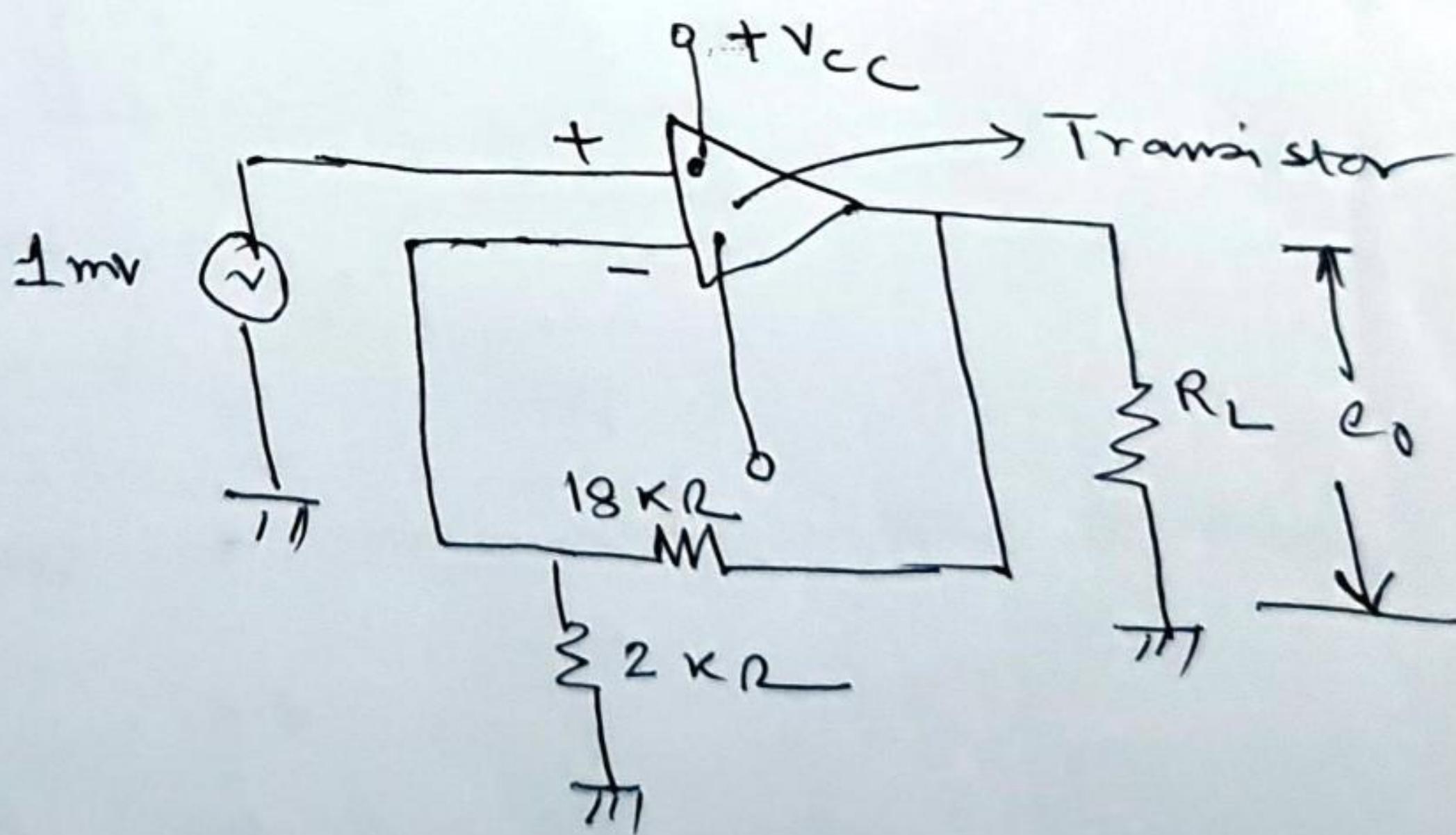


Voltage across  $R_1$ ,

$$= \left( \frac{R_1}{R_1 + R_2} \right) e_o$$

$$\therefore m = \frac{R_1}{R_1 + R_2}$$

Problem: Figure shows the negative feedback amplifier. If the gain of the amplifier without feedback is 10,000, find  
i) feedback fraction  
ii) overall voltage gain  
iii) output voltage if input voltage is 1 mV



## Junction Field-Effect Transistor (JFET)

→ uniformly doped semiconductor bar with ohmic contacts at both ends and with semiconductor junctions on both sides of the bar.

→ Semiconductor bar

n-type material → n-channel FET

p-type material → p-channel FET

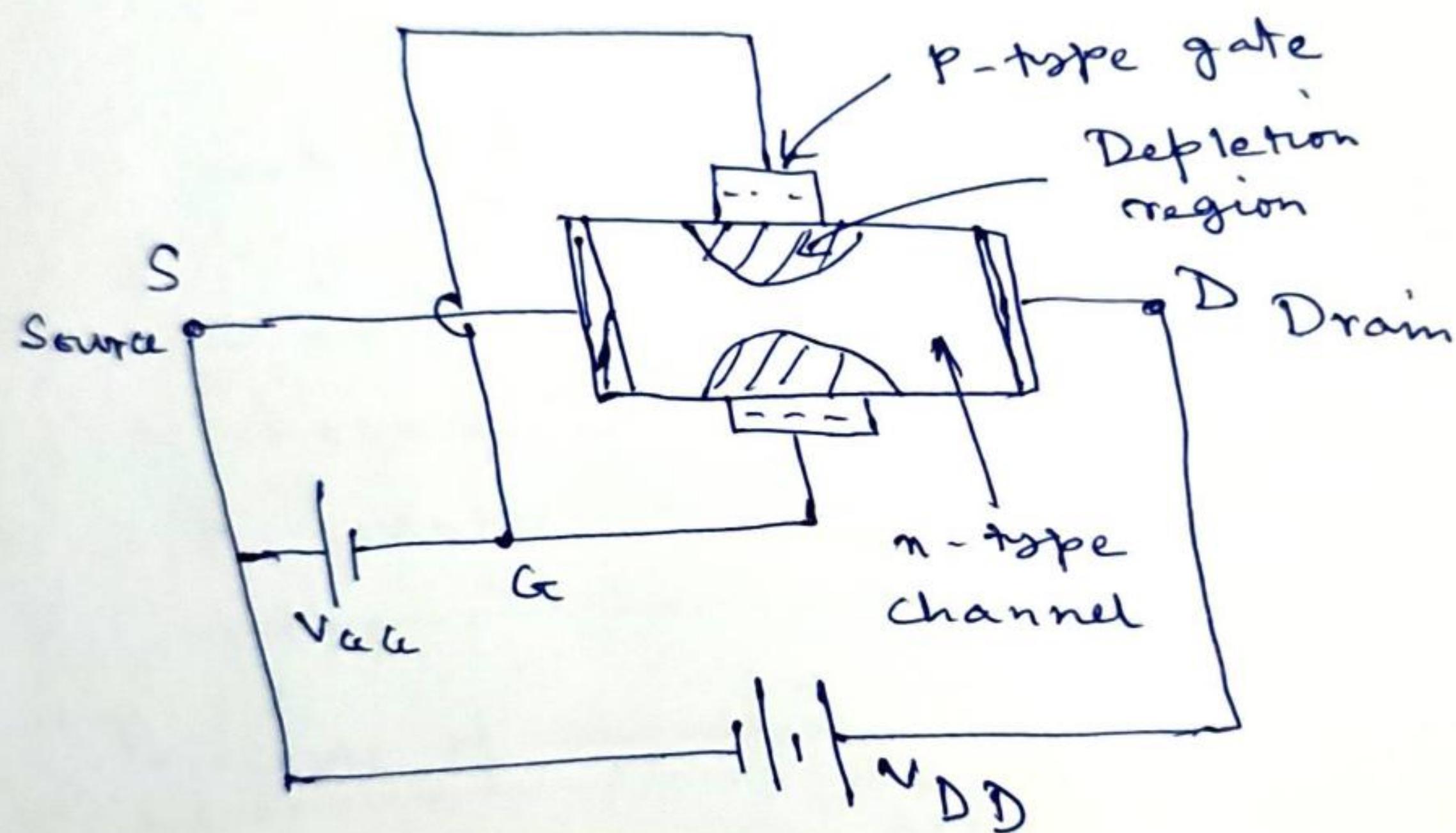


figure: A junction field-effect transistor

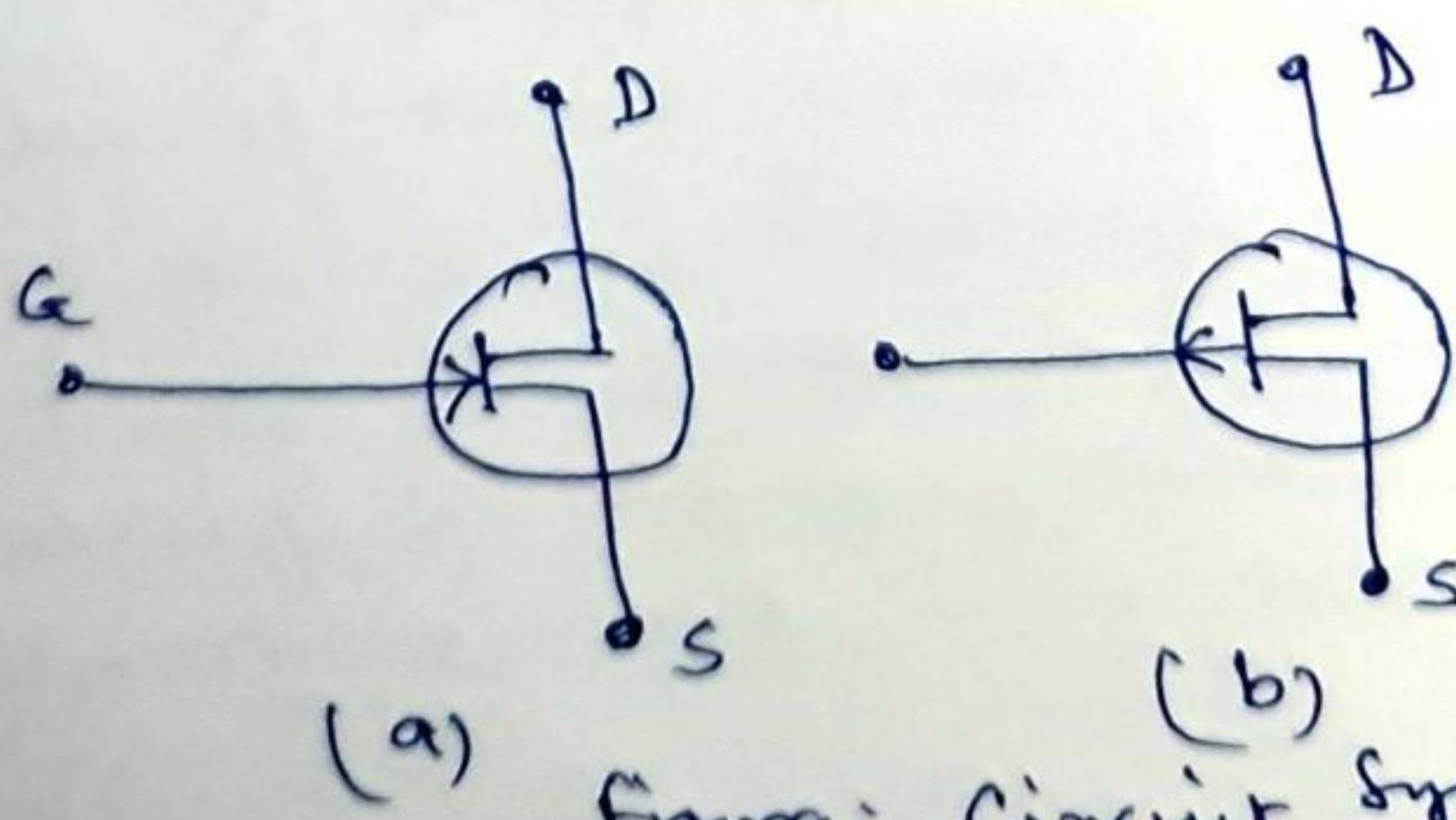


figure: Circuit symbols for  
(a) n-channel FET  
(b) p-channel FET

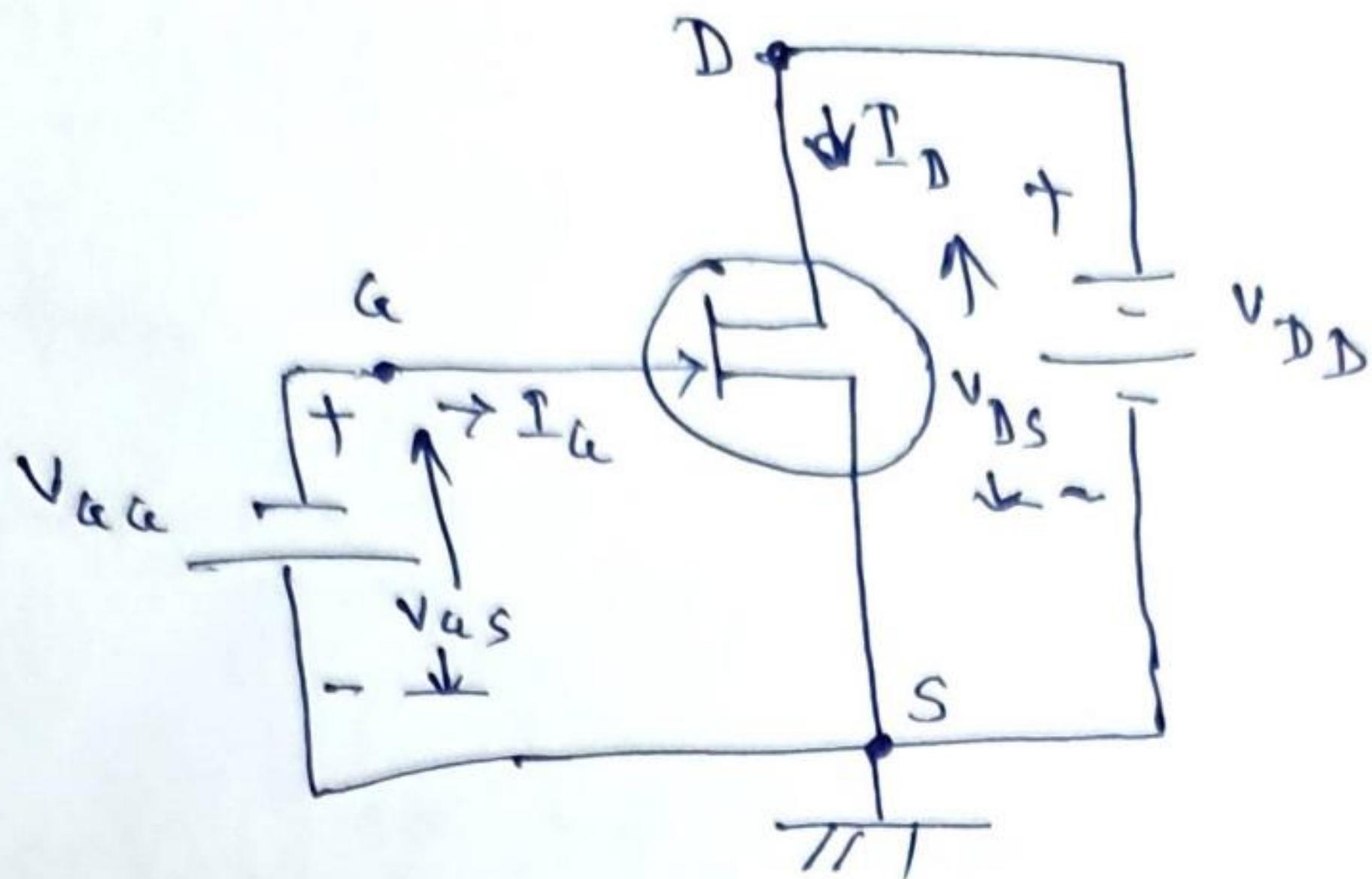


figure: Schematic diagram of an n-channel FET

	$I_D$	$I_G$	$V_{DS}$	$V_{GS}$
n-channel	+	-	+	-
p-channel	-	+	-	+

### Principle of operation.

⇒ when the junction between the gate and the source is reverse biased

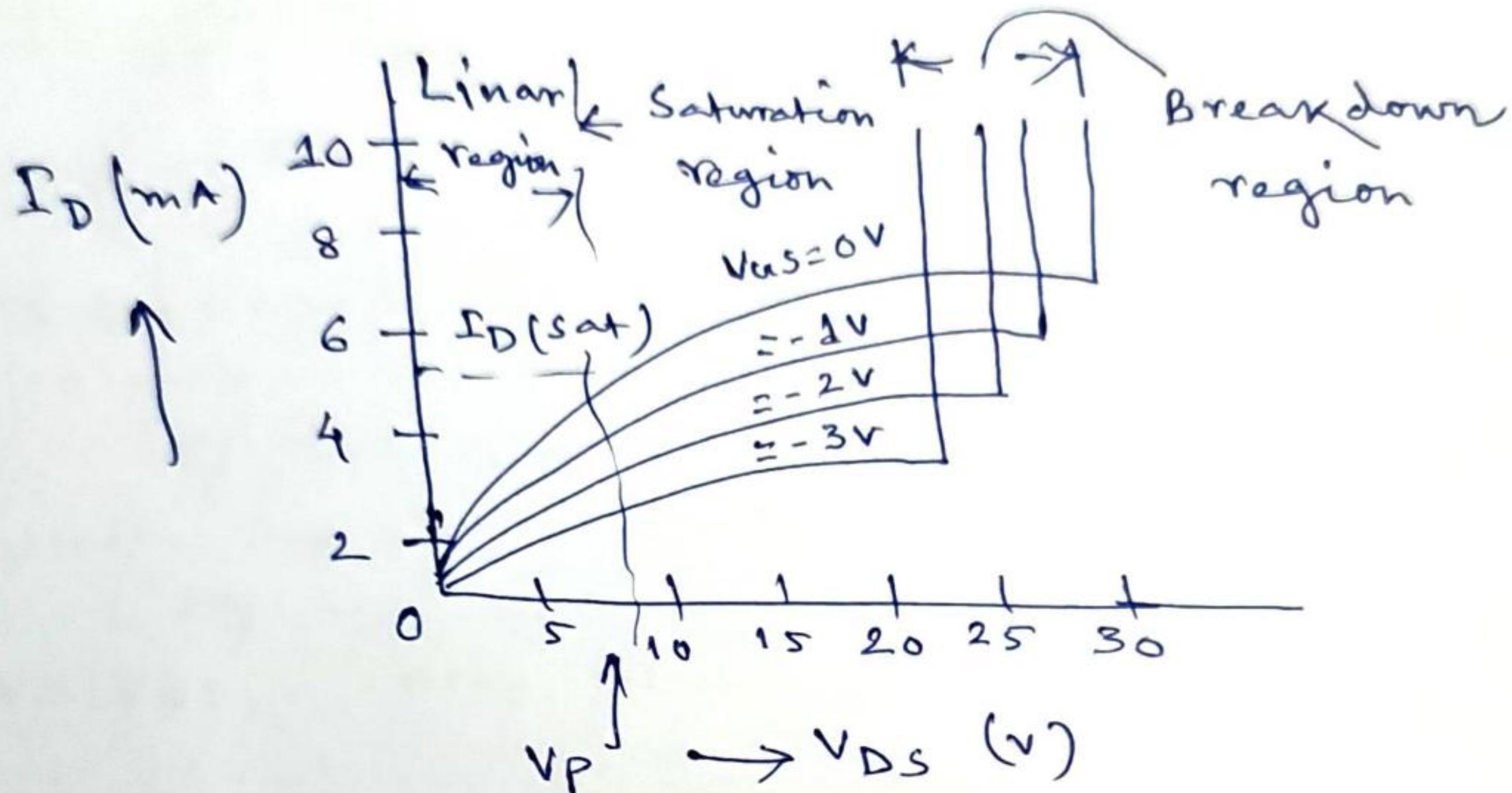
⇒ depletion regions on both sides of the channel.

⇒ the name field-effect is used for the device since the transverse field introduced by the gate controls the channel conductance and hence the device current

## Static characteristics

⇒  $I_D$  vs.  $V_{DS}$  with  $V_{GS}$  as

parameter  
⇒ Also known as common source  
drain characteristics of a junction FET.



Three regions:

- i) the ohmic or linear region
- ii) the saturation region
- iii) the breakdown region

⇒ At a value  $V_P$  of  $V_{DS}$ ,  $I_D$  saturates at a value  $(I_D)_{sat}$ . The channel is said to be pinched off.  
The voltage is called pinch-off voltage ( $V_P$ ).

Approximate Expression for  $V_P$

$$|V_P| = \frac{e N_D}{2G} a^2$$

$e$  = the magnitude of the electronic charge

$N_D$  = the donor concentration in the channel

$a$  = half of the channel width

$\epsilon$  = the permittivity of the channel material.

For a p-channel FET

$N_D$  should be replaced by  $N_A$ , the acceptor concentration.

### Metal-oxide Semiconductor FET (MOSFET)

- Has greater commercial importance than the junction FET
- n-channel and p-channel MOSFETs are there.

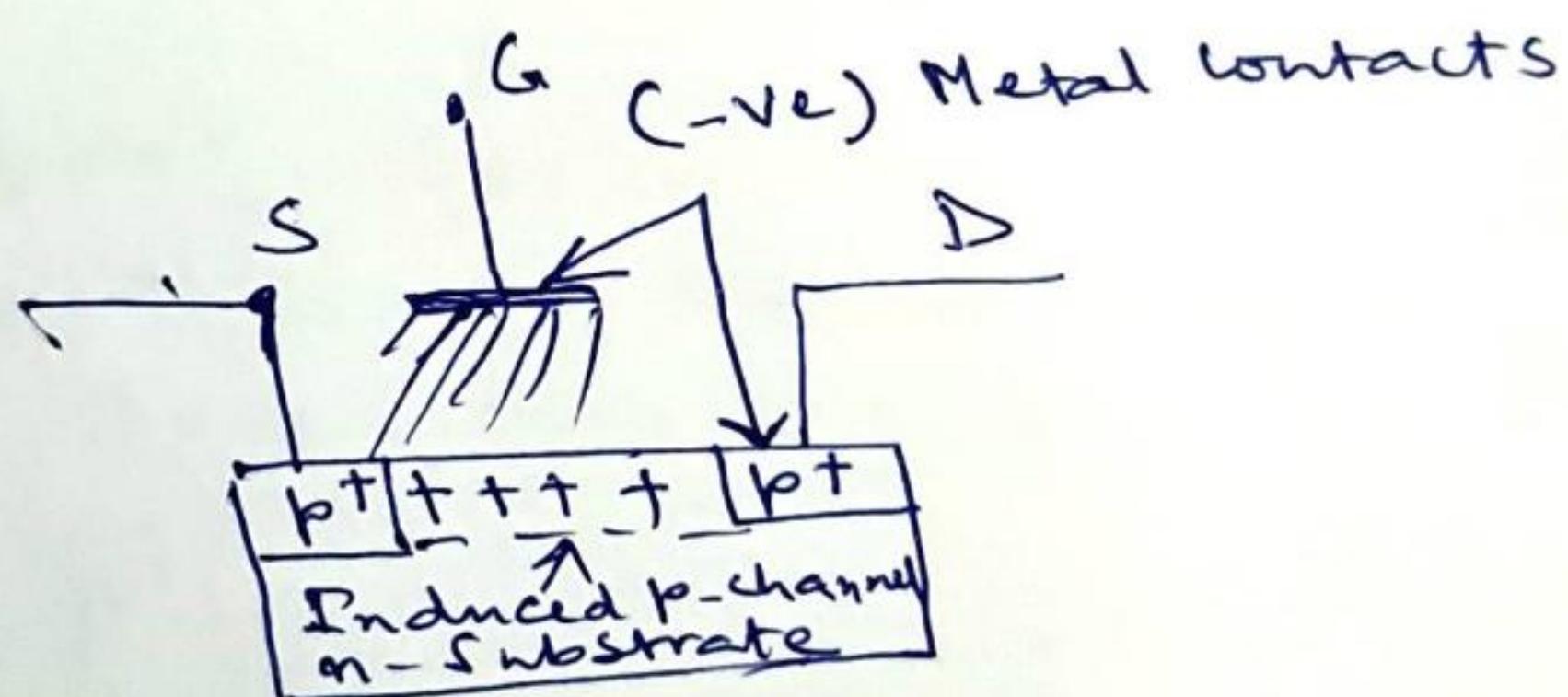


Figure: A p-channel MOSFET

⇒ An n-channel MOSFET has a similar structure. It has a p-type substrate and two n<sup>+</sup> end regions serving as the source and drain, respectively.

⇒ disadvantage of n-channel devices is that their fabrication is more difficult and hence they are more expensive than p-channel devices

n-channel and p-channel MOSFETs  
may again of two types:

- i) Enhancement MOSFET
- ii) Depletion MOSFET

### Static Drain Characteristics

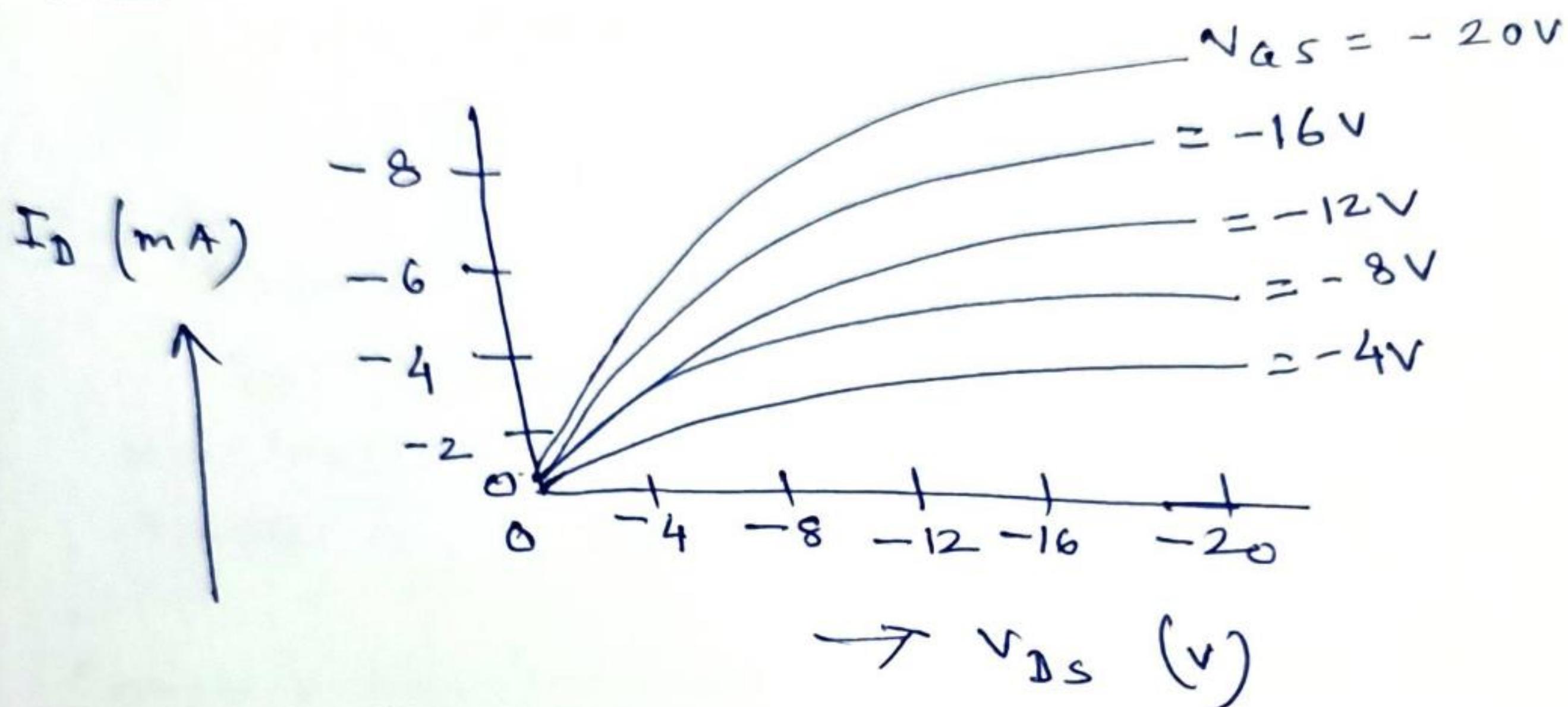


Figure: Typical drain characteristics  
of a p-channel enhancement  
mode MOSFET

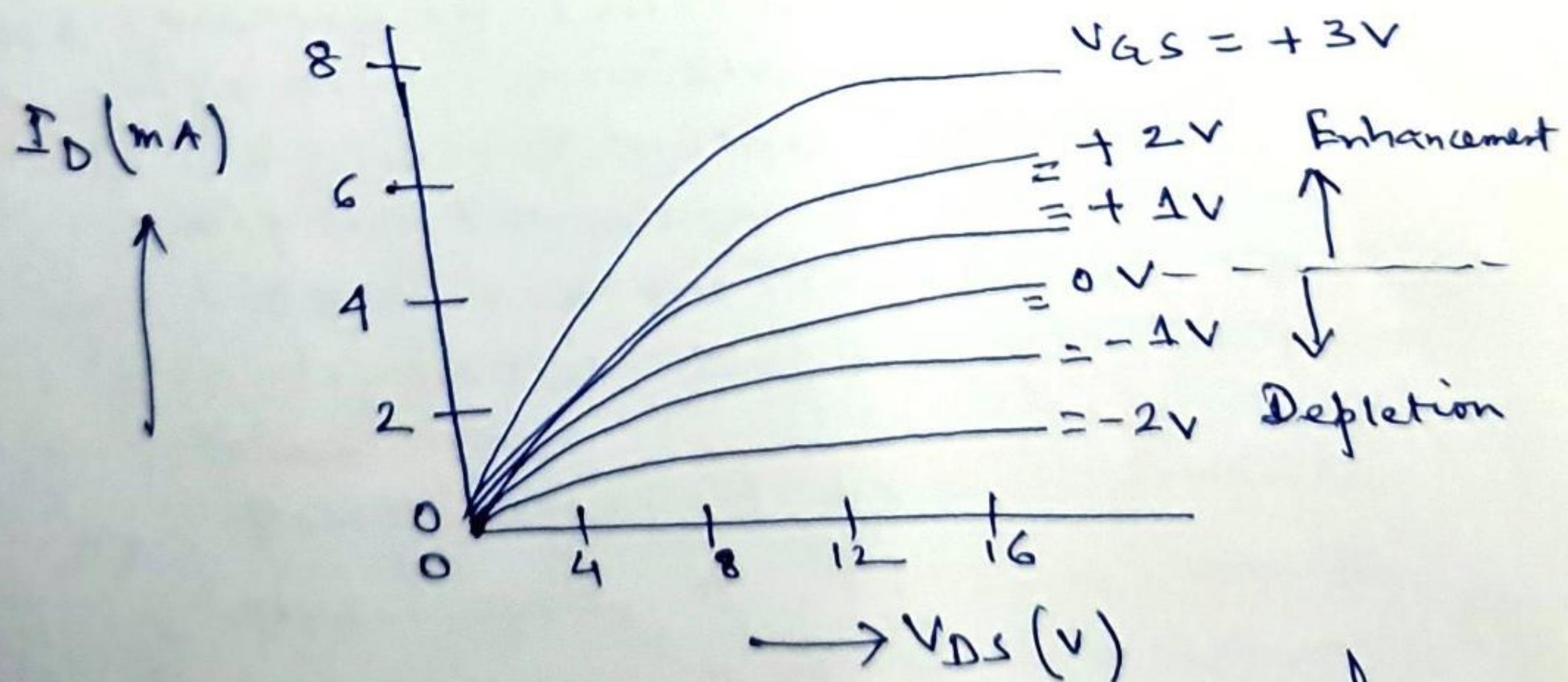


Figure: Static characteristics of an  
n-channel MOSFET in both  
enhancement and depletion mode

## Circuit Symbol

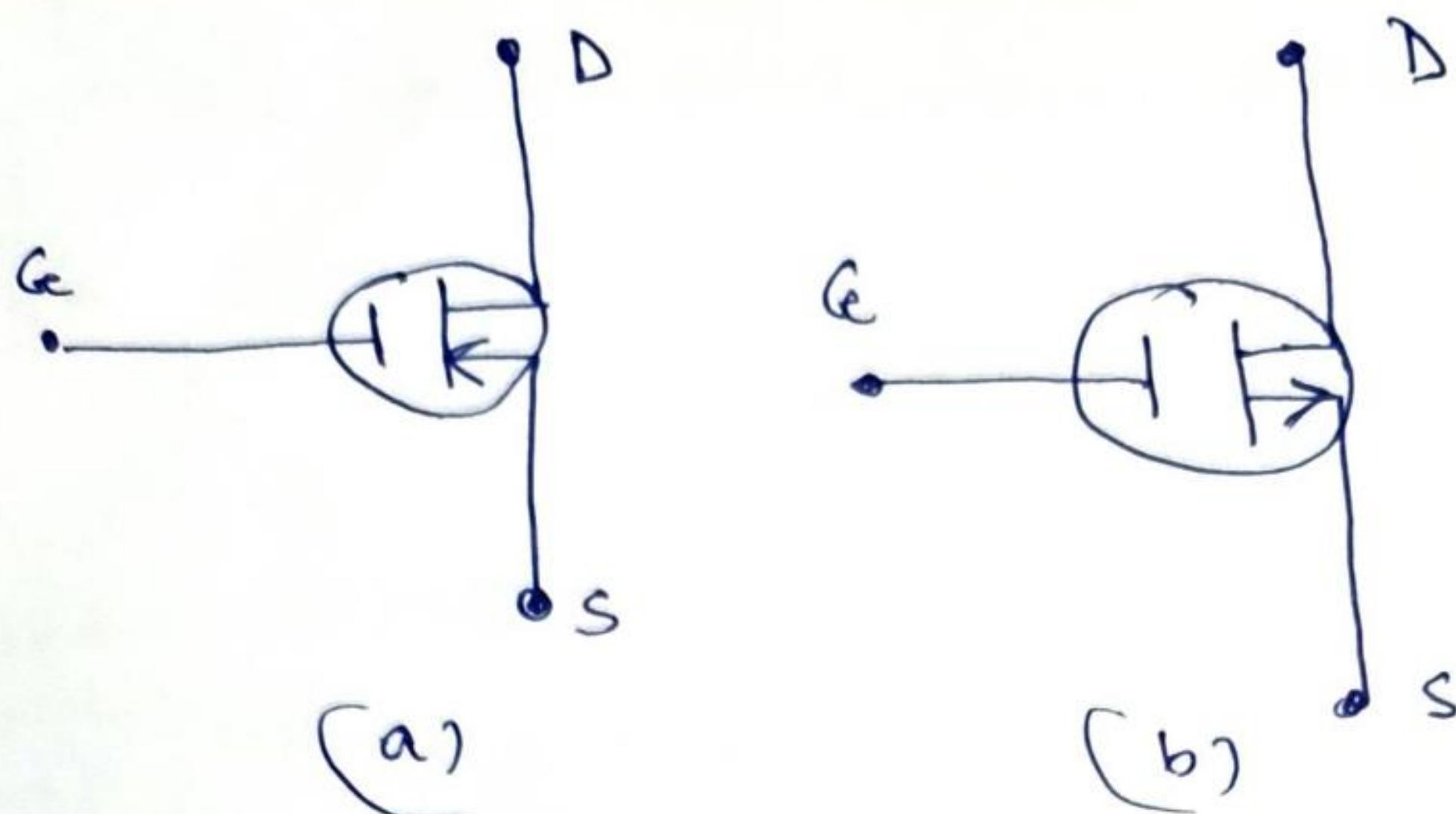


Figure: Circuit Symbols for  
(a) p - channel and (b) n - channel  
MOSFETs of depletion or enhancement  
type .

## Comparison between FETs and Bipolar Transistors

- ⇒ only majority carriers are involved in the operation of a FET. Both majority and minority carriers are involved in a bipolar transistor
- ⇒ FETs → voltage controlled
- ⇒ Bipolar transistor → current controlled.
- ⇒ FET → input impedance - very high compared to that of a bipolar transistor
- ⇒ Fabrication of FET is simpler
- ⇒ Power gain of FETs is much larger than that of bipolar transistors at audio frequencies

Problem: Determine the pinch-off voltage for an n-channel silicon FET with a channel width of  $5.6 \times 10^{-4}$  cm and a donor concentration of  $10^{15} \text{ cm}^{-3}$ . Given that the dielectric constant of Si is 12.

### Silicon Controlled Rectifier (SCR)

It is a rectifier but with control element which can control the conduction angle. In an ordinary rectifier, the rectifier has no control over portion of the conducting part of a cycle. In a half wave ordinary rectifier, the conduction is over entire half cycle. However, in an SCR, we can control the conduction during half the cycle by introducing a control element called gate.

An SCR is a four layer Semiconductor device consisting of alternate p-type and n-type material. It is a pnpn device. There are three junctions.

- 1) Anode (A)
- 2) Cathode (K)
- 3) Gate (G)

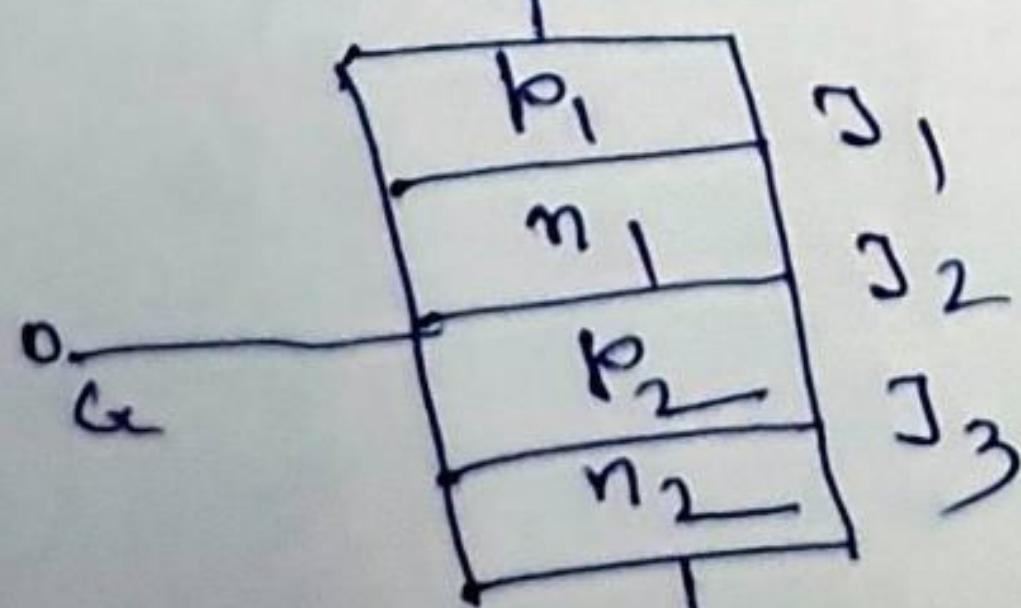


Figure: Structure of SCR

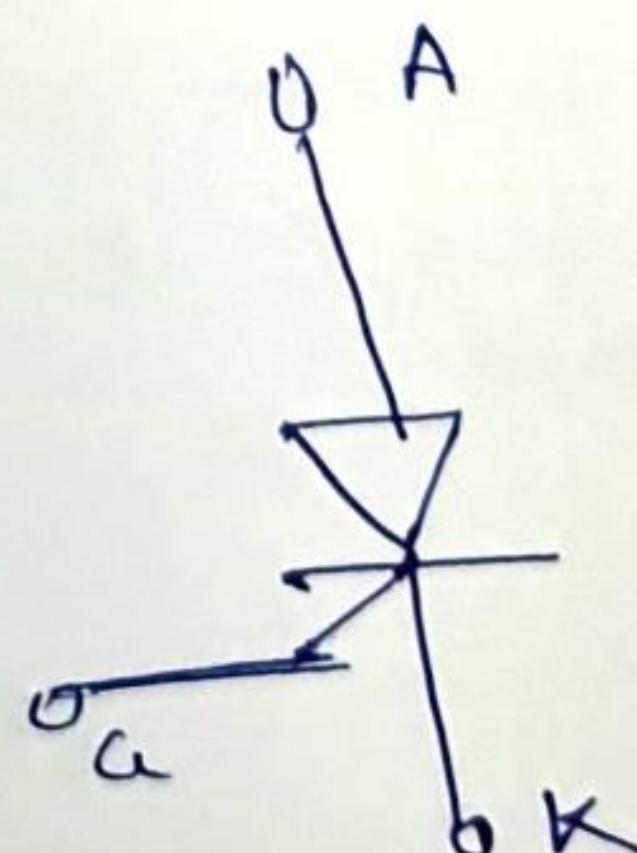


Figure: Circuit symbol of SCR

Anode  $\Rightarrow$  connected to +ve terminal of the battery

Cathode  $\Rightarrow$  to the -ve terminal

Gate  $\Rightarrow$  control element

Three junctions  $\Rightarrow J_1, J_2, J_3$

$J_1$  and  $J_2 \Rightarrow$  forward biased  
 $\Rightarrow$  low resistance

$J_3 \Rightarrow$  reverse biased

$\Rightarrow$  high resistance

We can split four layer device into  $p_{1a} n_{1a} p_{2a}$  and  $n_{1b} p_{2b} n_{2b}$

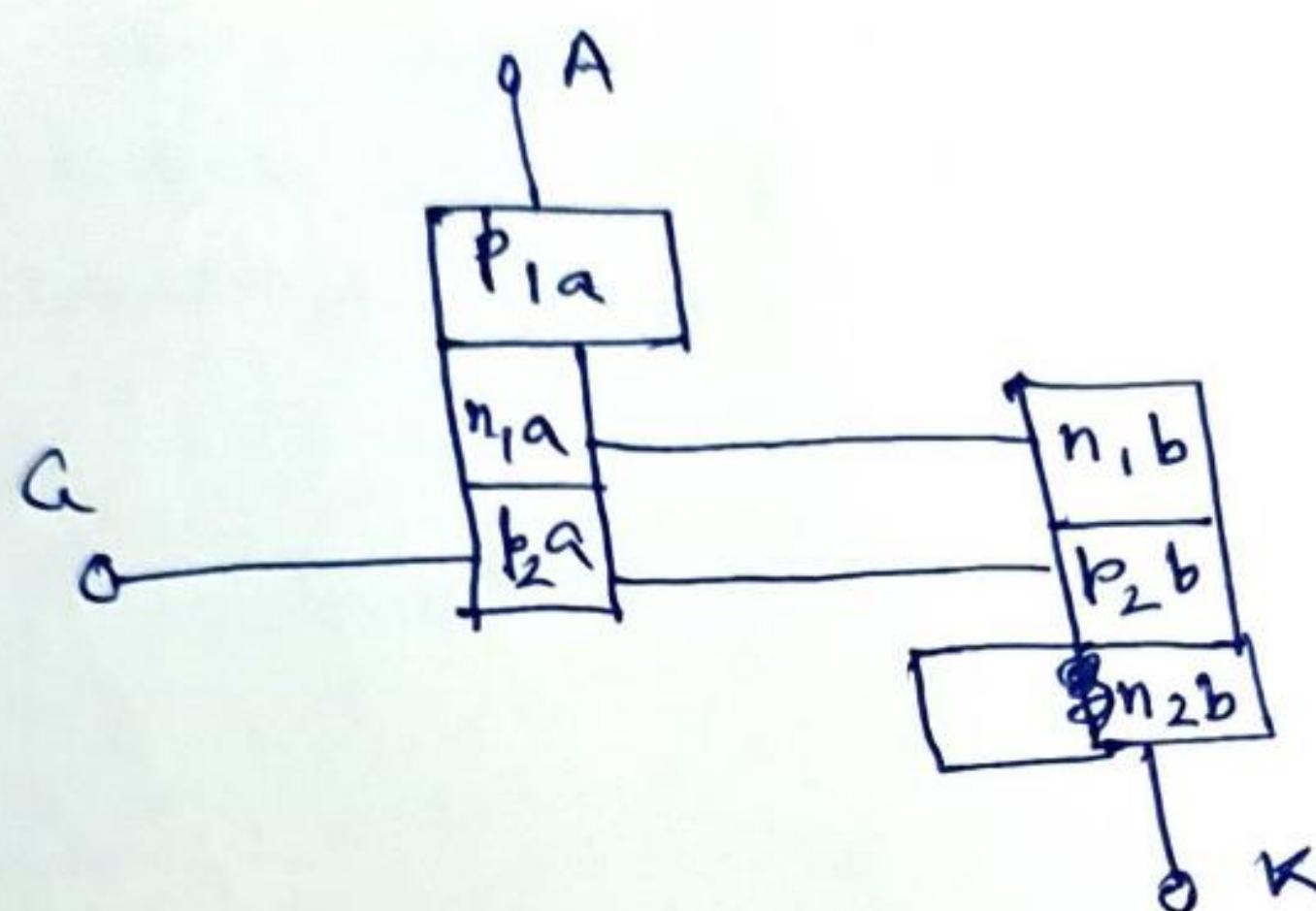
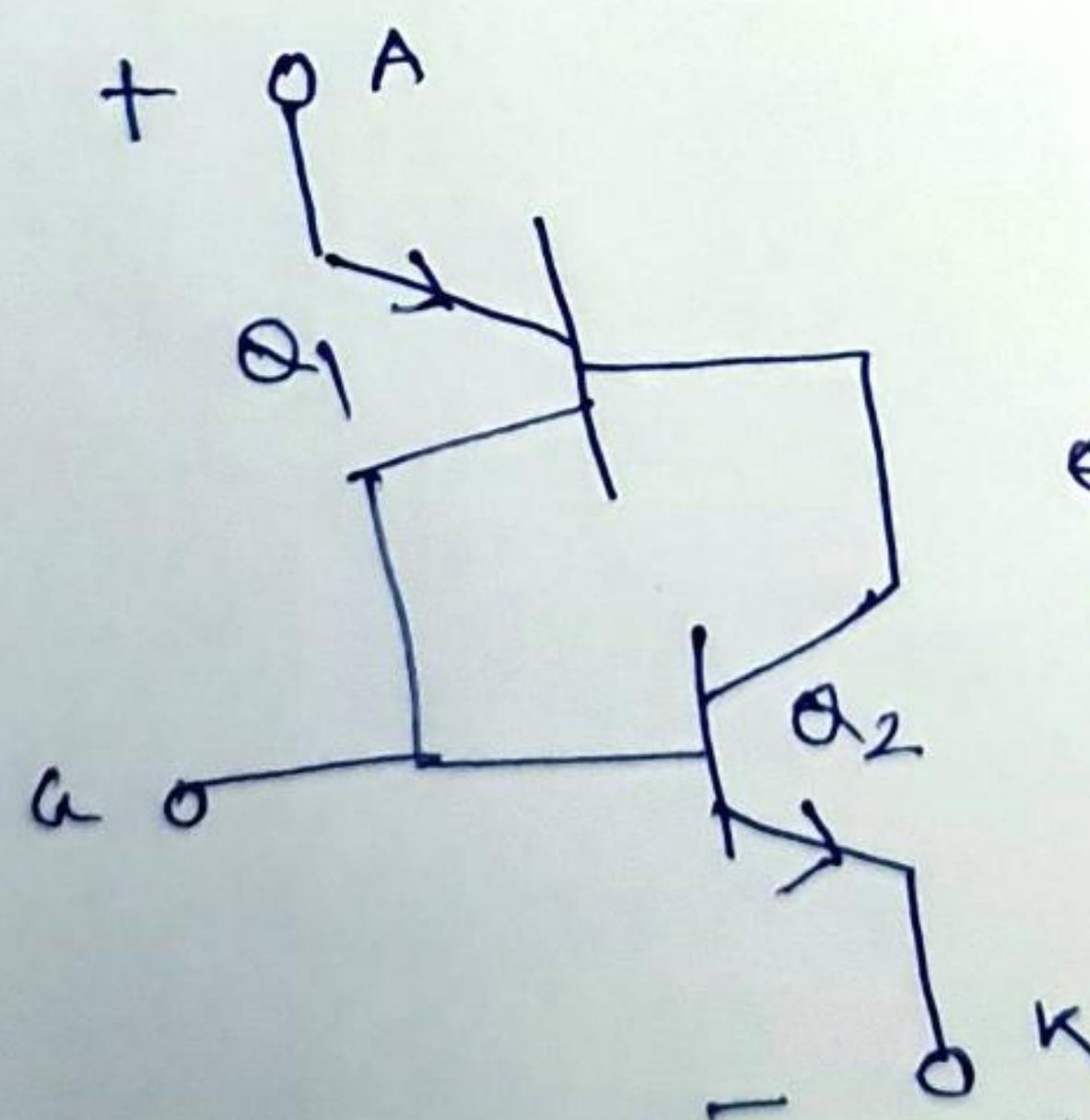


figure: Two transistor structure



$Q_1 \rightarrow p-n-p$  transistor  
 $Q_2 \rightarrow n-p-n$  transistor

figure: Two transistor circuit analogy

- ⇒ when the SCR is forward biased,
- ⇒ A is +ve wrt K
- ⇒ Assume that the gate is not connected to any supply but open.
- ⇒ There will be a small leakage current  $I_{FO}$  due to minority carriers in the reverse biased p-n junction  $J_2$
- ⇒ Hence no current flows except the leakage current  $I_{FO}$  which is negligible.
- ⇒ With gate open, a forward bias on SCR, there is only small current due to leakage  $I_{CO}$ .

## Operational Amplifiers

The operational amplifier (OP AMP) (abbreviated) is a direct coupled high gain differential input amplifier.

→ OP AMP can perform mathematical operations such as summation, subtraction, integration and differentiation.

### Circuit Symbol

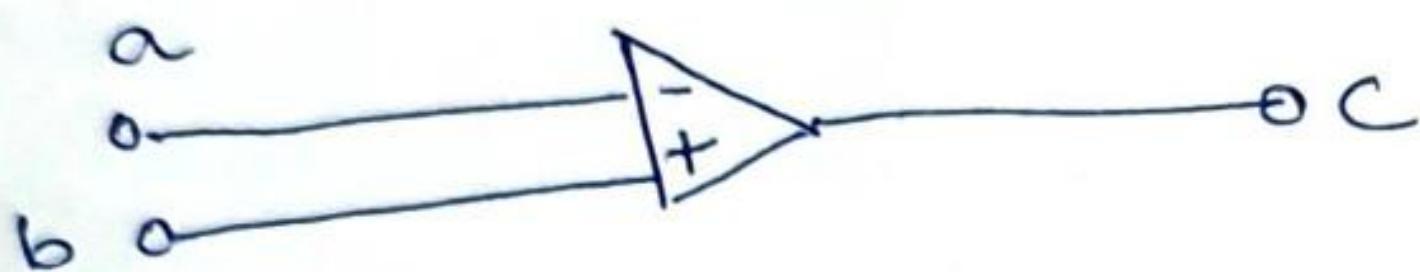


Figure: Circuit symbol of a basic OP AMP

Input terminals → 'a' and 'b'

a → inverting input terminal

| - |

b → non-inverting input terminal

| + |

c → output terminal

\* The output voltage at 'c' is proportional to the difference of the two signal voltages applied at the two input terminals simultaneously.

- ⇒ The constant of proportionality  
(A) ⇒ open loop voltage gain of the OP-AMP.

### OP AMP characteristics

The ideal op AMP has the following properties:

- 1) An infinite voltage gain
- 2) An infinite input impedance
- 3) Zero output impedance
- 4) An infinite bandwidth
- 5) Characteristics do not change with temperature
- 6) Perfect balance

But for practical op AMP

- ⇒ The low frequency voltage gain  
→  $10^3$  to  $10^6$
- ⇒ The bandwidth is finite
- ⇒ The input impedance →  
 $150 \text{ k}\Omega$  to a few hundred  $\text{M}\Omega$
- ⇒ The output impedance  
 $0.75$  to  $100 \Omega$
- ⇒ do not have a perfect balance

## Common Mode Rejection Ratio (CMRR)

⇒ An op AMP is basically a differential amplifier

$v_1$  → signal voltage w.r.t ground applied to NI terminal 'b'

$v_2$  → signal voltage w.r.t ground applied to I terminal 'a'

$v_o$  → output voltage w.r.t ground at the terminal 'c'

$v_d$  → difference signal  
=  $(v_1 - v_2)$

$v_c$  → Common mode signal  
=  $\left\{ \frac{v_1 + v_2}{2} \right\}$

$$v_o = A_1 v_1 + A_2 v_2 \quad \dots \quad (1)$$

$A_1$  → voltage gain when 'a' is grounded.

$A_2$  → voltage gain when 'b' is grounded.

$$\text{Now, } v_1 = v_c + \frac{1}{2} v_d \quad \dots \quad (2)$$

$$v_2 = v_c - \frac{1}{2} v_d \quad \dots \quad (3)$$

Using equations (2) & (3) in (1)

$$\begin{aligned} v_o &= \frac{1}{2} (A_1 - A_2) v_d + (A_1 + A_2) v_c \\ &= A_d v_d + A_c v_c \end{aligned}$$

$$A_d = \frac{1}{2} (A_1 - A_2)$$

$$A_c = (A_1 + A_2)$$

$A_d \rightarrow$  Voltage gain for the difference signal

$A_c \rightarrow$  Voltage gain for the common mode signal

In the ideal case

$A_d \rightarrow$  infinite large

$A_c \rightarrow$  zero

$$CMRR = \frac{A_d}{A_c}$$

CMRR is much larger than unity

Inverting Amplifier

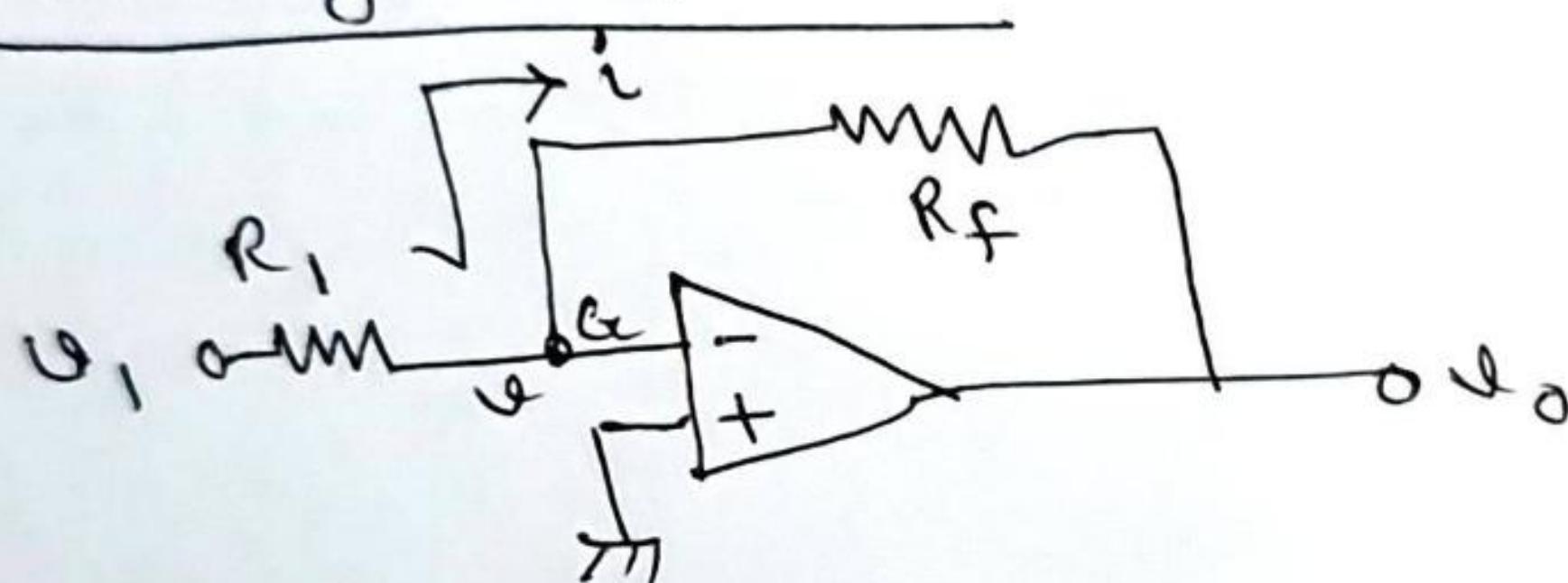


figure: Inverting amplifier

$R_i \rightarrow$  Input resistance

$R_f \rightarrow$  feedback resistance

$V_i \rightarrow$  Input voltage

$V_o \rightarrow$  output voltage

$v \rightarrow$  voltage at the inverting input

We have  $v = \frac{V_o}{A} \rightarrow 0$  as  $|A| \rightarrow \infty$

Therefore, the inverting input terminal is practically at the ground potential.

$$i = \frac{v_1 - v}{R_1} \dots (1)$$

$$\frac{v_1 - v}{R_1} = \frac{v - v_o}{R_f} \dots (2)$$

$v \approx 0$  due to virtual ground

thus equation (2) reduces to

$$\frac{v_1}{R_1} = - \frac{v_o}{R_f} \dots (3)$$

Closed-loop gain of the inverting amplifier is  $\frac{v_o}{v_1} = - \frac{R_f}{R_1} \dots (4)$

$R_{in}$  = input resistance of the amplifier system

$$= \frac{v_1}{i_1} \\ = \frac{v_1}{(v_1 - v)/R_1} \\ \approx R_1$$

### Non-inverting amplifier

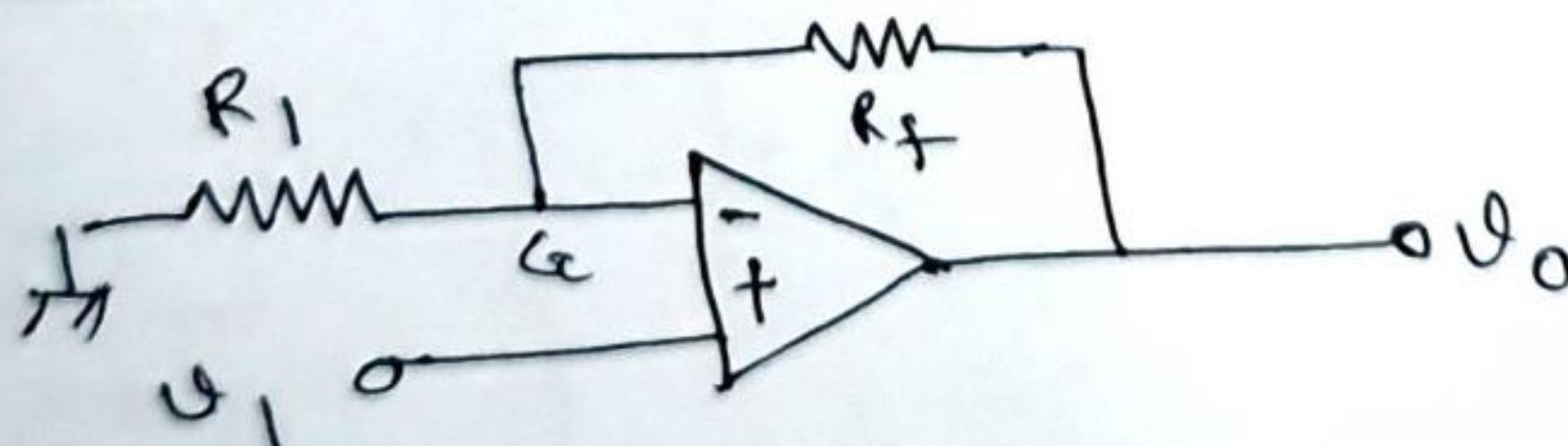


figure: Non-inverting amplifier

Applying Kirchhoff's Current Law at the point G,

$$\frac{V_o - V_1}{R_f} = \frac{V_1}{R_1}$$

$$\Rightarrow \frac{V_o}{V_1} = 1 + \frac{R_f}{R_1}$$

= Voltage gain of the amplifier system.

If  $R_f = 0$  and  $R_1 = \infty$ , the circuit reduces to

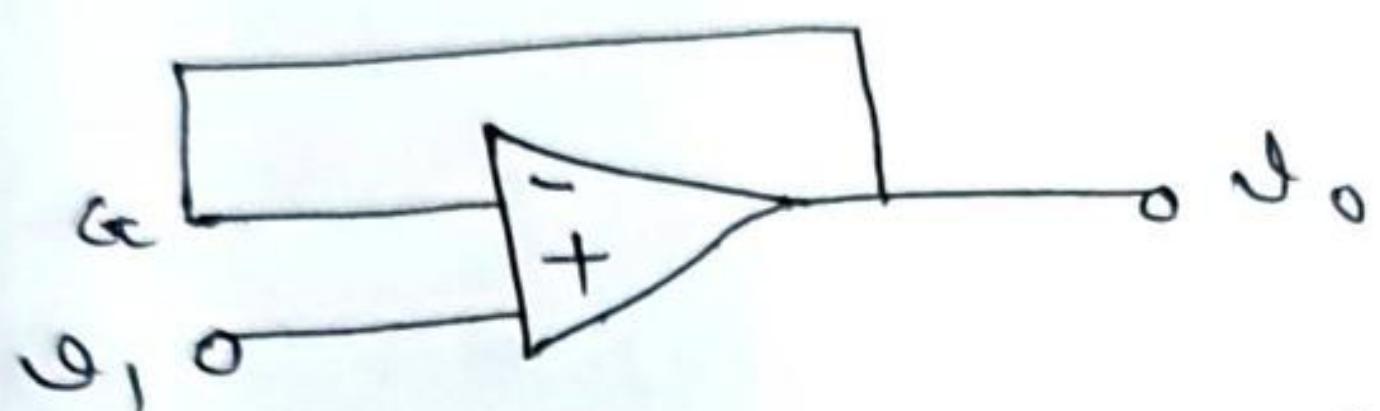


Figure: A voltage follower  
The voltage gain in this case is unity.

Adder or Summing amplifier

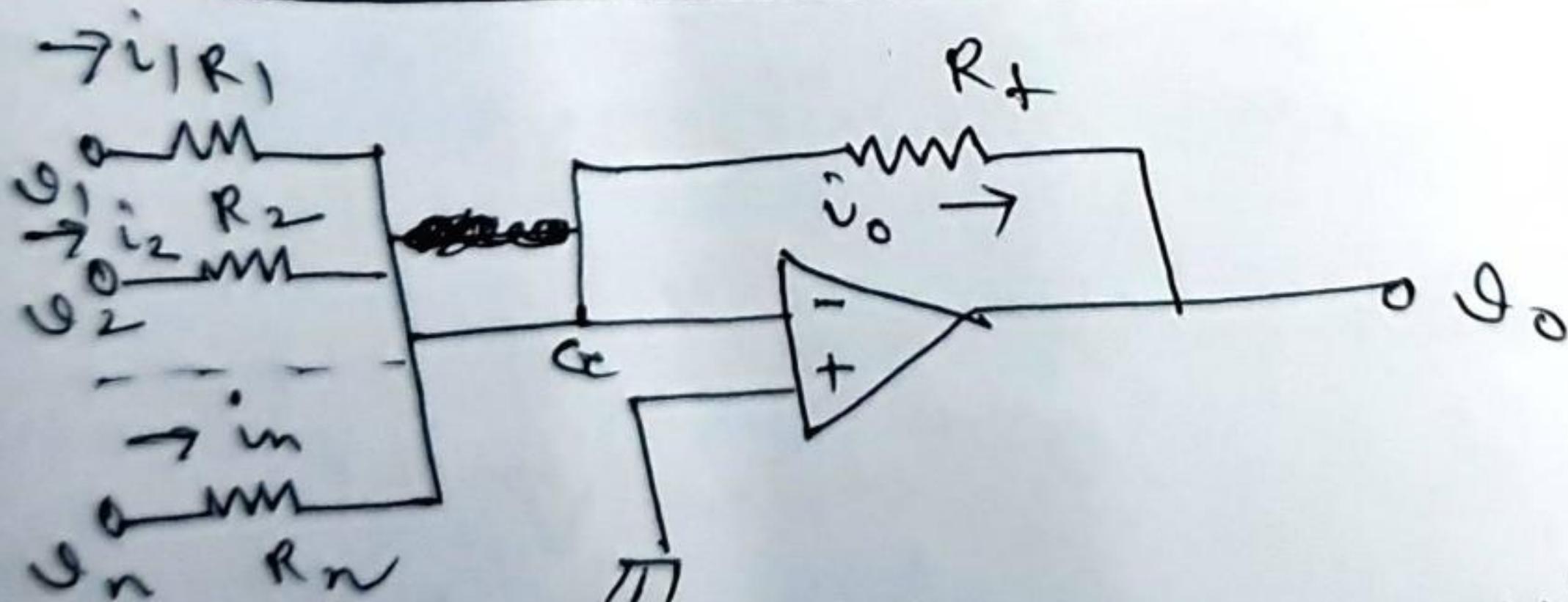


Figure: Summing amplifier

$G \rightarrow$  is at ground potential

By Kirchhoff's Current Law

$$i_1 + i_2 + \dots + i_n = i_o$$

$$\text{or } \frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n} = -\frac{V_o}{R_f}$$

$$\text{or } V_o = - \left\{ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \dots + \frac{R_f}{R_n} V_n \right\}$$

$$\text{If } R_1 = R_2 = \dots = R_n = R$$

$$V_o = - \frac{R_f}{R} (V_1 + V_2 + \dots + V_n)$$

$$\text{with } R_f = R$$

$$V_o = - (V_1 + V_2 + \dots + V_n)$$

Thus the circuit is termed a Summing amplifier or an adder

### Differentiator

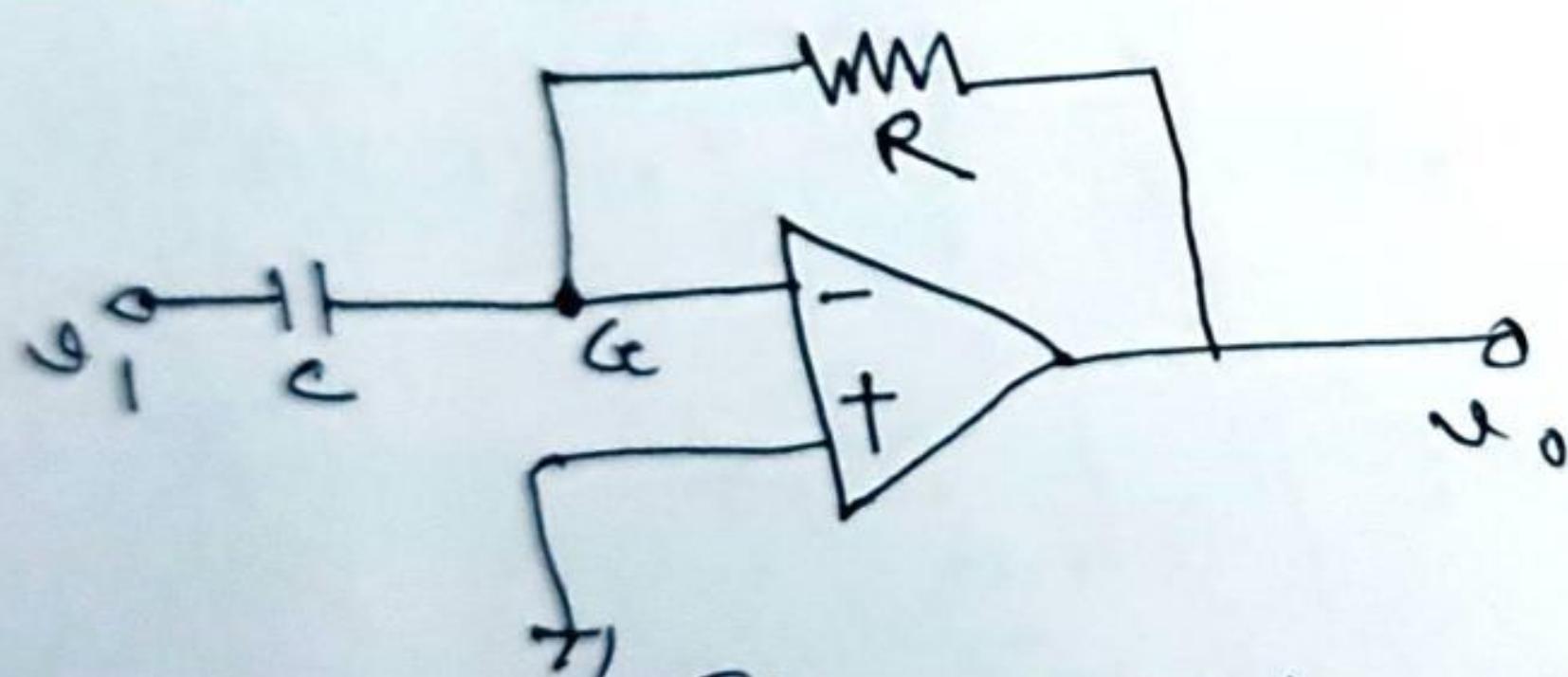


Figure: Differentiator

$$q = CV_1$$

$$\text{or } I_1 = q/C$$

$$\begin{aligned} \frac{dV_1}{dt} &= \frac{1}{C} \frac{dq}{dt} \\ &= \frac{i}{C} \end{aligned}$$

$i$  = Current through  $R$

$$= - \frac{v_o}{R}$$

Thus  $v_o = - R C \frac{dv_i}{dt}$

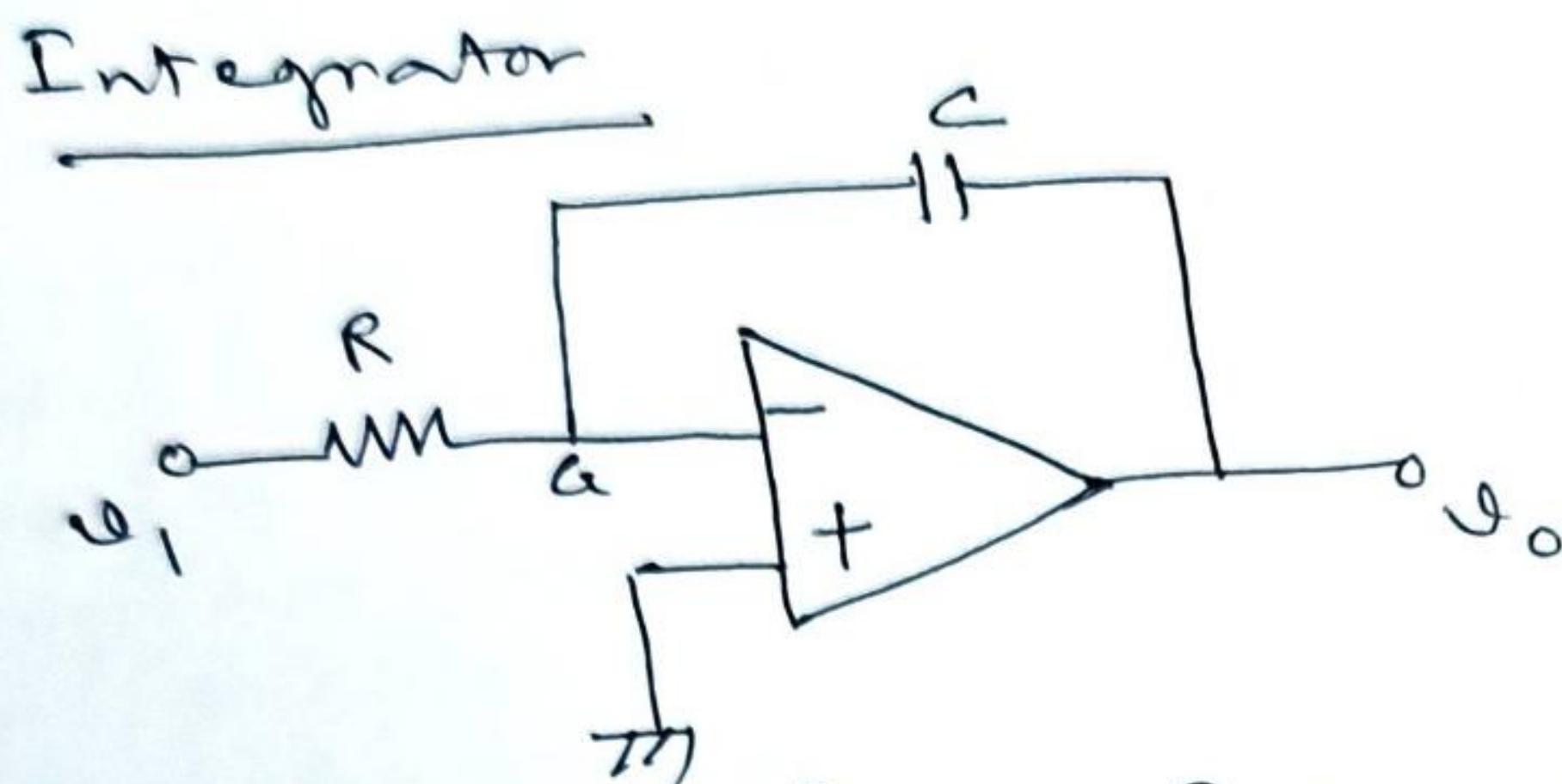


Figure: Integrator

$i$  = current flowing through  $R$

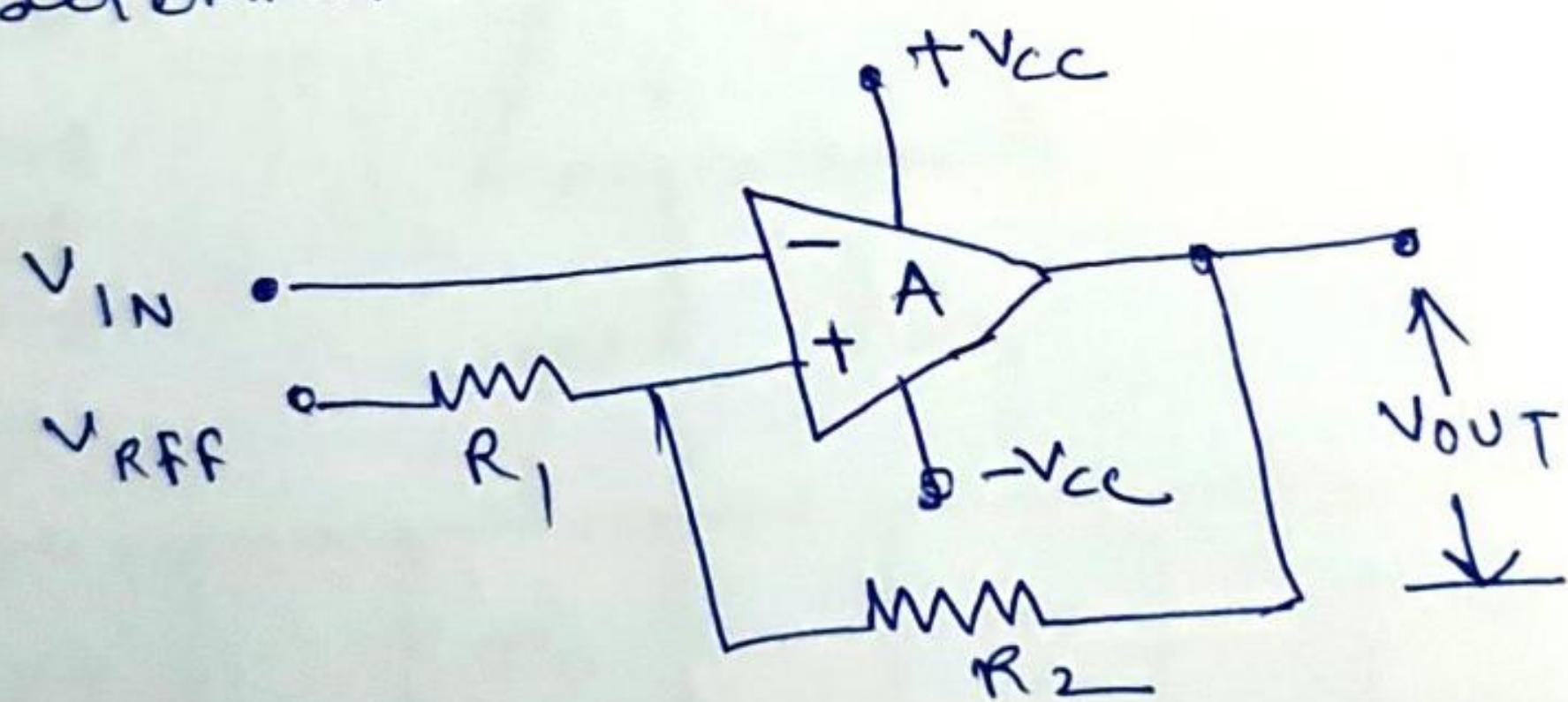
$$= \frac{v_i}{R}$$

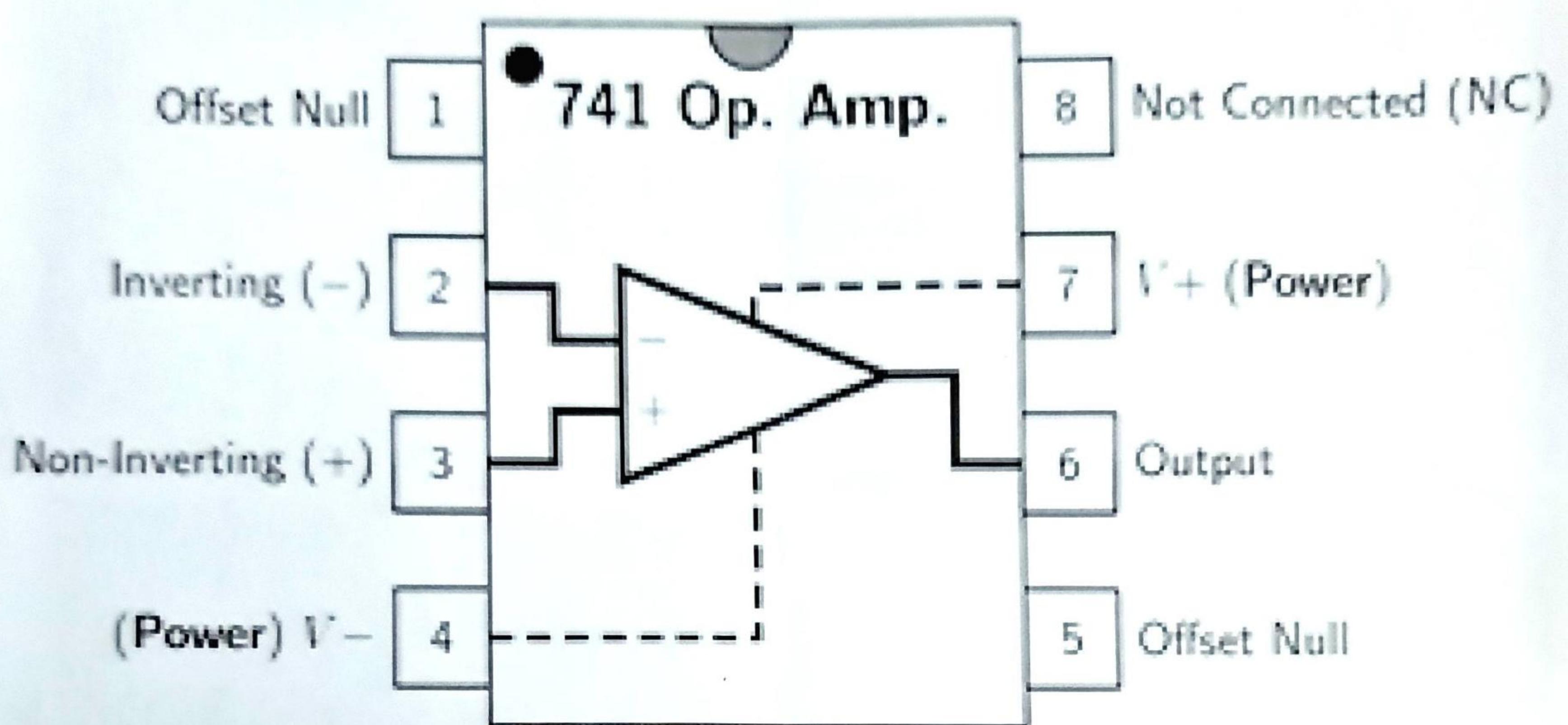
$$v_o = - \frac{1}{C} \int_0^t i dt$$

$$= - \frac{1}{RC} \int_0^t v_i dt$$

## OP-AMP Comparator

- ⇒ The Comparator is an electronic decision making circuit that makes use of an operational amplifier.
- ⇒ Very high gain in its open-loop state, that is, there is no feedback resistor.
- ⇒ The op-amp comparator compares one analog voltage level with another analog voltage level, or some preset reference voltage  $V_{REF}$  and produces an output signal based on this voltage comparison.
- ⇒ In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is largest of the two.





## Oscillators

An oscillator delivers an output voltage of a given waveform without the application of an external input signal.

### Types of oscillators

i) depending on the nature of the generated waveform

a) Sinusoidal or harmonic oscillators

b) Relaxation oscillators

ii) a) L-C oscillators

b) R-C oscillators

iii) depending on the frequency of the generated signals

a) Audio freq. oscillators

→ a few Hz - 20 kHz

b) Radio freq. oscillators

→ 20 kHz - 30 MHz

c) VHF oscillators

→ 30 MHz - 300 MHz

d) UHF oscillators

→ 300 MHz - 3000 MHz

e) Microwave oscillators

→ 3 GHz - Several GHz

L-C oscillators  $\Rightarrow$  Hartley oscillator,  
Colpitt oscillator

R-C oscillators  $\Rightarrow$  Phase Shift and  
Wein-Bridge oscillators

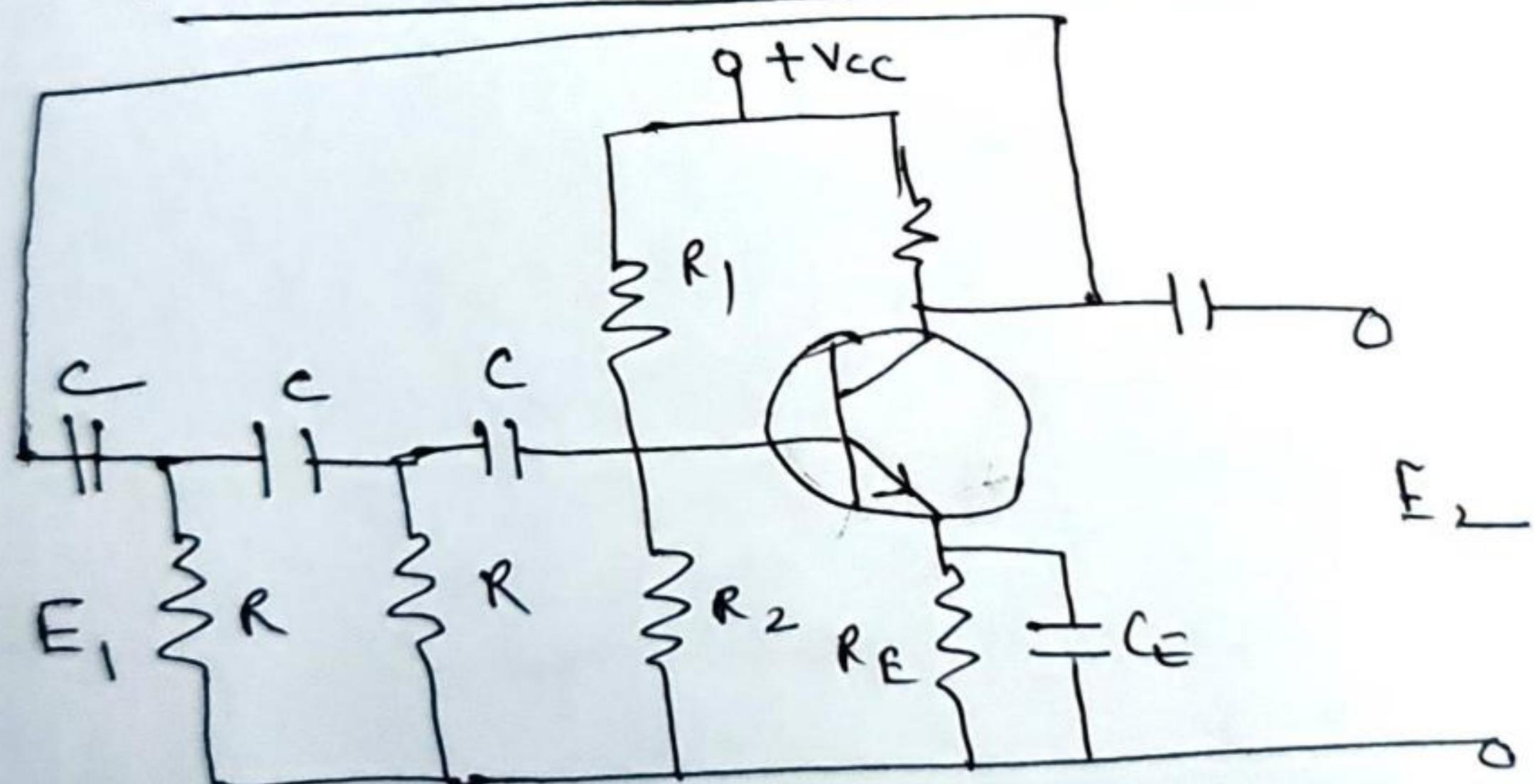
Concept of feedback in oscillators

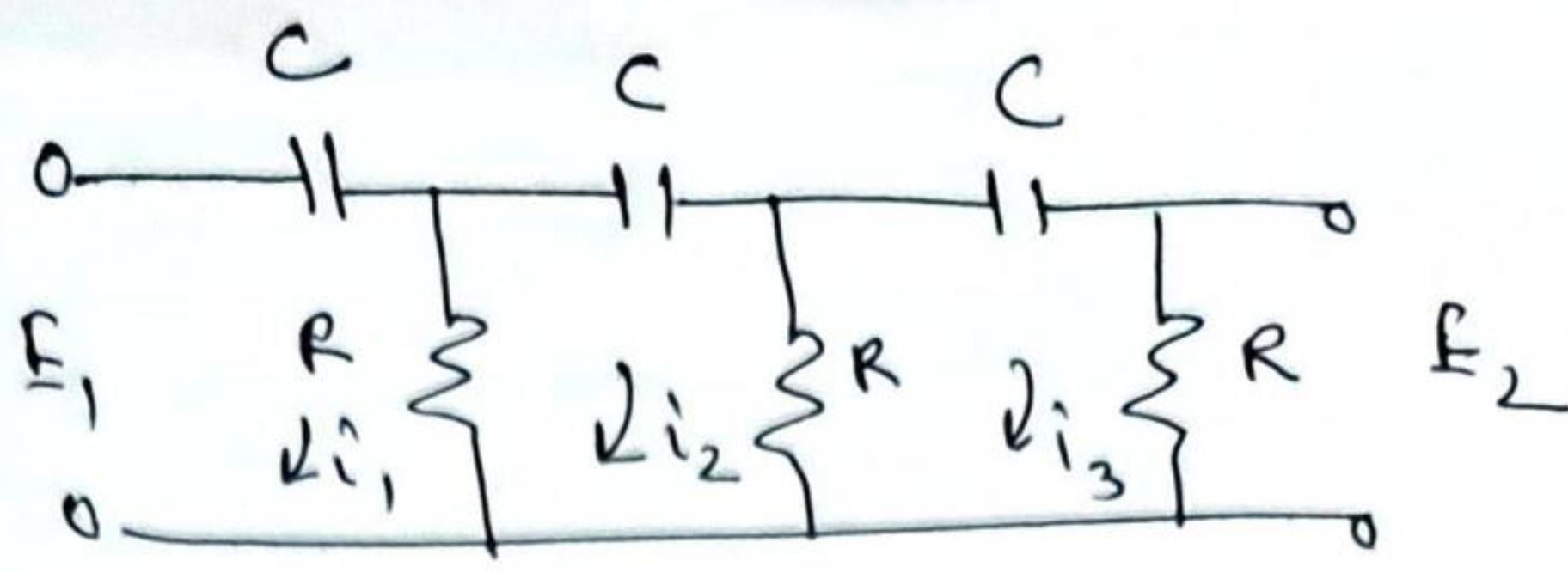
with +ve feedback

$$A_f = \frac{A}{1 - A_m}$$

If  $A_m = 1$ ,  $A_f \rightarrow \infty$   
The condition of unity loop gain  
(~~approx~~  $A_m = 1$ ) is known as  
Barkhausen Criterion.

Phase-shift oscillator





Considering  $j\omega = p$

the mesh equations are

$$E_1 = \left( R + \frac{1}{pC} \right) i_1 - Ri_2 + 0 \cdot i_3$$

$$0 = -Ri_1 + \left( 2R + \frac{1}{pC} \right) i_2 - Ri_3$$

$$0 = 0 \cdot i_1 - Ri_2 + \left( 2R + \frac{1}{pC} \right) i_3$$

$$\therefore i_3 = \frac{\begin{vmatrix} R + \frac{1}{pC} & -R & E_1 \\ -R & 2R + \frac{1}{pC} & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} \frac{1}{pC} + R & -R & 0 \\ -R & 2R + \frac{1}{pC} & -R \\ 0 & -R & 2R + \frac{1}{pC} \end{vmatrix}}$$

$$= \frac{E_1 R^2}{R^3 + \frac{5R}{p^2 C^2} + \frac{6R^2}{pC} + \frac{1}{p^3 C^3}}$$

Substituting  $p = j\omega$

$$i_3 = \frac{E_1 R^2}{\left( R^3 - \frac{5R}{\omega^2 C^2} \right) + j \left( \frac{1}{\omega^3 C^3} - \frac{6R^2}{\omega C} \right)}$$

Condition for  $E_2 = R i_3$  to be  $180^\circ$   
phase shift with  $E_1$  is

$$\frac{1}{\omega^3 C^3} - \frac{6R^2}{\omega C} = 0$$

$$\text{or } \omega^2 = \frac{1}{6C^2 R^2}$$

$$\text{or } \omega = \frac{1}{\sqrt{6} CR}$$

$$\therefore f = \frac{1}{2\pi\sqrt{6} RC}$$

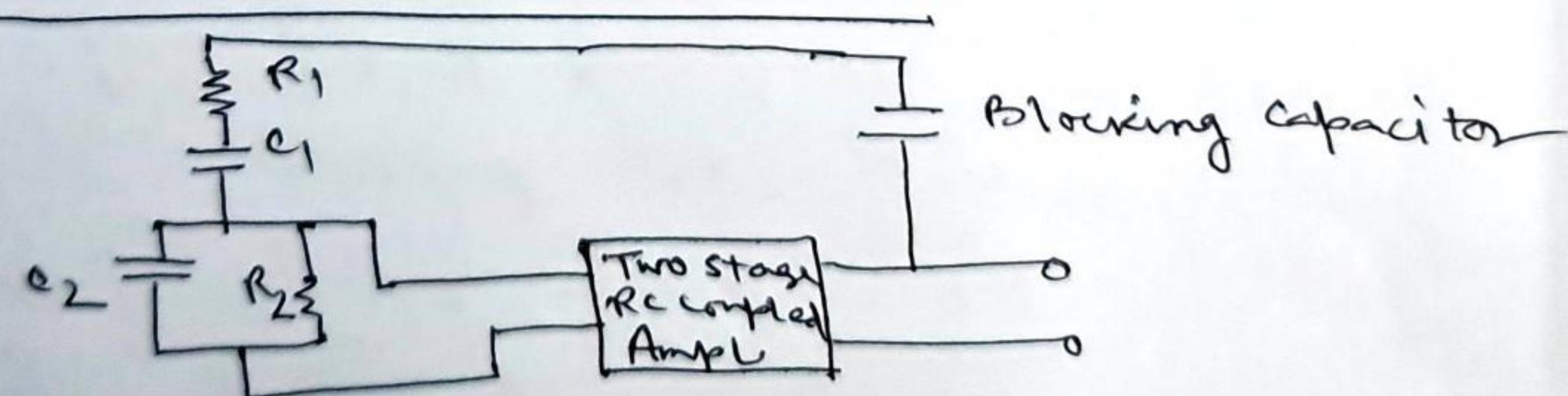
Problem: A two-stage phase shifting network as shown in figure below is used in a phase shift oscillator. Find out the frequency of oscillation.

$$\text{R C} \\ \text{Amplifier} \\ \text{Lip} = \frac{1}{2\pi f_0}$$

- Advantages
- i) It does not require transformers or inductors
  - ii) It can be used to produce very low frequencies
  - iii) The circuit provides good frequency stability

- Disadvantages
- i) It is difficult for the circuit to start oscillations as the feedback is generally small
  - ii) The circuit gives small output.

### Wein-Bridge oscillator



$$\beta = \frac{Z_2}{Z_1 + Z_2}$$

Condition for oscillation is  $A\beta = 1$

$$\therefore \frac{1}{A} = \beta = \frac{-jx_2R_2/R_2 - jx_2}{R_1 - jx_1 - jx_2R_2/(R_2 - jx_2)}$$

Simplifying

$$j \left[ x_2R_2A - x_1R_2 - x_2R_1 - x_2R_2 \right] \\ + \left[ R_1R_2 - x_1x_2 \right] = 0$$

$$\text{so, } i) \quad R_1R_2 = x_1x_2$$

$$\text{or} \quad R_1R_2 = \frac{1}{\omega C_1} \cdot \frac{1}{\omega C_2}$$

$$\therefore f = \frac{1}{2\pi \sqrt{C_1C_2R_1R_2}}$$

$$\text{If } C_1 = C_2 = C$$

$$\text{and } R_1 = R_2 = R$$

$$f = \frac{1}{2\pi RC}$$

$$ii) \quad x_2R_2 + -x_1R_2 - x_LR_1 - x_LR_2 = 0$$

$$\text{Putting } R_1R_2 = x_1x_L$$

$$A = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1$$

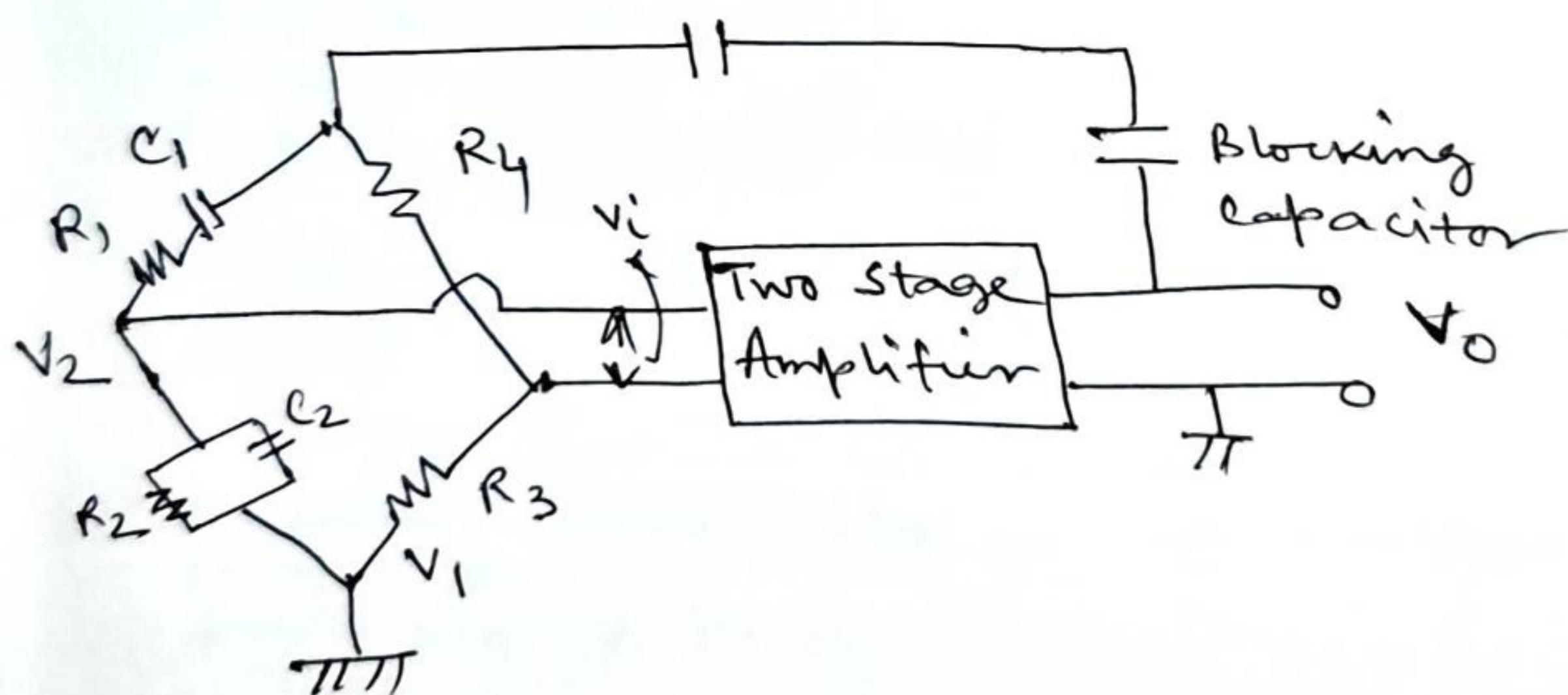
$$R_1 = R_L = R \quad \left| \begin{array}{l} \\ \\ \end{array} \right. \text{say}$$

$$C_1 = C_2 = C$$

$$\text{Amplification factor } A = 1 + 1 + 1 = 3$$

Problem: A Wein Bridge oscillator is to be used using standard value resistors and capacitors that are variable two-ganged units. The oscillator should tune from 1 to 3 kHz. Assume  $R_1 = R_2 = 100 \text{ k}\Omega$ , what range of values should be used for the two gang variable capacitor?

Problem: The Wein Bridge circuit shown in figure, add an inductor L in series with  $R_1, C_1$  combination and replace the parallel combination  $R_2, C_2$  by a resistor  $R_2$ . Find the frequency of oscillation and the minimum gain of the amplifier



100

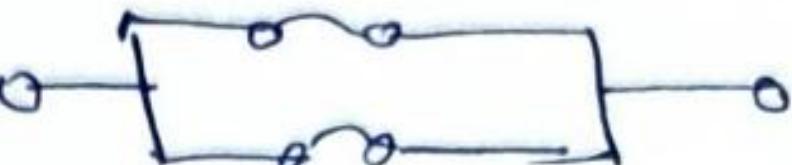
## Boolean Algebra

It is based on symbolic logic to express reasoning with the help of mathematical operations

$$(a) 0 \cdot 0 = 0$$



$$(b) 1 + 1 = 1$$



$$(a) 0 \cdot 1 = 1 \cdot 0 = 0$$



$$(b) 1 + 0 = 0 + 1 = 1$$



$$(a) 1 \cdot 1 = 1$$



$$(b) 0 + 0 = 0$$



$$(a) \bar{0} = 1$$

$$\mid$$

$$(b) \bar{1} = 0$$

$$(a) x = 1 \text{ if } x \neq 0$$

Indicates that a circuit cannot assume both states simultaneously

$$(b) x = 0 \text{ if } x \neq 1$$

Theorems: The theorems of Boolean algebra are stated below:

1) Commutative Law:

$$(a) A \cdot B = B \cdot A$$

$$(b) A + B = B + A$$

2) Associative Law:

$$(a) A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

$$(b) A + (B + C) = (A + B) + C$$

3) Distributive law

(a)  $A \cdot B + A \cdot C = A \cdot (B + C)$

(b)  ~~$(A+B) \cdot (A+C) = A + B + C$~~

~~(b)  $(A+B)(A+C) = A + B \cdot C$~~

4) Identities law

(a)  $A \cdot 1 = A$

(b)  $A + 0 = A$

5) Null elements

(a)  $A \cdot 0 = 0$

(b)  $A + 1 = 1$

6) Complements

(a)  $A \cdot \bar{A} = 0$

(b)  $A + \bar{A} = 1$

7) Idempotent property

(a)  $A \cdot A = A$

(b)  $A + A = A$

8) Absorption law

(a)  $A + A \cdot B = A$

(b)  $A \cdot (A + B) = A$

9) Involution

$$\overline{\overline{A}} = A$$

10) De-Morgan's Theorems

(a)  $\overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$

(b)  $\overline{A + B + C + \dots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \dots$

## De Morgan's Theorems

It can be stated in words as follows:

(a) The complement of the product of variables is equal to the sum of the complements of the individual variables.

(b) The complement of the sum of variables is equal to the product of individual complements of variables.

⇒ are extensively used in the simplification of Boolean expressions and in the design of switching networks.

Truth Table for verification of De Morgan's first theorem

A	B	$A \oplus B$	$\overline{A \oplus B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Verification of De Morgan's  
Second theorem

A	B	$A \cdot B$	$\bar{A} \cdot \bar{B}$	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Simplification of Boolean expressions

Illustrations:-

$$\begin{aligned} 1) \quad A \cdot (A+B) &= A \cdot A + A \cdot B \\ &= A + AB \\ &= A(1+B) \\ &= A \end{aligned}$$

$$\begin{aligned} 2) \quad A \cdot (\bar{A}+B) &= A \cdot \bar{A} + AB \\ &= 0 + AB \\ &= AB \end{aligned}$$

$$\begin{aligned} 3) \quad (x+y)(x+z) &= x \cdot x + x \cdot z + y \cdot x + y \cdot z \\ &= x + x \cdot z + x \cdot y + y \cdot z \\ &= x[1 + z + y] + y \cdot z \\ &= x + y \cdot z \end{aligned}$$

$$\begin{aligned} 4) \quad A + \bar{A}B &= A \cdot (1) + \bar{A}B \\ &= A(1+B) + \bar{A}B \\ &= A + AB + \bar{A}B \\ &= A + B(A + \bar{A}) \\ &= A + B(1) \\ &= A + B \end{aligned}$$

$$\begin{aligned}
 5) (\bar{P} + Q)(P + Q) &= \bar{P}P + \bar{P}Q + QP + QQ \\
 &= 0 + \bar{P}Q + QP + Q \\
 &= Q[\bar{P} + P + 1] \\
 &= Q
 \end{aligned}$$

$$\begin{aligned}
 6) ABC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}C \\
 &= ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC \\
 &= AB[C + \bar{C}] + C(A\bar{B} + \bar{A}B) \\
 &= AB + A\bar{B}C + \bar{A}BC \\
 &= A[B + \bar{B}C] + \bar{A}BC \\
 &= A[B + C] + \bar{A}BC \\
 &= AB + AC + \bar{A}BC \\
 &= AB + C(A + \bar{A}B) \\
 &= AB + C(A + B) \\
 &= AB + BC + CA
 \end{aligned}$$

### Binary Number System

The binary number system uses only two digits 0 and 1. The numbers in this system have a base of 2. Digits 0 and 1 are called bits and 8 bits together make a byte.

⇒ 10001<sub>2</sub>, 111101<sub>2</sub>, 1010101<sub>2</sub> are examples of numbers in binary number system.

Octal number system It uses eight digits 0, 1, 2, 3, 4, 5, 6 and 7 with the base of 8.

⇒ 35<sub>8</sub>, 23<sub>8</sub>, 141<sub>8</sub> are examples of numbers in octal number system

## Decimal number system

It uses ten digits: 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9 with the base 10.

⇒ Example  $723_{10}, 32_{10}, 4257_{10}$

## Hexadecimal number system

It uses sixteen digits/alphabets.  
0, 1, 2, 3, 4, 5, 6, 7, 8 and 9 and  
A, B, C, D, E, F with the base 16

⇒ Example  $7B3_{16}, 6F_{16}, 4B2A_{16}$

### Problem:

1) Convert the decimal 9 to binary.

### Solution:

$$\begin{aligned} 9 &= 8 + 1 \\ &= 2^3 + 2^0 \\ &= 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\ \therefore (9)_{10} &= 1001_2 \end{aligned}$$

$$\begin{aligned} (26)_{10} &= 16 + 8 + 2 \\ &= 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 \times 1 + 2^1 + 0 \times 2^0 \\ &= (11010)_2 \end{aligned}$$

$$\begin{aligned} (82)_{10} &= 64 + 16 + 2 \\ &= 1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 \\ &\quad + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 \\ &= (1010010)_2 \end{aligned}$$

Problem: Convert the decimal number 99 to binary

$$\begin{array}{r}
 & 99 \\
 2 | & 49 \\
 & \hline
 & 24 \\
 2 | & 12 \\
 & \hline
 & 6 \\
 2 | & 3 \\
 & \hline
 & 1
 \end{array}
 \quad \text{Reminder}
 \quad \begin{array}{r}
 1 \\
 1 \\
 0 \\
 0 \\
 0 \\
 1 \\
 1
 \end{array}$$

∴ Binary equivalent is 1100011

Problem: Convert the octal number 1527 to decimal number

$$\begin{aligned}
 (1527)_8 &= 1 \times 8^3 + 5 \times 8^2 + 2 \times 8^1 + 7 \times 8^0 \\
 &= 512 + 5 \times 64 + 16 + 7 \\
 &= (855)_{10}
 \end{aligned}$$

Conversion of octal to binary

Octal	binary
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1

Problem:

Convert

$\Rightarrow (251)_8$  to binary numbers

$$= \begin{array}{r} 010 \\ \times 2 \\ \hline 101 \end{array}$$

$$= (010101)_2$$

$$\Rightarrow (51)_8 = \begin{array}{r} 101 \\ \times 5 \\ \hline 001 \end{array}$$

$$= (101001)_2$$

$$\Rightarrow (47)_8 = \begin{array}{r} 100 \\ \times 4 \\ \hline 111 \end{array}$$

$$= (100111)_2$$

Representation of numbers in various number systems

Deci mal	Binary	Octal	Hexa decimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Convert

$$\Rightarrow (1011\ 0011)_2 = (B3)_{16}$$

$$\Rightarrow (110\ 0111\ 01000)_2$$

$$= \frac{1100}{C(12)} \quad \frac{1110}{E(14)} \quad \frac{1000}{8}$$

$$= (CE8)_{16}$$

Gray Code: The reflected binary code (RBC), also known as reflected binary (RB) or Gray code after Frank Gray, is an ordering of the binary numerical system such that two successive values differ in only one bit (binary digit).

⇒ For example, the representation of the decimal value "1" in binary would normally be "001" and "2" would be "010". In Gray code, these values are represented as "001" and "101". That way, incrementing a value from 1 to 2 requires only one bit to change, instead of two.

⇒ Applications: Gray codes are widely used to prevent spurious output from electromechanical switches and to facilitate error correction in digital communications such as some cable TV systems.

ASCII Code: ⇒ Abbreviated from American Standard Code for information interchange, is a character encoding standard for electronic communication. ASCII codes represent text in computers, telecommunications equipment and other devices.

BCD Binary Coded Decimal or BCD is another process for converting decimal numbers into their binary equivalents.

It is a form of binary encoding where each digit in a decimal number is represented in the form of bits.

⇒ Truth Table for Binary Coded Decimal

Decimal Number	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Problem: ⇒ convert  $(123)_{10}$  in BCD

$$1 - 0001$$

$$2 - 0010$$

$$3 - 0011$$

∴ BCD becomes 0001 0010 0011

2) Convert  $(324)_{10}$  in BCD

$$3 - 0011$$

$$2 - 0010$$

$$4 - 0100$$

∴ BCD → 0011 0010 0100

## Logic Gates

Three operations:-

- 1) OR addition (+) sign
- 2) AND multiplication ( $\times$  or .) sign
- 3) NOT operation indicated by a bar over a variable.

### OR Addition

$Y = A + B$  in Boolean algebra  
reads 'Y equals A or B'

⇒ Truth table

Input		Output
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

$Y = A + B + \dots + N$   
reads 'Y equals A or B or ... N'

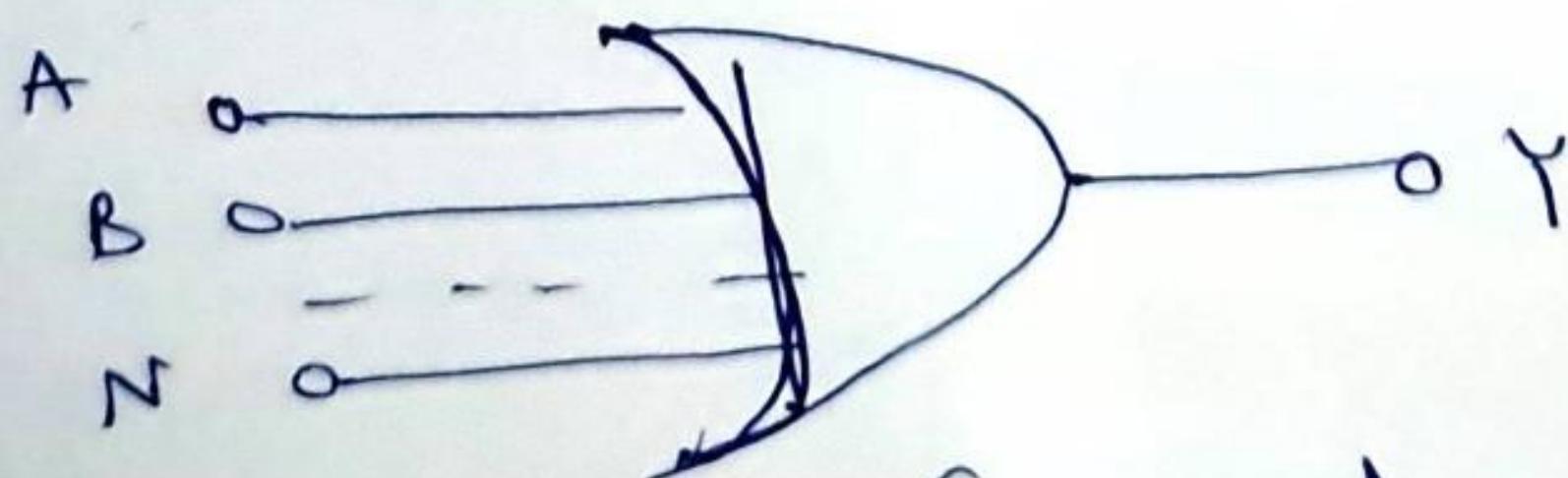


Figure: Symbol of an OR gate

## AND multiplication

$$Y = A \times B$$

$$\text{or } Y = A \cdot B$$

$$\text{or } Y = AB$$

reads "Y equals A and B"

⇒ Truth table

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$Y = AB \dots N$$

reads "Y equals A and B --- and N"

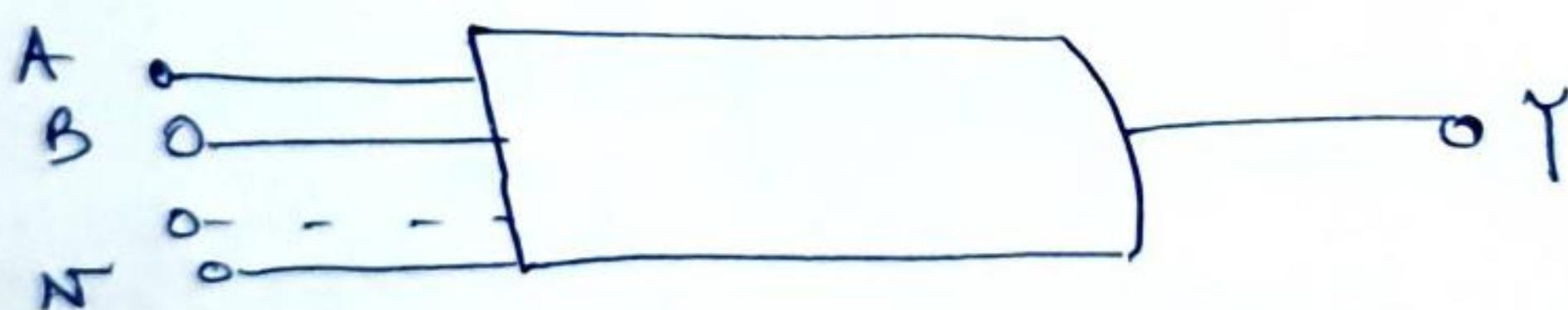


Figure: Symbol of an AND gate

## NOT operation

The NOT operation on a variable A is represented by  $\bar{A}$ .

i) If  $A = 0$ ,  $\bar{A} = 1$

ii) If  $A = 1$ ,  $\bar{A} = 0$

$$Y = \bar{A}$$

reads 'Y equals NOT A'

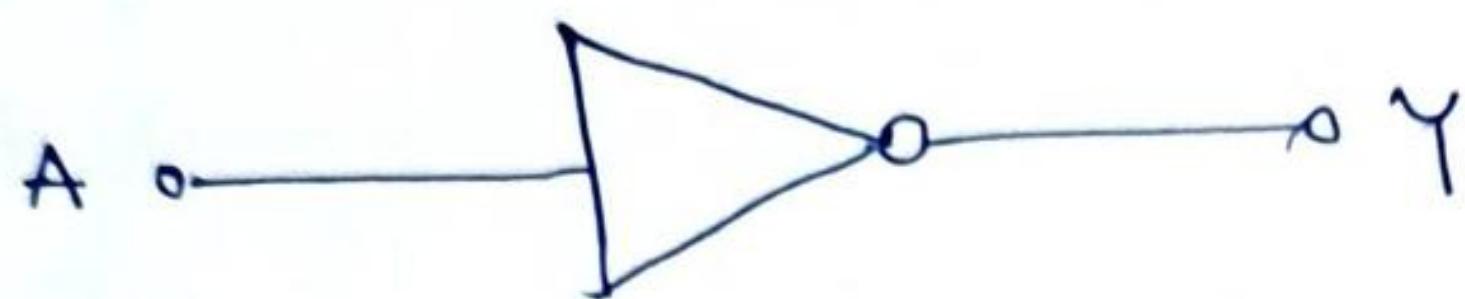


Figure: Symbol for a NOT gate

⇒ Truth table

Input A	Output Y
0	1
1	0

Prove that: i)  $\overline{A+B} = \overline{A} \cdot \overline{B}$

and ii)  $\overline{A \cdot B} = \overline{A} + \overline{B}$

### NOR gate

As per the proof of

$$\overline{A+B} = \overline{\overline{A} \cdot \overline{B}}$$
, an OR gate

followed by a NOT gate functions identically as an AND gate whose inputs are the outputs of two NOT gates

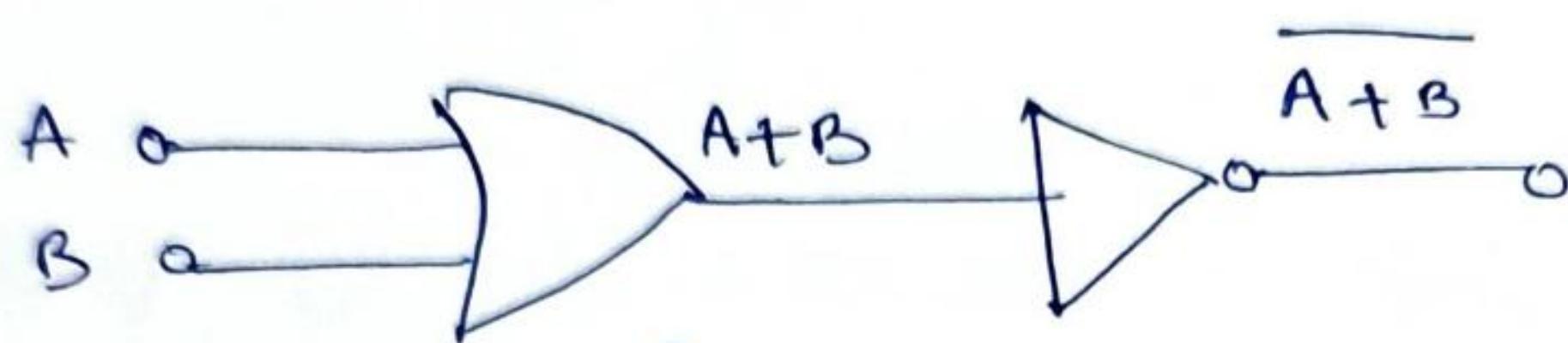


figure 1

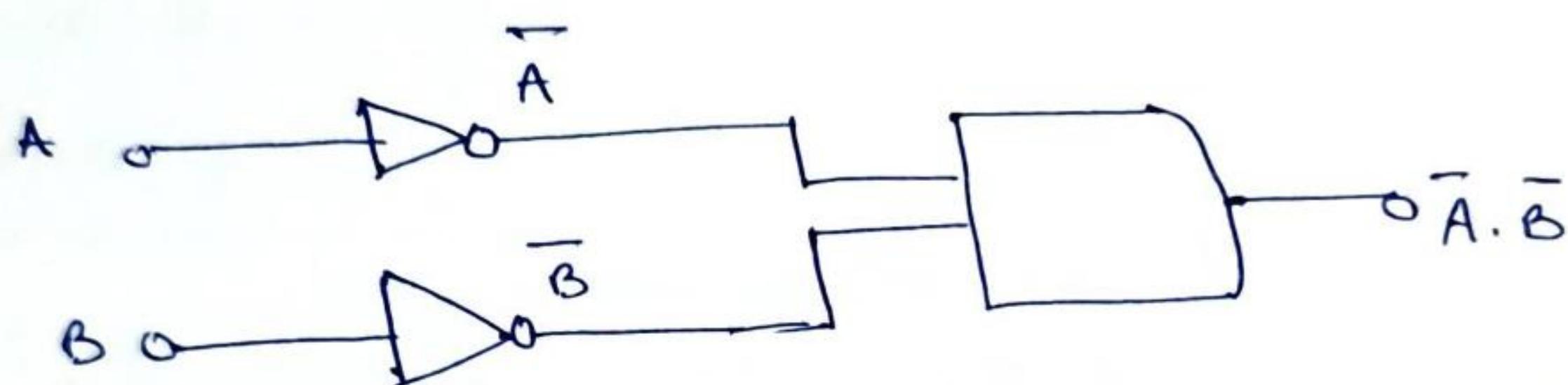


figure 2

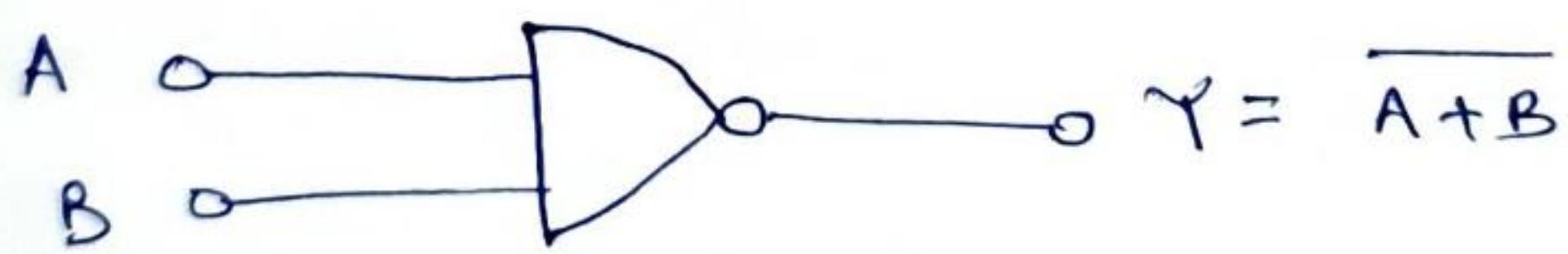


figure 3: Logic symbol of  
a NOR gate

$$Y = \overline{A+B}$$

Truth table  $\Rightarrow$

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$\Rightarrow$  NOR gate is said to be the universal building block of all digital circuits.

### NAND gate

As per the proof of  $\overline{A \cdot B} = \overline{\overline{A}} + \overline{\overline{B}}$ , an AND gate followed by a NOT gate functions identically as an OR gate whose inputs are the outputs of two NOT circuits.

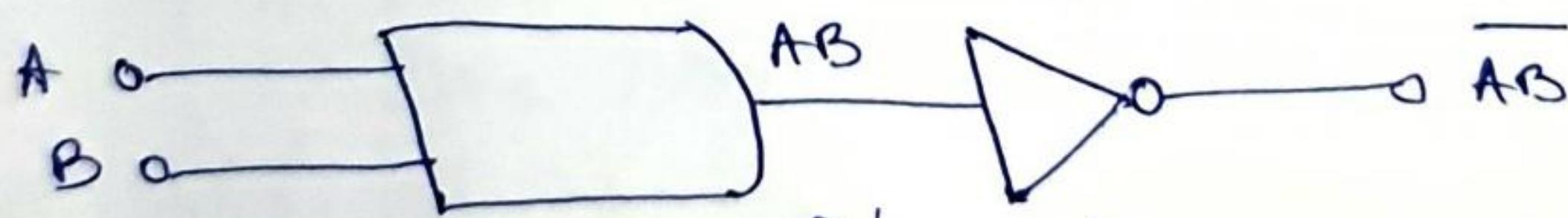


Figure 1

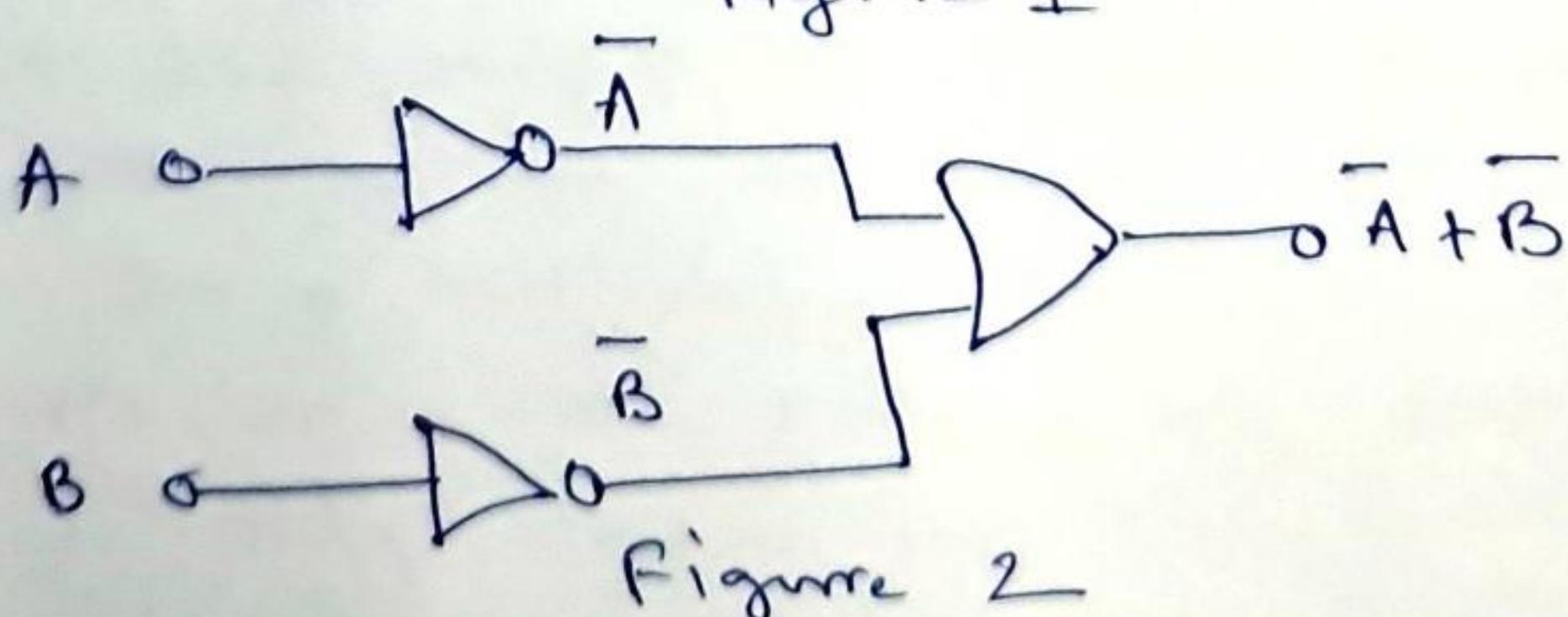


Figure 2

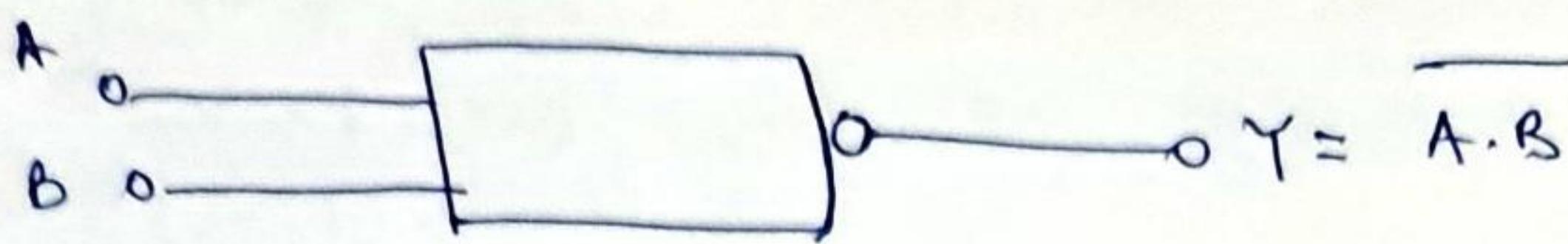


Figure 3. Logic symbol of  
NAND gate

$$Y = \overline{A \cdot B}$$

Truth table  $\Rightarrow$

Input		Output
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

$\Rightarrow$  NAND gate is said to be the universal building block of all digital circuits.

### EX-OR gate

$\Rightarrow$  The conventional OR gate is also referred to as an inclusive OR gate

$\Rightarrow$  The output of OR gate is high when one or all the inputs are high

$\Rightarrow$  In a two input exclusive OR gate or X-OR gate, the output is high only when any one of the inputs is high.

⇒ when both inputs are high or both inputs are low, the output is low.

$$Y = A \oplus B \\ = A\bar{B} + B\bar{A}$$

The Boolean expression

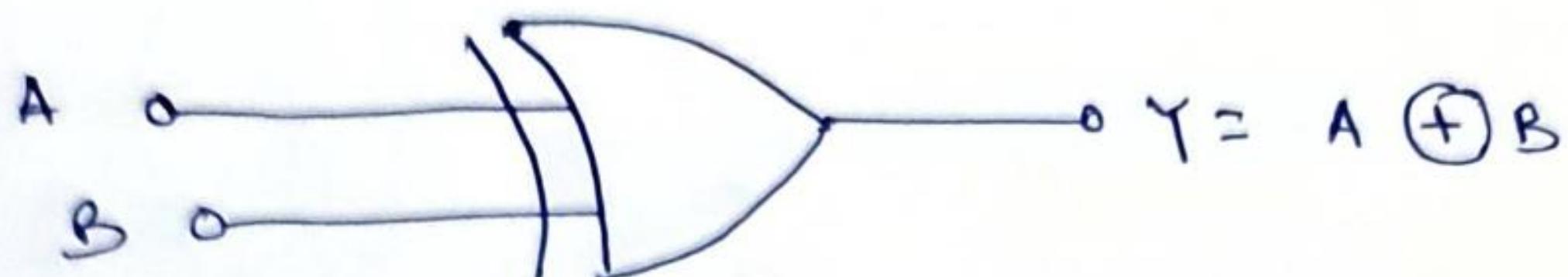


Figure: Circuit symbol of X-OR gate.

⇒ Truth table

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

### X-NOR gate

⇒ The output of X-NOR gate is the complement of the output of X-OR gate.

$$Y = \overline{A \oplus B}$$

The Boolean expression

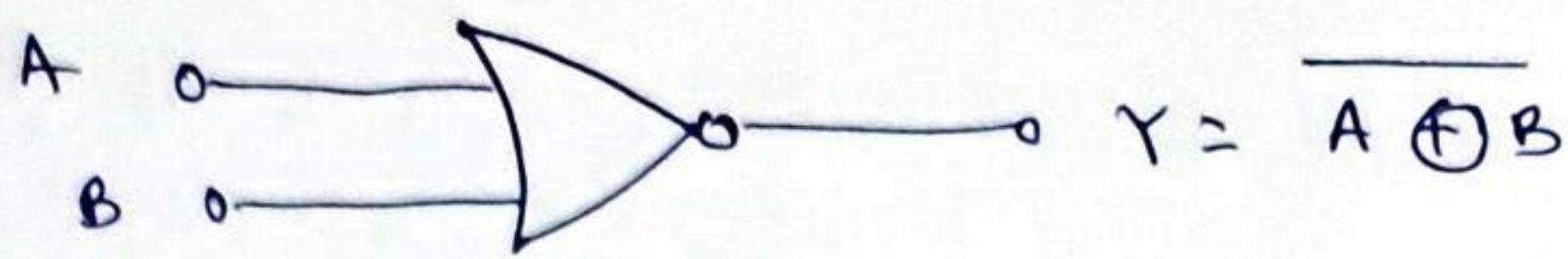


Figure: Logic symbol of X-NOR gate

⇒ Truth table

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

### Simplification of Logic functions

$$\begin{aligned} 1) \quad A \cdot (A + B) &= A \cdot A + A \cdot B \\ &= A + AB \\ &= A(1 + B) \\ &= A \end{aligned}$$

$$\therefore A \cdot (A + B) = A$$

$$\begin{aligned} 2) \quad A \cdot (\bar{A} + B) &= A \cdot \bar{A} + AB \\ &= 0 + AB \\ &= AB \end{aligned}$$

$$\begin{aligned} 3) \quad (x + y)(x + z) &= x \cdot x + x \cdot z + y \cdot x + y \cdot z \\ &= x + x \cdot z + x \cdot y + y \cdot z \\ &= x[1 + z + y] + y \cdot z \\ &= x + y \cdot z \end{aligned}$$

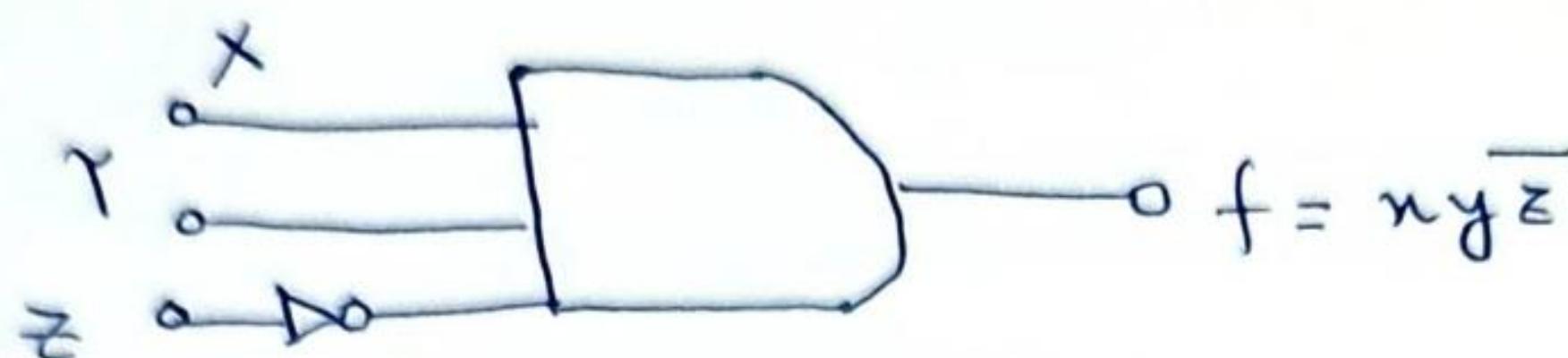
$$\begin{aligned}
 4) \quad Y &= A + \bar{A}B \\
 &= A \cdot 1 + \bar{A} \cdot B \\
 &= A(1+B) + \bar{A}B \\
 &= A + AB + \bar{A}B \\
 &= A + B(A + \bar{A}) \\
 &= A + B(1) \\
 &= A + B
 \end{aligned}$$

$$\begin{aligned}
 5) \quad Y &= (\bar{P} + Q)(P + Q) \\
 &= \bar{P} \cdot P + \bar{P} \cdot Q + Q \cdot P + Q \cdot Q \\
 &= 0 + \bar{P} \cdot Q + Q \cdot P + Q \\
 &= Q[\bar{P} + P + 1] \\
 &= Q
 \end{aligned}$$

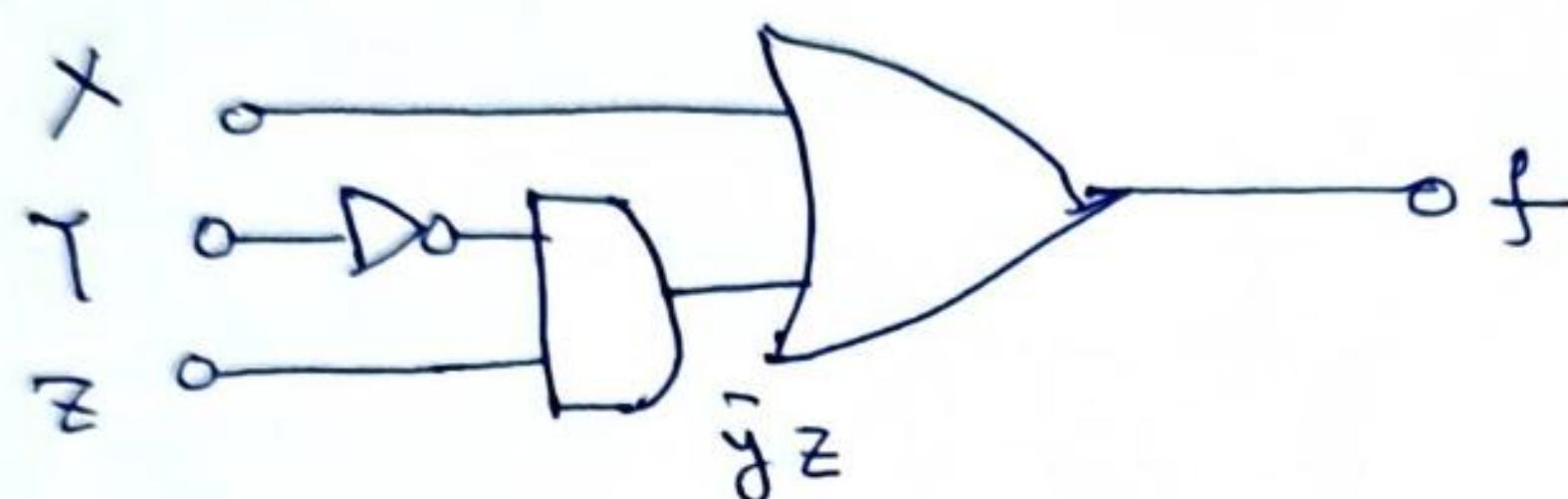
$$\begin{aligned}
 6) \quad Y &= ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC \\
 &= ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC \\
 &= AB(C + \bar{C}) + A\bar{B}C + \bar{A}BC \\
 &= AB + A\bar{B}C + \bar{A}BC \\
 &= A[B + BC] + \bar{A}BC \\
 &= A[B + C] + \bar{A}BC \\
 &= AB + AC + \bar{A}BC \\
 &= AB + C(A + \bar{A}B) \\
 &= AB + C(A + B) \\
 &= AB + BC + CA
 \end{aligned}$$

## Realizations of logic expressions using logic gates

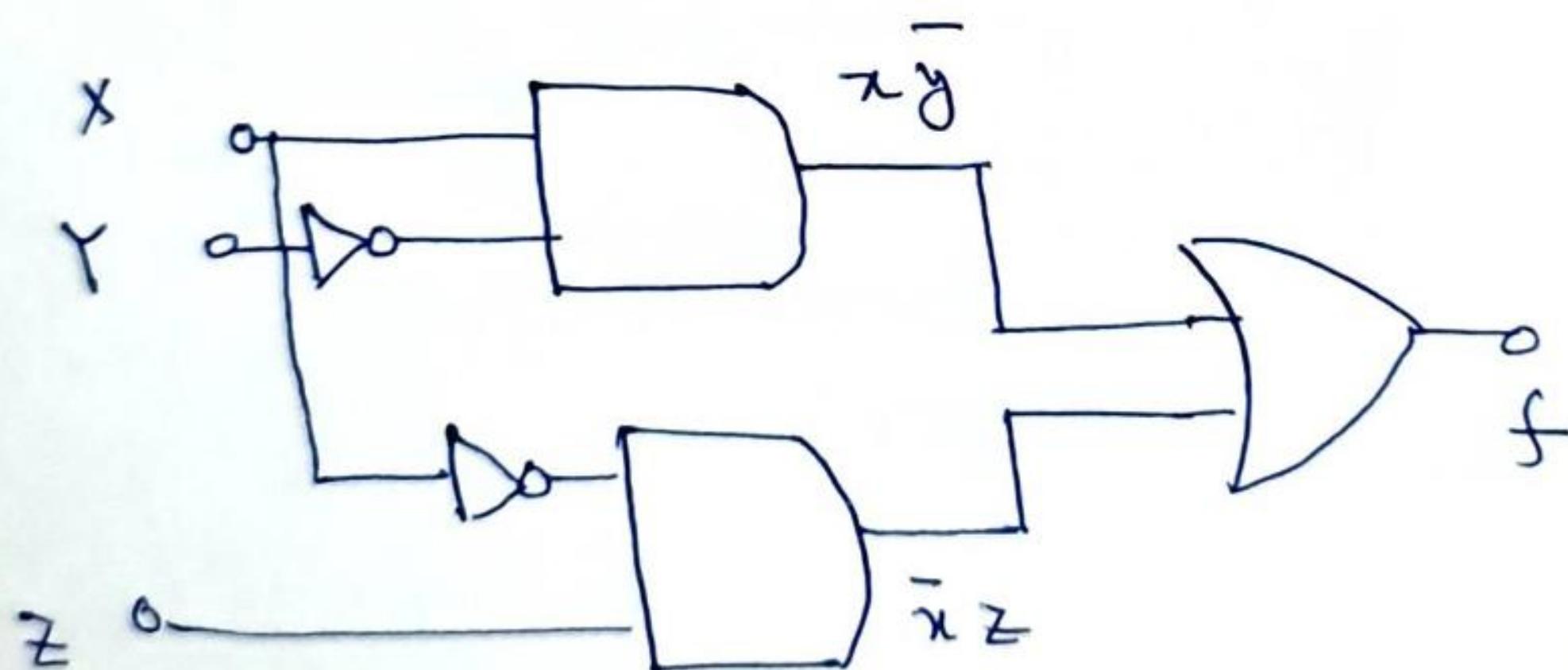
$$1) f = xy\bar{z}$$



$$2) f = x + \bar{y}z$$

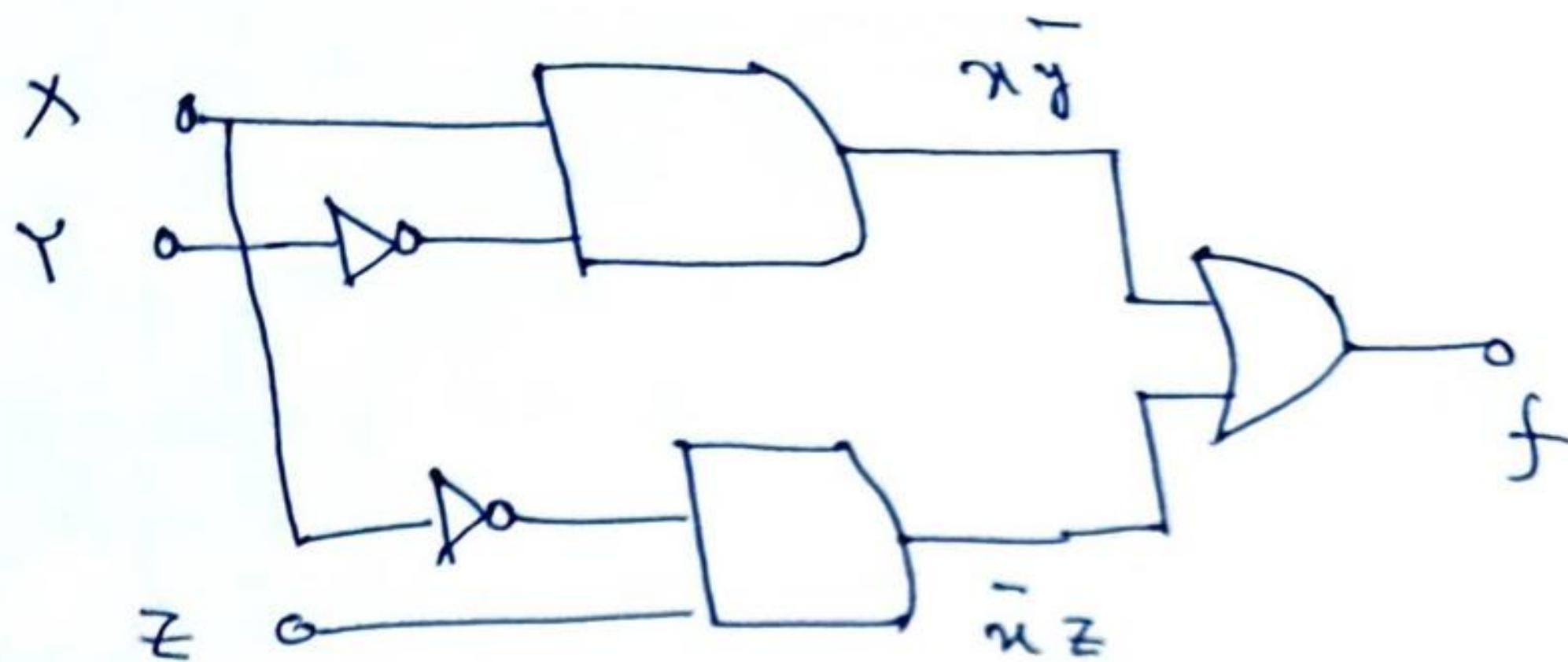


$$3) f = \bar{xy} + \bar{x}z$$



4) Simplify the following Boolean function and realise using logic gates.

$$\begin{aligned}
 f &= \overline{xy}z + \overline{x}yz + xy\overline{z} \\
 &= \overline{x}z(\overline{y} + y) + xy\overline{z} \\
 &= \overline{x}z + xy\overline{z} \quad [\because y + \overline{y} = 1]
 \end{aligned}$$



## CRO and its applications

- CRO  $\Rightarrow$  Cathode Ray oscilloscope
- $\Rightarrow$  Laboratory instrument
  - $\Rightarrow$  used for the measurement and analysis of waveforms and other phenomena in electronic circuits.
  - $\Rightarrow$  very fast X-Y plotters
  - $\Rightarrow$  displays an input signal versus another signal or versus time.
  - $\Rightarrow$  X-axis or horizontal input is an internally generated linear ramp voltage or time base
  - $\Rightarrow$  moves luminous spot periodically from left to right over the screen
  - $\Rightarrow$  Y-axis or vertical input
- ↓  
the voltage under examination
- $\Rightarrow$  CRO can present visual representations of many dynamic phenomena by means of transducers that convert current, pressure, strain, temperature, acceleration and many other physical quantities into voltages.

## Basic CRO operation

The major subsystems are

- (a) Cathode ray tube or CRT
- (b) Vertical amplifier
- (c) Delay line
- (d) Time base generator

- (e) Horizontal amplifier
- (f) Trigger circuit
- (g) Power Supply

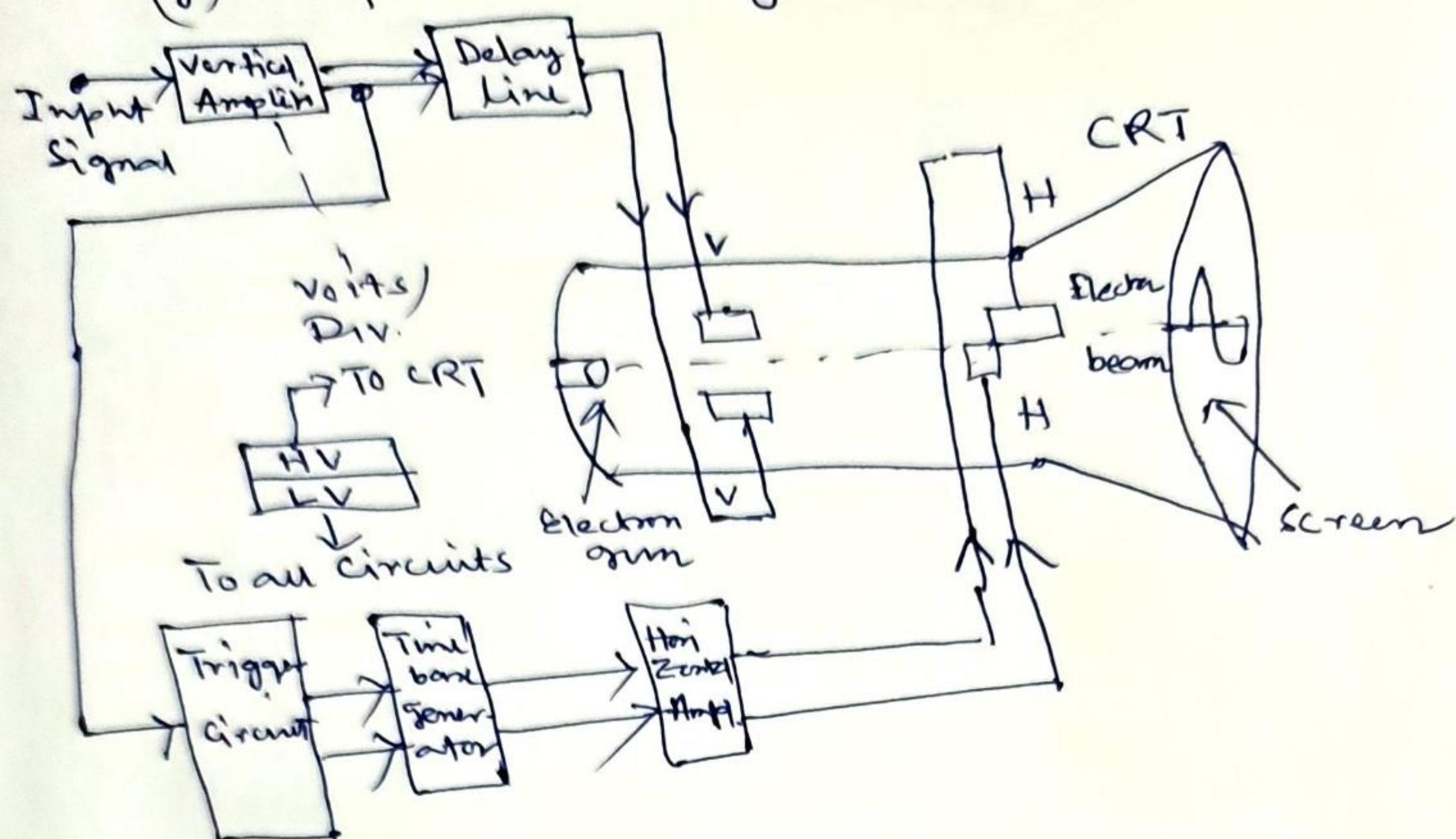


figure: Block diagram of a general purpose oscilloscope.

- ⇒ CRT is the heart of the oscilloscope
- ⇒ rest of the circuit to operate the CRT
- ⇒ the signal waveform to be viewed on the CRT screen is applied to the vertical amplifier input.
- ⇒ the gain of this amplifier is set by a calibrated input attenuator, marked VOLTS/DIV.

⇒ The time base generator develops a saw tooth waveform that is used as the horizontal deflection voltage of the CRT.

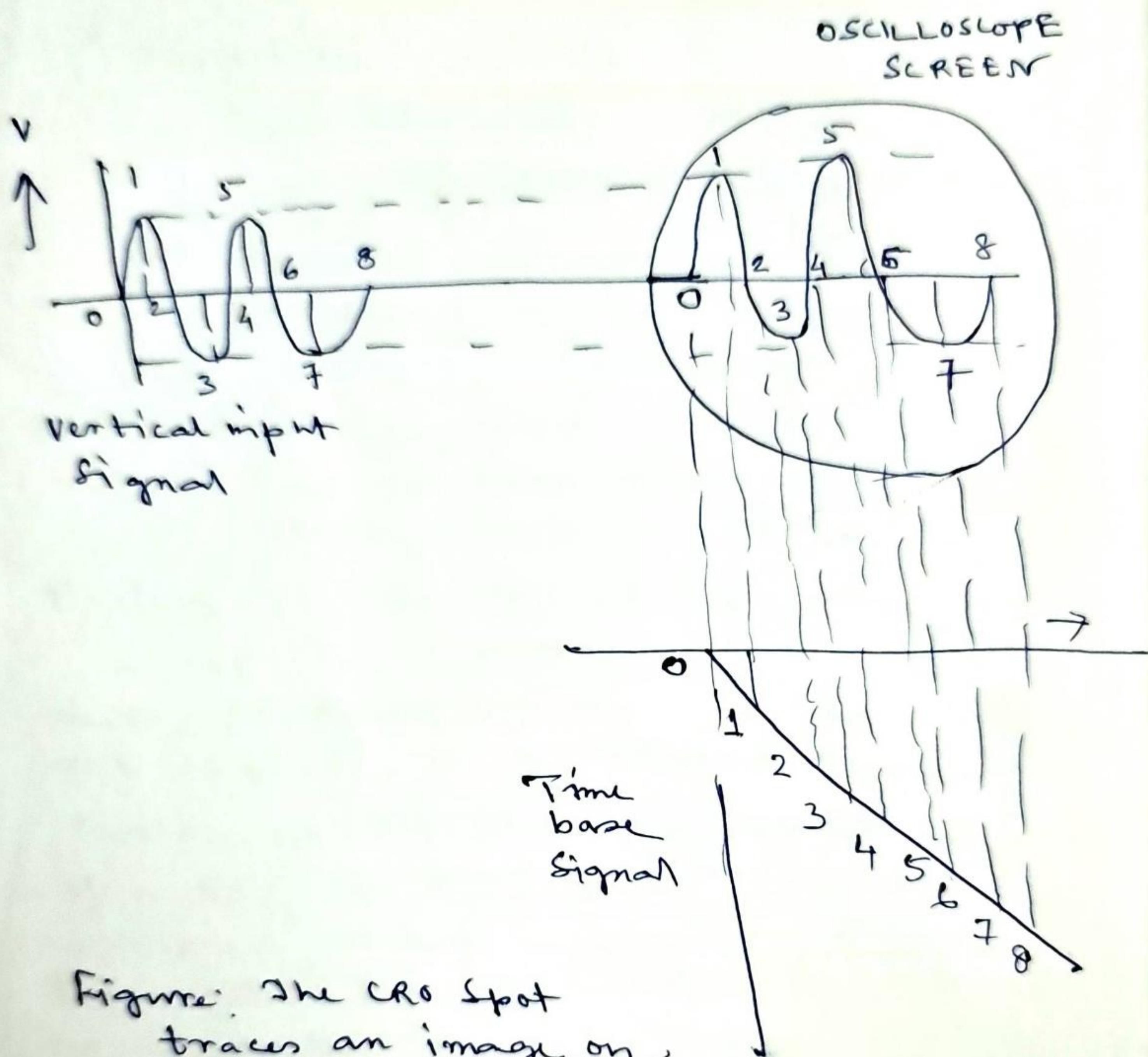


Figure: The CRO Spot traces an image on the screen when horizontal and vertical deflection voltages are applied

## Deflection Sensitivity of CRT

The shift of the spot of light on the screen per unit change in voltage across the deflection plates is known as "deflection sensitivity"

⇒ Spot deflection = Deflection Sensitivity × applied voltage.

⇒ Deflection Sensitivity depends on  
i) design of the tube  
ii) Voltage applied to the accelerating anode.

⇒ Low at high accelerating voltage and vice versa.

Problem: 1) If the deflection sensitivity of a CRT is  $0.01 \text{ mm/V}$ . Find the shift produced in the spot when  $400 \text{ V}$  are applied to the vertical plates.

Problem: 2) If the deflection sensitivity of a CRT is  $0.03 \text{ mm/V}$ . If an unknown voltage is applied to the horizontal plates, the spot shifts  $3 \text{ mm}$  horizontally. Find the value of unknown voltage.