Universidade Federal de Pelotas
Engenharia de Computação
Concepção de Circuitos Integrados
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Relatório sobre o Trabalho Prático
Somador Paralelo de 4 bits

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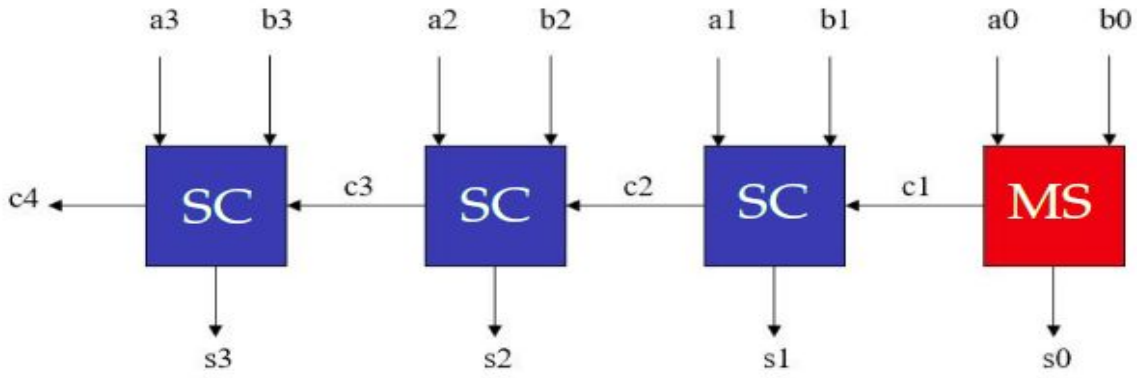
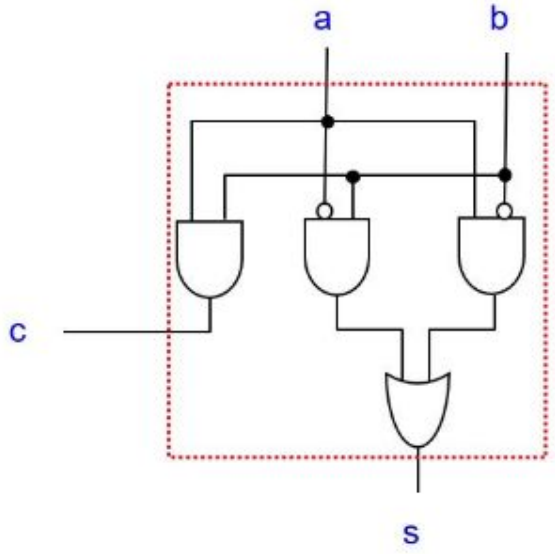
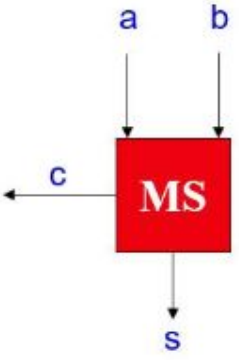
Esquemático de blocos:

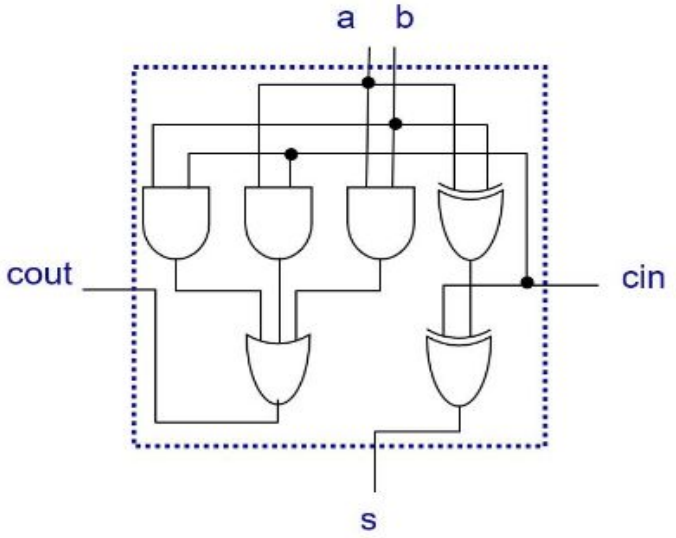


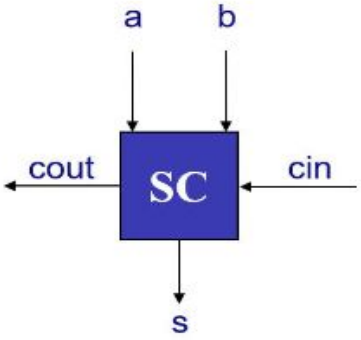




$s = \overline{a} \cdot b + a \cdot \overline{b}$

$c = a \cdot b$





$s = cin \oplus a \oplus b$

$cout = a \cdot b + a \cdot cin + b \cdot cin$

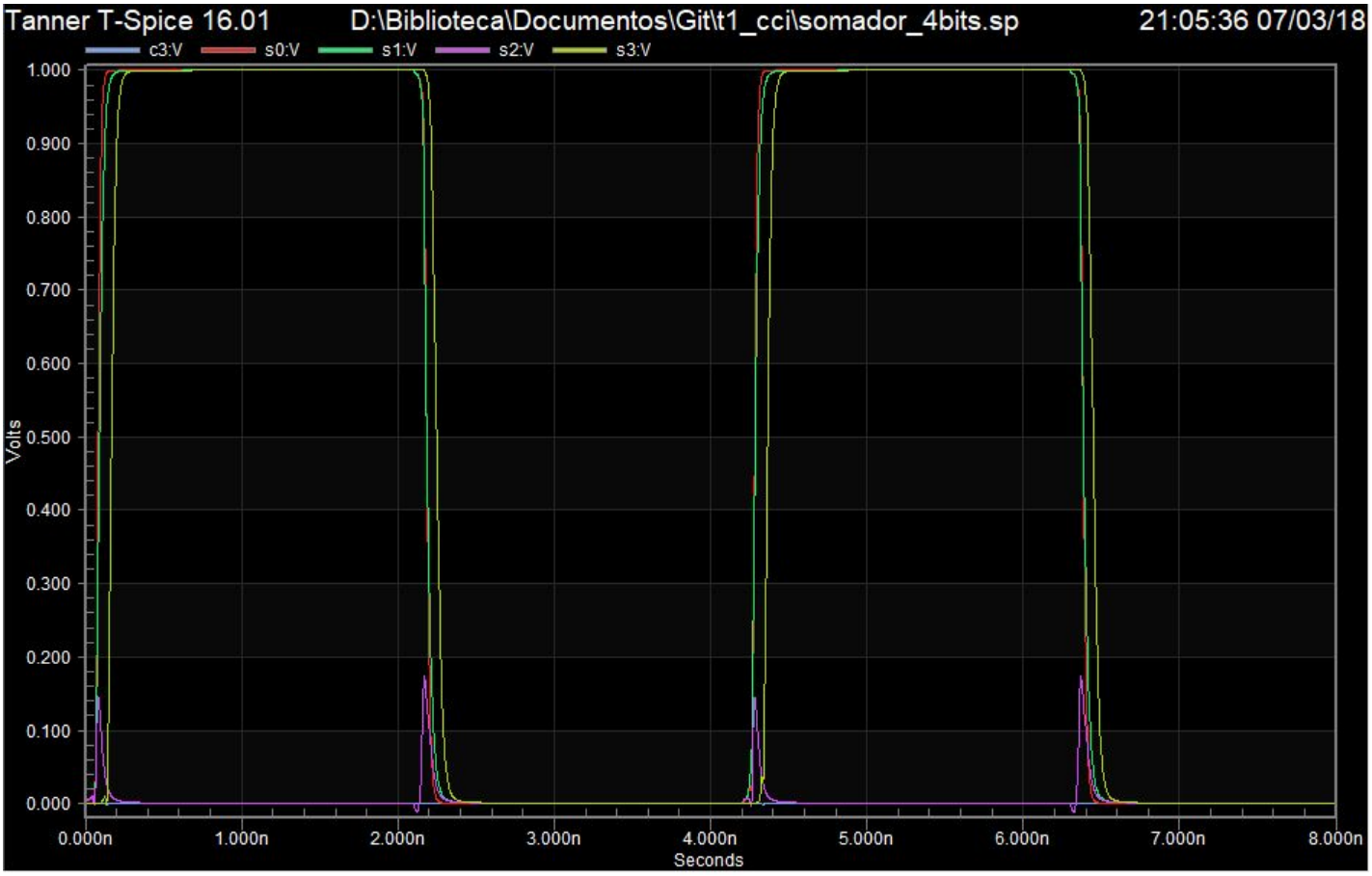
Topologia:

Para o presente trabalho, a topologia escolhida foi BDD.

Dimensionamento dos transistores:

W_pmos	0.1u * 2	W_nmos	0.1u
L_pmos	50n	L_nmos	50n

Formas de onda simuladas:



Dados de atraso:

pHL_s0	2.1347n
pLH_s0	-2.0666n
pHL_s1	2.1350n
pLH_s1	-2.0587n
pHL_s2	not found
pLH_s2	not found
pHL_s3	2.1982n
pLH_s3	-1.9811n

Dados de potência:

consumoCaso1_HL	-13.2118u
consumoCaso1_LH	-12.3909u

Dispositivos e nodos:

MOSFETs	141
MOSFET geometries	2
Capacitors	8
Voltage sources	2
Subcircuits	8
Model Definitions	2
Computed Models	2
Independent nodes	642

Boundary nodes	3
Total nodes	645