VLSI Design
PROJECT

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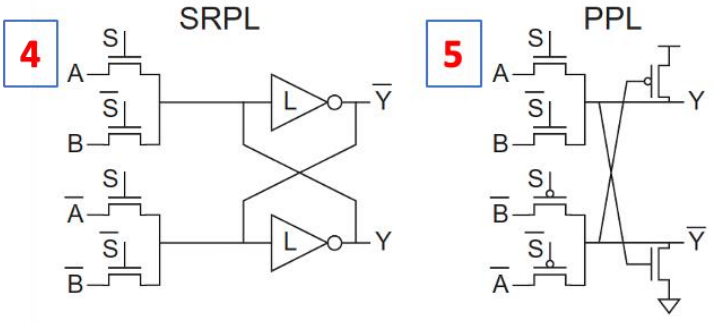
1. **Show via simulations that your design works as a MUX.**



Ans:

SWING RESTORED PASS – TRANSISTOR LOGIC (SRPL)

- The cross-coupled CMOS inverters restore the logic levels.
- Sizing is critical for speed and power dissipation issues.

The parameters that we are considering for this MUX are:

INPUT	RISE TIME	FALL TIME	PULSE WIDTH	PERIOD
A	10ps	10ps	5ns	10ns
B	10ps	10ps	10ns	20ns
S	10ps	10ps	15ns	30ns

S	Y
0	B
1	A

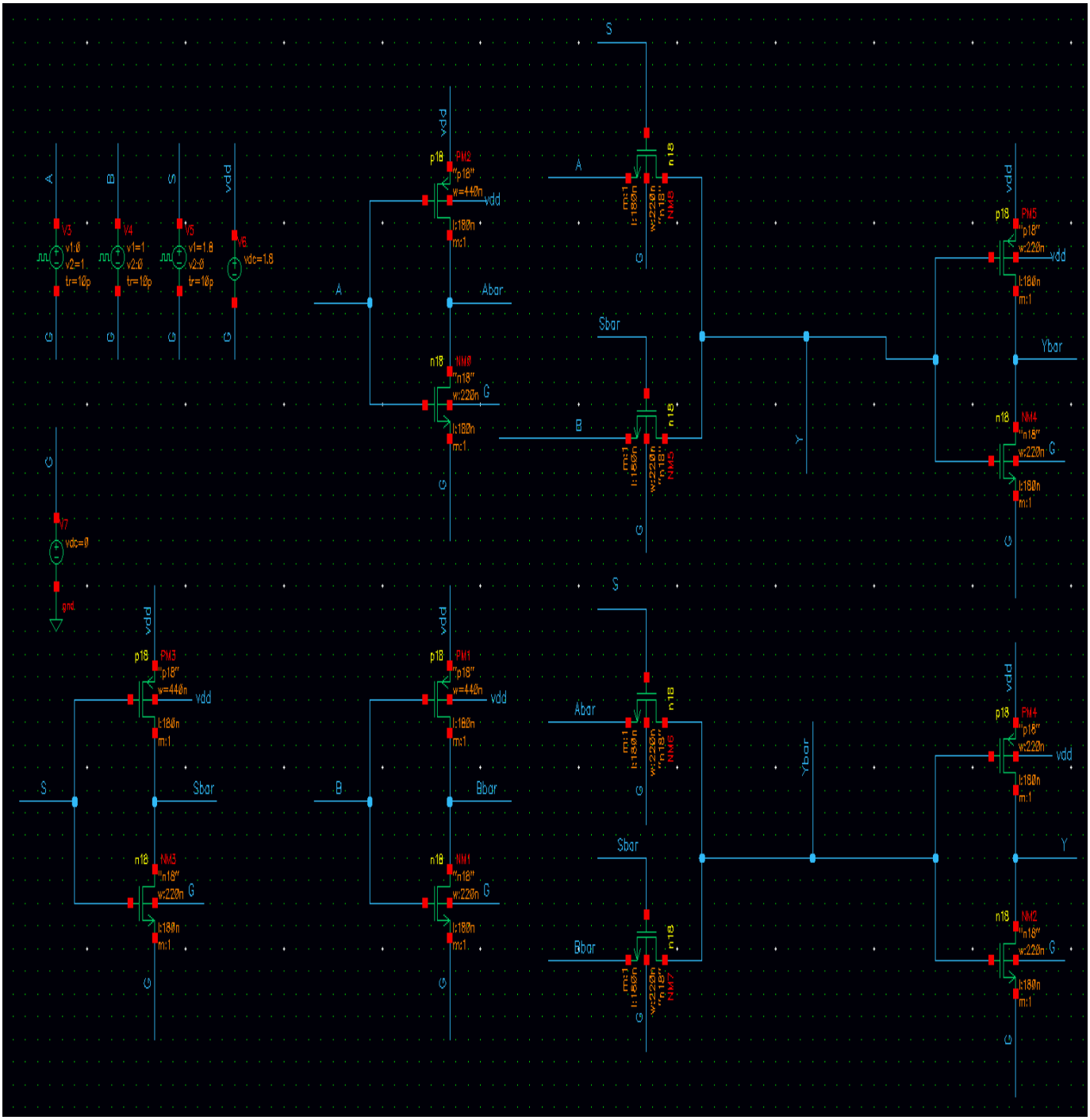


Figure 1.1

The above figure 1.1 shows the circuit diagram of SWING RESTORED PASS – TRANSISTOR LOGIC (SRPL).

The cross-coupled CMOS inverter sizing, in this case, is 1:1 (PMOS: 220nM, NMOS: 220nM)

The length of the designs would be 180nM as we are using 180nM technology.

The area of the design SWING RESTORED PASS – TRANSISTOR LOGIC (SRPL) = Width * Length

The total area of the design = 180 * 3740 = 673200 nM^2 or 673.200uM^2.

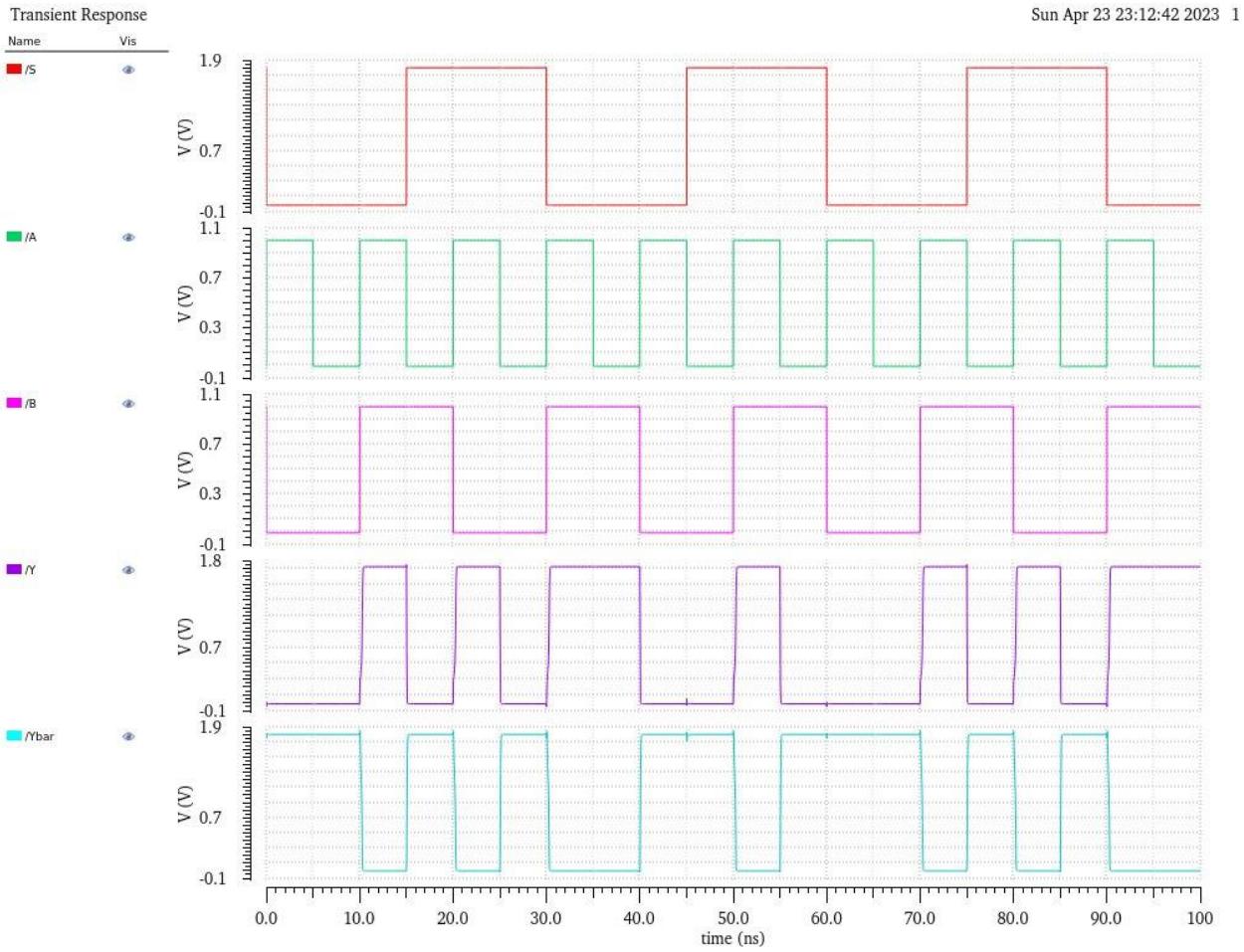


Figure 1.2

- Here in this case Y = A only if S = 1.
- And Y = B only if S = 0.

INPUT			OUTPUT
S	**A**	**B**	**Y**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

PUSH PULL PASS TRANSISTOR LOGIC (PPL)

- It is for low-power and low-voltage applications.
- Provides an efficient logic design by using a push–pull mechanism for level restoration.

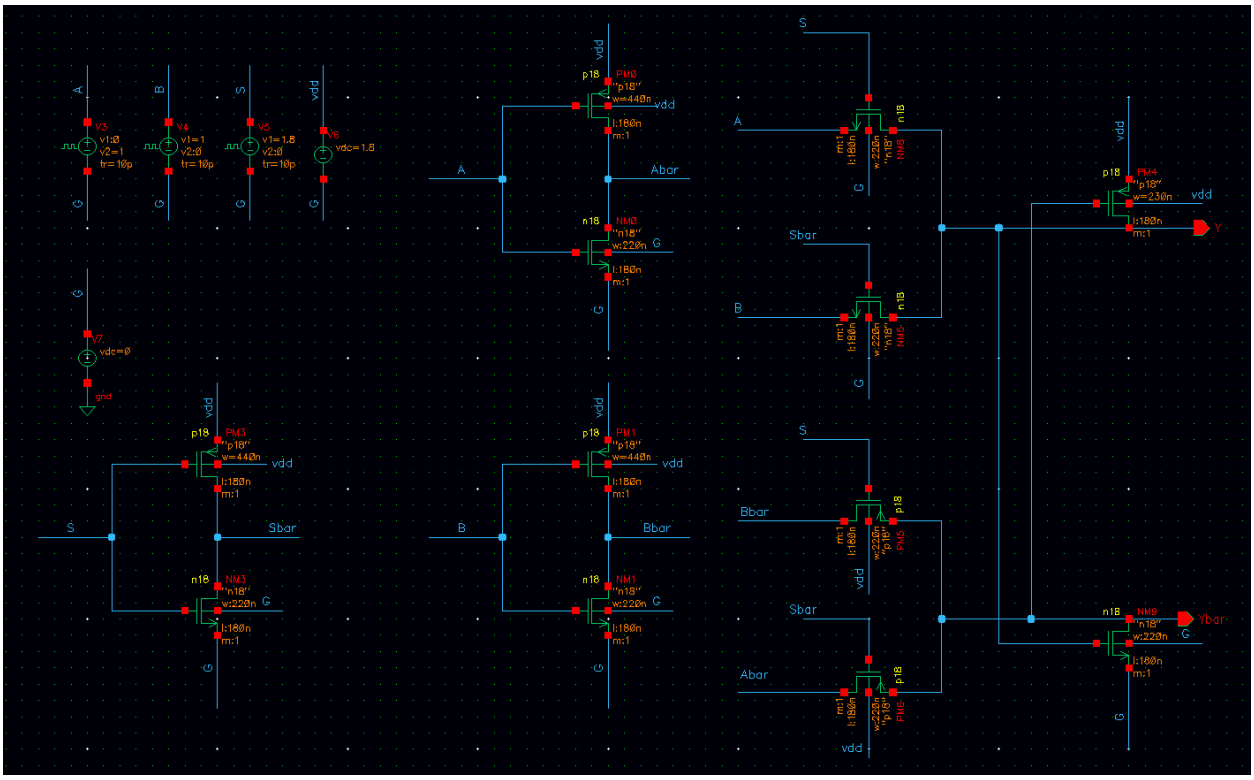


Figure 1.3

The above figure 1.3 shows the circuit diagram of the **PUSH PULL PASS TRANSISTOR LOGIC (PPL).**

The length of the designs would be 180nM as we are using 180nM technology.

The area of the design PUSH PULL PASS TRANSISTOR LOGIC (PPL)= Width * Length

The total area of the design = 180 * 3310 = 595800 nM² or 595.800uM².

INPUT	RISE TIME	FALL TIME	PULSE WIDTH	PERIOD
A	10ps	10ps	5ns	10ns
B	10ps	10ps	10ns	20ns
S	10ps	10ps	15ns	30ns

S	**Y**
0	B
1	A

Case 1:

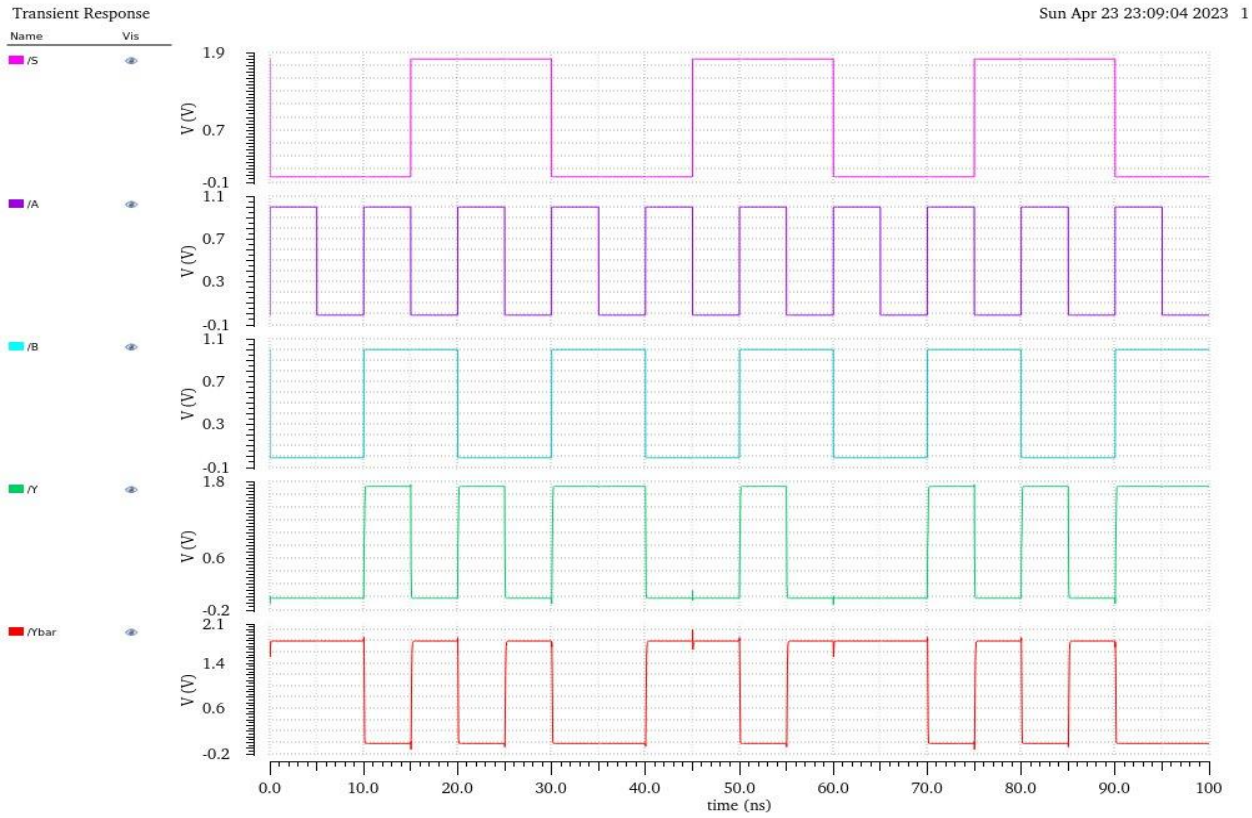


Figure 1.4

- Here in this case Y = A only if S = 1.
- And Y = B only if S = 0.
- Figure 1.4 indicates an analysis of 100ns.

INPUT			OUTPUT
S	**A**	**B**	**Y**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Case 2: Different inputs

INPUT	RISE TIME	FALL TIME	PULSE WIDTH	PERIOD
A	10ps	10ps	5ns	10ns
B	10ps	10ps	12ns	24ns
S	10ps	10ps	18ns	32ns

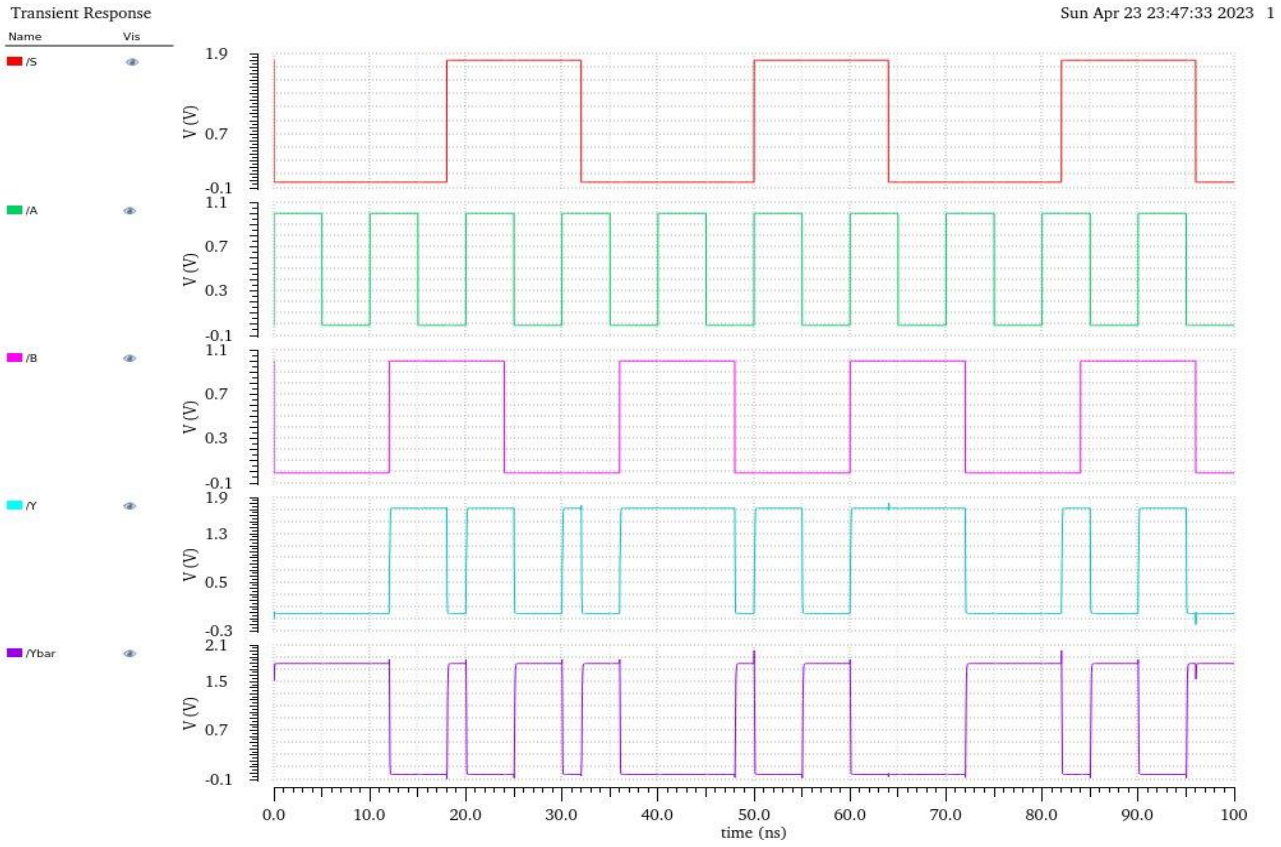


Figure 1.5

- Here in this case Y = A only if S = 1.
- And Y = B only if S = 0.

The total area of the design SWING RESTORED PASS – TRANSISTOR LOGIC (SRPL) = 180 * 3740 = 673200 nM^2 or 673.200uM^2.

The total area of the design PUSH PULL PASS TRANSISTOR LOGIC (PPL)= 180 * 3310 = 595800 nM^2 or 595.800uM^2.

2. **We can use two MUXs to make a D flip flop (D-FF) as shown here. Implement a D-FF following these rules: (a) Mux-1 (the one on the left) should be type-8 MUX, (b) Mux-2 can be one of your MUX designs from Q1. The D-FF must meet the following criteria:**
    a. **For 6000 level students: D-FF must run at atleast 1.5 GHz Clk**
    b. **Full swing should be achieved i.e., Vlow = 0V, Vhigh = 1.8V, at output**

Ans:
Note: The input should arrive before the positive edge of the clock.

D flip-flop (DFF) is a type of flip-flop circuit that stores a single bit of data. It is used to store a value that can be either a logic 0 or a logic 1, and it can be used for various purposes such as storage, synchronization, and sequencing of digital signals.

The D flip-flop has a single input, known as the data (D) input, which is used to set the value of the flip-flop. The output of the flip-flop, known as the Q output, represents the stored value of the flip-flop.

Our design is quite like the master-slave D flip-flop is made up of two D flip-flops, a master flip-flop, and a slave flip-flop, which are triggered on different phases of the clock signal to improve the reliability of the output.

- The condition we are given is that the clock should run at 1.5 GHz.
- Converting it to the time we have a clock period of 0.66ns with a pulse width of 0.33ns.
- $T = 1/f = 1 / (1.5 * 10^9) = 0.66$ ns.

Lean integration with pass transistor (Single – rail pass transistor logic).

- Good output driving capability.

We have implemented two designs:

1. LEAP + PPL
2. LEAP + SRPL

DESIGN 1: LEAP + PPL
Here we are going to analyze 2 multiplexers differently to get an idea of the design.
First, we analyze LEAP and the PPL separately with some random inputs.

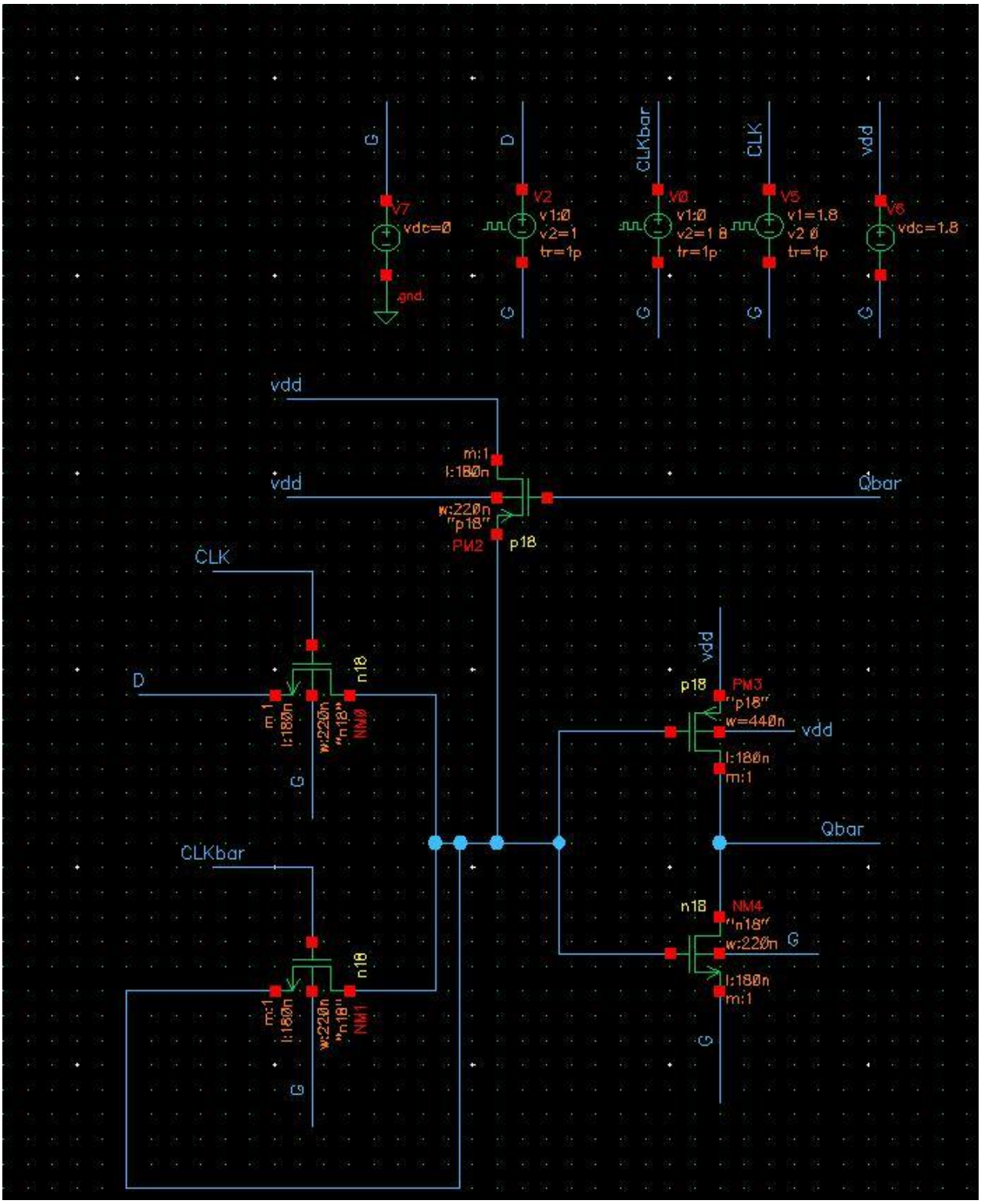


FIGURE 2.1 MUX 1 LEAP

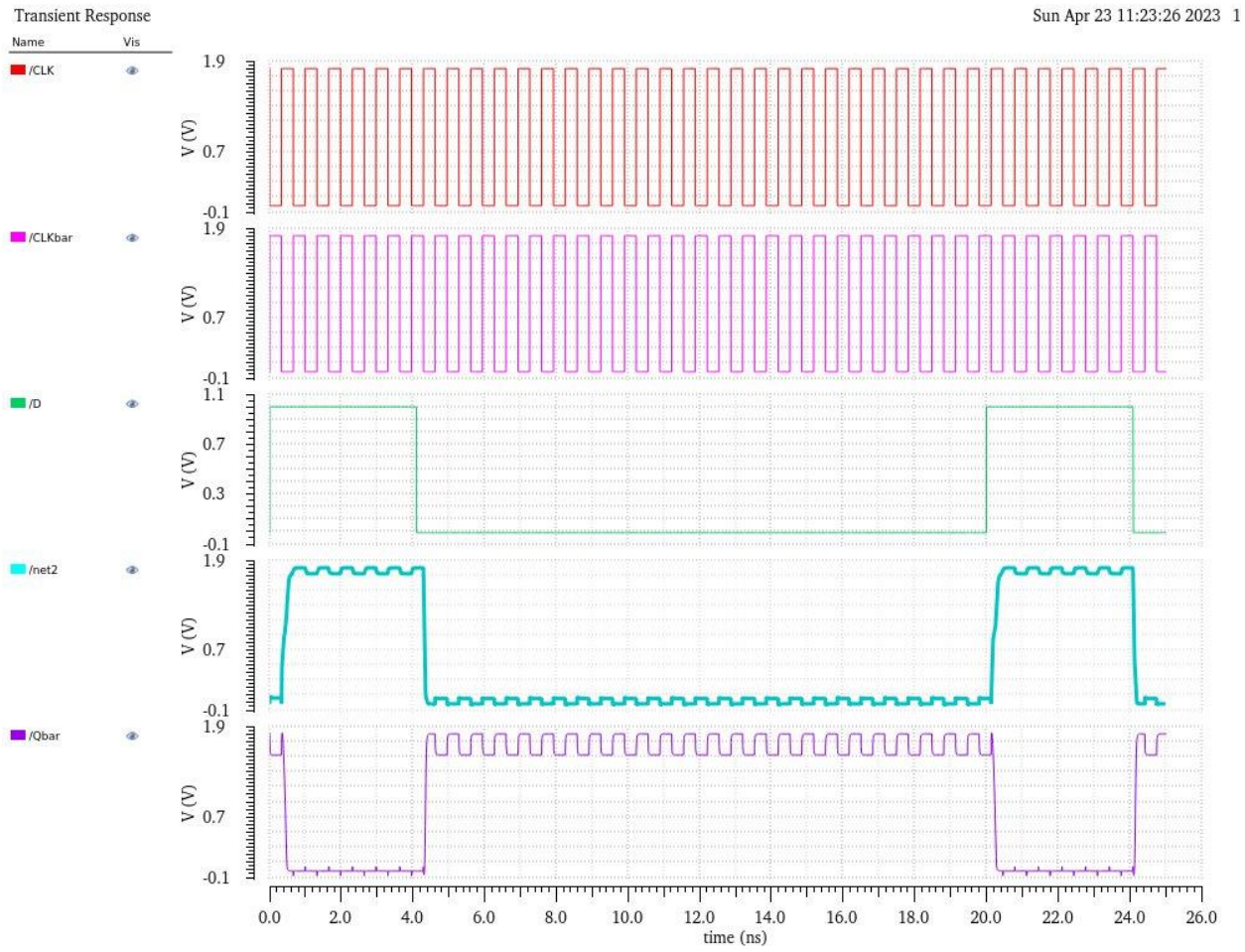


FIGURE 2.2 MUX1 OUTPUT

The operation of the D flip-flop is controlled by a clock input, which is used to trigger the flip-flop to store the value on the D input. When the clock input is high, the D input is sampled and stored in the flip-flop, and the Q output reflects the stored value. When the clock input is low, the flip-flop holds the stored value and does not change its state.

CLK	D	Q(t)	Qbar(t)
1	0	0	1
1	1	1	0
0	X	Q(t-1)	Qbar(t-1)

Truth Table for MUX 1

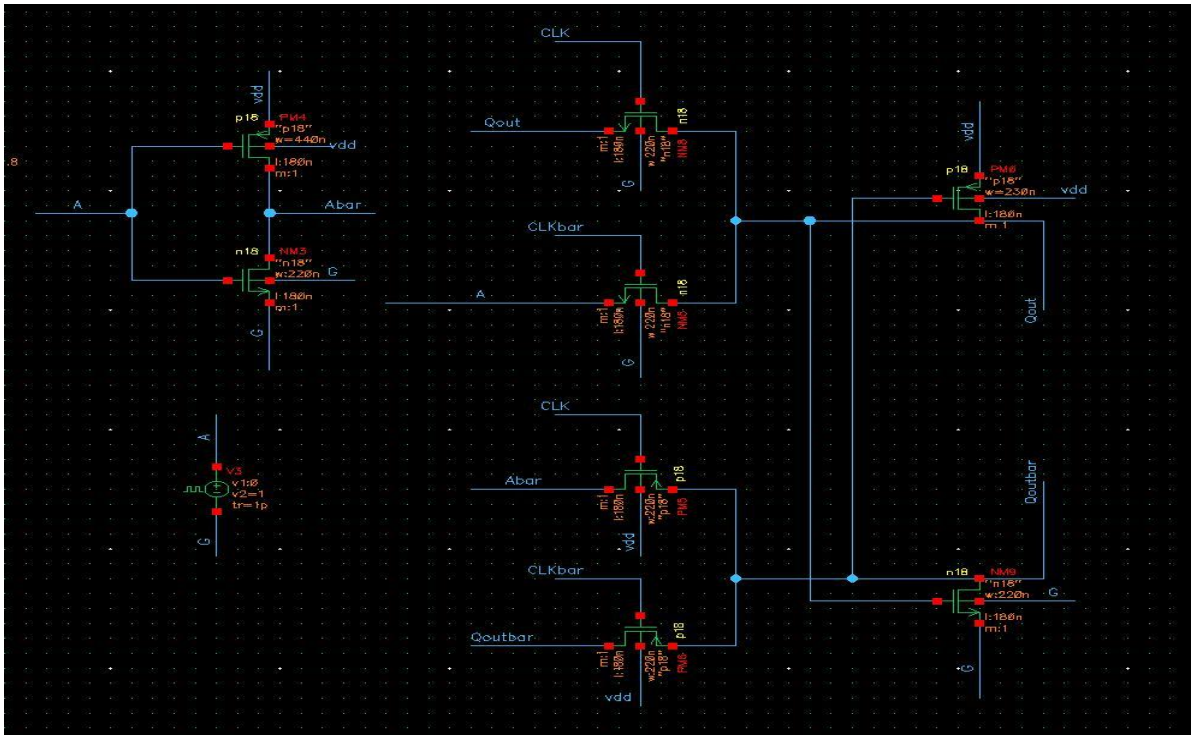


FIGURE 2.3 MUX 2 PPL with different inputs.

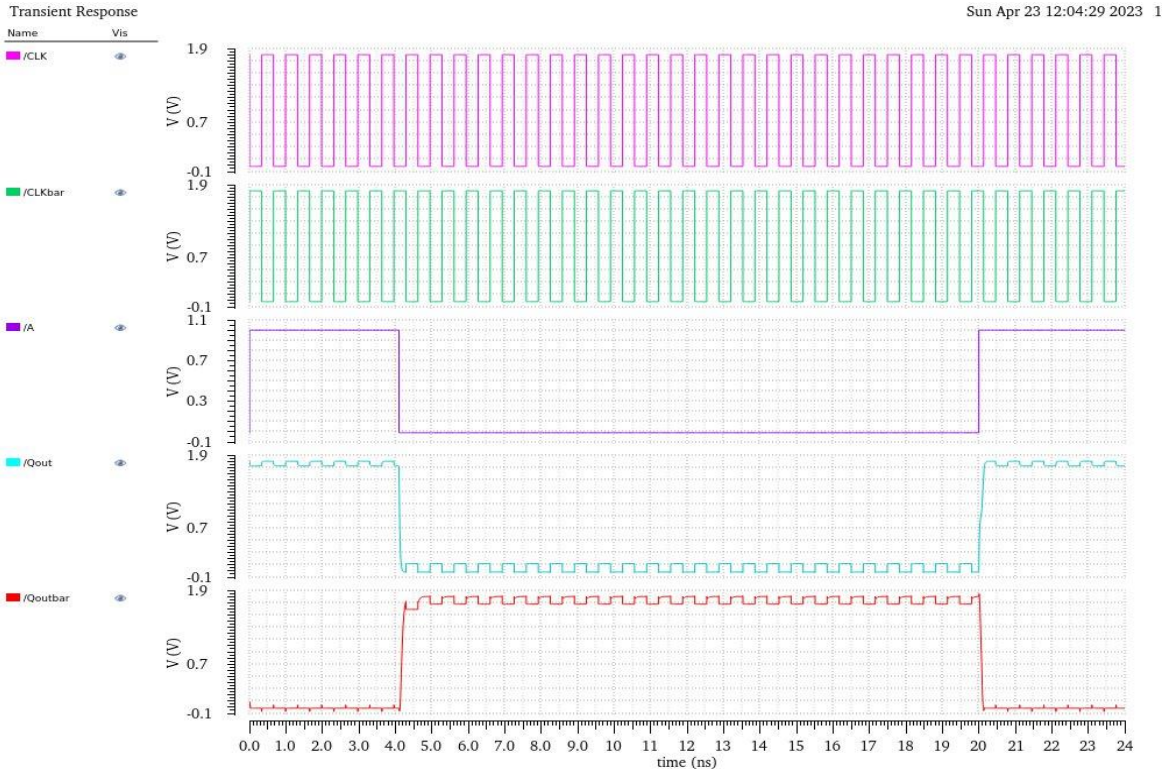


FIGURE 2.4 MUX2 OUTPUT

In this case, the operation of the D flip-flop is controlled by a clock input, which is used to trigger the flip-flop to store the value on the D input. When the clock input is low, the D input is sampled and stored in the flip-flop, and the Q output reflects the stored value. When the clock input is high, the flip-flop holds the stored value and does not change its state.

CLK	D	Q(t)	Qbar(t)
0	0	0	1
0	1	1	0
1	X	Q(t-1)	Qbar(t-1)

Truth Table for MUX 2

Now combining both the MUX.

DESIGN 1

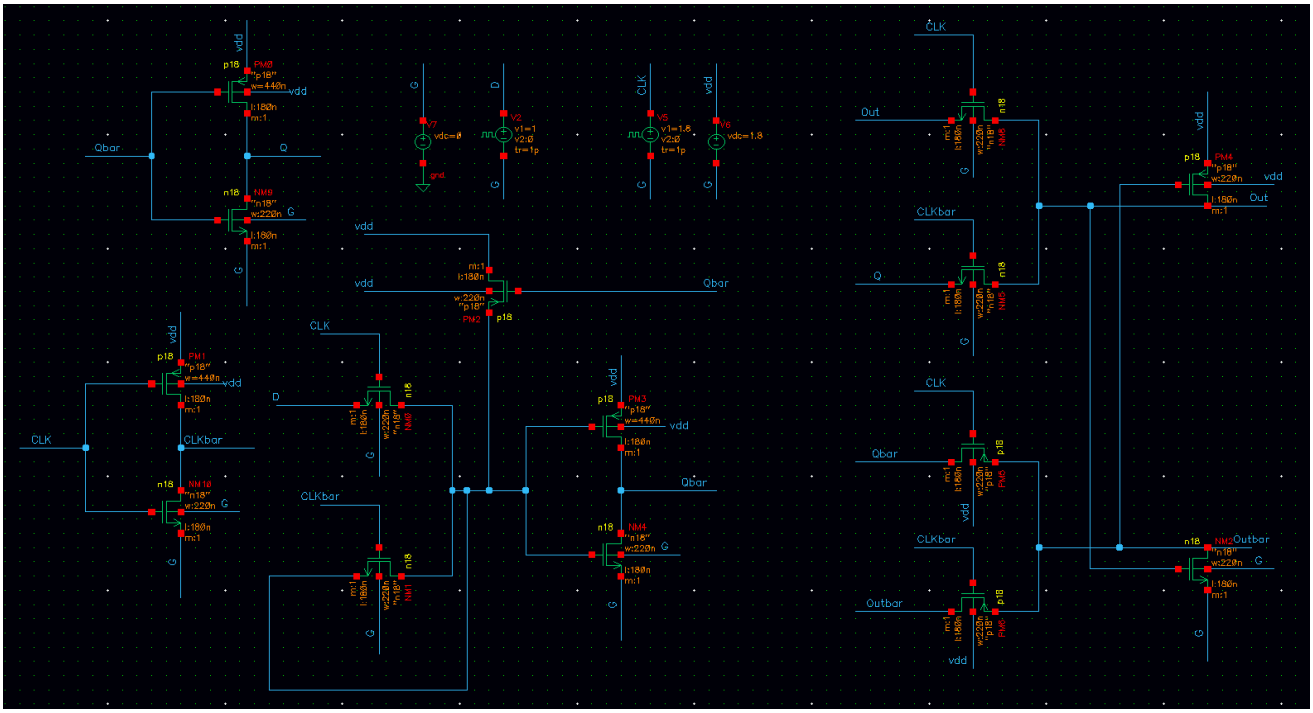


Figure 2.5

The total width of the design is 3960n M or 3.96u M.

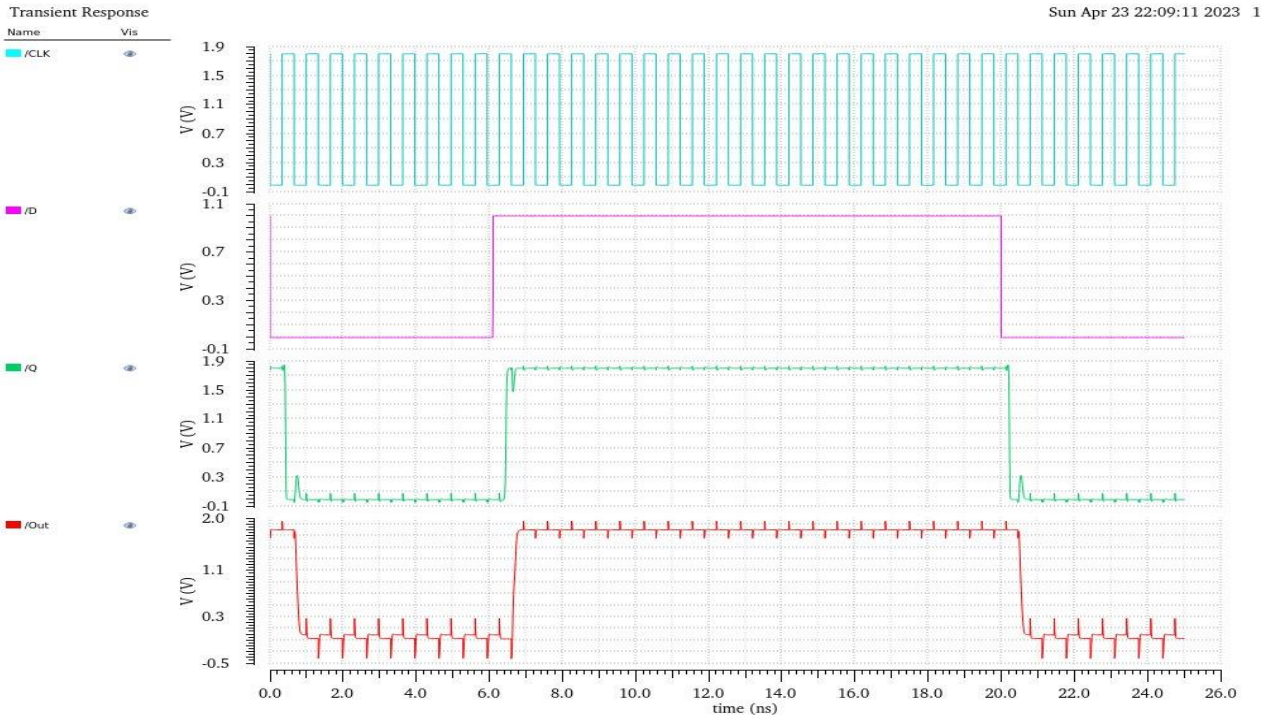


Figure 2.6

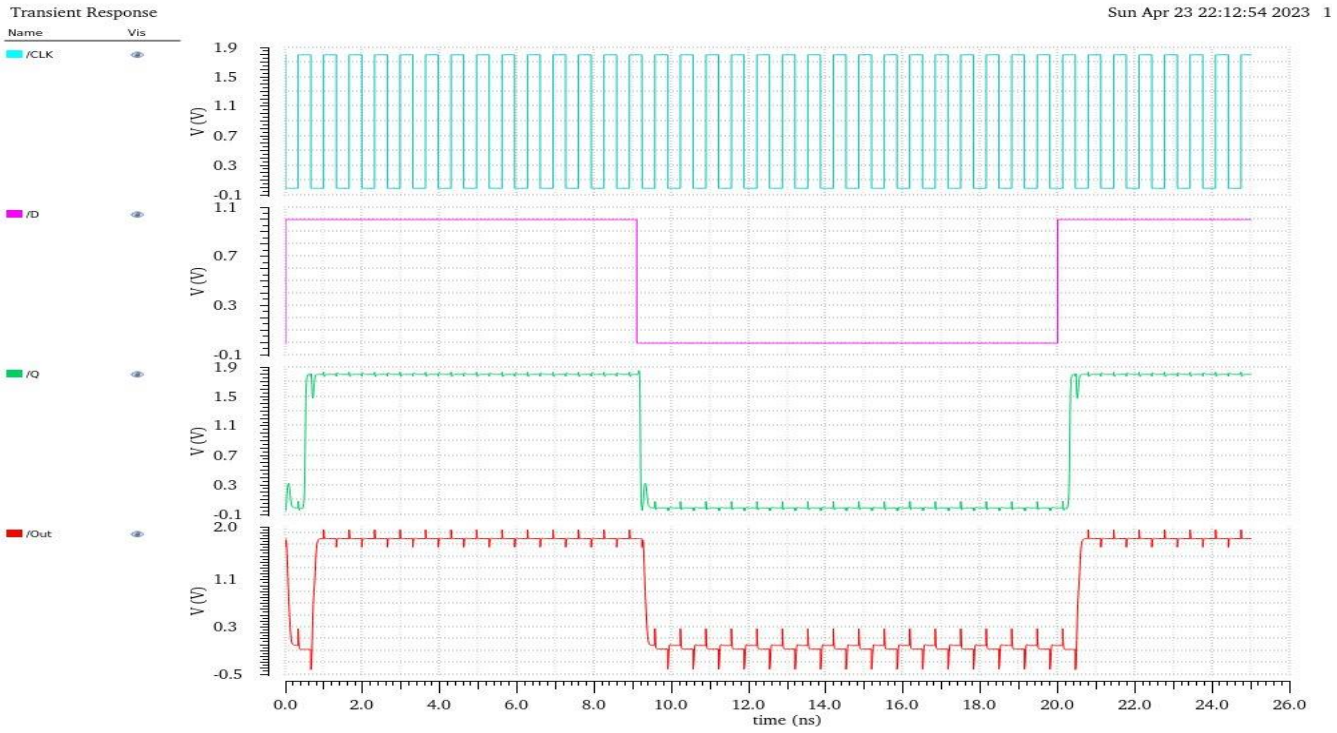


Figure 2.7 (output with different inputs)

In the above case pulse width of the D input is as follows:

- The pulse width of 0 is 11ns.
- The pulse width of 1 is 9ns.

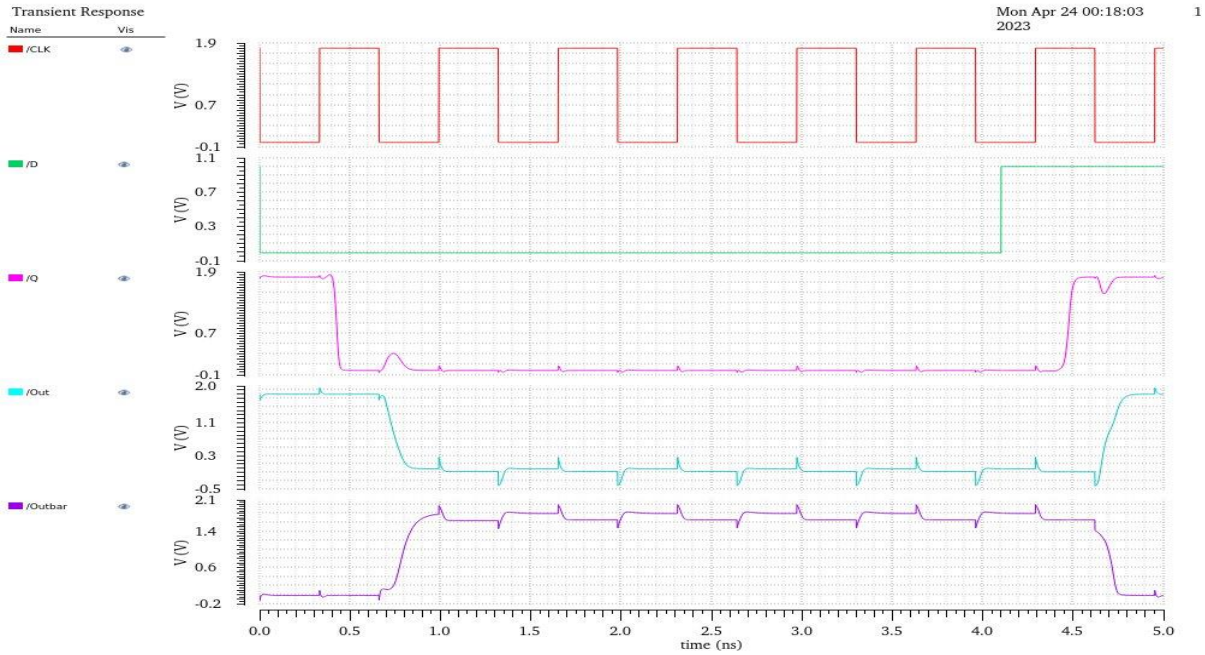


Figure 2.9 (a closer look at the output)

- Q indicates the output of the master flip-flop.
- Qout and Qoutbar indicate the output of the slave flip-flop.

Design 2: LEAP + SRPL

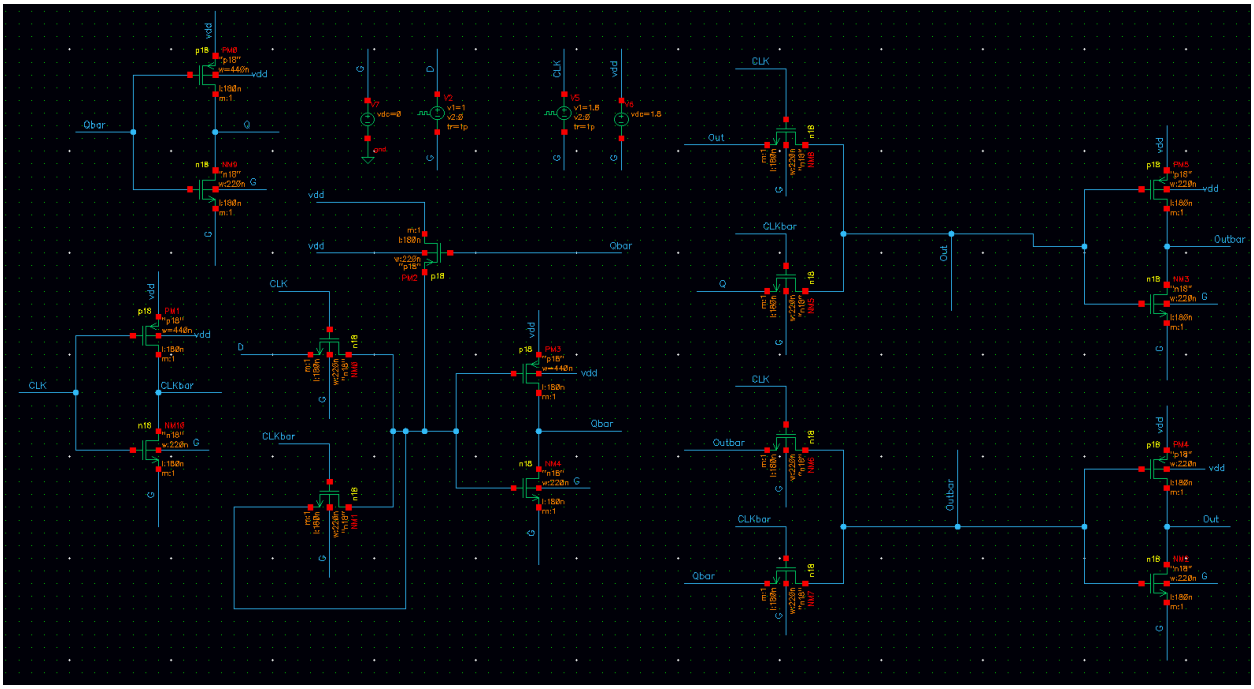


Figure 2.10

Total Width of the design = 4400n M or 4.4u M

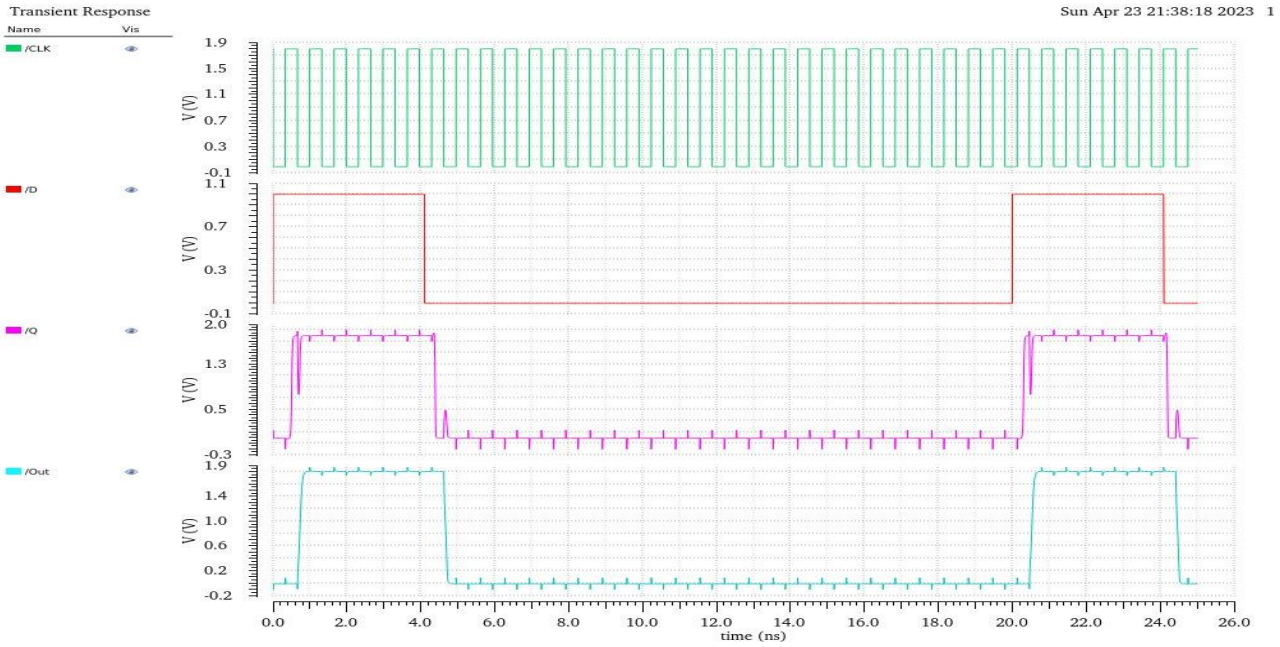


Figure 2.11

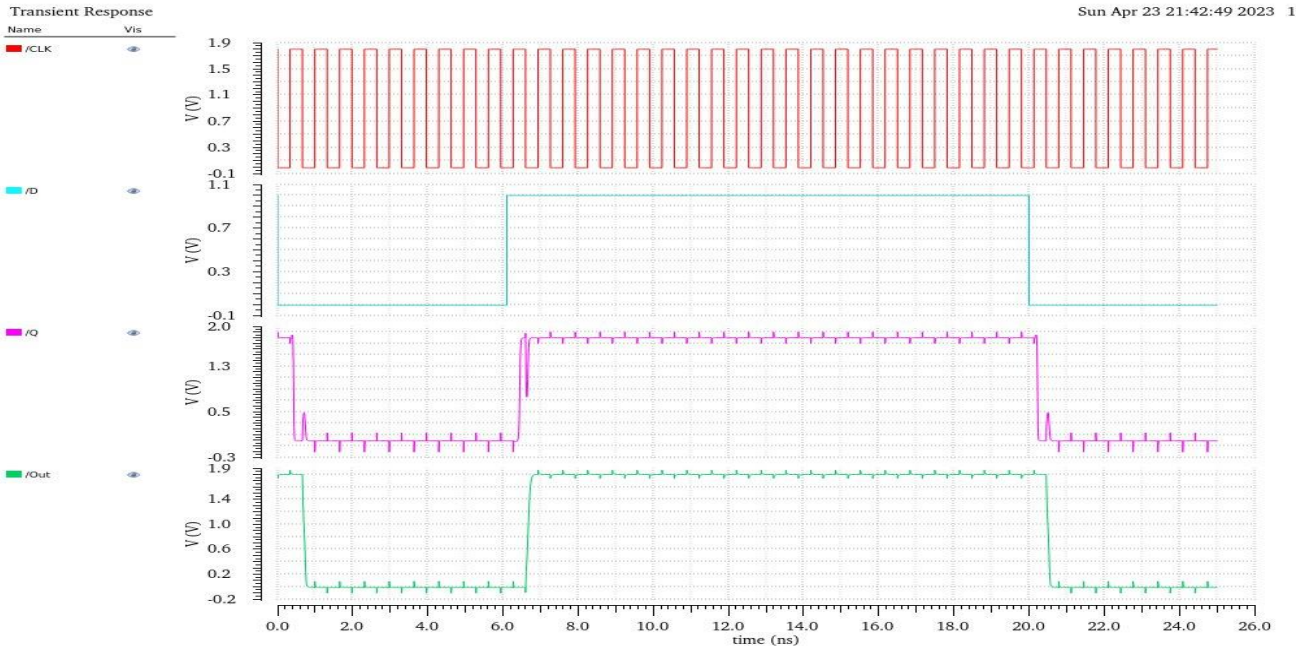


Figure 2.12

In the above case pulse width of the D input is as follows:

- The pulse width of 0 is 6.1ns.
- The pulse width of 1 is 13.9ns.

CLK	D	Q(t) (MASTER)	Qout(t) (SLAVE)
1	0	0	Qout(t-1)
1	1	1	Qout(t-1)
0	X	Q(t-1)	Q(t)

The truth table for master-slave flip flop

From the above designs, we are calculating the width and length of our project.
The length of the designs would be 180nM as we are using 180nM technology.
The total width of LEAP +PPL= 3920n M or 3.29u M.
Total width of LEAP + SRPL= 4400n M or 4.4u M

The total area of LEAP + PPL = 3960 x 180 = 712800 nM^2 or 712.800 uM^2.

The total area of LEAP + SRPL = 4400 x 180 = 792000 nM^2 or 792.000 uM^2.