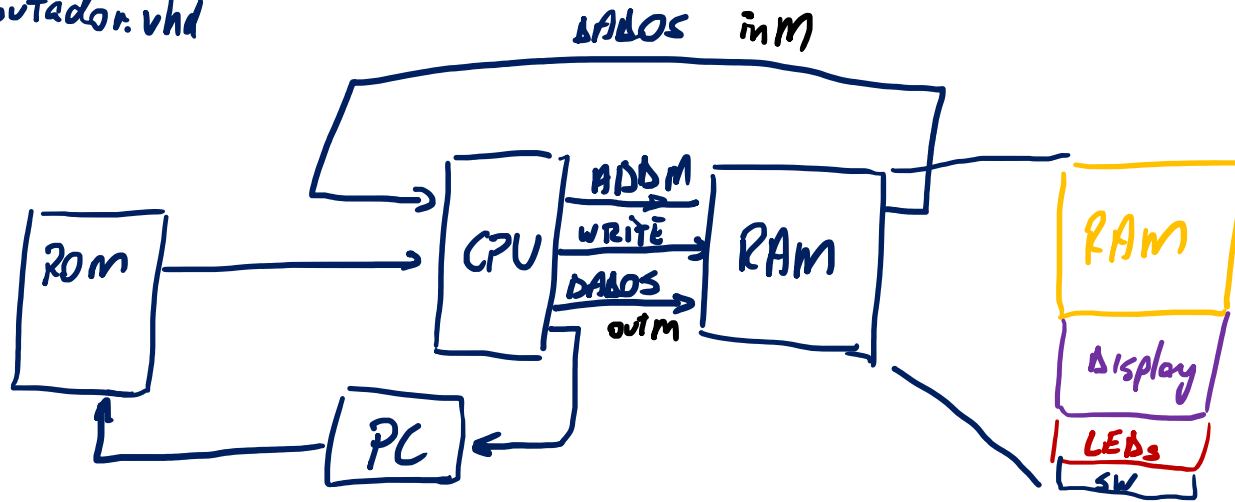
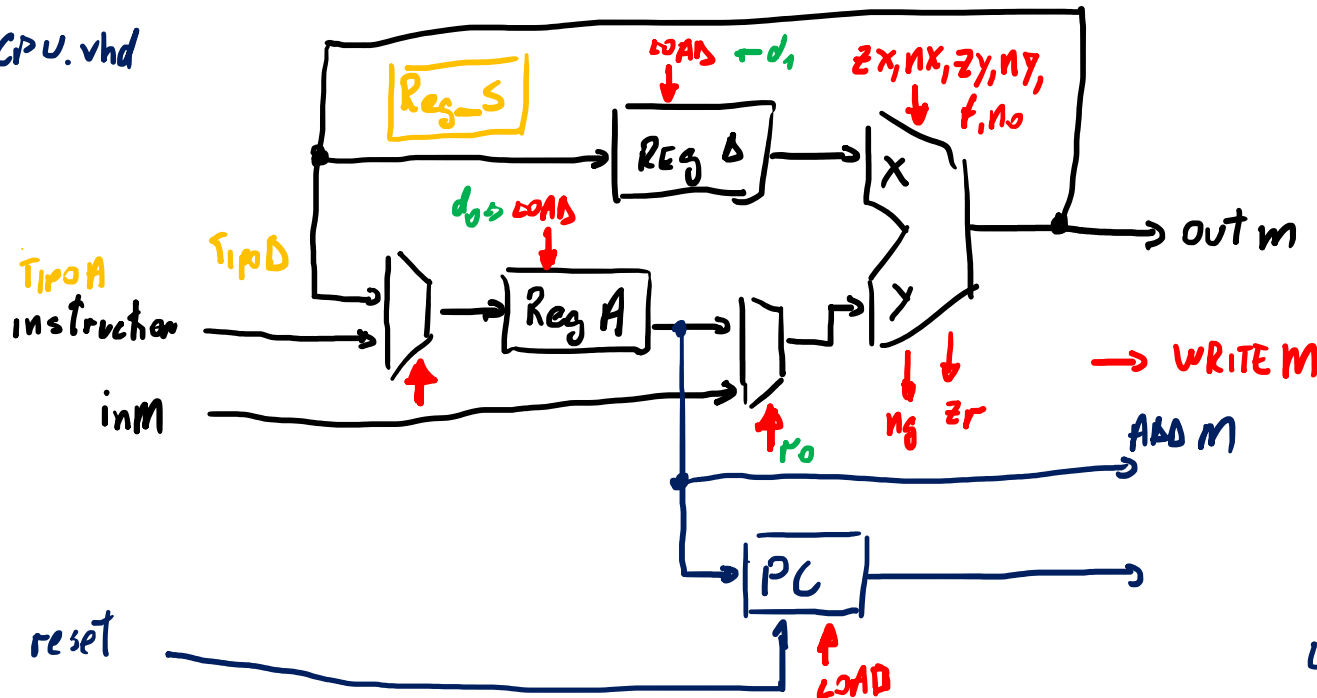


# Computador.vhd



## CPU.vhd



## Control Unit.vhd

Control Unit.vhd

LOAD\_B <= '1' when d<sub>1</sub> = '1' and instruction(17) = '1'

LOAD\_PC <= '1' when

Instruction format bits:

1 000 r<sub>0</sub> C<sub>5</sub> C<sub>4</sub> C<sub>3</sub> C<sub>2</sub> C<sub>1</sub> C<sub>0</sub> d<sub>2</sub> d<sub>1</sub> d<sub>0</sub> j<sub>2</sub> j<sub>1</sub> j<sub>0</sub>

Control signals:

z<sub>x</sub> n<sub>x</sub> z<sub>y</sub> n<sub>y</sub> f n<sub>0</sub>

Control signals:

n<sub>z</sub> j<sub>2</sub> j<sub>1</sub> j<sub>0</sub>

Control signals:

j<sub>0</sub> 0 0 0

Control signals:

j<sub>0</sub> 0 0 1

Control signals:

...

Control signals:

j<sub>mp</sub> 1 1 1

leaw \$3, %0

Tipo A - leaw

0 X

Tipo B

1 000 r<sub>0</sub> C<sub>5</sub> C<sub>4</sub> C<sub>3</sub> C<sub>2</sub> C<sub>1</sub> C<sub>0</sub> d<sub>2</sub> d<sub>1</sub> d<sub>0</sub> j<sub>2</sub> j<sub>1</sub> j<sub>0</sub>