Component Name: pcie_x8_gen3_3_0

Basic | Capabilities | PF0 IDs | PF0 BAR | Legacy/MSI Cap | MSIx Cap | Power Management | Extd. Capabilities-1 | Extd. Capabilities-2 | Shared Logic

Mode: Advanced

Device / Port Type: PCI Express Endpoint device

PCIe Block Location: X0Y1

Reference Clock Frequency (MHz): 100 MHz

Xilinx Development Board: VC709

Silicon Revision: Production

Number of Lanes

Lane Width: X8

Maximum Link Speed

○ 2.5 GT/s ○ 5.0 GT/s ◉ 8.0 GT/s

AXI-ST Interface Width

AXI-ST Interface Width: 256 bit

AXI-ST Interface Frequency (MHz)

AXI-ST Interface Frequency (MHz): 250

AXI-ST Alignment Mode

◉ DWORD Aligned ○ Address Aligned

Tandem Configuration

◉ None ○ Tandem PROM (Refer PG023) ○ Tandem PCIe (Refer PG023)

PIPE Mode Simulations

◉ None ○ Enable Pipe Simulation ○ Enable External PIPE Interface

☐ Enable AXI-ST Frame Straddle

☑ Disable Client Tag

☐ Additional Transceiver Control and Status Ports

☐ Enable External STARTUP primitive

☐ Enable External GT Channel DRP

☐ Enable RX Message INTFC

☐ PCIe DRP Ports

☐ Enable Powerdown Interface