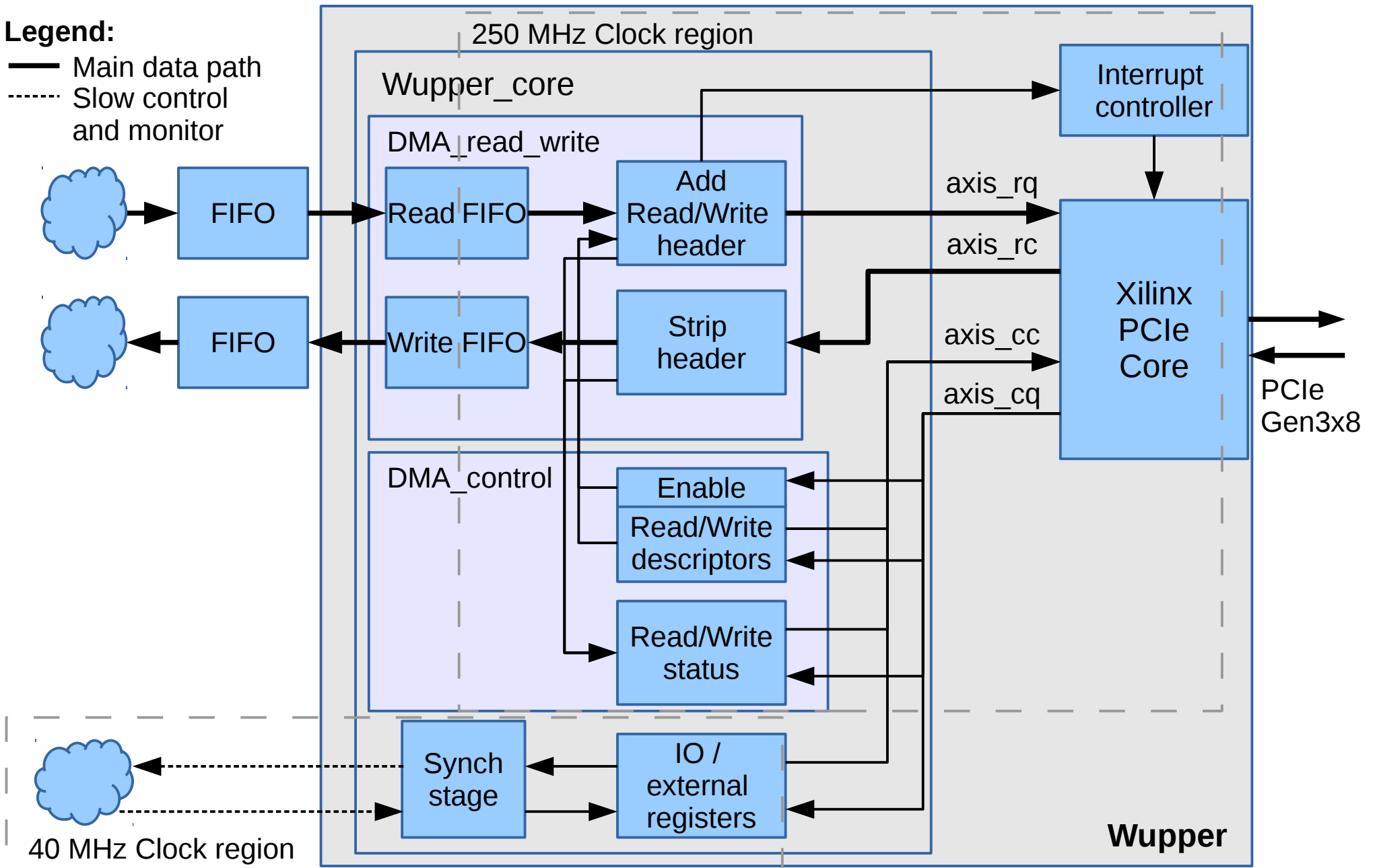# Wupper **functional** block diagram

Legend:
— Main data path
···· Slow control and monitor

250 MHz Clock region

Wupper_core

DMA_read_write

Read FIFO

Write FIFO

Add Read/Write header

Strip header

DMA_control

Enable

Read/Write descriptors

Read/Write status

axis_rq

axis_rc

axis_cc

axis_cq

Interrupt controller

Xilinx PCIe Core

PCIe Gen3x8

FIFO

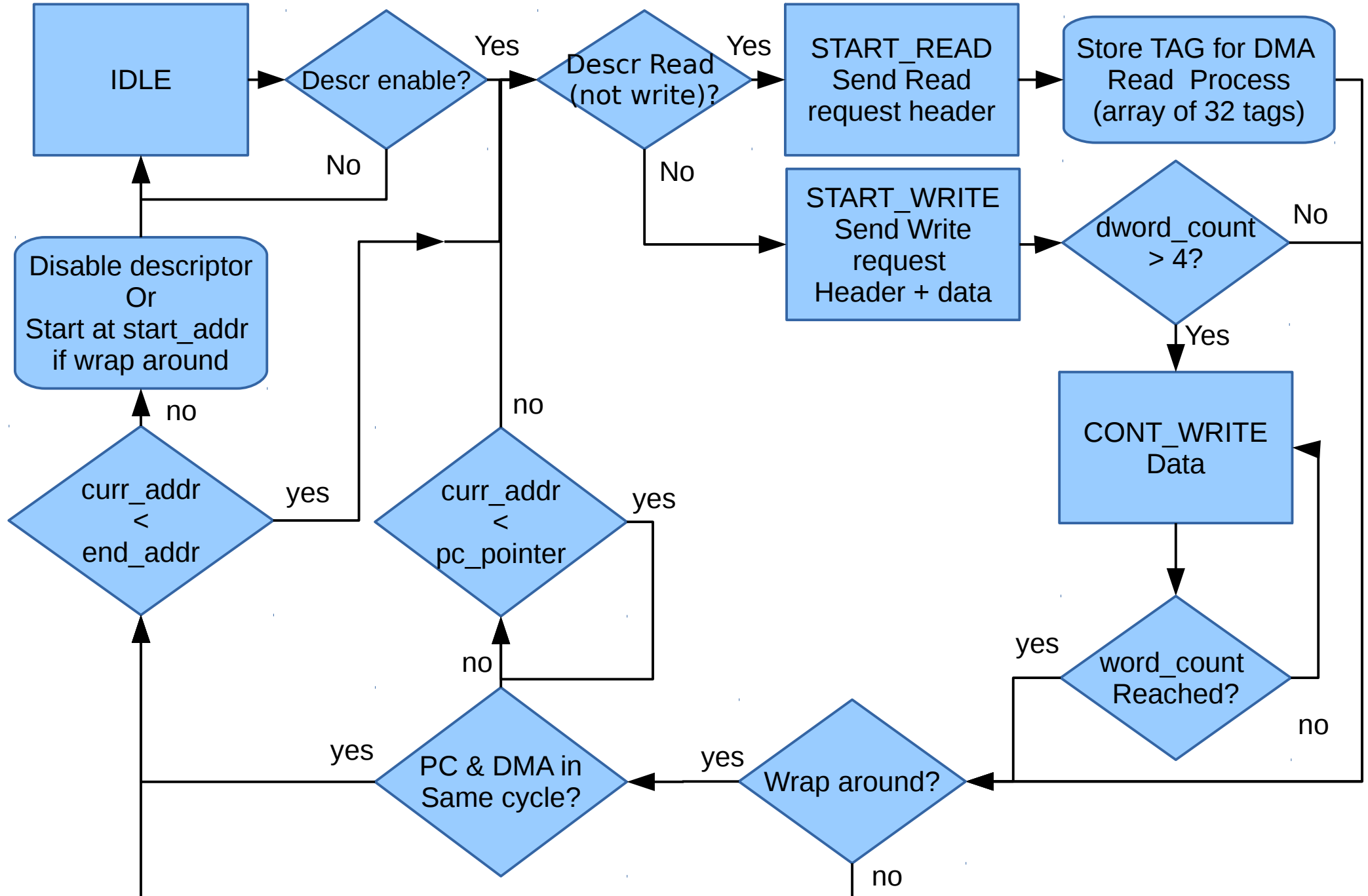FIFO

Synch stage

IO / external registers

40 MHz Clock region

Wupper

Wupper **firmware structure** block diagram
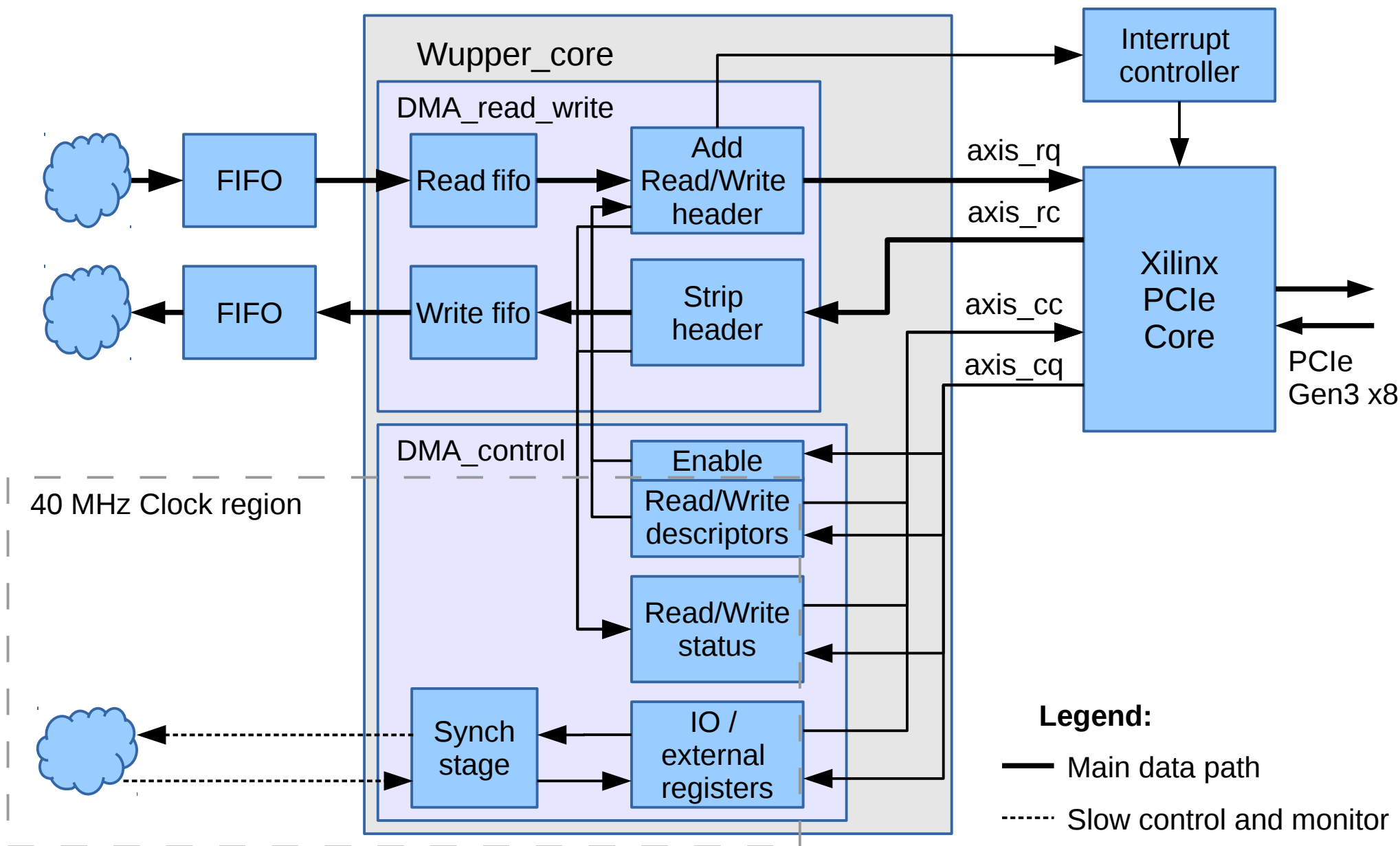
Register / Descriptor read / write
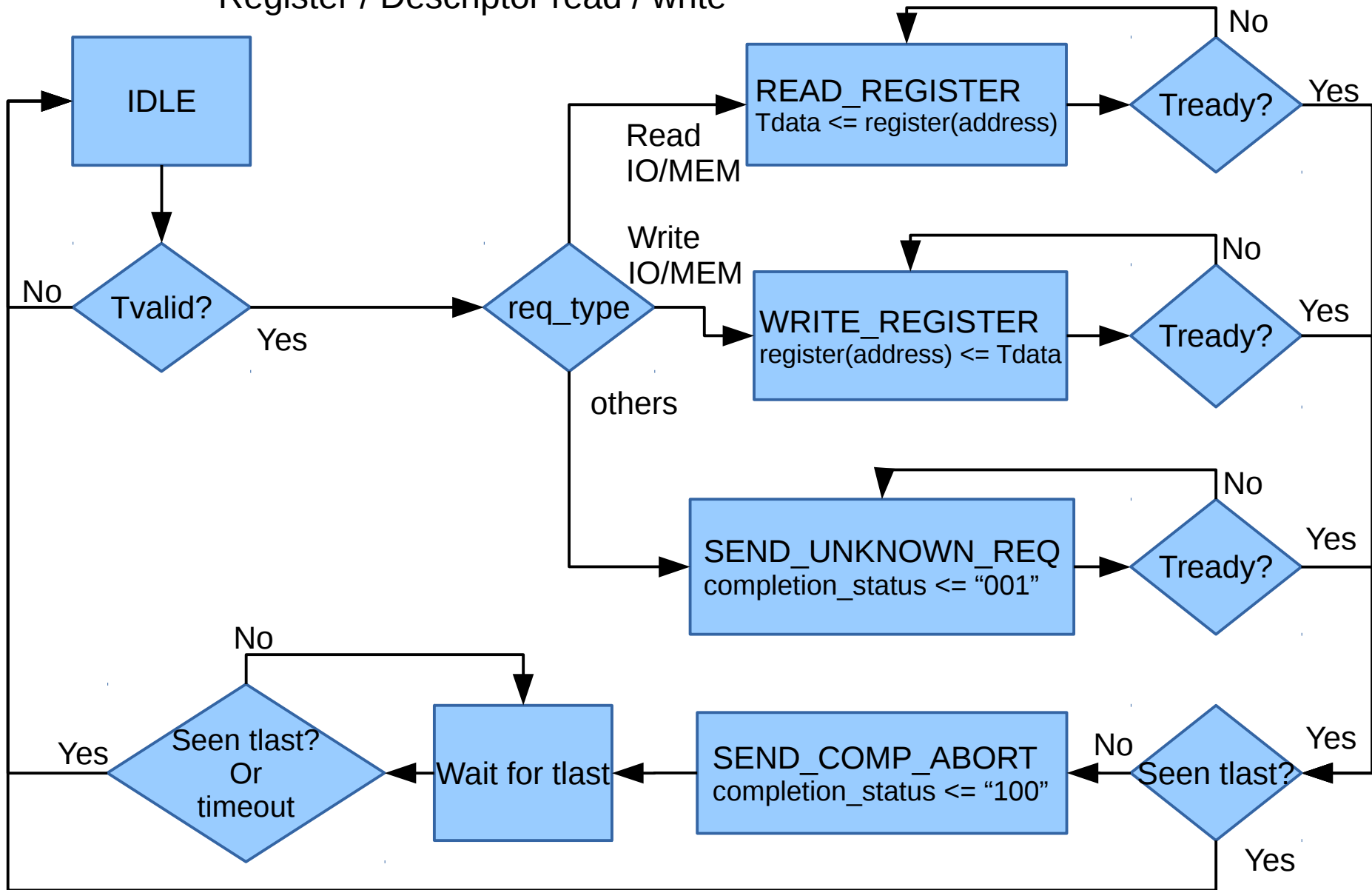
DMA Write (FPGA write, PC read)

```
IDLE → Descr enable?
         Yes → Descr Read (not write)?
         No → (back to IDLE)
```

Descr enable?
- Yes → Descr Read (not write)?
- No → IDLE

Descr Read (not write)?
- Yes → START_READ: Send Read request header
- No → START_WRITE: Send Write request Header + data

START_READ Send Read request header → Store TAG for DMA Read Process (array of 32 tags)

START_WRITE Send Write request Header + data → dword_count > 4?
- No → (to Wrap around?)
- Yes → CONT_WRITE Data

CONT_WRITE Data → word_count Reached?
- yes → Wrap around?
- no → CONT_WRITE Data

Wrap around?
- yes → PC & DMA in Same cycle?
- no → curr_addr < end_addr

PC & DMA in Same cycle?
- yes → curr_addr < end_addr
- no → curr_addr < pc_pointer

curr_addr < pc_pointer
- yes → (loop back)
- no → Descr enable? (yes path)

curr_addr < end_addr
- yes → (to Descr enable yes path)
- no → Disable descriptor Or Start at start_addr if wrap around

Disable descriptor Or Start at start_addr if wrap around → IDLE

DMA Read (FPGA read, PC write)

```
┌─────────────┐
│    IDLE     │
└─────────────┘
       │
       ▼
   Tvalid and  ──No──
   Contains
   data?a
       │Yes
       ▼
   Tag matches  ──Yes──►  PUSH_DATA      ──►  Tlast or      ──Yes──
   Request?              Push data            word_count
       │No               into FIFO            Reached?
                                                  │No
```

IDLE

Tvalid and Contains data?a —No—

Tag matches Request? —Yes— —No

PUSH_DATA Push data into FIFO

Tlast or word_count Reached? —Yes— —No

DMA Cache   **obsolete**

TRANSFER:
 axis_rq <= axis_rq
 backup(i) <= axis_rq
 I++

Tready = 1?

Yes

No

Restore

complete?

Yes

No

START_RESTORE:
 axis_rq <= axis_rq
 backup(i) <= axis_rq
 I++

Tlast = 1?

Yes

No

RESTORE:
 axis_rq <= backup(i)
 i++