Component Name: vc709_pcie_x8_gen3

Basic | **Capabilities** | PF0 IDs | PF0 BAR | Legacy/MSI Cap

Physical Functions

☑ Enable Physical Function 0

☐ Enable Physical Function 1

Device Capabilities Register PF

PF0 Max Payload Size: 1024 bytes

PF1 Max Payload Size: 512 bytes

☐ Extended Tag Field

Link Status Register

Selects whether the device reference clock is provided by the connector (Synchronous) or generated via an onboard PLL(Asynchronous)

☐ Enable Slot Clock Configuration