Component Name: vc709_pcie_x8_gen3

Basic | Capabilities | PF0 IDs | PF0 BAR | Legacy/MSI Cap

Mode: Basic

Device / Port Type: PCI Express Endpoint device

PCIe Block Location: X0Y1

Number of Lanes

Lane Width: X8

Maximum Link Speed

○ 2.5 GT/s ○ 5.0 GT/s ◉ 8.0 GT/s

AXI-ST Interface Width

AXI-ST Interface Width: 256 bit

AXI-ST Interface Frequency (MHz)

AXI-ST Interface Frequency (MHz): 250

AXI-ST Alignment Mode

◉ DWORD Aligned ○ Address Aligned

☐ Enable AXI-ST Frame Straddle

☐ Disable Client Tag

Reference Clock Frequency (MHz): 100 MHz

Xilinx Development Board: VC709

Silicon Revision: Production

Tandem Configuration

◉ None

○ Tandem PROM (Refer PG023)

○ Tandem PCIe (Refer PG023)

☐ Enable Pipe Simulation

☐ Enable External PIPE Interface

☐ Additional Transceiver Control and Status Ports

☐ Enable External STARTUP primitive

☐ Enable External GT Channel DRP