* BUFFER WRITE COMPLITON (or TURN-AROUND) INTERRUPTING

* MAIN DMA INPUT BUFFER NOT-EMPTY (⌐) INTERRUPT

* CONTROL DELAY BETWEEN Ⓐ and Ⓑ !

CIRCULAR BUFFER

① WRAP-AROUND : SET

② EN_DESCRIPTOR : SET   ALWAYS SET TURN-AR.

|||| 0101

Ⓞ EVEN_CYCLE_PC 0101

Ⓞ EVEN_CYCLE_DMA

↳ "4 bit counters"

PC READ : DMA BUFFER READ

Ⓑ

Ⓒ

WRITE

READ

START   END

CURRENT_ADDRESS : DMA BUFFER WRITE

Ⓐ
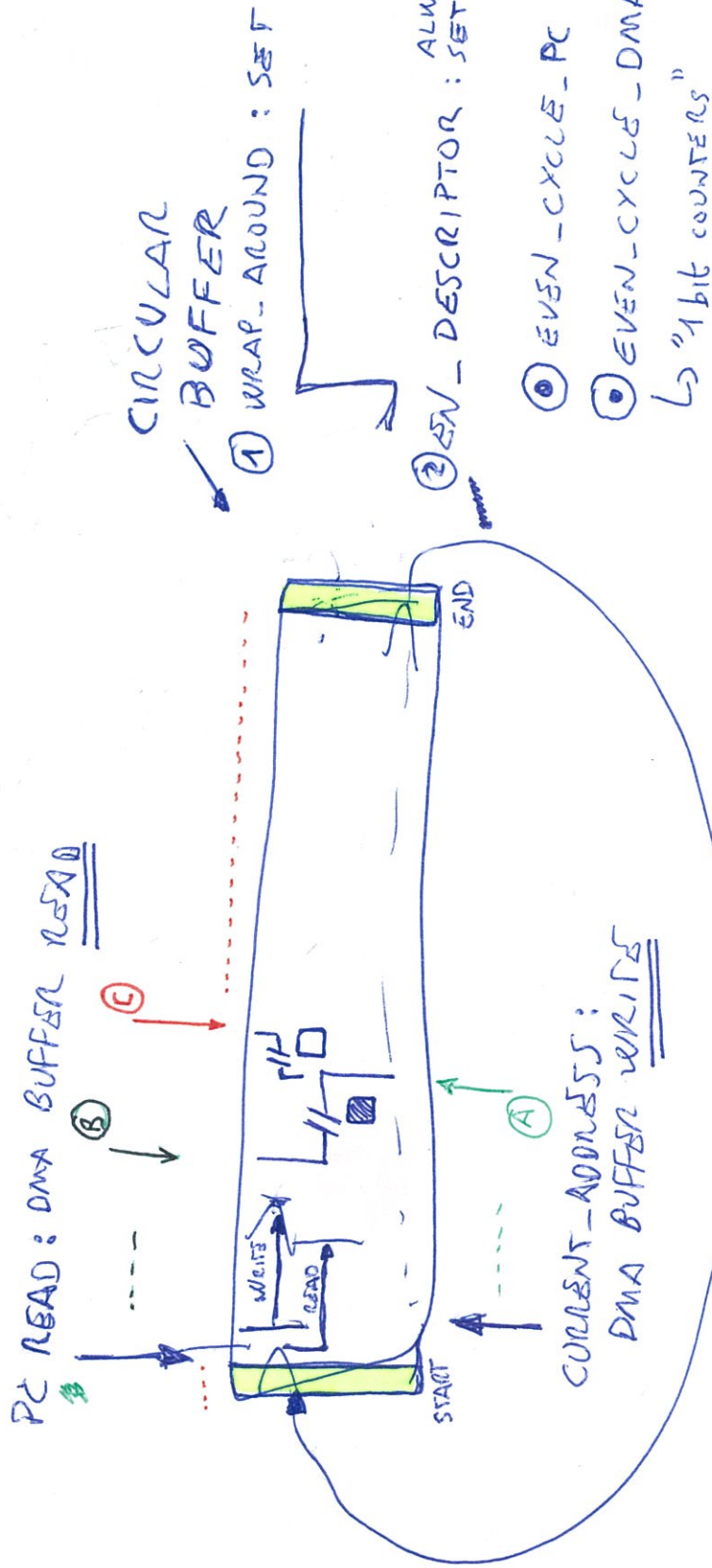
Ⓐ ALWAYS AHEAD OF Ⓑ : ▨

Ⓐ SHOULDN'T PASS Ⓑ , WORST CASE IT SHOULD BE A "BIT" : □

LAGGING BEHIND Ⓒ :