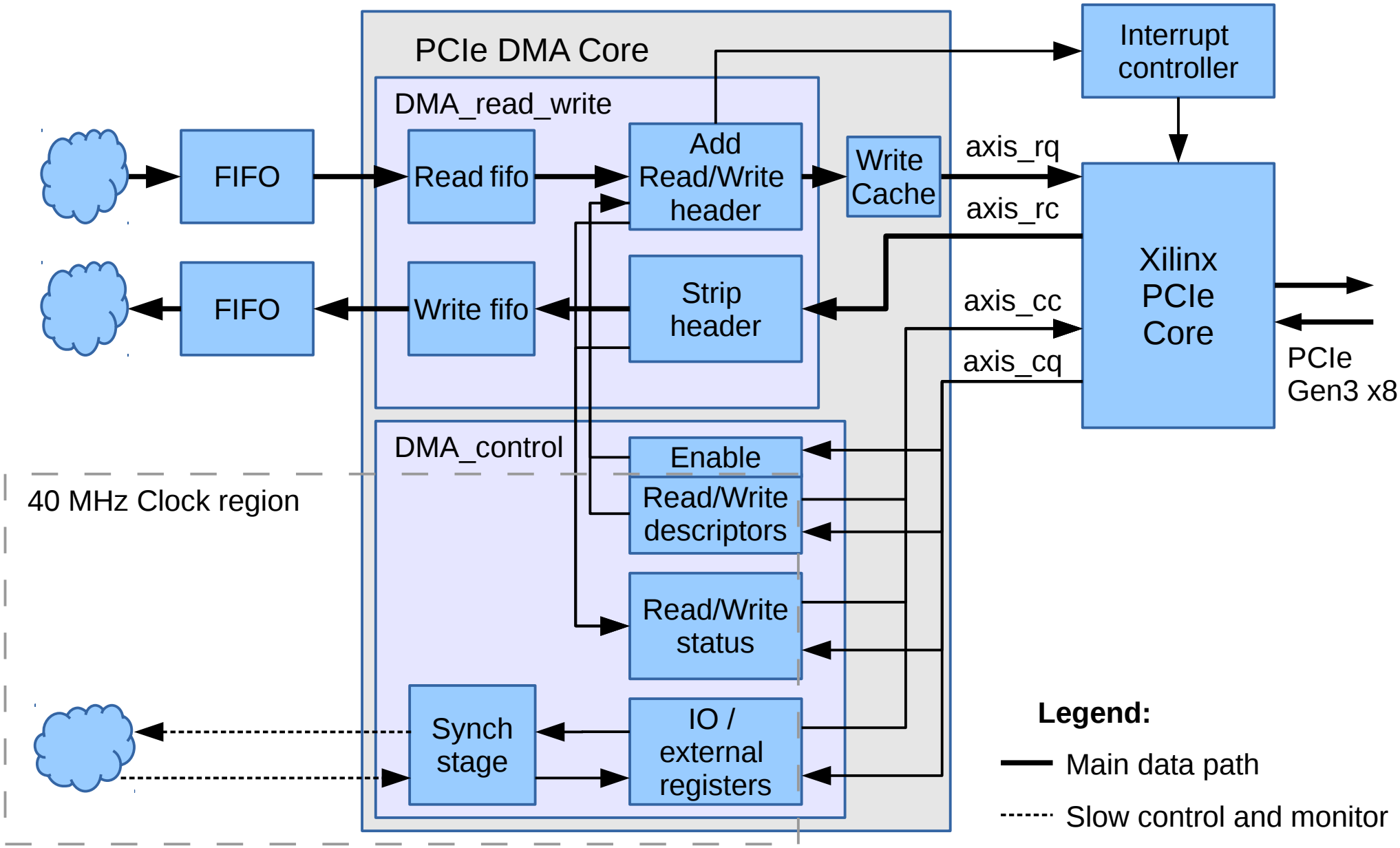
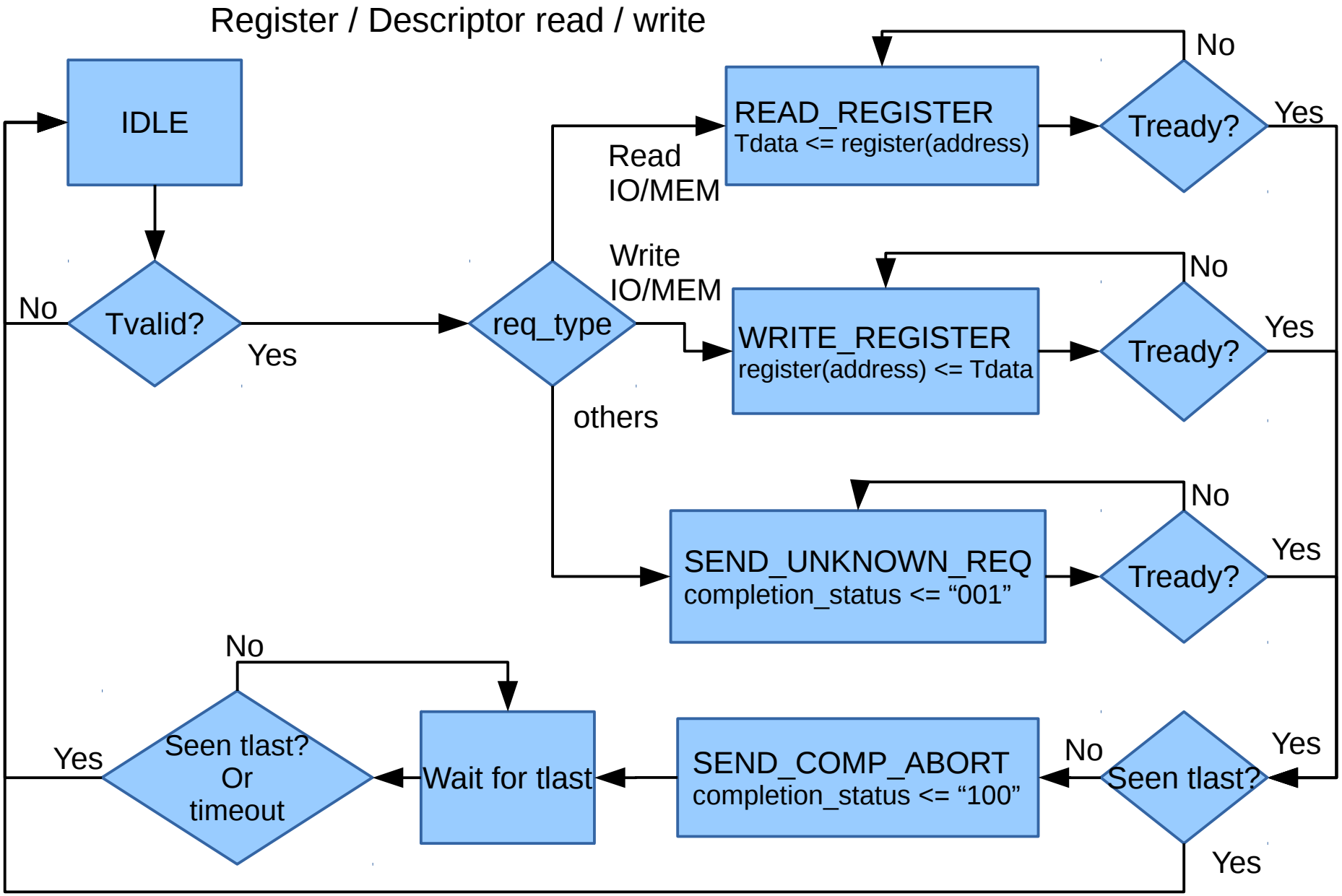
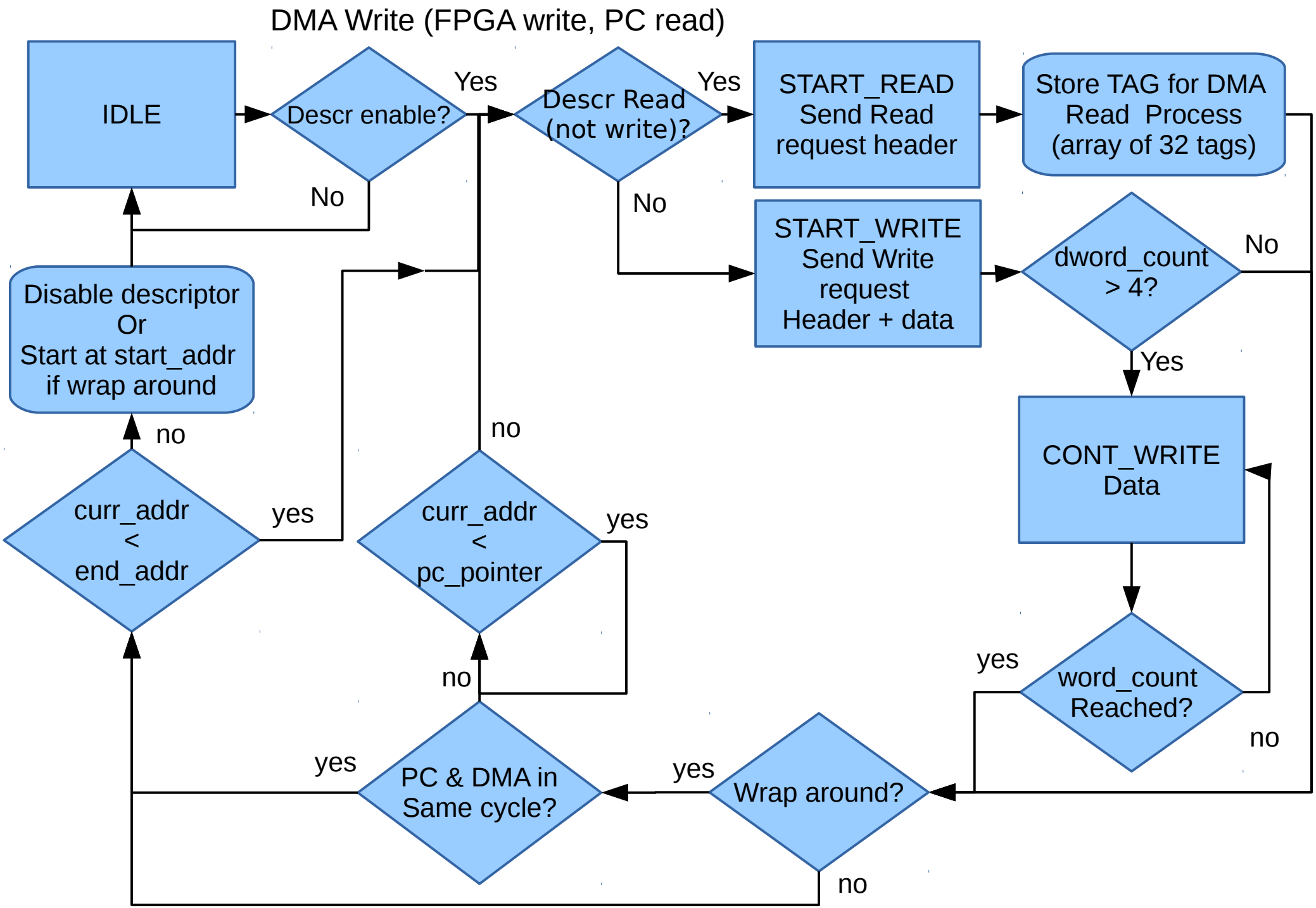
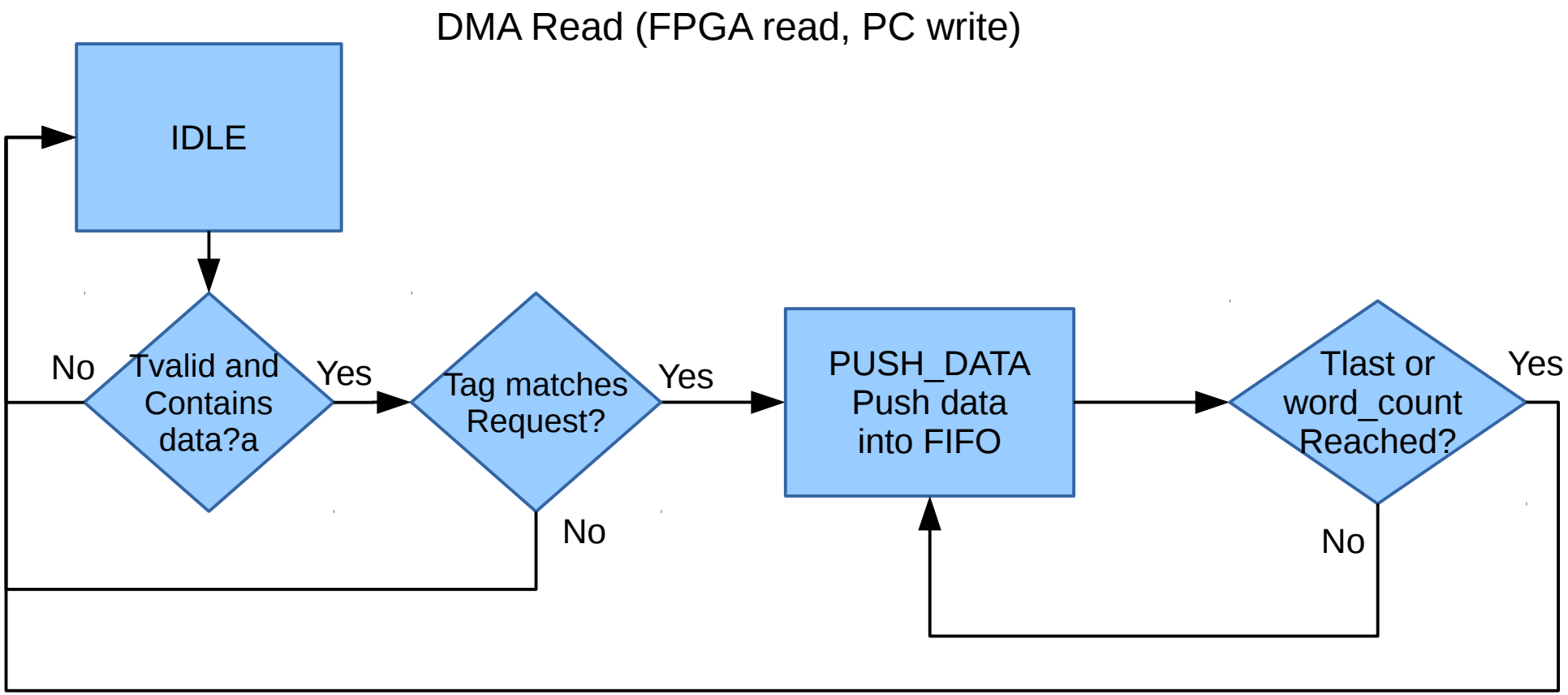
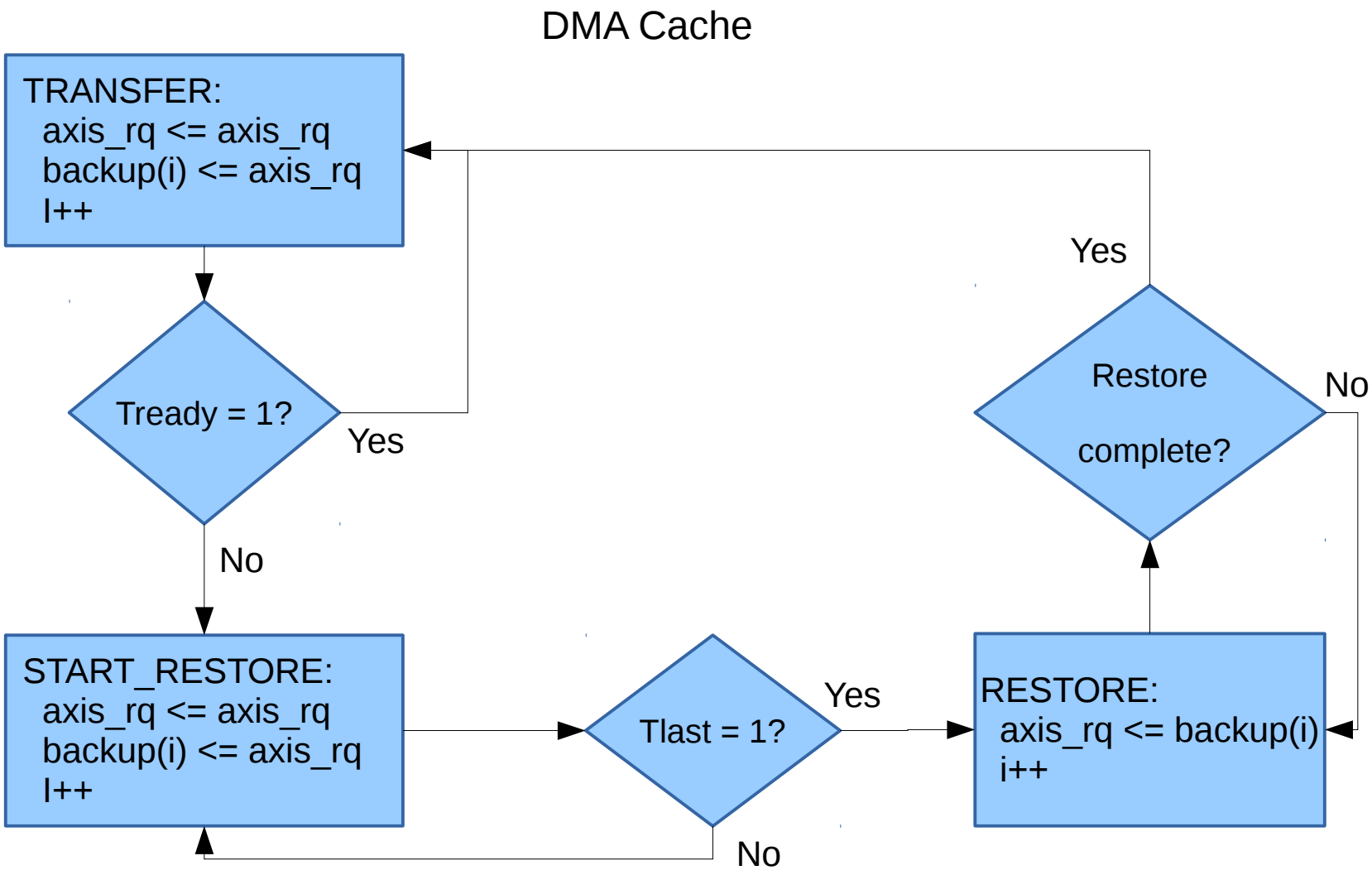

PCIe DMA Core
DMA_read_write
DMA_control
FIFO
FIFO
Read fifo
Write fifo
Add Read/Write header
Strip header
Write Cache
Enable
Read/Write descriptors
Read/Write status
IO / external registers
Synch stage
Interrupt controller
axis_rq
axis_rc
axis_cc
axis_cq
Xilinx PCIe Core
PCIe Gen3 x8
40 MHz Clock region
Legend:
Main data path
Slow control and monitor


Register / Descriptor read / write
IDLE
Tvalid?
No
Yes
req_type
Read
IO/MEM
READ_REGISTER
Tdata <= register(address)
Tready?
No
Yes
Write
IO/MEM
WRITE_REGISTER
register(address) <= Tdata
Tready?
No
Yes
others
SEND_UNKNOWN_REQ
completion_status <= “001”
Tready?
No
Yes
SEND_COMP_ABORT
completion_status <= “100”
Seen tlast?
No
Yes
Wait for tlast
Seen tlast?
Or
timeout
No
Yes
Yes


DMA Write (FPGA write, PC read)
IDLE
Descr enable?
Yes
No
Descr Read (not write)?
Yes
No
START_READ Send Read request header
Store TAG for DMA Read Process (array of 32 tags)
START_WRITE Send Write request Header + data
dword_count > 4?
No
Yes
CONT_WRITE Data
word_count Reached?
yes
no
Wrap around?
yes
no
PC & DMA in Same cycle?
yes
no
curr_addr < pc_pointer
yes
no
curr_addr < end_addr
yes
no
Disable descriptor Or Start at start_addr if wrap around


DMA Read (FPGA read, PC write)
IDLE
No
Tvalid and Contains data?a
Yes
Tag matches Request?
Yes
No
PUSH_DATA Push data into FIFO
Tlast or word_count Reached?
Yes
No


DMA Cache
TRANSFER:
axis_rq <= axis_rq
backup(i) <= axis_rq
I++
Tready = 1?
Yes
No
START_RESTORE:
axis_rq <= axis_rq
backup(i) <= axis_rq
I++
Tlast = 1?
Yes
No
RESTORE:
axis_rq <= backup(i)
i++
Restore
complete?
Yes
No