Wupper **functional** block diagram

Legend:
— Main data path
····· Slow control and monitor

250 MHz Clock region

Wupper_core

DMA_read_write

- ToHost FIFO ctl
- FromHost FIFO ctl
- Add Read/Write header
- Strip header

DMA_control

- Enable
- Read/Write descriptors
- Read/Write status

- ToHost FIFO
- FromHost FIFO

- Interrupt controller

- Xilinx PCIe Core

axis_rq
axis_rc
axis_cc
axis_cq

PCIe Gen3x8

- Synch stage
- IO / external registers

40 MHz Clock region

Wupper

Wupper **firmware structure** block diagram

Register / Descriptor read / write

IDLE

Tvalid?

No

Yes

req_type

Read IO/MEM

Write IO/MEM

others

READ_REGISTER
Tdata <= register(address)

Tready?

No

Yes

WRITE_REGISTER
register(address) <= Tdata

Tready?

No

Yes

SEND_UNKNOWN_REQ
completion_status <= "001"

Tready?

No

Yes

Seen tlast?

No

Yes

SEND_COMP_ABORT
completion_status <= "100"

Wait for tlast

No

Seen tlast?
Or
timeout

Yes

DMA toHost path

```
IDLE → Descr enable? 
  Descr enable? --No--> Disable descriptor Or Start at start_addr if wrap around
  Descr enable? --Yes--> Descr Read (not write)?
    Descr Read (not write)? --Yes--> START_READ Send Read request header
    Descr Read (not write)? --No--> START_WRITE Send Write request Header + data
  START_READ Send Read request header → Store TAG for DMA Read Process (array of 32 tags)
  START_WRITE Send Write request Header + data → dword_count > 4?
    dword_count > 4? --No--> (back)
    dword_count > 4? --Yes--> CONT_WRITE Data
  CONT_WRITE Data → word_count Reached?
    word_count Reached? --no--> CONT_WRITE Data
    word_count Reached? --yes--> Wrap around?
  Wrap around? --yes--> PC & DMA in Same cycle?
  Wrap around? --no--> (back)
  PC & DMA in Same cycle? --yes--> curr_addr < end_addr
  PC & DMA in Same cycle? --no--> curr_addr < pc_pointer
    curr_addr < pc_pointer? --yes--> (back)
    curr_addr < pc_pointer? --no--> (Descr enable junction)
  curr_addr < end_addr? --no--> Disable descriptor
  curr_addr < end_addr? --yes--> (Descr enable junction)
```

IDLE

Descr enable?

Descr Read (not write)?

START_READ Send Read request header

Store TAG for DMA Read Process (array of 32 tags)

START_WRITE Send Write request Header + data

dword_count > 4?

CONT_WRITE Data

word_count Reached?

Wrap around?

PC & DMA in Same cycle?

curr_addr < pc_pointer

curr_addr < end_addr

Disable descriptor Or Start at start_addr if wrap around

DMA fromHost path

```
        ┌──────────┐
        │          │
        │   IDLE   │
        │          │
        └────┬─────┘
             │
             ▼
           ◇ Tvalid and              ┌──────────────┐         ◇ Tlast or
   No     ◇ Contains    Yes          │  PUSH_DATA   │         ◇ word_count    Yes
◇─────────◇ data?a   ─────────────▶  │  Push data   │ ──────▶ ◇ Reached?   ─────────
          ◇                          │  into FIFO   │         ◇
                                     └──────────────┘         ◇
                                                                  No
```