

# Prem Mallappa

Software Architect • System & Embedded Software

Bengaluru, India

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Seasoned Software Architect with extensive expertise in designing and developing high-performance embedded systems, system software, Linux kernel drivers, and virtualization technologies. Proficient in a wide range of programming and scripting languages, with a proven track record of delivering robust, scalable solutions in complex technical environments.

A highly analytical and collaborative team player, recognized for strong problem-solving abilities, logical thinking, and a passion for mastering emerging technologies. Committed to driving innovation and excellence through clean architecture, optimized code, and best-in-class engineering practices.

## Experience

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### AMD Ltd.

Principal Engineer

Bengaluru, India

Feb. 2018 -- Present

- AMD Math Library: Optimizing exponential/power/logarithmic/trigonometric functions for latest AMD processors
- Improved performance of exp() and log() by 30% using look-up-table, Estrin's method polynomial, and fast integer conversion
- AMD Cryptographic Primitives Library: Optimizing AES/SHA/PKCS functions with AVX2 and AESNI/SHANI instruction sets
- Developed dynamic dispatcher using cpuid instruction for runtime algorithm selection
- Achieved 3x performance improvement in CFB-based parallel decrypting

### Broadcom Ltd.

Principal Engineer

Bengaluru, India

Jan. 2014 -- Oct. 2016

- Designed and developed initial software support for Broadcom Vulcan, a multicore-multithreaded ARMv8 64-bit processor
- Handled SMMUv3 (IOMMU) related issues and software stack implementation
- Developed SMMUv3 emulation model for QEMU which was merged into mainline codebase
- Implemented Command queue, STE/CD parsing, pagetable walk, and Stage1/Stage2 virtualization support

### Cavium India Pvt. Ltd.

Tech Lead

Bengaluru, India

May. 2011 -- Dec. 2013

- Worked on Cavium's Octeon III (MIPS64) series of processors

• Fixed major bug in KEXEC and developed MIPS port of Kexec and Kdump (patches merged upstream)

• Developed baremetal core-file generating software with host-based daemon for GDB debugging

• Designed and developed CavHv hypervisor for MIPS64 with experimental hardware virtualization

### ARM Ltd.

Sr. Development Engineer

Bengaluru, India

Aug. 2005 -- Jun. 2009

- Responsible for OS porting to latest ARM cores including ARM1176JZFS, TrustZone and Cortex-A8

• Developed touch-screen driver for Symbian OS and automated testing using Python scripts

• Designed interrupt latency measurement driver for TrustZone secure world overhead analysis

• Ported L4Ka::pistachio microkernel to ARM for virtualization experiments

## Sasken Communications Pvt Ltd.

Sr. Software Engineer

Bengaluru, India

Aug. 2004 -- Aug. 2005

- Module owner for EFS (Extended File System) developed for VxWorks, used in UMTS/BTS
- Developed reset-proof filesystem with wear-leveling and minimal data-loss features
- Implemented flat file tree structure optimized for Flash devices with limited read/write cycles

## Global Edge Software Ltd.

Software Engineer

Bengaluru, India

Jun. 2003 -- Aug. 2004

- Designed and developed SDIO driver for Linux on Intel StrongARM boards
- Developed fast SDIO driver supporting 4-bit mode for Marvell 802.11g WiFi chipset
- Achieved maximum throughput for WiFi communication via SDIO interface

## Short Stints

### VSPL Ltd.

Software Architect

Bengaluru, India

Nov. 2016 -- Jan. 2018

### Cisco Ltd.

Software Engineer

Bengaluru, India

Oct. 2010 -- Apr. 2011

### B-Labs, London UK

Sr. Engineer - Contractor

Bengaluru, India

Nov. 2009 -- Sep. 2010

### Harman International

Engineer

Bengaluru, India

Jul. 2009 -- Nov. 2009

## Open Source Contributions

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### QEMU

2014-2016

- SMMUv3 (IOMMU) emulation support for ARMv8

- Designed and implemented SMMUv3 model merged into mainline
- Added support for Stage1, Stage2, and nested virtualization
- Implemented command queue processing and page table walk

### Linux Kernel

2011-2016

- MIPS Kexec/Kdump port and IOMMU subsystem
- Developed MIPS64 port of Kexec and Kdump (merged upstream)
- Fixed critical bugs in KEXEC for Cavium Octeon platforms
- Contributed to IOMMU/SMMUv3 driver development

### GLIBC

2018-2020

- Performance optimizations for AMD processors
- Fixed memcpy behaviour on AMD processors
- Optimized string functions for x86\_64 architecture
- Performance improvements for memory operations

## AMD LibM

2018-Present

- Open source math library for AMD processors
- Core contributor to open sourcing AMD Math Library
- Optimized transcendental functions (exp, log, pow, trig)
- Implemented SIMD/FMA optimizations for vector operations

## Skills

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**Programming Languages** C, Assembly (x86, ARM, MIPS), Rust, Python, C++, Go, Shell, Haskell

**Libraries & Frameworks** GoogleTest, GoogleBench, Hugo, Qt

**Operating Systems** Linux, FreeBSD, QNX, VxWorks, Symbian

**Architecture & Platforms** x86/x86\_64, ARM (ARMv6, ARMv7, ARMv8), MIPS64, PowerPC

**Virtualization & Hypervisors** QEMU, KVM, Xen, Custom Hypervisors, TrustZone

**Development Tools** Git, Make, CMake, ARM Development Tools, Keil, Macraigor, RealView Trace/JTAG, Docker, Wordpress

**Specialized Skills** Linux Kernel Development, Device Drivers, IOMMU/SMMUv3, Embedded Systems, System Software, Performance Optimization, SIMD/FMA Instructions, Cryptography (AES, SHA), Filesystem Development

## Education

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### M.Tech (Computer Science)

*BITS Pilani*

Pilani, Rajasthan, India

2016

### B.E (Computer Science)

*Visvesvaraya Technological University (VTU)*

AIT, Karnataka, India

2002

## Awards

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Q3 2018	<b>Spotlight</b> , Helping Emulation team find design bug in data fabric	<i>AMD</i>
Q2 2019	<b>Spotlight</b> , Optimization of exp() and improving performance by 30%	<i>AMD</i>
Q2 2019	<b>Director Spotlight</b> , Supporting Arden Ubuntu emulation boot, fixing initramfs delayed mount	<i>AMD</i>
Q4 2020	<b>Spotlight</b> , Providing important patches to GLIBC to fix memcpy behaviour on AMD, open sourcing AMD LibM	<i>AMD</i>
Q3 2021	<b>Spotlight</b> , Delivering Cryptography PoC (CFB based parallel decrypting), increases performance by 3x	<i>AMD</i>

## Publications

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### Example Publication Title

2024

- *Authors:* Author Name, Co-Author Name
- *Venue:* Conference/Journal Name
- Brief description of the publication

# Projects

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## AMD Ltd.

PRINCIPAL ENGINEER

2018 – Present

Bengaluru, India

### AMD Pensando SmartNIC

Jun. 2025 – Present

**Summary:** Initiated as a proof-of-concept for an ISV experiencing performance issues with AES-CFB on AMD-Milan servers. Evolved into a comprehensive cryptographic primitives library.

**Contributions:**

- Designed and developed parallel AES-CFB decryption algorithm achieving 3x performance improvement
- Implemented cryptographic primitives library utilizing both AVX2 and AESNI/SHANI instruction sets
- Developed dynamic dispatcher for runtime selection of most efficient algorithm
- Created OpenSSL provider to enable seamless interoperability

**Languages:** C, ASM, P4, C++

**Tools:** Make, Git, P4, Qemu, Xen

**Tech:** SmartNIC, Storage

### AMD Cryptography Library

Jan. 2022 – Jun. 2025

**Summary:** Initiated as a proof-of-concept for an ISV experiencing performance issues with AES-CFB on AMD-Milan servers. Evolved into a comprehensive cryptographic primitives library.

**Contributions:**

- Designed and developed parallel AES-CFB decryption algorithm achieving 3x performance improvement
- Implemented cryptographic primitives library utilizing both AVX2 and AESNI/SHANI instruction sets
- Developed dynamic dispatcher for runtime selection of most efficient algorithm
- Created OpenSSL provider to enable seamless interoperability

**Languages:** C++

**Tools:** Git, OpenSSL

**Tech:** AES, SHA2, AVX2, AESNI,

SHANI

### AMD Math Library

Feb. 2018 – Dec. 2021

**Summary:** AMD Floating Point Math Library is a high-performance software library primarily written in Assembly (x86\_64) to leverage SIMD and FMA instructions. Led architectural modernization and algorithmic improvements to enhance performance and maintainability.

**Contributions:**

- Implemented advanced optimization techniques including look-up-tables, Estrin's method polynomial for parallel-FMA, and fast integer conversion
- Achieved 30% performance improvement for scalar operations and approximately 2x improvement for vector operations
- Developed dynamic dispatcher using cpuid instruction for runtime algorithm selection
- Redesigned architecture with cache-aligned and interleaved tables

**Languages:** C, Assembly, Python

**Tools:** CMake, GCC, AOCC

**Tech:** x86\_64, SIMD, FMA

## Sr. MEMBER OF TECHNICAL STAFF

### Model0

Feb. 2018 – May. 2021

**Summary:** Initiated as a proof-of-concept for an ISV experiencing performance issues with AES-CFB on AMD-Milan servers. Evolved into a comprehensive cryptographic primitives library.

**Contributions:**

- Designed and developed parallel AES-CFB decryption algorithm achieving 3x performance improvement
- Implemented cryptographic primitives library utilizing both AVX2 and AESNI/SHANI instruction sets
- Developed dynamic dispatcher for runtime selection of most efficient algorithm
- Created OpenSSL provider to enable seamless interoperability

**Languages:** C, ASM, P4, C++

**Tools:** Make, Git, P4, Qemu, Xen

**Tech:** SmartNIC, Storage

## Broadcom Ltd.

PRINCIPAL ENGINEER

2011 – 2016

Bengaluru, India

### ARM IO Virtualization with SMMUv3

Jan. 2014 – Oct. 2016

**Summary:** SMMUv3 is ARM's IOMMU implementation for ARMv8 platforms. Developed comprehensive emulation environment and software model to facilitate driver development.

**Contributions:**

- Designed and developed complete SMMUv3 emulation model for QEMU (merged into QEMU mainline)
- Implemented command queue processing, STE and CD parsing mechanisms
- Developed ARMv8/LPAE pagetable walk implementation supporting Stage1, Stage2, and nested translation
- Implemented comprehensive event reporting and interrupt handling mechanisms

**Languages:** C  
**Tools:** QEMU, Git  
**Tech:** ARMv8, SMMUv3, IOMMU

### SMMUv3 Driver for Vulcan

Jan. 2014 – Oct. 2016

**Summary:** Vulcan is Broadcom's ground-up ARMv8 processor design featuring up to 32 cores with 4 threads each. The SoC integrates SMMUv3 requiring comprehensive software support.

**Contributions:**

- Designed and developed initial Linux driver for SMMUv3 with minimal feature set
- Collaborated with hardware team to identify and resolve design issues
- Contributed bug fixes and enhancements to ARM's open-source SMMUv3 driver
- Developed comprehensive test suite for validating SMMU functionality

**Languages:** C  
**Tools:** Git, Linux Kernel  
**Tech:** ARMv8, SMMUv3, IOMMU

## TECH LEAD

### XLP (MIPS64) SDK Development

May. 2011 – Dec. 2013

**Summary:** XLP is Broadcom's multicore+multithreaded MIPS64 processor featuring up to 80 execution cores with integrated hardware accelerators for networking.

**Contributions:**

- Developed RNG (Hardware Random Number Generator) driver for cryptographic applications
- Implemented Clock Framework driver for dynamic frequency management
- Created CPU voltage and frequency scaling driver for power optimization
- Developed CDE (Compression/Decompression Engine) driver

**Languages:** C  
**Tools:** Linux Kernel, Git  
**Tech:** MIPS64, RNG, CLK Framework

## Cavium Networks

2011 – 2013

Bengaluru, India

TECH LEAD

### OCTEON III - Kexec/Kdump

May. 2011 – Dec. 2013

**Summary:** Kexec enables booting a secondary kernel from running Linux without full system reset. Kdump builds upon Kexec to preserve crashed kernel memory for offline debugging.

**Contributions:**

- Developed complete MIPS architecture port of Kexec and Kdump
- Debugged and resolved critical issues preventing Kexec functionality
- Submitted two patches to upstream Linux kernel, now part of mainline codebase
- Enabled seamless kernel upgrades without disrupting Hybrid SMP configurations

**Languages:** C  
**Tools:** Linux Kernel, GDB  
**Tech:** MIPS64, Kexec, Kdump

### CavHv Hypervisor

Jan. 2012 – Dec. 2013

**Summary:** CavHv is an experimental hypervisor for MIPS64 with hardware virtualization support, developed for Octeon-III series chips.

**Contributions:**

- Designed and implemented hypervisor based on draft MIPS virtualization specification
- Collaborated with compiler and hardware teams to validate virtualization extensions
- Successfully demonstrated concurrent execution of two Linux kernel instances
- Provided critical feedback for virtualization specification refinement

**Languages:** C  
**Tools:** Compiler Toolchain  
**Tech:** MIPS64, Hypervisor, Virtualization

## Cisco Systems

SOFTWARE ENGINEER

2010 – 2011

Bengaluru, India

## Garbage Detector for Linux

Oct. 2010 – Apr. 2011

**Summary:** Cisco IOS runs both as bare-metal and as Linux application, often executing for months or years before memory leak failures.

**Contributions:**

- Designed and implemented garbage detection system using custom C runtime
- Developed separate monitoring thread to intercept malloc() and free() calls
- Implemented intrusive mark-and-sweep algorithm
- Enabled proactive memory leak identification in long-running systems

**Languages:** C

**Tools:** Glibc, Clearcase

**Tech:** Memory Management, Mark-Sweep

## B-Labs

2009 – 2010

London, UK (Remote)

### SR. ENGINEER - CONTRACTOR

## CodeZero Hypervisor

Nov. 2009 – Sep. 2010

**Summary:** CodeZero is a microkernel-based hypervisor for ARM Cortex-A9 running directly on hardware.

**Contributions:**

- Ported CodeZero hypervisor to ARM Cortex-A9 SMP systems
- Developed optimized fast memcpy implementation for ARM
- Extended QEMU with new device and platform support
- Ported Linux kernel to run under CodeZero hypervisor

**Languages:** C, ARM Assembly

**Tools:** Git, QEMU

**Tech:** ARMv7, ARMv6, SMP

## Harman International

2009 – 2009

Bengaluru, India

### ENGINEER

## QNX BSP for PowerPC

Jul. 2009 – Nov. 2009

**Summary:** Porting QNX microkernel to Freescale QorIQ P4080 and P2020 PowerPC processors.

**Contributions:**

- Debugged and resolved P4080 SMP booting issue
- Ported I2C driver to new PowerPC platform
- Developed base drivers including timer and interrupt controller
- Enabled early QNX boot on P2020 and P4080 platforms

**Languages:** C

**Tools:** Make, QNX

**Tech:** PowerPC, P4080, P2020, SMP

## ARM Ltd.

2005 – 2009

Bengaluru, India

### SR. DEVELOPMENT ENGINEER

## OS Support for ARM Cores

Aug. 2005 – Jun. 2009

**Summary:** Platform team responsible for supporting new ARM cores across multiple operating systems.

**Contributions:**

- Developed touch-screen driver for Symbian OS with full gesture support
- Created Symbian OS test automation framework using Python
- Designed interrupt latency measurement driver for TrustZone analysis
- Ported L4Ka::pistachio microkernel to ARM

**Languages:** C, ARM Assembly, Python

**Tools:** FastModels, SoCDesigner

**Tech:** ARM1176, Cortex-A8, TrustZone

## Sasken Ltd.

2004 – 2005

Bengaluru, India

### SR. SOFTWARE ENGINEER

## EFFS Filesystem

Aug. 2004 – Aug. 2005

**Summary:** Developed specialized filesystem for UMTS BTS on VxWorks.

**Contributions:**

- Designed reset-proof filesystem with flat file tree structure
- Developed wear-leveling algorithm for Flash blocks
- Implemented atomic write operations
- Integrated with VxWorks APIs

**Languages:** C

**Tools:** VxWorks

**Tech:** Flash Storage, Wear-Leveling

**Linux SDIO Driver***Jun. 2003 – Aug. 2004***Summary:** Developed high-performance SDIO driver for Marvell 802.11g WiFi chipset.**Contributions:**

- Designed fast SDIO driver supporting 4-bit mode
- Developed 1-bit SDIO driver for legacy hardware
- Optimized data transfer protocols for maximum throughput
- Implemented robust error handling mechanisms

**Languages:** C**Tools:** Linux Kernel, Make**Tech:** ARM, SDIO, WiFi 802.11g