

Prem Mallappa

Software Architect • System & Embedded Software

Bengaluru, India

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Seasoned Software Architect with extensive expertise in designing and developing high-performance embedded systems, system software, Linux kernel drivers, and virtualization technologies. Proficient in a wide range of programming and scripting languages, with a proven track record of delivering robust, scalable solutions in complex technical environments.

A highly analytical and collaborative team player, recognized for strong problem-solving abilities, logical thinking, and a passion for mastering emerging technologies. Committed to driving innovation and excellence through clean architecture, optimized code, and best-in-class engineering practices.

Skills

Leadership Over 22 years of multidisciplinary team and project leadership experience; Software Architecture and Design.

Communications Excellent written and spoken communication skills.

Technology Broad and deep IT expertise, including cloud computing, computer security, operating systems, embedded systems, software & services development, programming languages, etc.

Computer Security Cryptography; virtualization and cloud computing security architecture and implementation; risk management and compliance; intrusion detection and prevention; software security and secure software development.

Programming Languages C, Assembly (x86, ARM, MIPS), Rust, Python, C++, Go, BASH

Operating Systems Linux, FreeBSD, QNX, VxWorks, Symbian

Architecture x86, ARM - v6,v7,v8, MIPS64, PowerPC, RISC-V

Development Tools GCC, Clang, Git, Make, CMake, ARM Development Tools, Keil, JTAG, Docker,

Specialized Skills Linux Kernel Development, Device Drivers, Embedded Systems, System Software, Performance Optimization, Cryptography, Filesystem Development

Education

Masters (Computer Science)

Pilani, Rajasthan, India

BITS Pilani

2016

Bachelors (Computer Science)

*Adichunchangiri Institute of Technology,
Karnataka, India*

Visvesvaraya Technological University (VTU)

2002

Experience

AMD Ltd.

2018 – Present

Bengaluru, India

PRINCIPAL ENGINEER

Worked in multiple teams within AMD including **AMD LibM**, **AOCL Cryptography**, **BSP**, and **NVMe in Pensando** BU. Every project was different, requiring quick learning and adaptation to new domains. The role also involved leading a team of four-to-six engineers in various projects. I was also part of the leadership team where I mentored engineers from across AOCL and Pensando BU.

SR. MEMBER OF TECHNICAL STAFF

Worked on Model0 project which was pre-silicon validation of next generation AMD cores, including Zen2 and Zen3. The role involved working with hardware team to bring up bare-minimum processor configuration with just core and memory controller, and run Linux, stressors and benchmarks. This involved working on low-level firmware, bootloaders, Linux kernel and performance analysis tools.

Broadcom Ltd.

2014 – 2016

Bengaluru, India

PRINCIPAL ENGINEER

Architected foundational software stack for Broadcom Vulcan, a multicore-multithreaded ARMv8 64-bit server processor. Engineered complete SMMUv3 (System Memory Management Unit) driver infrastructure supporting advanced IOMMU virtualization. Developed and contributed SMMUv3 emulation model to QEMU mainline, enabling early platform validation and ecosystem enablement. Implemented comprehensive virtualization features including command queue processing, STE/CD descriptor parsing, multi-level page table walks, and stage-1/stage-2 address translation.

Cavium India Pvt. Ltd.

2011 – 2013

Bengaluru, India

TECH LEAD

Led low-level software development for Cavium Octeon III (MIPS64) multicore network processors, delivering stable platform firmware for networking customers. Resolved a critical KEXEC kernel bug and authored the full MIPS64 port of the Kexec/Kdump crash dump infrastructure, ultimately merged into Linux mainline. Engineered a bare-metal core dump generation framework with a host-resident daemon that enabled detailed post-mortem GDB analysis during bring-up. Designed and implemented the CavHv hypervisor for MIPS64 architecture using experimental hardware virtualization extensions to validate next-generation features.

ARM Ltd.

2005 – 2009

Bengaluru, India

SR. DEVELOPMENT ENGINEER

Executed comprehensive OS porting initiatives for emerging ARM architectures including ARM1176JZFS with TrustZone security extensions and the Cortex-A8 application processor. Developed a production-grade touch-screen driver for Symbian OS along with a Python-based automated validation framework used across multiple programs. Designed a precision interrupt latency measurement infrastructure that quantified TrustZone secure-world context switching overhead for silicon partners. Ported the L4Ka::Pistachio microkernel to ARM architecture, enabling virtualization research and multiple proof-of-concept implementations.

Sasken Communication Technologies Ltd.

2004 – 2005

Bengaluru, India

SR. SOFTWARE ENGINEER

Architected and maintained the Extended File System (EFS) for VxWorks-based UMTS base station infrastructure, balancing throughput with resiliency requirements. Engineered a reset-resilient filesystem with advanced wear-leveling algorithms so data integrity held across unexpected power cycles in the field. Designed a flash-optimized flat file tree structure that minimized write amplification and significantly extended device longevity.

Global Edge Software Ltd.

2003 – 2004

Bengaluru, India

SOFTWARE ENGINEER

Designed and implemented a comprehensive SDIO host controller driver for Linux on Intel StrongARM embedded platforms used in consumer devices. Engineered a high-performance 4-bit SDIO driver for Marvell 802.11g WiFi chipsets that consistently achieved maximum theoretical throughput. Optimized DMA transfers and interrupt handling paths to minimize latency and maximize wireless data transfer efficiency under heavy load.

Short Stints

VSPL Ltd.

Bengaluru, India

Software Architect

Nov. 2016 – Jan. 2018

Cisco Ltd.

Bengaluru, India

Software Engineer

Oct. 2010 – Apr. 2011

B-Labs, London UK

Bengaluru, India

Sr. Engineer - Contractor

Nov. 2009 – Sep. 2010

Harman International

Bengaluru, India

Engineer

Jul. 2009 – Nov. 2009

Open Source

QEMU [\(Link\)](#)

2014-2016

- SMMUv3 (IOMMU) emulation support for ARMv8
- Designed and implemented SMMUv3 model merged into mainline
- Added support for Stage1, Stage2, and nested virtualization
- Implemented command queue processing and page table walk

Linux Kernel [\(Link\)](#)

2011-2016

- MIPS Kexec/Kdump port and IOMMU subsystem
- Developed MIPS64 port of Kexec and Kdump (merged upstream)
- Fixed critical bugs in KEXEC for Cavium Octeon platforms
- Contributed to IOMMU/SMMUv3 driver development

GLIBC [\(Link\)](#)

2018-2020

- Performance optimizations for AMD processors
- Fixed memcpy behaviour on AMD processors
- Optimized string functions for x86₆₄ architecture
- Performance improvements for memory operations

AMD LibM [\(Link\)](#)

2018-Present

- Open source math library for AMD processors
- Core contributor to open sourcing AMD Math Library
- Optimized transcendental functions (exp, log, pow, trig)
- Implemented SIMD/FMA optimizations for vector operations

Projects

AMD Ltd.

PRINCIPAL ENGINEER

2018 – Present

Bengaluru, India

AMD Pensando SmartNIC Platform

Jun. 2025 – Present –

Synopsis

Leading development of storage acceleration solutions on AMD Pensando Data Processing Units (DPUs). Architecting high-performance offload engines for NVMe-oF and storage virtualization leveraging programmable P4 pipelines and hardware acceleration.

Details

Architecting NVMe-over-Fabrics offload engine on Pensando DPU achieving sub-10µs latency. Developing P4-based packet processing pipelines for storage protocol acceleration. Implementing Xen-based virtualization stack for secure multi-tenant storage isolation. Designing hardware-accelerated compression and encryption for in-line data protection.

Languages: C, C++, P4, Python

Tools: Git, GDB, Qemu, Xen Hypervisor, DPDK

Tech: NVMe-oF, RDMA, SmartNIC, DPU, Hardware Offload, Packet Processing Pipelines

AMD Cryptography Library

Jan. 2023 – Jun. 2025 –

Synopsis

Initiated as proof-of-concept to address ISV performance bottlenecks with AES-CFB cryptography on AMD EPYC Milan servers. Evolved into comprehensive cryptographic primitives library delivering production-grade implementations of AES and SHA algorithms optimized for AMD processor architectures.

Details

Engineered parallel AES-CFB decryption algorithm delivering 3x performance improvement over standard OpenSSL implementation. Developed multi-algorithm cryptographic library supporting AVX2, AESNI, and SHANI instruction set extensions. Implemented CPUID-based runtime dispatcher for automatic selection of optimal algorithm variant per processor generation. Integrated library as OpenSSL provider enabling transparent drop-in replacement for existing applications.

Languages: C++, x86-64 Assembly

Tools: Git, CMake, GCC, Clang, OpenSSL Provider API

Tech: AES-CFB, AES-GCM, SHA256, SHA512, AVX2, AVX-512, AESNI, SHANI, VAES

AMD Math Library (AOCL-libm)

Dec. 2019 – Dec. 2022 –

Synopsis

High-performance mathematical library providing optimized implementations of transcendental functions (exp, log, pow, trigonometric) for AMD EPYC and Ryzen processors. Led comprehensive modernization initiative to enhance performance through advanced algorithmic techniques and microarchitecture-aware optimizations.

Details

Implemented Estrin's polynomial evaluation method enabling parallel FMA instruction utilization for reduced latency. Developed vectorized lookup table architecture with cache-line alignment and interleaving for optimal memory bandwidth. Achieved 30% performance improvement in scalar operations and 2x improvement in vector operations across function portfolio. Engineered CPUID-based dynamic dispatcher selecting optimal code paths based on processor generation and feature flags.

Languages: C, x86-64 Assembly, Python

Tools: CMake, GCC, Clang, AOCC, Git, Perf, VTune

Tech: AVX2, AVX-512, FMA3, FMA4, Estrin Polynomial, SIMD Vectorization, Cache Optimization

Sr. Member of Technical Staff

Modelo

Feb. 2018 – Dec. 2019 –

Synopsis

Next generation AMD processors needed to be tested before IO and other components are integrated, as part of the **shift-left** strategy. Allows faster integration and

Details

<TBD>

Languages: C, x86-64 Assembly, Python

Tools: CMake, GCC, Linux Kernel, Virtualization

Tech: AMD-SEV, AMD-SNP

Broadcom Ltd.

2011 – 2016

Bengaluru, India

PRINCIPAL ENGINEER

ARM IO Virtualization with SMMUv3

Jan. 2014 – Oct. 2016 –

Synopsis

Developed comprehensive SMMUv3 (ARM System Memory Management Unit) emulation infrastructure enabling early software development and validation for Broadcom Vulcan ARMv8 server platform. SMMUv3 provides hardware-based IO virtualization with multi-stage address translation and device isolation capabilities.

Details

Architected and implemented complete SMMUv3 device model for QEMU, successfully upstreamed to mainline repository. Developed command queue processing engine supporting asynchronous invalidation and event notification. Implemented ARMv8 LPAE page table walker supporting Stage-1, Stage-2, and nested translation modes. Designed comprehensive event reporting mechanism with configurable interrupt generation and fault handling.

Languages: C

Tools: QEMU Device Model, Git, GDB, ARM Fast Models

Tech: ARMv8, SMMUv3, IOMMU, 2-Stage Translation, Command Queue, Event Records

SMMUv3 Driver for Broadcom Vulcan

Jan. 2014 – Oct. 2016 –

Synopsis	Broadcom Vulcan represents ground-up ARMv8 server processor design featuring 32 cores with simultaneous multithreading (4 threads per core). Engineered production Linux driver for integrated SMMUv3 enabling secure IO virtualization and DMA protection for datacenter workloads.
Details	Developed initial Linux kernel driver implementing SMMUv3 core functionality including StreamID-based device isolation. Collaborated cross-functionally with hardware design team to identify and resolve silicon errata and performance bottlenecks. Contributed bug fixes and feature enhancements to ARM's reference SMMUv3 driver implementation. Designed and executed comprehensive validation suite covering multi-stage translation and fault handling scenarios.

Languages: C
Tools: Git, GCC, ARM Cross Compiler, Kernel Build System
Tech: Linux Kernel Driver, IOMMU Framework, DMA API, Device Tree, MSI Interrupts

TECH LEAD

Broadcom XLP (MIPS64) Platform Enablement

May. 2011 – Dec. 2013 –

Synopsis	Broadcom XLP represents high-performance multicore MIPS64 processor architecture featuring up to 32 cores with 2-way multithreading and integrated hardware acceleration engines for networking and security workloads. Led Linux kernel enablement delivering production-grade device drivers and power management infrastructure.
Details	Developed hardware random number generator driver providing high-entropy source for cryptographic applications. Implemented Common Clock Framework driver enabling dynamic frequency scaling across processor domains. Engineered DVFS (Dynamic Voltage and Frequency Scaling) driver reducing power consumption by 40% under variable workloads. Created CDE (Compression/Decompression Engine) driver offloading network packet processing to hardware accelerators.

Languages: C, MIPS Assembly
Tools: Git, GCC, MIPS Cross Compiler, Device Tree Compiler
Tech: MIPS64 Oceon, Common Clock Framework, DVFS, Hardware RNG, CDE Engine

Cavium Networks

2011 – 2013

Bengaluru, India

TECH LEAD

Cavium OCTEON III - Kexec/Kdump Implementation

May. 2011 – Dec. 2013 –

Synopsis	Kexec enables fast kernel reboot without firmware re-initialization, while Kdump leverages this mechanism for capturing crash dumps. Developed complete MIPS64 architecture port enabling zero-downtime kernel updates and comprehensive crash analysis for Cavium OCTEON network processors.
Details	Architected and implemented complete MIPS64 port of Kexec/Kdump infrastructure supporting OCTEON's Hybrid SMP topology. Resolved critical architectural bug preventing Kexec functionality on MIPS platforms. Successfully upstreamed two kernel patches to Linux mainline, now universally deployed across MIPS64 systems. Enabled seamless kernel hot-patching without disrupting Hybrid SMP core configurations or network traffic.

Languages: C, MIPS64 Assembly
Tools: Git, GDB, Crash Analysis, Kernel Build System
Tech: Kexec, Kdump, ELF Boot Protocol, Hybrid SMP, Memory Reservation, Crash Kernel

CavHv Hypervisor for MIPS64

Jan. 2012 – Dec. 2013 –

Synopsis	Experimental Type-1 hypervisor leveraging MIPS Virtualization (VZ) hardware extensions for Cavium OCTEON-III processors. Collaborated with MIPS architecture team and Cavium hardware designers to validate draft virtualization specification through practical implementation.
Details	Designed and implemented bare-metal Type-1 hypervisor based on MIPS Virtualization Extensions draft specification. Developed guest context management supporting CP0 register virtualization and root/guest mode transitions. Successfully demonstrated concurrent execution of two independent Linux kernel instances with isolated address spaces. Provided critical architectural feedback influencing finalization of MIPS VZ specification.

Languages: C, MIPS64 Assembly
Tools: GCC, MIPS Toolchain, GDB, QEMU
Tech: MIPS VZ Extensions, Type-1 Hypervisor, CP0 Virtualization, Root/Guest Mode

Cisco Systems
SOFTWARE ENGINEER

2010 – 2011

Bengaluru, India

Memory Leak Detection for Cisco IOS

Oct. 2010 – Apr. 2011 –

- Synopsis** Cisco IOS operates in both bare-metal and Linux environments with multi-month uptimes, making memory leak detection critical. Developed non-intrusive garbage detection system enabling proactive identification of unreachable memory in long-running network infrastructure.
- Details** Architected custom C runtime wrapper intercepting malloc/free operations without application source modifications. Implemented concurrent monitoring thread executing intrusive mark-and-sweep algorithm during idle periods. Designed reporting mechanism distinguishing legitimate long-lived allocations from leaked memory. Enabled field deployment teams to diagnose memory leaks before service-impacting failures occurred.

Languages: C
Tools: GCC, Glibc Hooks, Clearcase, Runtime Analysis
Tech: Mark-Sweep Algorithm, Malloc Interposition, Conservative GC, Graph Traversal

B-Labs

2009 – 2010

London, UK (Remote)

SR. ENGINEER - CONTRACTOR

CodeZero Hypervisor ARM Port

Nov. 2009 – Sep. 2010 –

- Synopsis** CodeZero represents microkernel-based hypervisor architecture targeting ARM Cortex-A9 multicore processors. Executed comprehensive platform bring-up enabling bare-metal execution on emerging ARMv7 SMP hardware.
- Details** Ported complete CodeZero hypervisor infrastructure to ARM Cortex-A9 SMP platforms including cache coherency management. Developed ARM-optimized memcpy implementation leveraging NEON SIMD instructions for enhanced performance. Extended QEMU device models supporting CodeZero-specific platform requirements. Ported Linux kernel as guest OS executing under CodeZero hypervisor supervision.

Languages: C, ARMv7 Assembly
Tools: Git, QEMU, ARM GCC, JTAG Debugger
Tech: ARM Cortex-A9 MPCore, SMP, Cache Coherency, NEON SIMD, Microkernel IPC

Harman International
ENGINEER

2009 – 2009

Bengaluru, India

QNX BSP for Freescale PowerPC Platforms

Jul. 2009 – Nov. 2009 –

- Synopsis** Board Support Package development for QNX real-time operating system on Freescale QorIQ P4080 (8-core) and P2020 (dual-core) PowerPC processors targeting automotive infotainment systems. Enabled QNX deployment on next-generation multicore embedded platforms.
- Details** Resolved critical SMP initialization bug preventing P4080 8-core bring-up on QNX RTOS. Ported I2C controller driver enabling communication with touchscreen, audio codecs, and sensor peripherals. Developed foundational BSP infrastructure including timer subsystem and interrupt controller drivers. Successfully achieved early boot milestones on both P2020 and P4080 reference platforms.

Languages: C, PowerPC e500 Assembly
Tools: QNX Momentics IDE, Make, PowerPC Cross Compiler
Tech: QorIQ P4080, P2020, e500mc Core, AltiVec, SMP Spinlocks, I2C Protocol

ARM Ltd.
SR. DEVELOPMENT ENGINEER

2005 – 2009

Bengaluru, India

Multi-OS Enablement for ARM Processor Portfolio

Aug. 2005 – Jun. 2009 –

- Synopsis** Platform engineering team responsible for enabling diverse operating systems on emerging ARM processor cores. Supported major OS ecosystems including Linux, Symbian, and QNX across ARM11 (ARM1176JZF-S with TrustZone) and Cortex-A8 architectures, facilitating early partner evaluation and ecosystem development.
- Details** Developed production-grade resistive touchscreen driver for Symbian OS with multi-touch gesture recognition. Architected Python-based test automation framework reducing Symbian OS validation cycle time by 60%. Designed precision interrupt latency measurement infrastructure quantifying TrustZone secure-world context switch overhead. Ported L4Ka::Pistachio microkernel to ARM architecture enabling virtualization research and proof-of-concepts.

Languages: C, ARMv6/v7 Assembly, Python
Tools: ARM Fast Models, DS-5 Debugger, RealView Compiler, SoCDesigner
Tech: ARM1176JZF-S, Cortex-A8, TrustZone, Symbian OS, L4 Microkernel, VFP

Sasken Ltd.

SR. SOFTWARE ENGINEER

2004 – 2005

Bengaluru, India

EFFS - Embedded Flash Filesystem for UMTS Infrastructure

Aug. 2004 – Aug. 2005 –

Synopsis

Designed and maintained Extended Flash File System (EFFS) for VxWorks-based UMTS base station controllers. Addressed unique constraints of Flash storage including limited erase cycles, asymmetric read/write performance, and power-failure resilience requirements for telecom infrastructure.

Details

Architected power-failure-resilient filesystem ensuring data integrity across unexpected resets in field deployments. Developed wear-leveling algorithm distributing write operations across Flash blocks extending device lifespan by 3x. Implemented atomic transaction mechanism with flat file tree optimized for Flash characteristics. Integrated filesystem with VxWorks I/O subsystem maintaining POSIX-like API compatibility.

Languages: C**Tools:** Tornado IDE, Wind River Compiler, VxWorks RTOS**Tech:** NOR Flash, Wear Leveling, Erase Block Management, Power-Fail Safe, POSIX I/O**Global Edge Software**

2003 – 2004

Bengaluru, India

SOFTWARE ENGINEER

Linux SDIO Host Controller Driver for Wireless Connectivity

Jun. 2003 – Aug. 2004 –

Synopsis

Developed high-performance SDIO host controller driver for Intel StrongARM embedded platforms enabling wireless connectivity through Marvell 802.11g WiFi chipsets. Optimized for maximum throughput on resource-constrained ARM processors targeting portable and embedded applications.

Details

Architected and implemented complete SDIO host controller driver supporting 4-bit wide bus mode and clock management. Engineered DMA-based transfer mechanism achieving maximum theoretical 802.11g throughput (54 Mbps) on StrongARM platform. Optimized interrupt handling and data transfer pathways minimizing CPU overhead and latency. Developed comprehensive integration with Marvell WiFi chipset firmware achieving production-grade wireless connectivity.

Languages: C**Tools:** Git, GCC, GDB, ARM Cross Compiler, Logic Analyzer**Tech:** Intel StrongARM SA-1110, SDIO Protocol, 802.11g WiFi, DMA Engine, IRQ Handling

Awards

Q3 2018 **Spotlight**

AMD

Helping Emulation team find design bug in data fabric

Q2 2019 **Spotlight**

AMD

Optimization of exp() and improving performance by 30%

Q2 2019 **Director Spotlight**

AMD

Supporting Arden Ubuntu emulation boot, fixing initramfs delayed mount

Q4 2020 **Spotlight**

AMD

Providing important patches to GLIBC to fix memcpy behaviour on AMD, open sourcing AMD LibM

Q3 2021 **Spotlight**

AMD

Delivering Cryptography PoC (CFB based parallel decrypting), increases performance by 3x