1. Description

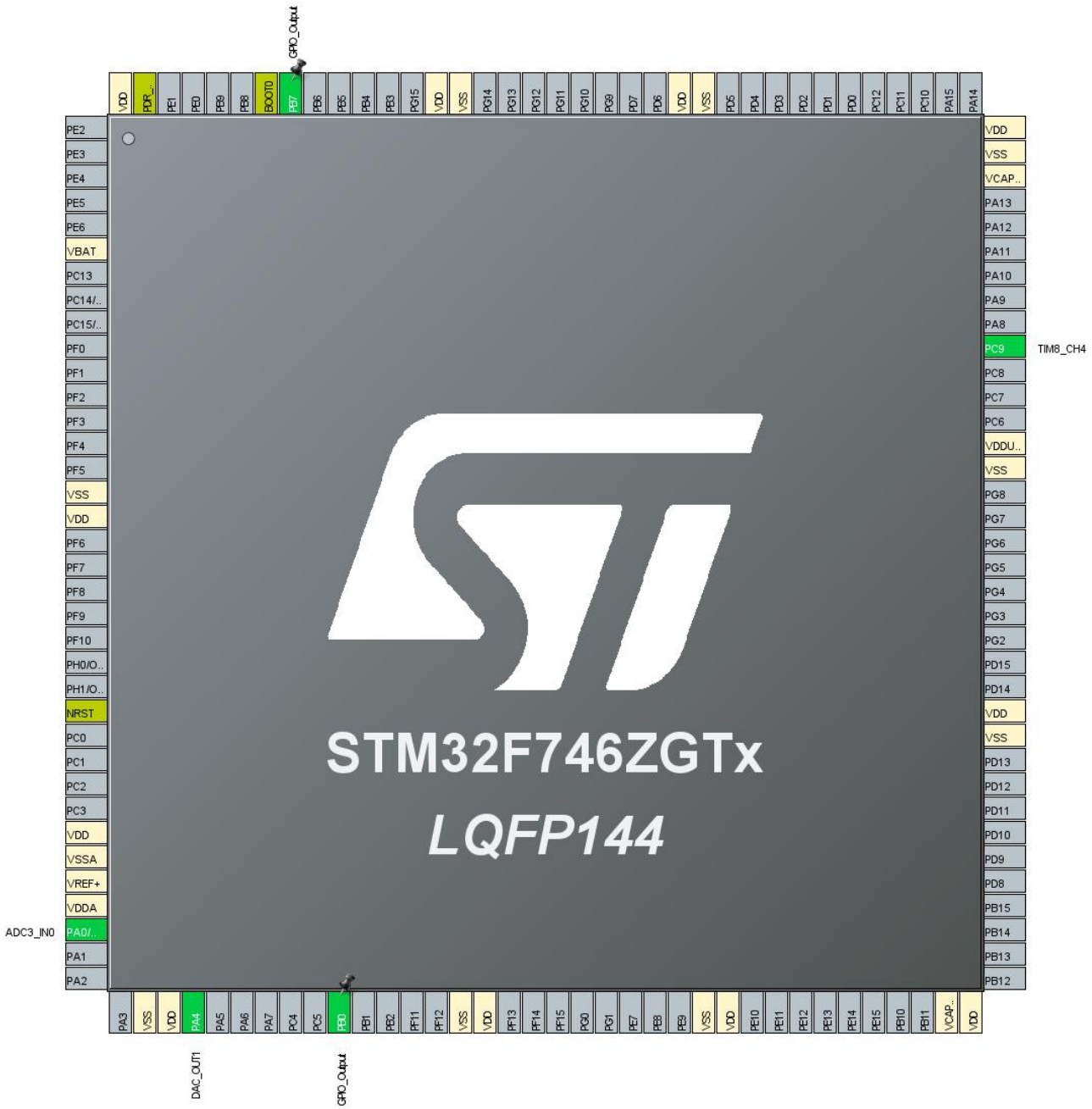
1.1. Project

Project Name	Body_sythesyser
Board Name	custom
Generated with:	STM32CubeMX 5.4.0
Date	02/19/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

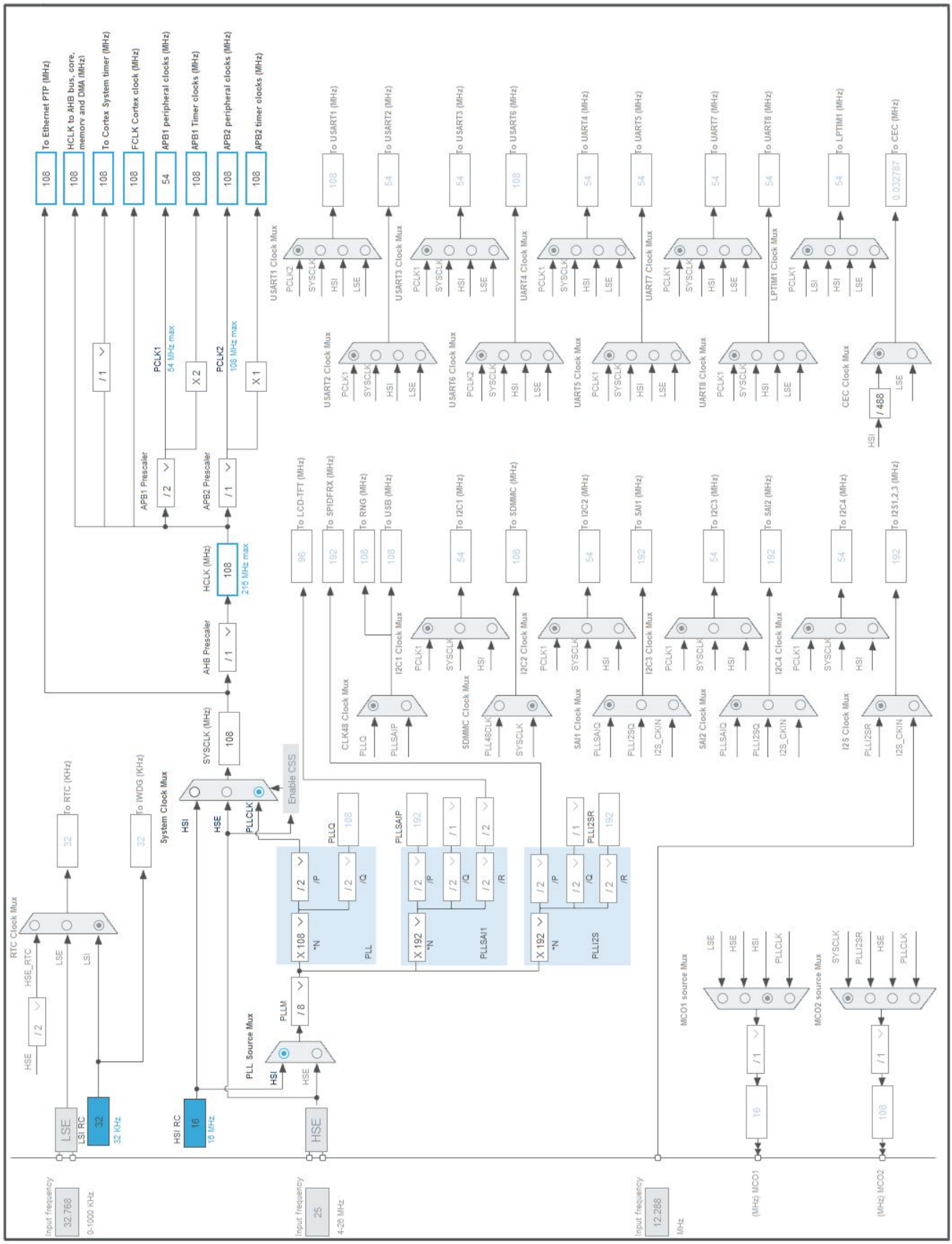


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC3_IN0	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
46	PB0 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
99	PC9	I/O	TIM8_CH4	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
137	PB7 *	I/O	GPIO_Output	
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Body_sythesyser
Project Folder	E:\UNI\DSP-Labor\Body_Synth_\Body_sythesyser
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	027590_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC3

mode: IN0

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 5 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. DAC

mode: OUT1 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 8 Trigger Out event ***
Wave generation mode	Disabled

7.4. GPIO

7.5. RCC

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

7.6. SYS

Timebase Source: SysTick

7.7. TIM6

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM8

Clock Source : Internal Clock

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10800 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable

Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PA0/WKUP	ADC3_IN0	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
TIM8	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	Low
ADC3	DMA2_Stream0	Peripheral To Memory	Low

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC3: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report