
STM32
CubeMX

1. Description

1.1. Project

Project Name	Body-Synthesizer_STM32_F746ZG
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	09/16/2021

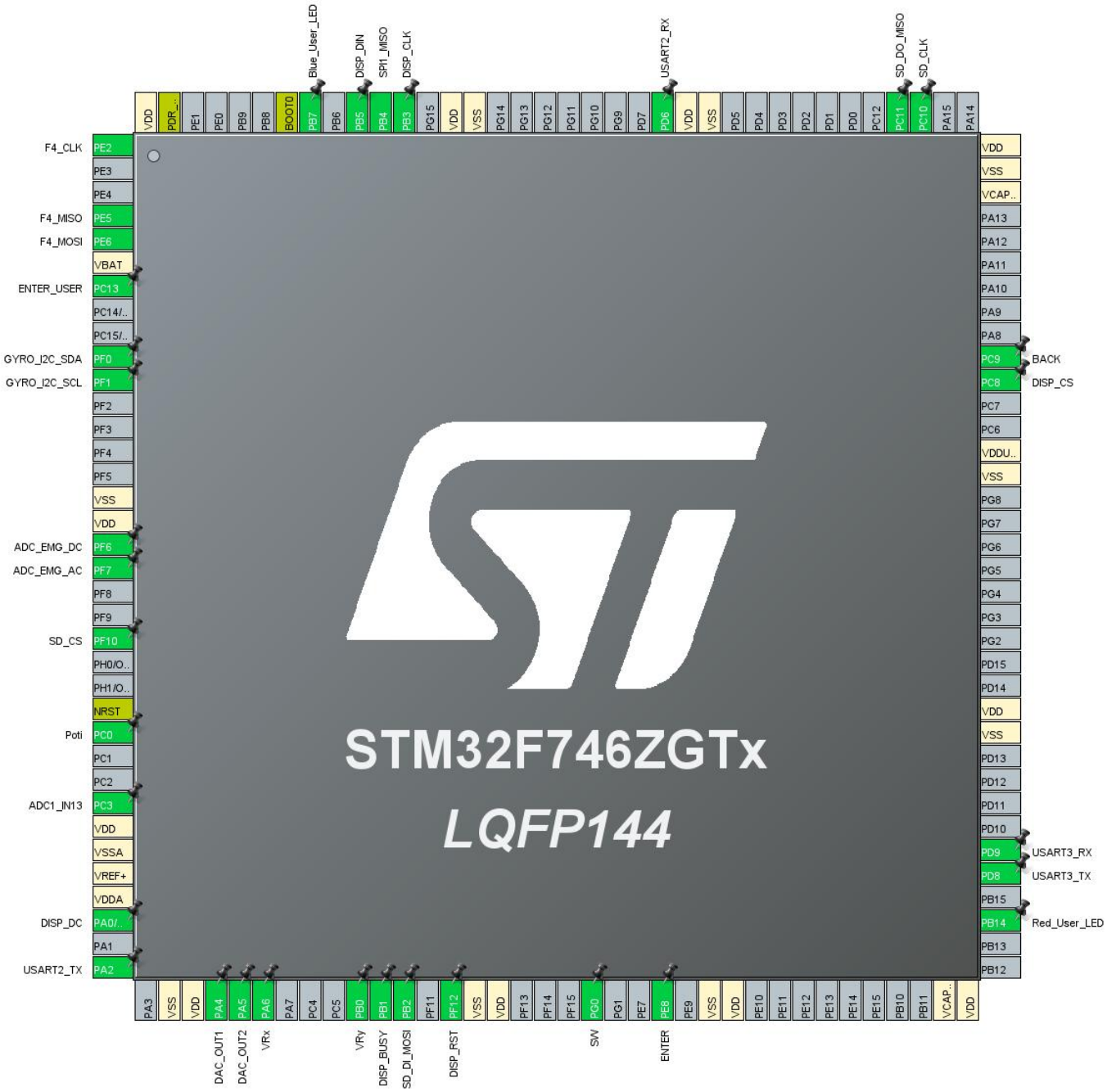
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



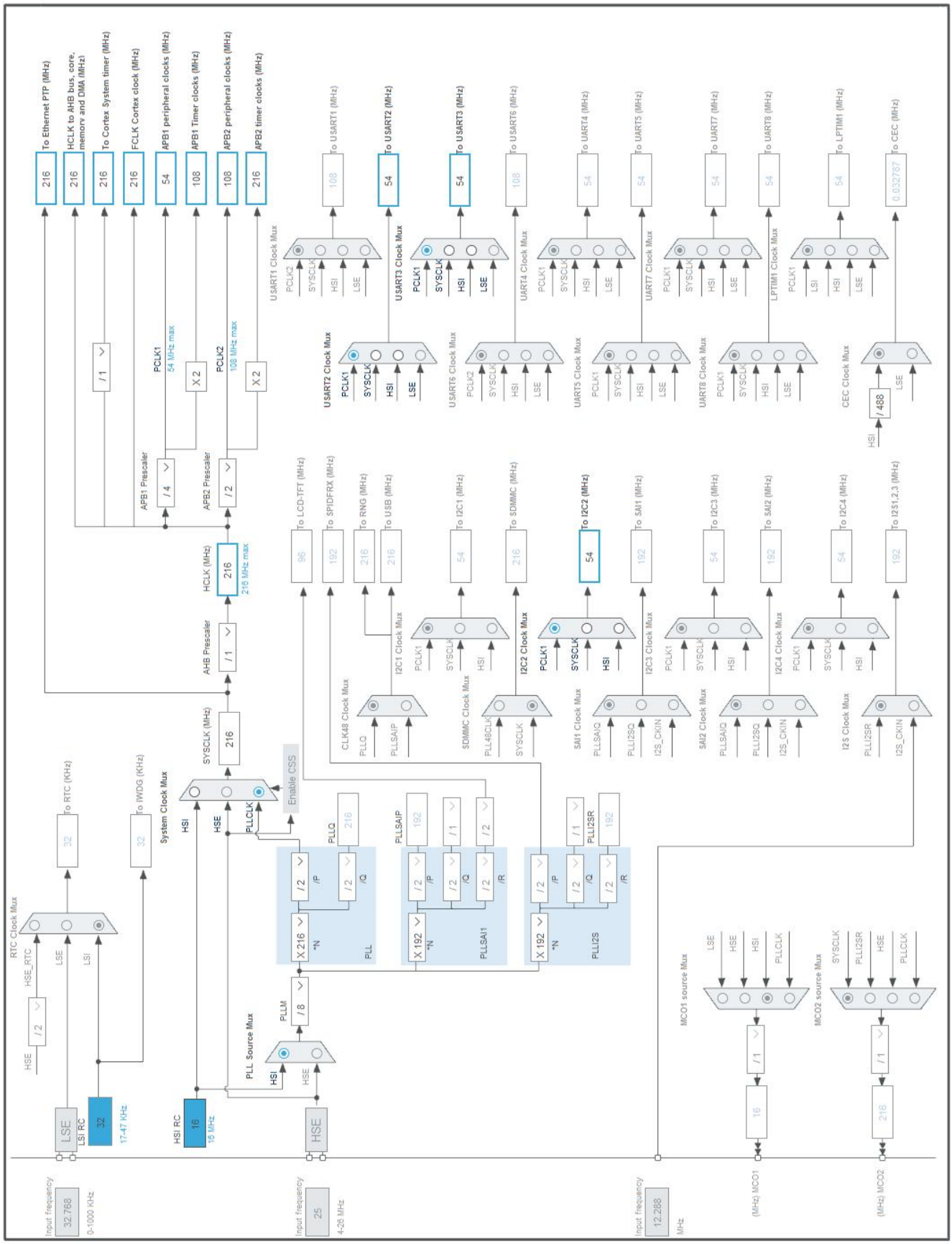
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	F4_CLK
4	PE5	I/O	SPI4_MISO	F4_MISO
5	PE6	I/O	SPI4_MOSI	F4_MOSI
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	ENTER_USER
10	PF0	I/O	I2C2_SDA	GYRO_I2C_SDA
11	PF1	I/O	I2C2_SCL	GYRO_I2C_SCL
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	ADC3_IN4	ADC_EMG_DC
19	PF7	I/O	ADC3_IN5	ADC_EMG_AC
22	PF10 *	I/O	GPIO_Output	SD_CS
25	NRST	Reset		
26	PC0	I/O	ADC2_IN10	Poti
29	PC3	I/O	ADC1_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP *	I/O	GPIO_Output	DISP_DC
36	PA2	I/O	USART2_TX	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
41	PA5	I/O	DAC_OUT2	
42	PA6	I/O	ADC2_IN6	VRx
46	PB0	I/O	ADC2_IN8	VRy
47	PB1 *	I/O	GPIO_Input	DISP_BUSY
48	PB2	I/O	SPI3_MOSI	SD_DI_MOSI
50	PF12 *	I/O	GPIO_Output	DISP_RST
51	VSS	Power		
52	VDD	Power		
56	PG0	I/O	GPIO_EXTI0	SW
59	PE8	I/O	GPIO_EXTI8	ENTER
61	VSS	Power		
62	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
71	VCAP_1	Power		
72	VDD	Power		
75	PB14 *	I/O	GPIO_Output	Red_User_LED
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
98	PC8 *	I/O	GPIO_Output	DISP_CS
99	PC9	I/O	GPIO_EXTI9	BACK
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
111	PC10	I/O	SPI3_SCK	SD_CLK
112	PC11	I/O	SPI3_MISO	SD_DO_MISO
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	USART2_RX	
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SPI1_SCK	DISP_CLK
134	PB4	I/O	SPI1_MISO	
135	PB5	I/O	SPI1_MOSI	DISP_DIN
137	PB7 *	I/O	GPIO_Output	Blue_User_LED
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Body-Synthesizer_STM32_F746ZG
Project Folder	C:\Users\Marc Bielen\Documents\Studium\Master TU Berlin\6. Semester\body-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM8_Init	TIM8
4	MX_DMA_Init	DMA
5	MX_DAC_Init	DAC
6	MX_TIM6_Init	TIM6
7	MX_USART3_UART_Init	USART3
8	MX_ADC2_Init	ADC2
9	MX_SPI1_Init	SPI1
10	MX_SPI3_Init	SPI3
11	MX_USART2_UART_Init	USART2

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_TIM4_Init	TIM4
14	MX_FATFS_Init	FATFS
15	MX_TIM1_Init	TIM1
16	MX_ADC1_Init	ADC1
17	MX_TIM5_Init	TIM5
18	MX_ADC3_Init	ADC3
19	MX_I2C2_Init	I2C2
20	MX_SPI4_Init	SPI4
21	MX_TIM7_Init	TIM7

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	DS10916_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

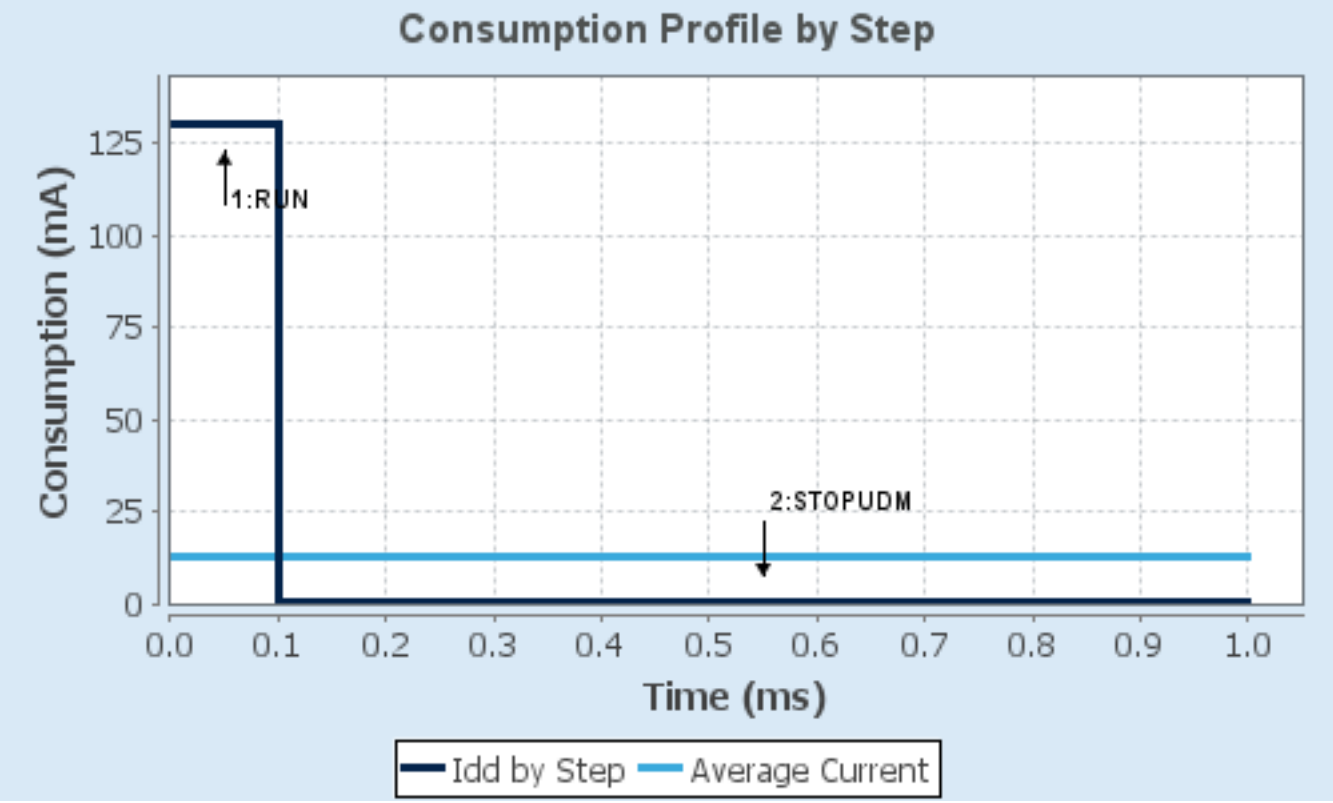
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	87.84	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN13

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 13
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN6

mode: IN8

mode: IN10

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**3 ***
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 6
Sampling Time	**15 Cycles ***
Rank	**2 ***
Channel	**Channel 8 ***
Sampling Time	**15 Cycles ***
Rank	**3 ***
Channel	**Channel 10 ***
Sampling Time	**15 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3

mode: IN4

mode: IN5

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion
ADC_Regular_ConversionMode:	
Number Of Conversion	**2 ***
External Trigger Conversion Source	**Timer 1 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 4
Sampling Time	**15 Cycles ***
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	**15 Cycles ***
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

7.4. DAC
mode: OUT1 Configuration
mode: OUT2 Configuration
7.4.1. Parameter Settings:

DAC Out1 Settings:	
Output Buffer	Enable
Trigger	**Timer 8 Trigger Out event ***
Wave generation mode	Disabled
DAC Out2 Settings:	
Output Buffer	Enable
Trigger	**Timer 8 Trigger Out event ***
Wave generation mode	Disabled

7.5. I2C2
I2C: I2C
7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola

Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**1.6875 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SPI3

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**1.6875 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.9. SPI4

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola

Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**6.75 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Software

7.10. SYS

Timebase Source: SysTick

7.11. TIM1

Clock Source : Internal Clock

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**215 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.12. TIM2

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**59999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.13. TIM4

Clock Source : Internal Clock

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**59999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.14. TIM5

mode: Clock Source

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.15. TIM6

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**53999 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.16. TIM7

mode: Activated

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.17. TIM8

Clock Source : Internal Clock

Channel4: PWM Generation No Output

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10800 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.18. USART2

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USART3

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. FATFS

mode: User-defined

7.20.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	**Enabled with static working buffer on the BSS ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	**4096 ***
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC0	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	Poti
	PA6	ADC2_IN6	Analog mode	No pull-up and no pull-down	n/a	VRx
	PB0	ADC2_IN8	Analog mode	No pull-up and no pull-down	n/a	VRy
ADC3	PF6	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	ADC_EMG_DC
	PF7	ADC3_IN5	Analog mode	No pull-up and no pull-down	n/a	ADC_EMG_AC
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	GYRO_I2C_SDA
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	GYRO_I2C_SCL
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DISP_CLK
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DISP_DIN
SPI3	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_DI_MOSI
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_CLK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_DO_MISO
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	F4_CLK
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	F4_MISO
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	F4_MOSI
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ENTER_USER
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PA0/WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_DC
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DISP_BUSY
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_RST
	PG0	GPIO_EXTI0	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	SW
	PE8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ENTER
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Red_User_LED
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_CS
	PC9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	BACK
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Blue_User_LED

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	**Very High ***
ADC2	DMA2_Stream2	Peripheral To Memory	**High ***
ADC3	DMA2_Stream1	Peripheral To Memory	**High ***
DAC2	DMA1_Stream6	Memory To Peripheral	**Very High ***
SPI4_RX	DMA2_Stream3	Peripheral To Memory	Low
SPI4_TX	DMA2_Stream4	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

DAC2: DMA1_Stream6 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

SPI4_RX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_TX: DMA2_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	0	0
EXTI line[9:5] interrupts	true	1	0
TIM2 global interrupt	true	1	0
TIM4 global interrupt	true	1	0
EXTI line[15:10] interrupts	true	1	0
TIM5 global interrupt	true	1	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	1	0
DMA2 stream2 global interrupt	true	2	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream4 global interrupt	true	0	0
SPI4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

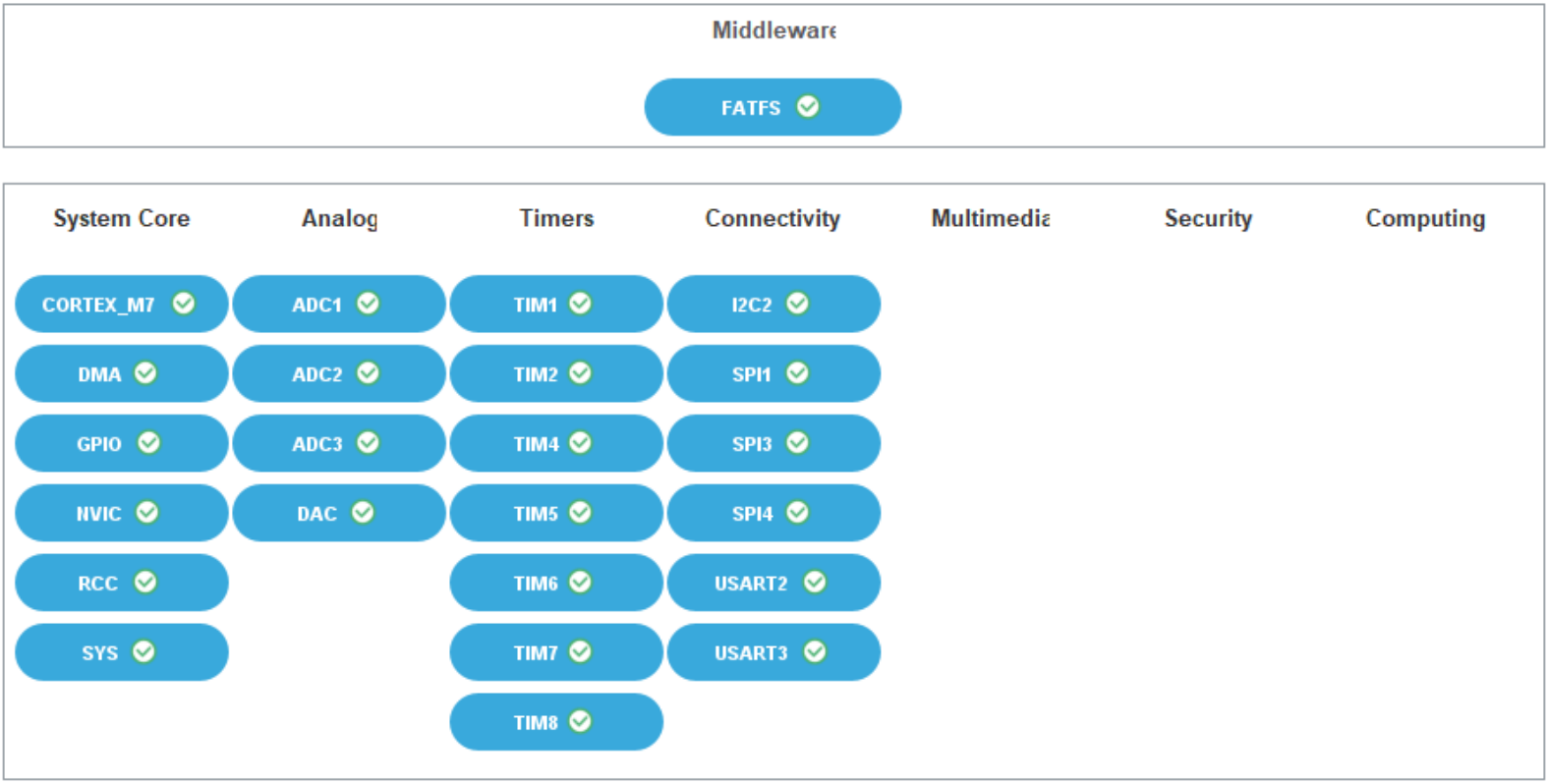
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM5 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream4 global interrupt	false	true	true
SPI4 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00166116.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00124865.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00145382.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00340311.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf