Processor Architecture

The CPU is a custom TTL design that shows significant similarities to the Hewlett-Packard 3000. It has virtual memory with a 2 kB page size, a stack-based instruction set, and fixed-width 16-bit instructions. Raw processor speed is about 0.8 MIPS per processor, giving 13 MIPS in a fully equipped 16-processor system.

Memory Addressing

The T/16 is a 16-bit machine, and the address space is limited to 16 bits in width. Even in the late 1970s, this was beginning to become a problem, and Tandem addressed it by providing a total of four address spaces at any one time:

User code
: This address space contains the executable code. It is read-only and shared between all processes that use it. Due to the architecture (separate memory for each CPU), the code can be shared only on a specific CPU.

User data
: The data space for user processes.

System code
: The code for the kernel.

System data
: The kernel data space.

With one exception, only one data space and one code space is accessible at any one time. They are specified in the *Environment Register*, which contains a number of flags describing the current CPU state, as shown in Figure 8-2.

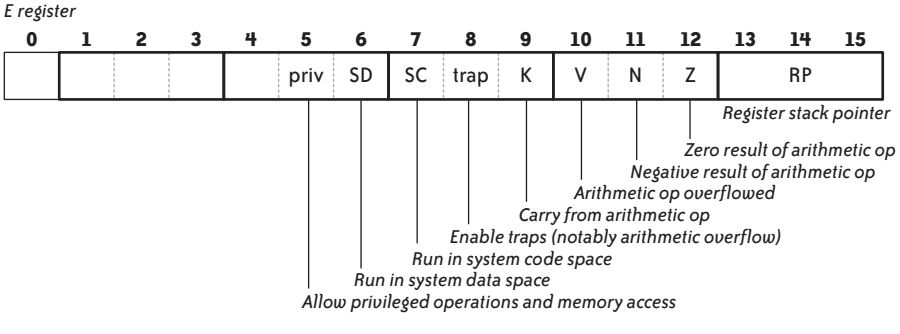

FIGURE 8-2. E register

The SD bit determines the data space, and the SC bit determines the code space. The SG-relative addressing mode is an exception to this rule: it always addresses system data.