



Automated Instruction Stream Throughput Prediction for Intel and AMD Microarchitectures

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Overview

1. Analytic Performance Modeling

Why?

Components

What we do in this work

2. Model Construction

Model assumptions: port model, full throughput,... Microbenchmarking for instruction throughput (and latency) Putting together a prediction

3. OSACA: Automating the in-core model construction

Overview
Structure and Output

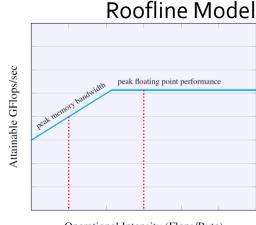
- 4. Schönauer Triad Benchmark Example
- 5. π Benchmark Example



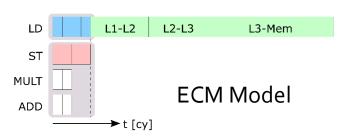


Performance Modeling For Loop Kernels

- How fast can my kernel run at best?
- What are the relevant hardware bottlenecks?
- Apply simplified model of underlying hardware
 - In-core execution
 - Data transfer
 - Putting execution and data transfer together



Operational Intensity (Flops/Byte)







Benefits

- Optimization within the kernel
- Guiding decisions for or against specific architecture
- Deeper understanding of code and hardware interaction





This Work

- Semi-automated machine instruction (throughput/latency) benchmarking
- Automated in-core runtime prediction for steady-state loops
- Open-Source Architecture Code Analyzer (OSACA) tool
- Case studies





OSACA – Workflow

User input

// TRIAD BENCHMARK

```
//STARTLOOP
for(int j=0; j<size; ++j){
    a[j] = b[j] + c[j]*d[j];
}
```

Throughput analysis

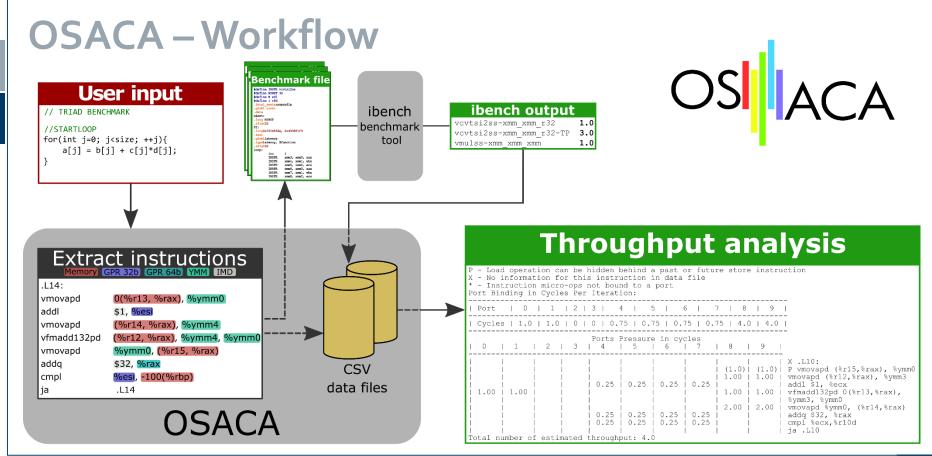
P - Load operation can be hidden behind a past or future store instruction

					Ports	Pressu	re	in cy	cres					
0	1		2	3	4	5		6	7	-	8	1	9	
	1				1	1			1			1		X .L10:
	ĺ	İ	ĺ		İ	İ	İ		ĺ	İ	(1.0)	Ĺ	(1.0)	P vmovapd (%r15,%rax), %ymm0
					1						1.00		1.00	vmovapd (%rl2,%rax), %ymm3
					0.25	0.25		0.25	0.25					addl \$1, %ecx
1.00) 1.0	0			1					- 1	1.00		1.00	vfmadd132pd 0(%r13,%rax),
					1									%ymm3, %ymm0
					1						2.00		2.00	vmovapd %ymm0, (%r14,%rax)
					0.25	0.25		0.25	0.25					addq \$32, %rax
					0.25	0.25	-	0.25	0.25	- 1				cmpl %ecx,%r10d
					1					- 1				ja .L10
otal	number	of	estima	ted	through	put: 4	.0							

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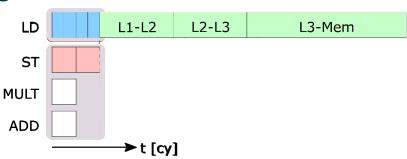
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Model Construction (I): Assumptions

- All Data in L1
- 2. Average distribution of port scheduling
- 3. Perfect out-of-order scheduling
- 4. Latencies hidden via speculative execution



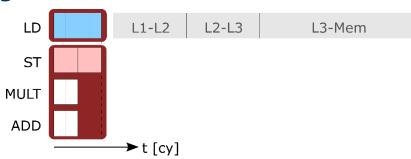
5. Runtime prediction == longest time any port is occupied





Model Construction (I): Assumptions

- All Data in L1
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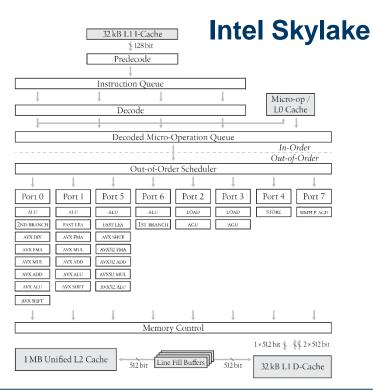


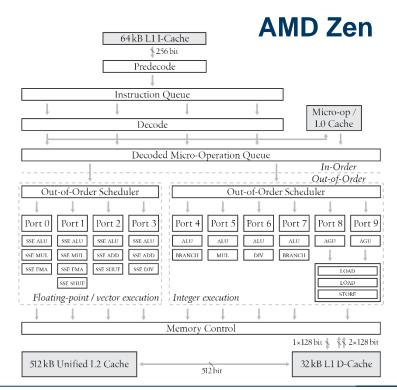
5. Runtime prediction == longest time any port is occupied





Model Construction (II): Port Models

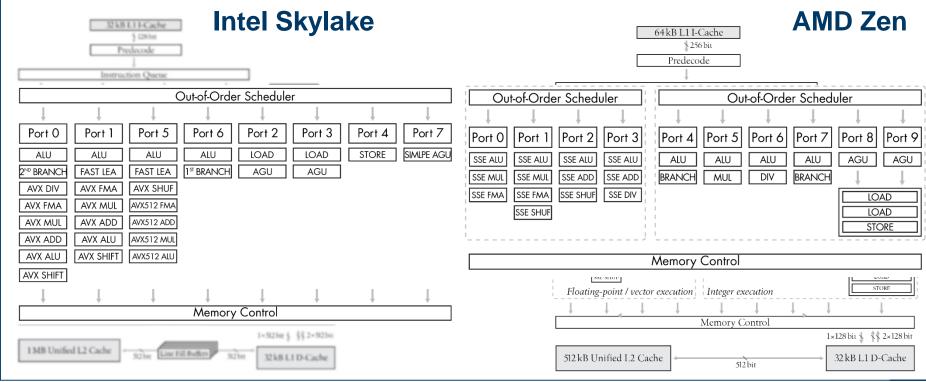






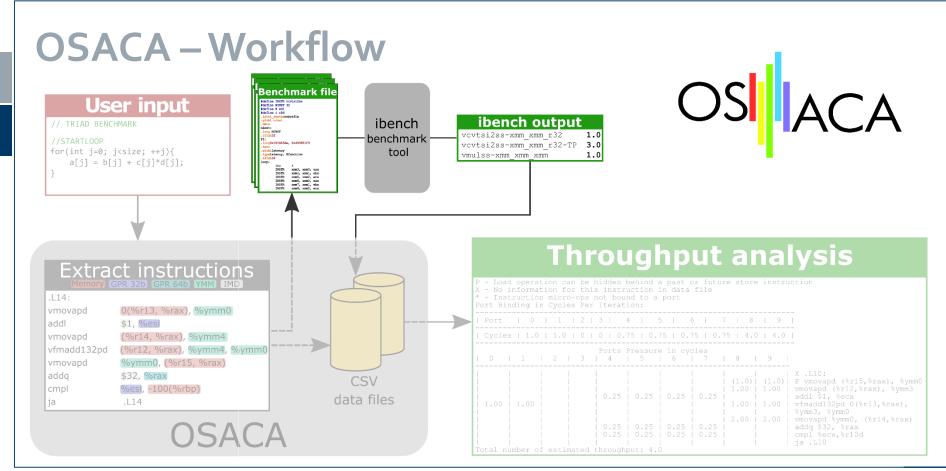


Model Construction (II): Port Models









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Model Construction (III): Microbenchmarks

Latency

```
loop:
  inc %eax
  vaddpd %xmm0, %xmm1, %xmm0
  vaddpd %xmm0, %xmm0, %xmm1
  vaddpd %xmm0, %xmm1, %xmm0
  ...
  vaddpd %xmm0, %xmm0, %xmm1
  cmp %eax, %edx #loop count
  jl loop
```

Throughput

```
loop:
   inc %eax
   vaddpd %xmm0, %xmm0, %xmm3
   vaddpd %xmm1, %xmm1, %xmm4
   vaddpd %xmm2, %xmm2, %xmm5
   vaddpd %xmm0, %xmm0, %xmm6
   vaddpd %xmm1, %xmm1, %xmm7
   vaddpd %xmm2, %xmm2, %xmm8
   vaddpd %xmm0, %xmm0, %xmm9
   ...
   cmp %eax, %edx #loop count
   jl loop
```





Model Construction (III): Microbenchmarks

Latency

```
loop:
  inc %eax
  vaddpd %xmm0, %xm1, %xmm0
  vaddpd %xmm0, %xmm1
  vaddpd %xmm0, %xmm1, %xmm0
  ...
  vaddxd %xmm0, %xmm0, %xmm1
  cmp %eax, %edx #loop count
  jl loop
```

Throughput

```
loop:
   inc %eax
   vaddpd %xmm0, %xmm0, %xmm3
   vaddpd %xmm1, %xmm1, %xmm4
   vaddpd %xmm2, %xmm2, %xmm5
   vaddpd %xmm0, %xmm0, %xmm6
   vaddpd %xmm1, %xmm1, %xmm7
   vaddpd %xmm2, %xmm2, %xmm8
   vaddpd %xmm0, %xmm0, %xmm9
   ...
   cmp %eax, %edx #loop count
   jl loop
```





Benchmark tool output

```
      Using frequency 1.80GHz.

      vaddpd-xmm_xmm_xmm-1:
      4.009

      vaddpd-xmm_xmm_xmm-2:
      2.006

      vaddpd-xmm_xmm_xmm-4:
      1.011

      vaddpd-xmm_xmm_xmm-5:
      0.805

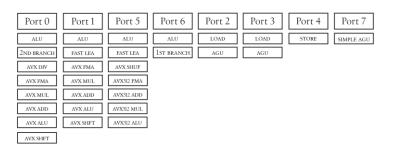
      vaddpd-xmm_xmm_xmm-8:
      0.556

      vaddpd-xmm_xmm_xmm-10:
      0.554

      vaddpd-xmm_xmm_xmm_xmm-12:
      0.551
```

database entry

```
vaddpd-xmm_xmm_xmm, 0.5, 4.0, \
"(0.5,0,0.5,0,0,0,0,0)"
```



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Benchmark tool output

```
      Using frequency 1.80GHz.

      vaddpd-xmm_xmm_xmm-1:
      4.009

      vaddpd-xmm_xmm_xmm-2:
      2.006

      vaddpd-xmm_xmm_xmm-4:
      1.011

      vaddpd-xmm_xmm_xmm-5:
      0.805

      vaddpd-xmm_xmm_xmm-8:
      0.556

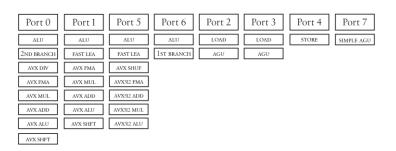
      vaddpd-xmm_xmm_xmm-10:
      0.554

      vaddpd-xmm_xmm_xmm-xmm-xmm-xmm-12:
      0.551
```

of independent instructions

database entry

```
vaddpd-xmm_xmm_xmm, 0.5, 4.0, \
"(0.5,0,0.5,0,0,0,0,0)"
```



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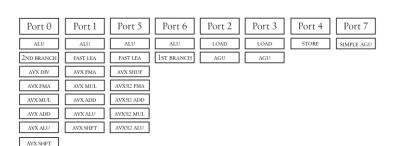
Benchmark tool output

of independent instructions

CPI

database entry

```
vaddpd-xmm_xmm_xmm, 0.5, 4.0, \
"(0.5,0,0.5,0,0,0,0,0)"
```



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Benchmark tool output

instructions

```
Using frequency 1.80GHz.
vaddpd-xmm xmm xmm-1:
                                 4.009
vaddpd-xmm xmm xmm-2:
                                 2,006
vaddpd-xmm xmm xmm-4:
                                 1.011
vaddpd-xmm xmm xmm-5:
                                 0.805
vaddpd-xmm xmm xmm-8:
                                 0.556
vaddpd-xmm_xmm_xmm-10:
                                 0.554
vaddpd-xmm_xmm_xmm-12:
                                 0.551
                                 CPI
         # of independent
```

database entry







Benchmark tool output

```
Using frequency 1.80GHz.
vaddpd-xmm xmm xmm-1:
                                 4.009
vaddpd-xmm xmm xmm-2:
                                 2,006
vaddpd-xmm xmm xmm-4:
                                 1.011
vaddpd-xmm xmm xmm-5:
                                 0.805
vaddpd-xmm xmm xmm-8:
                                 0.556
vaddpd-xmm_xmm_xmm-10:
                                 0.554
vaddpd-xmm_xmm_xmm-12:
                                 0.551
                                 CPI
```

of independent instructions

vaddpd-xmm xmm, 0.5, 4.0, \ "(0.5,0,0.5,0,0,0,0,0,0)" Port 0 Port 1 Port 5 Port 6 Port 2 Port 3 Port 4 Port 7 ALU ALU ALU ALU LOAD LOAD SIMPLE AGU 2ND BRANCE FAST LEA FAST LEA 1st branch AVX MUL AVX FMA AVX MUL AVX ADD AVX512 ADD

database entry

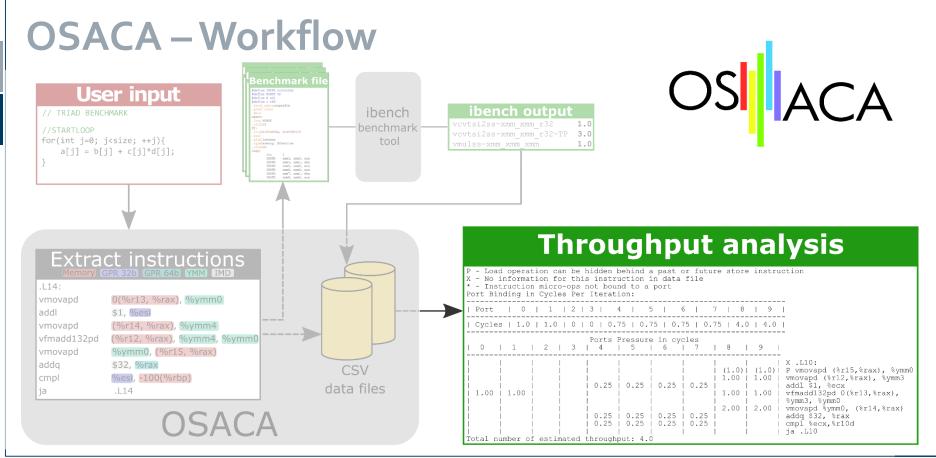
AVX SHFT

AVX SHFT

AVX512 ALU







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Schönauer Triad Benchmark Example

Load-bound

- Create code with -O1, -O2 and -O3 flag (+ architecture specific flags)
- Analyze for Intel Skylake & AMD Zen

```
for(int j=0; j<size; ++j)</pre>
           a[j] = b[j] + c[j]*d[j];
                       2x unrolling
.L10:
                 (%r13,%rax), %xmm0
  vmovaps
                 (%r15,%rax), %xmm3
  vmovaps
  incl
                 %esi
  vaddpd
                 (%r14,%rax), %xmm3, %xmm0
                 %xmm0, (%r12,%rax)
  vmovaps
  adda
                 $16, %rax
  cmpl
                 %esi, %r10d
  ja
                 .L10
```

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Insert marker for kernel detection

(done by tool or manually)

```
mov1
                $111, %ebx
                                       #START MARKER
  .byte
                100, 103, 144
                                       #START MARKER
.L10:
                (%r13,%rax), %xmm0
 vmovaps
                (%r15,%rax), %xmm3
 vmovaps
 incl
               %esi
 vaddpd
               (%r14,%rax), %xmm3, %xmm0
                %xmm0, (%r12,%rax)
 vmovaps
 addq
                $16, %rax
 cmpl
                %esi, %r10d
 jа
                .L10
 movl
                $222, %ebx
                                       #END MARKER
                100, 103, 144
  .byte
                                       #END MARKER
```





run on ZEN ZEN, \$ osaca --iaca --arch ZEN triad.s.zen.03.s Throughput Analysis Report P - Load operation can be hidden behind a past or future store instruction X - No information for this instruction in data file * - Instruction micro-ops not bound to a port Port Binding in Cycles Per Iteration: Port 3 -DV | Cycles | 1.25 | 1.25 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 2.0 | 2.0 | Ports Pressure in cycles DV X .L10: 0.25 0.25 0.25 0.25 (0.5) | (0.5) | P vmovaps 0(%r13,%rax), %xmm0 0.25 0.25 (%r15,%rax), %xmm3 0.25 0.25 0.50 0.50 vmovaps 0.25 0.25 0.25 0.25 incl %esi 0.50 0.50 0.50 0.50 vaddpd (%r14,%rax), %xmm3, %xmm0 0.25 0.25 0.25 0.25 1.00 1.00 vmovaps %xmm0, (%r12,%rax) \$16, %rax 0.25 0.25 0.25 0.25 addq %esi, %r10d 0.25 0.25 0.25 0.25 cmpl .L10 jа Total number of estimated throughput: 2.0





run on ZEN ZEN, \$ osaca --iaca --arch ZEN triad.s.zen.03.s Throughput Analysis Report P - Load operation can be hidden behind a past or future store instruction X - No information for this instruction in data file * - Instruction micro-ops not bound to a port Port Binding in Cycles Per Iteration: Port 3 -DV | Cycles | 1.25 | 1.25 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 2.0 | 2.0 | Ports Pressure in cycles DV X .L10: 0(%r13,%rax), %xmm0 0.25 0.25 0.25 0.25 (0.5)(0.5)P vmovaps 0.25 0.25 0.50 0.50 (%r15,%rax), %xmm3 0.25 0.25 vmovaps 0.25 0.25 0.25 0.25 incl %esi 0.50 0.50 0.50 0.50 vaddpd (%r14,%rax), %xmm3, %xmm0 0.25 0.25 0.25 0.25 1.00 1.00 vmovaps %xmm0, (%r12,%rax) \$16, %rax 0.25 0.25 0.25 0.25 addq 0.25 0.25 0.25 0.25 cmpl %esi, %r10d jа .L10

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Total number of estimated throughput: 2.0





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Results

Architecture executed on compiled for		Optimization flag	Unroll factor	MFLOP/s	Measured Mit/s	cy/it	Prediction OSACA	on [cy/it] IACA
Zen	Zen	-01	1x	1797	898	2.00	2.00	-
Zen	Zen	-02	1x	1797	898	2.00	2.00	-
Zen	Zen	-03	2x	3531	1754	1.02	2.00 / 2	-
Skylake	Zen	-01	1x	1770	885	2.03	2.00	2.24
Skylake	Zen	-02	1x	1768	884	2.04	2.00	2.00
Skylake	Zen	-03	2x	3505	1753	1.03	2.00/2	2.21
Zen	Skylake	-01	1x	1792	896	2.01	2.00	-
Zen	Skylake	-02	1x	1797	898	2.01	2.00	-
Zen	Skylake	-03	4x	3166	1589	1.01	4.00 / 4	-
Skylake	Skylake	-01	1x	1767	884	2.04	2.00	2.24
Skylake	Skylake	-02	1x	1776	888	2.03	2.00	2.00
Skylake	Skylake	-03	4x	6808	2738	0.53	2.00 / 4	2.21 / 4

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π Benchmark Example

Compute-bound

$$\pi = \int_0^1 \frac{4}{1+x^2} dx$$

```
int SLICES = 1000000000;
double sum = 0., delta_x = 1./SLICES;

for(int i=0; i<SLICES; ++i) {
    double x = (i+0.5)*delta_x;
    sum = sum + 4.0 / ( 1.0 + x * x);
}
double Pi = sum * delta_x;</pre>
```

8x unrolling

```
.L2:
 vextracti128 $0x1, %ymm2, %xmm0
 vcvtdq2pd
              %xmm2, %ymm1
 vaddpd
              %ymm7, %ymm1, %ymm1
 addl
              $1. %eax
 vcvtdq2pd
              %xmm0, %ymm0
 vaddpd
              %ymm7, %ymm0, %ymm0
              %ymm8, %ymm2, %ymm2
 vpaddd
 vmulpd
              %ymm6, %ymm1, %ymm1
 vmulpd
              %ymm6, %ymm0, %ymm0
 vaddpd
              %ymm1, %ymm5, %ymm1
              %ymm0, %ymm5, %ymm0
 vaddpd
 vdivpd
              %ymm1, %ymm4, %ymm1
 vdivpd
              %ymm0, %ymm4, %ymm0
              %ymm1, %ymm0, %ymm0
 vaddpd
 vaddpd
              %ymm0, %ymm3, %ymm3
 cmpl
              $125000000, %eax
 ine
               .L2
```

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\$ osacaiacaarch SKL pi.s.skl.03.s										
Port 0 - DV	1 2 3 4 5 6 7	run on SKYLAKE,								
		- On Corc.								
Cycles 8.83 16.0 4.	83 0 0 0 3.83 0.5 0	1 SKY, SKY,								
Ports P	ressure in cycles	-AKE LAKE								
0 - DV 1 2		7								
1.00		X .L2: vextracti128								
Total number of estimated t	hroughput: 16.0	Jiie								

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osacaia	caarch SKL p	i.s.skl.03.s				run on SKYLAKE
Port	0 - DV	1 2 3 4	4 5	6 7		run op led fo
Cycles 8	.83 16.0 4.	83 0 0 0	9 3.83	0.5 0		SKYISKYI
	Ports P	ressure in cyc	cles			AKELA
0 - DV			5	6 7	1	
	 		 	 I I	- X .L2:	
	i	i i	1.00	i		\$0x1, %ymm2, %xmm1
1.00	i i	i i	1.00	i i	vcvtdq2pd	%xmm2, %ymm0
0.50	0.50	i i	i	i i	vaddpd	%ymm7, %ymm0, %ymm0
0.25	0.25	i i	0.25	0.25	i addl	\$1, %eax
1.00	i i	i i	1.00	i i	vcvtdq2pd	%xmm1, %ymm1
0.50	0.50	i i	i	i i	vaddpd	%ymm7, %ymm1, %ymm1
0.33	0.33	i i	0.33	i i	vpaddd	%ymm8, %ymm2, %ymm2
0.50	0.50	i i	İ	i i	vmulpd	%ymm6, %ymm0, %ymm0
0.50	0.50	i i	Ì	İ	vmulpd	%ymm6, %ymm1, %ymm1
0.50	0.50				vaddpd	%ymm0, %ymm5, %ymm0
0.50	_ 0.50				vaddpd	%ymm1, %ymm5, %ymm1
1.00 8.00	9				vdivpd	%ymm0, %ymm4, %ymm0
1.00 8.00	9				vdivpd	%ymm1, %ymm4, %ymm1
0.50	0.50				vaddpd	%ymm1, %ymm0, %ymm0
0.50	0.50				vaddpd	%ymm0, %ymm3, %ymm3
0.25	0.25		0.25	0.25	cmpl	\$125000000, %eax
					jne	.L2





		pi.s.skl.03.s			, on the second			
Port 0	- DV	1 2 3 4	5		run on ed fo			
Cycles 8.83	3 16.0 4	.83 0 0 6	3.83	0.5 0		run on SKYLAKE		
,	Ports	Pressure in cyc	:les			AKE A		
0 - DV		3 4	5	6 7	1			
	 			 	 X .L2:			
	i	iii	1.00	i i	vextracti128	\$0x1, %ymm2, %xmm1		
1.00	i	i i	1.00	i i	vcvtdq2pd	%xmm2, %ymm0		
0.50	0.50	iii		i i	vaddpd	%ymm7, %ymm0, %ymm0		
0.25	0.25	i i	0.25	0.25	i addl	\$1, %eax		
1.00	i i	i i	1.00	i i	vcvtdq2pd	%xmm1, %ymm1		
0.50	0.50	i i	j	i i	vaddpd	%ymm7, %ymm1, %ymm1		
0.33	0.33	i i	0.33	i i	vpaddd	%ymm8, %ymm2, %ymm2		
0.50	0.50	i i	j	i i	vmulpd	%ymm6, %ymm0, %ymm0		
0.50	0.50	i i	İ	ĺĺ	vmulpd	%ymm6, %ymm1, %ymm1		
0.50	0.50	i i	İ	ĺ ĺ	vaddpd	%ymm0, %ymm5, %ymm0		
0.50	0.50				vaddpd	%ymm1, %ymm5, %ymm1		
1.00 8.00					vdivpd	%ymm0, %ymm4, %ymm0		
1.00 8.00					vdivpd	%ymm1, %ymm4, %ymm1		
0.50	0.50				vaddpd	%ymm1, %ymm0, %ymm0		
0.50	0.50				vaddpd	%ymm0, %ymm3, %ymm3		
0.25	0.25		0.25	0.25	cmpl	\$125000000, %eax		





Results

Architectur e			Measured Mit/s	cy/it	Prediction [cy/it] OSACA IACA	
Skylake	-01	1198	200	9.02	4.75	3.91
Skylake	-02	2697	450	4.00	4.25	4.00
Skylake	-03	5227	871	2.06	2.00	2.00
Zen	-01	1197	200	11.48	4.00	_
Zen	-02	2696	449	4.96	4.00	-
Zen	-03	5377	896	2.44	2.00	_





run on SKYLAKE, \$ osaca --iaca --arch SKL pi.s.skl.01.s Throughput Analysis Report Port Binding in Cycles Per Iteration: Port 0 - DV | | Cycles | 4.75 | 4.0 | 3.75 | 1.0 | 1.0 | 1.0 | 1.75 | 0.75 | 0 | Ports Pressure in cycles DV X .L2: 0.25 0.25 0.25 0.25 vxorpd %xmm0, %xmm0, %xmm0 0.50 1.00 %eax, %xmm0, %xmm0 0.50 vcvtsi2sd 0.50 0.50 vaddsd %xmm4, %xmm0, %xmm0 0.50 0.50 vmulsd %xmm3, %xmm0, %xmm0 0.50 0.50 vmulsd %xmm0, %xmm0, %xmm0 vaddsd 0.50 0.50 %xmm2, %xmm0, %xmm0 vdivsd %xmm0, %xmm1, %xmm0 1.00 4.00 0.50 0.50 0.50 0.50 vaddsd (%rsp), %xmm0, %xmm5 0.50 0.50 1.00 vmovsd %xmm5, (%rsp) 0.25 0.25 0.25 0.25 addl \$1, %eax 0.25 0.25 0.25 0.25 cmpl \$1000000000, %eax jne .L2 Total number of estimated throughput: 4.75





run on SKYLAKE, \$ osaca --iaca --arch SKL pi.s.skl.01.s Throughput Analysis Report Port Binding in Cycles Per Iteration: Port 0 - DV | | Cycles | 4.75 | 4.0 | 3.75 | 1.0 | 1.0 | 1.0 | 1.75 | 0.75 | 0 | Ports Pressure in cycles DV X .L2: 0.25 0.25 0.25 0.25 vxorpd %xmm0, %xmm0, %xmm0 0.50 1.00 %eax, %xmm0, %xmm0 0.50 vcvtsi2sd 0.50 0.50 vaddsd %xmm4, %xmm0, %xmm0 0.50 0.50 vmulsd %xmm3, %xmm0, %xmm0 vmulsd 0.50 0.50 %xmm0, %xmm0, %xmm0 vaddsd 0.50 0.50 %xmm2, %xmm0, %xmm0 vdivsd %xmm0, %xmm1, %xmm0 1.00 4.00 0.50 0.50 0.50 0.50 vaddsd (%rsp), %xmm0, %xmm5 0.50 0.50 %xmm5, (%rsp) 1.00 vmovsd 0.25 0.25 0.25 0.25 addl \$1, %eax 0.25 0.25 0.25 0.25 cmpl \$1000000000, %eax jne .L2 Total number of estimated throughput: 4.75





Future Work

- Latency modelling
- Critical Path
- Loop-carried dependencies
- Differentiate addressing modes
- Architecture specific heuristics
- Integration in KERNCRAFT
- Replacement / Additional instrumentalization of benchmark tools



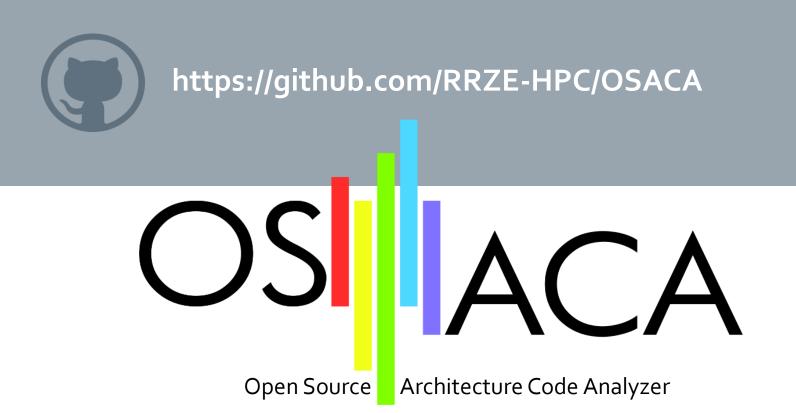


IACA — Intel Architecture Code Analyzer Why something new?

- OSACA is Open Source
- OSACA supports non-Intel architectures
- OSACA is based on benchmarks of individual instructions
- OSACA allows manual extension of the supported instruction set
- OSACA allows architectural exploration











Thank You for Your Attention!



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