Plak1a Development Board
User Guide

2009

Pedro Sampaio

INTRODUCTION

Plak1a is a starter kit which uses MCU LPC2294 from NXP. This powerful MCU supports various serial interfaces such as UART, SPI, I2C, etc. In addition on this board also accelerometer, JTAG throw a USB connector, Ethernet, touchscreen TFT display and SDCARD connector. All this along with the ARM7TDMI-S™ architecture allow you to build a diversity of powerful applications to be used in a wide range of situations.

BOARD FEATURES

MCU: LPC2294
LCD 3.2'' 320x240 18-bit color TFT with backlight and touchscreen
3-axis digital accelerometer with 11-bit accuracy
4 MB SRAM
4 MB NOR FLASH
100Mbit Ethernet
RS232 throw a USB connector

SD/MMC card connector
JTAG support throw a USB connector
2 buttons
1 joystick (five positions)
1 expansion port
Audio in/out
Bluetooth
4x4 Keypad
Dimensions: 146x102mm

ELECTROSTATIC WARNING

The Plak1a board must not be subject to high electrostatic potentials.
General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Cables: You will need different cables depending on the used programming or debugging tool.
You will need USB A-B cable for connect the debugger and can use OpenOCD to do the debug.

PROCESSOR FEATURES

Plak1a board use MCU LPC2294 from NXP with these features:
ARM7TDMI-S processor, running at up to 60 MHz. 256 KBytes on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities.
Flash program memory is on the ARM local bus for high performance CPU access.
16 KBytes on-chip SRAM.
Includes EMC provides support for asynchronous static memory devices such as RAM, ROM and flash.
Advanced Vectored Interrupt Controller (VIC), supporting up to 32 vectored interrupts.

Serial Interfaces

2 UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
CAN controller with two channels.
SPI controller.
SSP controller, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port.
I2C-bus interface (one with open-drain and two with standard port pins).

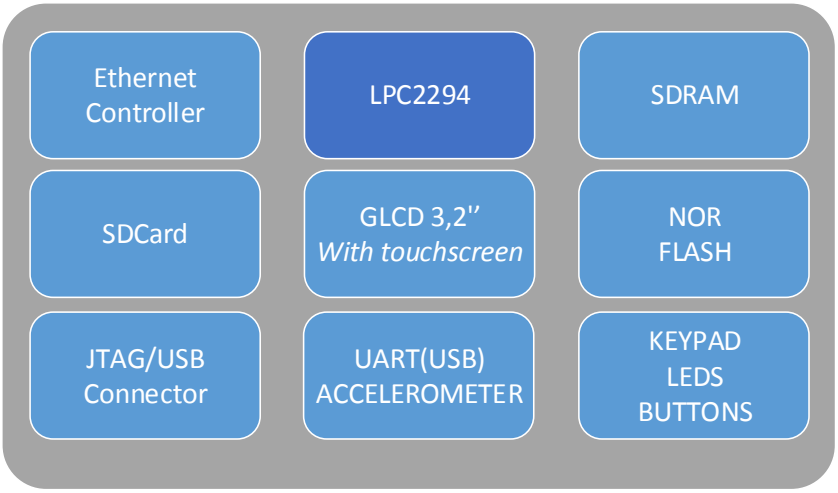
Other peripherals

160 General purpose I/O pins with configurable pull-up/down resistors.
10-bit ADC with input multiplexing among 8 pins.
10-bit DAC.
Four general purpose timers/counters with 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
PWM/timer blocks with support for three-phase motor control. Each PWM has an external count inputs.
Real-Time Clock (RTC)
WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
Up to 12 edge or level sensitive external interrupt pins available.
Two power saving modes, Idle mode and Power-down mode.
Peripheral clock scaling and individual enable/disable of peripheral functions for additional power optimization.
Processor wake-up from Power-down mode via external interrupt or CAN controllers.

Dual power supply

CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 8.3 %).
I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.
Four external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, port 0/2 pin interrupt).
Two independent power needed features.
Each peripheral has its own clock divider for further power saving.
These dividers help reduce active power by 20 % to 30 %.
On-chip power-on reset.
60 MHz maximum CPU clock available from programmable on-chip PLL with a possible input frequency of 10 MHz to 25 MHz and a settling time of 100 ms.
On-chip integrated oscillator operates with an external crystal in the range from
1 MHz to 25 MHz and with an external oscillator up to 50 MHz.
Boundary scan for simplified board testing.
Versatile pin function selections allow more possibilities for using on-chip peripheral functions.
Standard ARM test/debug interface for compatibility with existing tools.
Emulation trace module supports real-time trace.

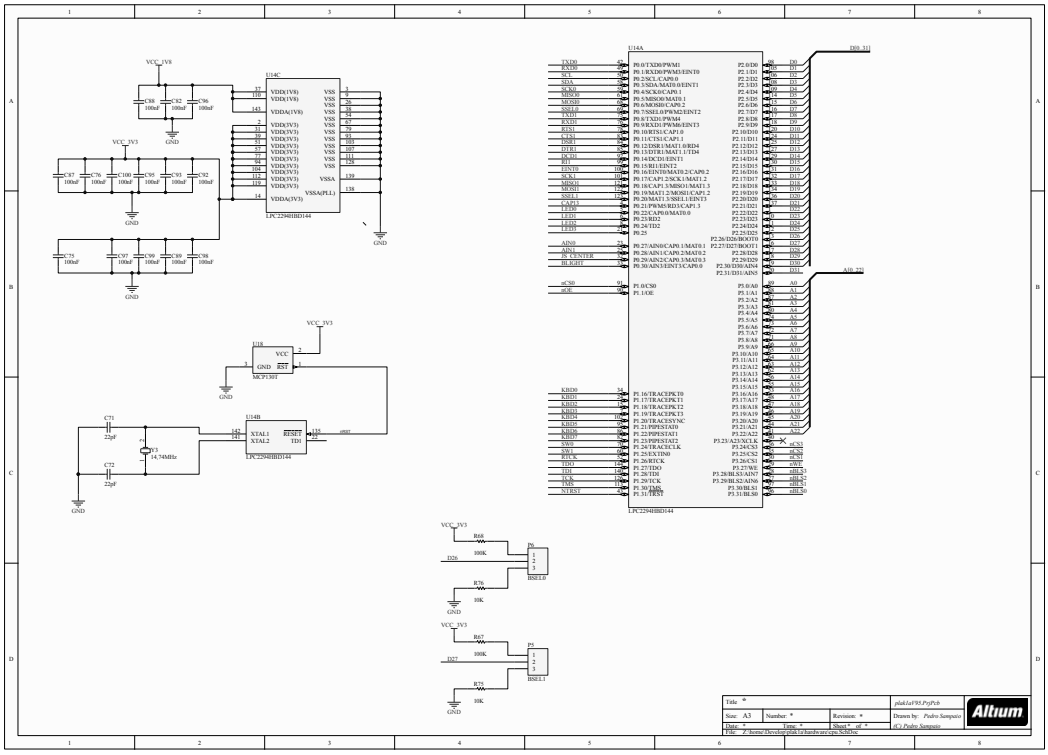
BLOCK DIAGRAM

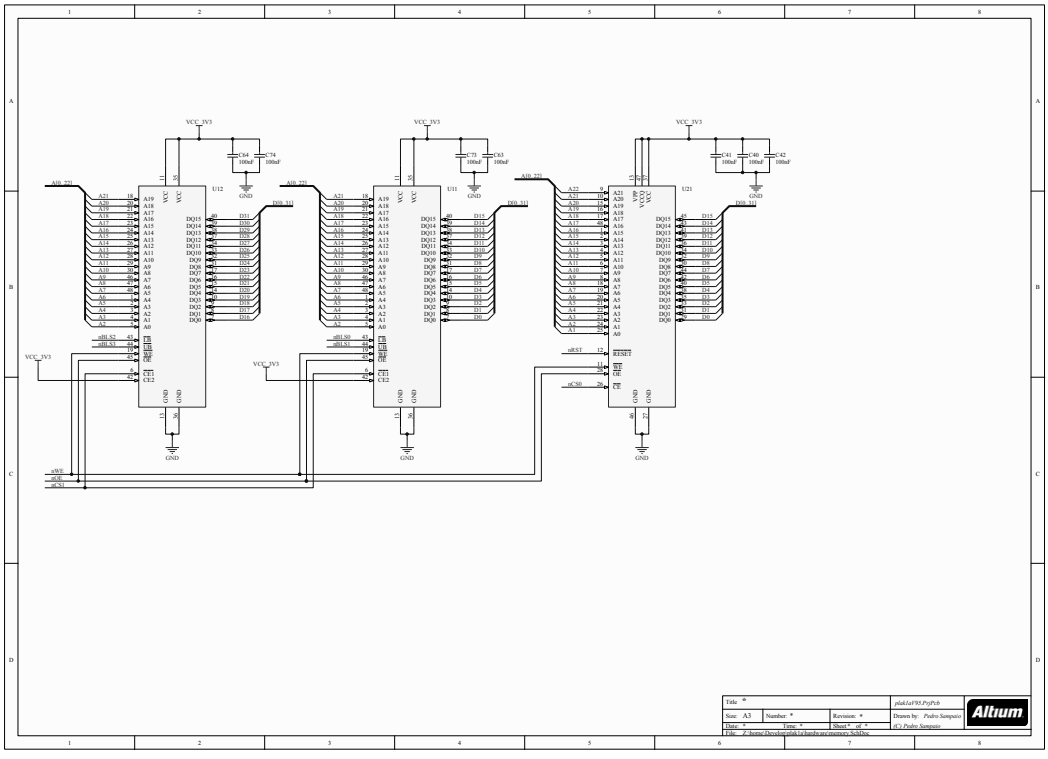


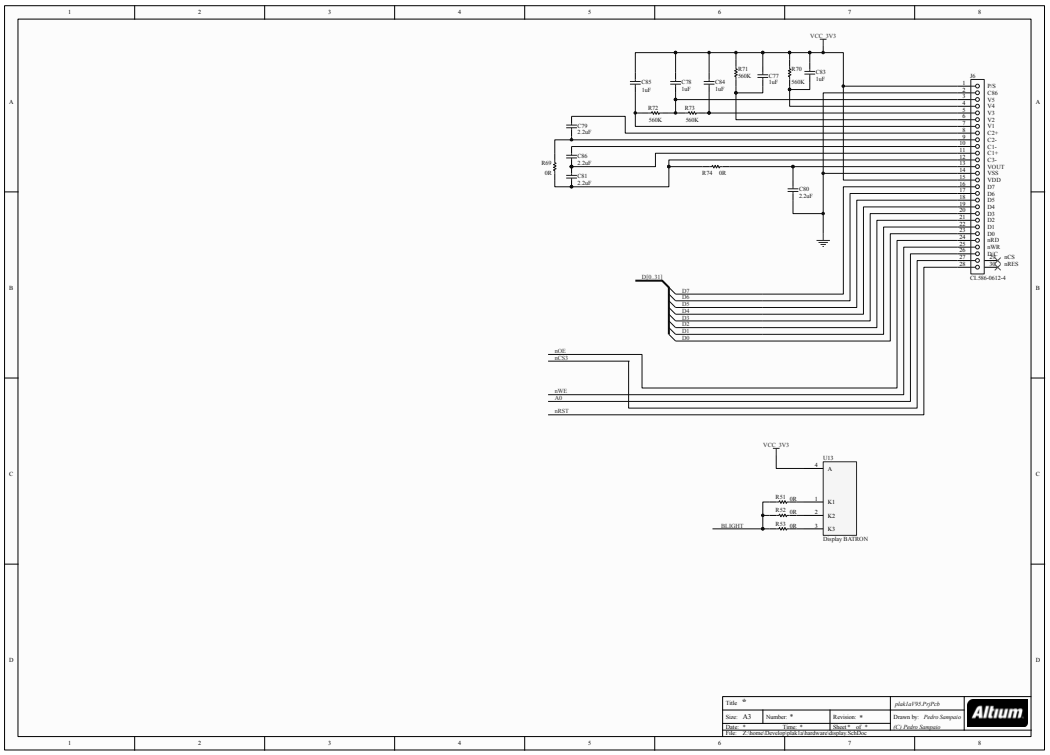
MEMORY MAP

	Address Range	Size
Internal Flash	0x00000000 – 0x0003FFFF	256 KBytes
Internal SRAM	0x40000000 – 0x40002FFF	16 Kbytes
External FLASH	0x80000000 – 0x803FFFFF	4 MBytes
External SRAM	0x81000000 – 0x813FFFFF	4 Mbytes
Lan Controller	0x82000000 – 0x820000FF	
GLCD	0x83000000 – 0x8303FFFF	

SCHEMATIC






VCC_3V3
C85 1uF
C78 1uF
C84 1uF
R71 560K
C77 1uF
C70 560K
C83 1uF
R72 560K
R73 560K
C79 2.2uF
C86 2.2uF
C81 2.2uF
R69 0R
R74 0R
C80 2.2uF
J6
P/S
C86
V5
V4
V3
V2
V1
C2+
C2-
C1-
C1+
C3-
VOUT
VSS
VDD
D7
D6
D5
D4
D3
D2
D1
D0
nRD
nWR
nCS
nRES
CT-586-0612-4
D[0..11]
D7
D6
D5
D4
D3
D2
D1
D0
nOE
nLCS3
nWE
A0
nRST
VCC_3V3
U13
A
K1
K2
K3
R31 0R
R32 0R
R33 0R
BL/GHT
Display BATRON
Title *
pdaUar93LPrjPcb
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Number: *
Revision: *
Drawn by: Pedro Sampaio
Date: *
Time: *
Sheet * of *
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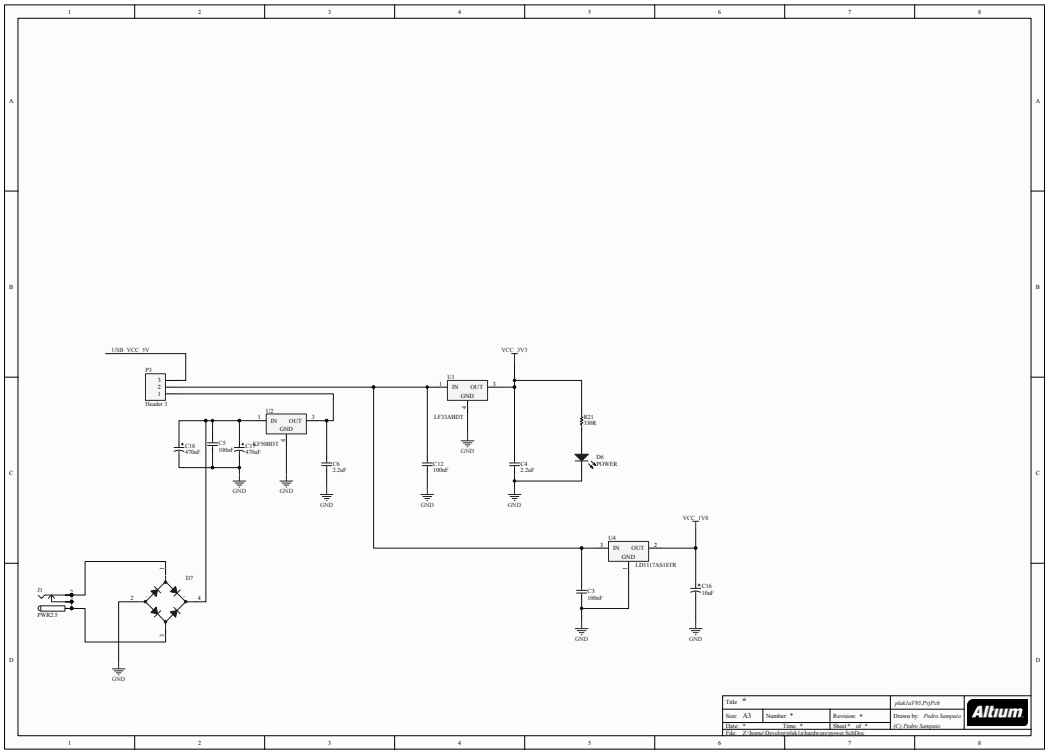
Altium


USB_VCC_5V
P3
Header 3
U2
IN
OUT
GND
LF50BDT
C18 470uF
C5 100nF
C19 470uF
C6 2.2uF
U1
LF33ABDT
C12 100nF
C4 2.2uF
VCC_3V3
R21 330R
D6
PWER
U4
LD1117AS18TR
C3 100nF
VCC_1V8
C16 10uF
J1
PWR2.5
D7
GND
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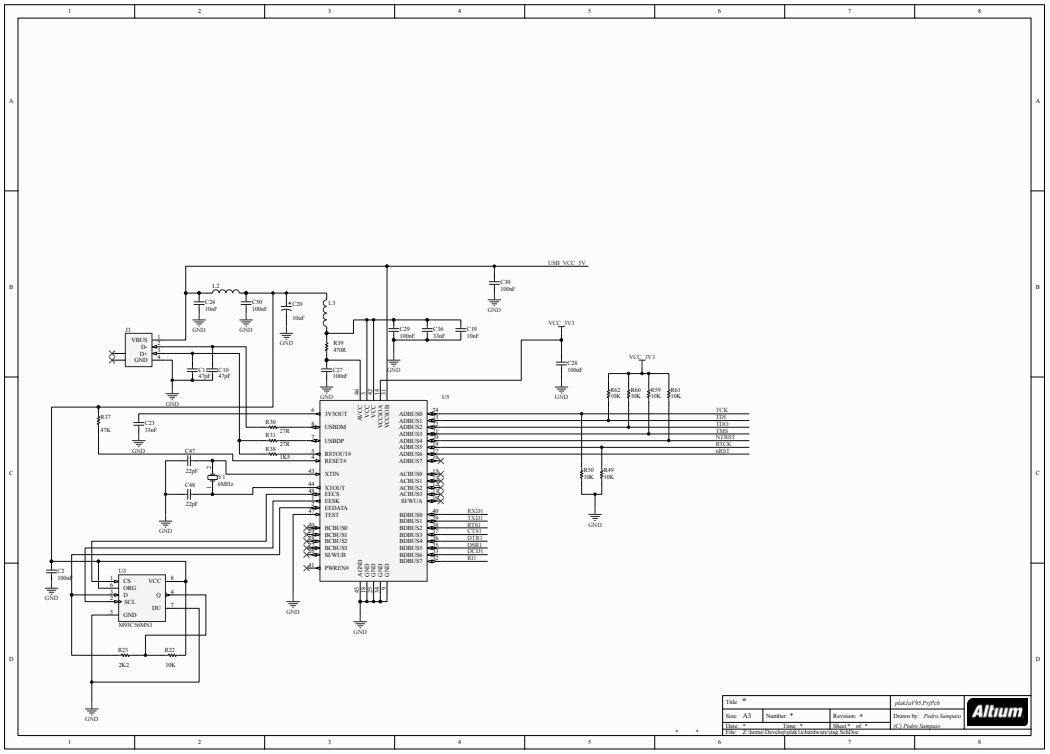
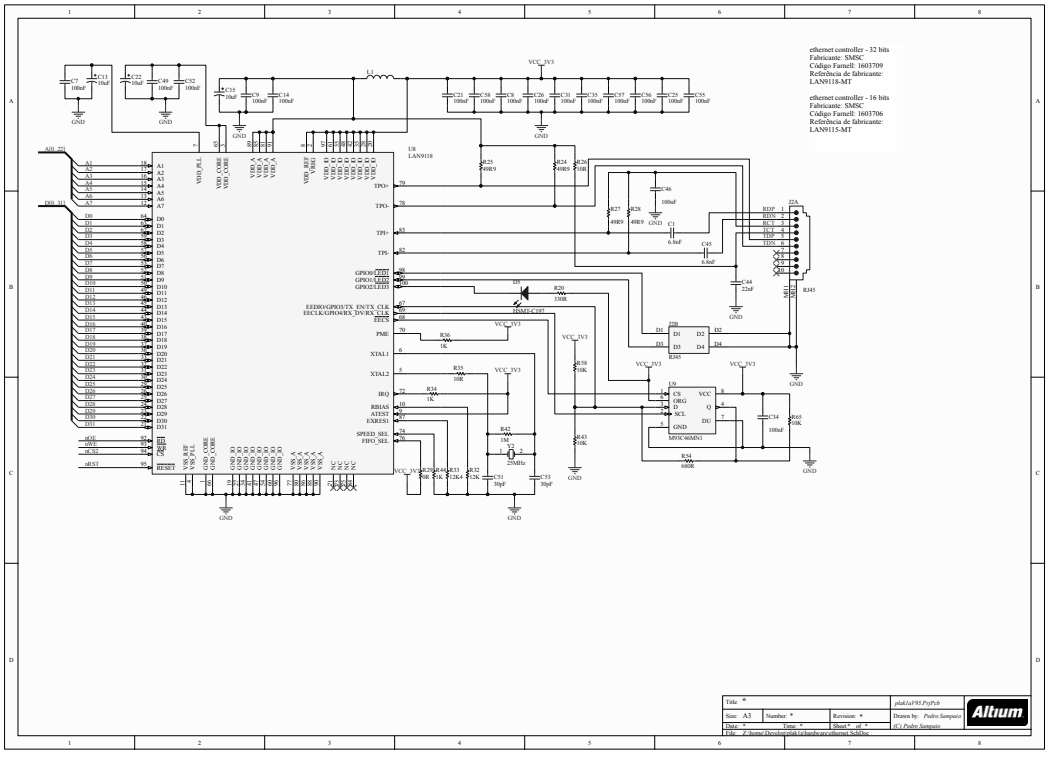
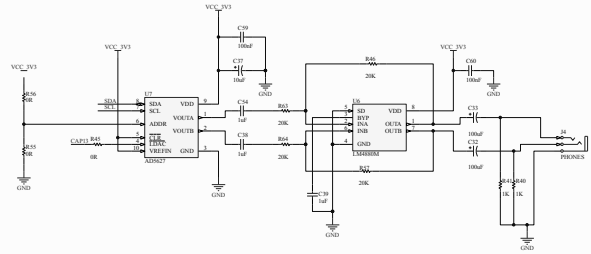

USB_VCC_5V
VCC_3V3
U5
U3
M93C56MN1
JV3OUT
USBDM
USBDP
RSTOUT#
RESET#
XTIN
XTOUT
EECS
EESK
EEDATA
TEST
BCBUS0
BCBUS1
BCBUS2
BCBUS3
SLWUB
PWREN#
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
SLWLA
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
TCK
TDI
TDO
TMS
NTRST
RTCK
nRST
RXD1
TXD1
RTS1
CTS1
DTR1
DSR1
DCD1
RI1
GND


ethernet controller - 32 bits
Fabricante: SMSC
Código Farnell: 1603709
Referência de fabricante: LAN9118-MT
ethernet controller - 16 bits
Fabricante: SMSC
Código Farnell: 1603706
Referência de fabricante: LAN9115-MT
U8
LAN9118
M93C46MN1
RJ45
GND
VCC_3V3



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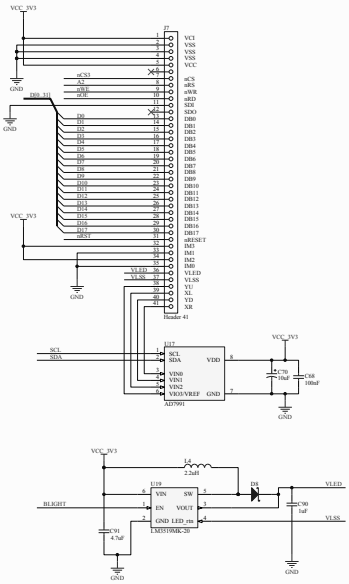

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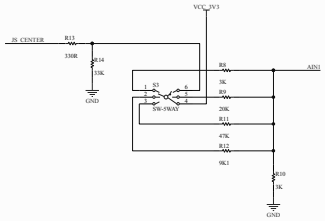
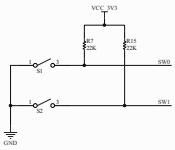
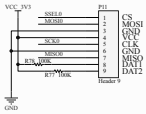
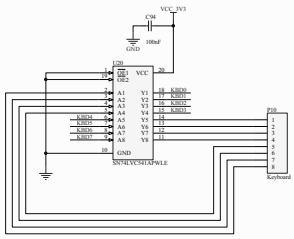

VCC_3V3
JS_CENTER
R13
330R
R14
33K
GND
S3
5WAY
R8
3K
AIN1
R9
20K
R11
47K
R12
9K1
R10
3K
GND


VCC_3V3
R7
22K
R15
22K
S1
SW0
S2
SW1
GND


VCC_3V3
SSEL0
MOSI0
SCK0
SSN0
MISO0
R76
10K
R77 100K
P11
CS
MOSI
GND
VCC
CLK
GND
MISO
DAT1
DAT2
Header 9
GND



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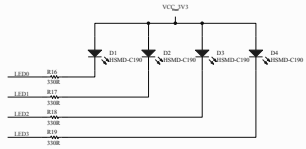

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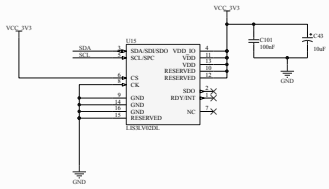
VCC_3V3
SDA
SCL
U15
SDA/SDI/SDO
SCL/SPC
CS
C
GND
GND
RESERVED
SDO
RDY/INT
NC
LSM303DLHC
VDD_IO
VDD
VDD
RESERVED
RESERVED
C101
100nF
C43
10uF
GND

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Revision *
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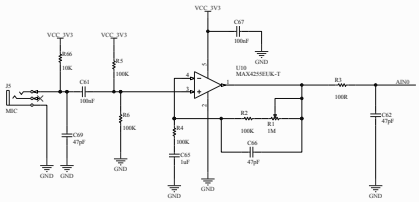
VCC_3V3
VCC_3V3
VCC_3V3
R66
10K
R65
100K
C67
100nF
GND
U10
MAX4255EUK-T
J5
MIC
C61
100nF
R6
100K
C69
47pF
GND
GND
GND
R64
100K
C65
1uF
GND
GND
R2
100K
R1
1M
C66
47pF
R3
100R
C62
47pF
GND
AIN0

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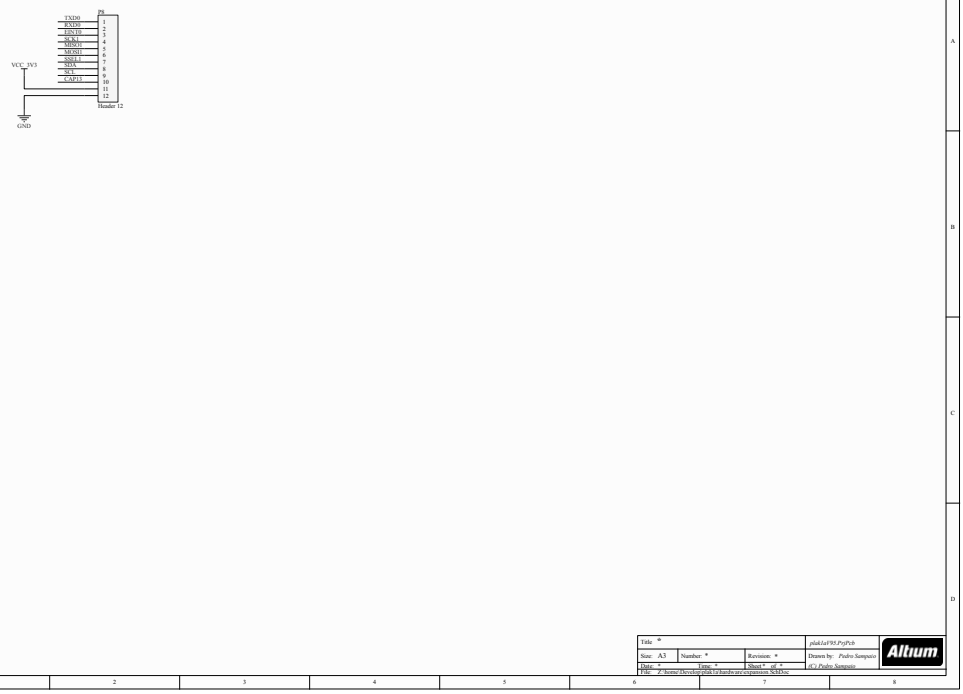
P8
TXD0
RXD0
EINT0
SCK1
MISO1
MOSI1
SSEL1
SDA
SCL
CAP1.1
1
2
3
4
5
6
7
8
9
10
11
12
Header 12
VCC_3V3
GND
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pdaiUart95LPxpVx0
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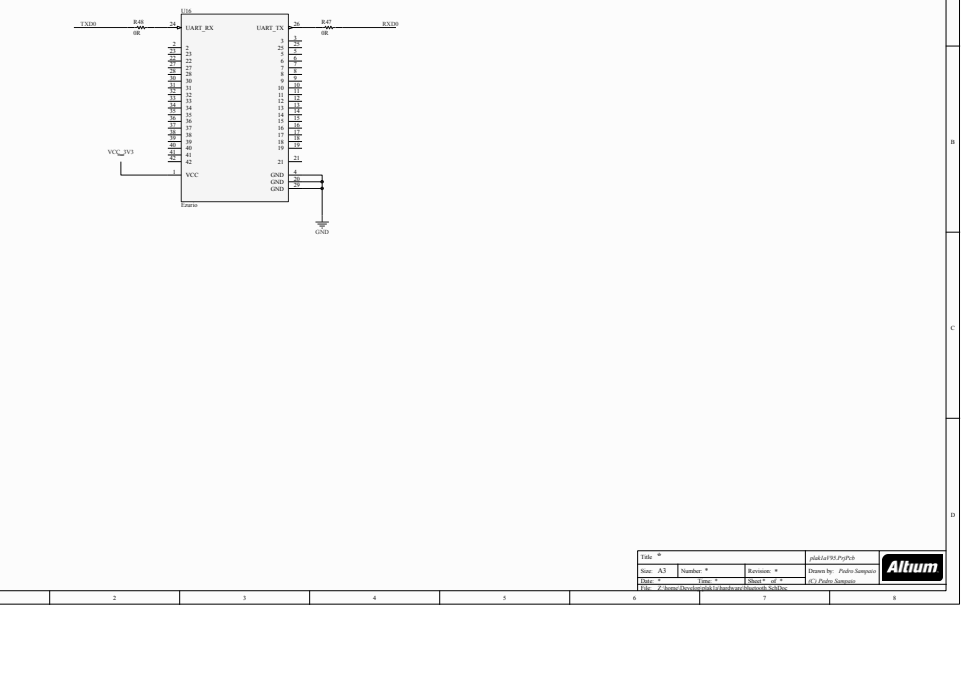
IFC | Pedro Sampaio
Altium


U16
TXD0
R48
0R
UART_RX
UART_TX
R47
0R
RXD0
VCC_3V3
VCC
GND
GND
GND
Exario
Title *
pdaiUart95LPxpVx0
Size: A3
Number: *
Revision: *
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Sheet * of *
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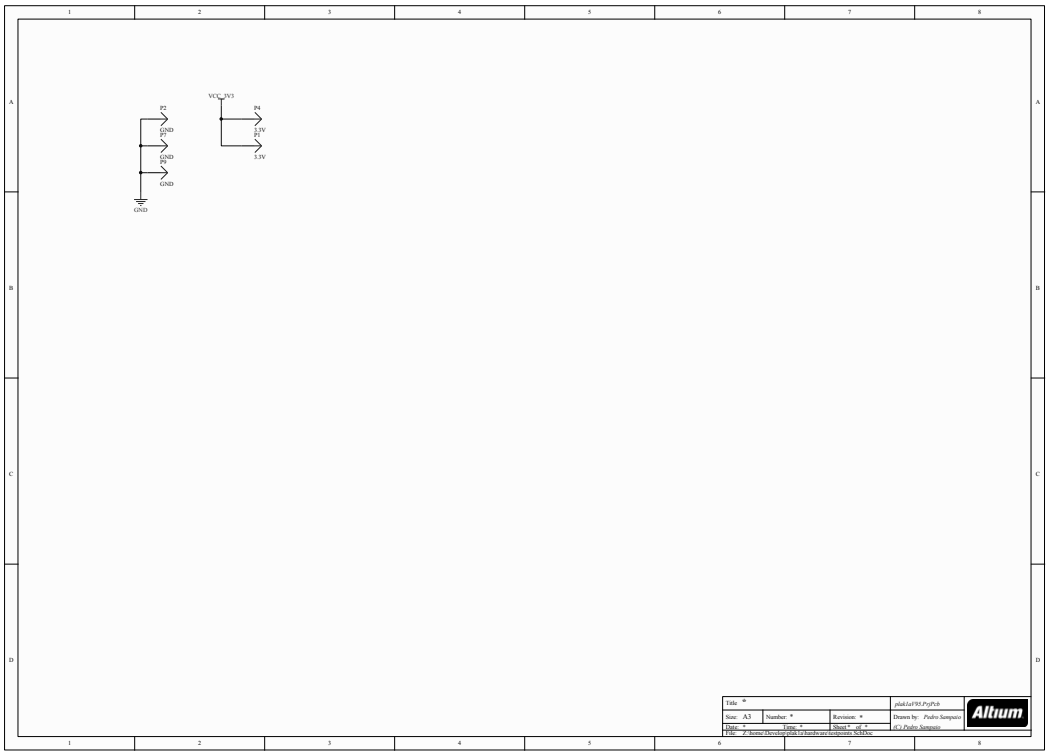
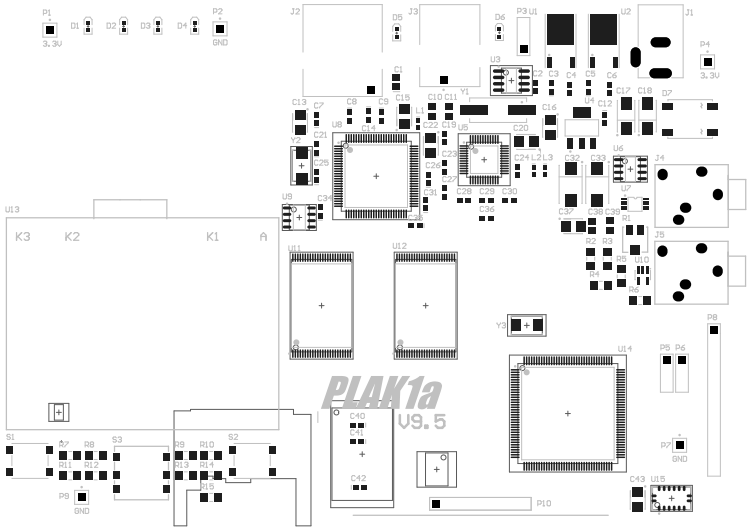
IFC | Pedro Sampaio
Altium

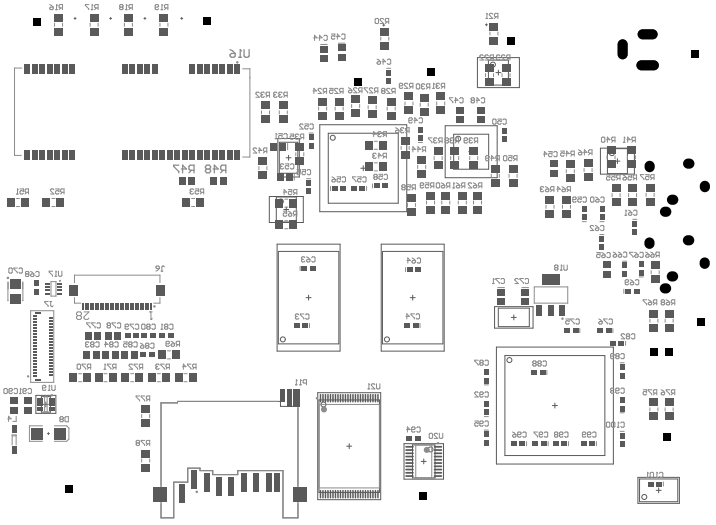

P2
GND
GND
P3
GND
GND
VCC_3V3
P4
3.3V
3.3V

BOARD LAYOUT

Front



Back



POWER SUPPLY CIRCUIT

Plak1a is powered by +9 to 12VDC/6VAC applied at the power jack.
Plak1a could also be powered by USB.
The consumption of Plak1a varies depending on the supplied power but at +10VDC it is about 250mA.

RESET CIRCUIT

Plak1a reset circuit is made MCP130D from Microchip.

CLOCK CIRCUIT

Quartz crystal 14, 7456 MHz is connected to LPC2294 pin XTAL1 and pin XTAL2.

JUMPER DESCRIPTION

Jumper P5 connected to BOOT0 and P6 connected to the BOOT1 do the LPC2294 allow to choose the boot configuration

BOOT1	BOOT0	Function
1-2	1-2	
1-2	2-3	
2-3	1-2	Selects 16 bit memory on CS0
2-3	2-3	Selects 8 bit memory on CS0

INPUT/OUTPUT

Power-on LED (red) – this LED shows that +3.3V is applied to the board.
User button with name S1 connected to LPC2294 pin P1[24]/TRACECLK.
User button with name S2 connected to LPC2294 pin P1[25]/EXTIN0.
User led with name D1 connected to LPC2294 pin P1[24]/TRACECLK.
User led with name D2 connected to LPC2294 pin P1[24]/TRACECLK.
User led with name D3 connected to LPC2294 pin P1[24]/TRACECLK.
User led with name D4 connected to LPC2294 pin P1[24]/TRACECLK.
TFT touchscreen display – 3.2'', 320x200, 18-bit color.

AUDIO IN

Connector J5

Pin 1 GND
Pin 2 MIC - Input Microphone Input. This pin is input to the MAX4255 amp-op.
Pin 3 NC

AUDIO OUT

Connector J4

Pin 1- GND
Pin 2 - LEFT - Output channel B. This pin is output for the LM4880 amplifier.
Pin 3 - RIGHT - Output channel A. This pin is output for the LM4880 amplifier.

EXPANSION

Connector P8

Pin 1 - TXD0
Pin 2 RXD0
Pin 3 EINT0
Pin 4 SCLK1
Pin 5 MISO1
Pin 6 MOSI1
Pin 7 SSEL1
Pin 8 SDA
Pin 9 SCL
Pin 10 CAP13
Pin 11 3V3
Pin 12 GND

LAN

Using the High Performance Single-Chip 10/100 Non-PCI Ethernet Controller LAN9118 and the connector J2.

LED Usage
Yellow – Activity
Green – 100MBits/s (Half/Full duplex)

TPO- Output Differential signal. This signal is output from the LAN9118.
TPO+ Output Differential signal. This signal is output from the LAN9118.
TPI- Input Differential signal. This signal is input for the LAN9118.
TPI+ Input Differential signal. This signal is input for the LAN9118.

SDCARD

SDCARD interface is implemented with SPI0
Connector P11

Pin 1 CS SSEL0

Pin 2 MOSI MOSI0
Pin 3 GND
Pin 4 VDD
Pin 5 CLK SCK0
Pin 6 GND
Pin 7 MISO MISO0
Pin 8 VDD
Pin 9 VDD

KEYPAD

Keypad 4x4
In connector P10