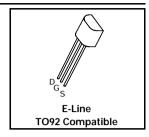
P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP2110A

ISSUE 2 - MARCH 94

FEATURES

- * 100 Volt V_{DS}
- * $R_{DS(on)} = 8\Omega$



ABSOLUTE MAXIMUM RATINGS.

SYMBOL	VALUE	UNIT
V _{DS}	-100	V
I _D	-230	mA
I _{DM}	-3	Α
V_{GS}	± 20	V
P _{tot}	700	mW
T _j :T _{stg}	-55 to +150	°C
	V _{DS} I _D I _{DM} V _{GS}	V _{DS} -100 I _D -230 I _{DM} -3 V _{GS} ± 20 P _{tot} 700

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

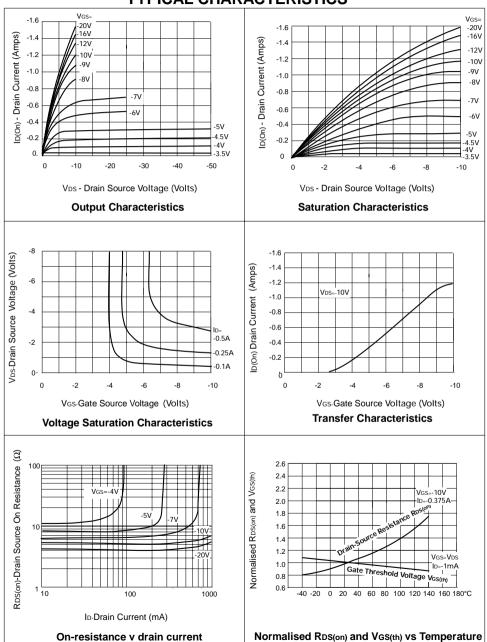
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.	
Drain-Source Breakdown Voltage	BV_DSS	-100		V	I _D =-1mA, V _{GS} =0V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	ID=-1mA, V _{DS} = V _{GS}	
Gate-Body Leakage	I _{GSS}		20	nA	V _{GS} =± 20V, V _{DS} =0V	
Zero Gate Voltage Drain Current	I _{DSS}		-1 -100	μ Α μ Α	V _{DS} =-100 V, V _{GS} =0 V _{DS} =-80 V, V _{GS} =0V, T=125°C(2)	
On-State Drain Current(1)	I _{D(on)}	-750		mA	V _{DS} =-25 V, V _{GS} =-10V	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}		8	Ω	V _{GS} =-10V,I _D =-375mA	
Forward Transconductance (1)(2)	g _{fs}	125		mS	V _{DS} =-25V,I _D =-375mA	
Input Capacitance (2)	C _{iss}		100	pF	V _{DS} =-25V, V _{GS} =0V, f=1MHz	
Common Source Output Capacitance (2)	C _{oss}		35	pF		
Reverse Transfer Capacitance (2)	C _{rss}		10	pF		
Turn-On Delay Time (2)(3)	t _{d(on)}		7	ns	V _{DD} ≈-25V, I _D =-375mA	
Rise Time (2)(3)	t _r		15	ns		
Turn-Off Delay Time (2)(3)	t _{d(off)}		12	ns		
Fall Time (2)(3)	t _f		15	ns		

⁽¹⁾ Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%

⁽²⁾ Sample test.

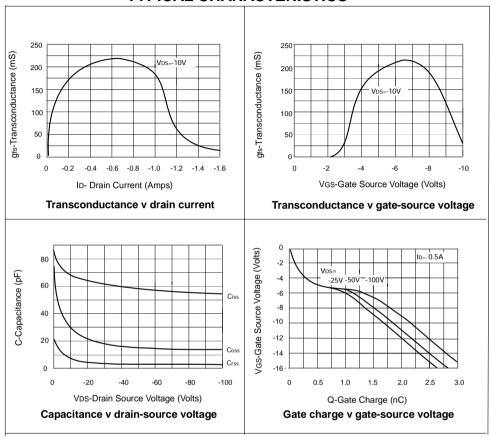
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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS



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