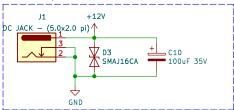
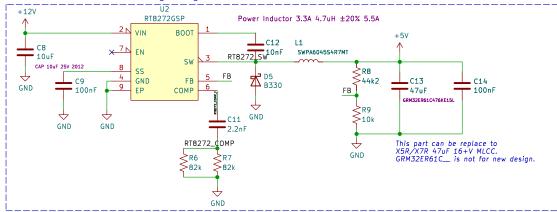


# Power Domain

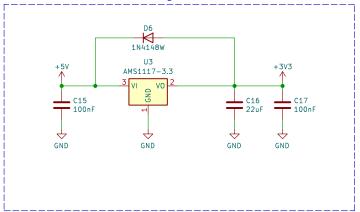
### 12V Input Jack



## 12V to 5V : Switching Regulator



### 5V to 3V3 : Linear Regulator





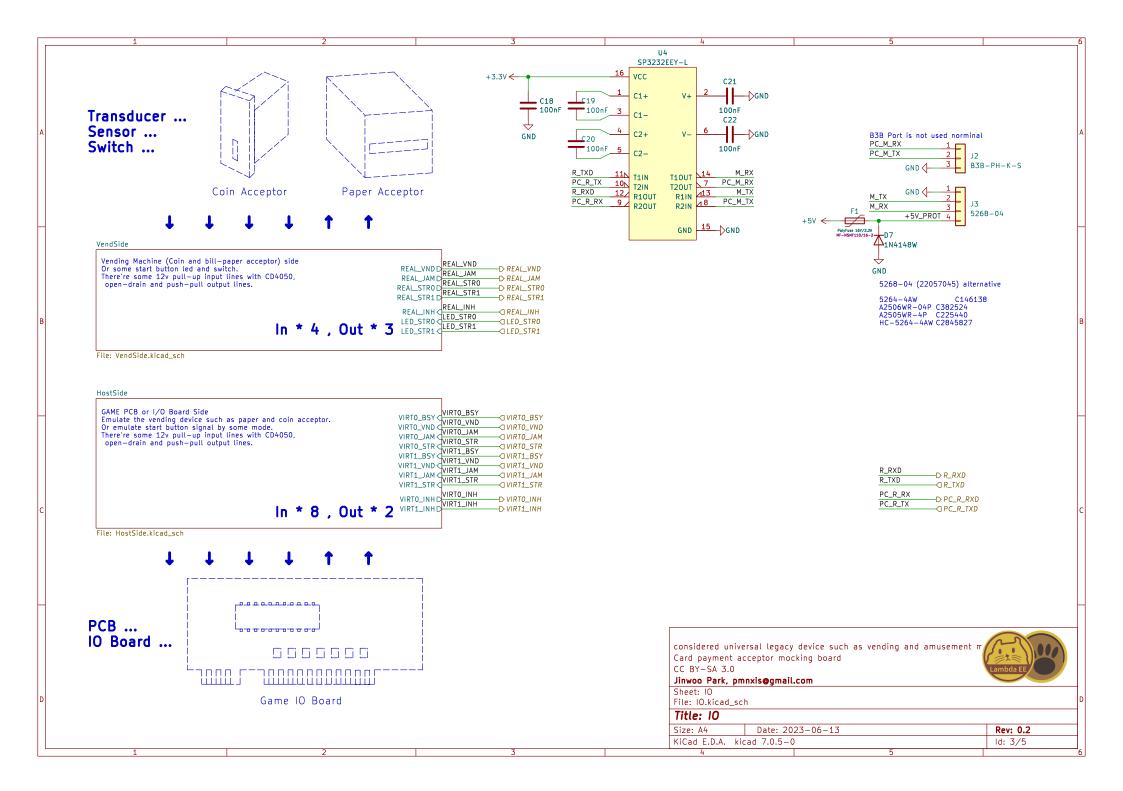
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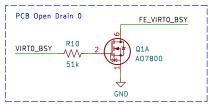
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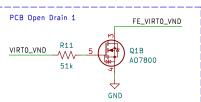
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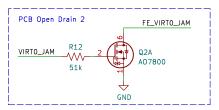
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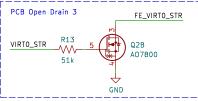


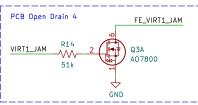


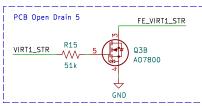










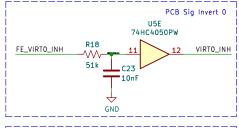


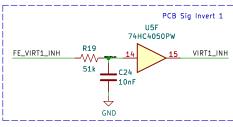
# CHANGE LOG

Formal arcade system use Game PCB have pull up line on input, and this domain make drop to OV very safely, even each pin's voltage level is different.

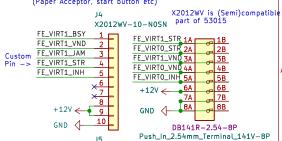
ULN2003AIDR has some issue COM line is shared. so we didn't used for seperate voltage level. Q4:7 was changed to PMV100ENEA from IRFL014PBF. Because IRFL014PBF was obsoleted JLCPCB type. JLCPCB Assembly service don't have stock or option for PMV100. DMN100 and PESD\_ is alternation for this assembly system. 2020-07-20 : DMN100 or PMV100 NMOS reduce to dual channel NMOS. Recommend is DMN3190LDW and Alternative is DMN2004DWK Requirements : high desity, high current , Volt accept. Gate, D-S Protection. 2023-05-18: 2022-05-16:
Dual-N: A07800, Used for open-drain output
Dual-P: DMP2004VK, Used for inverse voltage input protect.
N+P CH: DMG1016V, N/P role both

### PCB Side extSignal Invert Input





#### Emulated player 1/2 side common signal (Paper Acceptor, start button etc)



X2012WV-10-N0SN FE\_VIRTO\_BSY FE\_VIRTO\_VND 2 FE\_VIRTO\_JAM Custom FE\_VIRTO\_STR FE\_VIRTO\_INH

VIRTO_BSY VIRTO_VND VIRTO_JAM VIRTO_STR VIRT1_BSY VIRT1_VND VIRT1_JAM VIRT1_STR	Q VIRTO_BSY Q VIRTO_VND Q VIRTO_JAM Q VIRTO_STR Q VIRT1_BSY Q VIRT1_VND Q VIRT1_JAM Q VIRT1_JAM
VIRTO_INH VIRT1_INH	D VIRTO_INH

D VIRT1\_INH

J6

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Sheet: HostSide File: HostSide.kicad sch

Title: Host Side
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/,		F.	

PCB Open Drain 7 FE\_VIRT1\_BSY R17 VIRT1\_BSY Q4B A07800 51k GND

GND

FE\_VIRT1\_VND

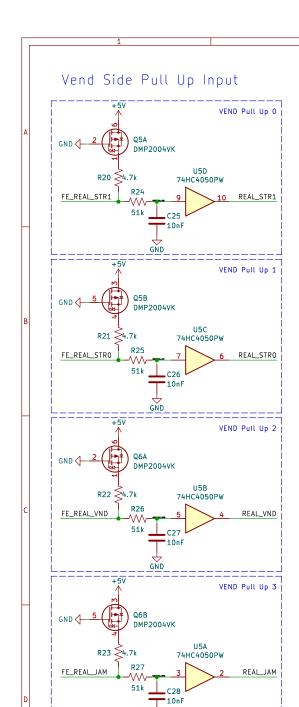
A07800

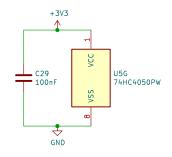
PCB Open Drain 6

VIRT1\_VND

R16

51k





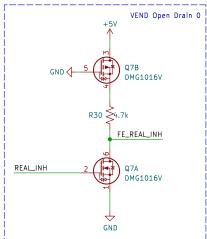
### CHANGE LOG

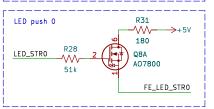
2020-07-16: LTV217 Optocopuler is removed. Replaced to high voltage input hex inverter. TI CD4049UBDR recommend 1uA input. TI require too few input current. So this design use "ONSemi MC414049UBDR26", "NSV HEF4049BT"

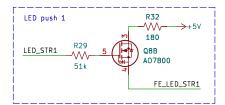
2020-07-20: DMM100 or PMV100 NMOS reduce to dual channel NMOS. DMN3190LDW or DMN2004DWK Recommend is DMN3190LDW , Alternative is DMN2004DWK Requirements: high desity, high current and voltage accept. Gate,D-S Protection.

2023-05-18:
Dual-N: AO7800, Used for open-drain output
Dual-P: DMP2004VK, Used for inverse voltage input protect.
N+P CH: DMG1016V, N/P role both

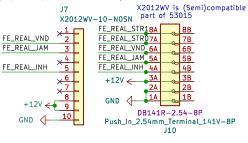
### Vend Side Push Pull Active Low



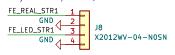




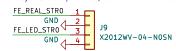
## Player 1/2 side common signal (Paper Acceptor, start button etc)



Player 2 side purchase/start button and led

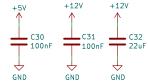


Player 1 side purchase/start button and led



REAL_VND	—D REAL_VND
REAL_JAM	
REAL_STR0	- REAL_SAM
REAL_STR1	D REAL_STRU
REAL_INH	— REAL INH
LED_STR0	LED STRO
LED_STR1	— TIED_SIRU

**Rev: 0.2** Id: 5/5



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Sheet: VendSide File: VendSide.kicad\_sch

Title: Vend	1 Side	
Size: A4	Date: 2023-06-13	
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