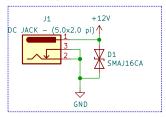
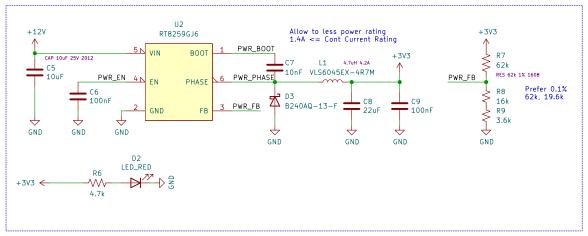


Power Domain

12V Input Jack



12V to 3V3 : Switching Regulator



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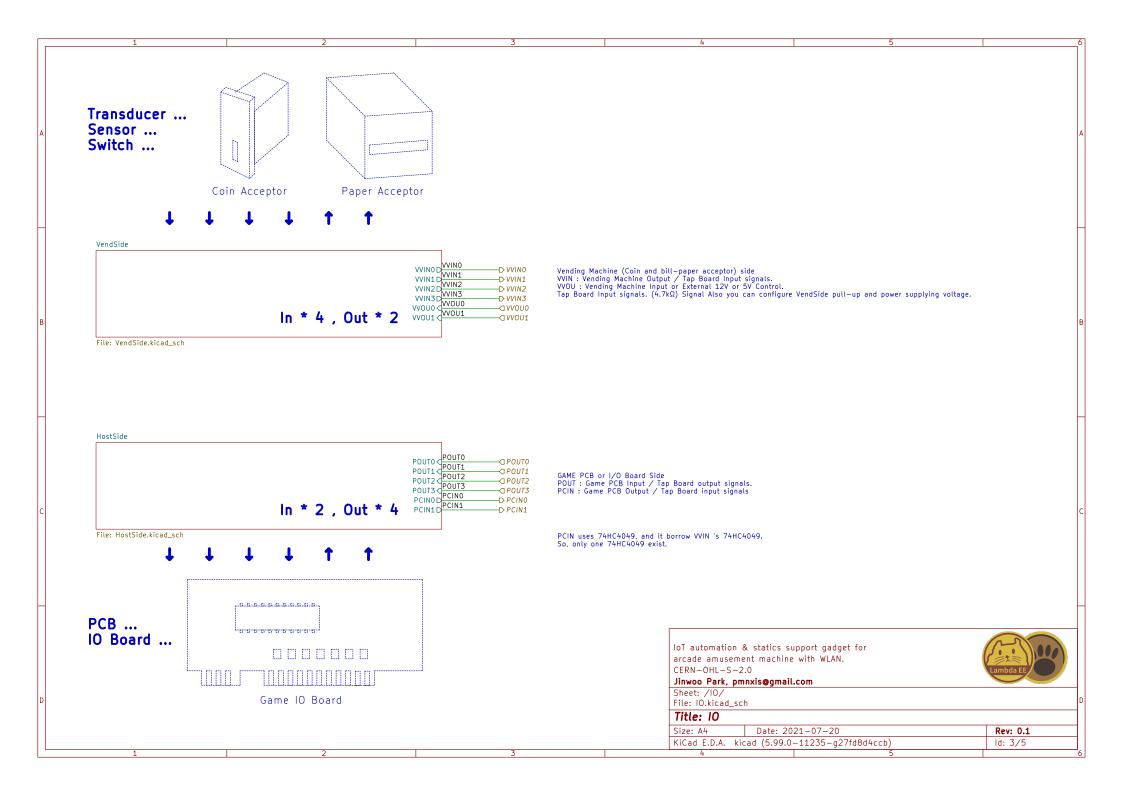


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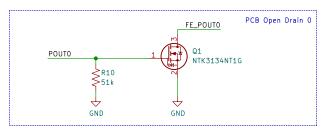
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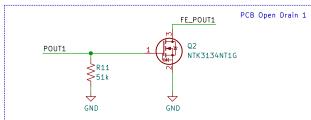
Size: A4	Date: 2021-07-20	Rev: 0.1	
KiCad E.D.A.	kicad (5.99.0-11235-g27fd8d4ccb)	ld: 2/5	

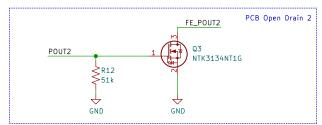
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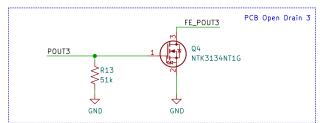


PCB Side Open Drain Output









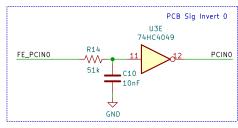
CHANGE LOG

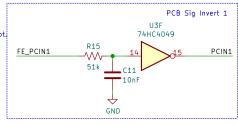
Formal arcade system use Game PCB have pull up line on input. and this domain make drop to OV very safely, even each pin's voltage level is different.

ULN2003AIDR has some issue COM line is shared, so we didn't used for seperate voltage level. Q4:7 was changed to PMY100ENEA from IRFL014PBF. Because IRFL014PBF was obsoleted JLCPCB type. JLCPCB Assembly service don't have stock or option for PMV100. DMN100 and PESD_ is alternation for this assembly system.

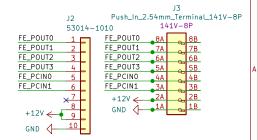
2020-07-20: DMN100 or PMV100 NMOS reduce to dual channel NMOS. Recommend is DMN3190LDW and Alternative is DMN2004DWK Requirements: high desity, high current , Volt accept. Gate,D-S Protection.

PCB Side extSignal Invert Input









POUT0	——⊲ P0UT0
POUT1	POUT1
POUT2	—— (1 POUT2
POUT3	——(1 POUT3
PCIN0	D PCINO
PCIN1	D PCINO

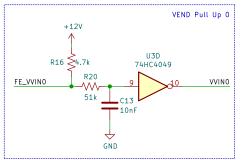
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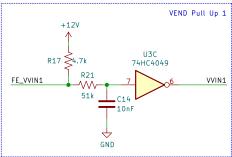
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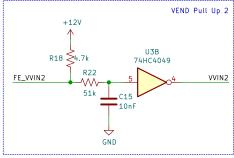
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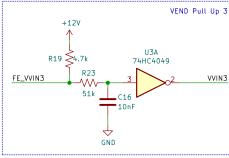
Size: A4	Date: 20	21-07-20	Rev: 0.1	
KiCad E.D.A.	kicad (5.99.0	-11235-g27fd8d4ccb)	ld: 4/5	

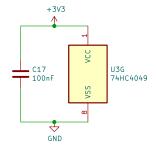
Vend Side Pull Up Input









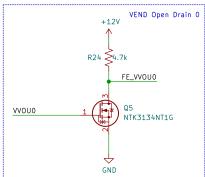


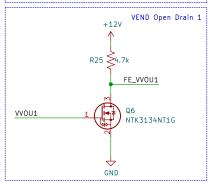
CHANGE LOG

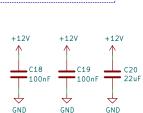
2020-07-16: LTV217 Optocopuler is removed. Replaced to high voltage input hex inverter. Ti CD4049UBDR recommend 1uA input. Ti require too few input current. So this design use "ONSemi MC14049UBDR2G" , "Nxp HEF4049BT"

2020-07-20: DMN100 or PMV100 NMOS reduce to dual channel NMOS. DMN3190LDW or DMN2004DWK Recommend is DMN3190LDW . Alternative is DMN2004DWK Requirements: high desity, high current and voltage accept. Gate, D-S Protection.

Vend Side Pull Up Input







J4	J5			
	Push_In_2.54r	nm_Terminal_141V-8P		
		141V-8P		
FE_VVINO 1	FE_VVINO 1	1B		
FE_VVIN1 2	FE_VVIN1 2	2B		
FE_VVIN2 3	FE_VVIN2 3/	3B		
FE_VVIN3 4	FE_VVIN3 4,	4B		
FE_VVOU0 5	FE_VVOU0 5	A 5B		
FE_VVOU1 6	FE_VVOU1 6			
<u>7</u>	+12V - 7 /	A 7B		
^8_	GND (8/	A 8B		
+12V ← 9	OND (<u> </u>		
GND (10				
GIAD (

VVIN0	D VVINO
VVIN1	D VVINC
VVIN2	D VVIN2
VVIN3	D VVINZ
VVOU0	
VVOU1	\\VV0U

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Sheet: /IO/VendSide/ File: VendSide.kicad_sch

	Title:	Vend	Side
- 1			

Size: A4	Date: 2021-07-20	Rev: 0.1
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