GENERAL INSTRUMENT

SP0264

PRELIMINARY INFORMATION

Narrator™ Speech Processor

FEATURES

- Natural speech
- Standalone operation with inexpensive support components
- Wide operating voltage
- Word, phrase, or sentence library, ROM expandable
- Expandable to 448K of ROM directly
- Simple interface to most microcomputers or microprocessors
- Supports L.P.C. Synthesis; Formant Synthesis; and Allophone Synthesis
- 28 pin dual in line package
- Available in -40°C to +85°C version, SP0264I

GENERAL DESCRIPTION

The SP0264 Speech Processor (SP) is a single chip N-Channel MOS LSI device that uses its stored program to synthesize speech or complex sounds.

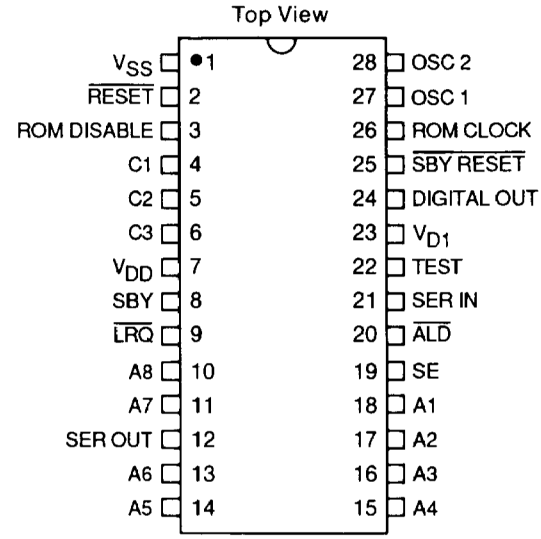
The achievable output is equivalent to a flat frequency response ranging from 0 to 5KHz, a dynamic range of 42dB, and a signal-to-noise ratio of approximately 35dB.

The SP0264 incorporates four basic functions:

- A software programmable digital filter that can be made to model a VOCAL TRACT.
- A 64K ROM that stores both data and instructions (THE PROGRAM).
- A MICROCONTROLLER that controls the data flow from the ROM to the digital filter, the assembly of the "word strings" necessary for linking speech elements; and the amplitude and pitch information to excite the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output that is converted to an analog signal when filtered by an external low-pass filter.

PIN CONFIGURATION

Top View



APPLICATIONS

- Telecommunications
- Appliances
- Computer peripherals
- Automotive
- Personal computers
- Toys/Games
- Educational aids
- Warning systems
- Security systems
- Electronic musical instruments
- Aids to the blind
- Narrow bandwidth
- Communication systems

34 Res Only

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OPERATION DESCRIPTION

The addressing of the SP0264 is controlled by the address pins (A1-A8), Address load ($\overline{ALD}$), and Strobe Enable (SE). Speech data for the SP0264 can be stored within the internal 64K ROM and/or an external serial speech ROM.

There are two modes available for loading an address into the chip. Strobe Enable (SE) controls which mode will be used.

Mode 0 (SE = 0). The speech processor will latch an address when any one (or more) address pin makes a low-to-high transition. All address lines must be returned to the low state prior to entering a new address. (NOTE: Address zero (0000 0000) is not a valid address in this mode of operation.) In order to best utilize this mode of operation, a vocabulary should consist of no more than eight individual words or phrases such that single address line transitions can be made. These words or phrases must be stored using the following entry point address: 1, 2, 4, 8, 16, 32, 64 and 128.

NOTE: There is a 2-byte overhead penalty paid for each dummy entry point between the entry points actually used.

Mode 1 (SE = 1). The SP0264 will latch an address using the $\overline{ALD}$ pin. The desired address is set up on the address bus (A1-A8) and then $\overline{ALD}$ is pulsed low. Any address can be loaded using this mode, but certain set up and hold times are required (refer to the timing diagrams for the specific times).

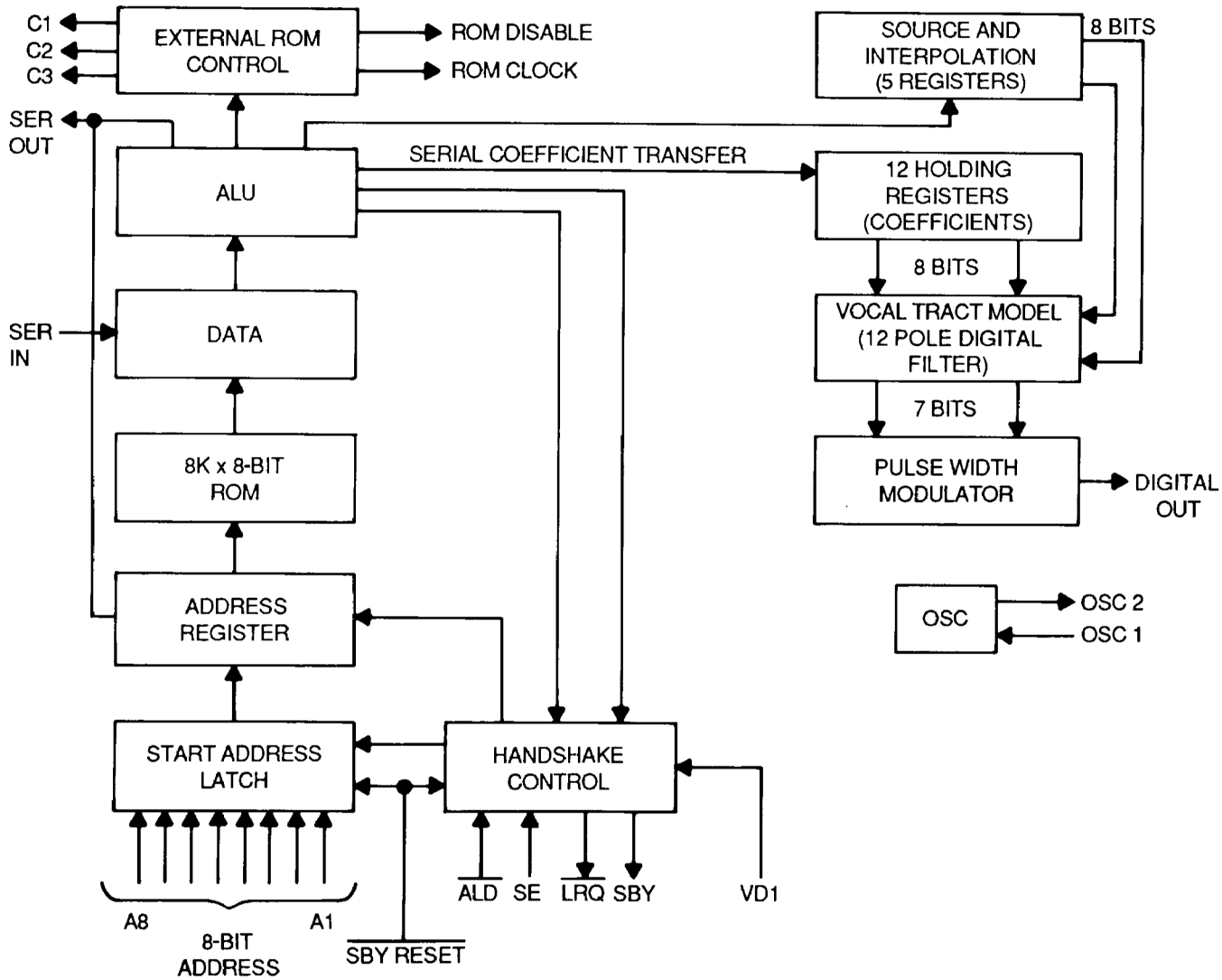
Two microprocessor interface pins are available for loading of addresses using mode 1. They are LRQ and SBY. Load Request ($\overline{LRQ}$) tells the processor when the address input buffer is full. Standby (SBY) tells the processor that the chip has stopped talking and no new address has been loaded.

When $\overline{LRQ}$ is low, a new address can be loaded onto the address bus. Strobing $\overline{ALD}$ will cause the new address to be loaded and $\overline{LRQ}$ to go high. $\overline{LRQ}$ will return low when the address buffer is available to accept a new address. The SP0264 is capable of latching one new address while speaking the last utterance (word or phrase). The time between address load requests is variable, depending on the length of the utterance currently being spoken.

Standby (SBY) goes low when an address is loaded and will stay low until all internal instructions have been completed (i.e., the speech chip stops talking). If a second address has been loaded before the chip stops speaking the first utterance, SBY will stay low through the completion of the second utterance (ad infinitum).

The SP0264 may be partially powered down when SBY is high to conserve battery life, provided VD1 remains powered. During power down and power up, reset should be held low to ensure the proper reset condition. While the speech processor is in the partial power down state, the handshake control signals ($\overline{ALD}$, SE, $\overline{LRQ}$, and SBY) and the address bus are active. However, the SP0264 will not output the addressed speech data until after V_{DD} is reapplied.

BLOCK DIAGRAM



PIN FUNCTIONS

PIN NUMBER	NAME	FUNCTION
1 (power supply)	V_{SS}	Ground
2 (input)	$\overline{\text{RESET}}$	A logic 0 resets the speech processor. Must be returned to a logic 1 for normal operation. Upon reset C1, C2, C3, and SER OUT go to "0", and $\overline{\text{SBY}}$ goes to "1."
3 (input)	ROM DISABLE	For use with an external serial speech ROM. A logic 1 disables the external ROM.
4,5,6 (outputs)	C1,C2,C3	Control lines for use with an external serial speech ROM.
7 (power supply)	V_{DD}	
8 (output)	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9 (output)	$\overline{\text{LRQ}}$	$\overline{\text{LOAD REQUEST}}$. LRQ is a logic 1 output whenever the input buffer is full. When LRQ goes to a logic 0, the input port is loaded by placing the 8 address bits on A1-A8 and pulsing the ALD input.
10,11,13,14 15,16,17,18 (inputs)	A8,A7,A6,A5 A4,A3,A2,A1	8-bit address that defines any one of 256 speech entry points.
12 (output)	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM. When $\overline{\text{SBY}}$ $\overline{\text{RESET}}$ and $\overline{\text{RESET}}$ go to "0", SER OUT goes to "0". When $\overline{\text{SBY}}$ $\overline{\text{RESET}}$ goes to "0" SER OUT goes to "0".
19 (input)	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, ALD is disabled and the SP will automatically latch in the address on the input bus approximately 1 us after detecting a logic 1 on any address line.
20 (input)	$\overline{\text{ALD}}$	$\overline{\text{ADDRESS LOAD}}$. A negative pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21 (input)	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22 (input)	TEST	A logic 1 places the SP in its test mode. This pin should be normally grounded.
23 (power supply)	VD1	Standby power supply for the interface logic and controller.
24 (output)	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5KHz low-pass filter and amplified, will drive a loudspeaker.

PIN FUNCTIONS (Continued)

PIN NUMBER	NAME	FUNCTION
25 (input)	$\overline{\text{SBY RESET}}$	STANDBY RESET. A logic 0 resets the interface logic. Normally should be a logic 1. $\overline{\text{SBY RESET}}$ must be tied to $\overline{\text{RESET}}$ (pin 2).
26 (output)	ROM CLOCK	This is a 1.56MHz clock for an external serial speech ROM.
27 (input)	OSC 1	XTAL IN. Input connection for a 3.12MHz crystal.
28 (output)	OSC 2	XTAL OUT. Output connection for a 3.12MHz crystal.

ELECTRICAL CHARACTERISTICS/SP0264

Maximum Ratings*

All pins with respect to V_{SS} ..... -0.3 to 8.0V
StorageTemperature..... -25°C to 125°C

Standard Conditions
Clock – Crystal Frequency..... 3.120 MHz
Operating Temperature..... T_A= 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS/SP0264

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	6.5	V	
Standby Supply Voltage	V_{D1}	4.5	-	6.5	V	
Primary Supply Current	I_{DD}	-	35	65	mA	$\overline{\text{RESET}}$ and $\overline{\text{SBY RESET}}$ high. OSC1 = 3.12 MHz. All other inputs floating.
Standby Supply Current	I_{D1}	-	15	25	mA	Same as above.
INPUTS						
A1-A8, $\overline{\text{ALD}}$, SER IN, TEST, SE						
LOGIC 0	V_{IL}	0.0	-	0.6	V	
LOGIC 1	V_{IH}	2.4	-	V_{D1}	V	
CAPACITANCE	C_{IN}	-	-	10	pF	0 volts bias, f = 3.12 MHz
LEAKAGE	I_L	-	-	+10	µA	V_{PIN} = 7.0V Other Pins = 0.0V
$\overline{\text{RESET}}$, $\overline{\text{SBY RESET}}$						
LOGIC 0	V_{RSIL}	0.0	-	0.6	V	
LOGIC 1	V_{RSIH}	4.0	-	V_{D1}	V	V_{D1} = 4.5V
		4.6	-	V_{D1}	V	V_{D1} = 6.5V
OUTPUTS						
SBY, Digital Out, C1, C2, C3, $\overline{\text{LRQ}}$, ROM DIS, ROM CLK, SER OUT						
LOGIC 0	V_{OL}	0.0	-	0.6	V	I_{OL} = 0.72mA (2LS TTL Loads)
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	I_{OH} = -50µA (2LS TTL Loads)
OSCILLATOR						
OSC 2 (Output)						When driven from external input
LOGIC 0	V_{OL}	0.0	-	1.0	V	OSC1 (Input) = 4.00V MIN at V_{D1} = 4.50V
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	OSC1 (Input) = 0.60V MAX
Short Circuit Current on OSC2	I_{SC}	-7.5	-	-0.4	mA	OSC1 (Input) = 0.60V OSC2 (Output) = 0.00V
OSC1 Input Current	I_{IN}	-4.9	-	-0.4	µA	OSC1 (Input) = 0.00V

ELECTRICAL CHARACTERISTICS/SP0264I

Maximum Ratings*

All pins with respect to V_{SS}..... -0.3 to 8.0V
StorageTemperature..... -25°C to 125°C

Standard Conditions
Clock – Crystal Frequency..... 3.120 MHz
Operating Temperature.....T_A= -40°C to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

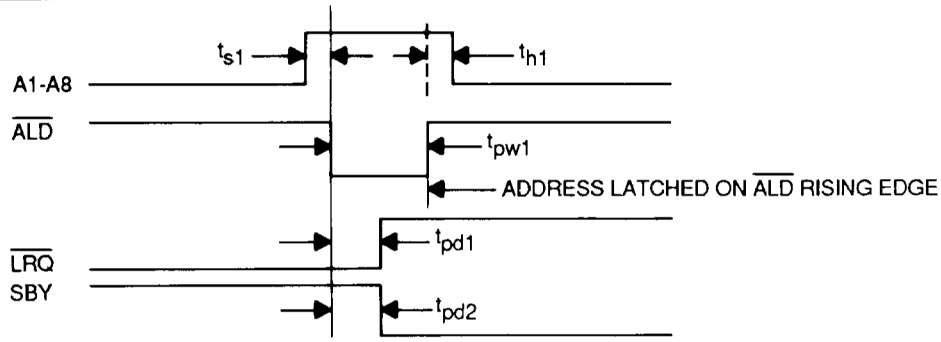
Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS/SP0264I (T_A = -40°C to +85°C)

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	6.5	V	
Standby Supply Voltage	V_{D1}	4.5	-	6.5	V	
Primary Supply Current	I_{DD}	-	35	65	mA	$\overline{\text{RESET}}$ and $\overline{\text{SBY RESET}}$ high. OSC1 = 3.12 MHz. All other inputs floating.
Standby Supply Current	I_{D1}	-	15	25	mA	Same as above.
INPUTS						
A1-A8, $\overline{\text{ALD}}$, SER IN, TEST, SE						
LOGIC 0	V_{IL}	0.0	-	0.6	V	
LOGIC 1	V_{IH}	2.4	-	V_{D1}	V	
CAPACITANCE	C_{IN}	-	-	10	pF	0 volts bias, f = 3.12 MHz
LEAKAGE	I_L	-	-	+10	µA	V_{PIN} = 7.0V Other Pins = 0.0V
$\overline{\text{RESET}}$, $\overline{\text{SBY RESET}}$						
LOGIC 0	V_{RSIL}	0.0	-	0.6	V	
LOGIC 1	V_{RSIH}	4.0	-	V_{D1}	V	V_{D1} = 4.5V
		4.6	-	V_{D1}	V	V_{D1} = 6.5V
OUTPUTS						
SBY, Digital Out, C1, C2, C3, $\overline{\text{LRQ}}$, ROM DIS, ROM CLK, SER OUT						
LOGIC 0	V_{OL}	0.0	-	0.6	V	I_{OL} = 0.72mA (2LS TTL Loads)
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	I_{OH} = -50µA (2LS TTL Loads)
OSCILLATOR						
OSC 2 (Output)						When driven from external input
LOGIC 0	V_{OL}	0.0	-	1.0	V	OSC1 (Input) = 4.00V MIN at V_{D1} = 4.50V
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	OSC1 (Input) = 0.60V MAX
Short Circuit Current on OSC2	I_{SC}	-7.5	-	-0.4	mA	OSC1 (Input) = 0.60V OSC2 (Output) = 0.00V
OSC1 Input Current	I_{IN}	-4.9	-	-0.4	µA	OSC1 (Input) = 0.00V

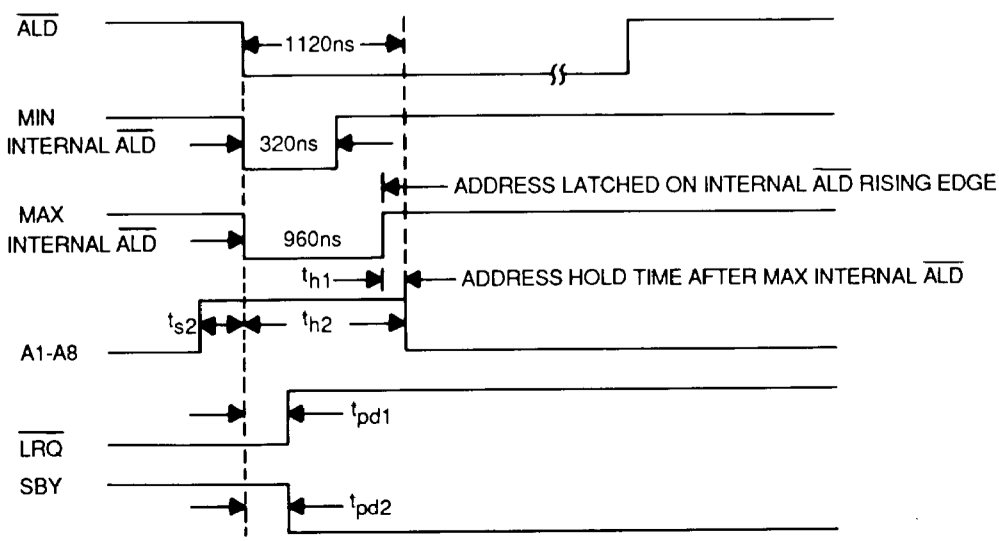
AC CHARACTERISTICS

	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{ALD}$	t_{pw1}	200	-	960	ns	$200 \le \overline{ALD} \le 960$ ns
A1 - A8 Set Up	t_{s1}	160	-	-	ns	
Hold	t_{h1}	160	-	-	ns	
$\overline{LRQ}$	t_{pd1}	-	-	300	ns	
SBY	t_{pd2}	-	-	300	ns	



AC CHARACTERISTICS

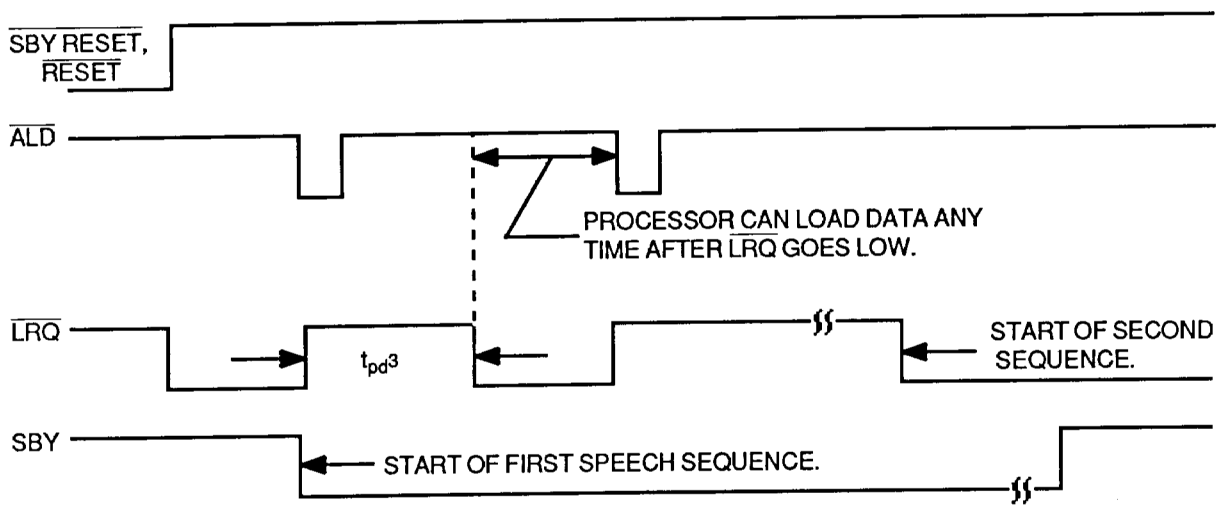
	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
A1 - A8 Set Up	t_{s2}	0	-	-	ns	$\overline{ALD} \ge 960$ ns
Hold	t_{h2}	1120	-	-	ns	
$\overline{LRQ}$	t_{pd1}	-	-	300	ns	
SBY	t_{pd2}	-	-	300	ns	



AC CHARACTERISTICS

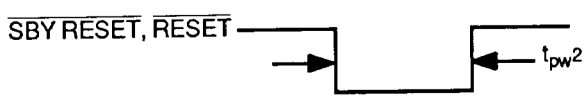
	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{LRQ}$	t_{pd3}	16.67	-	33.3	µs	Address Buffer ready for next load.

TYPICAL TIMING SEQUENCE

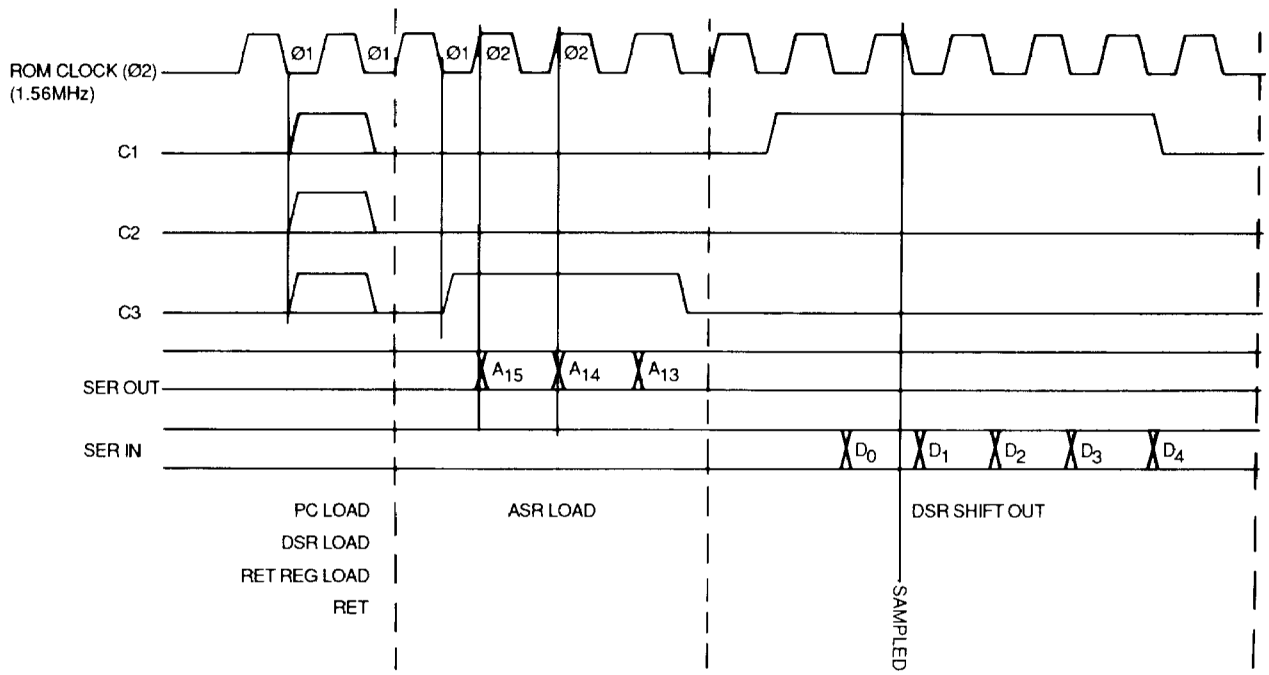


AC CHARACTERISTICS

	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Clock	F	3.11	3.120	3.13	MHz	Crystal oscillator driven from external.
Clock Duty Cycle	-	48	-	52	%	
$\overline{RESET}$, $\overline{SBY\ RESET}$	t_{pw2}	25	-	-	µs	

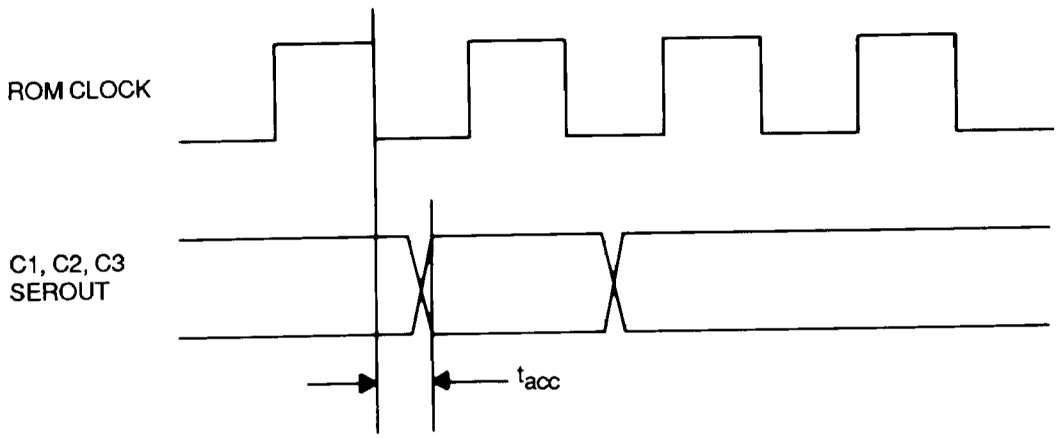


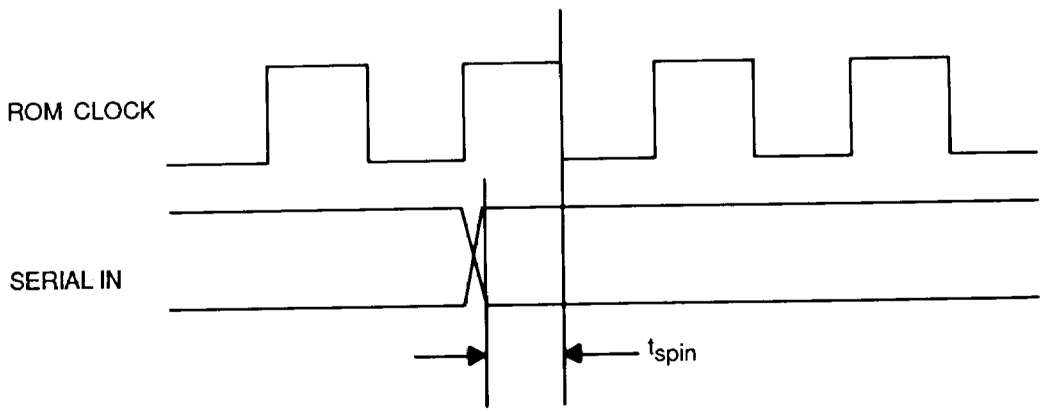
EXTERNAL ROM INTERFACE TIMING



AC CHARACTERISTICS

	SYM.	MIN	TYP	MAX	UNITS	CONDITIONS
Access time	t_{acc}		–	275	ns	
Serial in setup time	t_{spin}	200	-	-	ns	



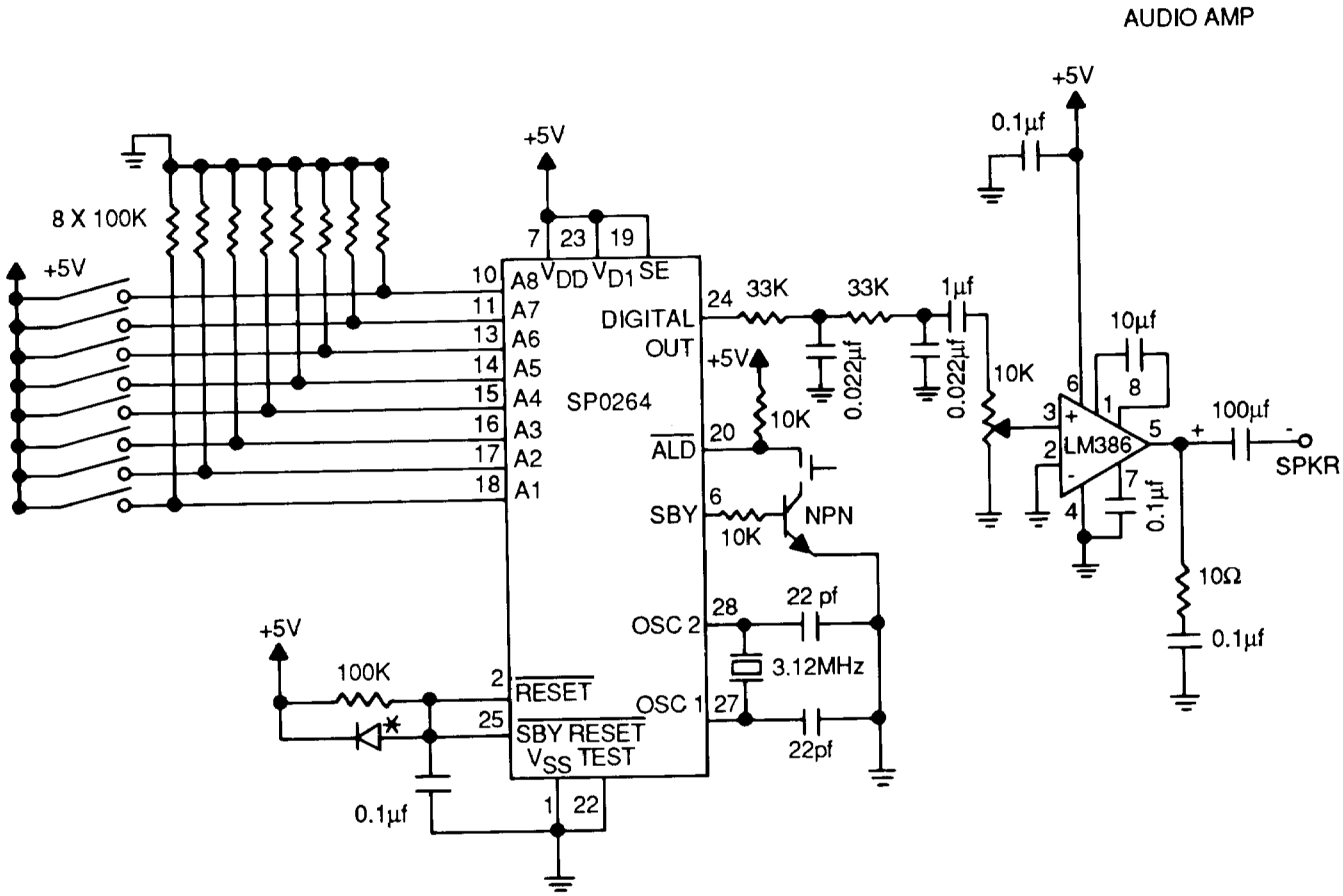


SP0264 EXTERNAL AND INTERNAL CONTROL LINES* (ALL SYNCHRONOUS TO THE ROM CLOCK)

C1	C2	C3		
0	0	0	NOP -	No Action Taken
0	0	1	ASRLD -	(Address Shift Register Load) Serially shifts data (MSB first) from the serial address out pin (also occurs internally in the SP0264) into the ASR reg in preparation for loading into the PC. The ASRLD loads the 16 bits of the ASR with two 8-bit load sequences followed shortly by PCLD.
0	1	0	PCLD -	Loads the contents of the ASR register into the PC. Occurs only after 16 ASRLDS have occurred.
0	1	1	DSRLD -	(Data Shift Register Load) Loads the 8 bit data shift register with the contents of the ROM pointed to by the current address in the PC. The DSRLD will also shift out the LSB of the 8 bit DSR and increment the PC.
1	0	0	DSRSH -	(Data Shift Register Shift) Shifts data out of DSR reg starting with the second LSB (the first LSB is shifted out with the occurrence of a DSRLD). There are seven (7) DSRSH's after every DSRLD (not necessarily consecutive).
1	0	1	STACK LD -	Loads the STACK with the current value of the PC.
1	1	0	RETURN -	Loads the PC with the contents of the STACK.
1	1	1		Op Code not implemented.

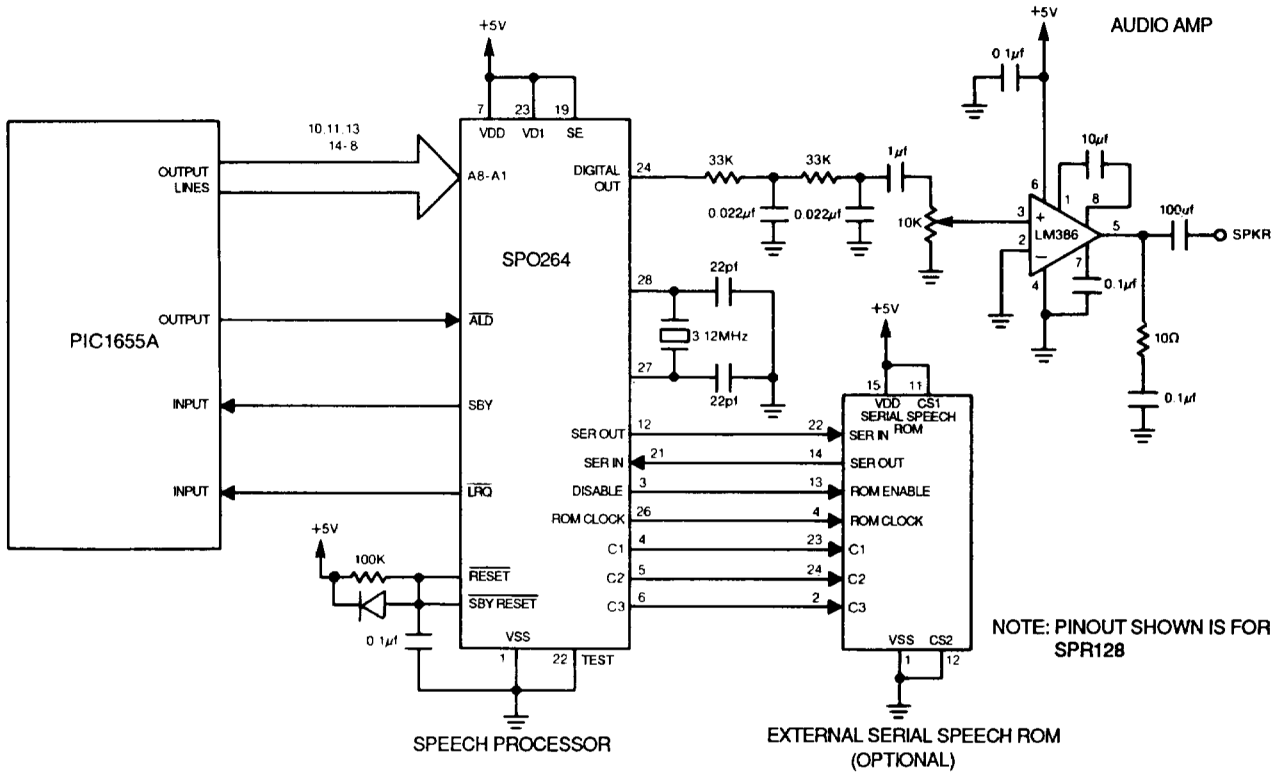
*All ROMs including the SP0264 internal ROM will be activated by the above control lines. However only the ROM with the current chip select will be enabled to send speech data to the SP0264.

TYPICAL APPLICATION STANDALONE CONFIGURATION



*Diode possibly necessary if power is turned off then on in less than 50ms.

TYPICAL APPLICATION MICROCOMPUTER INTERFACE



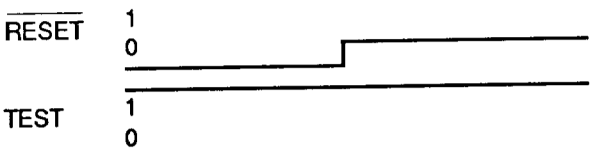
TEST MODES

The TEST pin (22) should be kept grounded at all times to avoid entering any test mode accidentally.

INTERNAL ROM DISABLE

This mode may be entered by wiring TEST to a permanent high and pulsing $\overline{\text{RESET}}$. This causes the SP0264 to ignore its internal ROM. Instructions must be supplied serially through pin 21 (Serial Data In). The chip should be interfaced to an SPR000 to fully utilize this mode.

Returning TEST to 0 will not rescind this mode unless $\overline{\text{RESET}}$ is pulsed.



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