

[A guide to using FETs for voltage controlled circuits, Part 2](#)

Ron Quan - January 02, 2018

In [Part 1](#) of this five-part series, we examined FET voltage controlled resistors, basic voltage controlled resistor circuits, and a balanced or push pull voltage controlled resistor (VCR) circuit. Next, let's take a look at an N-Channel JFET attenuator circuit with feedback (**Figure 8**).

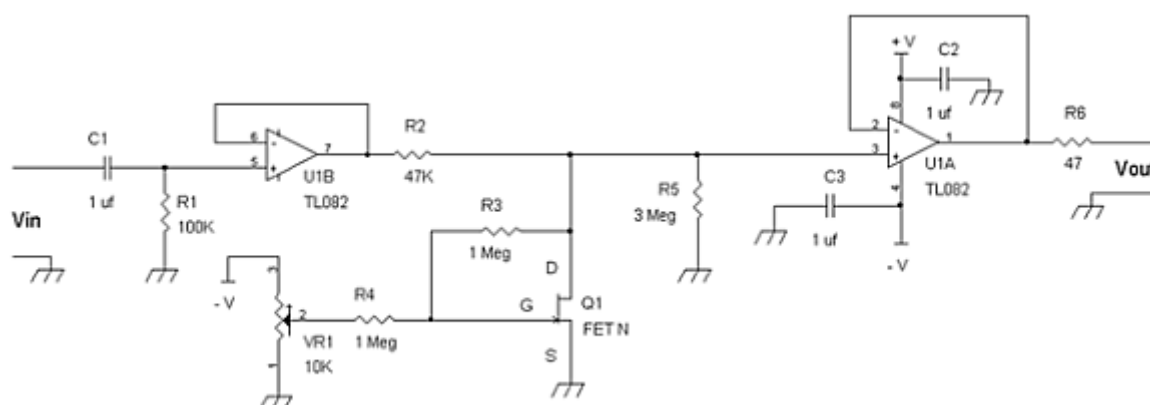


Figure 8 Feedback resistors R3 and R4 provide distortion reduction.

If we refer back to [Figure 2](#) in Part 1, for a voltage controlled resistor without feedback resistors, we see that for $V_{DS} > 0$ volt, the resistance is higher than when $V_{DS} < 0$ volts via the S1 and S2 slopes.

Intuitively, if $V_{DS} > 0$ volt or positive in **Figure 8**, a portion of V_{DS} (voltage across the drain and source of Q1) positive voltage via R3 gets added to the gate voltage. This makes the gate less negative when combined with VR1's slider voltage, which means that the drain to source resistance drops for $V_{DS} > 0$ volt.

When $V_{DS} < 0$ volt, there is additional negative voltage added to the gate via R3, which makes the gate voltage more negative resulting in higher resistance across the drain and source of Q1.

Therefore, the resistances at $V_{DS} > 0$ volt and $V_{DS} < 0$ volt become closer in value using the feedback resistor network R3 and R4, which will then reduce distortion.

Note that when $R3 = R4$, R3 and R4 provide half of the V_{DS} voltage back to gate. Let's see why this is good for cancelling out distortion.

Let's take a look at the drain current equation (1):

$$I_d = I_{DSS} \left[2\left(1 - \frac{V_{gs}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) - \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \right] \quad (1)$$

We will want to eliminate the terms related to (V_{ds}/V_p) (V_{ds}/V_p) so that the conductance (g_{ds}) is only a function of V_{gs} when we take the derivative of I_d with respect to V_{ds} . For a linear conductance, we still want a V_{ds} term in the drain current equation that is multiplied by a constant or a factor related to a control voltage.

Let $V_{gs} = V_c + k V_{ds}$, where V_c is the control voltage, $0 < k < 1$, and k is the feedback factor.

This leads to:

$$\begin{aligned} I_d &= I_{DSS} \left[2\left(1 - \frac{V_c + kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) - \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \right] \\ I_d &= I_{DSS} \left[2\left(1 - \frac{V_c + kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \\ I_d &= I_{DSS} \left[2\left(1 - \frac{V_c}{V_p} - \frac{kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \\ I_d &= I_{DSS} \left[2\left(1 - \frac{V_c}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) \right] + I_{DSS} \left[2\left(-\frac{kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \end{aligned} \quad (7)$$

We would like to set the last two terms to cancel each other, that is:

$$I_{DSS} \left[2\left(-\frac{kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{-V_p}\right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) = 0$$

$$I_{DSS} \left[2\left(\frac{kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) = 0$$

Or alternatively,

$$I_{DSS} \left[2\left(\frac{kV_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right) \right] = I_{DSS} \left(\frac{V_{ds}}{V_p}\right)\left(\frac{V_{ds}}{V_p}\right)$$

If we divide both sides by I_{DSS} , and then multiply both sides by (V_p) (V_p) , we get:

$$2(kV_{ds})(V_{ds}) = (V_{ds})(V_{ds})$$

Dividing by $(V_{ds})(V_{ds})$ on both sides and solving for k we get

$$2k = 1$$

$$k = 1/2$$

For the feedback resistors R_3 and R_4

$$k = 1/2 = R_4/(R_3 + R_4)$$

This means $R_3 = R_4$ for a feedback factor of $k = 1/2$.

With $V_{gs} = V_c + kV_{ds}$

$$k = 1/2$$

$$k = 0.5$$

$$V_{gs} = V_c + 0.5 V_{ds}$$

Now let's go back to equation (7)

$$I_d = I_{DSS} \left[2 \left(1 - \frac{V_c}{V_p} \right) \left(\frac{V_{ds}}{-V_p} \right) \right] + I_{DSS} \left[2 \left(-\frac{k V_{ds}}{V_p} \right) \left(\frac{V_{ds}}{-V_p} \right) \right] - I_{DSS} \left(\frac{V_{ds}}{V_p} \right) \left(\frac{V_{ds}}{V_p} \right) \quad (7)$$

With $k = 1/2$, the last two terms disappear in equation (7).

$$I_d = I_{DSS} \left[2 \left(1 - \frac{V_c}{V_p} \right) \left(\frac{V_{ds}}{-V_p} \right) \right] \quad (8)$$

$$g_{ds} = \frac{d}{dV_{ds}} I_d = \frac{d}{dV_{ds}} I_{DSS} \left[2 \left(1 - \frac{V_c}{V_p} \right) \left(\frac{V_{ds}}{-V_p} \right) \right] \quad (9)$$

$$g_{ds} = I_{DSS} \left[2 \left(1 - \frac{V_c}{V_p} \right) \left(\frac{1}{-V_p} \right) \right]$$

$$g_{ds} = I_{DSS} \left[-2 \left(\frac{1}{V_p} \right) \left(1 - \frac{V_c}{V_p} \right) \right] \quad (10)$$

$$R_{ds} = 1/g_{ds} = 1/\{I_{DSS} \left[-2 \left(\frac{1}{V_p} \right) \left(1 - \frac{V_c}{V_p} \right) \right]\}$$

$$R_{ds} = 1/\{I_{DSS} \left[-2 \left(\frac{1}{V_p} \right) \left(1 - \frac{V_c}{V_p} \right) \right]\} \quad (11)$$

With a given V_p and I_{DSS} , equation (11) then shows that the drain to source resistance R_{ds} is only dependent on the control voltage V_c and without any dependence on V_{ds} . Thus, using the feedback resistors R_3 and R_4 , on a first approximation, provides a linear voltage controlled resistor.

Figure 9 shows a P-Channel JFET version with feedback resistors to lower distortion.

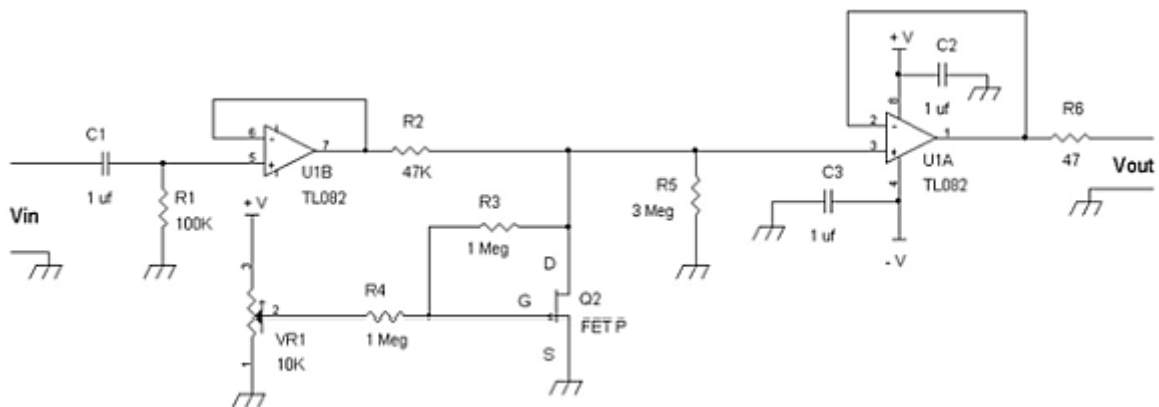


Figure 9 An example P-Channel voltage controlled resistor circuit with a feedback resistor network R_3 and R_4 to lower distortion.

If you will note that in **Figures 8 and 9**, the feedback resistor network uses high resistance values to allow the FET's (e.g., Q_1 and Q_2 in **Figures 8 and 9**) drain to source resistance to dominate in forming the voltage divider with R_2 .

For example, if R_3 and $R_4 = 22\text{K}\Omega$, then there will be approximately a $44\text{K}\Omega$ resistor in parallel with the R_5 and the FET's drain to source resistance. This $2\text{K}\Omega$ resistance will then “wash” out some of the FET's R_{ds} effects. This will not allow the input signal, V_{in} , to pass substantially unattenuated when the FET is at cut-off (e.g., at infinite resistance) with $R_2 = 47\text{K}\Omega$.

Using a feedback network to reduce distortion can also be applied to enhancement mode MOSFETs (**Figure 10**).

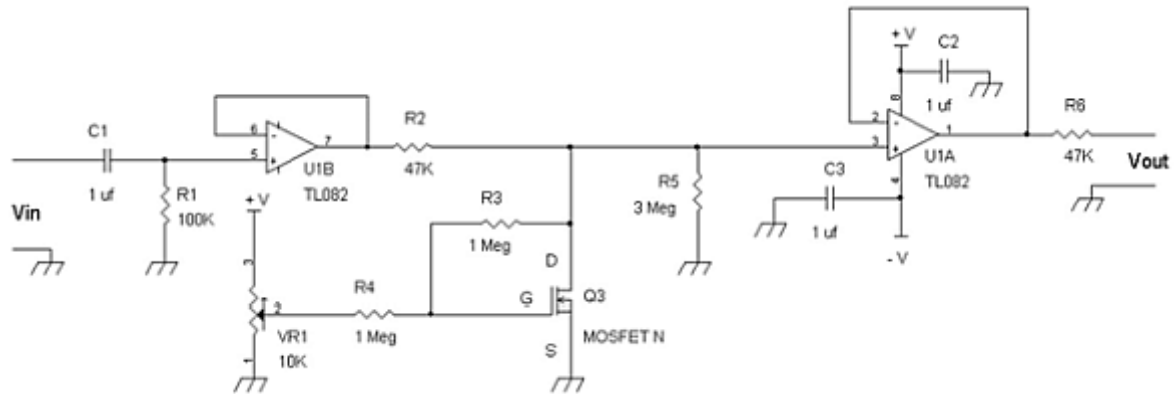


Figure 10 An N-Channel MOSFET voltage controlled attenuator circuit with a feedback network to reduce distortion.

As shown in Appendix A, the feedback network, R_3 and R_4 should be equal resistance for cancelling distortion for enhancement devices. However, in some cases, the distortion reduction worked even better with a buffer amplifier (e.g., **Figure 14**).

A P-Channel version is shown in **Figure 11**.

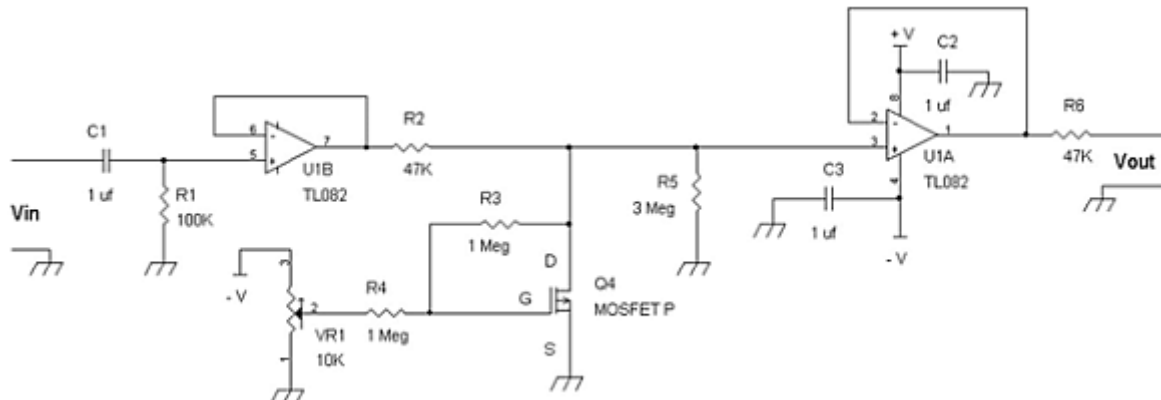


Figure 11 A P-Channel MOSFET voltage controlled attenuator with distortion reduction network R_3 and R_4 .

Improving the distortion reduction circuits

Improving the distortion reduction circuits

Figures 8, 9, 10, and 11 have feedback resistor networks R_3 and R_4 to lower distortion. There are a few drawbacks to reducing the distortion this way:

- 1) Only very large value resistors R_3 and R_4 are used, which limit the attenuation range.

- 2) The resistor network is connected to the control voltage that will leak a slight DC or control bias voltage into the drain terminal via R3 and R4.
- 3) The resistive network R3 and R4 halves the control voltage range into the gate. If the FET has a high pinch off voltage such as - 10 volts, then a - 20-volt control voltage is needed.

To improve on #1 and #2 above, **Figures 12, 13, 14, and 15** shows by taking advantage of the voltage follower, U1A, the buffered drain to source voltage can be fed back to the gate.

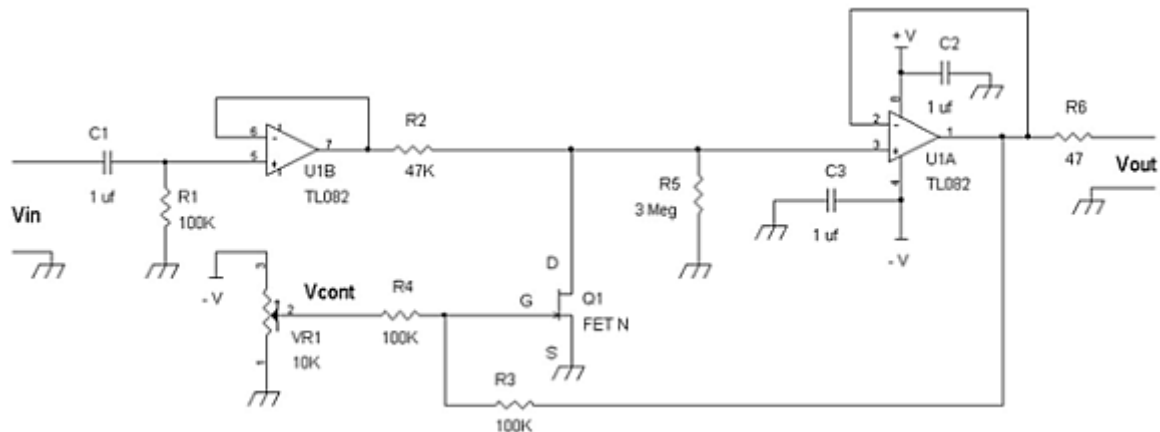


Figure 12 A buffered feedback method via U1A to reduce distortion via the R3 and R4 network to the N-Channel FET's gate.

The resistor values for R3 and R4 can be lowered without limiting the attenuation range.

Note that there are no additional parts added. We just used the existing output buffer amplifier, U1A. As can be seen, resistors R3 and R4 no longer add any DC bias or control voltage back to the FET's drain terminal. What's more is that the series resistance from R3 and R4 is no longer in parallel to R5 and the drain to source voltage controlled resistance of the FET.

As a bonus, R3 and R4 can be lower value resistors so that the control voltage can be run at higher frequencies without fear that the FET's gate to source capacitance will roll off the frequency response.

Similarly, **Figure 13** shows a P-Channel JFET example, and **Figures 14 and 15** show MOSFET versions.

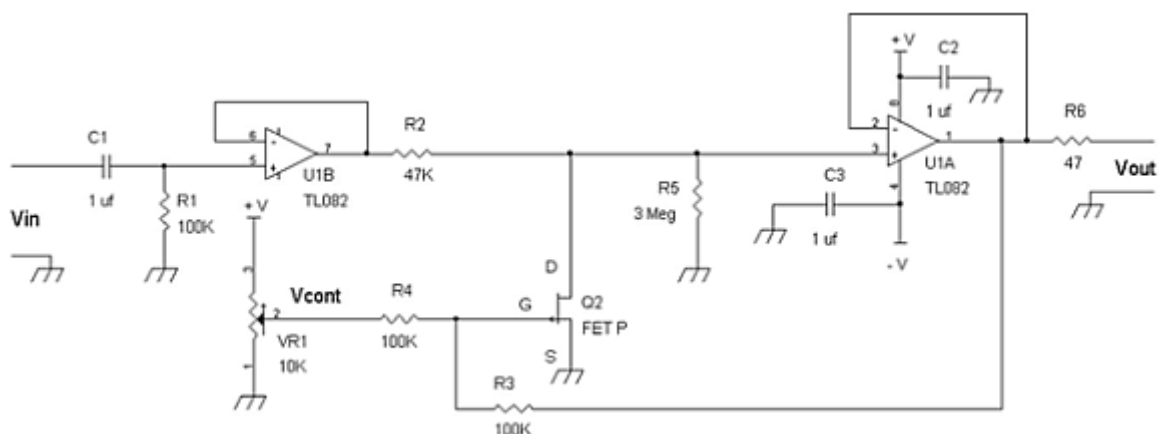


Figure 13 A P-Channel JFET voltage controlled resistor with distortion reduction network via a buffer amplifier, U1A.

Distortion reduction via the feedback resistor networks R3 and R4 generally works well whether the signal was buffered or not. However, at least in one example of MOSFETs, having the buffer improved lowering the distortion more than having R3 connected across the drain and gate (**Figure 14**).

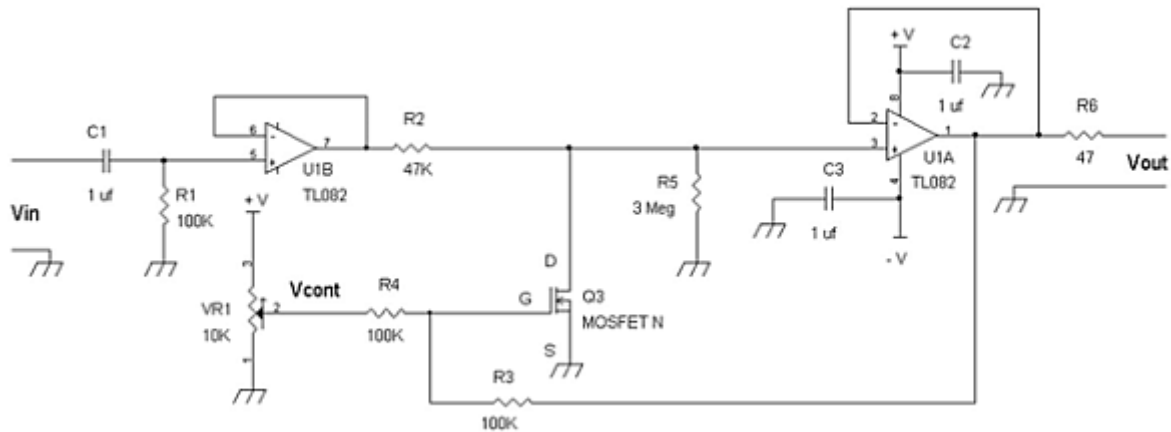


Figure 14 An N-Channel MOSFET version with distortion reduction via a buffer amplifier U1A.

For N-Channel MOSFETs such as the SD5000 DMOS devices, having the buffer amplifier U1A (or equivalent) reduced the distortion much better than having R3 connected across the drain and gate with R4 connected to the control voltage and gate. See **Figure 15** for a P-Channel example.

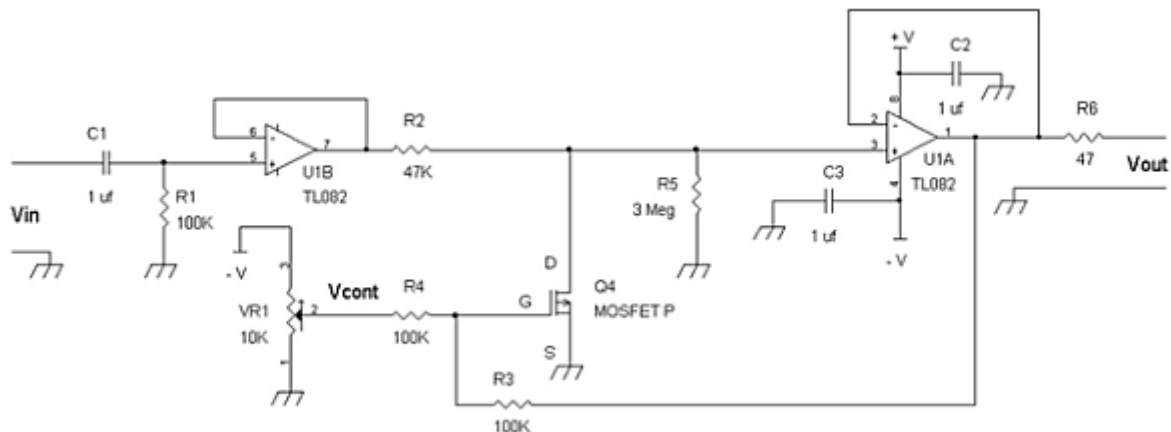


Figure 15 A P-Channel MOSFET attenuator circuit with distortion reduction via voltage follower U1A, with R3, and R4.

In **Figures 12, 13, 14, and 15**, the distortion is reduced and feedback resistor R3 is isolated from the drain of the FET. However, we should observe that the control voltage, V_{cont} , is attenuated by 50% into the gate of the FET.

We can transfer the entire control voltage into the gate by using a summing amplifier as shown in **Figures 16 and 17**. This way we do not require twice the control voltage.

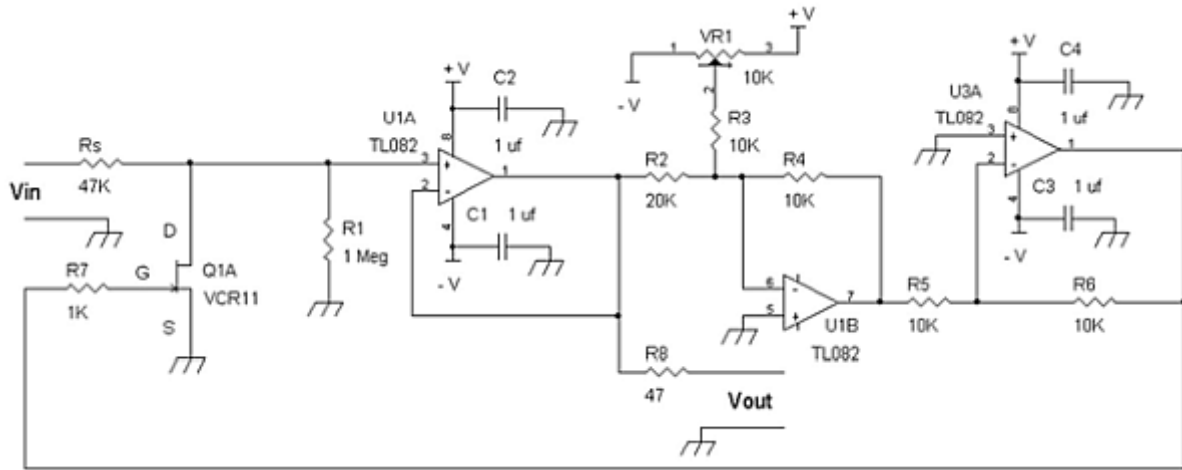


Figure 16 Summing amplifier circuit comprising U1B and U3A allows for avoiding control voltage attenuation into Q1A's gate.

To provide distortion reducing feedback from the drain back to the gate, buffer amplifier U1A couples the drain voltage to R2. Since the feedback resistor, R4 (10K Ω), for U1B is one half the resistance of R2 (20K Ω), there is a gain of - 0.5 at pin 7, U1B. A unity gain inverting amplifier circuit via R5, R6, and U3A inverts the phase from pin 7 U1B so that half of the voltage from Q1A's drain is sent to its gate. The control voltage via VR1 is sent to Q1A's gate without attenuation. This is done via summing amplifier circuit including U1B and U3A. **Figure 16** shows an N-Channel JFET Q1A where the control voltage varies from 0 volts to -V. If the N-Channel JFET is changed to a P-Channel JFET, the control voltage will vary from 0 volts to + V. Resistor R7 provides some protection to the gate of the FET just in case of power start up conditions that cause forward biasing the gate to source junction.

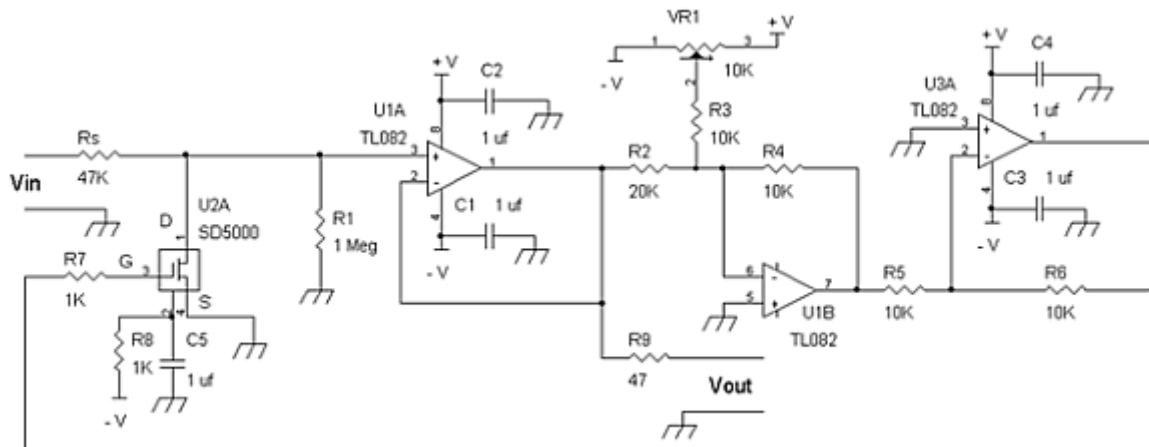


Figure 17 Summing amplifier via U1B and U3A allows for transferring the control voltage from VR1 without attenuation.

Similarly, for an N-Channel MOSFET in **Figure 17**, we have half the drain signal voltage transferred back to the gate via U1B and U3A. R2 and R4 forms a 50% inverting gain amplifier at U1B pin 7. Unity gain inverting amplifier U3 with R5 and R6 inverts the phase from U1B pin 7 such that 50% of the drain signal voltage is coupled to the gate of U2A. VR1 transfers its full control voltage U2A's gate via a unity gain amplifier including U1B with R3 and R4, and U3A with R5 and R6.

The control voltage varies from 0 volts to +V for an N-Channel MOSFET, and 0 volts to - V for a P-Channel device.

The [next article in this five-part series](#) will be about FET modulator circuits and variable gain

amplifier by reducing the drain-to-source voltage.

[Ron Quan](#) is an author, design engineer, and inventor with over 75 US patents.

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