Problem 1

Requirements

This stage is used to lay out all the requirements of the design.

It is not done with a tool in lab.

Its input is the problem to be solved.

Its output is the design requirements.

Design Specifications

This stage is used to set all of the specifications for the design.

It is not done with a tool in lab.

Its input is the problem and design requirements.

Its output is the design specifications.

Design Formulation

This stage is used for conceptualizing the design.

It does not use a tool from lab.

Its inputs are the specifications.

Its output is the design.

Design Entry

In this stage the design is entered in a schematic or HDL.

We use Modelsim and Vivado to enter our designs in Verilog.

The input is the formulated design.

Its output is the design described in a HDL.

Simulation

In this stage the design is simulated to make sure it functions correctly.

We use the Modelsim simulator to simulate our designs.

Its input is the design written in a HDL.

Its output is knowledge about design bugs or a confirmation of functionality.

Logic Synthesis

This stage is used to convert the HDL code into a description of the actual hardware components and connections.

We use the synthesis tool in Vivado to do this.

The input is the HDL code for the design.

The output is a netlist, which describes the actual hardware and connections.

Post-Synthesis Simulation

In this stage we simulate the actual hardware of the design to see if it works.

We use Modelsim's simulation tools to simulate post-synthesis implementation of the design.

The input is the netlist that describes the hardware of the design.

The output is a simulation of the design, which reveals bugs or is confirmed to work correctly.

Mapping, Placement, and Routing

In this stage the synthesized design is mapped to a specific technology, placed with specific parts, and routs the hardware connections.

We use an FPGA as the target technology of our design.

The input is the synthesized design.

The output is a physical device programmed with the design.

ASIC Masks

If the design is being implemented with ASIC then a photomask is used in the IC design.

We do not do this in our labs.

The input is the synthesized design to be implemented on ASIC.

The output is an ASIC programmed with the design.

FPGA Programming Unit

In this stage the design is translated to a format that is able to program the FPGA.

We use Vivado’s bitstream generating tool for this stage.

The input is the synthesized design.

The output is a bitstream that is able to program the FPGA with the design.

Configured FPGAs

In this stage the bitstream is used to configure the FPGA to represent the synthesized design.

We use Vivado’s programming tool to configure the FPGA with the bitstream file.

The input is the bitstream file representing the design.

The output is a FPGA configured with the design.