

Practical No. 11

Aim: To study shift register.

Apparatus: Sigma shift registers trainer - DSR08, Connecting wires

Theory:

A universal shift register is an integrated logic circuit that can transfer data in three different modes. Like a parallel register it can load and transmit data in parallel. Like shift registers it can load and transmit data in serial fashions, through left shifts or right shifts. In addition, the universal shift register can combine the capabilities of both parallel and shift registers to accomplish tasks that neither basic type of register can perform on its own. For instance, on a particular job a universal register can load data in series (e.g. through a sequence of left shifts) and then transmit/output data in parallel.

Universal shift registers, as all other types of registers, are used in computers as memory elements. Although other types of memory devices are used for the efficient storage of very large volume of data, from a digital system perspective when we say computer memory we mean registers. In fact, all the operations in a digital system are performed on registers. Examples of such operations include multiplication, division, and data transfer.

In order for the universal shift register to operate in a specific mode, it must first select the mode. To accomplish mode selection the universal register uses a set of two selector switches, S1 and S0. As shown in Table 1, each permutation of the switches corresponds to a loading/input mode.

Operating Mode	S1	S0
Locked	0	0
Shift-Right	0	1
Shift-Left	1	0
Parallel Loading	1	1

Table 1

In the locked mode ($S_1S_0 = 00$) the register is not admitting any data; so that the content of the register is not affected by whatever is happening at the inputs. You may verify this detail by playing around with the main interactive circuit. For example, set $L_3L_2L_1L_0 = 1010$ and then cycle the clock to see that nothing changes at the outputs as long as $S_1S_0 = 00$. See Table 2.

Clock Cycle	L3	L2	L1	L0		Q3	Q2	Q1	Q0
Initial Value	1	0	1	0		0	0	0	0
Cycle 1	1	0	1	0		0	0	0	0

Table 2

In the shift-right mode ($S1S0 = 01$) serial inputs are admitted from Q3 to Q0. You can confirm this aspect by setting the value of the shift-right switch according to the sequence 1100100 as you cycle the clock; see Table 3. Watch as the signals move from Q3 to Q0. In the shift-left mode ($S1S0 = 10$) the register works in a similar fashion, except that the signals move from Q0 to Q3.

Clock Cycle	Shift-Right Switch	Q3	Q2	Q1	Q0
Initial Value	Initial Value	0	0	0	0
Cycle 1	1	1	0	0	0
Cycle 2	1	1	1	0	0
Cycle 3	0	0	1	1	0
Cycle 4	0	0	0	1	1
Cycle 5	1	1	0	0	1
Cycle 6	0	0	1	0	0
Cycle 7	0	0	0	1	0

Table 3

Finally, in the parallel loading mode ($S1S0 = 11$) data is read from the lines L0, L1, L2,

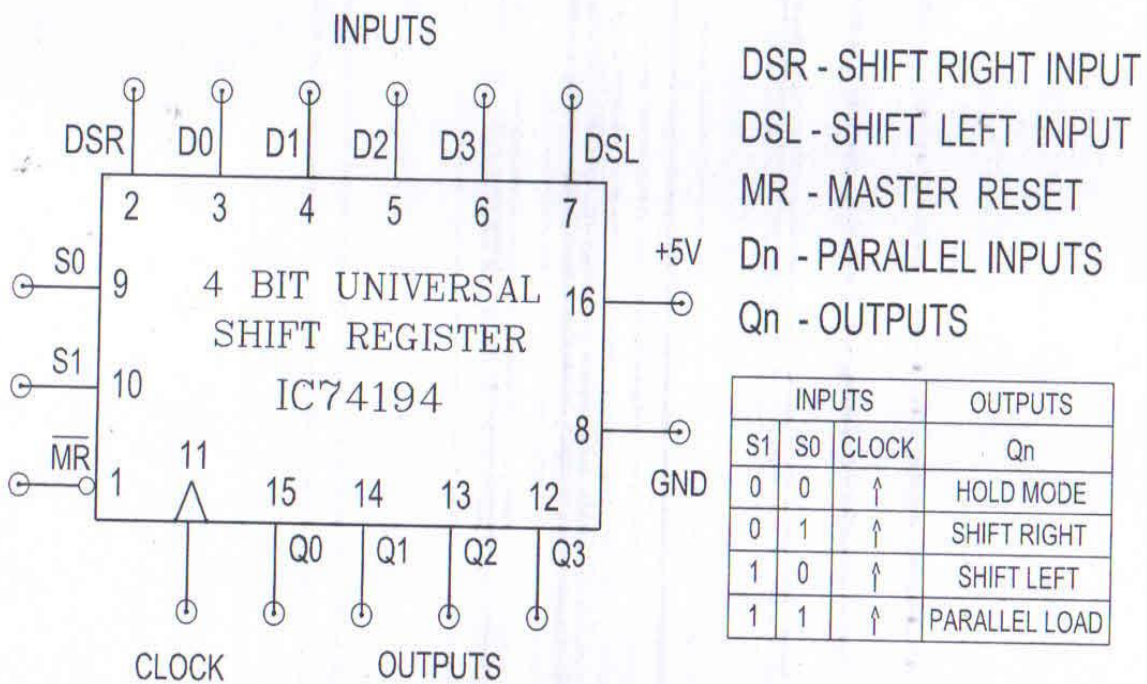
and L3 simultaneously. Here, setting $L3L2L1L0 = 1010$ will cause $Q3Q2Q1Q0 = 1010$ after cycling the clock as depicted in Table 4.

Clock Cycle	L3	L2	L1	L0		Q3	Q2	Q1	Q0
Initial Value	1	0	1	0		0	0	0	0
Cycle 1	1	0	1	0		1	0	1	0

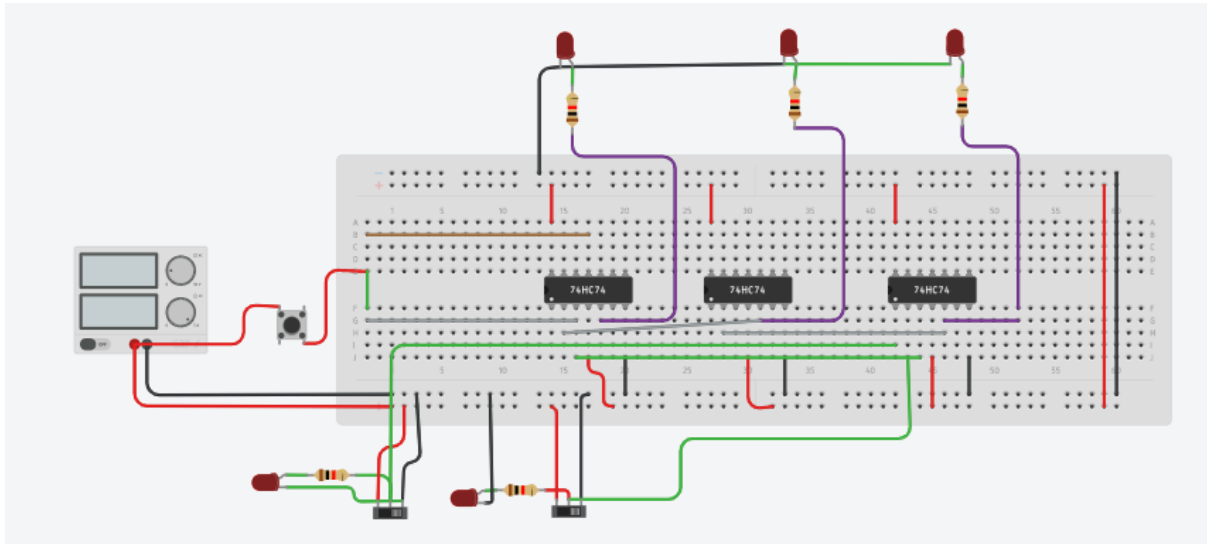
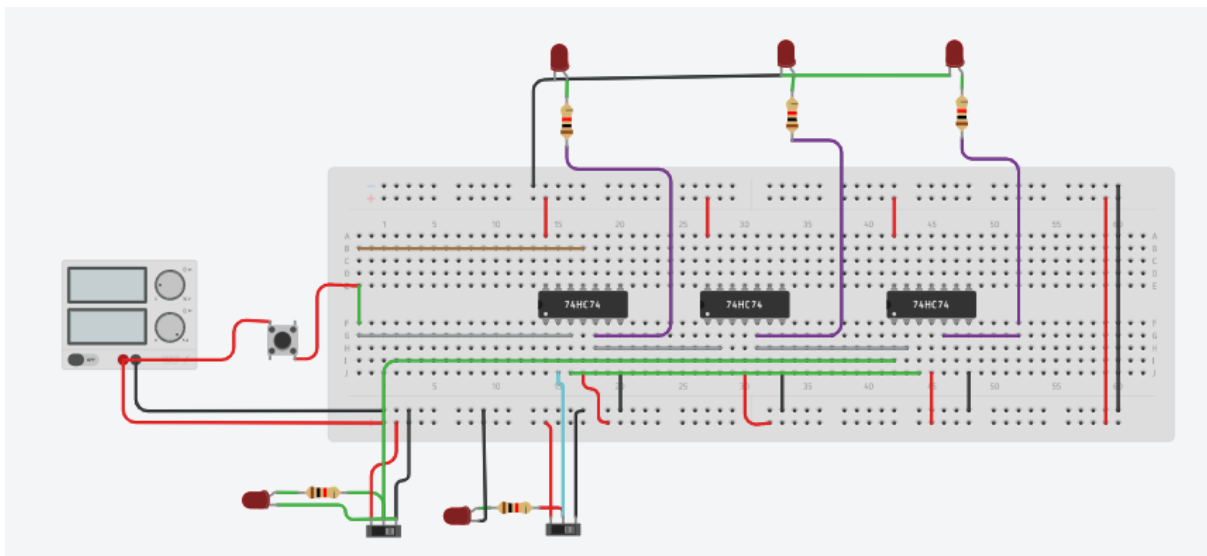
Table 4

Procedure:

- Do the connection as per below kit connection diagram for various shift register.
- Apply proper input condition and observe the output information of led on/off.
- Compare theoretical data with observation and write conclusion.



4 BIT UNIVERSAL SHIFT REGISTER

Tinker Cad simulation:**(1) 3 Bit Shift Left****(2) 3 Bit Shift right****Conclusion**

The information stored within these registers can be transferred with the help of shift registers. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data