

Designing step:- (procedure)

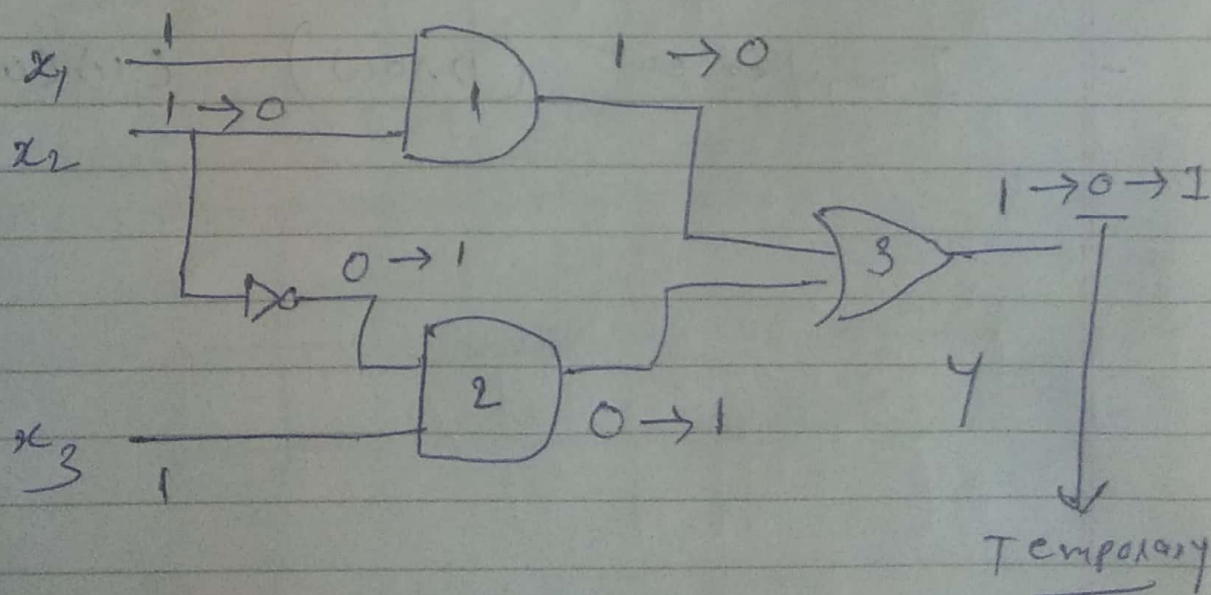
- observe the problem definition
- Determine the required i/p & o/p
- assign letter symbols to the i/p variables
- Make T.T.
- Determine Boolean Expression
- Implement (draw) circuit.

(problem)

* Hazards :-

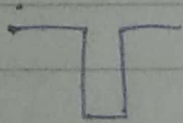
- Hazards are unwanted switching transients that may appear at the output of circuit because of different paths exhibit different propagation delay.
- Hazards occur in combinational circuits where they may cause a temporary false output values.

$$Y = x_1 x_2 + \bar{x}_2 x_3$$

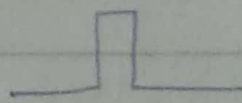


→ when x_2 changes from 1 to 0, both input at gate 3 may be equal to 0 momentarily, causing the output to go to 0 for the short interval of time

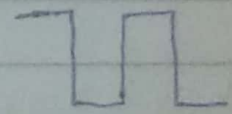
→ when the output momentarily go to 0 when it should remain 1 the hazard is ~~known~~ known as static - 1 hazard



a) static - 1



b) static - 0



c) Dynamic hazard

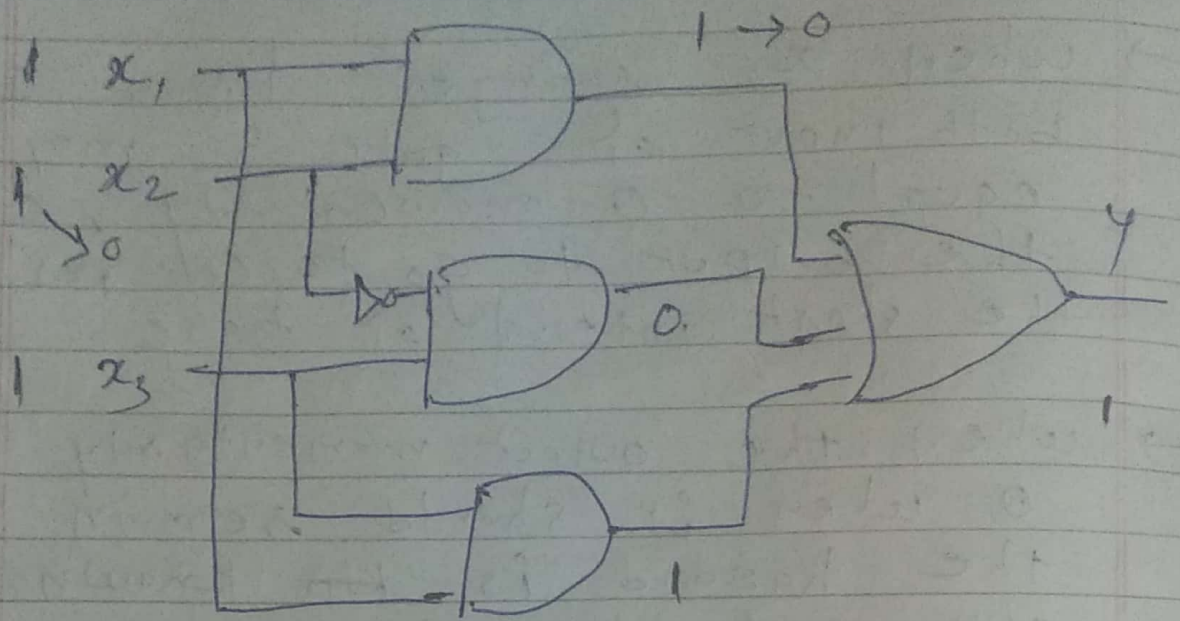
→ removing

$$y = x_1 x_2 + \bar{x}_2 x_3$$

$x_1 \searrow \begin{matrix} x_2 x_3 \\ \bar{x}_2 \bar{x}_3 & \bar{x}_2 x_3 & x_2 \bar{x}_3 & x_2 x_3 \end{matrix}$

\bar{x}_1	0	1	3	2
x_1	4	1	1	1
	1	5	7	6

$$y = \bar{x}_2 x_3 + x_1 x_2 + x_1 x_3$$



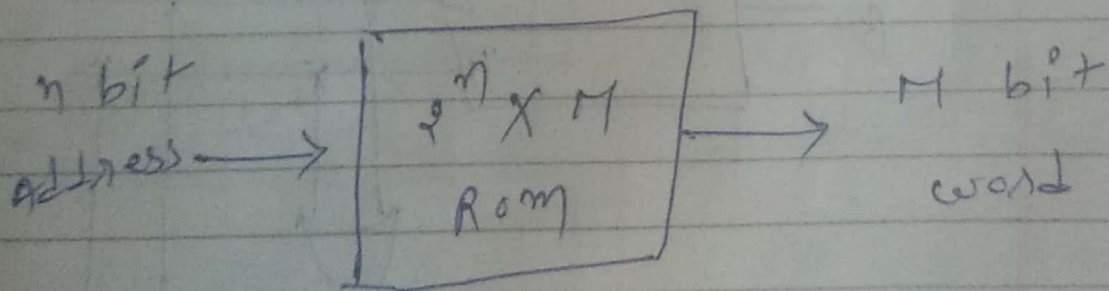
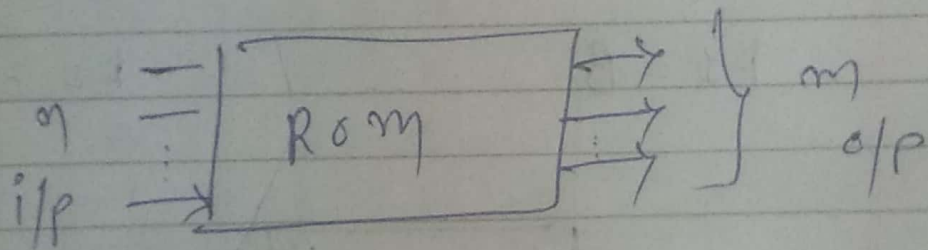
(prog. Logic Device)

PLD ✓

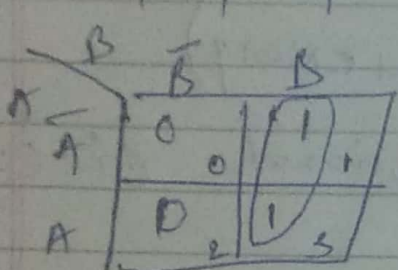
	AND	OR
1) ROM	fixed	prog
2) PLA	prog	prog
3) PAL	prog	fixed

1) ROM (Read Only Memory)

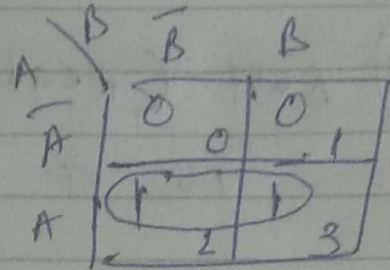
is a Combinational Circuit



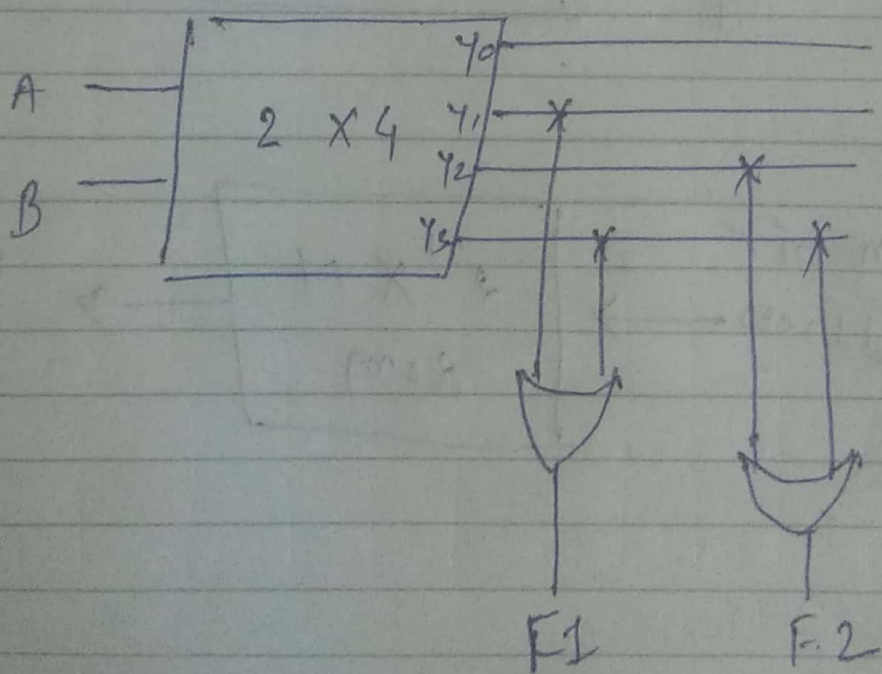
A	B	F ₁	F ₂
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1



$$F_1 = B$$



$$F_2 = A$$



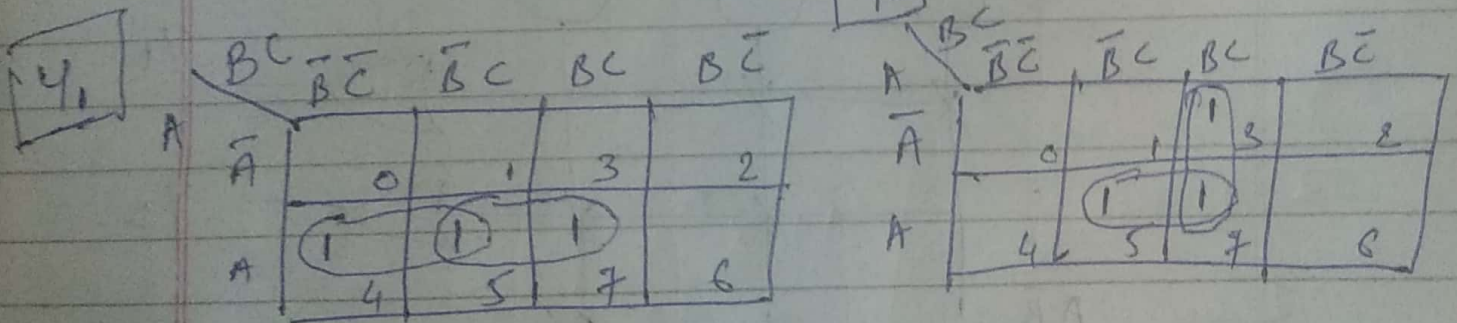
No. of OR = No. of output (2)

(PLA) \rightarrow (prog. Logic Array)

It is PLD with programmable AND gates followed by programmable OR gates

Step 1

A	B	C	y_1	y_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

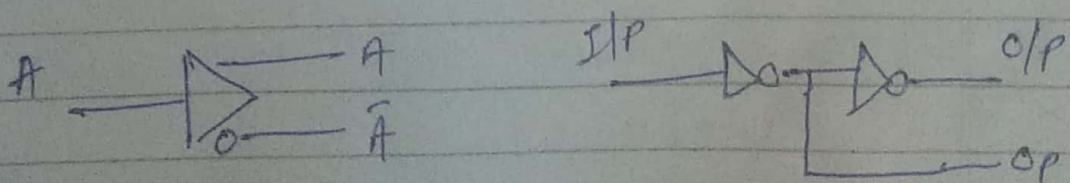


Step 2

$$y_1 = A\bar{B} + AC$$

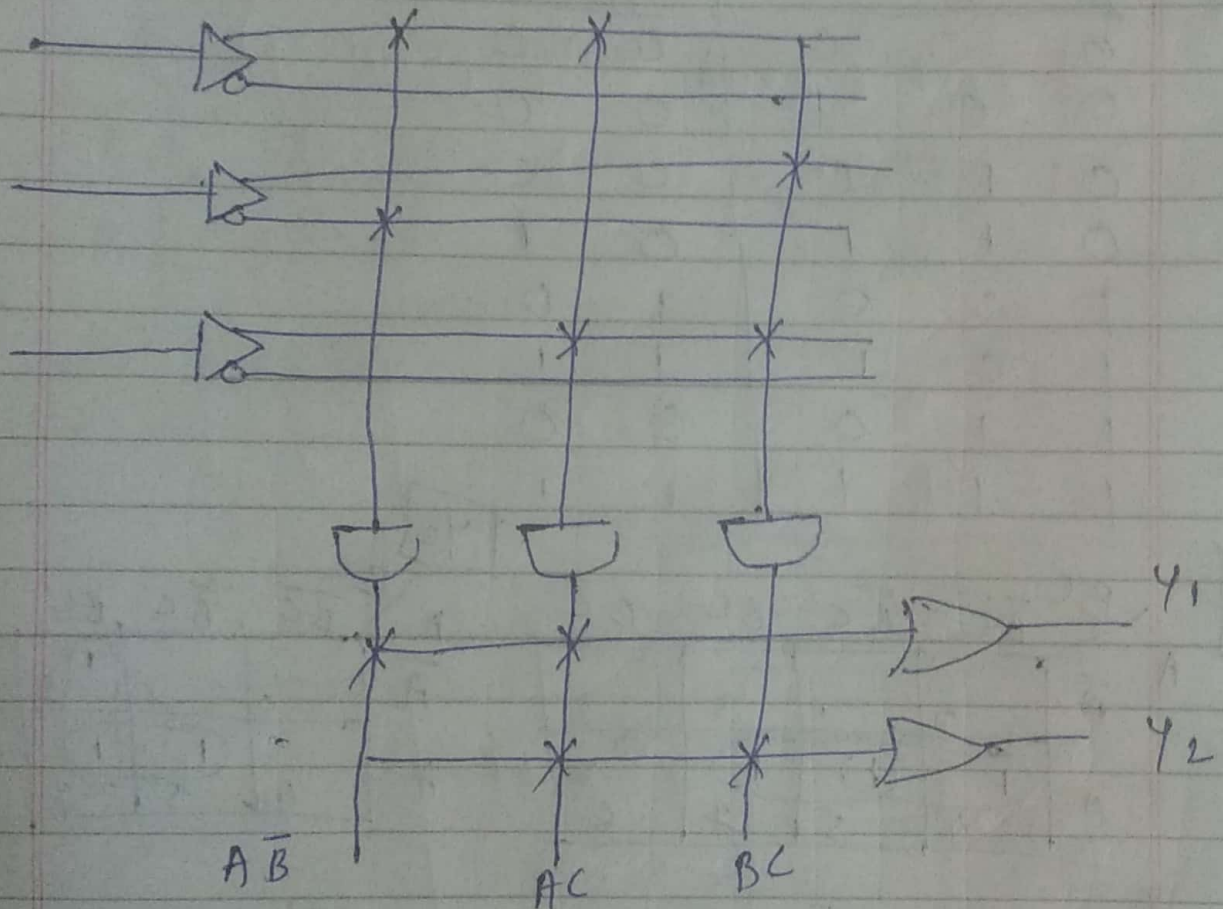
$$y_2 = AC + BC$$

Step 3 No. of i/p Buffer (Variable)



No of prog. AND gate = No. of minterm (non-repeatable) in output Expression

$$(A\bar{B} + AC + BC) = 3$$



No. prog. OR = No. of function = 2 (output)

(PAL) prog. Array Logic

A	B	C	X	Y	Z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	0	0

X

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	$B\overline{C}$	BC
\overline{A}	0	1	1	2
A	4	1	1	6

$$X = \overline{A}B + AC$$

Y

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	$B\overline{C}$	BC
\overline{A}	1	1	3	2
A	4	1	7	6

$$Y = \overline{A}\overline{B} + \overline{B}C$$

Z

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	$B\overline{C}$	BC
\overline{A}	1	0	1	2
A	4	1	7	6

$$Z = \overline{A}\overline{C} + \overline{A}B + A\overline{B}C$$

no. of i/p Buffer = no. of variable **(3)**

No. of AND gates = Max no. of minterms (For each function)

$$3(\text{in } z) * 3(\text{fun}) = \textcircled{9}$$

No. of OR gate = No. of output ^{AND} $\textcircled{3}$

