Practical No. 12

Aim: To study operation of binary and decade counter.

Apparatus: Sigma counters trainer - DCO13, connecting wires

Theory:

Counting is frequently required in digital computers and other digital systems to record the number of events occurring in a specified interval of time. Normally an electronic counter is used for counting the number of pulses coming at the input line in a specified time period. The counter must possess memory since it has to remember its past states. As with other sequential logic circuits counters can be synchronous or asynchronous. As the name suggests, it is a circuit which counts. The main purpose of the counter is to record the number of occurrence of some input. There are many types of counter both binary and decimal. Commonly used counters are

1. Binary Ripple Counter
2. Ring Counter
3. BCD Counter
4. Decade counter
5. Up down Counter
6. Frequency Counter

Binary Ripple Counter

A binary ripple counter is generally using bistable multivibrator circuits so that cache input applied to the counter causes the count to advance or decrease. A basic counter circuit is shown in Figure 1 using two triggered (T-type) flip flop stages. Each clock pulse applied to the T-input causes the stage to toggle. The Q and $\bar{Q}$ output terminals are always logically opposite. If the Q output is logical 1 (SET), the $\bar{Q}$ output is then logical 0. If the Q output is logical 0 (REST), then the $\bar{Q}$ output is logical 1.

The clock input causes the flip flop to toggle or change stage once clock pulse Figure 2 (a) shows the clock input signal and Q output signal. Notice that the circuit used in this case toggles on the trailing edge of the clock signal (when logic signal goes from 1 to 0). Referring back to Figure 1 the Q output of the first stage (called the 2o stage or units position stage) is used here as the toggle input to the second stage (called the 21 or two's position stage). The Q output from the

two successive stage are marked A and B, respectively, to differentiate them. Notice that the $\overline{Q}$ output of each stage is marked with a negative bar over the letter designation, so that whatever logical stage A is at, $\overline{A}$ is the opposite logical state. Since the Q output (A signal) from the first stage triggers the second stage, the second stage changes state only when the Q output of first stage goes from logical 1 to logical 0 as shown in Figure 2(b).

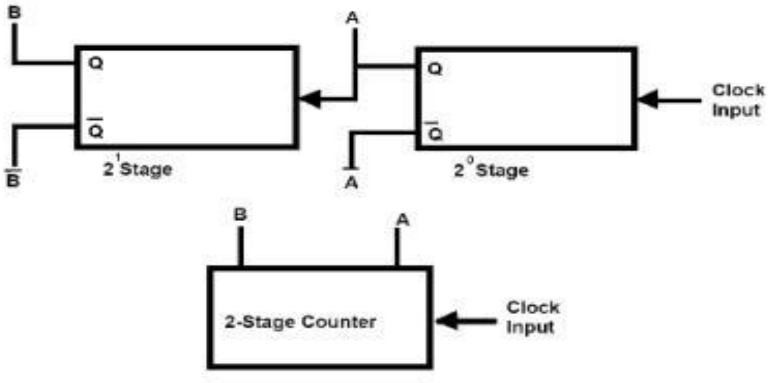


Fig 1: Basic Two-stage binary Counter

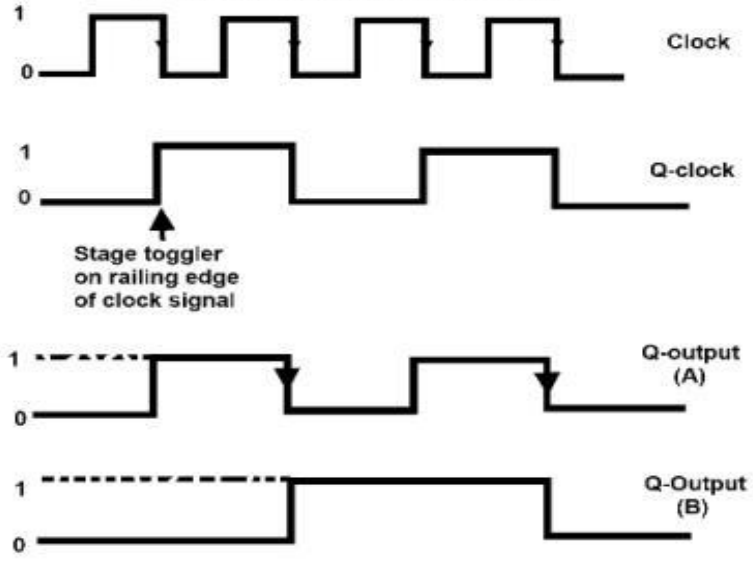


Fig 2: Toggle action of counter stage

Table 1

COUNT FOR 2-STAGE BINARY COUNTER		
Input Pulses	2^n Output (B)	2^n Output (A)
0	0	0
1	0	1
2	1	0
3	1	1
4 or 0	0	0

An arrow is included on the waveform of stage A as a reminder that it triggers stage B only on a trailing edge (1 or 0 logical change). Notice that the output waveform of succeeding stage operates half as fast as its input. To see that this circuit operates as a binary counter a table can be prepared to show the Q output states after each clock pulse is applied. Table 1 shows this operation for the circuit of Figure 1. To see how a counter is made using more stage considers the 4 stage counter of Figure 3. The counter is simply made with the Q output of each state connected as the toggle input to the succeeding state. With four stages the counter cycle will repeat every sixteen clock pulses. In general there are 2n counts with an n-stage counter. For the four stages used here the count goes 24 or 16 steps as a rule, for a binary counter.

Number of counts = N = 2n

Where, n = number of counter stage. A six stage counter n = 6 would be provide a count that repeats every N = 26 = 64 counts. A ten-stage counter (n = 10) would recycle every N = 210 = 1024 counts.

Decade Counter

A decade counter is the one which goes through 10 unique combinations of outputs and then resets as the clock proceeds. We may use some sort of a feedback in a 4-bit binary counter to skip any six of the sixteen possible output states from 0000 to 1111 to get to a decade counter. A decade counter does not necessarily count from 0000 to 1001 it could count as 0000,0001, 0010, 1000, 1001, 1010, 1011, 1110, 1111, 0000, 0001 and so on. Figure 6 shows a decade counter having a binary count that is always equivalent to the input pulse count. The circuit is essentially, a ripple counter which count up to 16. We desire however, a circuit operation in which the count advance from 0 to 9 and then reset to 0 for a new cycle. This reset is a accomplished at the desired count as follows.

With counter REST count = 0000 the counter is ready to stage counter cycle.

Input pulses advance counter in binary sequence up to count of a (count = 1001)

The next count pulse advance the count to 10 count = 1010. A logic NAND gate decodes the count of 10 providing a level change at that time to trigger the one shot unit which then resets all counter stages. Thus, the pulse after the counter is at count = 9, effectively results in the counter going to count = 0.

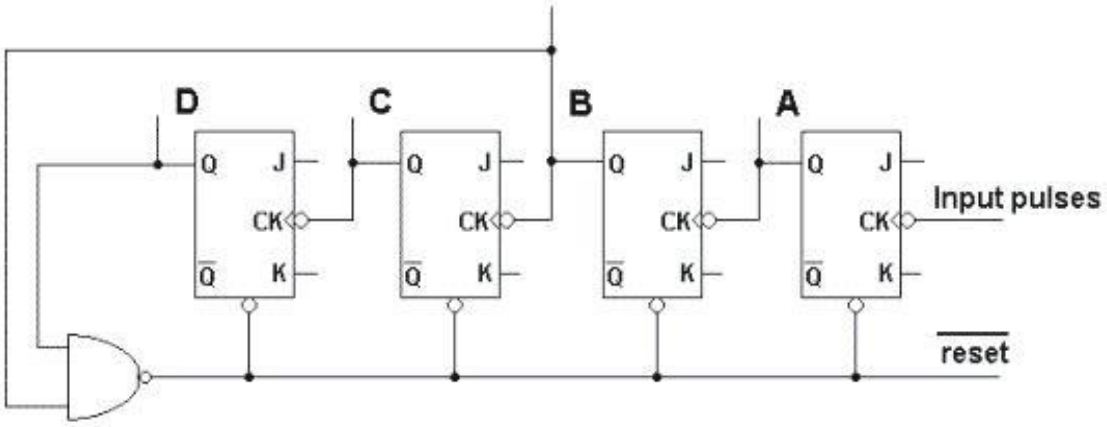


Figure 6: Decade Counter

Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

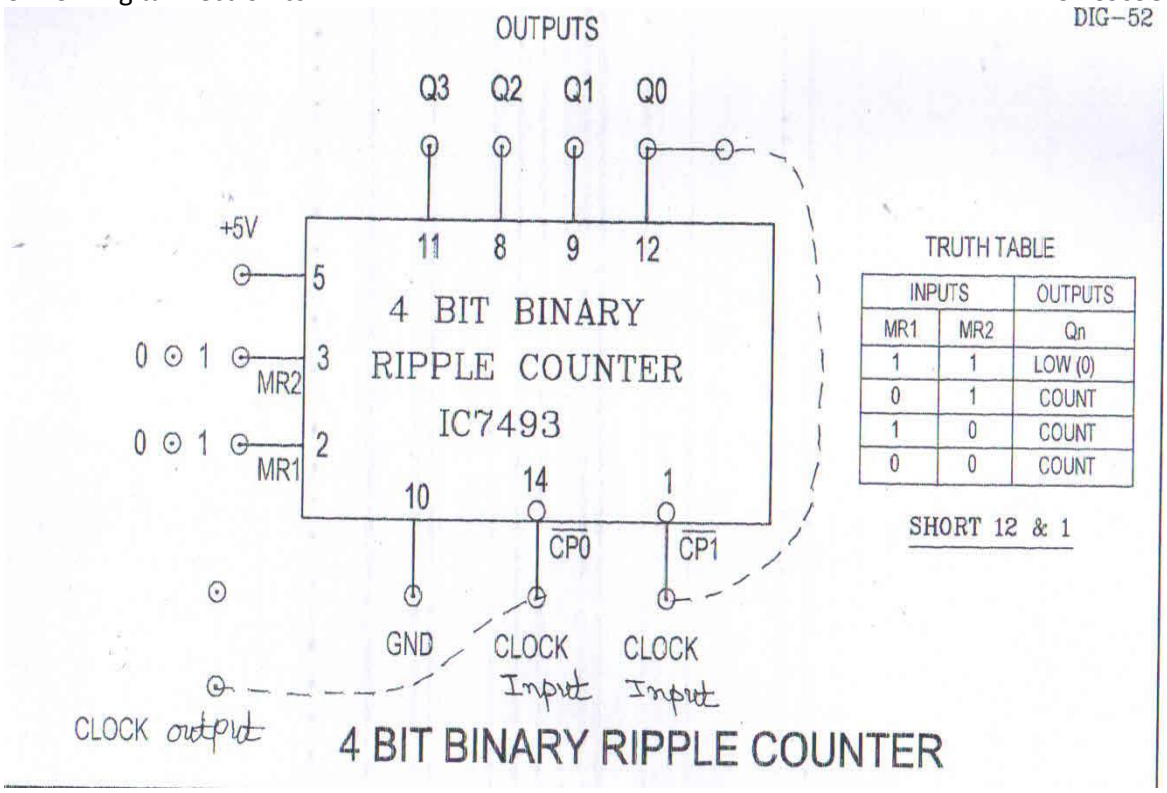
0	0	0	0	0

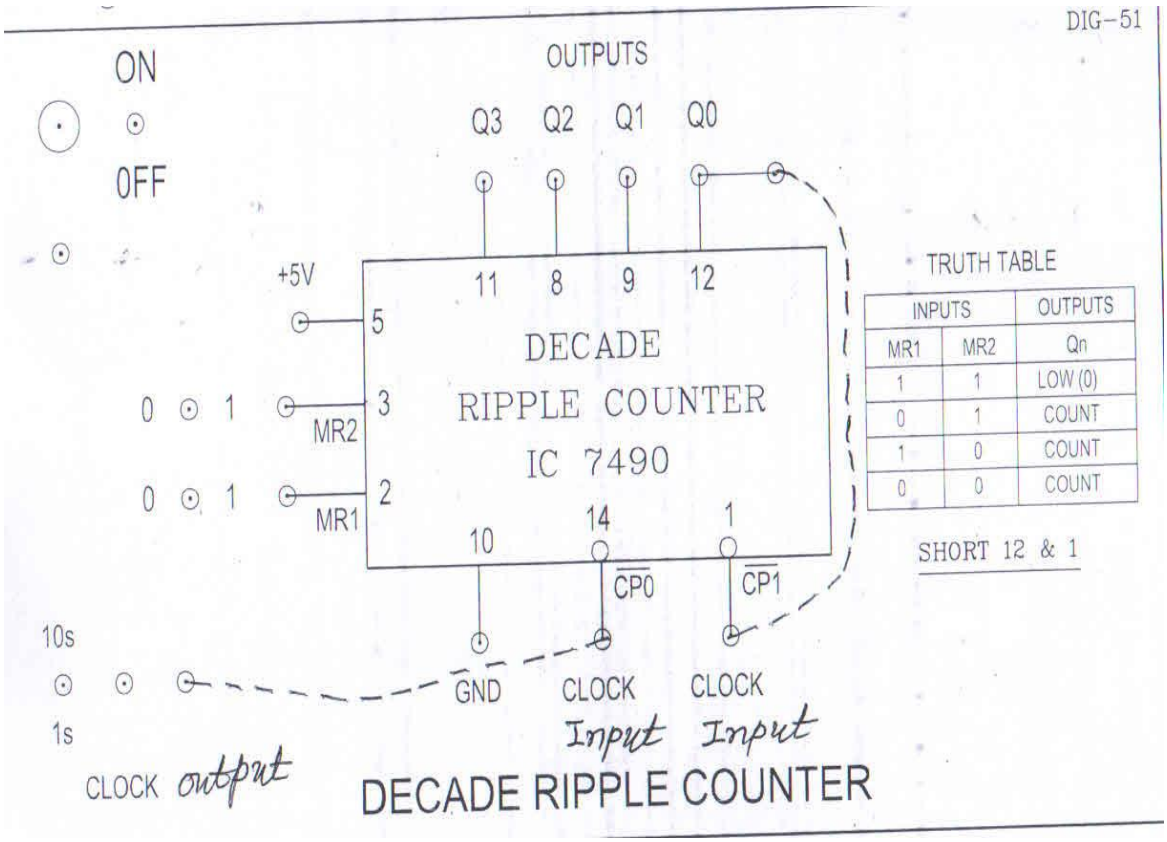
Table provides a count table showing the binary count equivalent to the decimal count of input pulses. The table also shows that the count goes momentarily count from nine (1001) to ten (1010) before resetting to zero (0000). The NAND gate provides an output of 1 until the count reach ten. The count of ten is decoded (or sensed in this case) by using logic inputs that are all 1 at the count of ten. When the count becomes ten the NAND gate output goes to logical 0, providing a 1 to 0 logic change to trigger the one shot unit, which then provides a short pulse to reset all counter stages.

The Q signal is used since it is normally high and goes low during the one shot timing period the flip flop in this circuit being reset by a low signal level (active low clearing). The one shot pulse need only be long enough so that slowest counter stage resets. Actually, at this time only the 21and 23 stage need be reset, but all stages are reset to insure that a new cycle at the count 0000.

Procedure:

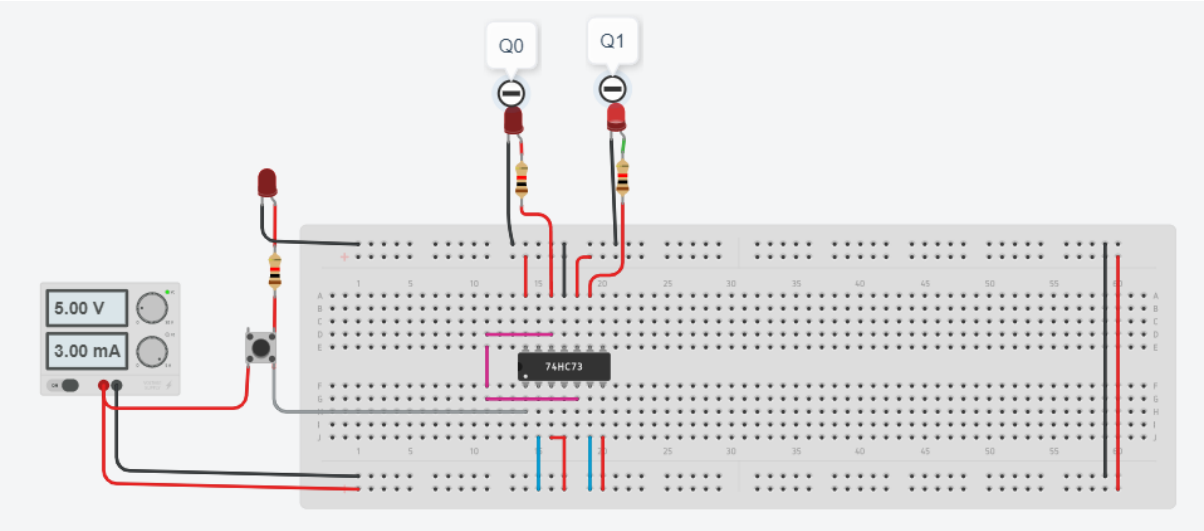
i) Do the connection as per below kit connection diagram for various shift register.
ii) Apply proper input condition and observe the output information of led on/off.
iii) Compare theoretical data with observation and write conclusion.


DIG–52
OUTPUTS
Q3 Q2 Q1 Q0
11 8 9 12
+5V
5
4 BIT BINARY
RIPPLE COUNTER
IC7493
0 ⊙ 1
3
MR2
0 ⊙ 1
2
MR1
10 14 1
CP0
CP1
GND CLOCK CLOCK
Input Input
CLOCK output
TRUTH TABLE
INPUTS OUTPUTS
MR1 MR2 Qn
1 1 LOW (0)
0 1 COUNT
1 0 COUNT
0 0 COUNT
SHORT 12 & 1
4 BIT BINARY RIPPLE COUNTER

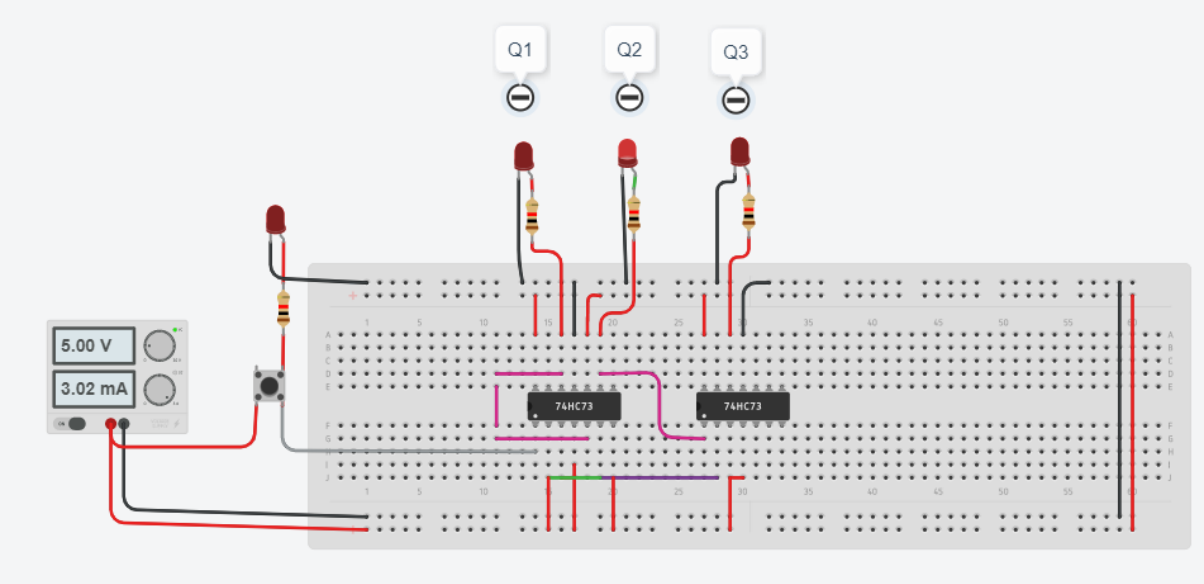

DIG–51
ON
OFF
OUTPUTS
Q3 Q2 Q1 Q0
11 8 9 12
+5V
5
DECADE
RIPPLE COUNTER
IC 7490
0 ⊙ 1
3
MR2
0 ⊙ 1
2
MR1
10 14 1
CP0
CP1
10s
1s
GND CLOCK CLOCK
Input Input
CLOCK output
TRUTH TABLE
INPUTS OUTPUTS
MR1 MR2 Qn
1 1 LOW (0)
0 1 COUNT
1 0 COUNT
0 0 COUNT
SHORT 12 & 1
DECADE RIPPLE COUNTER

TinkerCAD Simulation:

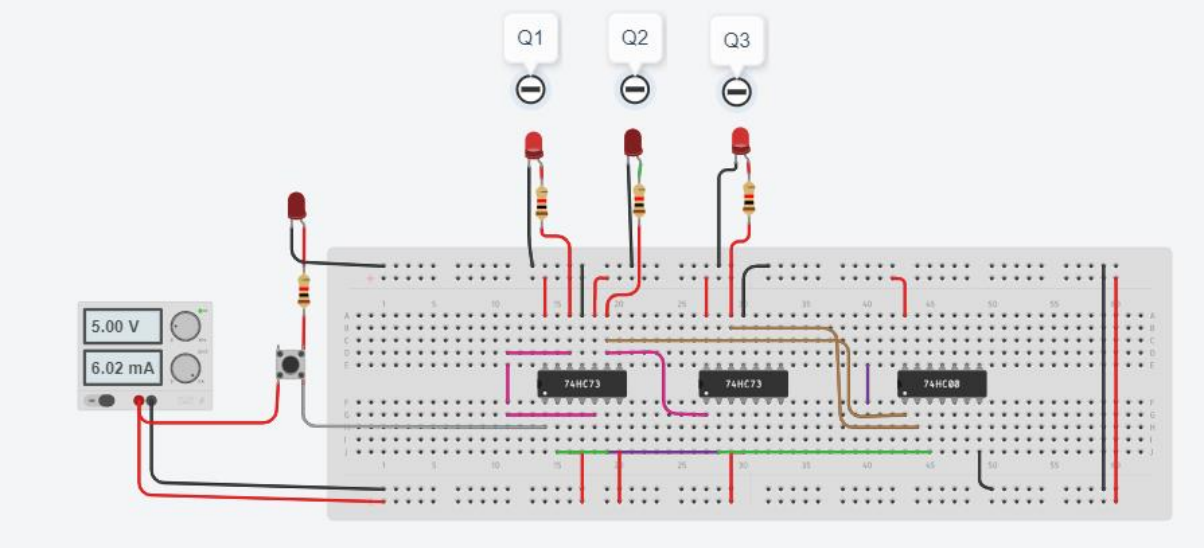
(1) 2-bit ripple counter



(2) 3 Bit Asynchronous Counter



TinkerCAD Simulation:



Design of a Mod-10 Asynchronous Counter using T FFs

- A mod-10 counter has ten stable state 0000,0001,0010,0011,0100, 0101,0110,0111,1000,1001, and when the tenth clock pulse is applied the counter temporarily goes to 1010 states, but immediately reset to 0000 because of the feedback provided
- It is divided-10 counter in the sense that it divides the input clock frequency by 10
- It requires the Four FFs
- Four FFs have sixteen possible states, out of which ten are utilized and the remaining states are invalid
- It is also called as a decade counter

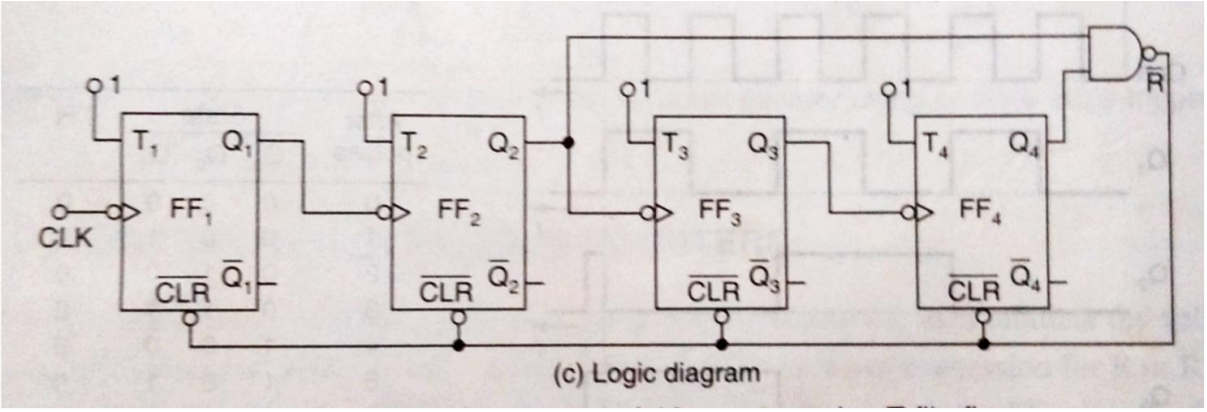
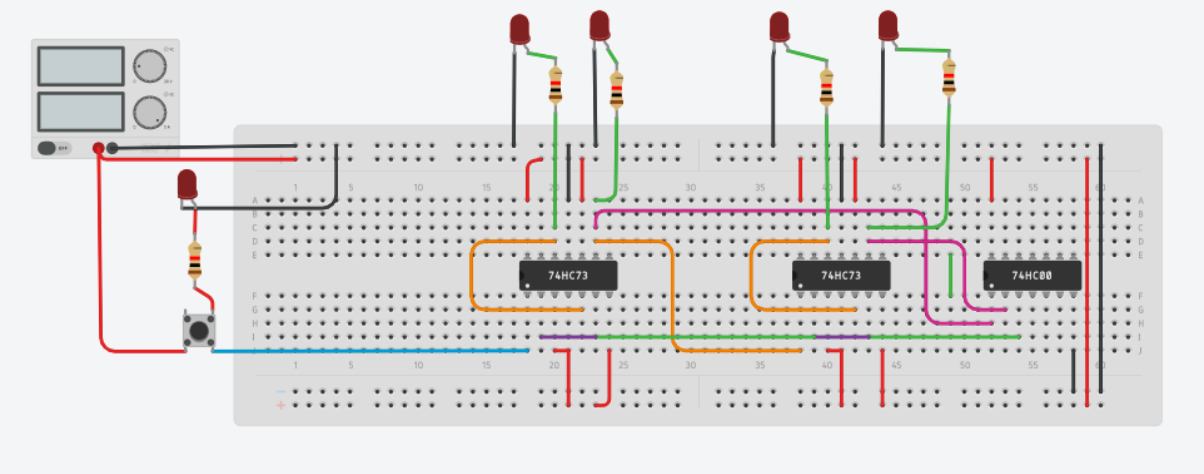


Fig: 3 Mod-10 asynchronouscounters

TinkerCAD Simulation:



Conclusion

in digital logic and computing, a Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit.