CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Third Semester of B. Tech. (CE/IT) Examination

November 2013

CE204 Digital Electronics

Date: 26.11.2013, Tuesday **Time:1.30p.m. To 4.30p.m.** **Maximum Marks: 70**

Instructions:

1. The question paper comprises of two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.

SECTION-I

Q-1	**Attempt the following.**	
1	Convert $(0.513)_{10}$ =( )$_8$	01
2	Represent decimal number 8620 (a) in BCD(b) in Excess-3 code.	01
3	Find 10's Complement of $(935)_{11}$	01
4	Using 2's complement perform $(1010100)_2$-$(1000100)_2$	02
5	Convert hexadecimal 2AC5D to decimal and octal.	02
Q-2(a)	Design Full Adder with two half adder and an OR gate.	04
(b)	Write a short note on Johnson counter with timing sequence.	04
(c)	Find the complement of the following Boolean function and reduce them to minimum number of literals. (i) F=(BC'+A'D)(AB'+CD') (ii) F=[(AB)'A][(AB)'B]	06
	OR	
Q-2 (a)	Design a combinational circuit with four input lines that represent decimal digit in BCD and four output lines that generate the 9's complement of input digit.	06
(b)	Design a combinational circuit to check for odd parity of 3 bits.	04
(c)	Explain the operation of RS flipflop along with its symbol, characteristic table and characteristic equation.	04
Q-3(a)	Determine the prime implicants of the function F (w, x, y, z) = Σ m (1,4,6,7,8,9,10,11,15).	06
(b)	Draw and Explain 4-bit binary ripple counter with JK flipflop.	04
(c)	(i) Implement the Boolean function: F=AB'CD'+A'BCD'+AB'CD+A'BC'D with EX-OR & AND gate. (ii) Show that A⊕B⊕C⊕D= $\sum$m(0,3,5,6,9,10,12,15)	04
	OR	
Q-3 (a)	Explain serial transfer operation from register A to register B.	04
(b)	Implement full adder with a decoder and two OR gate.	04

(c) Built the following function in SOP and POS form using kmap. 06
F (A,B,C,D) = ∑m(0,1,2,5,8,9,10)

SECTION II

Q-4 Do as directed.

1 Design 4x16 decoder with two 3x8 decoder. 02

2 What is the difference between synchronous and ripple counter. 02

3 Draw the logic diagram of 2 to 4 line decoder with enable(E) input 01

4 Show that the dual of the Exclusive-OR is equal to its complement. 02

Q-5 (a) Design a counter with the sequence 0,1,2,4,5,6 and repeat. Use J-K flip-flop. 05

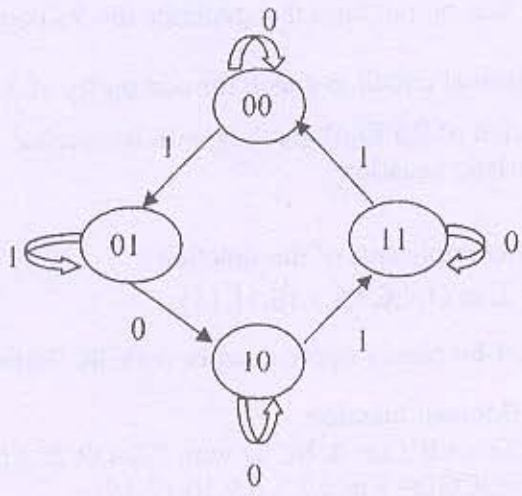
(b) Implement given function with multiplexer: F(A,B,C,D)= Σm(0,1,3,4,8,9,15). 04

(c) Write a short note on magnitude comparator with necessary diagrams. 05

OR

Q-5 (a) A combinational circuit is defined by the functions: 05
$F_1(A,B,C)= \Sigma(0,1,2,4)$
$F_2(A,B,C)= \Sigma(0,5,6,7)$
Implement the boolean equation with PLA.

(b) Design a clocked sequential circuit whose state diagram is given below. The type of flipflop to be used is JK. 07

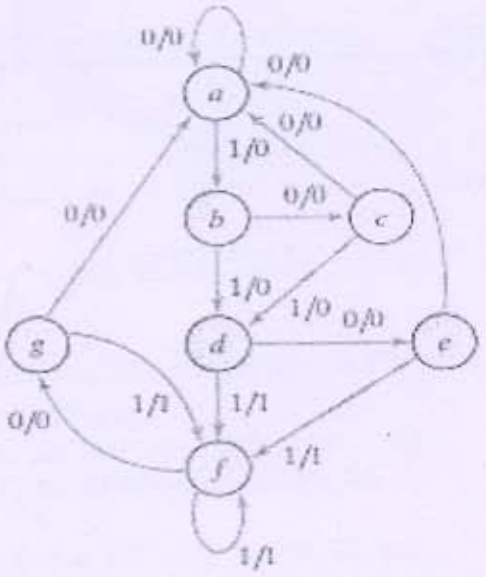


(c) Define: Propagation delay, Power dissipation. 02

Q-6 (a) Design Mod-6 counter using T- flip flop. 06

(b) Give the logic implementation of 32x4 ROM using a decoder of suitable size. 04

(c) Draw state table for the following state diagram and reduce it to possible number of states and redraw the state diagram. 04



OR

Q-6(a) Reduce the following function using kmap and implement it with NAND gates. 05

$F(a,b,c,d) = \sum m(0,1,2,3,5,7,8,9,10,12,13)$

(b) Implement EX-NOR gate using NAND and NOR gate. 05

(c) i) The content of 4 bit shift register is initially 1101.The register is shifted 4 times to right; with the serial input 101101.What is the content of the register after each shift? 04

ii) What is the difference between serial and parallel transfer?