Candidate Seat no…….

CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Third Semester of B. Tech. (CE) Examination

March 2018

CE242 / CE204.01 / CE204 Digital Electronics

Date: 30.03.2018, Friday **Time: 01.30 p.m. To 04.30 p.m.** **Maximum Marks: 70**

Instructions:

1. The question paper comprises two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

SECTION – I

Q - 1	**Answer the following questions.**	**[06]**
a.	Represent Decimal Number 865 into its equivalent BCD	[01]
b.	Convert $(201BC)_{16}$ into its equivalent Decimal & Octal number.	[02]
c.	Draw the Equivalent circuit for the given function USING NAND GATE ONLY, F = A B' + B' C D + A B' D + B' C	[03]
Q – 2	**Answer the following questions. (Any Three)**	**[15]**
a.	Explain Half Adder & Half Subtractor	[05]
b.	Simplify the following Boolean function using K-Map: F (A, B, C, D) = ∑m (1, 3, 7, 11, 15) + d (0, 2, 5)	[05]
c.	Implement the following Boolean function using an 8:1 multiplexer. (Use A as input) F(A, B, C, D) = ∑m (0, 1, 3, 4, 8, 9, 15)	[05]
d.	Implement the following functions using ROM: F1(A1, A0) = ∑ (1, 2, 3) F2(A1, A0) = ∑ (0, 2)	[05]
e.	Design 5 X 32 Decoder Using 3 X 8 and 2 X 4 Decoders	[05]
Q - 3	**Answer the following questions. (Any two)**	**[14]**
a.	Design a circuit for BCD to excess-3 code conversion	[07]
b.	Simplify the following function by using the Tabulation Method: F(A, B, C, D) = ∑m (0, 1, 2, 8, 10, 11, 14, 15)	[07]
c.	Implement the following functions using PLA F0(X, Y, Z) = ∑m (0, 2, 3, 4) F1(X, Y, Z) = ∑m (0, 1, 4) F2(X, Y, Z) = ∑m (0, 1, 2, 3)	[07]
d.	Why NAND & NOR gates are called as Universal Gates? Explain NAND & NOR as Universal Gates	[07]

SECTION – II

Q - 4	**Answer the following questions.**	**[06]**
a.	Define: Sequential Circuit	[01]
b.	Define: Propagation Delay, Noise Margin	[02]
c.	Demonstrate by means of truth tables the validity of the Distributive Law * over +	[03]

Q –5 Answer the following questions. (Any Three) **[15]**

a. Express the following function as a sum of min-terms and product of max-terms: [05]
F(A, B, C, D) = B'D + A'D + BD

b. Explain clocked R-S flip flop with symbol, logic diagram and characteristic table [05]

c. Draw the State Diagram for the following State Table. Also reduce the numbers of the states of the State Table. Tabulate reduced State Table & Draw the reduced State Diagram of it. [05]

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
A	D	C	0	0
B	G	A	1	0
C	F	B	1	1
D	G	A	1	0
E	F	B	0	0
F	F	E	0	0
G	D	C	0	0
H	G	H	0	1

d. Design 3-bit binary counter using D Flip-Flip [5]

e. A sequential circuit with Two D flip-flops, A and B; Two Inputs X & Y; and One Output Z, specified by the following Next State & Output Equations: [5]

$A(t+1) = X'Y + XA$

$B(t+1) = A$

$Z = B$

- Derive the State Table
- Draw the logic diagram of the circuit

Q – 6 Answer the following questions. (Any Two) **[14]**

a. Explain 4-bit Bidirectional Shift Register with Parallel load with Diagram [07]

b. Explain BCD Ripple Counter using J-K flip flops and state diagram. [07]

c. Design a Decimal Counter using J-K Flip-Flop [07]

d. Design a clocked sequential circuit for the given state diagram using T Flip-Flop [07]