Seat no._____

CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Third semester of B. Tech (IT) Examination

March-April 2018

IT241 Digital Electronics

Date: 30.03.2018, Friday **Time: 1.30 p.m. To 04.30 p.m.** **Maximum Marks: 70**

Instructions:

1. The question paper comprises two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

SECTION Ⅰ

Q - 1 **Do as directed.** [8]

1) Given function F=A⊕B' ⊕C ⊕D' ⊕E' is equivalent to Ex-NOR function. State **TRUE** or **FALSE**
2) Write Dual of boolean equation: X + XY = X
3) Boolean equation AB(A+B)=_____
4) If boolean function X ⊕Y=1 and Y=1 then what is the value of X ?
5) Which one of the following is universal gate?
   a) Ex-OR gate c) NAND gate
   b) AND gate d) NOT gate
6) How many inputs does a full subtractor has?
   a) 1 c) 3
   b) 2 d) 4
7) In a multiplexer the output depends on its_____
   a) Data inputs c) Select outputs
   b) Select inputs d) None of the Mentioned
8) Ex-OR operation is associative. State **TRUE** or **FALSE**.

Q - 2 **Do as directed. (Any Three)** [12]

1) Implement ex-or function using NAND gates only. Draw circuit diagram of the same.
2) Discuss design procedure of full adder circuit in detail. Also draw neat and clean logic diagram of the same.
3) Reduce boolean function F = BC + AC' + AB + BCD to four literals.
4) Draw neat and clean logic diagram of 2 x 4 decoder.

Q - 3 **Do as directed.** [15]

1) Design a combinational circuits to convert BCD code to Excess-3 code.
2) Simplify boolean function F(A,B,C,D)=(m0,m2,m5,m6,m8,m10) using K-Map.
3) Implement function F(A,B,C) = (m1,m3,m5,m6) using multiplexer.

SECTION Ⅱ

Q - 4 **Do as directed.** [9]

1) Draw Block diagram of sequential circuit.
2) If Current state of a T-FlipFlop is 1 and input is 1 then next state will also be 1. State **TRUE** or **FALSE**.
3) Represent $(12)_{10}$ in excess-3 encoding.
4) Represent $(15)_{10}$ in BCD encoding.

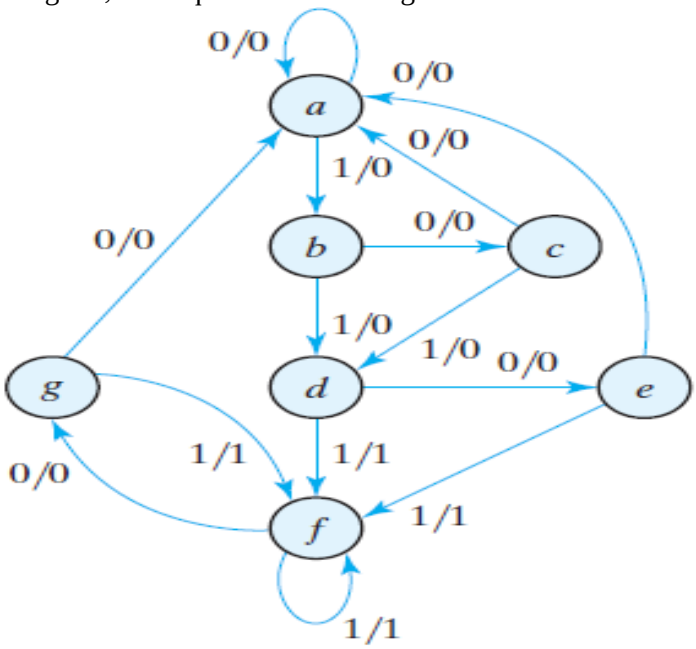
5) If SR-FlipFlop is given then we can construct a D-FlipFlop by just adding one NOT gate to it. state **TRUE** or **FALSE**.
6) Draw state table of T-FlipFlop
7) Which input combination of SR-FlipFlop is invalid?
   a) 00 c) 10
   b) 01 d) 11
8) How is a J-K flip-flop made to toggle?
   a) J=0, K=0 c) J=0, K=1
   b) J=1, K=0 d) J=1, K=1
9) How many flip-flops are required to make a MOD-32 binary counter?
   a) 3 c) 5
   b) 4 d) 6

Q - 5 **Do as directed. (Any three)** [12]

1) Discuss design procedure of SR-FlipFlop in detail. Also draw digital circuit of same. Why one of its input combinations are not valid?
2) $M=(1010100)_2$ and $N=(1000100)_2$. Perform M - N with 2's complement representation.
3) What is Asynchronous and synchronous sequential circuits?
4) Draw logic diagram of Johnson counter.

Q - 6 **Do as directed.(Any two)** [14]

1) For given state diagram, find equivalent state diagram with minimal states.



2) Explain design procedure of binary up counter to count sequence 0 to 3. Also draw all necessary diagrams.
3) Draw a circuit of 4-bit registers with parallel load.

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