Practical No. 8

Aim: To implement 4-bit magnitude comparator.

Apparatus: 4 bit magnitude comparator IC (74LS85), Connecting wires, Bread Board, Power supply, LED, DMM.

Theory:

Definition

A magnitude comparator is a combinational circuit that compares two numbers A & B to determine whether:

- A > B, or
- A = B, or
- A < B

Inputs

First *n*-bit number A

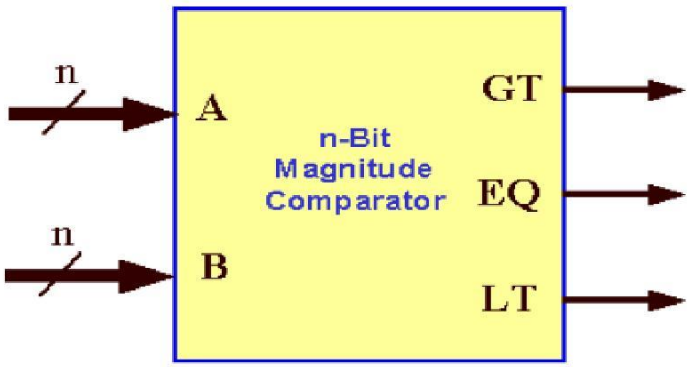
Second *n*-bit number B

Outputs

3 output signals (GT, EQ, LT), where:

1. GT = 1 IFF A > B
2. EQ = 1 IFF A = B
3. LT = 1 IFF A < B

Note: *Exactly One* of these 3 outputs equals 1, while the other 2 outputs are 0`s



4-bit magnitude comparator

Inputs: 8-bits (A ⇒ 4-bits , B ⇒ 4-bits)

A and B are two 4-bit numbers

- Let $A = A_3A_2A_1A_0$, and
- Let $B = B_3B_2B_1B_0$
- Inputs have 2^8 (*256*) possible combinations
- Not easy to design using conventional techniques

Design of the EQ output (A = B) in 4-bit magnitude comparator

Define $X_i = (A_i B_i) + (A_i' B_i')$

Thus $X_i = 1$ IFF $A_i = B_i$ $\forall i = 0, 1, 2$ and 3
$X_i = 0$ IFF $A_i \neq B_i$

Condition for A= B
EQ=1 (i.e., *A*=*B*) IFF

1. $A_3=B_3 \rightarrow (X_3 = 1)$, and
2. $A_2=B_2 \rightarrow (X_2 = 1)$, and
3. $A_1=B_1 \rightarrow (X_1 = 1)$, and
4. $A_0=B_0 \rightarrow (X_0 = 1)$.

Thus, *EQ*=1 IFF $X_3 X_2 X_1 X_0 = 1$. In other words, $EQ = X_3 X_2 X_1 X_0$

Design of the GT output (A > B) 4-bit magnitude comparator

If $A_3 > B_3$, then A > B (GT=1) irrespective of the relative values of the other bits of A & B. Consider, for example, A = 1000 and B = 0111 where A > B.
This can be stated as GT=1 if $\mathbf{A_3 B_3'} = 1$

If $A_3 = B_3$ ($X_3 = 1$), we compare the next significant pair of bits (A_2 & B_2).

If $A_2 > B_2$ then A > B (GT=1) irrespective of the relative values of the other bits of A & B. Consider, for example, A = 0100 and B = 0011 where A > B.
This can be stated as GT=1 if $\mathbf{X_3 A_2 B_2'} = 1$

If $A_3 = B_3$ ($X_3 = 1$) and $A_2 = B_2$ ($X_2 = 1$), we compare the next significant pair of bits (A_1 & B_1).

If $A_1 > B_1$ then A > B (GT=1) irrespective of the relative values of the remaining bits A_0 & B_0. Consider, for example, A = 0010 and B = 0001 where A > B
This can be stated as GT=1 if $\mathbf{X_3 X_2 A_1 B_1'} = 1$

If $A_3 = B_3$ ($X_3 = 1$) and $A_2 = B_2$ ($X_2 = 1$) and $A_1 = B_1$ ($X_1 = 1$), we compare the next pair of bits (A_0 & B_0).
If $A_0 > B_0$ then A > B (GT=1). This can be stated as GT=1 if $\mathbf{X_3 X_2 X_1 A_0 B_0'} = 1$

To summarize, GT =1 (A > B) IFF:

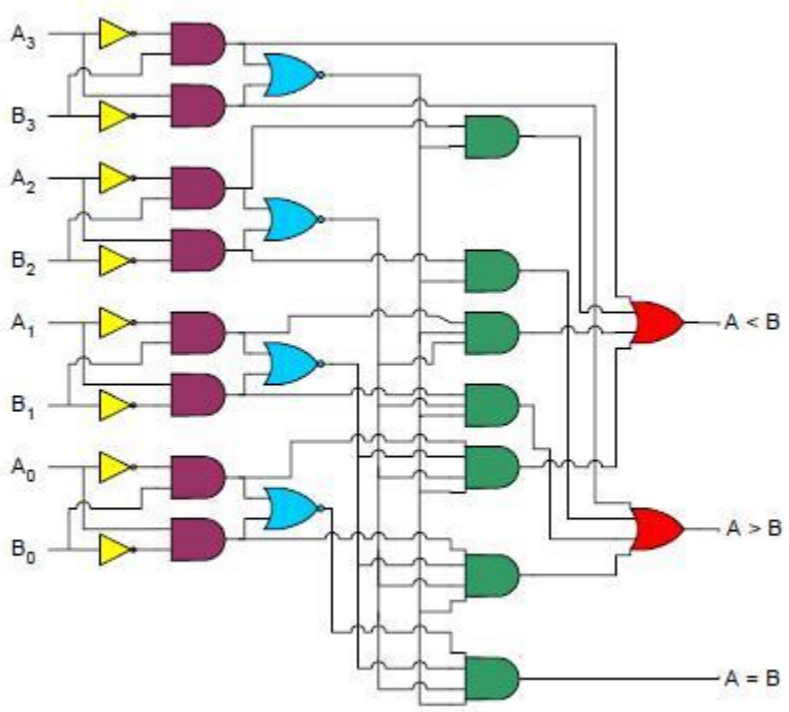
1. $\mathbf{A_3 B_3'} = 1$, or
2. $\mathbf{X_3 A_2 B_2'} = 1$, or
3. $\mathbf{X_3 X_2 A_1 B_1'} = 1$, or
4. $\mathbf{X_3 X_2 X_1 A_0 B_0'} = 1$

In other words, $\mathbf{GT = A_3 B_3' + X_3 A_2 B_2' + X_3 X_2 A_1 B_1' + X_3 X_2 X_1 A_0 B_0'}$

Design of the LT output (A < B) 4-bit magnitude comparator

In the same manner as above, we can derive the expression of the LT (A < B) output
$\mathbf{LT = B_3 A_3' + X_3 B_2 A_2' + X_3 X_2 B_1 A_1' + X_3 X_2 X_1 B_0 A_0'}$
The gate implementation of the three output variables (EQ, GT & LT) is shown in the figure below.

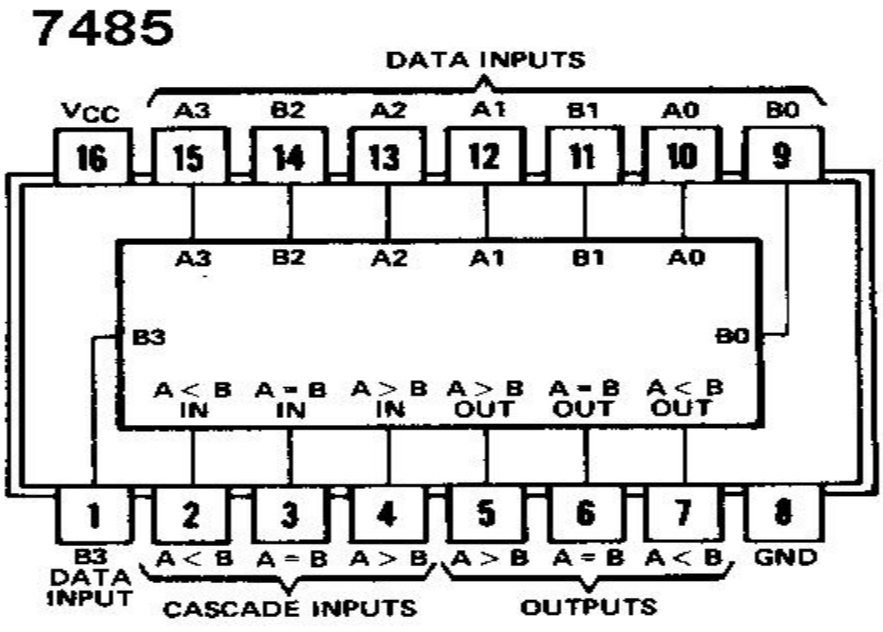
Logic Diagram:

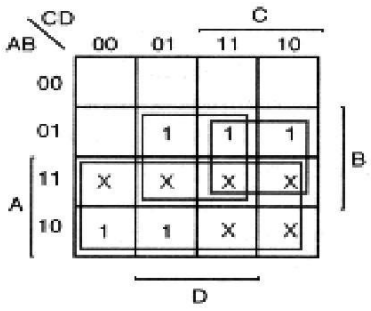


Procedure:

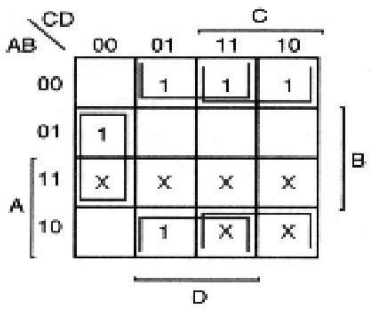
i) Do the connection as per below pin diagram for various input data or 4 bit number.
ii) Apply proper input condition and observe the output information of led on/off.
iii) Compare theoretical data with observation and write conclusion.

Pin Diagram:

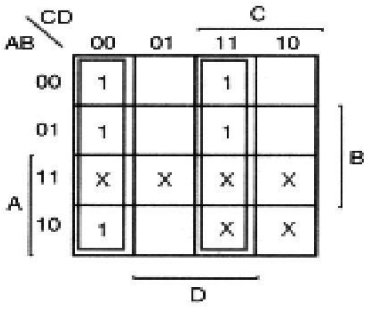




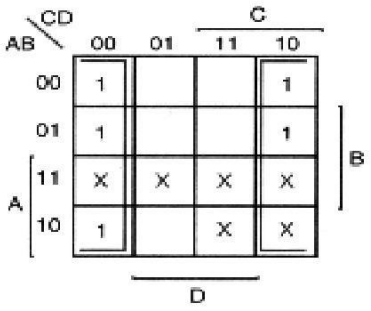
$W = A + BC + BD$



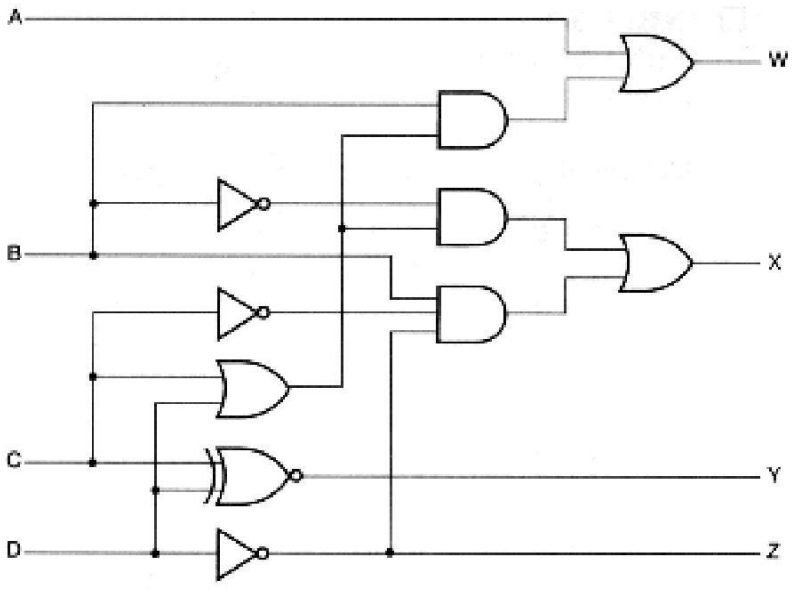
$X = \overline{B}C + \overline{B}D + B\overline{C}\overline{D}$



$Y = CD + \overline{C}\,\overline{D}$



$Z = \overline{D}$



BCD to Excess-3 Code conversion logic diagram

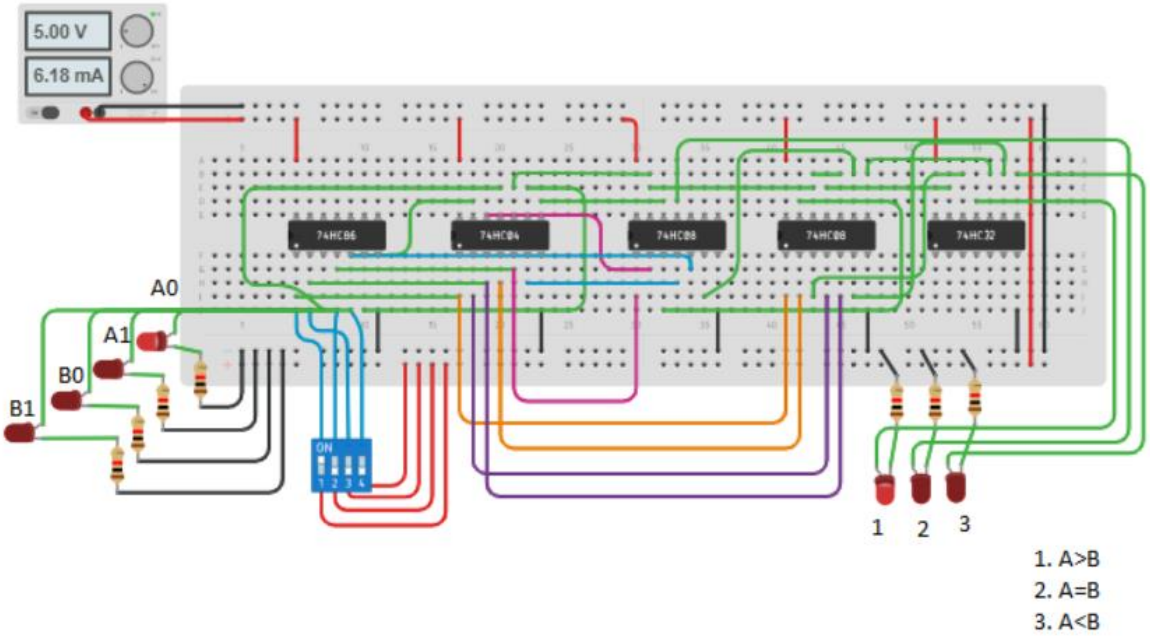
Procedure:

i) Do the connection as per Combinational logic diagram for various input data.
ii) Apply proper input condition and observe the output information of using DMM.
Compare theoretical data with observation and write conclusion

Inputs					Outputs		
A_1	A_0	B_1	B_0		G	E	L
0	0	0	0		0	1	0
0	0	0	1		0	0	1
0	0	1	0		0	0	1
0	0	1	1		0	0	1
0	1	0	0		1	0	0
0	1	0	1		0	1	0
0	1	1	0		0	0	1
0	1	1	1		0	0	1
1	0	0	0		1	0	0
1	0	0	1		1	0	0
1	0	1	0		0	1	0
1	0	1	1		0	0	1
1	1	0	0		1	0	0
1	1	0	1		1	0	0
1	1	1	0		1	0	0
1	1	1	1		0	1	0

CIRCUIT DIAGRAMS:

2- Bit Magnitude comparator



CONCLUSION:

Comparators compares an input signal with a reference voltage and has as a result a logic stage, which indicates whether the signal is lower or higher.