PRACTICAL 5

AIM: To study and verify the design of half adder and half subtractor combinational circuit.

APPARATUS:

Logic gates, slide switches, resistors, L.E.D (red and green), wires, bread board, power supply.

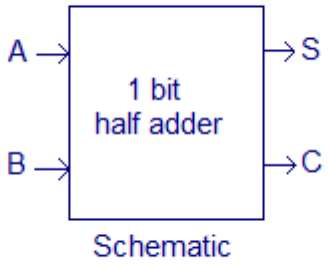
THEORY:

(I) HALF ADDER

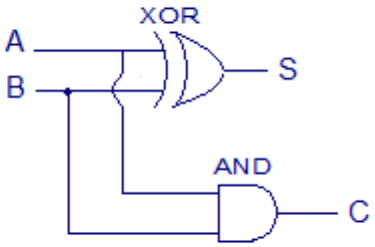
Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder. The truth table, schematic representation and XOR//AND realization of a half adder are shown in the figure below.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic



Realization

K-MAP FOR SUM: SUM = A'B+AB', CARRY = A.B

SUM

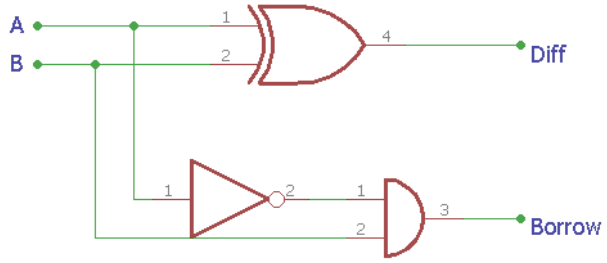
A \ B	0	1
0		1
1	1	

CARRY

A \ B	0	1
0		1
1	1	

(II) HALF SUBTRACTOR

So a Half-Subtractor logical circuit can be made by combining two gates Ex-OR and NAND gate.



Input A	Input B	DIFF(XOR out)	Borrow(NAND out)
0	0	0	0
1	0	1	0
0	1	1	1
1	1	0	0

This is the construction of Half-Subtractor circuit, as we can see two gates are combined and the same input A and B are provided in both gates and we get the Diff output across EX-OR gate and the Borrow bit across NAND gate.

DIFF = A XOR B **BORROW = A' AND B (A'.B)**

K-MAP FOR DIFFERENCE:

DIFFERENCE

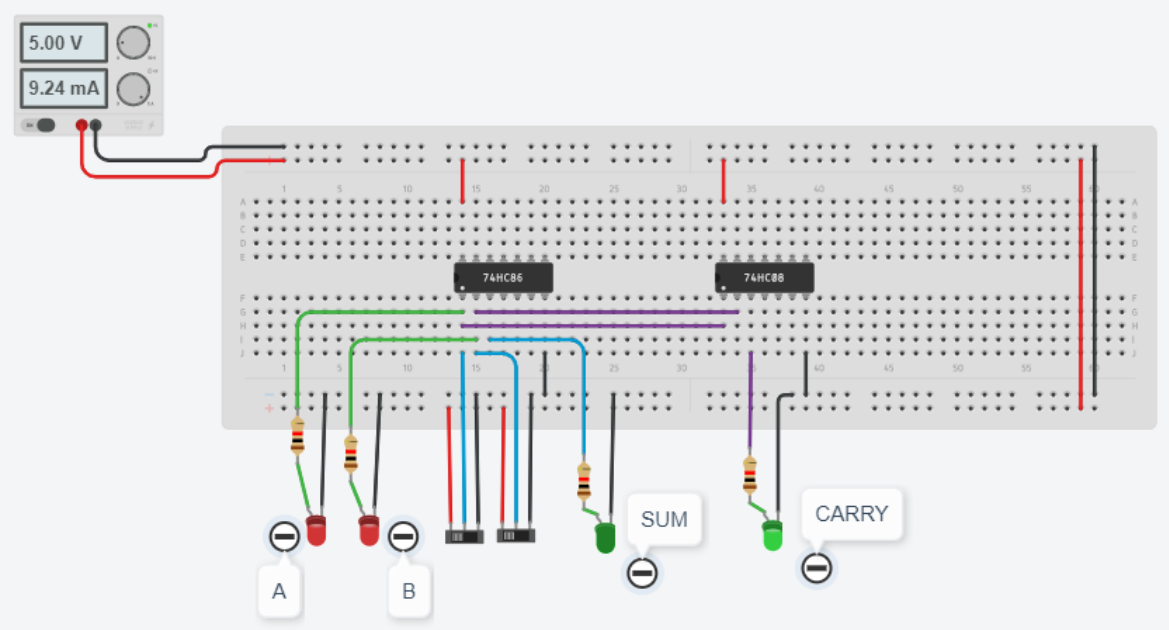
A \ B	0	1
0		1
1	1	

BORROW

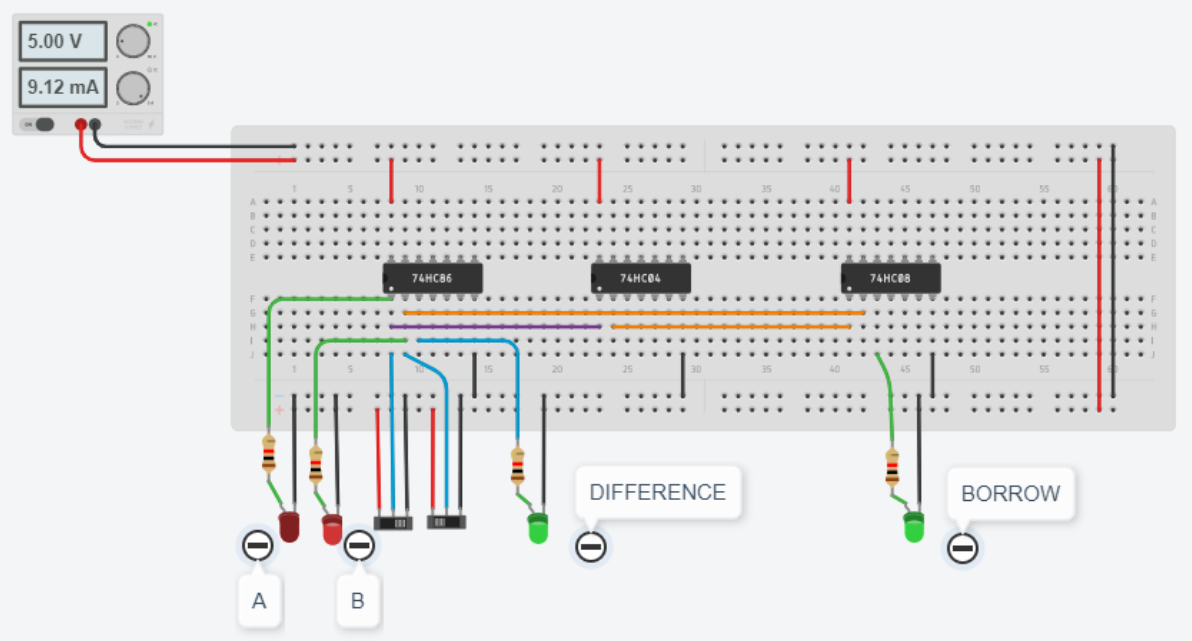
A \ B	0	1
0		1
1		

CIRCUIT DIAGRAMS:

(I) HALF ADDER



(II) HALF SUBTRACTOR



CONCLUSION:

Binary Addition- Half Adder. Summarize the circuit requirements to add 2 binary digits. Circuit simulates the addition of two digits in the binary system. The XOR gate makes the binary sum of the two inputs mean while the AND gate makes the carry of the outputs.

A half subtractor is a logical circuit that performs a subtraction operation on two binary digits. The half subtractor produces a sum and a borrow bit for the next stage.