Ø0.5μm 15/25V BCD

0.5 Micron Modular BCD Technology for Analog Product Applications

l Overview

BCD050 is CSMC's standard BCD process platform. In addition to the double poly, dual gate, triple metal 0.5 micron drawn gate length process for digital applications, process modules are available for five volt drain-source and isolated transistors, double-poly and MIM capacitor and high resistance poly resistors. MOS Transistors are available. All main modules are comparable in Design Rules and Transistor Performance with other state of the 0.5μm CMOS Processes. Comprehensive design rules, accurate SPICE models, analog and digital libraries, IP's and development kits support the process on platforms supplied by the major EDA tool vendors.

l Key Features

- ü - 5V logic layout & performance compatible with the industry standard
- ü - Modular concept (HR/ Zener / BJT / JFET / Schottky/ depletion MOS / Special require)
- ü - 5V/15v/17V/25v/40v/60v/200V
- ü - Double poly capacitor
- ü - High value poly resistor
- ü - Epi process for isolated devices
- ü - I/O cell library with 4kV HBM ESD protection levels
- ü - Provide high temperature models - (MOS, BJT, RES, CAP)

l Applications

- ü - DC-DC, Display Driver, LED Driver, Class D

l Quality Assurance

CSMC continue to improve the process quality and reliability and to provide competent support to the customers. CSMC follow APQP procedures developed process technology. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, ISO TS 16949 and other standards.

l Deliverables

- ü PCM tested wafers
- ü Optional production services: wafer probe sort
- ü Optional production services(turn key): packages and final sort
- ü Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Service (MLM)
- ü Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

CSMC Technologies Corporation
www.csmc.com.cn Tel:86-510-88118888 Fax:86-510-88115883
Headquarters: 8 Xinzhou Road, Wuxi,Jiangsu,China

Power IC -0.5μm 15/25V BCD

Process Option list

CSMC 0.5um BCD Process family			
	Layer	Description	Typical primitive devices application
Base line	15	BCD 20V process base line (2P1M)	5V N/PMOS, BJT(VPNP/LPNP/VNPN),20V LDMOS, HVPMOS, PIP(orONO) Cap.
	16	BCD 40V process base line (2P1M)	5V N/PMOS, BJT(VPNP/LPNP/VNPN),40V LDMOS, HVPMOS, PIP(orONO) Cap.
	17	BCD 60V process base line (2P1M)	5V N/PMOS, BJT(VPNP/LPNP/VNPN),60V LDMOS, HVPMOS, PIP(orONO) Cap.
The main module can be combined with one or more of the following additional modules;			
ESD	1	ESD implant module specific implant for ESD protection.	20V ESD-NMOS ESD protection with improved ESD robustness
HV	1	Define LDMOS and HVMOS gate area for thick oxide	LDNMOS (Vg=20V), HVNMOS (Vg=20V), HVPMOS (Vg=18V),
Zener	1	For Zener diode use.	zener diode (zener beakdown voltage tuning)
Schottky	1	For Schottky diode use.	schottky diode
NF	1	For 40V HVPMOS implant module	extended high voltage PMOS (40V)
NLDD	1	NLDD implant module	extended NLDD resistos , 5V NMOS
IM	1	For High resistance 1K/2K use. (choose one of the two) For Low TC resistance use.	poly1 resistors (high resistive and/or low TC) for analog applications
P-base	1	For P-base resistance and high performance BJT use	high HFE VNPN bipolars, extended JFET(pitch off 7.8V), extended P-base resistors.
HVN	1	For Symmetric HV NMOS use.	thin gate HVNMOS(20V) ,thin gate HVNMOS(40V) medium voltage NMOS (9V)
JFET	1	For JFET option device use.	JFET optical applications (pinch off tuning)

Thick metal		25K top metal for high power	
Metal fuse		Metal fuse	
poly Fuse		poly fuse	
ONO cap.		for high voltage breakdown or high	

Library Cells

Tech. Node	Process	Available Libraries
0.5um	Mixed-Signal	MS Standard Cell Library, Inline PAD Cell Library, High Density OP Inline PAD Cell Library
	BCD	BCD Standard Cell Library, Inline PAD Cell Library
	High Voltage	HV Standard Cell Library, Inline PAD Cell Library

For the Detailed information can reference design service web.

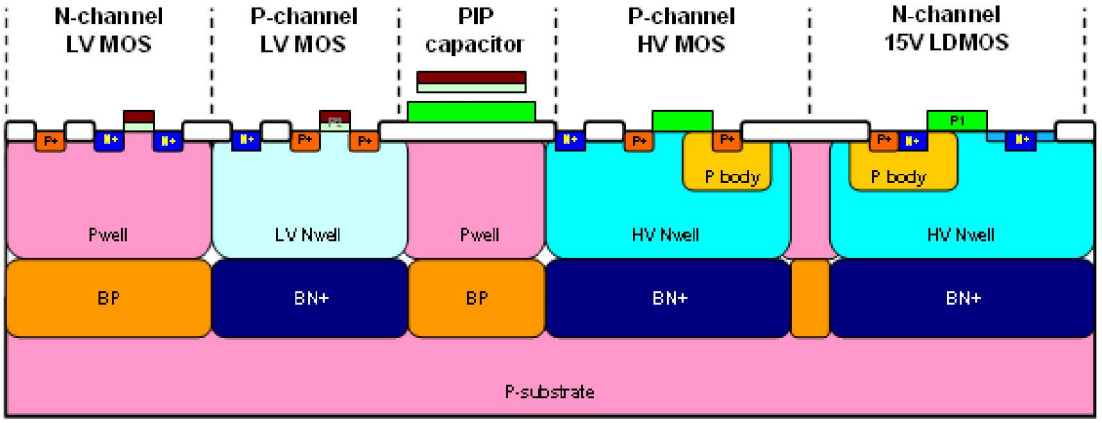
PDKs at CSMC

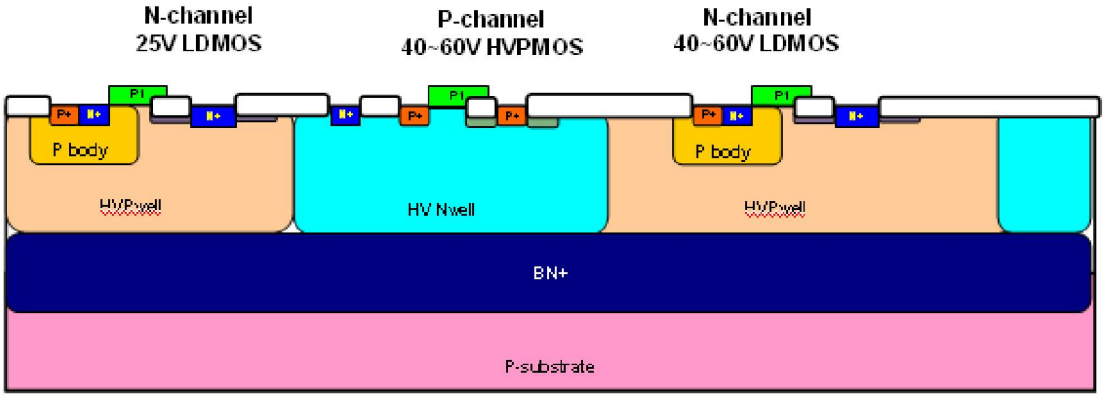
Tech. Node	Available PDKs
0.5um	Mixed-Signal, Mixed-Signal High Ca, BCD, High Voltage, 0.5um FE 0.35um BE, 0.5um FE 0.35um BE High Ca

IP Alliance

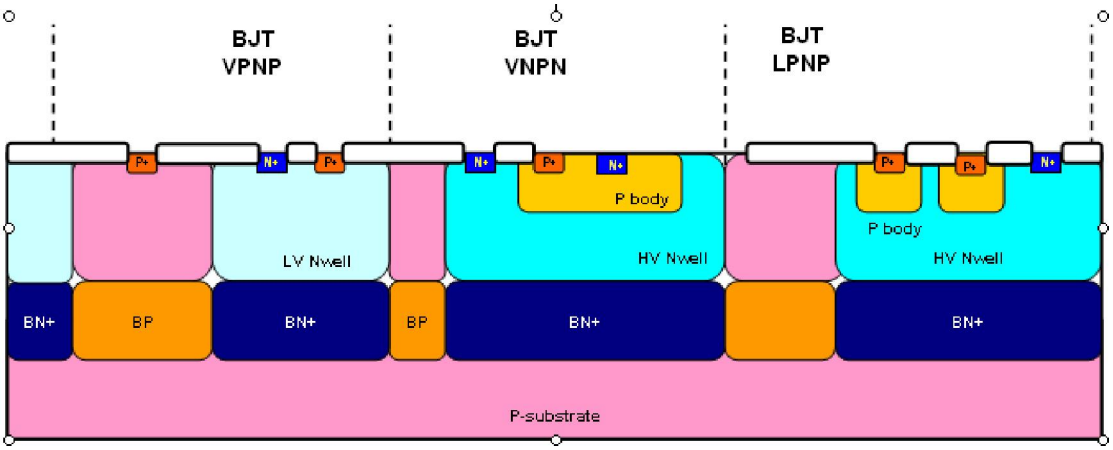
Tech. Node	Process	Available Libraries
0.5um	BCD	OTP

Schematic Cross Sections





Schematic Cross Sections (Continue)



Power IC -0.5μm 15/25V BCD

Basic Design Rules

CSMC 0.5um BCD			
Parameter	Width(μm)	Space(μm)	Pitch(μm)
Active	0.6	0.8	1.4
Poly 1 resistor	1	1	2.0
Poly 2 (NMOS/PMOS)	0.6 / 0.7	0.5	1.1/1.2
Poly 2 resistor	0.5	0.5	1.0
Contact	0.5	0.5	1.0
M1	0.6	0.6	1.2
Via	0.55	0.6	1.05
M2	0.7	0.65	1.35
Via2	0.6	0.6	1.20
Top Metal (Thin / Thick)	0.8 / 1.2	0.8 / 1.2	1.6 / 2.4

Key Device Parameters

MOS Transistor						
Device	Device Name	VT [V]	IDS@VGS [uA/um@V]	BVDSS [V]	Max.[VDS] [V]	Max.[VGS] [V]
N-channel 5V nominal MOSFET.	NMOS 5V	0.75	450@5	13	6	6
N-channel 5V isolation MOSFET.	NMOS 5V	0.75	450@5	13	6	6
P-channel 5V nominal MOSFET.	PMOS 5V	-0.85	225@5	-14	6	6
N-channel 9V norminal MOSFET.	NMOS 9V	1.1	450@5	18	9	9
N-channel 20V/20V asymmetry MOSFET.	LDMOS 20V	1.8	600@18	24	20	20
N-channel 20V/20V symmetric MOSFET	HVNMOS 20V	0.8	315@18	38	20	20
P-channel 20V/20V asymmetry MOSFET.	HVPMOS 20V	-1.35	450@18	-24	20	20
P-channel 20V/20V symmetry MOSFET.	HVPMOS 20V	-1.38	320@18	-24	20	20
N-channel 20V/5V asymmetry MOSFET.	LDMOS 20V	0.83	275@5	24	15	6
N-channel 20V/5V symmetric MOSFET	HVNMOS 20V	1	--	38	--	6
P-channel 20V/5V asymmetry MOSFET.	HVPMOS 20V	-1.1	125@5	-24	18	6
P-channel 20V/5V symmetry MOSFET.	HVPMOS 20V	-1.1	70@5	-24	18	6
40V/25V LDNMOSFET-(LS device).	LDMOS 40V	2.1	750@25	44	25	25
40V/25V LDNMOSFET-Isolated(HS device).	LDMOS 40V-Isolated	2.1	750@25	44	25	25
N-channel 40V/25V symmetric MOSFET(LS)	HVNMOS 40V	0.92	520@25	44	25	25
N-channel 40V/25V symmetric MOSFET(HS)	HVNMOS 40V-Isolated	0.92	520@25	44	25	25
40V/5V LDNMOSFET-(LS device).	LDMOS 40V	1	290@5	44	30	6
40V/5V LDNMOSFET-Isolated(HS device).	LDMOS 40V-Isolated	1	290@5	44	30	6
N-channel 40V/5V symmetric MOSFET(LS)	HVNMOS 40V	0.95	80@5	44	30	6
N-channel 40V/5V symmetric MOSFET(HS)	HVNMOS 40V-Isolated	0.95	80@5	44	30	6

Bipolar Transistor				
Device	Device Name	Beta	[BVCEO] [V]	[Max VCE] [V]
Parasitical vertical PNP	VPNP	4.8	20	6
Parasitical lateral PNP	LPNP	70	30	6
Parasitical Vertical NPN	VNPN	58	25	5
Vertical NPN with P-base (option)	VNPN	100	12	6
Capactior				
Device	Device Name	Area Cap [fF/um^2]	BV [V]	
Poly1/oxide/Poly2 capactior	PIP	1.02	14	
Poly1/ONO/Poly2 capacitor	ONO	1.2	25	
Diffusion capacitor (Poly/LV oxide/NW)	GOI/NW_5V	2	15	
Diffusion capacitor (Poly/LV oxide/PW)	GOI/PW_5V	2	-15	
Diffusion capacitor (Poly/Thin oxide/NW)	GOI/NW	1.5	20	
Diffusion capacitor (Poly/Thin oxide/PW)	GOI/PW	1.5	-20	
Diffusion capacitor (Poly/Thick oxide/NW)	GOI/NW	0.8	40	
Diffusion capacitor (Poly/Thick oxide/PW)	GOI/PW	0.8	-40	

CSMC Technologies Corporation
www.csmc.com.cn Tel:86-510-88118888 Fax:86-510-88115883
Headquarters: 8 Xinzhou Road, Wuxi,Jiangsu,China

Examples for measured and modeled parameter characteristics

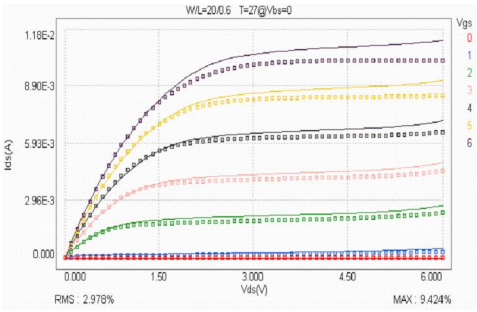


Figure1. NMOS W/L=20/0.6

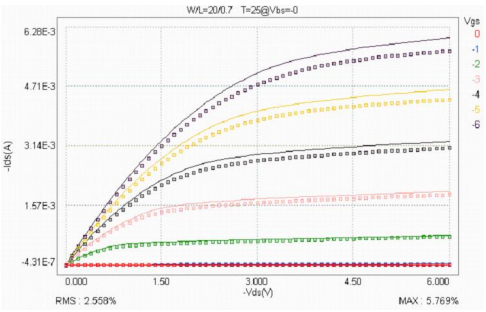


Figure2. PMOS W/L=20/0.7

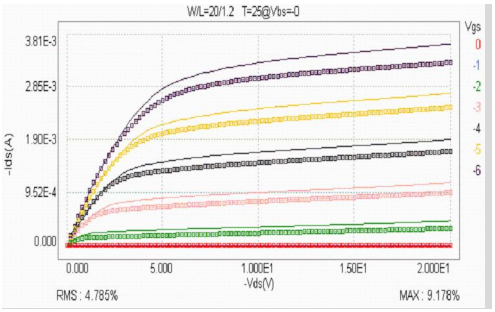


Figure3. 15VDMOS W/L=20/1.2

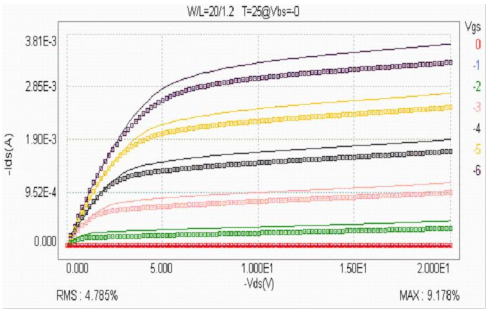


Figure4. 15VPMOS W/L=20/1.2

Process Design Handbook list

- ü Mask Tooling Information
- ü Electrical Design Rule
- ü PCM Specification
- ü ESD Protection Design Guideline
- ü Process Outline
- ü Process Design Kit